A 0.18-μm Monolithic Li-Ion Battery Charger for Wireless Devices Based on Partial Current Sensing and Adaptive Reference Voltage

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***Abstract*—An Li-ion battery charger based on a charge-control buck regulator operating at 2.2 MHz is implemented in 180 nm CMOS technology. The novelty of the proposed charge-control converter consists of regulating the average output current by only sensing a portion of the inductor current and using an adaptive reference voltage. By adopting this approach, the charger average output current is set to a constant value of 900 mA regardless of the battery voltage variation. In constant-voltage (CV) mode, a feedback loop is established in addition to the preexisting current control loop, preserving the smoothness of the output voltage at the transition from constant-current (CC) to CV mode. A small-signal model has been developed to analyze the system stability and subharmonic oscillations at low current levels. Transistor-level simulations of the proposed switching charger are presented. The output voltage ranges from 2.1 to 4.2 V, and the power efficiency at 900 mA has been measured to be 86% for an input voltage of 10 V. The accuracy of the output current using the proposed sensing technique is 9.4% at 10 V.**

***Index Terms*—Buck converter, charge control, current sensing, $G_{\rm M}C$ filter, LDMOS, Li-ion battery charger, power management unit, sample-and-hold system.**

I. Introduction

MODERN mobile phones are required to support increasingly faster CPUs, causing Li-ion batteries to get discharged at a higher rate. In order to replenish the Li-ion cells at the same rate as they deplete, a very effective technique preserving battery lifecycle must be employed. The most popular charging method for Li-Ion batteries, namely CC-CV charging technique [1], [2], implements constant-current charging up to 1 A when the battery voltage exceeds 2.1–2.5 V (CC mode), and gradually reduces the charging current as the cell voltage approaches 4.2 V (CV mode). Although charging at larger current levels helps the cell voltage reach its final value faster, a considerable voltage drop across the internal resistance of the battery (up to 300 mΩ) develops. The actual cell voltage, decremented by the resistive voltage drop, is therefore significantly low at the transition to CV mode. The CC-CV charging technique for wireless appliances relies on three power conversion topologies: low-dropout (LDO) voltage regulators [1]–[3], switch-mode power supplies (SMPSs) [4], and charge-pump converters [5]. Although LDOs can be fully integrated and have excellent stability performance, they are characterized by low-power efficiency at the beginning of the charge process. To remedy this problem, an adaptive reference voltage can be used to keep the difference between the dc power supply and the battery voltage within 150–300 mV during the whole charging process. This approach provides greater efficiency, even though a boosting switching supply is required to build the adaptive supply voltage of the LDO [2]. The efficiency of such a topology will still be lower than that of a single-stage switching charger. As with conventional LDOs, charge pump topologies exhibit low efficiency, which is emerging from research studies [4]. As far as battery chargers based on SMPSs are concerned, passive components such as inductors and capacitors cannot be integrated on-chip. The switching frequency thus needs to be increased in order to maintain low-profile components and reduce the printed circuit board (PCB) area. In this regard, the technological advancements in the field of integrated circuit design have enabled the development of power management applications in the megahertz range, motivating the research on new battery charger systems based on high-frequency switching converters.

Switch-mode power converters operating under average-current-mode control are attractive for battery charging, since the average output current of the charger determines the charging time of the Li-ion battery. One of the main issues encountered in this control topology is the need for sensing the inductor current. Although sensing resistors are suitable for this function, they contribute to a decrease of the power efficiency by 2%–10% when a current of 1 A is considered. A solution to this problem utilizes on-chip current-sensing transistors matched with the main power pMOS and nMOS switches [6], [9]. Using this method, both the pMOS and nMOS transistors' currents are sensed by two different sensing circuits and then summed together to create a scaled version of the inductor current. The main drawbacks associated with this approach are the increased design complexity and noise due to the switches commutation. To remedy this problem, an accurate and lossless self-learning sensing has been proposed in [6]. In this approach, the $G_{\rm M}$-C filter-based current-sensing circuit achieves high accuracy regardless of the inductor value. In addition, the inductor current is continuously sensed, thus avoiding the issues associated with the switching noise. Nevertheless, to implement the above technique the $G_{\rm M}$ cell needs to exhibit a linear characteristic over the differential input-voltage range $[V_{\rm IN}-V_{\rm OUT}, -V_{\rm OUT}]$

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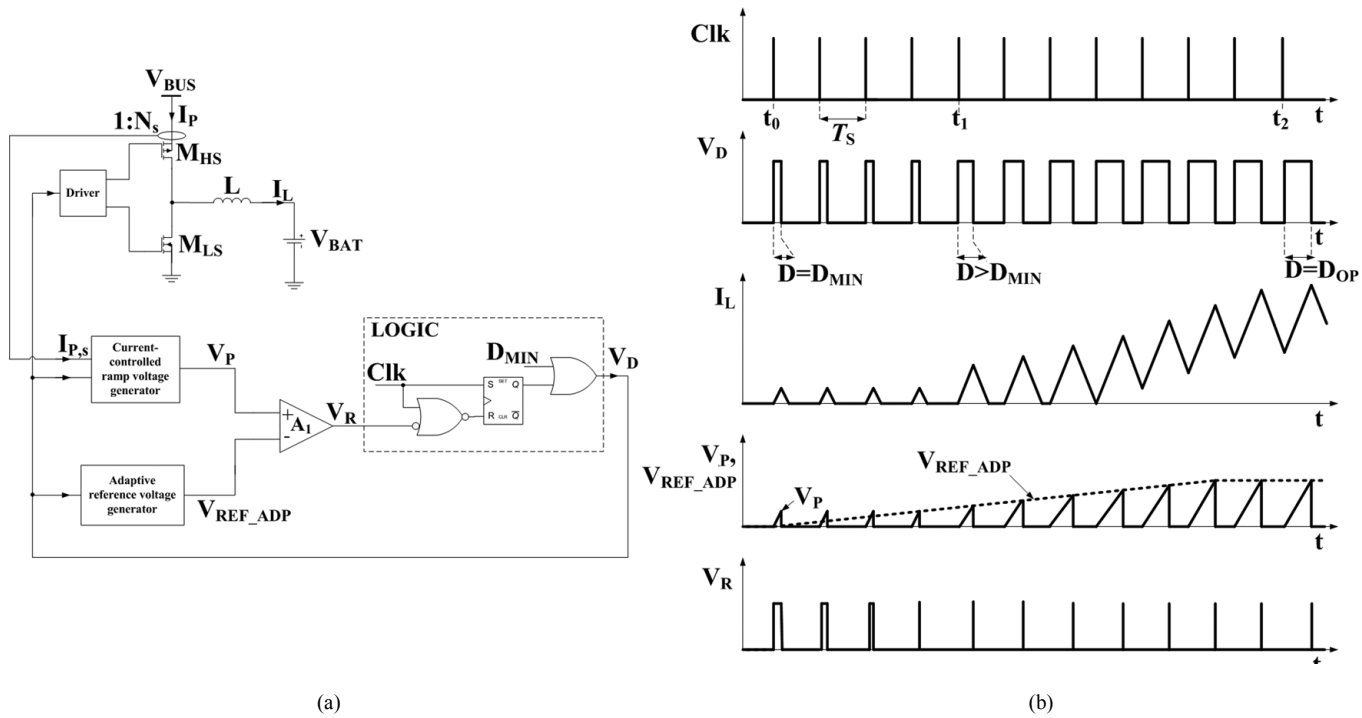


Fig. 1. (a) Conceptual schematic of the proposed charger in CC mode and (b) qualitative startup waveforms. N_S represents the mirroring ration of the current sensor. A logical NOR gate with one inverted input is used to prevent the SR flip-flop from entering the forbidden state. For simplicity, V_{REF_ADP} is considered to be a linear ramp, although implementation-wise it features a step-like characteristic.

(where V_{IN} and V_{OUT} are, respectively, the input and output voltage of the switching converter). As a result, the accuracy of the sensing circuit will be lower in wide input range dc–dc converters.

Another alternative to control the charger output current is to adopt a charge-control technique [7] with partial current measurement [8]. This control method combines the advantages of both peak-current and average-current control, based, respectively, on partial and full current sensing, while avoiding their respective shortcomings. In detail, by sensing the current of one switch, the true average of the inductor current is regulated just like in average-current control. But a simpler and more efficient sensing circuitry such as in peak-current control is required. However, since the above control method requires a fixed duty-cycle, no control of the average output current is possible over the entire range of the output voltage. To remove this limitation, we propose in this paper a control technique based on partial current sensing and adaptive reference voltage to regulate the output current of a switching-mode battery charger over the entire range of the output voltage. As explained in Section II, the partial current measurement is processed through a feed-forward control loop to accurately regulate the battery charging current. In Section III, the accuracy of the proposed architecture is analyzed, while a small-signal frequency-response model of the charge-control system is employed in Section IV to assess the stability of the control system. Additionally, a bifurcation analysis of the charger in CC and CV mode is presented in Section V. Section VI reports an experimental characterization of the 2.2-MHz battery charger prototype implemented in the 0.18-μm CMOS process. In conformity with Li-ion battery charging requirements, an average constant current of 900 mA was specified for constant-current charging when the battery voltage is higher than 2.1 V. Conclusions are drawn in Section VII.

II. Development of the Control Technique

In charge-control buck converters, the average output current is given by $\langle I_{OUT}\rangle = k_1 V_K/D$, where $\langle I_{OUT}\rangle$ is the average output current, k_1 is a constant determined by the controller parameters, V_K is a constant reference voltage, and D is the duty cycle [8]. As in battery-charging applications D linearly increases with the battery voltage,[1] one can deduce that $\langle I_{OUT}\rangle$ decreases with increasing duty cycle. Aiming at extending the applicability of a partial current-sensing technique to variable-duty cycle applications, a novel control strategy based on adaptive reference voltage is proposed. The proposed method prevents the variation of the battery voltage during the charging process from modifying the average output current.

A. Control Principle

The conceptual schematic of the switching charger in CC mode is presented in Fig. 1, along with its qualitative wave-

[1]This argument is based on the assumption that the charger operates in continuous conduction mode, where the well-known relationship $D = V_{BAT}/V_{BUS}$ holds (V_{BAT} and V_{BUS} are, respectively, the battery and bus voltage). In fact, the operating current of 900 mA is significantly above the boundary level between continuous and discontinuous conduction mode (= 250 mA at V_{BUS} = 10 V and V_{BAT} = 4.2 V, and 55 mA at V_{BUS} = 5 V and V_{BAT} = 4.2 V), thus confirming the above premise. It is worth noting that the proposed control technique is employed in CC mode to regulate the average output current. Thus, the relationship $D = V_{BAT}/V_{BUS}$, upon which the control method is based, is only required to hold in this mode. When the converter enters CV mode, the charging current eventually decreases below the CCM/DCM boundary and the relationship $D = V_{BAT}/V_{BUS}$ is not valid. Nevertheless, the control target here is the output voltage and the output current becomes variable.

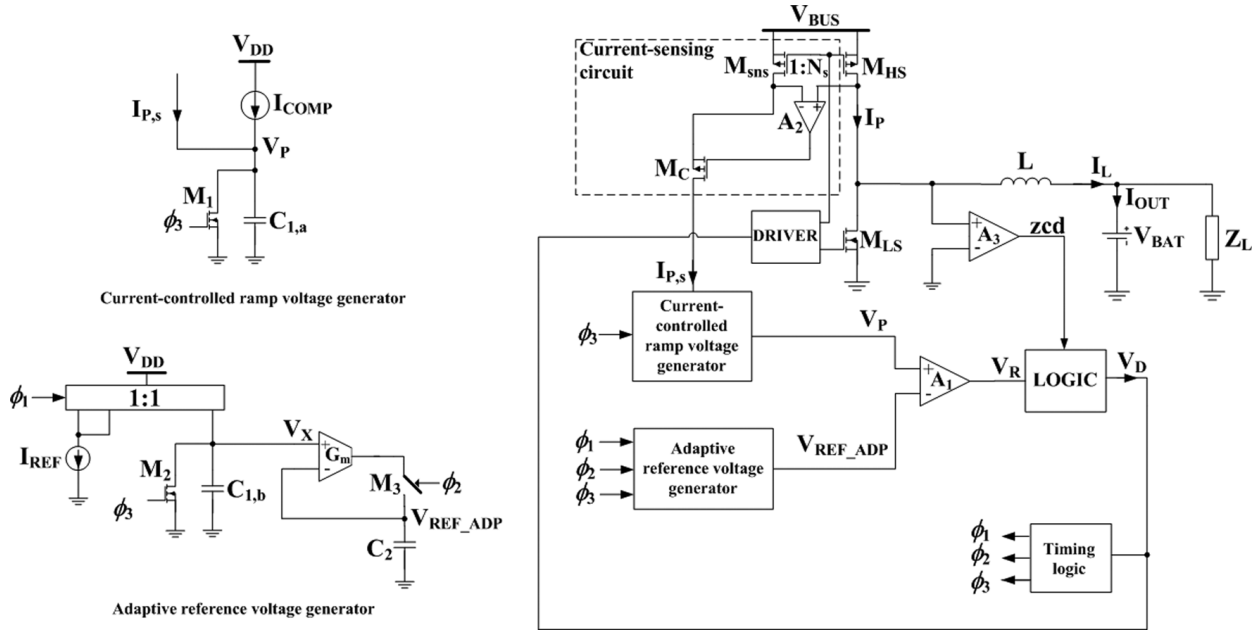


Fig. 2. Switching charger with partial current sensing in CC mode. Zero-current detection is performed by comparator A_3 to prevent the battery from being discharged during CV mode, when the converter enters discontinuous conduction mode. $Z_{\rm L}$ represents the input capacitors of circuits connected to the battery, i.e., switching regulators and LDOs, and a capacitor in parallel with the battery that prevents over-voltage at battery removal.

forms. A buck topology has been chosen to down-convert from an input range of [5 V, 10 V] to an output voltage range of [2.1 V, 4.2 V]. A negative-feedback current-control loop is implemented by sensing current $I_{\rm P}$, when $M_{\rm HS}$ is on, and integrating $I_{\rm P,s} = I_{\rm P}/N_{\rm S}$ to generate ramp voltage $V_{\rm P}$. The duty cycle is determined by comparing the latter with $V_{\rm REF\_ADP}$, which varies according to expression $V_{\rm REF\_ADP} = k_2 D\left(1-{\rm e}^{-(t/\tau)}\right)$, where k_2 is a constant and τ is the time constant of the reference voltage generator. At the beginning of CC mode, reference voltage $V_{\rm REF\_ADP}$ evolves in the following way.

- Assuming an initial battery voltage of 2.1 V, a 2.2-MHz clock signal is enabled at time t_0 to drive the logic circuit. A minimum duty-cycle pulse signal is forced to start up the system, the reason being that $V_{\rm P}$ and $V_{\rm REF\_ADP}$ are initially set to zero. As $V_{\rm D}$ goes high, $M_{\rm HS}$ is turned on hence supplying current $I_{\rm P,s}$ to the ramp voltage generator. Meanwhile, $V_{\rm REF\_ADP}$ starts increasing according to the expression $k_2 D_{\rm MIN}\left(1-{\rm e}^{-(t/\tau)}\right)$ since D is initially equal to $D_{\rm MIN}$ $(=0.01)$. After time interval $D_{\rm MIN}T_{\rm S}$ elapses, $M_{\rm HS}$ and $M_{\rm LS}$ are subsequently turned off and on, respectively, and $V_{\rm P}$ is pulled down to 0 V. The same operation repeats in the following switching cycles until $V_{\rm REF\_ADP}$ exceeds the peak value of $V_{\rm P}$.
- At time $t = t_1$, $M_{\rm HS}$ is turned on, and $V_{\rm P}$ reaches $V_{\rm REF\_ADP}$ after a time interval longer than $D_{\rm MIN}T_{\rm S}$. Consequently, the SR flip flop takes control over the duty cycle. Since D is larger than $D_{\rm MIN}$, both $I_{\rm L}$ and $V_{\rm REF\_ADP}$ will grow further. The same consideration applies in the next cycles. Eventually, when the DCM/CCM boundary is crossed, D sets to $D_{\rm OP} = V_{\rm BAT}/V_{\rm IN}$ and $V_{\rm REF\_ADP}$, now equal to $k_2 D_{\rm OP}\left(1-{\rm e}^{-(t/\tau)}\right)$, tends to its final value.
- At time $t = t_2$, $V_{\rm REF\_ADP}$ sets to $k_2 D_{\rm OP}$, hence limiting the peak value of $V_{\rm P}$. As the latter is proportional to the average inductor current $\langle I_{\rm L}\rangle$ and to the duty cycle (now constant), this means that current regulation has been achieved. When the battery voltage increases by effect of the charging current, $D_{\rm OP}$ will change as well, and $V_{\rm REF\_ADP}$ will tend to a new value to keep $\langle I_{\rm L}\rangle$ constant.

From the above discussion, we conclude that the proposed approach makes both $V_{\rm P}(DT_{\rm S})$ and $V_{\rm REF\_ADP}$ linearly proportional to D. So, the dependence of the average inductor current on the duty cycle, typical of charge-control converters with constant reference voltage, has been removed. This will be more evident in the following implementation analysis.

B. Development of the Control Technique in CC Mode

The accuracy of the charging current relies on the sensing circuitry providing $I_{\rm P,s}$, because the latter is fed back to the current-control loop. When a current-sensing transistor matched with $M_{\rm HS}$ ($M_{\rm sns}$ in Fig. 2) is employed, careful attention must be paid to the $V_{\rm DS}$ mismatch between the two transistor, since they both operate in the triode region [6], [9]. A $V_{\rm DS}$-matching control loop, realized by operational amplifier A_2 and MOSFET $M_{\rm C}$, is hence employed to produce an accurate scaled replica of $I_{\rm P}$. It should be noted that the ramp voltage generator supplied by $I_{\rm P,s}$ employs capacitor $C_{1,\rm a}$ to create ramp voltage $V_{\rm P}$. Accordingly, the current spike related to $I_{\rm P,s}$ is naturally filtered out, and the high-frequency content of $I_{\rm P,s}$ contributes negligibly to the generation of $V_{\rm P}$ [9].

Based on the above consideration, we assume the waveform profile of $I_{\rm P,s}$ shown in Fig. 3(a), where

$$\langle I_{\rm P,s}\rangle = \frac{D_{\rm n}}{N_{\rm S}}\langle I_{\rm OUT}\rangle . \tag{1}$$

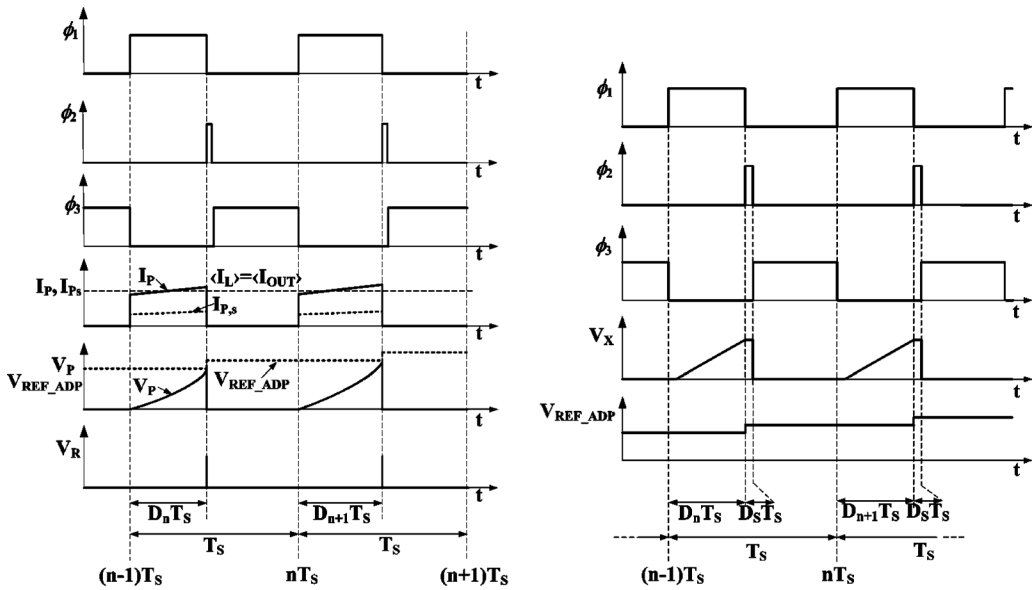


Fig. 3. (a) Qualitative waveforms of the charger in transient regime and (b) of the sample-and-hold circuit implementing the feed-forward control loop.

According to Figs. 2 and 3(a), when ϕ_3 is low, $I_{\mathrm{P,s}}$ is sourced into $C_{1,\mathrm{a}}$, leading to

$$V_{\mathrm{P}}(t) = \frac{1}{C_{1,\mathrm{a}}} \int_0^t (I_{\mathrm{P,s}} + I_{\mathrm{COMP}})\, \mathrm{d}t \tag{2}$$

where I_{COMP} is the ramp compensation current and $V_{\mathrm{P}}(t)$ is the control signal generated by the saw-tooth voltage generator. Using (1) and (2) (the latter being evaluated at $t = DT_{\mathrm{S}}$), and with the aid of Fig. 3(a), the following relationship can be obtained:

$$V_{\mathrm{REF\_ADP}}\,(D_{\mathrm{n}}T_{\mathrm{S}}) = \frac{\langle I_{\mathrm{OUT}}\rangle}{N_{\mathrm{S}}C_{1,\mathrm{a}}} D_{\mathrm{n}}T_{\mathrm{S}} + \frac{I_{\mathrm{COMP}}}{C_{1,\mathrm{a}}} D_{\mathrm{n}}T_{\mathrm{S}} \tag{3}$$

where D_{n} is the duty cycle relative to the nth switching cycle and T_{S} is the switching period. Equation (3) states that, to keep $\langle I_{\mathrm{OUT}}\rangle$ constant during charging, we need to make $V_{\mathrm{REF\_ADP}}$ linearly proportional to the duty cycle. Accordingly, our reference voltage $V_{\mathrm{REF\_ADP}}$ is a variable quantity in the proposed control approach.

The circuital implementation of the adaptive reference voltage generator in Fig. 2 is described by inspecting the corresponding operating waveforms in Fig. 3(b). In every switching cycle, V_{X} is ramped from zero up to

$$V_{\mathrm{X}}(D_{\mathrm{n}}T_{\mathrm{S}}) = \frac{I_{\mathrm{REF}}}{C_{1,\mathrm{b}}} D_{\mathrm{n}}T_{\mathrm{S}} \tag{4}$$

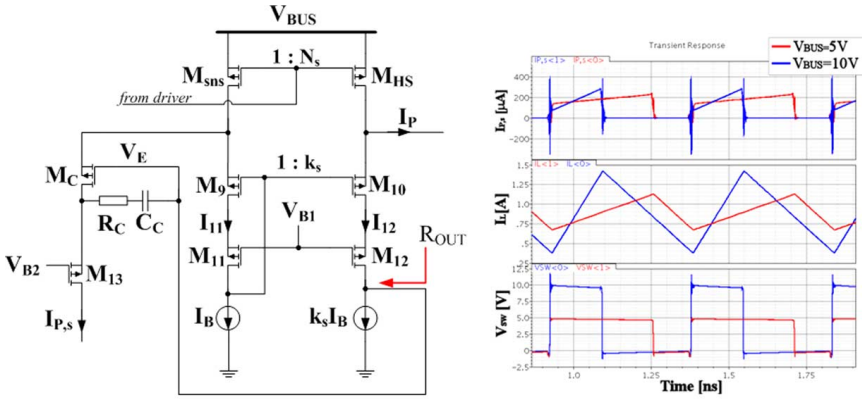
where I_{REF} is a constant reference current. Next, the G_{m} cell is configured as a buffer, thus sampling $V_{\mathrm{X}}(D_{\mathrm{n}}T_{\mathrm{S}})$ during interval $D_{\mathrm{S}}T_{\mathrm{S}}$. $C_{1,\mathrm{b}}$ is then discharged to ground via M_2, while C_2 holds the value of $V_{\mathrm{X}}(D_{\mathrm{n}}T_{\mathrm{S}})$ previously sampled. In conclusion, assuming $C_{1,\mathrm{a}} = C_{1,\mathrm{b}} = C_1$, (3) and (4) lead to the following expression:

$$\langle I_{\mathrm{OUT}}\rangle = N_{\mathrm{S}}\,(I_{\mathrm{REF}} - I_{\mathrm{COMP}})\,. \tag{5}$$

From (5), it is evident that the proposed control concept yields an average output current which is linearly proportional to the difference between reference current I_{REF} and slope compensation current I_{COMP}. It should be observed that (5) has been derived by assuming that $V_{\mathrm{REF\_ADP}}$ has reached its steady-state value as depicted in Fig. 1(b). The time constant of $V_{\mathrm{REF\_ADP}}$ specified in our design is about 0.5 ms, which is relatively low in comparison with the battery-charging time.

III. Accuracy of the Proposed Charger

Since the sensing circuitry of the switching charger is simplified using a feed-forward control mechanism, it is necessary to assess the accuracy performance of the proposed architecture. First, the detailed current-sensing circuit adopted in the proposed charger is shown in Fig. 4(a). A cascode current mirror is adopted to increase the loop gain of the state-of-the-art current sensor to 60 dB [10]. In addition, an *RC* compensation network is applied to achieve a worst-case phase margin of 60 degrees across process–voltage–temperature (PVT) corners, because a second-pole effect is significant near the unitary-gain bandwidth of 40 MHz (typical value). Such a bandwidth is adequate for an operating switching frequency of 2.2 MHz as shown by transistor-level simulations in Fig. 4(b). The sensing currents at $V_{\mathrm{BUS}} = 5$ V and $V_{\mathrm{BUS}} = 10$ V have different slopes because the inductor current ripple is related to the bus voltage. However, according to our expectations, the average value (nominally 900 mA) does not change except for a deviation related to propagation delay (see Section III-B). This means that the average output current of the charger is now independent of the duty cycle. Bonding-wire parasitics extracted through a 3-D field simulator have been included in the above simulations to



(a) (b)

Fig. 4. (a) Current sensing circuit and (b) simulation results in the 0.18-μm process.

show the intrinsic immunity of the control circuit against spurious signals.

A. Random Variation of the Charging Current

The accuracy of the battery current in CC mode can be estimated by resorting to the simplified battery charger model in Fig. 5. As shown, equivalent voltage sources have been employed to represent the voltages across $C_{1,\mathrm{a}}$ and $C_{1,\mathrm{b}}$. Inherently to the sample-and-hold characteristic and slow-scale dynamics of the adaptive reference voltage generator, we have depicted this block as a buffer with a low-frequency pole. The reason for including this block in our model is that clock frequency fluctuations present at its input are filtered out. Accordingly, in this picture, $T_{\mathrm{S,f}}$ denotes the switching period in absence of short-term time variations such as clock jitter. This implies that the voltage comparison at the input of comparator A_1 does not reject short-term jitter but it does cancel long-term variations out of the switching period. The input-referred offsets of comparator A_1 and G_{M} cell, are represented by $V_{\mathrm{OFF},1}$ and $V_{\mathrm{OFF},2}$, respectively. The other terms degrading the accuracy of $\langle I_{\mathrm{OUT}}\rangle$, namely $\sigma_{\langle I_{\mathrm{OUT}}\rangle}$, are the reference and compensation current standard deviations ($\sigma_{I_{\mathrm{REF}}}$ and $\sigma_{I_{\mathrm{COMP}}}$, respectively) and capacitor mismatch $\sigma_{\mathrm{C_1}}$.

The following theoretical analysis is now performed. First, the two input voltages of A_1 are equated to derive a relationship between $\langle I_{\mathrm{OUT}}\rangle$ and the quantities indicated in Fig. 5. Next, a first-order perturbation is applied to I_{REF}, I_{COMP}, $C_{1,\mathrm{a-b}}$, T_{S}, and their contribution to $\sigma_{\langle I_{\mathrm{OUT}}\rangle}$ is determined. Finally, all error terms are summed according to a square-law model, as a normal distribution is considered, and we obtain (6), shown at the bottom of the page.

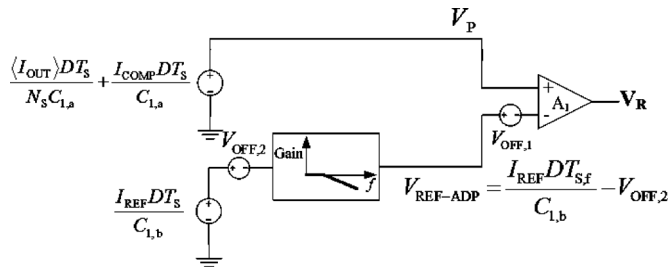


Fig. 5. Simplified model of the battery charger for error analysis in CC mode.

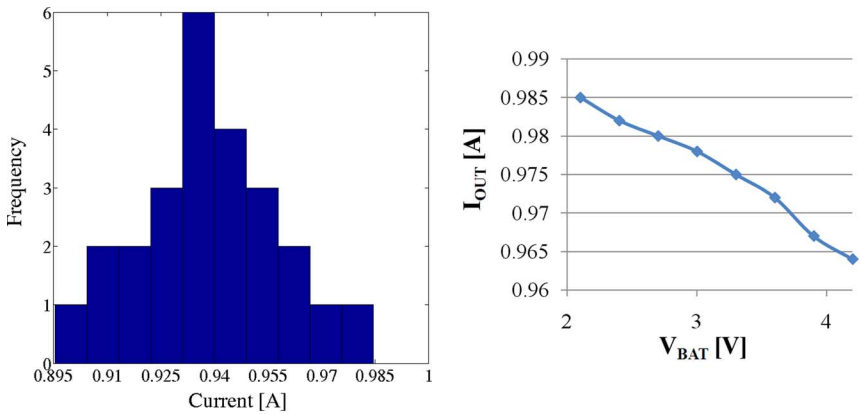
The following considerations, which are worth mentioning, can be drawn.

- The influence of $V_{\mathrm{OFF},1}$ and $V_{\mathrm{OFF},2}$ on $\sigma_{\langle I_{\mathrm{OUT}}\rangle}$ increases with N_{S} and C_1. As a matter fact, the amplitudes of V_{P} and $V_{\mathrm{REF\_ADP}}$ are inversely proportional to such parameters. In addition, at the beginning of the battery charging process, where D is at its minimum value, the degradation of $\langle I_{\mathrm{OUT}}\rangle$ by $V_{\mathrm{OFF},1}/V_{\mathrm{OFF},2}$ is worst.
- Capacitor mismatch can significantly affect the accuracy of the charging current, unless values larger than 10 pF are chosen and careful device layout is realized.
- Short-term jitter effects are remarkable at very high switching frequencies, hence calling for an optimized PLL (phase-locked loop) design. Nevertheless, in the present design, clock jitter amounts to 1.2 ns, and, since the switching frequency is 2.2 MHz, the term $N_{\mathrm{S}}I_{\mathrm{REF}}/T_{\mathrm{S}}\sigma_{T_{\mathrm{S}}}$ in (6) can be neglected.

B. Propagation Delay t_{D}

The propagation delay related to the control loop must be also taken into consideration because this prolongs the charge time

$$\sigma_{\langle I_{\mathrm{OUT}}\rangle} = \sqrt{N_{\mathrm{S}}^2\left(\sigma_{I_{\mathrm{REF}}}^2+\sigma_{I_{\mathrm{COMP}}}^2\right)+\left(\frac{I_{\mathrm{OUT}}}{N_{\mathrm{S}}}\right)^2\sigma_{N_{\mathrm{S}}}^2+\left(\frac{N_{\mathrm{S}}I_{\mathrm{REF}}}{C_1}\right)^2\sigma_{\mathrm{C_1}}^2+\left(\frac{N_{\mathrm{S}}I_{\mathrm{REF}}}{T_{\mathrm{S}}}\right)^2\sigma_{T_{\mathrm{S}}}^2+\left(\frac{N_{\mathrm{S}}C_1}{DT_{\mathrm{S}}}\right)^2(V_{\mathrm{OFF},1}+V_{\mathrm{OFF},2})} \quad (6)$$



(a) (b)

Fig. 6. (a) Statistical measurement of the average output current. $V_{\rm BUS} = 10$ V, $V_{\rm BAT} = 2.1$ V. (b) Variation of the output current across the battery voltage range ($V_{\rm BUS} = 10$ V).

of capacitors $C_{1,\rm a}$ and $C_{1,\rm b}$. Most of the propagation delay is attributed to comparator A_1 in Fig. 2. Accordingly, the quiescent current of the comparator needs to be increased in order to achieve higher speed. Unfortunately, power consumption is a stringent requirement in mobile platforms and consequently a different strategy must be adopted.

The propagation delay affects both the inductor current ripple and the adaptive reference voltage amplitude. The increase of the inductor current ripple due to $t_{\rm D}$ amounts to $((V_{\rm BUS} - V_{\rm BAT})/L)t_{\rm D}$, which needs to be halved to get the battery current error in the average sense. The resulting quantity represents the first term of the output current error. Next, the adaptive reference voltage generator is considered. Ideally ($t_{\rm D} = 0$), $V_{\rm REF\_ADP}$ is proportional to $DT_{\rm S}$. However, as $t_{\rm D}$ becomes significant, the effective integration time of $I_{\rm REF}$ in Fig. 2 is $DT_{\rm S} + t_{\rm D}$. Recalling the working principle of the reference voltage generator, this translates into a positive offset causing $V_{\rm REF\_ADP}$ to be

$$V_{\rm REF\_ADP} = \frac{I_{\rm REF}}{C_{1,\rm b}} \left(D_{\rm n} T_{\rm S} + t_{\rm D}\right). \tag{7}$$

$V_{\rm REF\_ADP}$ has thus accumulated an offset equal to $I_{\rm REF} t_{\rm D}/C_{1,\rm b}$ causing $V_{\rm P}(D\,T_{\rm S})$ to grow by the same quantity. Based on the theoretical analysis presented in Section II-B, the second term degrading the accuracy of $I_{\rm OUT}$ can be derived by equating (7) and $V_{\rm P}(D\,T_{\rm S})$. The total variation of $\langle I_{\rm OUT}\rangle$ is therefore

$$\Delta\langle I_{\rm OUT}\rangle = \frac{V_{\rm BUS} - V_{\rm BAT}}{2L} t_{\rm D} + N_{\rm S} I_{\rm REF} \frac{t_{\rm D}}{DT_{\rm S}}. \tag{8}$$

The left-hand error contribution is typical of average-current control architectures based on partial current sensing, while the right-hand one belongs to the proposed control technique. The latter can be linearly compensated by employing a blanking-time generator, which delays ramp voltage $V_{\rm X}$ by $t_{\rm D}$ and hence causes its peak value to decrease by $I_{\rm REF} t_{\rm D}/C_{1,\rm b}$. Accordingly, the right-hand error term in (8) can be fully removed. It should be noticed that the delay time associated with the driver stage exhibits a dependence on the bus voltage. However, since such a delay (2.2 ns, max.) is lower than the total propagation delay (12.5 ns), the influence of the bus voltage can be neglected.

C. Experimental Results

As the profile of the output inductor can sometimes be a stringent constraint in the design of a PMU, in this work we consider a multilayer inductor. The latter is known for its worst saturation characteristic compared to a wire-wound inductor. For instance, a typical multilayer inductor ($L = 4.7$ μH, rated current $=$ 1.1 A) saturates to 1 μH at 900 mA. As this represents the worst-case scenario, the charger has been analyzed under this condition. The error due to the current ripple has been estimated to be 4.4%, at $V_{\rm BUS} = 10$ V and $V_{\rm BAT} = 2.1$ V, when a multilayer inductor is used and reduces to nearly 1% in case of a wire-wound inductor. The 1σ standard deviation of the output current is estimated by (6) and multiplied by 3 to get a total random error of 58.5 mA (3σ value) or 6.5% in terms of relative error. Eventually, by linearly summing the 4.4% deterministic error to the above estimated error, the worst-case accuracy of the proposed architecture ends up being 10.9%. In Fig. 6(a), a statistical measurement of the average output current over 25 samples is shown. The average value of the distribution is 0.94 A because of the deterministic error, while the total standard deviation (intended as 3σ value) amounts to 45 mA. As a result, the measured total error is 9.4%, which is in agreement with the 10.9% error previously estimated. Based on Fig. 6(b), the variation of the output current across the battery voltage range is 2.2%. In this test, the sample exhibiting the largest current deviation, in accordance with Fig. 6(a), has been considered.

From the above analysis, it emerges that the battery charger architecture proposed in this paper exhibits a very good accuracy performance in wide-input voltage range applications such as wall ac adaptors. It should be reminded that in the previous estimation we have addressed the issue of the inductor saturation. Although no relationship exists between this phenomenon and the propagation delay, their combined effect provokes the left-hand term in (8), that is, if $t_{\rm D}$ were zero, L would not play a role in the accuracy performance of the average output current,

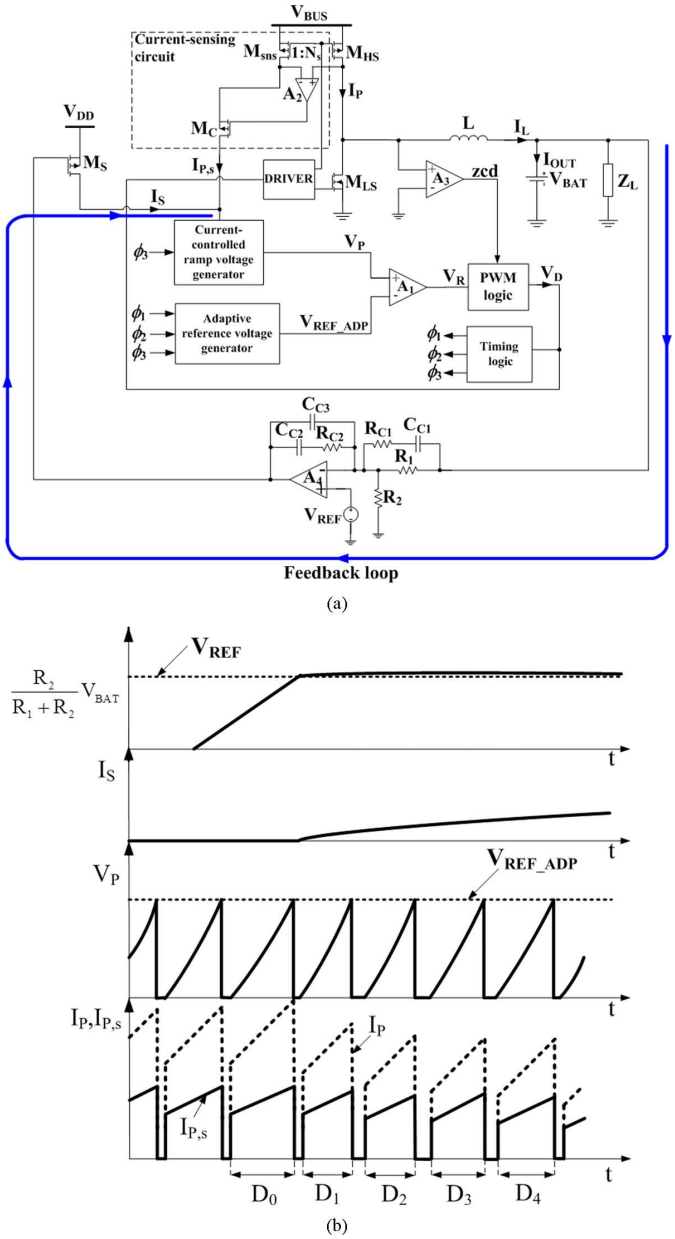


Fig. 7. (a) Circuital diagram of the switching charger with constant-voltage loop. (b) Qualitative waveforms at the CC/CV transition.

even if the inductor were strongly saturated. But when $t_{\rm D}$ is finite, the average output current is dependent on L, and is therefore sensitive to inductor saturation. It should also be mentioned that in this paper a 10-V wall ac adaptor application has been explored, which has been shown to represent the worst condition for output current accuracy.

IV. Stability Analysis at the CC/CV Boundary

The battery voltage accuracy at the CC-CV boundary is a critical aspect in the design of a battery charger, as a current-regulated feedback loop transitions to a voltage-regulated feedback loop. If the transition from CC to CV mode is not smooth, the battery voltage can significantly exceed its float level (= 4.2 V), thus affecting Li-ion capacity and cycle-life. A stability analysis

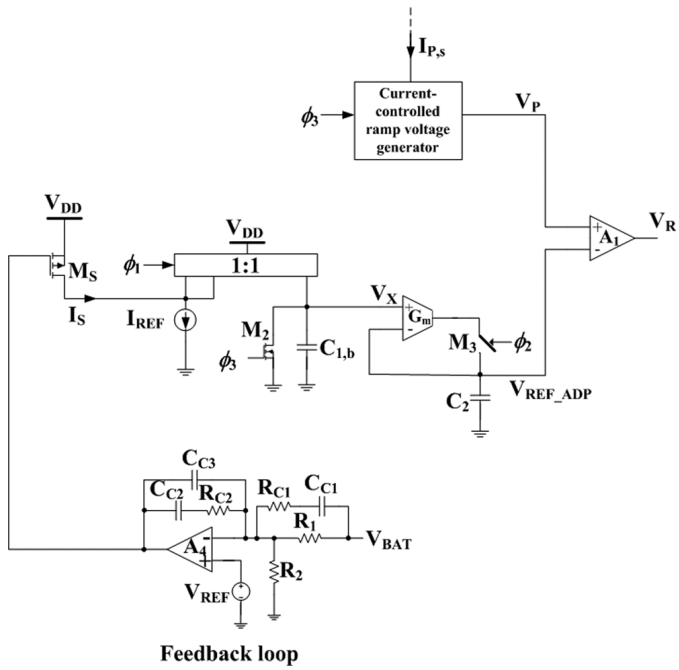


Fig. 8. Alternative voltage-control loop modulating $V_{\rm REF\_ADP}$.

conducted by a small-signal ac model is therefore presented. Emphasis is given on the interaction between the CC and CV control loops, which occurs when both loops are active.

The implementation of the CV control loop is shown in Fig. 7(a), while the pertaining waveforms at the CC/CV transition are illustrated in Fig. 7(b). When $V_{\rm BAT}$, opportunely scaled, exceeds reference voltage $V_{\rm REF}$, the voltage error at the output of the type-III compensating network causes $I_{\rm S}$ to increase from zero. Since $dV_{\rm P}/{\rm d}t$ is proportional to $I_{\rm S}+\langle I_{\rm P,s}\rangle$, the effect of increasing $I_{\rm S}$ is to make $V_{\rm P}$ steeper. Whereas $V_{\rm REF\_ADP}$ is a slowly varying signal, D decreases and $\langle I_{\rm P}\rangle$ starts reducing. In accordance with this, sensing current $\langle I_{\rm P,s}\rangle$ follows the same trend as $\langle I_{\rm P}\rangle$ and further diminishes while $I_{\rm S}$ grows. It should be noted that the charging current decay is so slow that the above perturbations are hardly visible over a short time window. Thus, Fig. 7(b) just gives a qualitative trend description of the system dynamics in CV mode. Apart from small perturbations, D can thus be considered constant to $V_{\rm FL}/V_{\rm BUS}$ (as long as the converter operates in CCM), because the voltage control loop imposes $V_{\rm BAT}=V_{\rm FL}=(R_1+R_2)/R_2V_{\rm REF}$. This also requires $dV_{\rm P}/{\rm d}t$ to be nearly constant, because the intersection of $V_{\rm P}$ with $V_{\rm REF\_ADP}$ defines the duty cycle. It is then implied that $I_{\rm S}+\langle I_{\rm P,s}\rangle$ does not change throughout the current decay process. In conclusion, $I_{\rm S}$ and $\langle I_{\rm P,s}\rangle$ vary by the same amount but in opposite directions.

Based on the above analysis, the voltage and current control loops operate at the same time. However, the strategy of reducing $\langle I_{\rm OUT}\rangle$ by increasing $I_{\rm S}$ (voltage-control variable) allows the voltage feedback loop over-ruling the current control loop. This is, de facto, equivalent to reduce reference current $I_{\rm REF}$ of the adaptive reference voltage generator and force $\langle I_{\rm P,s}\rangle$ to track it (see Fig. 8). Unfortunately, due to the poor dynamics of the adaptive reference voltage, this optional implementation would considerably slow down the system response.

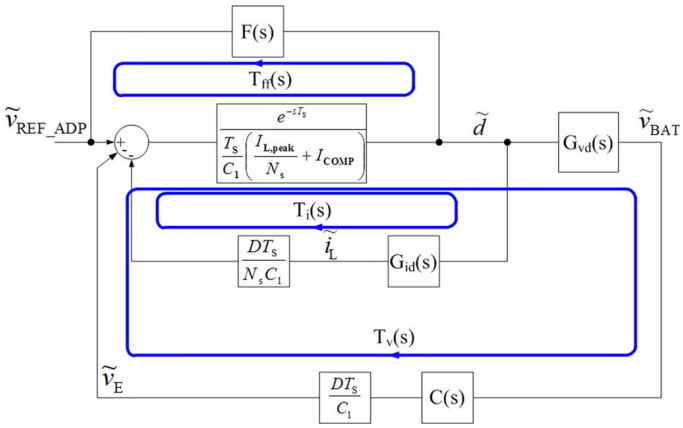


Fig. 9. Complete small-signal model of the charger with indication of the low-frequency feed-forward loop.

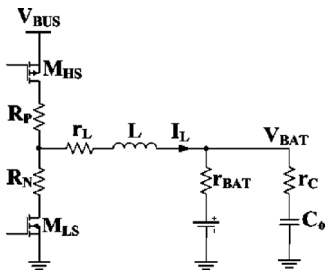


Fig. 10. Indication of the parasitic components of the switching converter.

A. Modeling of the Adaptive Reference Voltage Generator

The dynamics of the adaptive reference voltage can be expressed by the following equation (see the Appendix):

$$\frac{d\langle v_{\mathrm{REF\_ADP}}\rangle}{\mathrm{d}t} = \frac{G_{\mathrm{m}} I_{\mathrm{REF}} D_{\mathrm{S}} T_{\mathrm{S}}}{C_1 C_2} d - \frac{D_{\mathrm{S}} G_{\mathrm{m}}}{C_2} \langle v_{\mathrm{REF\_ADP}}\rangle \tag{9}$$

which provides the transfer function

$$\begin{aligned} F(s) &= \frac{v_{\mathrm{REF\_ADP}}(s)}{d(s)} = \frac{V_0}{1+\frac{s}{\omega_{\mathrm{p}}}} \\ V_0 &= \frac{I_{\mathrm{REF}} T_{\mathrm{S}}}{C_1} \\ \omega_{\mathrm{p}} &= \frac{D_{\mathrm{S}} G_{\mathrm{m}}}{C_2}. \end{aligned} \tag{10}$$

As previously discussed, the circuit under analysis hence behaves as a single-pole system having a -3 dB bandwidth ω_{p}. Accordingly, the dynamics of the adaptive reference voltage and, thus, the startup behavior of the charger can be controlled by the parameters of the SH circuit, i.e., G_{m}, C_2 and D_{s}. The location of this pole must be at lower frequency in order to avoid interactions with the current feedback loop, i.e., $\omega_{\mathrm{p}}/2\pi < f_{\mathrm{ci}}/10$, where f_{ci} is the cross-over frequency of the current loop gain.

B. Loop Gain

The small-signal behavior of the charging system is analyzed by considering the schematic in Fig. 9 (see the Appendix). The transfer functions of the plant, namely G_{vd} and G_{id}, have been derived by resorting to classical modeling methods and are reported in Table I. The transfer function of the compensating network has been denoted as $C(s)$. The meaning of the parameters in Table I not previously explained can be inferred by considering the schematic of the power stage in Fig. 10, where r_{BAT} represents the ESR of the Li-ion battery, r_{C} is the equivalent resistance of the parallel capacitor C_{o} and $G_{\mathrm{m,S}}$ is the transconductance gain of M_{S}.

TABLE I
TRANSFER FUNCTIONS OF THE SMALL-SIGNAL MODEL.

Control-to-output-voltage transfer function	$G_{\mathrm{vd}} = V^{\bullet}_{\mathrm{BUS}} \dfrac{1+sr_{\mathrm{C}}C_{\mathrm{o}}}{\Delta(s)}$
Control-to-output-current transfer function	$G_{\mathrm{id}} = \dfrac{V^{\bullet}_{\mathrm{BUS}}}{r_{\mathrm{BAT}}} \dfrac{1+sr_{\mathrm{BAT}}C_{\mathrm{o}}}{\Delta(s)}$
Compensation transfer function	$C = -\dfrac{G_{\mathrm{m,S}}}{R_1(C_{\mathrm{C2}}+C_{\mathrm{C3}})} \bullet \dfrac{(1+s(R_1+R_{\mathrm{C1}})C_{\mathrm{C1}})(1+sR_{\mathrm{C2}}C_{\mathrm{C2}})}{s(1+sR_{\mathrm{C1}}C_{\mathrm{C1}})(1+sR_{\mathrm{C2}}C_{\mathrm{eq}})}$
Parameters of the transfer functions	$\Delta(s) = 1+\dfrac{r_{\mathrm{eq}}}{r_{\mathrm{BAT}}}+s\left(\dfrac{L}{r_{\mathrm{BAT}}}+r_{\mathrm{eq}}C_{\mathrm{o}}\right)+s^2LC_{\mathrm{o}}$, $V^{\bullet}_{\mathrm{BUS}} = V_{\mathrm{BUS}} - (R_{\mathrm{P}}-R_{\mathrm{N}})I_{\mathrm{L}}$, $r_{\mathrm{eq}} = r_{\mathrm{L}} + DR_{\mathrm{P}} + (1-D)R_{\mathrm{N}}$, $C_{\mathrm{eq}} = \dfrac{C_{\mathrm{C2}}C_{\mathrm{C3}}}{C_{\mathrm{C2}}+C_{\mathrm{C3}}}$

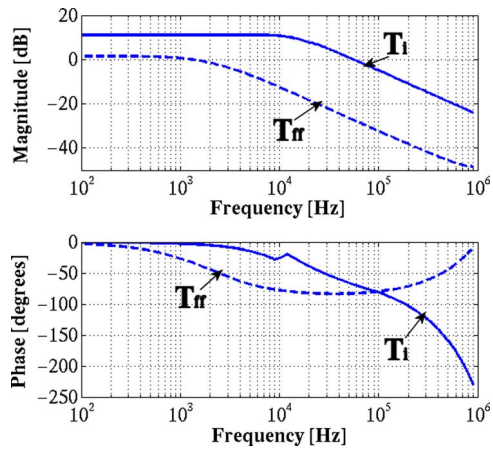


Fig. 11. Simulation results concerning the current-loop transfer function (solid line) and feed-forward loop transfer function (dashed line).

The system under study exhibits a feedback current control loop having transfer function T_{i} and a feedback voltage control loop with transfer function T_{v}. In addition, a feed-forward control loop with transfer function T_{ff} is created, as previously discussed, by the adaptive reference voltage generator. Concerning the effects of this control mechanism on the system stability, it can be noticed by the open-loop transfer function

$$T_{\mathrm{OL}} = \frac{T_{\mathrm{v}}}{1+T_{\mathrm{i}}-T_{\mathrm{ff}}} \tag{11}$$

that T_{ff} subtracts from T_{i}. As T_{ff} is only significant in the low-frequency region, the high frequency dynamics of the converter is not affected by the feed-forward control loop. Accordingly, the stability of the proposed architecture is not compromised by the additional control loop. In Fig. 11, Bode plots of the above transfer functions are shown to confirm this observation. The

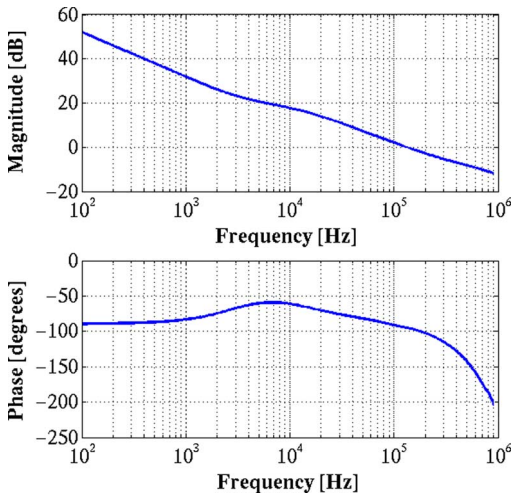


Fig. 12. Simulation results concerning the open-loop transfer function.

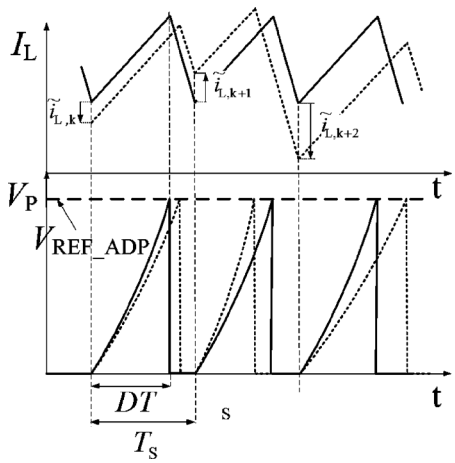


Fig. 13. Qualitative waveforms of the proposed charger at low $\langle I_{\rm OUT}\rangle$. Solid lines: unperturbed waveforms, dashed lines: perturbed waveforms.

-3 dB bandwidth of the feed-forward control loop is lower than that of the feedback current control loop. In addition, the magnitude of $T_{\rm ff}$ is much lower than that of $T_{\rm i}$. Therefore, only the dc regulation of the system is corrected to achieve the desired average output current. The typical Bode plot of the open-loop transfer function $T_{\rm OL}$ is reported in Fig. 12, where it is apparent that the system features good stability performance at the CC-CV transition. As the CC control loop is over-ruled without causing abrupt variations of the control signal, we will show the battery voltage to reach its float level in a smooth way.

V. Bifurcation Analysis

Because charge-control converters are prone to subharmonic oscillations at low current levels, it is necessary to adopt ramp compensation to prevent erratic system behavior. The origin of subharmonic oscillations can be easily explained by referring to the charger waveforms in Fig. 13. In this diagram, the charger is considered to be operating at low current, but still in continuous conduction mode (CCM). The effect of a low $\langle I_{\rm OUT}\rangle$ and large D is to reduce the slope of ramp $V_{\rm P}$ and increase the on-time of the converter. We hence notice that $I_{\rm L}$ is steeper during the off-time. Let now a small-signal perturbation, namely $\tilde{i}_{\rm L,k}$, be applied to the inductor current at the beginning of the first switching cycle. Such a perturbation propagates throughout the time interval $DT_{\rm S}$ and grows up to $\tilde{i}_{\rm L,k+1}$ when the inductor current changes slope. Such a perturbation has reverse polarity but higher amplitude than $\tilde{i}_{\rm L,k}$. At the end of the second switching cycle, the inductor current perturbation $\tilde{i}_{\rm L,k+2}$ is even larger, indicating that system has entered a local instability regime eventually culminating in a $2T$-periodic motion (T is the period of the orbit under standard operating conditions) [11], [12]. It should be noticed that, in Fig. 13, we have assumed the converter to be operating in continuous conduction mode, implying that the origin of subharmonic oscillation has not to be attributed to the transition to discontinuous conduction mode. Whereas the charger operating conditions are different in CC and CV mode, a bifurcation analysis will now be conducted in both cases. Besides, the alternative implementation of voltage-control loop shown in Fig. 8 will be investigated to show its additional disadvantages with reference to the current study.

A. Proposed Control Mechanism in CC Mode

To determine the operating point where the converter undergoes the phenomenon of flip bifurcation, the following analysis is performed. According to Fig. 7(a), $I_{\rm S}$ is zero since our analysis is focused on CC mode. Assuming that the adaptive reference voltage varies slowly in comparison with the inductor current, $V_{\rm REF\_ADP}$ can be considered constant over several switching cycles. By perturbing the inductor current and the duty cycle, the following equation can be written (see Fig. 14):

$$\frac{1}{N_{\rm S}C_1}\int_{T_{\rm S,k-1}}^{\left(D_{\rm k}+\tilde{d}_{\rm k}\right)T_{\rm S}+T_{\rm S,k-1}}\left(I_{\rm L}(t)+\tilde{i}_{\rm L,k-1}\right)\,{\rm d}t = V_{\rm REF\_ADP}. \tag{12}$$

Neglecting constant- and second-order terms in the previous equation, the following relationship can be easily derived:

$$\tilde{d}_{\rm k} = -\frac{D_{\rm k}}{I_{\rm L,peak}}\tilde{i}_{\rm L,k-1}. \tag{13}$$

Assuming a constant duty cycle in k switching cycles, i.e., $D_{\rm k} = D_{\rm k-1} = \cdots = D_0 = D$, after iterating, we finally obtain [13]

$$\tilde{i}_{\rm L,k} = \left(1-(m_1-m_2)\frac{DT_{\rm S}}{I_{\rm L,peak}}\right)^{\rm k}\tilde{i}_{\rm L,0} \tag{14}$$

where

$$m_1 = \frac{V_{\rm BUS}-V_{\rm BAT}}{L} \tag{15}$$

$$m_2 = -\frac{V_{\rm BAT}}{L}. \tag{16}$$

For $\tilde{i}_{\rm L,k}$ to vanish, it is necessary that the argument within brackets in (14) be less than one. The constraint on the output current and duty cycle, guaranteeing subharmonic-free operation, is thus obtained:

$$\langle I_{\rm OUT}\rangle > \frac{V_{\rm BUS}}{2L}D^2T_{\rm S}. \tag{17}$$

In the $\langle I_{\rm OUT}\rangle$-$D$ state plane, this equation describes a parabola which delimits the domain of instability of the switching

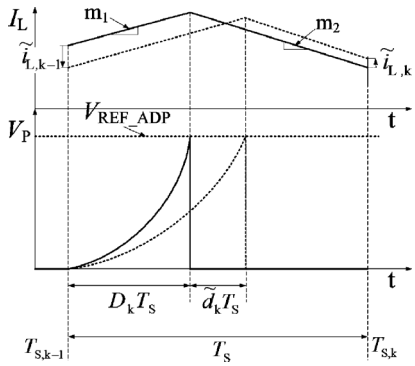


Fig. 14. Perturbed waveforms of the charge-control buck converter.

charger. Depending on the design specifications, $\langle I_{\rm OUT}\rangle$ and D may cross the region of instability to satisfy the current-control law. For instance, in CC mode, $\langle I_{\rm OUT}\rangle$ is fixed and D is variable. At the battery voltage approaching $V_{\rm FL}$, a large duty cycle is needed for current regulation. If the charging current setting is low, the condition expressed by (17) might be violated and subharmonic oscillation subsequently occurs. It is worth noting that period-doubling is not recorded in the current application during CC mode, because the battery charging current is 900 mA. However, if a lower charging current is demanded, appropriate measures must be taken remove the region of instability from the operating range of the charger. To this aim, ramp compensation is a very straightforward technique which is easily realizable by injecting current $I_{\rm COMP}$ into capacitor C_1. Though its simplicity, it allows to extend the region of stability of the charger to its full operating range.

To determine the value of the ramp slope, we can rewrite (13) as

$$\widetilde{d}_{\rm k} = -\frac{D_{\rm k}}{I_{\rm L,peak} + m_{\rm C}N_{\rm S}C_1}\widetilde{i}_{\rm L,k-1} \tag{18}$$

where $m_{\rm C} = I_{\rm COMP}/C_1$. The condition for stability then becomes

$$\frac{\langle I_{\rm OUT}\rangle}{N_{\rm S}} + m_{\rm C}C_1 > \frac{V_{\rm BUS}}{2LN_{\rm S}}D^2T_{\rm S}. \tag{19}$$

By imposing

$$I_{\rm COMP} > \frac{V_{\rm BUS}}{2LN_{\rm S}}D^2T_{\rm S} \tag{20}$$

we observe that (20) is always satisfied throughout the operating range of the charger. Therefore, if the application requirements cause (17) to be violated, the value of $I_{\rm COMP}$ must abide by (20) to avoid the appearance of subharmonic oscillations, while $I_{\rm REF}$ has to be set according to (5) to achieve the desired output current.

B. Proposed Control Mechanism in CV Mode

By including $I_{\rm S}$ in (12) and further developing, the perturbation on the duty cycle becomes

$$\widetilde{d}_{\rm k} = -\frac{D_{\rm k}}{I_{\rm S} + \frac{I_{\rm L,peak}}{N_{\rm S}}}\left(\widetilde{i}_{\rm S,k-1} + \frac{\widetilde{i}_{\rm L,k-1}}{N_{\rm S}}\right). \tag{21}$$

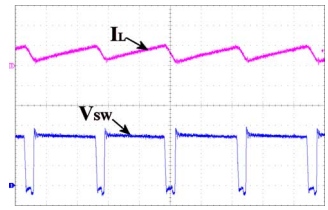


Fig. 15. Operation of the charger at low current and large duty cycle. Top trace: $I_{\rm L}$ [100 mA/div]; bottom trace: $V_{\rm SW}$ [2 V/div]. Time: 200 ns/div. $V_{\rm BAT} = 4.2$ V, $V_{\rm BUS} = 5$ V.

In Section IV, it was explained that, during CV mode $I_{\rm S} + \langle I_{\rm P,s}\rangle$ is constant, as the duty cycle is fixed by the voltage-control loop. So, the denominator in (21) is constant and eliminates the sensitivity of the duty-cycle perturbation on the load current level as expected in CV mode. This is different from CC mode, where the duty cycle perturbation is inversely proportional to the load current. Consequently, the voltage-control loop confers the charger a higher robustness against subharmonic oscillation. It should be pointed out that perturbation $\widetilde{i}_{\rm S,k-1}$ induced by $\widetilde{i}_{\rm L,k-1}$ cannot be easily determined, since all the gain and phase contributions from the converter output node to node $V_{\rm P}$ need to be computed. Accordingly, a stability criterion similar to (17) cannot be obtained, and software tools like MATLAB need to be used to assess the stability of the system. An algorithm was hence implemented to analyze the system stability in CV mode and, as reported in Fig. 15, subharmonic-free operation of the charger at low current and large duty cycle ($I_{\rm COMP} = 0$) is achieved.

C. Alternative Control Mechanism in CV Mode

The alternative implementation of the voltage-control loop in Fig. 8 is now analyzed to show its higher susceptibility to flip bifurcations. In CC mode, this version is exactly the same as the one in Fig. 7(a). The same considerations drawn in Section VA hence apply. As far as CV mode is concerned, we can still use (17) to predict period doubling as $I_{\rm S}$ does not concur to the generation of $V_{\rm P}$, and $V_{\rm REF\_ADP}$ is, once again, slowly varying. In Fig. 16, the simulated trajectory of the charger under standard and abnormal operating conditions is depicted. The analysis is referred to $V_{\rm BUS} = 5$ V, because this yields the largest duty cycle, and accordingly the worst-case scenario is presented. R_0 denotes the instability region at $I_{\rm COMP} = 0$, while $R_{\rm m}$ is the instability region corresponding to $I_{\rm COMP} = 20$ μA. First, we consider the case relative to $I_{\rm COMP} = 0$. During the output current decay and outside region R_0, the state trajectory under standard operating condition applies. When the $\langle I_{\rm OUT}\rangle$-$D$ characteristic enters R_0, the space trajectory bifurcates and the duty cycle assumes a set of values including 1 (maximum duty cycle). Following the CCM/DCM boundary crossing, the branches of the bifurcation diagram join together while the duty cycle reduces with the load current. As a matter of fact, it has been discussed that the behavior in Fig. 16 holds at large values of the duty cycle. After ramp compensation is applied, instability region R_0 is fully removed from the operating range of the converter ($D = [0, 0.84]$, $\langle I_{\rm OUT}\rangle = [0, 900$ mA$]$), and is now denoted by $R_{\rm m}$. In accordance with this, the state trajectory under standard operating conditions applies in the full operating range

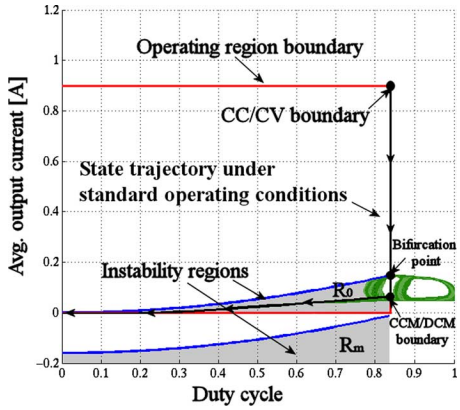


Fig. 16. State plane of the charger during current decay. $V_{\rm BUS} = 5$ V, $V_{\rm BAT} = 4.2$ V. When the region of instability intersects the operating range of the charger, the state trajectory bifurcates (green areas). If ramp compensation is adopted, the instability region falls outside the above range, and the space trajectory under standard operating conditions now applies in the full operating range of the charger (black solid line).

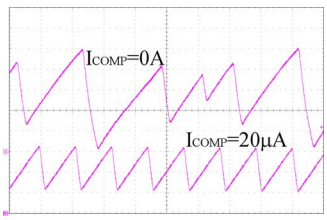


Fig. 17. Inductor current at $I_{\rm COMP} = 0$ A and $I_{\rm COMP} = 20\ \mu$A: $I_{\rm L}$ [50~mA/div], Time: 400 ns/div. $I_{\rm LOAD} = 90$ mA, $V_{\rm BAT} = 4.2$ V, $V_{\rm BUS} = 5$ V.

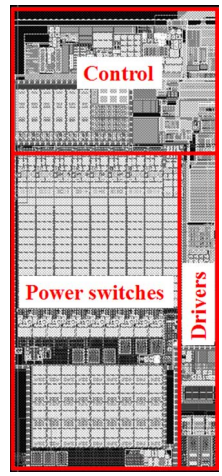


Fig. 18. Chip layout of the proposed switching charger.

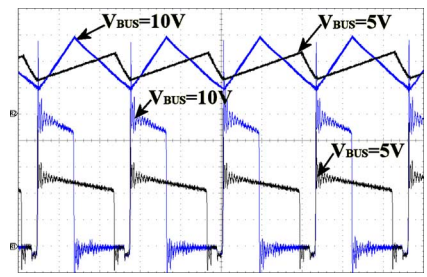


Fig. 19. Steady-state performances of the proposed charger at two voltage steps of $V_{\rm BUS}$. Top trace: $I_{\rm L}$ [500 mA/div], bottom trace: $V_{\rm SW}$ [2 V/div]. Time: 200 ns/div. $V_{\rm BAT} = 3.6$ V.

of the charger and global stability is achieved. As we previously mentioned, the CCM/DCM boundary lies within R_0, showing that the formation of period doubling is not to be attributed to the transition into DCM.

The experimental results captured at $\langle I_{\rm OUT}\rangle = 120$ mA in Fig. 17 confirm the above theoretical analysis. When $I_{\rm COMP} = 0$ A, the switching period clearly doubles, but the converter is still operating in CCM. So, for charge-control converters, the origin of subharmonic oscillations is only depending upon the load current level and duty cycle amplitude. To restore stability, $I_{\rm COMP}$ is set to 20 μA, hence fully removing period doubling.

VI. Experimental Results

Fig. 18 depicts the layout of the monolithic switching charger based on the proposed control approach. As reported in Table II, the microchip is based on a 1P6M TSMC 0.18-μm process and the charger die-size area is 1.6 mm^2. Measurements of the implemented battery charger IC are illustrated in Fig. 19, at two steps of the bus voltage. It can be observed that the average value of the inductor current stays rather constant at 900 mA despite the input voltage variation, while the ac ripple changes accordingly. The largest deviation from 900 mA occurs at $V_{\rm BUS} = 10$ V and amounts to 85 mA in accordance with the results in Section III.In Fig. 20, the startup characteristic of the switching charger is reported. In this measurement the input voltage is 10 V, which explains the large current ripple. It is worth noting

TABLE II
Switching Charger Specifications

Technology	TSMC 0.18μm 1P6M
Power supply range	5V-10V
Output voltage	2.1V-4.2V
Quiescent current (during charging)	2mA
Efficiency	86%
Switching frequency	2.2 MHz
Charging current	900mA
Chip area	1.6mm^2

that the inductor current increases very smoothly as the reference voltage generator exhibits a 3-dB bandwidth of 2 kHz. Finally, in Fig. 21, the transition from CC to CV mode has been experimentally analyzed by capturing the inductor current and output voltage waveforms with a data acquisition system. It should be observed that when the load current reduces, the current ripple decreases as the inductor current is moving away from the saturation region of the inductor-current characteristic. Accordingly, the output voltage ripple progressively decreases. When the output current falls below 250 mA, the converter enters discontinuous conduction mode and, as soon as the peak current is lower than 100 mA, the charger is eventually shut down. As emerging by visual inspection, the voltage error at shutdown is 0.15%, while the estimated worst case error is 0.65%. The smooth variation of the output voltage at the CC-CV

TABLE III
PERFORMANCE COMPARISON AMONG SEVERAL BATTERY CHARGERS

Reference	[1]	[5]	[2]	This work
Topology	LDO with smooth control and built-in resistance compensation	Charge pump with speed control circuit	LDO with adaptive reference	Charge-control buck with partial current sensing
Technology	TSMC 0.35 μm	TSMC 0.35 μm	*	TSMC 0.18 μm
Input voltage [V]	[4.5-6.5]	5	5	[5-10]
Output voltage [V]	[2.5-4.2]	[2.4-4.2]	[2.7-4.2]	[2.1-4.2]
Output current [mA]	500	700	800	900
Switching frequency	NA	10 MHz	NA	2.2 MHz
Efficiency [%]	NA	67.89	83	86
Die-size area [mm^2]	1.1	1.96	**	1.6

* Discrete components,
** Discrete components; IC embodiment suggested through simulations based on AMI's 0.35 μm technology.

TABLE IV
COMPARISON OF CURRENT ACCURACIES

Reference	[6]	[9]	This work
Accuracy	8%	4%	9.4%
Technology	AMI's 0.5 μm	AMS 0.6 μm	TSMC 0.18 μm
Input voltage [V]	3.5	5.2	10
Output current [mA]	800	450	900
Switching frequency	780 kHz	1 MHz	2.2 MHz
Die-size area [mm^2]	4.5	2.87	1.6

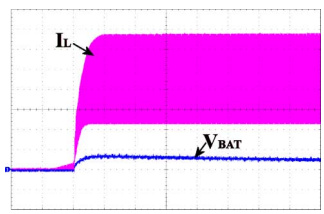


Fig. 20. Startup characteristics of the proposed charger. Top trace: $I_{\rm L}$ [200 mA/div]; bottom trace: $V_{\rm BAT}$ (ac) [100 m/div]. Time: 1 ms/div. $V_{\rm BAT} = 3$ V, $V_{\rm BUS} = 10$ V.

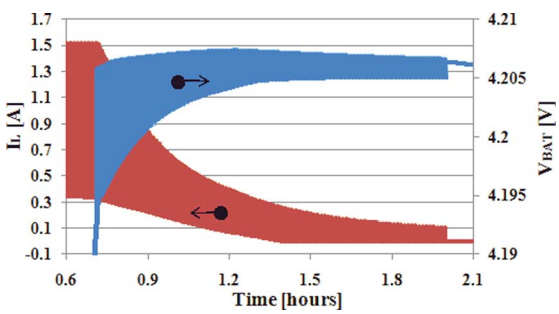


Fig. 21. Transition from CC to CV mode when the float level of 4.2 V is reached. $V_{\rm BUS} = 10$ V.

transition thus confers validity on the stability analysis carried out in Section IV.

A performance comparison among various charger architectures, including the one in this work, is reported in Table III. The comparison includes several charger topologies based on LDOs and charge pumps. The specified output voltage range refers to CC mode operation. As shown, the efficiency of the proposed switching charger is higher than those of its LDO and charge-pump counterparts, even at the supply voltage of 10 V. Coherently with the accuracy analysis presented in Section III, the results in Table III refer to an inductor saturating to 1 μH at $I_{\rm OUT} = 900$ mA. This low inductance value along with the high bus voltage of 10 V yield an inductor ripple current of 850 mA (peak-to-peak value). As a result, the rms losses associated with the switches' on-resistances and package parasitics limit the power efficiency to 86%. However, when we test the proposed charger at the same voltage as its counterparts ($V_{\rm BUS} = 5$ V), the rms losses reduce, hence increasing the efficiency up to 90.1%. A comparison in terms of current accuracy between the proposed converter and two state-of-the-art switching regulators is reported in Table IV. Although the proposed circuit has a higher current error of 9.4%, it is reminded that this measurement refers to an input voltage of 10 V and to a saturated inductor of 1 μH (see Section III). Therefore, a higher output current accuracy can be achieved by using inductors with better saturation characteristics.

Based on the above analysis, it emerges that the proposed control mechanism achieves very good performance in terms of efficiency and accuracy. Recall that the switching charger presented in this paper is suitable for high input voltage and high current applications, using a simple current sensing circuitry. It has also been observed that the charger start-up function is inherent to the adaptive reference voltage generator, thus simplifying the design of the IC controller.

VII. CONCLUSION

In this paper, a Li-Ion battery charger based on a 2.2-MHz charge-control buck regulator has been proposed. The novelty of the proposed charge-control converter consists of regulating the average output current by only sensing a portion of the inductor current and using an adaptive reference voltage. By adopting this approach, the charger average output current is

set to a constant value of 900 mA regardless of the battery voltage variation. The current sensing circuit is thus kept simple by using the proposed feed-forward control loop. In CV mode, a voltage feedback loop is established in addition to the pre-existing current control loop, preserving the smoothness of the output voltage at the transition from CC to CV mode.

An exhaustive accuracy analysis has been presented to assess the system performance with the innovative control strategy. A small-signal model accounting for the sampling effects of the adaptive reference voltage generator has been developed to analyze the system stability and subharmonic oscillations at low current levels. The output voltage of the charger ranges from 2.1 V to 4.2 V, and the power efficiency at 900 mA has been measured to be 86% at the input voltage of 10 V. The accuracy of the output current based on the proposed sensing technique is 9.4% at $V_{\rm BUS} = 10$ V when multilayer inductors featuring low saturation current are used.

APPENDIX
DERIVATION OF THE SMALL-SIGNAL MODEL AT THE CC/CV BOUNDARY

The small-signal transfer function of the adaptive reference voltage generator is obtained by considering the circuital schematic in Fig. 2 and the operating waveforms in Fig. 3. Perfectly matching between capacitors yields $C_{1,\rm a} = C_{1,\rm b} = C_1$. As capacitor C_2 is charged during interval $[(n-1+D_{\rm n})\,T_{\rm S}, (n-1+D_{\rm n}+D_{\rm S})\,T_{\rm S}]$, we can write by simple analysis

$$v_{\rm REF\_ADP,n} = v_{\rm REF\_ADP,n-1} + \frac{1}{C_2}\int_{(\rm n-1+d_n)T_S}^{(\rm n-1+d_n+D_S)T_S} G_{\rm m}(v_{\rm X} - v_{\rm REF\_ADP,n})\,{\rm d}t \quad \text{(A1)}$$

where $v_{\rm X}(t)$ is

$$v_{\rm X}(t) = \frac{I_{\rm REF} d_{\rm n} T_{\rm S}}{C_1} \quad \text{(A2)}$$

and $G_{\rm m}$ is the transconductance gain of the $G_{\rm m}$ cell. To simplify the model derivation, we observe that the integral in (A1) can be approximated by $(G_{\rm m}/C_2)\,(v_{\rm X} - \langle v_{\rm REF\_ADP}\rangle)\,D_{\rm S}T_{\rm S}$, as $D_{\rm S}T_{\rm S}$ is a narrow interval and because of the slow-scale dynamics of the sample-and-hold system. Under the latter assumption, we can also write

$$\frac{v_{\rm REF\_ADP,n} - v_{\rm REF\_ADP,n-1}}{T_{\rm S}} = \frac{d\,\langle v_{\rm REF\_ADP}\rangle}{{\rm d}t}. \quad \text{(A3)}$$

Equation (A1) hence reduces to (9).

From Fig. 3, we observe that $v_{\rm P}$ is compared at instant $(n-1+D_{\rm n})\,T_{\rm S}$ with the value of $v_{\rm REF\_ADP}$ generated in the previous interval, that is,

$$v_{\rm P,n-1+D_n} = v_{\rm REF\_ADP,n-1}. \quad \text{(A4)}$$

It follows that

$$\frac{1}{N_{\rm S}C_1}\int_{(\rm n-1)T_S}^{(\rm n-1+d_n)T_S} i_{\rm L}{\rm d}t + I_{\rm COMP} d_{\rm n}\frac{T_{\rm S}}{C_1} + \frac{1}{C_1}\int_{(\rm n-1)T_S}^{(\rm n-1+d_n)T_S} i_{\rm S}{\rm d}t = v_{\rm REF\_ADP,n-1}. \quad \text{(A5)}$$

By perturbing (A5) and converting the resulting expression in the Laplace domain, the small-signal model of the switching charger in Fig. 9 is derived.

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