Cycle	Reset	PC	Instr	(FSM) state	SrcA	SrcB	ALU Result	Zero	PCWrite	MemWrite	IRWrite	Branch
1	1	00	0	FETCH	00	04	04	0	1	0	1	0
2	0	04	addi 20020005	DECODE	04	x	x	x	0	0	0	0
3	0	04	addi 20020005	ADDIEX	00	05	05	0	0	0	0	0
4	0	04	addi 20020005	ADDIWB	x	x	x	0	0	0	0	0
5	0	04	addi 20020005	FETCH	04	04	08	0	1	0	1	0
6	0	08	addi 2003000c	DECODE	08	x	x	x	0	0	0	0
7	0	08	addi 2003000c	ADDIEX	00	0c	0c	0	0	0	0	0
8	0	08	addi 2003000c	ADDIWB	x	x	x	x	0	0	0	0
9	0	08	addi 2003000c	FETCH	08	04	0c	0	1	0	1	0
10	0	0c	addi 2067fff7	DECODE	0c	x	x	x	0	0	0	0
11	0	0c	addi 2067fff7	ADDIEX	0c	17	03	0	0	0	0	0
12	0	0c	addi 2067fff7	ADDIWB	x	x	x	x	0	0	0	0
13	0	0c	addi 2067fff7	FETCH	0c	04	10	0	1	0	1	0
14	0	10	or 00e22025	DECODE	10	x	x	x	0	0	0	0
15	0	10	or 00e22025	RTYPEEX	03	05	07	0	0	0	0	0
16	0	10	or 00e22025	RTYPEWB	x	x	x	x	0	0	0	0
17	0	10	or 00e22025	FETCH	10	04	14	0	1	0	1	0
18	0	14	and 00642824	DECODE	14	x	x	x	0	0	0	0
19	0	14	and 00642824	RTYPEEX	0c	07	04	0	0	0	0	0
20	0	14	and 00642824	RTYPEWB	x	x	x	x	0	0	0	0
21	0	14	and 00642824	FETCH	14	04	18	0	1	0	1	0
22	0	18	add 00a42820	DECODE	18	x	x	x	0	0	0	0
23	0	18	add 00a42820	RTYPEEX	04	07	0b	0	0	0	0	0
24	0	18	add 00a42820	RTYPEWB	x	x	x	x	0	0	0	0

25	0	18	add 00a42820	FETCH	18	04	1c	0	1	0	1	0
26	0	1c	beq 10a7000a	DECODE	1c	x	x	x	0	0	0	0
27	0	1c	beq 10a7000a	BRANCH	0b	03	08	0	0	0	0	0
28	0	1c	beq 10a7000a	FETCH	1c	04	20	x	1	0	1	0
29	0	20	slt 0064202a	DECODE	20	x	x	x	0	0	0	0
30	0	20	slt 0064202a	RTYPEEX	0c	07	00	x	0	0	0	0
31	0	20	slt 0064202a	RTYPEWB	x	x	x	x	0	0	0	0
32	0	20	slt 0064202a	FETCH	20	04	24	x	1	0	1	0
33	0	24	beq 10800001	DECODE	24	x	x	x	0	0	0	0
34	0	24	beq 10800001	BRANCH	00	00	00	1	0	0	0	1
35	0	24	beq 10800001	FETCH	24	08	2c	x	1	0	1	0
36	0	2c	slt 00e2202a	DECODE	2c	x	x	x	0	0	0	0
37	0	2c	slt 00e2202a	RTYPEEX	03	05	01	x	0	0	0	0
38	0	2c	slt 00e2202a	RTYPEWB	x	x	x	x	0	0	0	0
39	0	2c	slt 00e2202a	FETCH	2c	04	30	x	1	0	1	0
40	0	30	add 00853820	DECODE	30	x	x	x	0	0	0	0
41	0	30	add 00853820	RTYPEEX	01	0b	0c	0	0	0	0	0
42	0	30	add 00853820	RTYPEWB	x	x	x	x	0	0	0	0
43	0	30	add 00853820	FETCH	30	04	34	0	1	0	1	0
44	0	34	sub 00e23822	DECODE	34	x	x	x	0	0	0	0
45	0	34	sub 00e23822	RTYPEEX	0c	05	07	0	0	0	0	0
46	0	34	sub 00e23822	RTYPEWB	x	x	x	x	0	0	0	0
47	0	34	sub 00e23822	FETCH	34	04	38	0	1	0	1	0
48	0	38	sw ac670044	DECODE	38	x	x	x	0	0	0	0

49	0	38	sw	ac670044	MEMADR	0c	44	50	0	0	0	0	0
50	0	38	sw	ac670044	MEMWR	x	x	x	x	0	1	0	0
51	0	38	sw	ac670044	FETCH	38	04	3c	0	1	0	1	0
52	0	3c	lw	8c020050	DECODE	3c	x	x	x	0	0	0	0
53	0	3c	lw	8c020050	MEMADR	00	50	50	0	0	0	0	0
54	0	3c	lw	8c020050	MEMRD	x	x	x	x	0	0	0	0
55	0	3c	lw	8c020050	MEMWB	x	x	x	x	0	0	0	0
56	0	3c	lw	8c020050	FETCH	3c	04	40	0	1	0	1	0
57	0	40	j	08000011	DECODE	40	x	x	x	0	0	0	0
58	0	40	j	08000011	JUMP	x	x	x	x	1	0	0	0
59	0	40	j	08000011	FETCH	44	04	48	0	1	0	1	0
60	0	48	sw	ac020054	DECODE	48	x	x	x	0	0	0	0
61	0	48	sw	ac020054	MEMADR	00	54	54	0	0	0	0	0
62	0	48	sw	ac020054	MEMWR	x	x	x	x	0	1	0	0

Table 1. Expected Instruction Trace