**ECE 212 Lab 9**

**Table for Prelab**

**Spring 2022**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| State | pcwrite | memwrite | irwrite | regwrite | alusrca | branch | iord | memtoreg | regdesg | alusrcb[1:0] | pcsrc[1:0] | aluop[1:0] |
| FETCH (0) | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 01 | 00 | 00 |
| DECODE (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 00 | 00 |
| MEMADR (2) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 00 | 00 |
| MEMRD (3) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 00 | 00 | 00 |
| MEMWB (4) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 00 | 00 | 00 |
| MEMWR (5) | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 00 | 00 | 00 |
| RTYPEEX (6) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 00 | 00 | 10 |
| RTYOEWB (7) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 00 | 00 | 00 |
| BEQEX (8) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 00 | 01 | 01 |
| ADDIEX (9) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 00 | 00 | 00 |
| ADDIWB (10) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 10 | 00 | 00 |
| JEX (11) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 10 | 00 |

Table 1 – Main Decoder Output Table