OmniVision

datasheet

PRODUCT SPECIFICATION

1/13" color CMOS VGA (640x480) CameraCubeChip™
with OmniBSI+™ technology

OVM7695-RAEA

color CMOS VGA (640 x480) CameraCubeChip™ with OmniBSI+™ technology

datasheet
PRODUCT SPECIFICATION

version 2.03
september 2013

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular and picture phones

ordering information

- **OVM7695-RAEA** (color, lead free)
  CameraCubeChip™ with black coating

features

- support image sizes: VGA (640x480), QVGA (320x240), QQVGA (160x120), and HF (640x20)
- support output formats: YUV4:2:2, RAW8 through MIPI, YUV422, RAW8, RAW10 through OmniVision's proprietary SPI
- on-chip phase lock loop (PLL)
- built-in 1.5V regulator for digital block
- capable of maintaining register values at software power down
- programmable controls for frame rate, mirror and flip, AEC/AGC, and windowing
- support horizontal and vertical sub-sampling
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB) and automatic black level calibration (ABLC)
- image quality controls: defect pixel correction and lens shading correction
- support black sun cancellation
- standard serial SCCB interface
- parallel I/O tri-state configurability and programmable polarity

key specifications (typical)

- **active array size:** 656 x 496
- **power supply:**
  analog: 2.8V ± 5%
  core: 1.5VDC ± 5% (internal regulator)
  I/O: 2.8V, 1.8V
- **power requirements:**
  I_{DD-A}: 15 mA
  I_{DD-IO}: 20 mA
  XSHUTDOWN: 5 µA
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 4-2**)
  stable image: 0°C to 50°C junction temperature (see **table 4-2**)
- **output formats:** YUV422, RAW RGB
- **diagonal field of view (FOV):** 61°
- **f no.:** 2.7
- **focal length:** 1.21 mm
- **input clock frequency:** 6 ~ 27 MHz (see **table 4-5**)
- **scan mode:** progressive
- **maximum image transfer rate:**
  VGA (640 x 480): 30 fps
  QVGA (320 x 240): 60 fps
  QQVGA (160 x 120): 120fps
  HF (640 x 20): 120 fps
- **sensitivity:** 1200mV/Lux-sec
- **shutter:** rolling shutter
- **max S/N ratio:** 35.9 dB
- **dynamic range:** 66.7 dB @ 16x gain
- **maximum exposure interval:** 536 x t_{ROW}
- **pixel size:** 1.75 µm x 1.75 µm
- **dark current:** 10 e^-/s @ 50°C junction temperature
- **image area:** 1148 µm x 868 µm
- **package dimensions (including ball height):** 2420 µm x 2350 µm x 2325 µm

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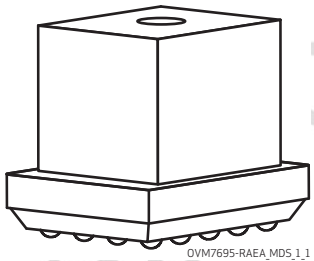
1 system level description

1.1 overview

The CameraCubeChip™ (see **figure 1-1**) consists of a low voltage high-performance 1/13-inch VGA CMOS image sensor that provides the full functionality of a single-chip VGA (640x480) camera and image processor in a small footprint package. The OVM7695 provides full-frame, sub-sampled and cropped images in various formats via the Serial Camera Control Bus (SCCB) interface.

figure 1-1 OVM7695 CameraCubeChip

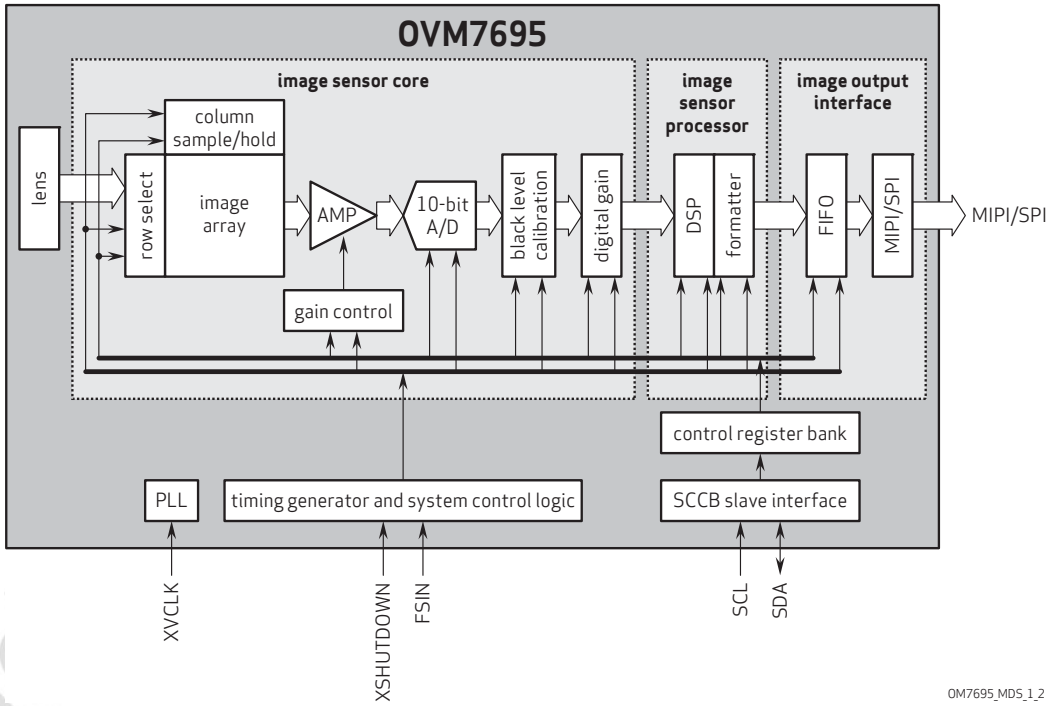


The OVM7695 has an image array capable of operating at up to 30 frames per second (fps) in VGA resolution with complete user control over image quality, formatting and output data transfer. Enabling 640 x 480 pixels to be output allows the user to perform image stabilization functions with post processing. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc.,are programmable through the SCCB interface. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise (FPN), smearing, blooming, etc., to produce a clean, fully stable color image.

1.2 architecture

figure 1-2 shows the functional block diagram of the image sensor in the OVM7695.

figure 1-2 OVM7695 sensor block diagram



1.3 format and frame rate

The OVM7695 supports the following formats: YUV422 and RAW8 through MIPI and YUV422, RAW8, and RAW10 through OmniVision's proprietary SPI.

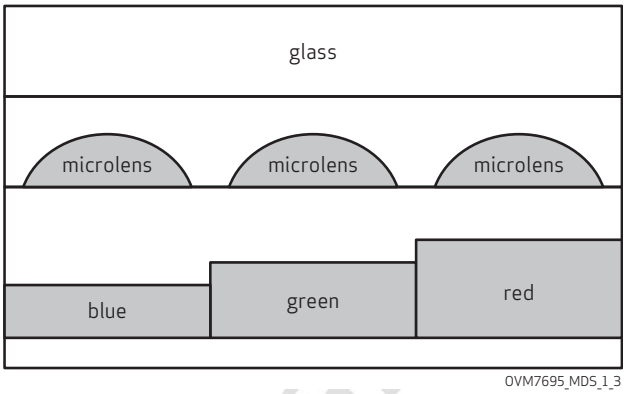
table 1-1 format and frame rate

format	resolution	frame rate	methodology	pixel clock
VGA	640x480	30 fps	full	24/12 MHz
QVGA	320x240	60 fps	subsampling	24/12 MHz
QQVGA	160x120	120 fps	subsampling	24/12 MHz
HF	640x20	120 fps	cropping	24 MHz

1.3.1 image sensor array

The OVM7695 sensor has an image array of 656 x 496 pixels for a total of 325,376 pixels, of which 640 x 480 are active (307,200 pixels). **figure 1-3** shows a cross-section of the image sensor array.

figure 1-3 image sensor array



1.3.2 timing generator

In general, the timing generator controls the following functions:

- array control and frame generation
- internal timing signal generation and distribution
- frame rate timing
- automatic exposure control (AEC)

1.3.3 analog signal processor

This block performs all analog image functions including Automatic Gain Control (AGC).

1.3.4 A/D converter

After the analog processing block, the Bayer pattern Raw signal is fed to a 10-bit analog-to-digital (A/D) converter shared by RGB channels. This A/D converter operates at speeds up to 12 MHz and is fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- automatic black-level calibration (ABLC)
- additional A/D range controls

In general, the combination of the A/D range multiplier and A/D range control sets the A/D range and maximum values.

1.3.5 test pattern generator

The test pattern generator features the following:

- 8-bar color bar pattern

1.3.6 digital signal processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- automatic white balance (AWB)
- edge enhancement (a two-dimensional high pass filter)
- color space converter (can change Raw data to RGB or YUV)
- saturation control
- white/black pixel correction
- lens correction
- programmable gamma control

1.4 power up sequence

The digital and analog supply voltages can be powered up in any order, for example (DOVDD then AVDD or AVDD then DOVDD).

1.4.1 on-chip power up

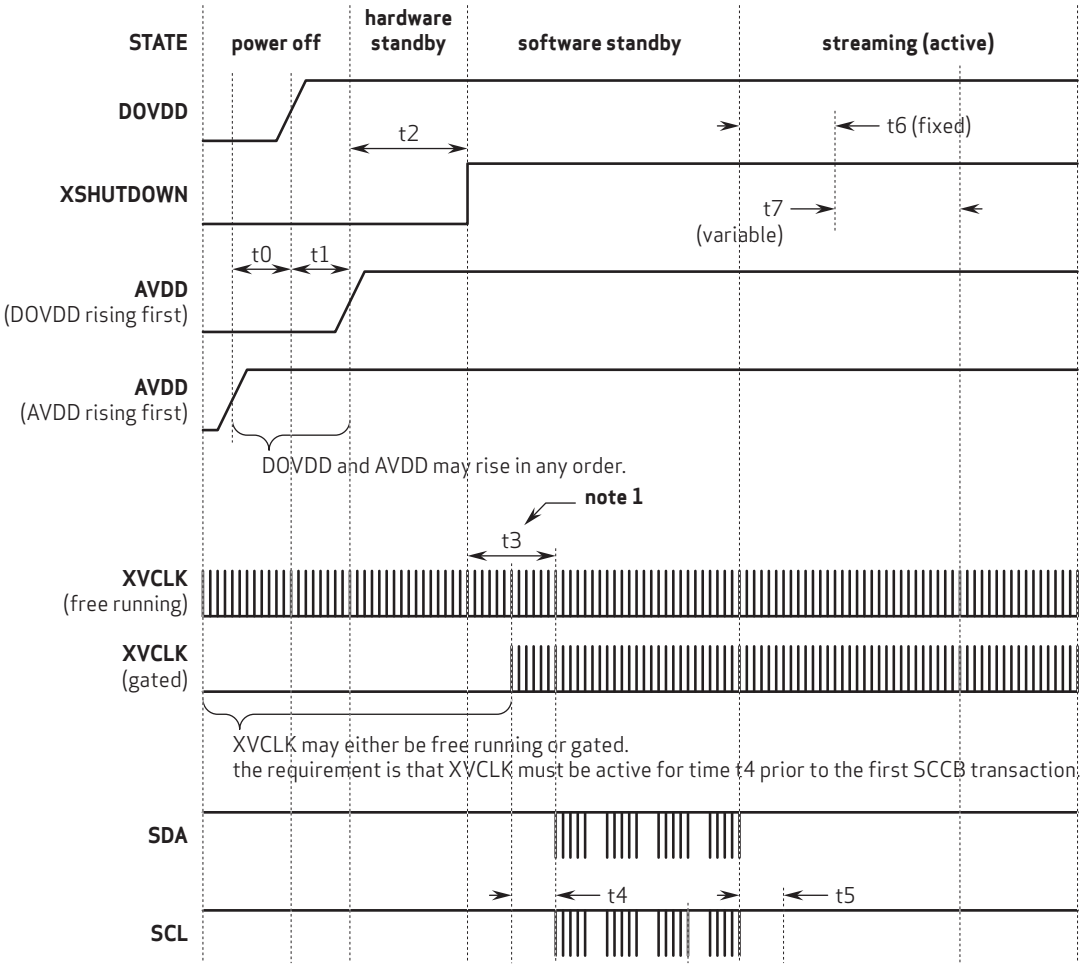
- if XSHUTDOWN is low when the power supplies are brought up, sensor will go into hardware standby mode
- if XSHUTDOWN is high when the power supplies are brought up, sensor will go into software standby mode

The XVCLK clock can either be initially low and then enabled during software standby mode or XVCLK can be a free running clock.

table 1-2 power up sequence timing constraints

constraint	label	min	max	unit
AVDD rising - DOVDD rising	t0	AVDD and DOVDD may rise in any order		ns
DOVDD rising - AVDD rising	t1	rising separation can vary from 0 ns to infinity		ns
AVDD rising - XSHUTDOWN rising	t2	0.0		
XSHUTDOWN rising - first SCCB transaction	t3	8192		XVCLK cycles
minimum number of XVCLK cycles prior to the first SCCB transaction	t4	8192		XVCLK cycles
PLL start up/lock time	t5		0.2	ms
entering streaming mode - first frame start sequence (fixed part)	t6		10	ms
entering streaming mode - first frame start sequence (variable part)	t7	delay is the integration time value		lines

figure 1-4 power up sequence 1



note 1 when using the internal DVDD, an additional 1ms must be added to t3 to wait for SCCB to become stable

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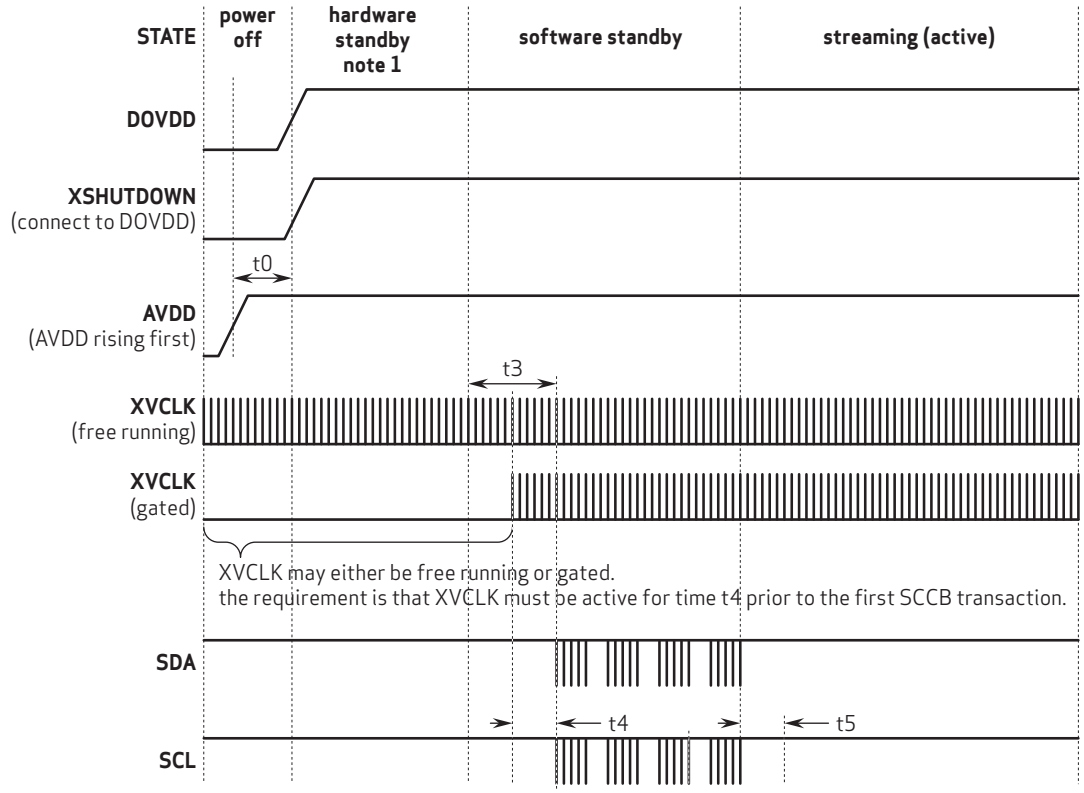
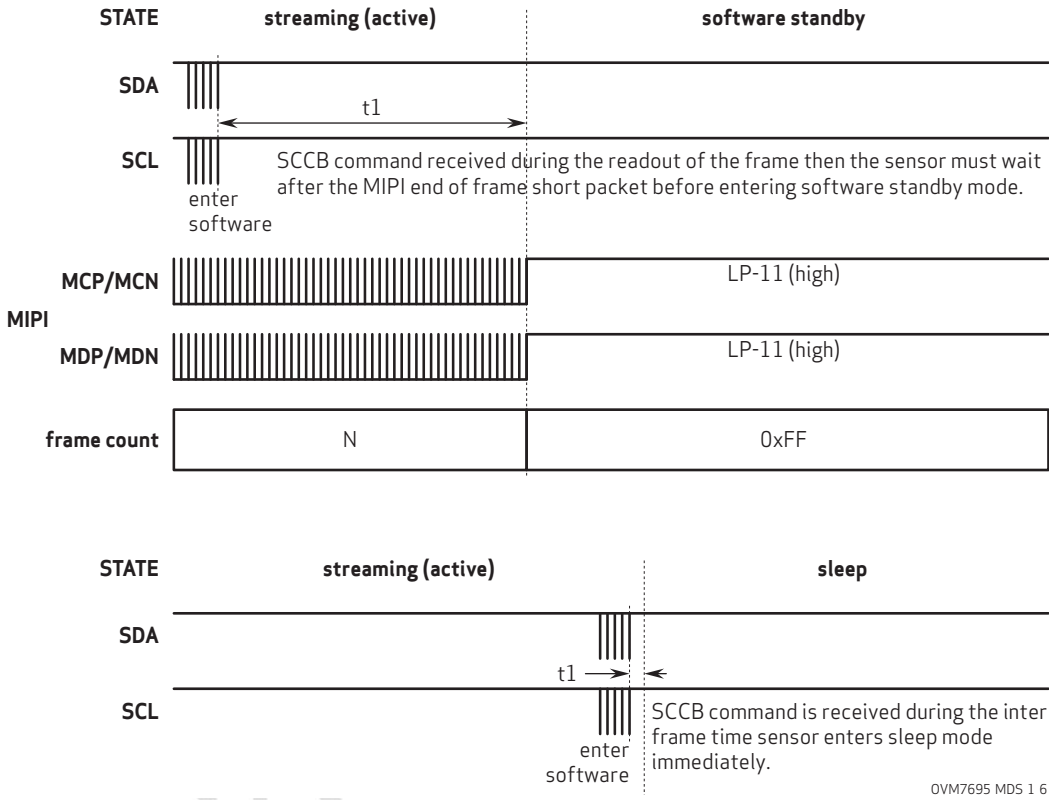
figure 1-5 power up sequence 2



note 1 with low power consumption

OVM7695_DS_1_5

figure 1-6 standby sequence



1.5 power down sequence

The digital and analog supply voltages can be powered down in any order (e.g. DOVDD, then AVDD or AVDD, then DOVDD). Similar to the power-up sequence, the XVCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of MIPI data is being output, then the sensor must wait for the MIPI frame end code before entering software standby mode.

If the SCCB command to exit streaming mode is received during the enter frame time, then the sensor must enter software standby mode immediately.

table 1-3 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of XVCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		XVCLK cycles
XSHUTDOWN falling - AVDD falling	t3	0.0		ns
AVDD falling - DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling - AVDD falling	t5			ns

figure 1-7 power down sequence 1

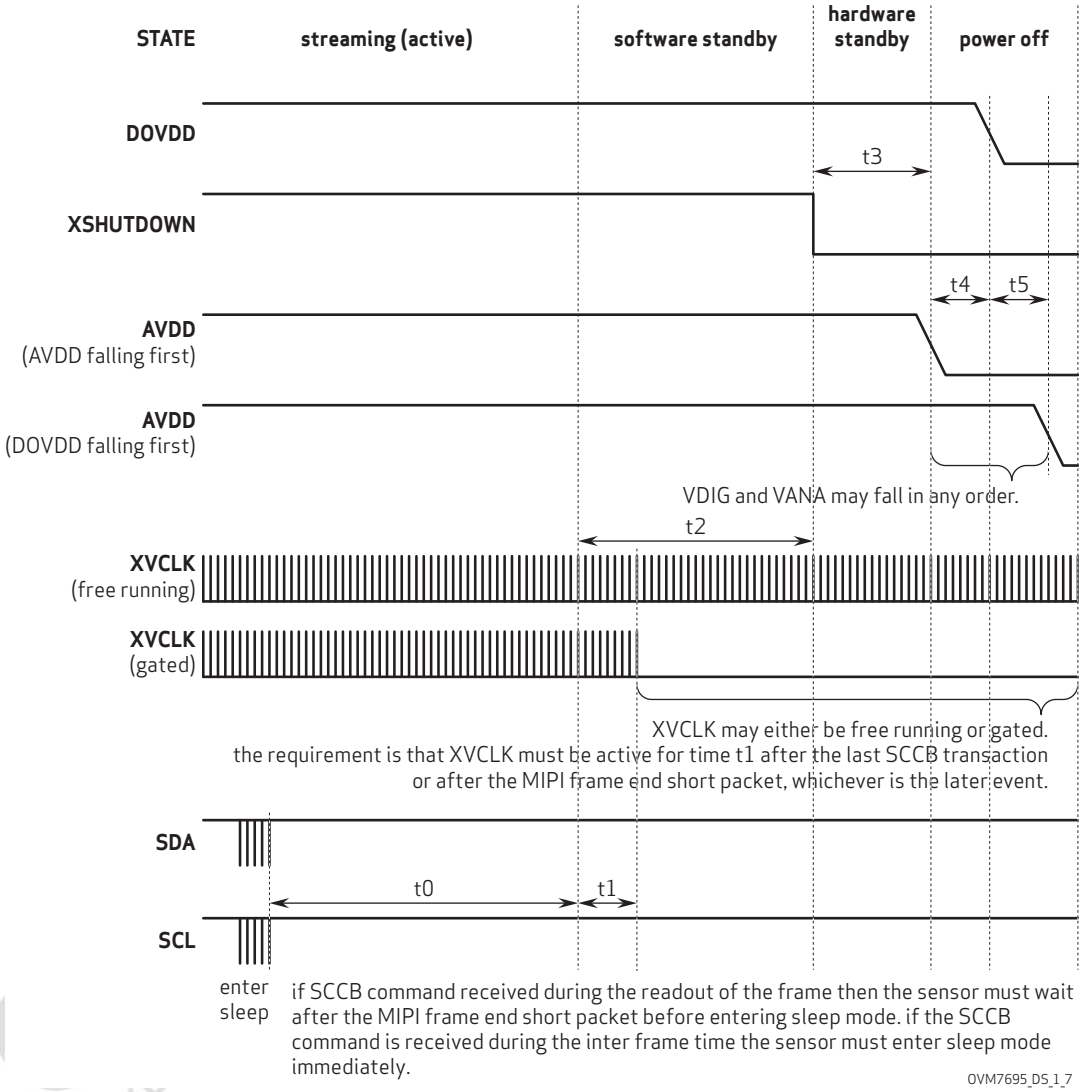
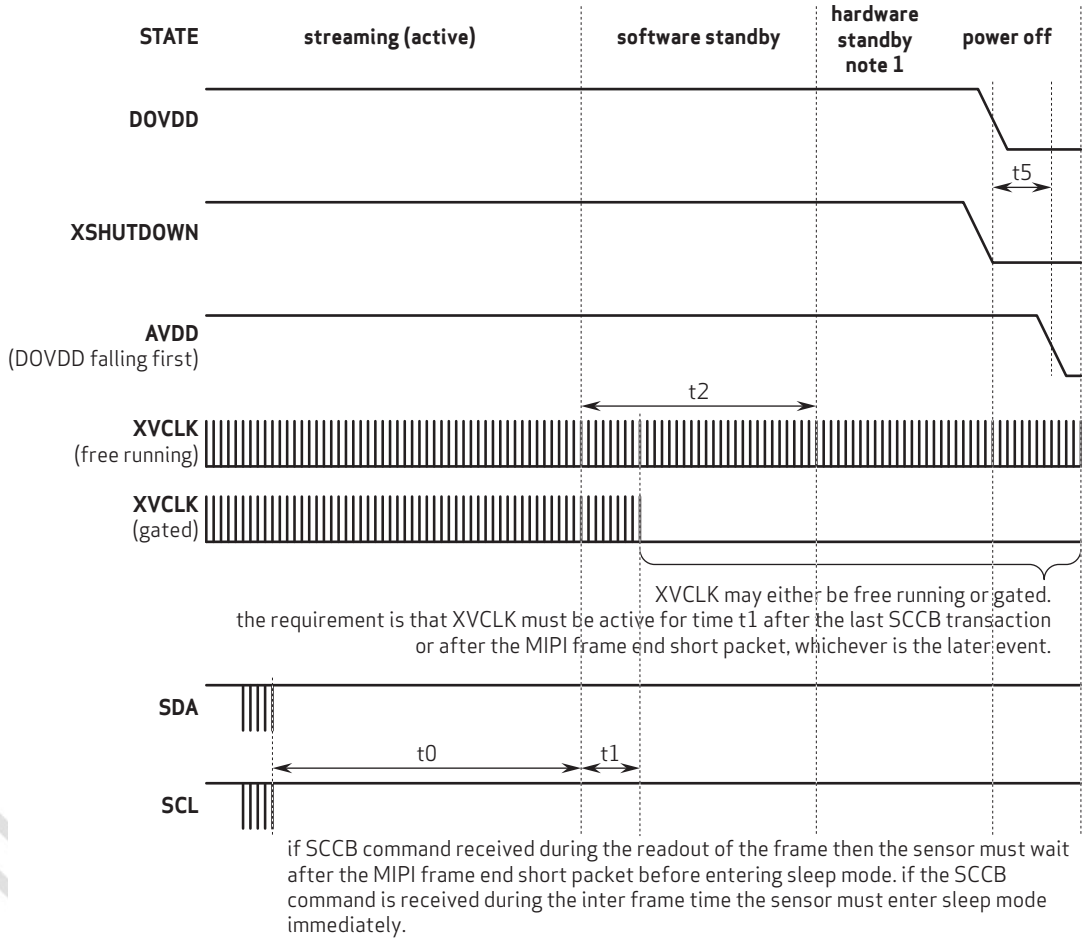


figure 1-8 power down sequence 2



note 1 with low power consumption

OVM7695_MDS_1_8

1.6 system clock control

The OVM7695 PLL allows for an input clock frequency ranging from 6~27 MHz.

The PLL can be bypassed by setting register 0x3104[1] to 1.

1.7 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

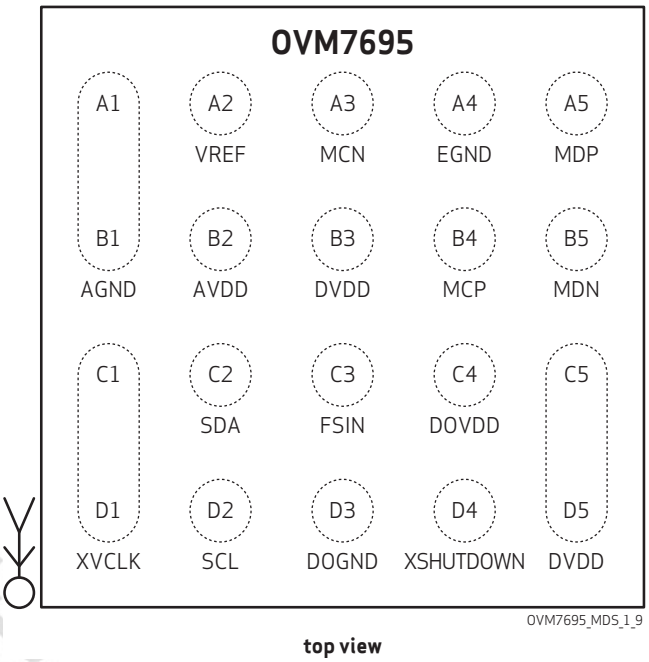
1.8 signal descriptions

table 1-4 lists the signal descriptions and their corresponding pin numbers for the OVM7695 image sensor.

table 1-4 signal descriptions

pin number	signal name	pin type	description
A1	AGND	ground	ground for analog circuit
A2	VREF	reference	reference for analog circuit
A3	MCN	output	MIPI TX clock negative output
A4	EGND	power	ground for MIPI circuit
A5	MDP	output	MIPI TX data lane positive output
B1	AGND	ground	ground for analog circuit
B2	AVDD	power	power for analog circuit
B3	DVDD	power	power for digital circuit
B4	MCP	output	MIPI TX clock lane positive output
B5	MDN	output	MIPI TX data lane negative output
C1	XVCLK	input	system clock input
C2	SDA	I/O	SCCB interface data I/O
C3	FSIN	input	frame sync signal
C4	DOVDD	power	power for I/O circuit
C5	DVDD	power	power for digital circuit
D1	XVCLK	input	system clock input
D2	SCL	input	SCCB interface input clock
D3	DOGND	ground	ground for I/O circuit
D4	XSHUTDOWN	input	reset and power down (active low with internal pull down resistor)
D5	DVDD	power	power for digital circuit

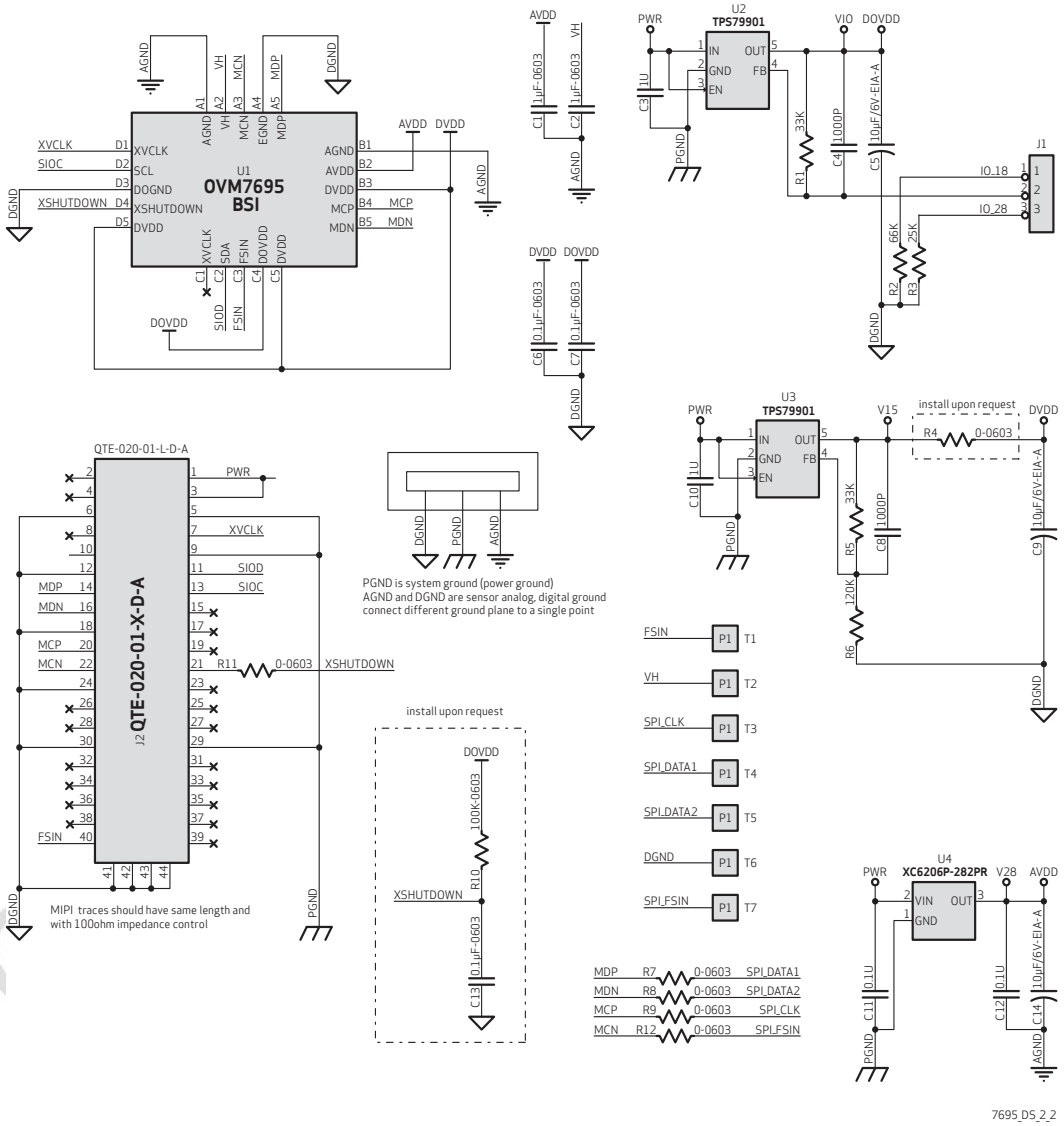
figure 1-9 pin diagram



top view

1.9 reference schematic

figure 1-10 OVM7695 reference schematic



7695_DS_2_2

2 mechanical specifications

2.1 physical specifications

figure 2-1 package specifications

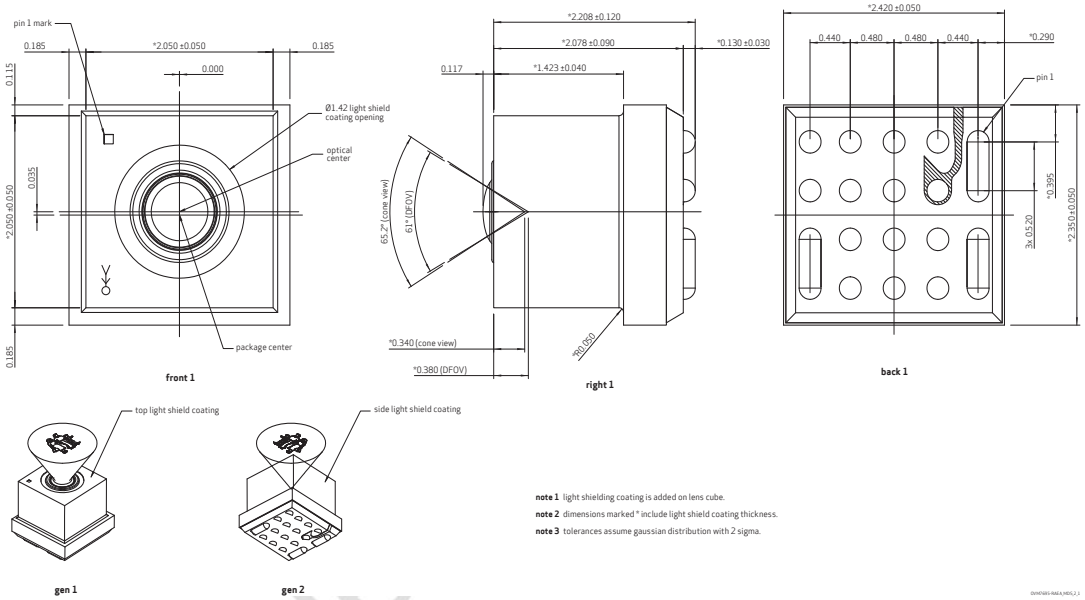
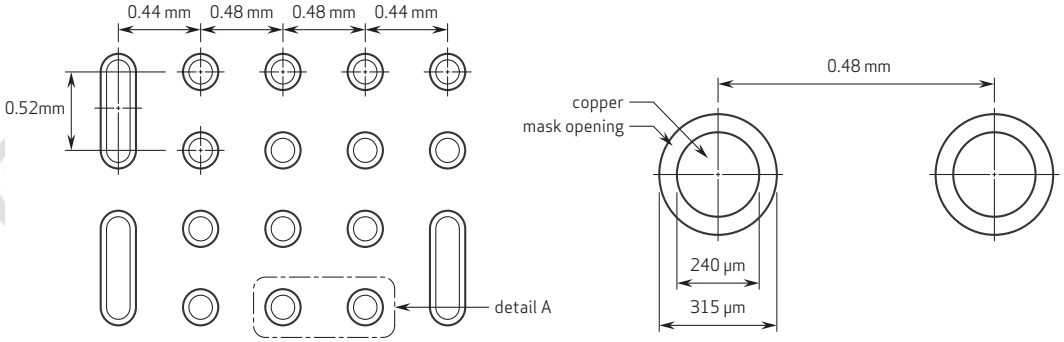


figure 2-2 recommended component layout



OVM7695 pad pattern **detail A**

note to enhance solder joint reliability, we recommend an underfill process be used on this component.

OVM7695_MDS_2_2

2.2 IR reflow specifications

note
The OVM7695 uses a lead free package.

figure 2-3 IR reflow ramp rate requirements

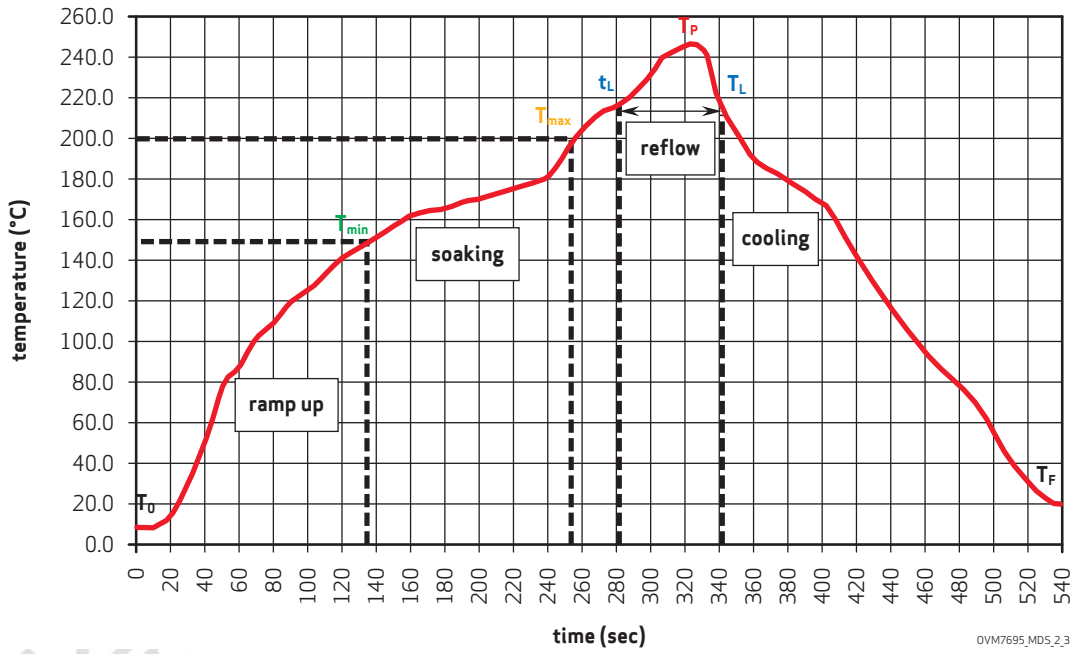


table 2-1 reflow conditions[ab]

zone	description	exposure
ramp up to A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_p)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak	maximum temperature in SMT	245°C ± 5°C (duration max. 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (t_p to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_p	room temperature to peak temperature	≤ 8 minutes

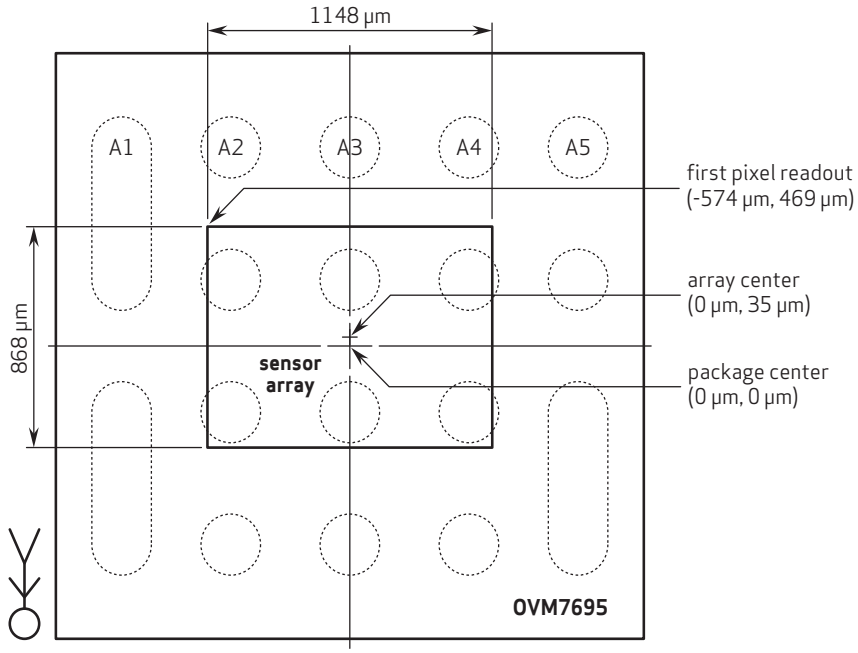
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommended

3 optical specifications

3.1 sensor array center

figure 3-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A5 oriented down on the PCB.

OVM7695_MDS_3_1

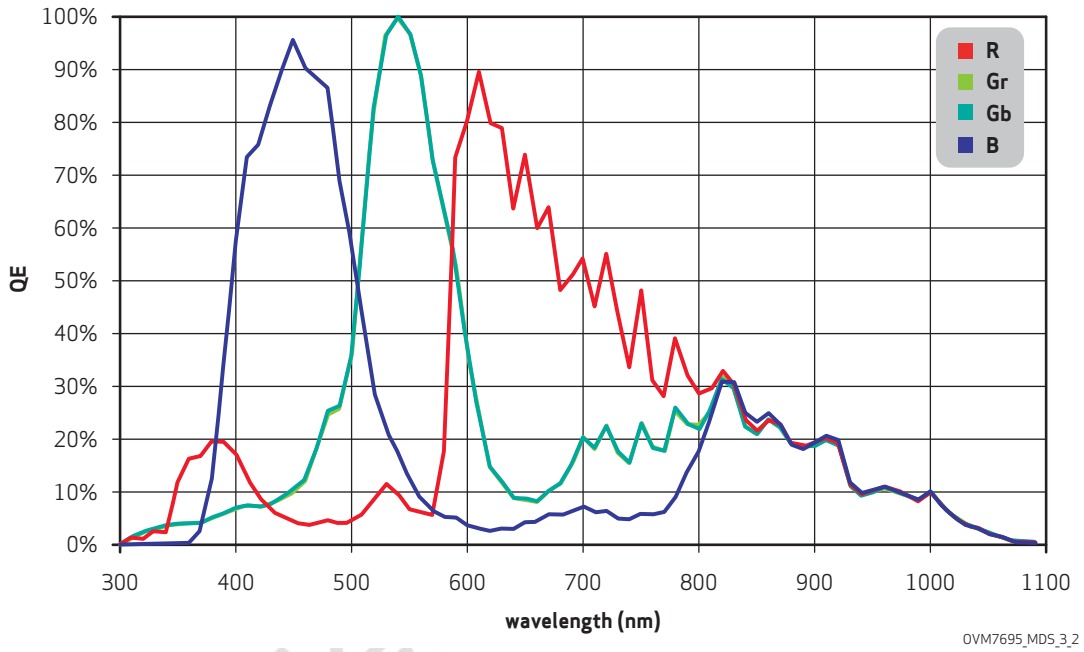
3.2 optical specifications

table 3-1 optical specifications

lens parameter		specification
field-of-view (FOV)	horizontal	50.0°
	diagonal	61.0°
f no.		f/2.7
focal length		1.21 mm
optical layout		2-element lens
maximum image circle		1.58 mm diameter
TV distortion		<3% at 95% field
relative illumination (optical)		67% @ y = 0.7 mm
focus	mechanism	fixed focus
	depth of field	30 cm → ∞
IR elimination filter 50% cut-off		665 nm ± 10 nm

3.3 spectrum response

figure 3-2 spectrum response graph



4 operating specifications

4.1 absolute maximum ratings

table 4-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 functional temperature

table 4-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to 50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

4.3 DC characteristics

table 4-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current		15	25	mA
I_{DD-IO}			20	30	mA
$I_{DDS-SCCB}$	standby current		120	650	µA
$I_{DDS-XSHUTDOWN}$			5	20	µA
digital inputs (typical conditions: DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[a]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[a]	SCL and SDA	1.26	1.8	2.3	V

a. based on DOVDD = 1.8V

4.4 AC characteristics

table 4-4 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V, V_{DD-IO} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 4-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

5 image sensor processor digital functions

5.1 ISP general control

table 5-1 ISP general control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[7]: bcc_en LCDC function enable signal 0: Disable 1: Enable Bit[6]: gamma_en Gamma function enable signal 0: Disable 1: Enable Bit[5]: awb_en AWB function enable signal 0: Disable 1: Enable Bit[4]: awbg_en AWBG function enable signal 0: Disable 1: Enable Bit[3]: bc_en Black DPC function enable signal 0: Disable 1: Enable Bit[2]: wc_en White DPC function enable signal 0: Disable 1: Enable Bit[1]: lenc_en LENC function enable signal 0: Disable 1: Enable Bit[0]: isp_en ISP functions enable signal 0: Disable 1: Enable

table 5-1 ISP general control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x3F	RW	Bit[5]: avg_en AVG functions enable signal 0: Disable 1: Enable Bit[4]: blc_en BLC functions enable signal 0: Disable 1: Enable Bit[3]: sde_en SDE functions enable signal 0: Disable 1: Enable Bit[2]: uv_avg_en UVAAVG functions enable signal 0: Disable 1: Enable Bit[1]: cmx_en CMX functions enable signal 0: Disable 1: Enable Bit[0]: cip_en CIP functions enable signal 0: Disable 1: Enable

table 5-1 ISP general control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5002	ISP CTRL02	0x88	RW	Bit[7:6]: avg_sel AVG source select option 00: WINC output (Y/RAW) 01: LENC RAW 10: DPC RAW 11: CMX Y Bit[5]: isp_eof_sel ISP output EOF option 0: ISP output EOF is window EOF 1: ISP output EOF is its input EOF Bit[4]: isp_sof_sel ISP output SOF option 0: ISP output SOF is pre SOF 1: ISP output SOF is its input SOF Bit[3]: lenc_bias_plus 0: Bias plus option is disabled in LENC 1: Bias plus option is enabled in LENC Bit[2]: lcdc_bf_awbg LCD correction module location option 0: LCDC is after gamma 1: LCDC is before AWBG Bit[1]: F5060 Manual 50Hz or 60Hz frequency 0: 60Hz 1: 50Hz Bit[0]: raw_aft_cip When the sensor outputs in RAW image format, this option selects RAW output source 0: Output RAW after DPC 1: Output RAW after CIP DNS
0x5003	ISP CTRL03	0x00	RW	Bit[7]: dns_opt Bit[6]: bl_rblue_rvs Black line Rblue reverse signal Bit[5]: gfirst_rvs Reverse signal of GFirst Bit[4]: rblue_rvs Normal image Rblue reverse signal Bit[3]: isp_raw_en Option used in PRE ISP Bit[2:0]: win_yoff_adj Option used in PRE ISP
0x5004	ISP CTRL04	0x40	RW	Bit[7:0]: bcc_red_gain Gain for LCDC module red channel It has 6 fractions

table 5-1 ISP general control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5005	ISP CTRL05	0x40	RW	Bit[7:0]: bcc_grn_gain Gain for LCDC module green channel It has 6 fractions
0x5006	ISP CTRL06	0x40	RW	Bit[7:0]: bcc_blu_gain Gain for LCDC module blue channel It has 6 fractions
0x5007	ISP CTRL07	0x07	RW	Bit[7]: gamma_bias_man_en Manual enable signal for gamma bias Bit[6]: bcc_bias_man_en Manual enable signal for LCDC bias Bit[5]: awb_bias_man_en Manual enable signal for AWB bias Bit[4]: lenc_bias_man_en Manual enable signal for LENC bias Bit[3]: gamma_bias_en Enable signal for gamma bias Bit[2]: bcc_bias_en Enable signal for LCDC bias Bit[1]: awb_bias_en Enable signal for AWB bias Bit[0]: lenc_bias_en Enable signal for LENC bias
0x5008	ISP CTRL08	0x10	RW	Bit[7:0]: bias_man Manual bias used in gamma, LCDC, AWB and LENC modules
0x5009	ISP CTRL09	0x00	RW	Bit[1]: sram_test_cip Bit[0]: sram_test_dpc
0x500A	ISP CTRL0A	0xAA	RW	Bit[7:4]: sram_rm_cip Bit[3:0]: sram_rm_dpc

5.2 lens correction (LENC)

The LENC algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature.

table 5-2 LENC related registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[1]: lenc_en LENC function enable signal 0: Disable 1: Enable
0x5100	RED X0	0x01	RW	Bit[1:0]: red_x0[9:8] MSB of horizontal center position of red channel
0x5101	RED X0	0x50	RW	Bit[7:0]: red_x0[7:0] LSB of horizontal center position of red channel
0x5102	RED Y0	0x00	RW	Bit[1:0]: red_y0[9:8] MSB of vertical center position of red channel
0x5103	RED Y0	0xF8	RW	Bit[7:0]: red_y0[7:0] LSB of vertical center position of red channel
0x5104	RED A1	0x22	RW	Bit[6:0]: red_a1 Gain coefficient for the square of distance of current red pixel position and red center
0x5105	RED A2	0x07	RW	Bit[3:0]: red_a2 Precision of gain coefficient for the square of distance of current red pixel position and red center
0x5106	RED B1	0xC2	RW	Bit[7:0]: red_b1 Gain coefficient for the distance of current red pixel position and red center
0x5107	RED B2	0x08	RW	Bit[3:0]: red_b2 Precision of gain coefficient for the distance of current red pixel position and red center. Gain of current red pixel is defined with the distance (r), red_a1, red_a2, red_b1 and red_b2 Gain = [(red_a1×r2)>>red_a2]+[(red_b1×r)>>red_b2]
0x5108	GRN X0	0x01	RW	Bit[1:0]: grn_x0[9:8] MSB of horizontal center position of green channel
0x5109	GRN X0	0x50	RW	Bit[7:0]: grn_x0[7:0] LSB of horizontal center position of green channel

table 5-2 LENC related registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x510A	GRN Y0	0x00	RW	Bit[1:0]: grn_y0[9:8] MSB of vertical center position of green channel
0x510B	GRN Y0	0xF8	RW	Bit[7:0]: grn_y0[7:0] LSB of vertical center position of green channel
0x510C	GRN A1	0x22	RW	Bit[6:0]: grn_a1 Gain coefficient for the square of distance of current green pixel position and green center
0x510D	GRN A2	0x07	RW	Bit[3:0]: grn_a2 Precision of gain coefficient for the square of distance of current green pixel position and green center
0x510E	GRN B1	0xC2	RW	Bit[7:0]: grn_b1 Gain coefficient for the distance of current green pixel position and green center
0x510F	GRN B2	0x08	RW	Bit[3:0]: grn_b2 Precision of gain coefficient for the distance of current green pixel position and green center. Gain of current green pixel is defined with the distance (r), grn_a1, grn_a2, grn_b1 and grn_b2 Gain = [(grn_a1×r2)>>grn_a2] + [(grn_b1×r)>>grn_b2]
0x5110	BLUE X0	0x01	RW	Bit[1:0]: blu_x0[9:8] MSB of horizontal center position for blue channel
0x5111	BLUE X0	0x50	RW	Bit[7:0]: blu_x0[7:0] LSB of horizontal center position for blue channel
0x5112	BLUE Y0	0x00	RW	Bit[1:0]: blu_y0[9:8] MSB of vertical center position for blue channel
0x5113	BLUE Y0	0xF8	RW	Bit[7:0]: blu_y0[7:0] LSB of vertical center position for blue channel
0x5114	BLUE A1	0x22	RW	Bit[6:0]: blu_a1 Gain coefficient for the square of distance of current blue pixel position and blue center
0x5115	BLUE A2	0x07	RW	Bit[3:0]: blu_a2 Precision of gain coefficient for the square of distance of current blue pixel position and blue center
0x5116	BLUE B1	0xC2	RW	Bit[7:0]: blu_b1 Gain coefficient for the distance of current blue pixel position and blue center

table 5-2 LENC related registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5117	BLUE B2	0x08	RW	Bit[3:0]: blu_b2 Precision of gain coefficient for the distance of current blue pixel position and blue center Gain of current blue pixel is defined with the distance (r), blu_a1, blu_a2, blu_b1 and blu_b2 Gain = [(blu_a1×r2)>>blu_a2] + [(blu_b1×r)>>blu_b2]
0x5118	LENC CTRL	0x04	RW	Bit[2]: rnd_en Round enable which can be enable to generate random round bit Bit[1:0]: Not used

5.3 gamma

Gamma correction converts the linear response data of the image sensor to compensate for properties of human vision. It maximizes the use of digital data relative to how humans perceive light and color. Higher gain is added at low light levels and lower gain at higher light levels. This non-linear function can be described by the power function, whose exponent value is called gamma. This module is designed to implement the gamma curve correction in piece-wise linear segments.

table 5-3 gamma registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[6]: gamma_en Gamma function enable signal 0: Disable 1: Enable
0x5300	GAMMA CTRL	0x01	RW	Bit[1]: yslp15_man_en Manual yst15 slope enable 0: Use calculated slope 1: Use register YSLP15 as slope Bit[0]: bias_en Bias enable 0: Bias is not used in gamma function 1: Bias is used in gamma function data_o = (data_i - bias) × gamma_gain + bias
0x5301	YST1	0x26	RW	Bit[7:0]: Yst1 Gamma gain coefficient for data not larger than 4 For data not larger than 4, the gamma data is calculated with the following equation: yst1×data/4
0x5302	YST2	0x35	RW	Bit[7:0]: Yst2 Gamma gain coefficient for data that is 8 For data larger than 4 and less than 8, the gamma data are calculated with the following equation: yst1+(yst2-yst1)×(data-4)/4
0x5303	YST3	0x48	RW	Bit[7:0]: Yst3 Gamma gain coefficient for data that is 16 For data larger than 8 and less than 16, the gamma data is calculated with the following equation: yst2+(yst3-yst2)×(data-8)/8

table 5-3 gamma registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5304	YST4	0x57	RW	Bit[7:0]: Yst4 Gamma gain coefficient for data that is 32 For data larger than 16 and less than 32, the gamma data is calculated with the following equation: yst4+(yst4-yst3)×(data-16)/16
0x5305	YST5	0x63	RW	Bit[7:0]: Yst5 Gamma gain coefficient for data that is 40 For data larger than 32 and less than 40, the gamma data is calculated with the following equation: yst5+(yst5-yst4)×(data-32)/8
0x5306	YST6	0x6E	RW	Bit[7:0]: Yst6 Gamma gain coefficient for data that is 48 For data larger than 40 and less than 48, the gamma data is calculated with the following equation: yst6+(yst6-yst5)×(data-40)/8
0x5307	YST7	0x77	RW	Bit[7:0]: Yst7 Gamma gain coefficient for data that is 56 For data larger than 48 and less than 56, the gamma data is calculated with the following equation: yst7+(yst7-yst6)×(data-48)/8
0x5308	YST8	0x80	RW	Bit[7:0]: Yst8 Gamma gain coefficient for data which is 64 For data larger than 56 and less than 64, the gamma data is calculated with the following equation: yst8+(yst8-yst7)×(data-56)/8
0x5309	YST9	0x88	RW	Bit[7:0]: Yst9 Gamma gain coefficient for data that is 72 For data larger than 64 and less than 72, the gamma data is calculated with the following equation: yst9+(yst9-yst8)×(data-64)/8
0x530A	YST10	0x96	RW	Bit[7:0]: Yst10 Gamma gain coefficient for data that is 80 For data larger than 72 and less than 80, the gamma data is calculated with the following equation: yst10+(yst10-yst9)×(data-72)/8
0x530B	YST11	0xA3	RW	Bit[7:0]: Yst11 Gamma gain coefficient for data that is 96 For data larger than 80 and less than 96, the gamma data is calculated with the following equation: yst11+(yst11-yst10)×(data-80)/16

table 5-3 gamma registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x530C	YST12	0xAF	RW	Bit[7:0]: Yst12 Gamma gain coefficient for data that is 112 For data larger than 96 and less than 112, the gamma data is calculated with the following equation: yst12+(yst12-yst11)×(data-96)/16
0x530D	YST13	0xC5	RW	Bit[7:0]: Yst13 Gamma gain coefficient for data that is 144 For data larger than 112 and less than 144, the gamma data is calculated with the following equation: yst13+(yst13-yst12)×(data-112)/32
0x530E	YST14	0xD7	RW	Bit[7:0]: Yst14 Gamma gain coefficient for data that is 176 For data larger than 144 and less than 176, the gamma data is calculated with the following equation: yst14+(yst14-yst13)×(data-144)/32
0x530F	YST15	0xE8	RW	Bit[7:0]: Yst15 Gamma gain coefficient for data that is 208 For data larger than 176 and less than 208, the gamma data is calculated with the following equation: yst15+(yst15-yst14)×(data-176)/32
0x5310	YSLP15	0x0F	RW	Bit[7:0]: Yslp15 Manual gamma gain coefficient slope for data larger than 208 For data larger than 208, the gamma data is calculated with the following equation: yst15+yslp15×(data-208)/64

5.4 auto white balance (AWB)

The purpose of the auto white balance (AWB) block is to avoid unrealistic colors, so that objects that appear white to the human eye are rendered white in the final image or video. This image sensor supports both manual white balance and simple auto white balance.

table 5-4 AWB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[5]: awb_en AWB function enable signal 0: Disable 1: Enable Bit[4]: awbg_en AWBG function enable signal 0: Disable 1: Enable
0x5200	AWB CTRL00	0x00	RW	Bit[6]: freeze_gain_en Bit[5]: gain_man_en Bit[4]: after_gma Bit[3:0]: awb_frame_cnt
0x5201	AWB CTRL01	0x50	RW	Bit[7:6]: fast_step Bit[5:4]: locale_step Bit[3:0]: local_limit
0x5202	STABLE RANGE	0x04	RW	Bit[7:0]: stable_range[7:0] Stable range
0x5203	STABLE RANGEW	0x08	RW	Bit[7:0]: stable_rangew[7:0] Stable wide range
0x5204	RED GAIN	0x04	RW	Bit[3:0]: red_gain[11:8] MSB of manual red gain
0x5205	RED GAIN	0x00	RW	Bit[7:0]: red_gain[7:0] LSB of manual red gain
0x5206	GRN GAIN	0x04	RW	Bit[3:0]: grn_gain[11:8] MSB of manual green gain
0x5207	GRN GAIN	0x00	RW	Bit[7:0]: grn_gain[7:0] LSB of manual green gain
0x5208	BLU GAIN	0x04	RW	Bit[3:0]: blu_gain[11:8] MSB of manual blue gain
0x5209	BLU GAIN	0x00	RW	Bit[7:0]: blu_gain[7:0] LSB of manual blue gain

table 5-4 AWB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x520A	GAIN R LIMIT	0xF0	RW	Bit[7:4]: gain_r_up_limit MSB of red gain top limitation LSB is 0xFF Bit[3:0]: gain_r_dn_limit MSB of red gain bottom limitation LSB is 0x00
0x520B	GAIN G LIMIT	0xF0	RW	Bit[7:4]: gain_g_up_limit MSB of green gain top limitation LSB is 0xFF Bit[3:0]: gain_g_dn_limit MSB of green gain bottom limitation LSB is 0x00
0x520C	GAIN B LIMIT	0xF0	RW	Bit[7:4]: gain_b_up_limit MSB of blue gain top limitation LSB is 0xFF Bit[3:0]: gain_b_dn_limit MSB of blue gain bottom limitation LSB is 0x00

5.5 defect pixel cancellation (DPC)

Defect pixel correction function corrects white and black defective pixels.

table 5-5 DPC registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[3]: bc_en Black DPC function enable signal 0: Disable 1: Enable Bit[2]: wc_en White DPC function enable signal 0: Disable 1: Enable
0x5400	DPC CTRL00	0x03	RW	Bit[4]: man_en Bit[1:0]: edge_opt
0x5401	DPC CTRL01	0x0E	RW	Bit[3]: sc_en Bit[2]: dc_en Bit[1]: cross_en Bit[0]: saturate_en
0x5402	DPC CTRL02	0x32	RW	Bit[6:4]: wthre_list0 Bit[2:0]: wthre_list1
0x5403	DPC CTRL03	0x04	RW	Bit[4]: adpt_ptn Bit[3:0]: bthre_ratio
0x5404	DPC CTRL04	0x0F	RW	Bit[6:0]: gain_list
0x5405	DPC CTRL05	0x46	RW	Bit[7:4]: Thre1 Bit[3:0]: Saturate

5.6 color interpolation (CIP), DNS and sharpen

The color interpolation (CIP) functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. De-noise and edge enhancement work in both manual and auto modes.

figure 5-1 DNS_TH diagram

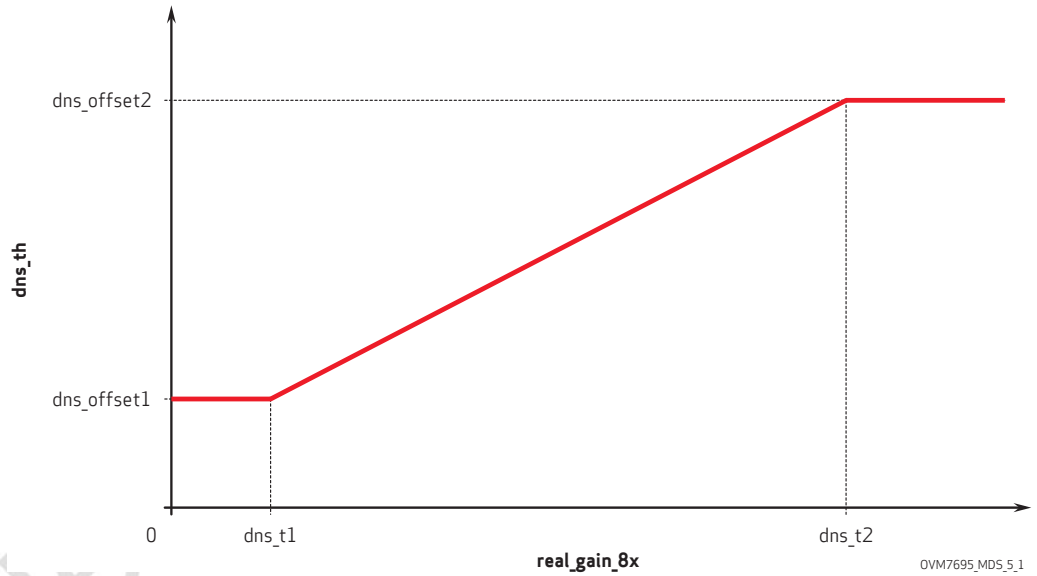


figure 5-2 sharpen_MT diagram

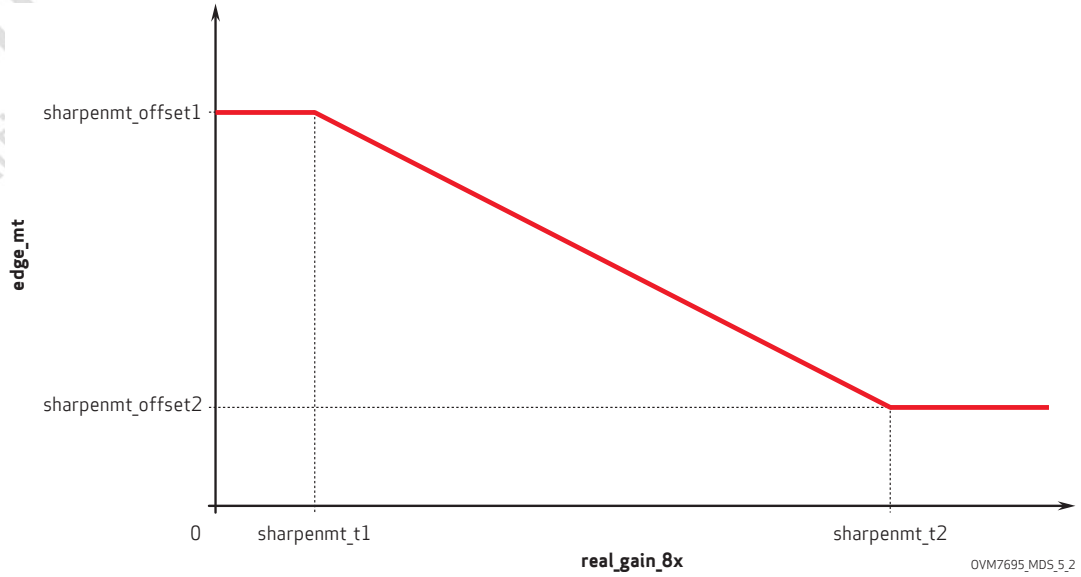


figure 5-3 sharpen_TH diagram

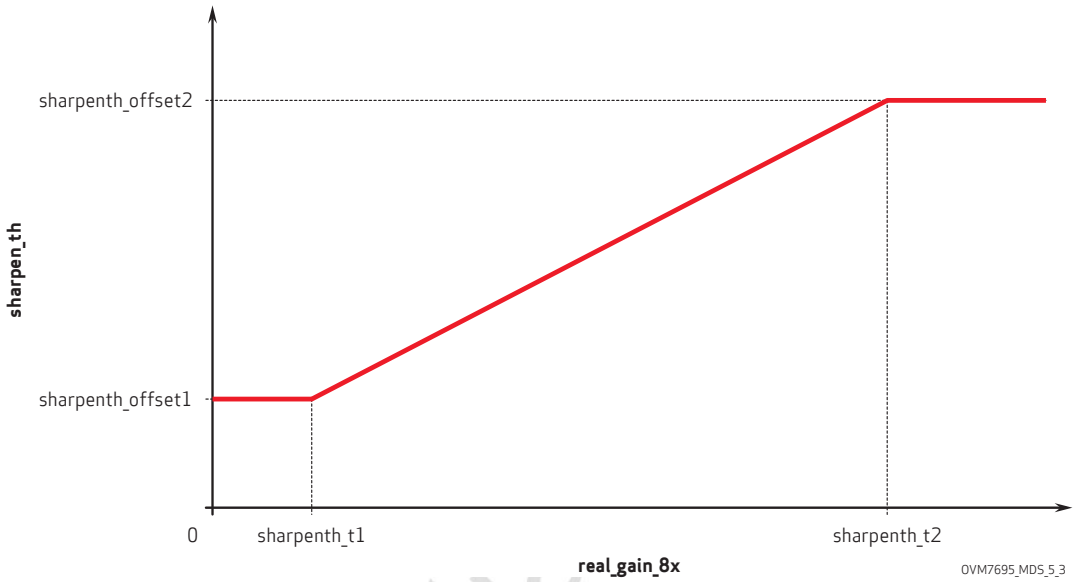


table 5-6 CIP registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x3F	RW	Bit[0]: cip_en CIP function enable signal 0: Disable 1: Enable
0x5500	SHRP MT GAIN TH1	0x08	RW	Bit[7:0]: shrp_mt_gain_th1 Sharpen strength lower gain threshold It has 3-bit precision. When the current real gain, which has 3-bit precision, is less than shrp_mt_gain_th1, the sharpen strength is shrp_mt_th1. When the current real gain, which has 3-bit precision, is greater than shrp_mt_gain_th2×4, the sharpen strength is shrp_mt_th2. When the current real gain, which has 3-bit precision, is not less than shrp_mt_gain_th1 and not greater than shrp_mt_gain_th2×4, the sharpen strength is shrp_mt_th2 + (cur-rent_real_gain_8x - shrp_mt_gain_th1) × (shrp_mt_th1-shrp_mt_th2) / (shrp_mt_gain_th2×4-shrp_mt_gain_th1)

table 5-6 CIP registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5501	SHRP MT GAIN TH2	0x48	RW	Bit[7:0]: shrp_mt_gain_th2 Sharpen strength higher gain threshold It has 1 bit precision. See shrp_mt_gain_th1 description
0x5502	SHRP MT TH1	0x18	RW	Bit[6:0]: shrp_offset1 Sharpen strength threshold for lower gain When shrp_man_en is enabled, it is shrp_mt_th_man. See shrp_mt_gain_th1 description
0x5503	SHRP MT TH2	0x0E	RW	Bit[6:0]: shrp_offset2 Sharpen strength threshold for higher gain See shrp_mt_gain_th1 description
0x5504	DNS GAIN TH1	0x08	RW	Bit[7:0]: dns_gain_th1 Denoise lower gain threshold It has 3 bit precision. When the current real gain, which has 3-bit precision, is less than dns_gain_th1, the DNS threshold is dns_th1. When the current real gain, which has 3-bit precision, is greater than dns_gain_th2×4, the DNS threshold is dns_th2. When the current real gain, which has 3-bit precision, is not less than dns_gain_th1 and not greater than dns_gain_th2×4, the DNS threshold is dns_th1 + (current_real_gain_8x - dns_gain_th1) × (dns_th2-dns_th1) / (dns_gain_th2×4-dns_gain_th1)
0x5505	DNS GAIN TH2	0x48	RW	Bit[7:0]: dns_gain_th2 Denoise higher gain threshold It has 1 bit precision. See dns_gain_th1 description
0x5506	DNS TH1	0x09	RW	Bit[6:0]: dns_offset1 Denoise threshold for lower gain When dns_man_en is enabled, it is dns_th_man. See dns_gain_th1 description
0x5507	DNS TH2	0x16	RW	Bit[6:0]: dns_offset2 Denoise threshold for higher gain See dns_gain_th1 description

table 5-6 CIP registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5508	CIP CTRL	0xAD	RW	Bit[7]: interlace_en Interlace mode enable 0: Input image is normal image 1: Input image is interlace image Bit[6]: shrp_man_en Sharpen manual mode 0: Automatic sharpen 1: Manual sharpen Bit[5]: bd_opt Boundary process enable 0: No boundary process 1: Do boundary process Bit[4]: dns_man_en Denoise manual mode enable. 0: Use automatic dns_th 1: Use manual dns_th Bit[3]: bw_mode01_sel BW mode0 and BW mode1 selection signal. 0: BW mode0 1: BW mode1 Note: In BW mode0, there is interlace mode and progressive mode. In BW mode1, there is no interlace mode and progressive mode difference Bit[2:0]: br_shrp_ctrl_th BR sharpen control threshold To adjust the weight of high frequency of chroma. The bigger threshold, the higher weight. It is commended that it cannot be adjusted
0x5509	SHRP TH GAIN TH1	0x08	RW	Bit[7:0]: shrp_th_gain_th1 Sharpen threshold lower gain threshold It has 3-bit precision. When the current real gain, which has 3-bit precision, is less than shrp_th_gain_th1, the sharpen threshold is shrp_th1. When the current real gain, which has 3-bit precision, is greater than shrp_th_gain_th2×4, the sharpen threshold is shrp_th2. When the current real gain, which has 3-bit precision, is not less than shrp_th_gain_th1 and not greater than shrp_th_gain_th2×4, the sharpen threshold is shrp_th1 + (current_real_gain_8x - shrp_th_gain_th1) × (shrp_th2-shrp_th1) / (shrp_th_gain_th2×4-shrp_th_gain_th1)

table 5-6 CIP registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x550A	SHRP TH GAIN TH2	0x48	RW	Bit[7:0]: shrp_th_gain_th2 Sharpen threshold higher gain threshold It has 1 bit precision. See shrp_th_gain_th1 description
0x550B	SHRP TH1	0x04	RW	Bit[4:0]: shrp_th1 Sharpen threshold for lower gain When the shrp_man_en is enabled, it is shrp_th_man. See shrp_th_gain_th1 description
0x550C	SHRP TH2	0x06	RW	Bit[4:0]: shrp_th2 Sharpen threshold for higher gain See shrp_th_gain_th1 description
0x550D	RECURSIVE DNS ENABLE	0x01	RW	Bit[0]: recursivedns_en Recursive denoise function enable 0: Disable 1: Enable

5.7 color matrix (CMX)

The main purpose of CMX function is to perform color correction and convert images from the RGB domain to YUV domain.

table 5-7 CMX registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x3F	RW	Bit[1]: cmx_en CMX function enable signal 0: Disable 1: Enable
0x5600	CMX CTRL	0x00	RW	Bit[1]: precision_opt Selection option for CMXxy. Both x and y are in [1, 3] 0: 1 MSB for integer gain and 7 LSBs for fraction 1: 2 MSBs for integer gain and 6 LSBs for fraction Bit[0]: uv_cbcr_en UV CbCr enable signal 0: Disable 1: Enable

table 5-7 CMX registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5601	CMX1	0x20	RW	Bit[7:0]: CMX11 Absolute value of coefficient of R for calculating Y
0x5602	CMX2	0x64	RW	Bit[7:0]: CMX12 Absolute value of coefficient of G for calculating Y
0x5603	CMX3	0x08	RW	Bit[7:0]: CMX13 Absolute value of coefficient of B for calculating Y
0x5604	CMX4	0x30	RW	Bit[7:0]: CMX21 Absolute value of coefficient of R for calculating U
0x5605	CMX5	0x90	RW	Bit[7:0]: CMX22 Absolute value of coefficient of G for calculating U
0x5606	CMX6	0xC0	RW	Bit[7:0]: CMX23 Absolute value of coefficient of B for calculating U
0x5607	CMX7	0xA0	RW	Bit[7:0]: CMX31 Absolute value of coefficient of R for calculating V
0x5608	CMX8	0x98	RW	Bit[7:0]: CMX32 Absolute value of coefficient of G for calculating V
0x5609	CMX9	0x08	RW	Bit[7:0]: CMX33 Absolute value of coefficient of B for calculating V
0x560A	CMXSIGN	0x01	RW	Bit[0]: cmx33_sign Sign bit of CMX33 0: Used coefficient is CMX33 1: Used coefficient is -1 × CMX33

table 5-7 CMX registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x560B	CMXSIGN	0x98	RW	Bit[7]: cmx32_sign Sign bit of CMX32 0: Used coefficient is CMX32 1: Used coefficient is -1 × CMX32 Bit[6]: cmx31_sign Sign bit of CMX31 0: Used coefficient is CMX31 1: Used coefficient is -1 × CMX31 Bit[5]: cmx23_sign Sign bit of CMX23 0: Used coefficient is CMX23 1: Used coefficient is -1 × CMX23 Bit[4]: cmx22_sign Sign bit of CMX22 0: Used coefficient is CMX22 1: Used coefficient is -1 × CMX22 Bit[3]: cmx21_sign Sign bit of CMX21 0: Used coefficient is CMX21 1: Used coefficient is -1 × CMX21 Bit[2]: cmx13_sign Sign bit of CMX13 0: Used coefficient is CMX13 1: Used coefficient is -1 × CMX13 Bit[1]: cmx12_sign Sign bit of CMX12 0: Used coefficient is CMX12 1: Used coefficient is -1 × CMX12 Bit[0]: cmx11_sign Sign bit of CMX11 0: Used coefficient is CMX11 1: Used coefficient is -1 × CMX11

5.8 special digital effect (SDE)

The special digital effects (SDE) functions include saturation control, brightness, contrast, etc

table 5-8 SDE registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x3F	RW	Bit[3]: sde_en SDE function enable signal 0: Disable 1: Enable
0x5800	SDE EN CTRL	0x00	RW	Bit[7]: Fix Y enable When set to 1, Y output will be a fixed value which is set in register yoffset/fixy Bit[6]: Neg enable When set to 1, output data will be a reversed value Bit[5]: Gray enable When set to 1, UV output will be a fixed value 128. Output image is black and white Bit[4]: fix_v enable When set to 1, V output will be a fixed value set in register sat_th1/fixv Bit[3]: fix_u enable When set to 1, U output will be a fixed value set in register sat_th2/fixu Bit[2]: Contrast enable Y contrast function enable signal 0: Disable 1: Enable Bit[1]: Saturation enable Color saturation function enable signal 0: Disable 1: Enable
0x5801~ 0x5802	NOT USED	–	–	Not Used
0x5803	SATURATION TH2	0x40	RW	Bit[7:0]: sat_th2 When fixu_en is enabled, it is the fixed U value When the fixu_en is 0 and uvadj_man_en is 1, it is saturation coefficient for U. When both fixu and uvadj_man_en are 0, it is the top saturation threshold to calculate the UV adjust coefficient

table 5-8 SDE registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5804	SATURATION TH1	0x00	RW	Bit[7:0]: sat_th1 When fixv_en is enabled, it is the fixed V value When fixv_en is 0 and uvadj_man_en is 1, it is saturation coefficient for V. When both fixv and uvadj_man_en are 0, it is the bottom saturation threshold to calculate the UV adjust coefficient
0x5805	Y OFFSET	0x00	RW	Bit[7:0]: Yoffset Offset coefficient for Y contrast calculation It is combined with ygain and ybright to calculate contrasted Y
0x5806	Y GAIN	0x20	RW	Bit[7:0]: Ygain Gain coefficient for Y contrast calculation It is combined with yoffset and ybright to calculate contrasted Y
0x5807	Y BRIGHT	0x00	RW	Bit[7:0]: Ybright Bright coefficient for Y contrast calculation It is combined with ygain and yoffset to calculate contrasted Y
0x5808	SIGN BITS	0x00	RW	Bit[3]: ybright_sign_bit Sign bit for ybright 0: Ybright is positive number (ybright) 1: Ybright is negative number (-1×ybright) Bit[2]: yoffset_sign_bit Sign bit for yoffset When auto offset is used, this sign bit is not used 0: Yoffset is positive number (yoffset) 1: Yoffset is negative number (-1×yoffset) Bit[1:0]: Not used Y contrast calculation equation: Yout = [Yin+ (1 - 2×ybright_sign_bit)×ybright + (2×yoffset_sign_bit - 1) × yoffset)] × ygain + (1-2×yoffset_sign_bit)×yoffset

table 5-8 SDE registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5809	UVADJ GAIN TH1	0x08	RW	Bit[7:0]: gain_th1 UV adjust curve bottom gain threshold When real gain, which has 3-bit precision, is less than gain_th1, the uv_adj is sat_th2. When real gain, which has 3-bit precision, is larger than gain_th2, the uv_adj is sat_th1. When real gain, which has 3-bit precision, is larger than gain_th1 and less than gain_th2, the uv_adj is sat_th1 + (sat_th2-sat_th1)×(gain_th2-real_gain)/(gain_th2-gain_th1)
0x580A	UVADJ GAIN TH2	0x80	RW	Bit[7:0]: gain_th2 UV adjust curve top gain threshold When real gain, which has 3-bit precision, is less than gain_th1, the uv_adj is sat_th2. When real gain, which has 3-bit precision, is larger than gain_th2, the uv_adj is sat_th1. When real gain, which has 3-bit precision, is larger than gain_th1 and less than gain_th2, the uv_adj is sat_th1 + (sat_th2-sat_th1)×(gain_th2-real_gain)/(gain_th2-gain_th1)
0x580B	UVADJ MAN EN	0x00	RW	Bit[1]: offset_man_en 0: Offset used in Y contrast is input Y average 1: Offset used in Y contrast is set in yoffset Bit[0]: uvadj_man_en UV adjust manual enable 0: Use the calculated uv_adj for UV adjust coefficient 1: Use the sat_th1 for V saturation coefficient; use the sat_th2 for U saturation coefficient

6 image sensor output interface digital functions

6.1 MIPI interface

The OVM7695 supports a single lane MIPI interface with a data transfer rate of up to 192 Mbps and supports YUV422 and RAW8 output format. MIPI provides a single uni-directional clock lane and uni-directional data lane to communicate to components in a mobile device. The data lane has full support for high speed (HS) and low power (LP) data transfer modes. Contact your local OmniVision FAE for more details.

figure 6-1 MIPI timing

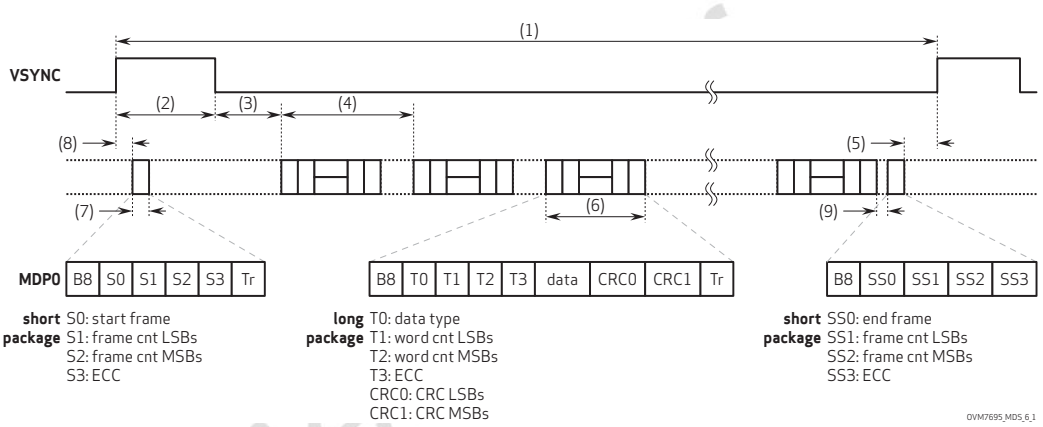


table 6-1 MIPI timing specifications

mode	timing
VGA (full) 640x480 30 fps	(1) 399,856 tps (2) 3,024 tps (3) 549,724.47 tpp (4) 11,936 tpp (5) 71865.7 tpp (6) 10,348 tpp (7) 92 tpp (8) 33.14 tpp (9) 228 tpp where tps = 1 Tsclk, tpp = 1 Tpclk = 1 UI

table 6-2 MIPI control registers

address	register name	default value	R/W	description
0x3014	MIPI CTRL0	0x00	RW	Bit[5]: mipi_phy_rst_o 1: Reset MIPI PHY High speed transmitter Bit[4]: r_phy_pd_mipi 1: Power down MIPI PHY High speed transmitter
0x301F	MIPI CTRL1	0x23	RW	Bit[5]: MIPI clock lane control 0: Clock lane hold LP00 when power down MIPI 1: Clock lane is high-z when power down MIPI Bit[0]: cen_global_o for SRAM test use
0x4800	MIPI REG0	0x0F	RW	Bit[7:0]: r_t_hs_zero Value of hs_zero, unit: 2 UI
0x4801	MIPI REG1	0x0B	RW	Bit[7:0]: r_t_da_trail Value of trailing data, unit: 2 UI
0x4802	MIPI REG2	0x0B	RW	Bit[7:0]: r_hs_exit Value of hs exit time, unit: 2 UI
0x4803	MIPI REG3	0x07	RW	Bit[7:0]: r_hs_prepare Value of hs prepare time, unit: 2 UI
0x4804	MIPI REG4	0x05	RW	Bit[7:0]: r_ck_prepare Value of clock prepare time, unit: 2 UI
0x4805	MIPI REG5	0x06	RW	Bit[7:0]: r_lpx_p Value of lpx_p time, unit: 2 UI
0x4806	MIPI REG6	0x19	RW	Bit[7:0]: r_t_ck_hs_zero Value of clock hs zero time, unit: 2 UI
0x4807	MIPI REG7	0x05	RW	Bit[3:0]: r_t_clk_pre Value of clock prepare time, unit: 2 UI
0x4808	MIPI REG8	0x21	RW	Bit[7:0]: r_t_clk_post Value of clock post time, unit: 2 UI
0x4809	MIPI REG9	0x07	RW	Bit[7:0]: r_t_clk_trail Value of clock trailing time, unit: 2 UI
0x480B	MIPI REGB	0x1E	RW	Bit[7:0]: tx_lp_data
0x480F	MIPI REGF	0x00	RW	Bit[7]: Not used Bit[6]: lp_ck_n manual control Bit[5]: lp_ck_p manual control Bit[4]: lp_n manual control Bit[3]: lp_p manual control Bit[2]: lp_tx_ck manual control Bit[1]: lp_tx_da manual control Bit[0]: lp_sel manual control

6.2 OmniVision's proprietary serial peripheral interface (SPI)

The SPI module used in the OVM7695 is based on OmniVision's proprietary SPI. It is a simplified SPI module, which is intended for internal communication among OmniVision sensors such as SPI to OV5645 or OV5648 for ViV function, and may not be compatible with an external SPI receiver. The user will need to build their own SPI receiver in order to use the OVM7695 SPI interface.

The OVM7695 supports SPI data transfer interface in master mode. In master mode, three pins are used, CSK (camera serial clock) and CSD[1:0] (camera serial data). The OVM7695 supports output formats: RAW8, RAW10, and YUV422. MIPI and SPI share the same data bus; therefore, please disable MIPI interface (0x3820[2] = 1) when using the SPI interface.

table 6-3 SPI control registers

function	register	description
bypass MIPI	0x3820	Bit[2]: Bypass MIPI interface
lane control	0x4F05	Bit[0]: SPI two lane enable 0: Disable 1: Enable
SPI control	0x4F06	Bit[0]: SPI/MIPI control 0: For SPI 1: For MIPI

6.2.1 transmission protocol

The OVM7695 SPI is used to convert parallel data coming from the upstream port to two serial data ports or one serial data port. It supports RAW8, RAW10 and YUV422 data.

The transmission protocol starts with the lowest significant bit (LSB) first.

table 6-4 SPI data sequence

data format	transfer order
RAW 8	RAW8[0]→RAW8[1]→...→RAW8[7]
RAW 10	RAW10[0]→RAW10[1]→...→RAW10[9]
YUV422	YUV422[0]→...YUV422[7]→...→YUV422[15]

7 register tables

The following tables provide descriptions of the device control registers contained in the OVM7695. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x42 for write and 0x43 for read.

7.1 general status [0x0005 - 0x006, 0x0100 - 0x0106, 0x300A - 0x300B, 0x302A]

table 7-1 general status registers (sheet 1 of 2)

address	byte	register name	default value	R/W	description
0x0005		FRAME_COUNT	0xFF	R	8-bit (0-255) Frame Counter Value
0x0006		PIXEL_ORDER	0x02	R	Color Pixel Order 0x00: GR/BG 0x01: RG/GB 0x02: BG/GR 0x03: BG/RG
0x0100		MODE_SELECT	0x00	RW	Mode Select for Software Standby 0: Sleep 1: Streaming
0x0101		IMAGE_ORIENTATION	0x00	RW	Image Orientation Bit[7:2]: Not used Bit[1]: Vertical flip enable 0: Disable 1: Enable Bit[0]: Horizontal mirror 0: Disable 1: Enable
0x0103		SOFTWARE_RESET	0x00	RW	Software Reset Setting this register to 1 resets sensor to its power up defaults. Value of this bit is also reset 0: Off 1: On
0x0104		GROUPED_ PARAMETER_HOLD	0x00	RW	Grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0: Consume as normal 1: Hold
0x0105		MASK_CORRUPTED_ FRAMES	0x00	RW	Mask Corrupted Frames 0: Allow corrupted frames 1: Mask corrupted frames

table 7-1 general status registers (sheet 2 of 2)

address	byte	register name	default value	R/W	description
0x0106		FAST_STANDBY_CTRL	0x00	RW	Fast Standby Control 0: Frame completes before mode entry 1: Frame may be truncated before mode entry
0x300A	Hi	CHIP ID	0x76	R	Sensor Chip ID High Byte
0x300B	Lo	CHIP ID	0x95	R	Sensor Chip ID Low Byte
0x302A		CHIP REVISION	0xB0/ 0xB1	R	Bit[7:0]: Chip revision number

7.2 SCCB control [0x0107, 0x303B]

table 7-2 SCCB control registers

address	register name	default value	R/W	description
0x0107	CCI_ADDRESS_PGM_ID	0x42	RW	Expressed as 8-bit SCCB Programmable ID
0x303B	CCI_ADDRESS_PGM_ID_ ENABLE	0x10	RW	Expressed as 8-bit Bit[7:5]: Not used Bit[4]: SCCB programmable ID enable Bit[3:0]: Not used

7.3 clock configuration [0x0300 - 0x030B, 0x3106]

table 7-3 clock configuration registers (sheet 1 of 2)

address	byte	register name	default value	R/W	description
0x0300 0x0301	Hi Lo	VT_PIX_CLK_DIV	0x00 0x08	RW	Video Timing Pixel Clock Divider
0x0302 0x0303	Hi Lo	VT_SYS_CLK_DIV	0x00 0x01	RW	Video Timing System Clock Divider
0x0304 0x0305	Hi Lo	PRE_PLL_CLK_DIV	0x00 0x02	RW	Pre PLL Clock Divider Value

table 7-3 clock configuration registers (sheet 2 of 2)

address	byte	register name	default value	R/W	description
0x0306	Hi	PLL_MULTIPLIER	0x00	RW	PLL Multiplier Value Bit[15]: Multiplier step by 2 enable Bit[14:9]: Not used Bit[8:0]: Multiplier
0x0307	Lo		0x40		
0x0308	Hi	DAC_CLK_DIV	0x00	RW	Output Pixel Clock Divider Bit[15:4]: Not used Bit[3:0]: Only valid at 0x2: Div by 2 0x3: Div by 3 0x4: Div by 4 0x5: Div by 5
0x0309	Lo		0x04		
0x030A	Hi	PRE_SYS_CLK_DIV	0x00	RW	Output System Clock Divider Value Bit[15:4]: Not used Bit[3:0]: Only valid at 0x1: Div by 1 0x2: Div by 2 0x4: Div by 4 0x8: Div by 8
0x030B	Lo		0x02		
0x3106		YUV_CLK_SELECT	0x92	RW	Bit[7:2]: Reserved Bit[1:0]: YUV CLK select 00: Not used 01: RAW8 / RAW10 10: YUV422 11: Not used

7.4 frame timing [0x0340 - 0x0343]

table 7-4 frame timing registers

address	byte	register name	default value	R/W	description
0x0340	Hi	FRAME_LENGTH_LINES	0x02	RW	Frame Length
0x0341	Lo		0x18		
0x0342	Hi	LINE_LENGTH_PCK	0x02	RW	Line Length
0x0343	Lo		0xEA		

7.5 image size [0x0344 - 0x034F]

table 7-5 image size registers

address	byte	register name	default value	R/W	description
0x0344	Hi	X_ADDR_START	0x00	RW	X-address of Top Left Corner of Visible Pixel Data
0x0345	Lo		0x00		
0x0346	Hi	Y_ADDR_START	0x00	RW	Y-address of Top Left Corner of Visible Pixel Data
0x0347	Lo		0x00		
0x0348	Hi	X_ADDR_END	0x02	RW	X-address of Bottom Right Corner of Visible Pixel Data
0x0349	Lo		0x7F		
0x034A	Hi	Y_ADDR_END	0x01	RW	Y-address of Bottom Right Corner of Visible Pixel Data
0x034B	Lo		0xDF		
0x034C	Hi	X_OUTPUT_SIZE	0x02	RW	Width of Image Data Output from Sensor
0x034D	Lo		0x80		
0x034E	Hi	Y_OUTPUT_SIZE	0x01	RW	Height of Image Data Output from Sensor
0x034F	Lo		0xE0		

7.6 sub-sampling [0x0380 - 0x0387, 0x3820 - 0x3821, 0x4500]

table 7-6 sub-sampling registers (sheet 1 of 2)

address	byte	register name	default value	R/W	description
0x0380	Hi	X_EVEN_INC	0x00	RW	Increment for Even Pixels - 0, 2, 4, etc.
0x0381	Lo		0x01		
0x0382	Hi	X_ODD_INC	0x00	RW	Increment for Odd Pixels - 1, 3, 5, etc.
0x0383	Lo		0x01		
0x0384	Hi	Y_EVEN_INC	0x00	RW	0, 2, 4, etc.
0x0385	Lo		0x01		
0x0386	Hi	Y_ODD_INC	0x00	RW	1, 3, 5, etc.
0x0387	Lo		0x01		

table 7-6 sub-sampling registers (sheet 2 of 2)

address	byte	register name	default value	R/W	description
0x3820		V_BIN_CONTROL	0x90	RW	Bit[7:3]: Not used Bit[2]: Bypass MIPI Bit[1]: Vertical binning enable Bit[0]: Not used
0x3821		H_BIN_CONTROL	0x00	RW	Bit[7:1]: Not used Bit[0]: Horizontal binning enable
0x4500		X_SUB_CONTROL	0x25	RW	Bit[7:2]: Not used Bit[1]: X sub control 0: Full resolution or cropping 1: Horizontal sub-sample at any scale Bit[0]: Not used

7.7 gain/exposure control [0x3500 - 0x3503, 0x350A - 0x350B]

table 7-7 gain/exposure control registers

address	byte	register name	default value	R/W	description
0x3500	Hi	EXPO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Expo[15:12] Manual exposure control value
0x3501	Mi	EXPO	0x02	RW	Bit[7:0]: Expo[11:4] Manual exposure control value
0x3502	Lo	EXPO	0x00	RW	Bit[7:4]: Expo[3:0] Manual exposure control value Bit[3:0]: Not used
0x3503		GAIN_EXPO_CTRL	0x00	RW	Bit[7]: Digital gain manual control enable Bit[6]: Not used Bit[5:4]: Digital gain manual control value Bit[3:2]: Not used Bit[1]: Manual gain control enable Bit[0]: Manual exposure control enable
0x350A	Hi	GAIN	0x00	RW	Bit[7:1]: Not used Bit[0]: Gain[8] Manual gain control value
0x350B	Lo	GAIN	0x00	RW	Bit[7:0]: Gain[7:0] Manual gain control value

7.8 IO control [0x3001 - 0x3002, 3005, 3038]

table 7-8 IO control registers

address	register name	default value	R/W	description
0x3001	OUTPUT DRIVE CAPABILITY CTRL	0x1A	RW	Input/Output Control for SPI/MIPI Bit[7:4]: Not used Bit[3:2]: Output drive capability for SPI IO 00: 0.75x 01: 1.75x 10: 2.75x 11: 3.75x Bit[1:0]: Output drive capability for FSIN 00: 0.25x 01: 0.75x 10: 1.25x 11: 1.75x
0x3002	FSIN OEN	0x08	RW	Bit[7:1]: Not used Bit[0]: Input/output control for FSIN 0: Input 1: Output
0x3005	IO Y OEN	0x00	RW	Input/Output Control for SPI/MIPI Bit[7:4]: Not used Bit[3]: SPI_SCK shared with MCP Bit[2]: MDN Bit[1]: SPI_SDA1 shared with MDP Bit[0]: SPI_SDA0 shared with MDN
0x3038	FSIN IN SEL	0x00	RW	Bit[7:5]: Not used Bit[4]: Input selection for FSIN_IN 0: FSIN_IN through FSIN 1: FSIN_IN through MDP Bit[3:0]: Not used

7.9 frame control [0x4201 - 0x4202]

table 7-9 frame control registers

address	register name	default value	R/W	description
0x4201	FC CTRL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Number of frame on
0x4202	FC CTRL2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Number of frame off

7.10 output data clipping [0x4302 - 0x430D]

table 7-10 output data clipping registers

address	register name	default value	R/W	description
0x4302	YMAX	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Ymax[9:8] Ymax high byte
0x4303	YMAX	0xFF	RW	Bit[7:0]: Ymax[7:0] Ymax low byte
0x4304	YMIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Ymin[9:8] Ymin high byte
0x4305	YMIN	0x00	RW	Bit[7:0]: Ymin[7:0] Ymin low byte
0x4306	UMAX	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Umax[9:8] Umax high byte
0x4307	UMAX	0xFF	RW	Bit[7:0]: Umax[7:0] Umax low byte
0x4308	UMIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Umin[9:8] Umin high byte
0x4309	UMIN	0x00	RW	Bit[7:0]: Umin[7:0] Umin low byte
0x430A	VMAX	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Vmax[9:8] Vmax high byte
0x430B	VMAX	0xFF	RW	Bit[7:0]: Vmax[7:0] Vmax low byte
0x430C	VMIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Vmin[9:8] Vmin high byte
0x430D	VMIN	0x00	RW	Bit[7:0]: Vmin[7:0] Vmin low byte

7.11 output format control [0x4300]

table 7-11 output format control register

address	register name	default value	R/W	description
0x4300	FMT CTRL	0x3F	RW	Output Format Control 0x3F: YUV422 0xF8: RAW8/RAW10

7.12 MIPI control [0x3014, 0x301F, 0x4800 - 0x480F]

table 7-12 MIPI control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3014	MIPI CTRL0	0x00	RW	Bit[7:6]: Not used Bit[5]: mipi_phy_rst_o 0: Not used 1: Reset MIPI PHY high speed transmitter Bit[4]: r_phy_pd_mipi 0: Not used 1: Power down MIPI PHY high speed transmitter Bit[3:0]: Not used
0x301F	MIPI CTRL1	0x23	RW	Bit[7:6]: Not used Bit[5]: MIPI clock lane control 0: Clock lane hold LP00 when power down MIPI 1: Clock lane is high-z when power down MIPI Bit[4:1]: Not used Bit[0]: cen_global_o for SRAM test use
0x4800	MIPI REG0	0x0F	RW	Bit[7:0]: r_t_hs_zero Value of hs_zero, unit: 2 UI
0x4801	MIPI REG1	0x0B	RW	Bit[7:0]: r_t_da_trail Value of trailing data, unit: 2 UI
0x4802	MIPI REG2	0x0B	RW	Bit[7:0]: r_hs_exit Value of hs exit time, unit: 2 UI
0x4803	MIPI REG3	0x07	RW	Bit[7:0]: r_hs_prepare Value of hs prepare time, unit: 2 UI
0x4804	MIPI REG4	0x05	RW	Bit[7:0]: r_ck_prepare Value of clock prepare time, unit: 2 UI

table 7-12 MIPI control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4805	MIPI REG5	0x06	RW	Bit[7:0]: r_lpx_p Value of lpx_p time, unit: 2 UI
0x4806	MIPI REG6	0x19	RW	Bit[7:0]: r_t_ck_hs_zero Value of clock hs_zero time, unit: 2 UI
0x4807	MIPI REG7	0x05	RW	Bit[7:4]: Not used Bit[3:0]: r_t_clk_pre Value of clock prepare time, unit: 2 UI
0x4808	MIPI REG8	0x21	RW	Bit[7:0]: r_t_clk_post Value of clock post time, unit: 2 UI
0x4809	MIPI REG9	0x07	RW	Bit[7:0]: r_t_clk_trail Value of clock trailing time, unit: 2 UI
0x480B	MIPI REGB	0x1E	RW	Bit[7:0]: tx_lp_data
0x480F	MIPI REGF	0x00	RW	Bit[7]: Not used Bit[6]: lp_ck_n manual control Bit[5]: lp_ck_p manual control Bit[4]: lp_n manual control Bit[3]: lp_p manual control Bit[2]: lp_tx_ck manual control Bit[1]: lp_tx_da manual control Bit[0]: lp_sel manual control

7.13 SPI control [0x3820, 0x4F05 - 0x4F06]

table 7-13 SPI control registers

address	register name	default value	R/W	description
0x3820	VBIN CONTROL	0x90	RW	Bit[7:3]: Not used Bit[2]: Bypass MIPI Bit[1]: Vertical binning enable Bit[0]: Not used
0x4F05	SPI CTRL1	0x80	RW	Bit[7:1]: Not used Bit[0]: SPI two lane enable 0: Disable 1: Enable
0x4F06	SPI CTRL2	0x03	RW	Bit[7:1]: Not used Bit[0]: SPI/MIPI control 0: For SPI 1: For MIPI

7.14 test pattern [0x0600 - 0x0609]

table 7-14 test pattern registers

address	byte	register name	default value	R/W	description
0x0600	Hi	TEST_PATTERN_MODE	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Test pattern control 000: No pattern 001: Solid color 100: PN9 Others: Undefined
0x0601	Lo		0x00		
0x0602	Hi	TEST_DATA_RED	0x00	RW	Bit[15:10]: Not used Bit[9:0]: Test data value which is used to replace red pixel data
0x0603	Lo		0x00		
0x0604	Hi	TEST_DATA_GR	0x00	RW	Bit[15:10]: Not used Bit[9:0]: Test data value which is used to replace green pixel on rows that also have red pixels
0x0605	Lo		0x00		
0x0606	Hi	TEST_DATA_BLUE	0x00	RW	Bit[15:10]: Not used Bit[9:0]: Test data value which is used to replace blue pixel data
0x0607	Lo		0x00		
0x0608	Hi	TEST_DATA_GB	0x00	RW	Bit[15:10]: Not used Bit[9:0]: Test data value which is used to replace green pixel on rows that also have blue pixels
0x0609	Lo		0x00		

7.15 AEC control [0x3A00 - 0x3A62]

table 7-15 AEC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3A00	AEC CTRL0	0x78	RW	Bit[7:6]: Not used Bit[5]: band_en Bit[4]: less_1_band_en Bit[3]: start_sel Bit[2]: night_mode Bit[1]: new_bal Bit[0]: Freeze

table 7-15 AEC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3A01	MIN EXPO	0x04	RW	Bit[7:0]: min_expo[7:0]
0x3A02	MAX EXPO 60	0x02	RW	Bit[7:0]: max_expo_60[15:8]
0x3A03	MAX EXPO 60	0x14	RW	Bit[7:0]: max_expo_60[7:0]
0x3A05	AEC CTRL5	0x30	RW	Bit[7]: f50_reverse Bit[6]: frame_insert Bit[5]: step_auto_en Bit[4:0]: step_auto_ratio
0x3A06	AEC CTRL6	0x10	RW	Bit[7:5]: r_aec_ctrl6[7:5] Bit[4:0]: step_man1
0x3A07	AEC CTRL7	0x18	RW	Bit[7:4]: step_man2 Bit[3:0]: step_man3
0x3A08	B50 STEP	0x00	RW	Bit[7:2]: Not used Bit[1:0]: b50_step[9:8]
0x3A09	B50 STEP	0xA0	RW	Bit[7:0]: b50_step[7:0]
0x3A0A	B60 STEP	0x00	RW	Bit[7:2]: Not used Bit[1:0]: b60_step[9:8]
0x3A0B	B60 STEP	0x86	RW	Bit[7:0]: b60_step[7:0]
0x3A0C	AEC CTRL0C	0xE4	RW	Bit[7:4]: e1_max Bit[3:0]: e1_min
0x3A0D	B60 MAX	0x03	RW	Bit[7:6]: Not used Bit[5:0]: b60_max[5:0]
0x3A0E	B50 MAX	0x03	RW	Bit[7:6]: Not used Bit[5:0]: b50_max[5:0]
0x3A0F	WPT	0x78	RW	Bit[7:0]: Wpt[7:0]
0x3A10	BPT	0x68	RW	Bit[7:0]: Bpt[7:0]
0x3A11	VPT HIGH	0xD0	RW	Bit[7:0]: vpt_high[7:0]
0x3A13	AEC CTRL13	0x90	RW	Bit[7]: pre_gain_en Bit[6:0]: pre_gain
0x3A14	MAX EXPO 50	0x02	RW	Bit[7:0]: max_expo_50[15:8]
0x3A15	MAX EXPO 50	0x14	RW	Bit[7:0]: max_expo_50[7:0]
0x3A17	GNIGHT THRE	0x01	RW	Bit[7:2]: Not used Bit[1:0]: gnight_thre[1:0]
0x3A18	GAIN CEIL	0x03	RW	Bit[7:3]: Not used Bit[2:0]: gain_ceil[10:8]
0x3A19	GAIN CEIL	0xE0	RW	Bit[7:0]: gain_ceil[7:0]

table 7-15 AEC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3A1A	R DIFF MIN I	0x06	RW	Bit[7:0]: r_diff_min_i
0x3A1B	WPT2	0x78	RW	Bit[7:0]: Wpt2[7:0]
0x3A1C	R LED ADD ROW	0x06	RW	Bit[7:0]: r_led_add_row[15:8]
0x3A1D	R LED ADD ROW	0x18	RW	Bit[7:0]: r_led_add_row[7:0]
0x3A1E	BPT2	0x68	RW	Bit[7:0]: Bpt2[7:0]
0x3A1F	VPT LOW	0x40	RW	Bit[7:0]: vpt_low[7:0]
0x3A20	AEC CTRL1C	0x20	RW	Bit[7]: blc_en Bit[6:3]: BLC Bit[2]: stb_opt Bit[1]: man_avg_en Bit[0]: expo_nochange_en
0x3A21	AEC CTRL21	0x72	RW	Bit[7]: Not used Bit[6:4]: f_insert_num Bit[3:2]: Not used Bit[1]: new_vts_en Bit[0]: gain_adj_opt
0x3A25	AEC CTRL25	0x00	RW	Bit[7:5]: Not used Bit[4:2]: freeze_cnt Bit[1]: frac_constrain Bit[0]: same_step_auto
0x3A26	EXPO LINE	0x02	RW	Bit[7:0]: expo_line[7:0]
0x3A50	AVERAGE	–	R	Bit[7:0]: Average[7:0]
0x3A51	CURR STATE	–	R	Bit[7:2]: Not used Bit[1:0]: curr_state[1:0]
0x3A52	AEC CTRL52	–	R	Bit[7:3]: Not used Bit[2]: inc_cur Bit[1]: dec_cur Bit[0]: bal_cur
0x3A53	AEC CTRL53	–	R	Bit[7:6]: Not used Bit[5]: aec_update Bit[4]: Ch Bit[3]: Ch3 Bit[2]: Ch2 Bit[1]: Ch1 Bit[0]: Ch0
0x3A54	STEP	–	R	Bit[7:4]: Not used Bit[3:0]: Step[11:8]
0x3A55	STEP	–	R	Bit[7:0]: Step[7:0]
0x3A56	E TMP	–	R	Bit[7:0]: e_tmp[31:24]

table 7-15 AEC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3A57	E TMP	–	R	Bit[7:0]: e_tmp[23:16]
0x3A58	E TMP	–	R	Bit[7:0]: e_tmp[15:8]
0x3A59	E TMP	–	R	Bit[7:0]: e_tmp[7:0]
0x3A5A	E TMP PG	–	R	Bit[7:0]: e_tmp_pg[31:24]
0x3A5B	E TMP PG	–	R	Bit[7:0]: e_tmp_pg[23:16]
0x3A5C	E TMP PG	–	R	Bit[7:0]: e_tmp_pg[15:8]
0x3A5D	E TMP PG	–	R	Bit[7:0]: e_tmp_pg[7:0]
0x3A5E	AEC VTS	–	R	Bit[7:0]: aec_vts[15:8]
0x3A5F	AEC VTS	–	R	Bit[7:0]: aec_vts[7:0]
0x3A60	AEC CTRL60	–	R	Bit[7:2]: Not used Bit[1]: f_5060_new Bit[0]: f_5060
0x3A61	MAX 1FRAME	–	R	Bit[7:5]: Not used Bit[4:0]: max_1frame[12:8]
0x3A62	MAX 1FRAME	–	R	Bit[7:0]: max_1frame[7:0]

7.16 BLC control [0x4000 - 0x400B]

table 7-16 BLC control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x01	RW	Bit[7:4]: avg_weight Weight of current offsets for weight avg Bit[3]: target_adj_dis Target adjustment function disable 0: Enable function 1: Disable function Bit[2]: cmp_en Offset gain compensation function enable 0: Disable 1: Enable Bit[1]: dither_en Dither function enable 0: Disable 1: Enable Bit[0]: mf_en Median filter function enable 0: Disable 1: Enable
0x4001	BLC CTRL01	0x00	RW	Bit[7:5]: Not used Bit[4]: off_man_en Manual offset enable 0: Applied offsets are calculated offsets 1: Applied offsets are manual offsets, which are set in OFF MAN registers Bit[3]: Not used Bit[2]: blk_ln_out_en Black line output enable 0: Do not output black lines 1: Output black lines Bit[1:0]: byp_mode Data bypass mode 00: Output data is limited input data 01: Output data is input data LSBs 1x: Output data is input data MSBs
0x4002	BLK LVL TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blk_lvl_target[9:8] High byte of black level target
0x4003	BLK LVL TARGET	0x10	RW	Bit[7:0]: blk_lvl_target[7:0] Low byte of black level target
0x4004	HWIN OFF	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hwin_off[9:8] High byte of horizontal window offset

table 7-16 BLC control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4005	HWIN OFF	0x02	RW	Bit[7:0]: hwin_off[7:0] Low byte of horizontal window offset
0x4006	HWIN PAD	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hwin_pad[9:8] High byte of horizontal window pad
0x4007	HWIN PAD	0x02	RW	Bit[7:0]: hwin_pad[7:0] Low byte of horizontal window pad
0x4008	BLC CTRL08	0x00	RW	Bit[7:0]: bl_start Start line of used black lines
0x4009	BLC CTRL09	0x0B	RW	Bit[7:0]: bl_end End line of used black lines
0x400A	OFF LIM TH	0x02	RW	Bit[7:3]: Not used Bit[2:0]: off_lim_th[10:8] High byte of offset limitation threshold
0x400B	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0] Low byte of offset limitation threshold

table 7-16 BLC control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4010	BLC CTRL10	0xF0	RW	Bit[7]: off_trig_en Offset trigger enable 0: Disable 1: Enable Bit[6]: gain_chg_trig_en Gain change trigger enable 0: Disable 1: Enable Bit[5]: fmt_chg_trig_en Format trigger enable 0: Disable 1: Enable Bit[4]: rst_trig_en Reset trigger enable 0: Disable 1: Enable Bit[3]: man_avg_en Manual trigger average enable 0: Update 1: Avg Bit[2]: man_trig Manual trigger enable 0: Disable 1: Enable Bit[1]: off_frz_en Offset freeze enable. It has highest priority 0: Disable 1: Enable Bit[0]: off_always_up Offset always update enable. It has second priority 0: Disable 1: Enable

table 7-16 BLC control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x4011	BLC CTRL11	0x00	RW	Bit[7]: off_chg_mf_en Offset change multi-frame trigger enable Bit[6]: Not used Bit[5]: fmt_chg_mf_en Format change multi-frame trigger enable Bit[4]: gain_chg_mf_en Gain change multi-frame trigger enable Bit[3]: rst_mf_mode Reset multi-frame trig mode 0: Update 1: Average Bit[2]: off_chg_mf_mode Offset change multi-frame trigger mode 0: Update 1: Average Bit[1]: fmt_chg_mf_mode Format change multi-frame trigger mode 0: Update 1: Average Bit[0]: gain_chg_mf_mode Gain change multi-frame trigger mode 0: Update 1: Average
0x4012	BLC CTRL12	0x08	RW	Bit[7:6]: Not used Bit[5:0]: rst_trig_fn Frame number of reset multi-frame trigger
0x4013	BLC CTRL13	0x00	RW	Bit[7:6]: Not used Bit[5:0]: fmt_trig_fn Frame number of format change multi-frame trigger
0x4014	BLC CTRL14	0x00	RW	Bit[7:6]: Not used Bit[5:0]: gain_trig_fn Frame number of gain change multi-frame trigger
0x4015	BLC CTRL15	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_trig_fn Frame number of offset change multi-frame trigger
0x4016	OFF TRIG TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_trig_th[9:8] High byte of offset trigger threshold
0x4017	OFF TRIG TH	0x04	RW	Bit[7:0]: off_trig_th[7:0] Low byte of offset trigger threshold

table 7-16 BLC control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x4020	OFF CMP TH00	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_th000 Offset gain compensation threshold for B channel
0x4021	OFF CMP TH00	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_k000 Offset gain compensation slope for B channel
0x4022	OFF CMP TH01	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_th001 Offset gain compensation threshold for Gb channel
0x4023	OFF CMP TH01	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_k001 Offset gain compensation slope for Gb channel
0x4024	OFF CMP TH10	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_th010 Offset gain compensation threshold for Gr channel
0x4025	OFF CMP TH10	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_k010 Offset gain compensation slope for Gr channel
0x4026	OFF CMP TH11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_th011 Offset gain compensation threshold for R channel
0x4027	OFF CMP TH11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_cmp_k011 Offset gain compensation slope for R channel
0x4030	OFF MAN000	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man000[9:8] High byte of manual offset for B channel
0x4031	OFF MAN000	0x00	RW	Bit[7:0]: off_man000[7:0] Low byte of manual offset for B channel
0x4032	OFF MAN001	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man001[9:8] High byte of manual offset for Gb channel
0x4033	OFF MAN001	0x00	RW	Bit[7:0]: off_man001[7:0] Low byte of manual offset for Gb channel

table 7-16 BLC control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x4034	OFF MAN010	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man010[9:8] High byte of manual offset for Gr channel
0x4035	OFF MAN010	0x00	RW	Bit[7:0]: off_man010[7:0] Low byte of manual offset for Gr channel
0x4036	OFF MAN011	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man011[9:8] High byte of manual offset for R channel
0x4037	OFF MAN011	0x00	RW	Bit[7:0]: off_man011[7:0] Low byte of manual offset for R channel
0x4040	BLC OFFSET000	–	R	Bit[7:2]: Not used Bit[1:0]: off_man000[9:8] High byte of offset for B channel
0x4041	BLC OFFSET000	–	R	Bit[7:0]: off_man000[7:0] Low byte of offset for B channel
0x4042	BLC OFFSET001	–	R	Bit[7:2]: Not used Bit[1:0]: off_man001[9:8] High byte of offset for Gb channel
0x4043	BLC OFFSET001	–	R	Bit[7:0]: off_man001[7:0] Low byte of offset for Gb channel
0x4044	BLC OFFSET010	–	R	Bit[7:2]: Not used Bit[1:0]: off_man010[9:8] High byte of offset for Gr channel
0x4045	BLC OFFSET010	–	R	Bit[7:0]: off_man010[7:0] Low byte of offset for Gr channel
0x4046	BLC OFFSET011	–	R	Bit[7:2]: Not used Bit[1:0]: off_man011[9:8] High byte of offset for R channel
0x4047	BLC OFFSET011	–	R	Bit[7:0]: off_man011[7:0] Low byte of offset for R channel

7.17 ISP control [0x5000 - 0x500E]

table 7-17 ISP control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFF	RW	Bit[7]: cip_en CIP function enable signal 0: Disable CIP module 1: Enable CIP module Bit[6]: gamma_en Gamma function enable signal 0: Disable gamma module 1: Enable gamma module Bit[5]: awb_en AWB function enable signal 0: Disable AWB module 1: Enable AWB module Bit[4]: awbg_en AWBG function enable signal 0: Disable AWB_GAIN module 1: Enable AWB_GAIN module Bit[3]: bc_en Black DPC function enable signal 0: Disable black DPC module 1: Enable black DPC module Bit[2]: wc_en White DPC function enable signal 0: Disable white DPC module 1: Enable white DPC module Bit[1]: lenc_en LENC function enable signal 0: Disable LENC module 1: Enable LENC module Bit[0]: isp_en ISP functions enable signal, not including BLC and DGC modules 0: Disable ISP module 1: Enable ISP module

table 7-17 ISP control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x3F	RW	Bit[7:6]: Reserved Bit[5]: Avg_en Avg function enable signal 0: Disable avg module 1: Enable avg module Bit[4]: blc_en BLC function enable signal 0: Disable BLC module 1: Enable BLC module Bit[3]: SDE_en SDE function enable signal 0: Disable SDE module 1: Enable SDE module Bit[2]: uv_avg_en uv_avg_en function enable signal 0: Disable uv_avg_en module 1: Enable uv_avg_en module Bit[1]: CMX_en CMX function enable signal 0: Disable CMX module 1: Enable CMX module Bit[0]: CIP_en CIP function enable signal 0: Disable CIP module 1: Enable CIP module

table 7-17 ISP control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5002	ISP CTRL02	0x88	RW	Bit[7:6]: avg_sel AVG input data select 00: Input data from WINC module 01: Input data from LENC module 10: Input data from DPC module 11: Input data from CMX module Bit[5]: isp_eof_sel EOF signal select 0: Signal from ISP module 1: Signal from timing control module Bit[4]: isp_sof_sel SOF signal select 0: Signal from ISP module 1: Signal from timing control module Bit[3]: lenc_bias_plus 0: Bias plus option is disabled in LENC 1: Bias plus option is enabled in LENC Bit[2]: lcdc_bf_awbg LCD correction module location option 0: LCDC is after gamma 1: LCDC is before AWBG Bit[1]: F5060 Manual 50Hz or 60Hz frequency 0: 60Hz 1: 50Hz Bit[0]: raw_aft_cip When the sensor outputs in RAW image format, this option selects RAW output source 0: Output RAW after DPC 1: Output RAW after CIP DNS
0x5003	ISP CTRL03	0x00	RW	Bit[7]: dns_opt Bit[6]: bl_rblue_rvs Black line Rblue reverse signal Bit[5]: gfirst_rvs Reverse signal of GFirst Bit[4]: rblue_rvs Normal image Rblue reverse signal Bit[3]: isp_raw_en Option used in pre ISP Bit[2:0]: win_yoff_adj Option used in pre ISP
0x5004	ISP CTRL04	0x40	RW	Bit[7:0]: bcc_red_gain Gain for LCDC module red channel. It has 6 fractions
0x5005	ISP CTRL05	0x40	RW	Bit[7:0]: bcc_grn_gain Gain for LCDC module green channel. It has 6 fractions

table 7-17 ISP control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5006	ISP CTRL06	0x40	RW	Bit[7:0]: bcc_blu_gain Gain for LCDC module blue channel. It has 6 fractions
0x5007	ISP CTRL07	0x07	RW	Bit[7]: gamma_bias_man_en Manual enable signal for gamma bias Bit[6]: bcc_bias_man_en Manual enable signal for LCDC bias Bit[5]: awb_bias_man_en Manual enable signal for AWB bias Bit[4]: lenc_bias_man_en Manual enable signal for LENC bias Bit[3]: gamma_bias_en Enable signal for gamma bias Bit[2]: bcc_bias_en Enable signal for LCDC bias Bit[1]: awb_bias_en Enable signal for AWB bias Bit[0]: lenc_bias_en Enable signal for LENC bias
0x5008	ISP CTRL08	0x10	RW	Bit[7:0]: bias_man Manual bias used in gamma, LCDC, AWB and LENC modules
0x5009	ISP CTRL09	0x00	RW	Bit[7:2]: Not used Bit[1]: sram_test_cip Bit[0]: sram_test_dpc
0x500A	ISP CTRL0A	0xAA	RW	Bit[7:4]: sram_rm_cip Bit[3:0]: sram_rm_dpc
0x500E	ISP CTRL0E	0x00	RW	Bit[7]: sram_rst_scalup2 Bit[6]: sram_rst_scalup1 Bit[5]: sram_rst_scalup0 Bit[4]: sram_rst_awb Bit[3]: sram_rst_cip2 Bit[2]: sram_rst_cip1 Bit[1]: sram_rst_cip0 Bit[0]: sram_rst_dpc

7.18 pre ISP [0x5080 - 0x50A5]

table 7-18 pre ISP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5080	PRE ISP CTRL00	0x00	RW	Bit[7]: test_en 0: Disable test function 1: Enable test function Bit[6]: rolling_bar_en 0: Disable rolling bar function 1: Enable rolling bar function Bit[5]: transparent_en 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: square_mode 0: Color square 1: Black-white square Bit[3:2]: color_bar_style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: test_mode 00: Color bar 01: Random data 10: Square 11: Black image
0x5081	PRE ISP CTRL01	0x41	RW	Bit[7]: Not used Bit[6]: win_cut_en 0: Do not cut the redundant pixels 1: Cut the redundant pixels Bit[5]: two_lsb_0_en When set, two LSB of output date are 0 Bit[4]: random_rest When set, the seed used to generate the random data is the same as set in the seed register Bit[3:0]: random_seed Seed used in generating random data
0x5082	PRE ISP CTRL02	0x00	RW	Bit[7:0]: line_number[15:8]
0x5083	PRE ISP CTRL03	0x01	RW	Bit[7:0]: line_number[7:0]
0x5084	PRE ISP CTRL04	0x00	RW	Bit[7:0]: scale_x_input_manual_size[15:8]
0x5085	PRE ISP CTRL05	0x00	RW	Bit[7:0]: scale_x_input_manual_size[7:0]
0x5086	PRE ISP CTRL06	0x01	RW	Bit[7:0]: scale_y_input_manual_size[15:8]
0x5087	PRE ISP CTRL07	0x00	RW	Bit[7:0]: scale_y_input_manual_size[7:0]

table 7-18 pre ISP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5088	PRE ISP CTRL08	0x00	RW	Bit[7:0]: x_manual_offset[15:8]
0x5089	PRE ISP CTRL09	0x00	RW	Bit[7:0]: x_manual_offset[7:0]
0x508A	PRE ISP CTRL10	0x00	RW	Bit[7:0]: y_manual_offset[15:8]
0x508B	PRE ISP CTRL11	0x00	RW	Bit[7:0]: y_manual_offset[7:0]
0x5090	PRE ISP CTRL16	0x0C	RW	Bit[7:6]: Not used Bit[5]: mirror_opt Mirror option for x offset Bit[4]: flip_opt Flip option for y offset Bit[3]: mirror_order Mirror order, bg or gb Bit[2]: flip_order Flip order, br or rb Bit[1]: offset_man_en Offset manual enable Bit[0]: scale_man
0x5091	PRE ISP CTRL17	0x00	RW	Bit[7]: dmy_man_en Dummy line manual mode Bit[6:4]: dmy_ln_num Bit[3]: dmy_blk_half Bit[2:0]: dmy_man_ration
0x508C	PRE ISP CTRL12	–	R	Bit[7:0]: pixel_number[15:8]
0x508D	PRE ISP CTRL13	–	R	Bit[7:0]: pixel_number[7:0]
0x508E	PRE ISP CTRL14	–	R	Bit[7:0]: line_number[15:8]
0x508F	PRE ISP CTRL15	–	R	Bit[7:0]: line_number[7:0]
0x5097	PRE ISP CTRL23	–	R	Bit[7:4]: x_odd_inc Bit[3:0]: y_odd_inc
0x5098	PRE ISP CTRL24	–	R	Bit[7:0]: x_offset[15:8]
0x5099	PRE ISP CTRL25	–	R	Bit[7:0]: x_offset[7:0]
0x509A	PRE ISP CTRL26	–	R	Bit[7:0]: y_offset[15:8]
0x509B	PRE ISP CTRL27	–	R	Bit[7:0]: y_offset[7:0]
0x509C	PRE ISP CTRL28	–	R	Bit[7:0]: win_x_offset[15:8]
0x509D	PRE ISP CTRL29	–	R	Bit[7:0]: win_x_offset[7:0]
0x509E	PRE ISP CTRL30	–	R	Bit[7:0]: win_y_offset[15:8]
0x509F	PRE ISP CTRL31	–	R	Bit[7:0]: win_y_offset[7:0]
0x50A0	PRE ISP CTRL32	–	R	Bit[7:0]: win_x_output_size[15:8]

table 7-18 pre ISP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x50A1	PRE ISP CTRL33	–	R	Bit[7:0]: win_x_output_size[7:0]
0x50A2	PRE ISP CTRL34	–	R	Bit[7:0]: win_y_output_size[15:8]
0x50A3	PRE ISP CTRL35	–	R	Bit[7:0]: win_y_output_size[7:0]
0x50A4	PRE ISP CTRL36	–	R	Bit[7:6]: Not used Bit[5:4]: x_skip Bit[3:2]: Not used Bit[1:0]: y_skip
0x50A5	PRE ISP CTRL37	–	R	Bit[7:4]: x_even_inc Bit[3:0]: y_even_inc

7.19 LENC control [0x5100 - 0x5118]

table 7-19 LENC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5100	RED X0	0x01	RW	Bit[7:2]: Not used Bit[1:0]: red_x0[9:8] High byte of horizontal center position of red channel
0x5101	RED X0	0x48	RW	Bit[7:0]: red_x0[7:0] Low byte of horizontal center position of red channel
0x5102	RED Y0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: red_y0[9:8] High byte of vertical center position of red channel
0x5103	RED Y0	0xF8	RW	Bit[7:0]: red_y0[7:0] Low byte of vertical center position of red channel
0x5104	RED A1	0x22	RW	Bit[7]: Not used Bit[6:0]: red_a1 Gain coefficient for the square distance of current red pixel position and red center
0x5105	RED A2	0x07	RW	Bit[7:4]: Not used Bit[3:0]: red_a2 Precision gain coefficient for the square distance of current red pixel position and red center

table 7-19 LENC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5106	RED B1	0xC2	RW	Bit[7]: Sign bit of red_b1 Bit[6:0]: red_b1 Gain coefficient for the distance of current red pixel position and red center
0x5107	RED B2	0x08	RW	Bit[7:4]: Not used Bit[3:0]: red_b2 Precision gain coefficient for the distance of current red pixel position and red center. Gain of current red pixel is defined with the distance (r), red_a1, red_a2, red_b1 and red_b2.
0x5108	GRN X0	0x01	RW	Bit[7:2]: Not used Bit[1:0]: grn_x0[9:8] High byte of horizontal center position of green channel
0x5109	GRN X0	0x48	RW	Bit[7:0]: grn_x0[7:0] Low byte of horizontal center position of green channel
0x510A	GRN Y0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: grn_y0[9:8] High byte of vertical center position of green channel
0x510B	GRN Y0	0xF8	RW	Bit[7:0]: grn_y0[7:0] Low byte of vertical center position of green channel
0x510C	GRN A1	0x22	RW	Bit[7]: Not used Bit[6:0]: grn_a1 Gain coefficient for the square distance of current green pixel position and green center
0x510D	GRN A2	0x07	RW	Bit[7:4]: Not used Bit[3:0]: grn_a2 Precision gain coefficient for the square distance of current green pixel position and green center
0x510E	GRN B1	0xC2	RW	Bit[7]: Sign bit of grn_b1 Bit[6:0]: grn_b1 Gain coefficient for the distance of current green pixel position and green center
0x510F	GRN B2	0x08	RW	Bit[7:4]: Not used Bit[3:0]: grn_b2 Precision gain coefficient for the distance of current green pixel position and green center. Gain of current green pixel is defined with the distance (r), grn_a1, grn_a2, grn_b1 and grn_b2.

table 7-19 LENC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5110	BLUE X0	0x01	RW	Bit[7:2]: Not used Bit[1:0]: blu_x0[9:8] High byte of horizontal center position of blue channel
0x5111	BLUE X0	0x48	RW	Bit[7:0]: blu_x0[7:0] Low byte of horizontal center position of blue channel
0x5112	BLUE Y0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blu_y0[9:8] High byte of vertical center position of blue channel
0x5113	BLUE Y0	0xF8	RW	Bit[7:0]: blu_y0[7:0] Low byte of vertical center position of blue channel
0x5114	BLUE A1	0x22	RW	Bit[7]: Not used Bit[6:0]: blu_a1 Gain coefficient for the square distance of current blue pixel position and blue center
0x5115	BLUE A2	0x07	RW	Bit[7:4]: Not used Bit[3:0]: blu_a2 Precision gain coefficient for the square distance of current blue pixel position and blue center
0x5116	BLUE B1	0xC2	RW	Bit[7]: Sign bit of blu_b1 Bit[6:0]: blu_b1 Gain coefficient for the distance of current blue pixel position and blue center
0x5117	BLUE B2	0x08	RW	Bit[7:4]: Not used Bit[3:0]: blu_b2 Precision gain coefficient for the distance of current blue pixel position and blue center. Gain of current blue pixel is defined with the distance (r), blu_a1, blu_a2, blu_b1 and blu_b2.
0x5118	LENC CTRL	0x04	RW	Bit[7:3]: Not used Bit[2]: rnd_en Round enable generates random round bit Bit[1:0]: Not used

7.20 AWB control [0x5200 - 0x5220]

table 7-20 AWB control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5200	AWB CTRL00	0x00	RW	Bit[7]: Not used Bit[6]: freeze_gain_en Bit[5]: gain_man_en Bit[4]: after_gma Bit[3:0]: awb_frame_cnt
0x5201	AWB CTRL01	0x50	RW	Bit[7:6]: fast_step Bit[5:4]: locale_step Bit[3:0]: local_limit
0x5202	STABLE RANGE	0x04	RW	Bit[7:0]: stable_range[7:0]
0x5203	STABLE RANGEW	0x08	RW	Bit[7:0]: stable_rangew[7:0] Stable wide range
0x5204	RED GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: red_gain[11:8] High byte of manual red gain
0x5205	RED GAIN	0x00	RW	Bit[7:0]: red_gain[7:0] Low byte of manual red gain
0x5206	GRN GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: grn_gain[11:8] High byte of manual green gain
0x5207	GRN GAIN	0x00	RW	Bit[7:0]: grn_gain[7:0] Low byte of manual green gain
0x5208	BLU GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: blu_gain[11:8] High byte of manual blue gain
0x5209	BLU GAIN	0x00	RW	Bit[7:0]: blu_gain[7:0] Low byte of manual blue gain
0x520A	GAIN R LIMIT	0xF0	RW	Bit[7:4]: gain_r_up_limit 4 MSBs of red gain top limitation. 8 LSBs are 0xFF Bit[3:0]: gain_r_dn_limit 4 MSBs of red gain bottom limitation. 8 LSBs are 0x00
0x520B	GAIN G LIMIT	0xF0	RW	Bit[7:4]: gain_g_up_limit 4 MSBs of green gain top limitation. 8 LSBs are 0xFF Bit[3:0]: gain_g_dn_limit 4 MSBs of green gain bottom limitation. 8 LSBs are 0x00

table 7-20 AWB control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x520C	GAIN B LIMIT	0xF0	RW	Bit[7:4]: gain_b_up_limit 4 MSBs of blue gain top limitation. 8 LSBs are 0xFF Bit[3:0]: gain_b_dn_limit 4 MSBs of blue gain bottom limitation. 8 LSBs are 0x00
0x5210	CURR RED GAIN	–	R	Bit[7:4]: Not used Bit[3:0]: curr_red_gain[11:8] Current red gain high byte
0x5211	CURR RED GAIN	–	R	Bit[7:0]: curr_red_gain[7:0] Current red gain low byte
0x5212	CURR GRN GAIN	–	R	Bit[7:4]: Not used Bit[3:0]: curr_grn_gain[11:8] Current green gain high byte
0x5213	CURR GRN GAIN	–	R	Bit[7:0]: curr_grn_gain[7:0] Current green gain low byte
0x5214	CURR BLU GAIN	–	R	Bit[7:4]: Not used Bit[3:0]: curr_blu_gain[11:8] Current blue gain high byte
0x5215	CURR BLU GAIN	–	R	Bit[7:0]: curr_blu_gain[7:0] Current blue gain low byte
0x5216	RED BFG AVG	–	R	Bit[7:0]: red_bfg_avg[7:0] Red before gain average
0x5217	GRN BFG AVG	–	R	Bit[7:0]: grn_bfg_avg[7:0] Green before gain average
0x5218	BLU BFG AVG	–	R	Bit[7:0]: blu_bfg_avg[7:0] Blue before gain average
0x521A	RED AFG AVG	–	R	Bit[7:2]: Not used Bit[1:0]: red_afg_avg[9:8] Red after gain average high byte
0x521B	RED AFG AVG	–	R	Bit[7:0]: red_afg_avg[7:0] Red after gain average low byte
0x521C	GRN AFG AVG	–	R	Bit[7:2]: Not used Bit[1:0]: grn_afg_avg[9:8] Green after gain average high byte
0x521D	GRN AFG AVG	–	R	Bit[7:0]: grn_afg_avg[7:0] Green after gain average low byte
0x521E	BLU AFG AVG	–	R	Bit[7:2]: Not used Bit[1:0]: blu_afg_avg[9:8] Blue after gain average high byte

table 7-20 AWB control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x521F	BLU AFG AVG	–	R	Bit[7:0]: blu_afg_avg[7:0] Blue after gain average low byte
0x5220	AWB CALC	–	R	Bit[7:1]: Not used Bit[0]: awb_calc

7.21 gamma control [0x5300 - 0x5310]

table 7-21 gamma control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5300	GAMMA CTRL	0x01	RW	Bit[7:2]: Not used Bit[1]: yslp15_man_en Manual yst15 slope enable 0: Use calculated slope 1: Use register YSLP15 as slope Bit[0]: bias_en Bias enable 0: Bias is not used in gamma function 1: Bias is used in gamma function data_o=data_i - bias×gamma_gain+bias
0x5301	YST1	0x26	RW	Bit[7:0]: Yst1 Gamma gain coefficient for data not larger than 4 For data not larger than 4, gamma data is calculated with the following equation: yst1×data/4
0x5302	YST2	0x35	RW	Bit[7:0]: Yst2 Gamma gain coefficient for data that is 8 For data larger than 4 and less than 8, gamma data is calculated with the following equation: yst1+(yst2-yst1)×(data-4)/4
0x5303	YST3	0x48	RW	Bit[7:0]: Yst3 Gamma gain coefficient for data that is 16 For data larger than 8 and less than 16, gamma data is calculated with the following equation: yst2+(yst3-yst2)×(data-8)/8
0x5304	YST4	0x57	RW	Bit[7:0]: Yst4 Gamma gain coefficient for data that is 32 For data larger than 16 and less than 32, gamma data is calculated with the following equation: yst4+(yst4-yst3)×(data-16)/16

table 7-21 gamma control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5305	YST5	0x63	RW	Bit[7:0]: Yst5 Gamma gain coefficient for data that is 40 For data larger than 32 and less than 40, gamma data is calculated with the following equation: yst5+(yst5-yst4)×(data-32)/8
0x5306	YST6	0x6E	RW	Bit[7:0]: Yst6 Gamma gain coefficient for data that is 48 For data larger than 40 and less than 48, gamma data is calculated with the following equation: yst6+(yst6-yst5)×(data-40)/8
0x5307	YST7	0x77	RW	Bit[7:0]: Yst7 Gamma gain coefficient for data that is 56 For data Larger than 48 and less than 56, gamma data is calculated with the following equation: yst7+(yst7-yst6)×(data-48)/8
0x5308	YST8	0x80	RW	Bit[7:0]: Yst8 Gamma gain coefficient for data that is 64 For data larger than 56 and less than 64, gamma data is calculated with the following equation: yst8+(yst8-yst7)×(data-56)/8
0x5309	YST9	0x88	RW	Bit[7:0]: Yst9 Gamma gain coefficient for data that is 72 For data larger than 64 and less than 72, gamma data is calculated with the following equation: yst9+(yst9-yst8)×(data-64)/8
0x530A	YST10	0x96	RW	Bit[7:0]: Yst10 Gamma gain coefficient for data that is 80 For data larger than 72 and less than 80, gamma data is calculated with the following equation: yst10+(yst10-yst9)×(data-72)/8
0x530B	YST11	0xA3	RW	Bit[7:0]: Yst11 Gamma gain coefficient for data that is 96 For data larger than 80 and less than 96, gamma data is calculated with the following equation: yst11+(yst11-yst10)×(data-80)/16
0x530C	YST12	0xAF	RW	Bit[7:0]: Yst12 Gamma gain coefficient for data that is 112 For data larger than 96 and less than 112, gamma data is calculated with the following equation: yst12+(yst12-yst11)×(data-96)/16
0x530D	YST13	0xC5	RW	Bit[7:0]: Yst13 Gamma gain coefficient for data that is 144 For data larger than 112 and less than 144, gamma data is calculated with the following equation: yst13+(yst13-yst12)×(data-112)/32

table 7-21 gamma control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x530E	YST14	0xD7	RW	Bit[7:0]: Yst14 Gamma gain coefficient for data that is 176 For data larger than 144 and less than 176, gamma data is calculated with the following equation: yst14+(yst14-yst13)×(data-144)/32
0x530F	YST15	0xE8	RW	Bit[7:0]: Yst15 Gamma gain coefficient for data that is 208 For data larger than 176 and less than 208, gamma data is calculated with the following equation: yst15+(yst15-yst14)×(data-176)/32
0x5310	YSLP15	0x0F	RW	Bit[7:0]: Yslp15 Manual gamma gain coefficient slop for data that is larger than 208 For data larger than 208, gamma data is calculated with the following equation: yst15+yslp15×(data-208)/64

7.22 DPC control [0x5400 - 0x540F]

table 7-22 DPC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5400	DPC CTRL00	0x03	RW	Bit[7:5]: Not used Bit[4]: man_en Bit[3:2]: Not used Bit[1:0]: edge_opt
0x5401	DPC CTRL01	0x0E	RW	Bit[7:4]: Not used Bit[3]: sc_en Bit[2]: dc_en Bit[1]: cross_en Bit[0]: saturate_en
0x5402	DPC CTRL02	0x32	RW	Bit[7]: Not used Bit[6:4]: wthre_list0 Bit[3]: Not used Bit[2:0]: wthre_list1
0x5403	DPC CTRL03	0x04	RW	Bit[7:5]: Not used Bit[4]: adpt_ptn Bit[3:0]: bthre_ratio
0x5404	DPC CTRL04	0x0F	RW	Bit[7]: Not used Bit[6:0]: gain_list

table 7-22 DPC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5405	DPC CTRL05	0x46	RW	Bit[7:4]: Thre1 Bit[3:0]: Saturate
0x540E	DPC CTRL0E	–	R	Bit[7:5]: Not used Bit[4]: ro_thre3 Bit[3]: Not used Bit[2:0]: ro_wthre
0x540F	RO BTHRE	–	R	Bit[7:5]: Not used Bit[4:0]: ro_bthre

7.23 CIP control [0x5500 - 0x5510]

table 7-23 CIP control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5500	SHRP MT GAIN TH1	0x08	RW	Bit[7:0]: shrp_mt_gain_th1 Sharpen strength lower gain threshold It has 3-bit precision When the current real gain, which has 3-bit precision, is less than shrp_mt_gain_th1, the sharpen strength is shrp_mt_th1. When the current real gain, which has 3-bit precision, is greater than shrp_mt_gain_th2×4, the sharpen strength is shrp_mt_th2. When the current real gain, which has 3-bit precision, is not less than shrp_mt_gain_th1 and not greater than shrp_mt_gain_th2×4, the sharpen strength is shrp_mt_th2 + (current_real_gain_8x - shrp_mt_gain_th1) × (shrp_mt_th1-shrp_mt_th2) / (shrp_mt_gain_th2×4-shrp_mt_gain_th1)
0x5501	SHRP MT GAIN TH2	0x48	RW	Bit[7:0]: shrp_mt_gain_th2 Sharpen strength higher gain threshold It has 1 bit precision. See shrp_mt_gain_th1 description.
0x5502	SHRP MT TH1	0x18	RW	Bit[7]: Not used Bit[6:0]: shrp_offset1 Sharpen strength threshold for lower gain When shrp_man_en is enabled, it is shrp_mt_th_man. See shrp_mt_gain_th1 description.

table 7-23 CIP control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5503	SHRP MT TH2	0x0E	RW	Bit[7]: Not used Bit[6:0]: hrp_offset2 Sharpen strength threshold for higher gain See shrp_mt_gain_th1 description.
0x5504	DNS GAIN TH1	0x08	RW	Bit[7:0]: dns_gain_th1 Denoise lower gain threshold It has 3-bit precision. When the current real gain, which has 3-bit precision, is less than dns_gain_th1, the DNS threshold is dns_th1. When the current real gain, which has 3-bit precision, is greater than dns_gain_th2×4, the DNS threshold is dns_th2. When the current real gain, which has 3-bit precision, is not less than dns_gain_th1 and not greater than dns_gain_th2×4, the DNS threshold is dns_th1 + (current_real_gain_8x - dns_gain_th1) × (dns_th2-dns_th1) / (dns_gain_th2×4-dns_gain_th1).
0x5505	DNS GAIN TH2	0x48	RW	Bit[7:0]: dns_gain_th2 Denoise higher gain threshold It has 1 bit precision. See dns_gain_th1 description
0x5506	DNS TH1	0x09	RW	Bit[7]: Not used Bit[6:0]: dns_offset1 Denoise threshold for lower gain When dns_man_en is enabled, it is dns_th_man. See dns_gain_th1 description.
0x5507	DNS TH2	0x16	RW	Bit[7]: Not used Bit[6:0]: dns_offset2 Denoise threshold for higher gain See dns_gain_th1 description.

table 7-23 CIP control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5508	CIP CTRL	0xAD	RW	Bit[7]: interlace_en Interlace mode enable 0: Input image is normal image 1: Input image is interlaced image Bit[6]: shrp_man_en Sharpen manual mode 0: Automatic sharpen 1: Manual sharpen Bit[5]: bd_opt Boundary process enable 0: Disable boundary process 1: Enable boundary process Bit[4]: dns_man_en Denoise manual mode enable 0: Use automatic dns_th 1: Use manual dns_th Bit[3]: bw_mode01_sel BW mode0 and BW mode1 selection signal 0: BW mode0 1: BW mode1 Note: In BW mode0, there is interlace mode and progressive mode. In BW mode1, there is no interlace mode and progressive mode difference. Bit[2:0]: br_shrp_ctrl_th BR sharpen control threshold to adjust the weight of high frequency of chroma. The larger the threshold, the higher weight. Changing these bytes is not recommended
0x5509	SHRP TH GAIN TH1	0x08	RW	Bit[7:0]: shrp_th_gain_th1 Sharpen threshold lower gain threshold It has 3-bit precision. When the current real gain, which has 3-bit precision, is less than shrp_th_gain_th1, the sharpen threshold is shrp_th1. When the current real gain, which has 3-bit precision, is greater than shrp_th_gain_th2×4, the sharpen threshold is When the current real gain, which has 3-bit precision, is not less than shrp_th_gain_th1 and not greater than shrp_th_gain_th2×4, the sharpen threshold is shrp_th1 + (current_real_gain_8x - shrp_th_gain_th1) × (shrp_th2-shrp_th1) / (shrp_th_gain_th2×4-shrp_th_gain_th1).
0x550A	SHRP TH GAIN TH2	0x48	RW	Bit[7:0]: shrp_th_gain_th2 Sharpen threshold higher gain threshold It has 1-bit precision. See shrp_th_gain_th1 description.

table 7-23 CIP control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x550B	SHRP TH1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: shrp_th1 Sharpen threshold for lower gain When the shrp_man_en is enabled, it is shrp_th_man. See shrp_th_gain_th1 description.
0x550C	SHRP TH2	0x06	RW	Bit[7:5]: Not used Bit[4:0]: shrp_th2 Sharpen threshold for higher gain See shrp_th_gain_th1 description.
0x550D	RECURSIVE DNS EN	0x01	RW	Bit[7:1]: Not used Bit[0]: recursivedns_en Recursive denoise function enable 0: Disable 1: Enable
0x550E	SHRP MT	–	R	Bit[7]: Not used Bit[6:0]: shrp_mt Auto calculate sharpen strength
0x550F	DNS TH	–	R	Bit[7]: Not used Bit[6:0]: dns_th Auto calculate denoise threshold
0x5510	SHRP TH	–	R	Bit[7:5]: Not used Bit[4:0]: shrp_th Auto calculate sharpen threshold

7.24 CMX control [0x5600 - 0x560B]

table 7-24 CMX control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5600	CMX CTRL	0x00	RW	Bit[7:2]: Not used Bit[1]: precision_opt Selection option for CMXxy in which both x and y are in [1, 3] 0: 1 MSB for integer gain and 7 LSBs for fraction 1: 2 MSBs for integer gain and 6 LSBs for fraction Bit[0]: uv_cbcr_en UV CbCr enable signal 0: Disable 1: Enable
0x5601	CMX1	0x20	RW	Bit[7:0]: CMX11 Absolute value of coefficient of R for calculating Y
0x5602	CMX2	0x64	RW	Bit[7:0]: CMX12 Absolute value of coefficient of G for calculating Y
0x5603	CMX3	0x08	RW	Bit[7:0]: CMX13 Absolute value of coefficient of B for calculating Y
0x5604	CMX4	0x30	RW	Bit[7:0]: CMX21 Absolute value of coefficient of R for calculating U
0x5605	CMX5	0x90	RW	Bit[7:0]: CMX22 Absolute value of coefficient of G for calculating U
0x5606	CMX6	0xC0	RW	Bit[7:0]: CMX23 Absolute value of coefficient of B for calculating U
0x5607	CMX7	0xA0	RW	Bit[7:0]: CMX31 Absolute value of coefficient of R for calculating V
0x5608	CMX8	0x98	RW	Bit[7:0]: CMX32 Absolute value of coefficient of G for calculating V
0x5609	CMX9	0x08	RW	Bit[7:0]: CMX33 Absolute value of coefficient of B for calculating V

table 7-24 CMX control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x560A	CMXSIGN	0x01	RW	Bit[7:1]: Not used Bit[0]: cmx33_sign Sign bit of CMX33 0: Used coefficient is CMX33 1: Used coefficient is -1 × CMX33
0x560B	CMXSIGN	0x98	RW	Bit[7]: cmx32_sign Sign bit of CMX32 0: Used coefficient is CMX32 1: Used coefficient is -1 × CMX32 Bit[6]: cmx31_sign Sign bit of CMX31 0: Used coefficient is CMX31 1: Used coefficient is -1 × CMX31 Bit[5]: cmx23_sign Sign bit of CMX23 0: Used coefficient is CMX23 1: Used coefficient is -1 × CMX23 Bit[4]: cmx22_sign Sign bit of CMX22 0: Used coefficient is CMX22 1: Used coefficient is -1 × CMX22 Bit[3]: cmx21_sign Sign bit of CMX21 0: Used coefficient is CMX21 1: Used coefficient is -1 × CMX21 Bit[2]: cmx13_sign Sign bit of CMX13 0: Used coefficient is CMX13 1: Used coefficient is -1 × CMX13 Bit[1]: cmx12_sign Sign bit of CMX12 0: Used coefficient is CMX12 1: Used coefficient is -1 × CMX12 Bit[0]: cmx11_sign Sign bit of CMX11 0: Used coefficient is CMX11 1: Used coefficient is -1 × CMX11

7.25 SDE control [0x5800 - 0x580C]

table 7-25 SDE control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5800	SDE EN CTRL	0x00	RW	Bit[7]: Fixy enable When set to 1, Y output will be a fixed value, set by register yoffset/fixy Bit[6]: Neg enable When set to 1, output data will be a reversed value Bit[5]: Gray enable When set to 1, UV output will be a fixed value 128. Output image is black and white Bit[4]: fix_v enable When set to 1, V output will be a fixed value, set by register sat_th1/fixv Bit[3]: fix_u enable When set to 1, U output will be a fixed value, set by register sat_th2/fixu Bit[2]: Contrast enable Y contrast function enable signal 0: Disable 1: Enable Bit[1]: Saturation enable Color saturation function enable signal 0: Disable 1: Enable Bit[0]: Not used
0x5801	HUE COSINE	0x80	RW	Bit[7:0]: Not used
0x5802	HUE SINE	0x00	RW	Bit[7:0]: Not used
0x5803	SATURATION TH2	0x40	RW	Bit[7:0]: sat_th2 When fixu_en is enabled, it is the fixed U value. When fixu_en is 0 and uvadj_man_en is 1, it is saturation coefficient for U. When both of fixu and uvadj_man_en are 0, it is the top saturation threshold to calculate the UV adjust coefficient
0x5804	SATURATION TH1	0x00	RW	Bit[7:0]: sat_th1 When fixv_en is enabled, it is the fixed V value. When fixv_en is 0 and uvadj_man_en is 1, it is saturation coefficient for V. When both of fixv and uvadj_man_en are 0, it is the bottom saturation threshold to calculate the UV adjust coefficient

table 7-25 SDE control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5805	Y OFFSET	0x00	RW	Bit[7:0]: Yoffset Offset coefficient for Y contrast calculation It is combined with ygain and ybright to calculate contrasted Y.
0x5806	Y GAIN	0x20	RW	Bit[7:0]: Ygain Gain coefficient for Y contrast calculation It is combined with yoffset and ybright to calculate contrasted Y.
0x5807	Y BRIGHT	0x00	RW	Bit[7:0]: Ybright Bright coefficient for Y contrast calculation It is combined with ygain and yoffset to calculate contrasted Y.
0x5808	SIGN BITS	0x00	RW	Bit[7:4]: Not used Bit[3]: ybright_sign_bit Sign bit for Ybright 0: Ybright is positive number (ybright) 1: Ybright is negative number (-1×ybright) Bit[2]: yoffset_sign_bit Sign bit for Yoffset When the auto offset is used, this sign bit is not used 0: Yoffset is positive number (yoffset) 1: Yoffset is negative number (-1×yoffset) Bit[1:0]: Not used Note: Y contrast calculation equation: Yout = [Yin+ (1 - 2×ybright_sign_bit)×ybright + (2×yoffset_sign_bit - 1) × yoffset)] × ygain + (1-2×yoffset_sign_bit)×yoffset
0x5809	UVADJ GAIN TH1	0x08	RW	Bit[7:0]: gain_th1 UV adjust curve bottom gain threshold When real gain, which has 3-bit precision, is less than gain_th1, the uv_adj is sat_th2. When real gain, which has 3-bit precision, is larger than gain_th2, the uv_adj is sat_th1. When real gain, which has 3-bit precision, is larger than gain_th1 and less than gain_th2, uv_adj = sat_th1 + (sat_th2-sat_th1) × (gain_th2-real_gain) / (gain_th2-gain_th1).

table 7-25 SDE control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x580A	UVADJ GAIN TH2	0x80	RW	Bit[7:0]: gain_th2 UV adjust curve top gain threshold When real gain, which has 3-bit precision, is less than gain_th1, uv_adj is sat_th2. When real gain, which has 3-bit precision, is larger than gain_th2, uv_adj is sat_th1. When real gain, which has 3-bit precision, is larger than gain_th1 and less than gain_th2, uv_adj = sat_th1 + (sat_th2-sat_th1) × (gain_th2-real_gain) / (gain_th2-gain_th1)
0x580B	UVADJ MAN EN	0x00	RW	Bit[7:2]: Not used Bit[1]: offset_man_en 0: Offset used in Y contrast is input Y average 1: Offset used in Y contrast is set in yoffset Bit[0]: uvadj_man_en UV adjust manual enable 0: Use the calculated uv_adj for UV adjust coefficient 1: Use the sat_th1 for V saturation coefficient; use the sat_th2 for U saturation coefficient
0x580C	UV ADJ	–	R	Bit[7:0]: uv_adj Calculated uv_adj

7.26 AVG control [0x5900 - 0x5913]

table 7-26 AVG control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5900	SUBWIN XSTART	0x00	RW	Bit[7:5]: Not used Bit[4:0]: xstart_sub[12:8] AVG sub-window horizontal start position
0x5901	SUBWIN XSTART	0x00	RW	Bit[7:0]: xstart_sub[7:0] AVG sub-window horizontal start position
0x5902	SUBWIN YSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ystart_sub[11:8] AVG sub-window vertical start position
0x5903	SUBWIN YSTART	0x00	RW	Bit[7:0]: ystart_sub[7:0] AVG sub-window vertical start position

table 7-26 AVG control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5904	SUBWIN HSIZE	0x02	RW	Bit[7:5]: Not used Bit[4:0]: hsize_sub[12:8] Sub-window width
0x5905	SUBWIN HSIZE	0x80	RW	Bit[7:0]: hsize_sub[7:0] Sub-window width
0x5906	SUBWIN VSIZE	0x01	RW	Bit[7:2]: Not used Bit[3:0]: vsize_sub[11:8] Sub-window height
0x5907	SUBWIN VSIZE	0xE0	RW	Bit[7:0]: vsize_sub[7:0] Sub-window height
0x5908	WEIGHT001	0x11	RW	Bit[7:4]: Weight01 Weight of zone01 Bit[3:0]: Weight00 Weight of zone00
0x5909	WEIGHT023	0x11	RW	Bit[7:4]: Weight03 Weight of zone03 Bit[3:0]: Weight02 Weight of zone02
0x590A	WEIGHT101	0x11	RW	Bit[7:4]: Weight11 Weight of zone11 Bit[3:0]: Weight10 Weight of zone10
0x590B	WEIGHT123	0x11	RW	Bit[7:4]: Weight13 Weight of zone13 Bit[3:0]: Weight12 Weight of zone12
0x590C	WEIGHT101	0x11	RW	Bit[7:4]: Weight21 Weight of zone 21 Bit[3:0]: Weight20 Weight of zone20
0x590D	WEIGHT123	0x11	RW	Bit[7:4]: Weight23 Weight of zone23 Bit[3:0]: Weight22 Weight of zone22
0x590E	WEIGHT201	0x11	RW	Bit[7:4]: Weight31 Weight of zone31 Bit[3:0]: Weight30 Weight of zone30
0x590F	WEIGHT223	0x11	RW	Bit[7:4]: Weight33 Weight of zone33 Bit[3:0]: Weight32 Weight of zone32

table 7-26 AVG control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5910	AVG CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: sum_opt 0: Sum=(4×B+9×G×2+10×R)/8 1: Sum=B+G×2+R Bit[0]: sub_win_en Sub-window function enable signal 0: Disable 1: Enable
0x5911	WEIGHT SUM	–	R	Bit[7:0]: Weight-sum Sum of weight
0x5912	AVG DONE	–	R	Bit[7:1]: Not used Bit[0]: avg_done Avg calculated indicating signal for SCCB read
0x5913	AVG	–	R	Bit[7:0]: Avg High 8 bits of whole image avg output

7.27 WINC control [0x5A00 - 0x5A0C]

table 7-27 WINC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5A00	XSTART	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Xstart[12:8] High byte of horizontal start of manual window
0x5A01	XSTART	0x00	RW	Bit[7:0]: Xstart[7:0] Low byte of horizontal start of manual window
0x5A02	YSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Ystart[11:8] High byte of vertical start of manual window
0x5A03	YSTART	0x00	RW	Bit[7:0]: Ystart[7:0] Low byte of vertical start of manual window
0x5A04	X WIN	0x02	RW	Bit[7:5]: Not used Bit[4:0]: x_win[12:8] High byte of horizontal size of manual window
0x5A05	X WIN	0x80	RW	Bit[7:0]: x_win[7:0] Low byte of horizontal size of manual window

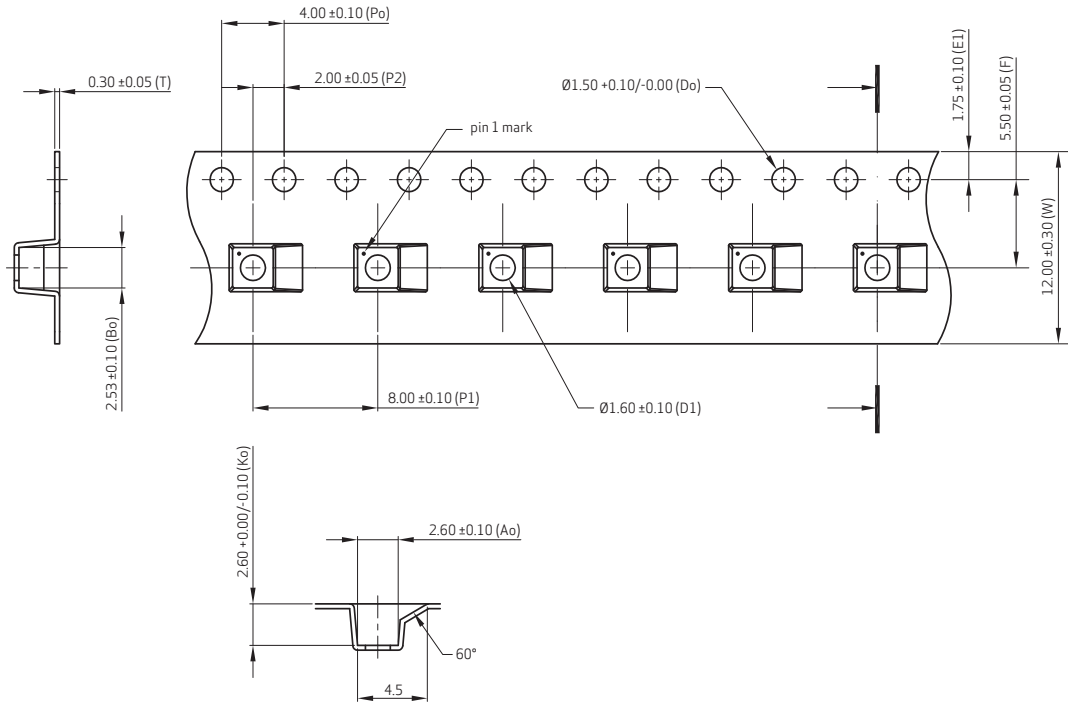
table 7-27 WINC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A06	Y WIN	0x01	RW	Bit[7:4]: Not used Bit[3:0]: y_win[11:8] High byte of vertical size of manual window
0x5A07	Y WIN	0xE0	RW	Bit[7:0]: y_win[7:0] Low byte of vertical size of manual window
0x5A08	CONTROL	0x00	RW	Bit[7:3]: Not used Bit[2]: flip_offset_en When set, output raw image will be adjusted automatically in vertical direction Bit[1]: mirror_offset_en When set, output raw image will be adjusted automatically in horizontal direction Bit[0]: win_man_en Manual window enable
0x5A09	PX CNT	–	R	Bit[7:5]: Not used Bit[4:0]: px_cnt[12:8]
0x5A0A	PX CNT	–	R	Bit[7:0]: px_cnt[7:0]
0x5A0B	LN CNT	–	R	Bit[7:4]: Not used Bit[3:0]: ln_cnt[11:8]
0x5A0C	LN CNT	–	R	Bit[7:0]: ln_cnt[7:0]

8 shipping and packaging

8.1 tape and reel

figure 8-1 tape specifications



note 1 dimensions in millimeters unless otherwise specified.

note 2 10 sprocket hole pitches cumulative tolerance ±0.20 mm.

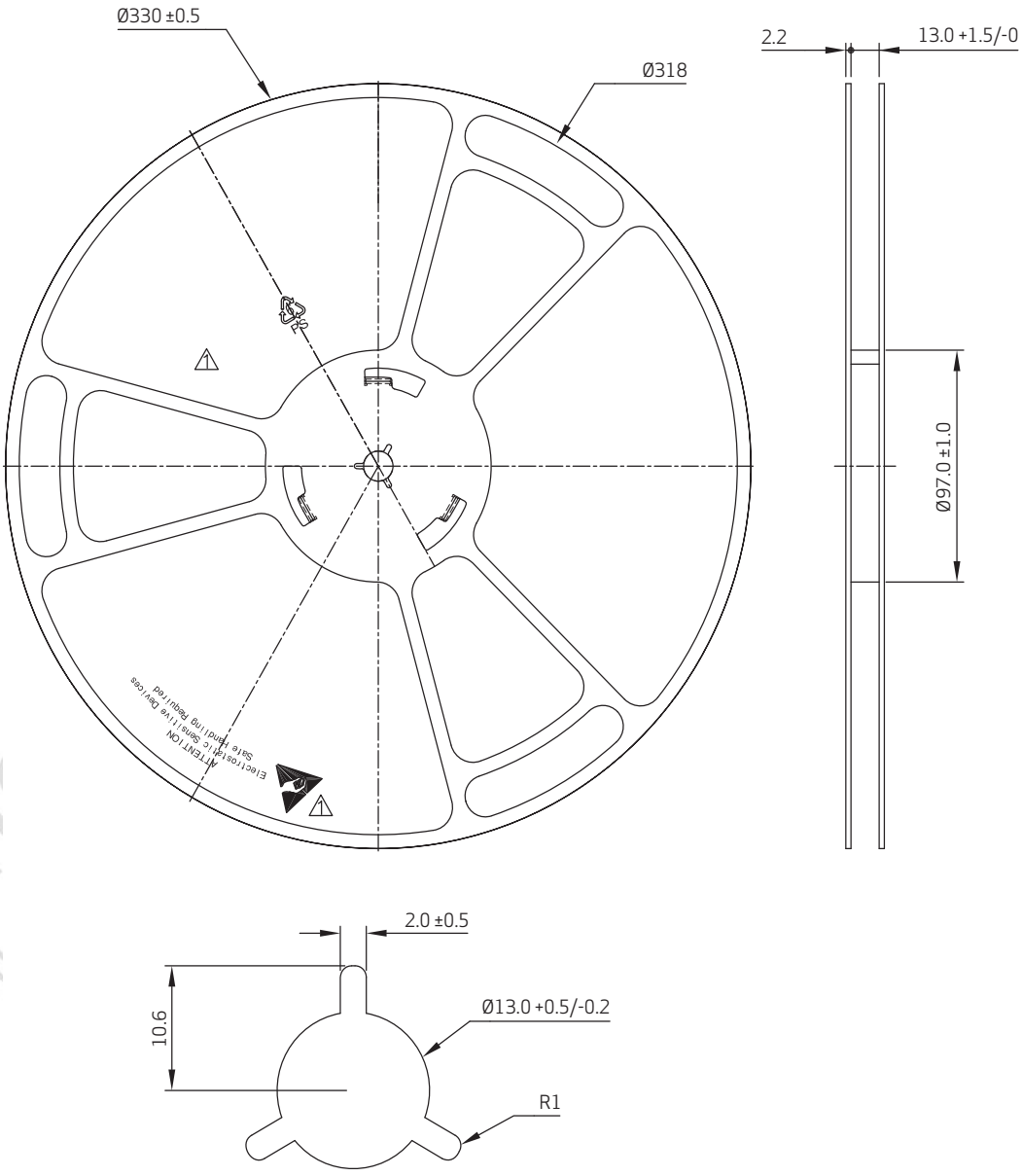
note 3 camber not to exceed 1 mm in 250 mm.

note 4 pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

note 5 (S.R. OHM/SQ.) means surface electric resistivity of the carrier tape.

OVM7695-RAEA_MDS_8_1

figure 8-2 reel specifications



note 1 all dimensions are in millimeters unless otherwise specified.

0VM7695_RAEA_RYEA_MDS_8_2

revision history

version 1.0 08.16.2012

- initial release

version 1.1 11.28.2012

- in features, added RAW8 to support output formats
- in features, changed diagonal field of view (FOV) from 62° to 61°, changed f no. from 2.89 to 2.7, and changed focal length from 1.18 mm to 1.21 mm
- in features, changed package dimensions (including ball height) from "2420 µm x 2350 µm x 2338 µm" to "2420 µm x 2350 µm x 2325 µm"
- in chapter 1, updated figure 1-2 and removed figure 1-3
- in chapter 2, updated figure 2-1
- in table 3-1, changed field-of- view (FOV), diagonal from 62° to 61°, changed field-of- view (FOV), horizontal from 50.8° to 50°, changed f no. from 2.89 to 2.7, changed focal length from 1.18 mm to 1.21mmm, changed optical layout from "3-surface lens" to "2-element lens", changed maximum image circle from "1.52 mm diameter" to "1.58 mm diameter", changed TV distortion from "<2% at 95% field" to "<3% at 95% field", changed relative illumination (optical) from "49% @ y = 0.7 mm" to "67% @ y = 0.7 mm", and changed IR elimination filter 50% cut-off from "660 nm ± 10 nm" to "665 nm ± 10 nm"
- in table 4-1, changed ambient storage temperature from "-40°C to +95°C" to "-40°C to +85°C"
- in table 4-3, removed V_{DDA} and changed VDD-IO typical value from 2.8V to 1.8V
- in section 6.1, added RAW 8 to "The OVM7695 supports a single lane MIPI interface... to communicate to components in a mobile device".
- in table 6-2, changed bit description for register 0x480F[7] to "Not used", 0x480F[6:0] to "p_ck_n manual control, lp_ck_p manual control, lp_n manual control, lp_p manual control, p_tx_ck manual control, p_tx_da manual control, p_sel manual control", respectively
- in chapter 6, added section 6.2
- in table 7-12, changed bit description for register 0x480F[7] to "Not used" and updated 0x480F[6:0] to "p_ck_n manual control, lp_ck_p manual control, lp_n manual control, lp_p manual control, p_tx_ck manual control, p_tx_da manual control, p_sel manual control", respectively
- in table 7-13, changed register bit descriptions for registers 0x3820[7:3] to "Not used", 0x3820[2] from "bypass_mipi" to "Bypass MIPI interface", 0x3820[1] to "vertical binning enable", 0x4F05[0] from "r_bypass_2to1" to "SPI two lane enable", 0x4F06[1] to "Not used" and 0x4F06[0] from "r_spi_gt_en" to "SPI/MIPI control"

version 1.11 01.15.2013

- in chapter 2, updated figure 2-1, figure 2-3, and table 2-1
- in chapter 8, updated figure 8-1 and 8-2

version 1.2 01.30.2013

- in key specifications, changed sensitivity to "1200 mV/Lux-sec"
- in chapter 3, added section 3.3 and figure 3-2
- in table 5-1, added register 0x5003[7], "dns_opt"
- in table 5-8, changed default value of register 0x5800 from "0x02" to "0x00" and changed default value of register 0x5804 from "0x20" to "0x00"
- in section 6-2, changed second paragraph to "For more details about OmniVision's proprietary SPI, please contact your local OmniVision FAE."
- in section 7, changed last sentence to "The device slave addresses are 0x42 for write and 0x43 for read."
- in section 7, removed all columns labeled "decimal", changed column name "index (hex)" to "address", changed column name "hex" to "default value", and changed column name "function" to "description" in all applicable tables
- in table 7-1, changed default value of register 0x302A from "B0" to "0xB0/0xB1"
- in table 7-3, changed default value of register 0x3106 from "02" to "0x92"
- in table 7-8, changed description of register bit 0x3005[0] to "SPI_SDA0 shared with MDN"
- in table 7-17, changed description of register bit 0x5003[7] to "dns_opt"
- in table 7-19, changed description of register 0x5106 to "Bit[7]: Sign bit of red_b1; Bit[6:0]: red_b1"
- in table 7-19, removed formula from description of register 0x5107
- in table 7-19, changed description of register 0x510E to "Bit[7]: Sign bit of grn_b1; Bit[6:0]: grn_b1"
- in table 7-19, removed formula from description of register 0x510F
- in table 7-19, changed description of register 0x5116 to "Bit[7]: Sign bit of blu_b1; Bit[6:0]: blu_b1"
- in table 7-19, removed formula from description of register 0x5117
- in table 7-25, change default value of register 0x5800 from "0x02" to "0x00" and changed default value of register 0x5804 from "0x20" to "0x00"

version 2.0 06.27.2013

- changed datasheet from Preliminary Specification to Product Specification
- in key specifications, updated all TBDs, changed dynamic range from "69.2 dB @ 16x gain" to "66.7 dB @ 16x gain", and changed dark current from "2.2 mV/s @ 50°C junction temperature" to "10 e^-/sec @ 50°C junction temperature"
- in tables 4-3, 4-4, and 4-5, updated all TBDs
- in table 4-3, added "$I_{DDS-SCCB}$ typical, 120 µA"

version 2.01 07.19.2013

- in table 5-2, changed register bits 0x5118[1:0] to "Not used" and removed registers 0x5119, 0x511A, 0x511B, and 0x511C

version 2.02 08.01.2013

- in chapter 1, update figure 1-10 (changed C1 and C2 from 0.1µF to 1µF)

version 2.03 09.03.2013

- in features, added "YUV422, RAW8, RAW10 through OmniVision's proprietary SPI" to support output formats
- in section 1.3, changed "The OVM7695 supports the following formats:" to "The OVM7695 supports the following formats: YUV422 and RAW8 through MIPI and YUV422, RAW8, and RAW10 through OmniVision's proprietary SPI."
- in section 6.2, added first paragraph, "The SPI module used in the OVM7695...to use the OVM7695 SPI interface." and deleted "For more details about OmniVision's proprietary SPI, contact your local OmniVision FAE."

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