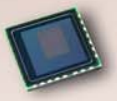
OmniVision



datasheet

PRODUCT SPECIFICATION

1/13" color CMOS VGA (640x480) image sensor
with OmniPixel3-HS™ technology

OV7692

color CMOS VGA (640 x 480) image sensor with OmniPixel3-HS™ technology

datasheet (CSP3)
PRODUCT SPECIFICATION

version 2.01
december 2010

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- digital still cameras
- cellular phones
- toys

ordering information

- **OV07692-A25A** (color, lead-free)
  25-pin CSP3

features

- OmniPixel3-HS™ structure using 0.11 µm process
- optical size of 1/13"
- automatic/manual control of automatic exposure control (AEC), automatic gain control (AGC), automatic 50/60 Hz luminance detection and automatic black level calibration (ABLC)
- support for horizontal and vertical sub-sampling
- mirror, flip, scaling, windowing
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- digital video port (DVP) parallel output interface
- MIPI serial output interface
- serial camera control bus (SCCB) interface
- programmable I/O drive capability
- on-chip phase lock loop (PLL)
- 2.8V power supply
- built-in 1.5V regulator for sensor core power
- low power consumption

key specifications (typical)

- **active array size:** 640 x 480
- **power supply:**
  analog: 2.6V ~ 3.0V
  I/O: 1.7V ~ 3.0V
- **power requirements:**
  active: ~120 mW @ AVDD= 2.8V, DOVDD=1.8V
  standby: 23 µA
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-1**)
  stable image: 0°C to 50°C junction temperature (see **table 8-1**)
- **output formats:** RAW 8-bit, RAW 10-bit (for MIPI only), YUV422, RGB565/444
- **lens size:** 1/13"
- **lens chief ray angle:** 24.2° (see **figure 10-2**)
- **input clock frequency:** 6 ~ 27 MHz, 54 MHz
- **max S/N ratio:** 38 dB
- **dynamic range:** 66 dB @ 8x gain
- **maximum image transfer rate:**
  VGA (640x480): 30 fps
  CIF (352x288): 30 fps
  QVGA (320x240): 60 fps
  QCIF (176x144): 60 fps
- **sensitivity:** 960 mV/Lux-sec
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 511 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.75 µm x 1.75 µm
- **dark current:** 10 mV/s @ 60°C junction temperature
- **image area:** 1148 µm x 861 µm
- **package dimensions:** 2765 µm x 3129 µm

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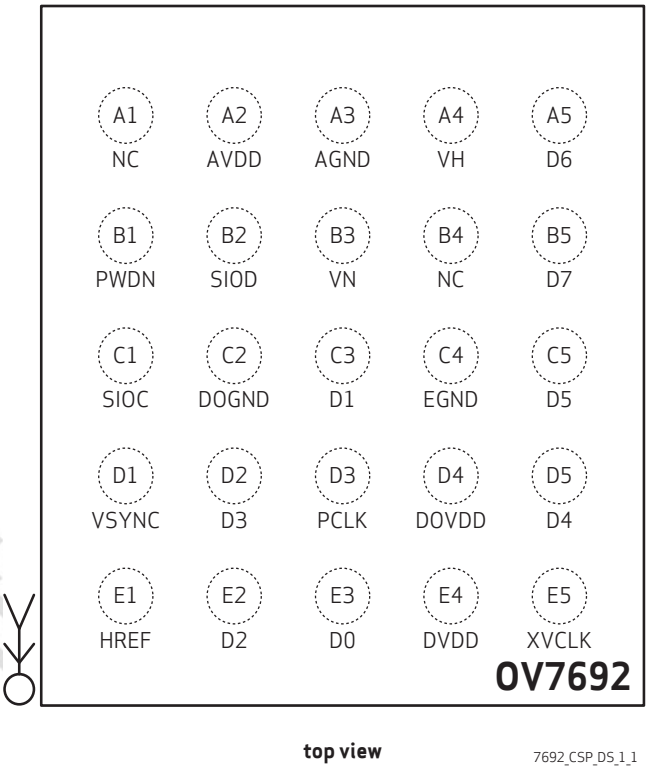
1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7692 image sensor. The package information is shown in section 9.

table 1-1 signal descriptions

pin number	signal name	pin type	description
A1	NC	–	–
A2	AVDD	power	power for analog circuit
A3	AGND	ground	ground for analog circuit
A4	VH	reference	internal analog reference
A5	D6	I/O	digital video port (DVP) bit[6] / MIPI data positive output
B1	PWDN	input	power down (active high with internal pull down resistor)
B2	SIOD	I/O	SCCB data
B3	VN	reference	internal analog reference
B4	NC	–	–
B5	D7	I/O	digital video port (DVP) bit[7] / MIPI data negative output
C1	SIOC	input	SCCB input clock
C2	DOGND	ground	ground for IO circuit
C3	D1	I/O	digital video port (DVP) bit[1]
C4	EGND	ground	ground for MIPI circuit
C5	D5	I/O	digital video port (DVP) bit[5] / MIPI clock negative output
D1	VSYNC	I/O	vertical sync output
D2	D3	I/O	digital video port (DVP) bit[3]
D3	PCLK	I/O	pixel clock output
D4	DOVDD	power	power for IO circuit
D5	D4	I/O	digital video port (DVP) bit[4] / MIPI clock positive output
E1	HREF	I/O	horizontal sync output
E2	D2	I/O	digital video port (DVP) bit[2]
E3	D0	I/O	digital video port (DVP) bit[0]
E4	DVDD	reference	power for digital circuit
E5	XVCLK	input	system clock input

figure 1-1 pin diagram



top view

7692_CSP_DS_1_1

2 system level description

2.1 overview

The OV7692 (color) image sensor is a low voltage, high-performance 1/13-inch CMOS VGA image sensor. It provides the full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit (DVP/MIPI) / 10-bit (MIPI) images with resolution higher than QQCIF in various formats (scaling is not available in RAW format) via the control of the Serial Camera Control Bus (SCCB) interface.

The OV7692 has an image array capable of operating at up to 30 frames per second (fps) in VGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

Compared to its predecessor, the OV7692 has a MIPI interface which supports high speed serial output. The OV7692 supports both a digital video parallel port and a serial MIPI port.

2.2 architecture

The OV7692 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV7692 image sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of the array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV7692 block diagram

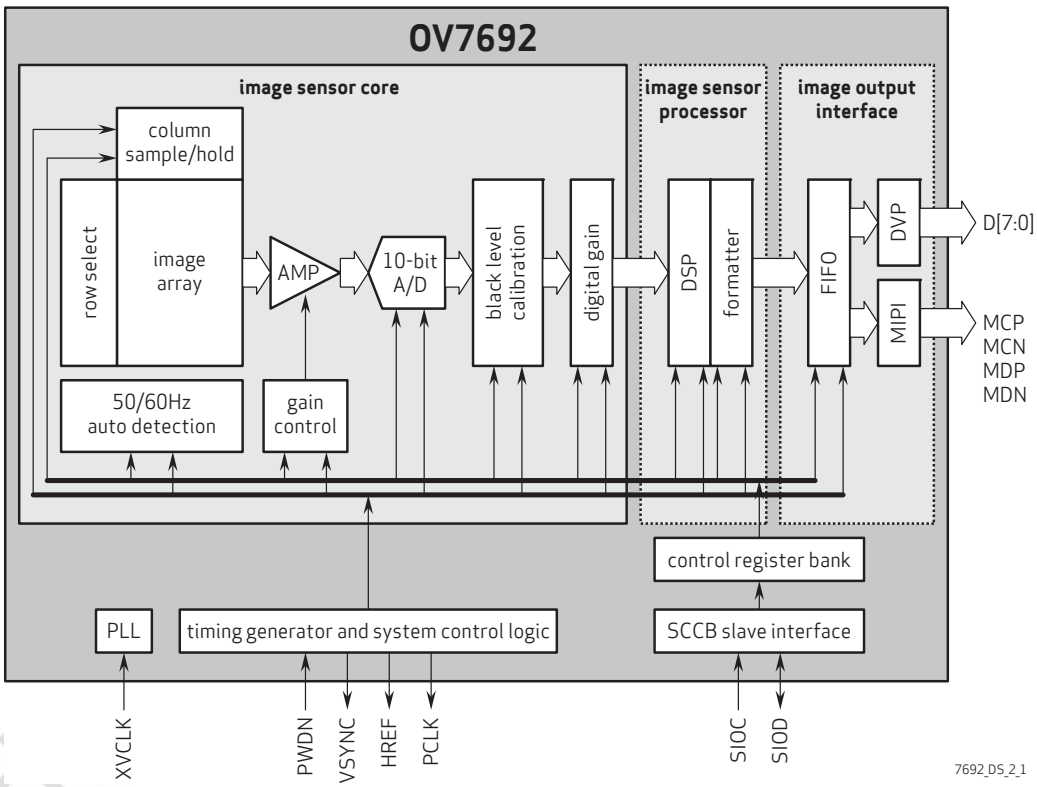
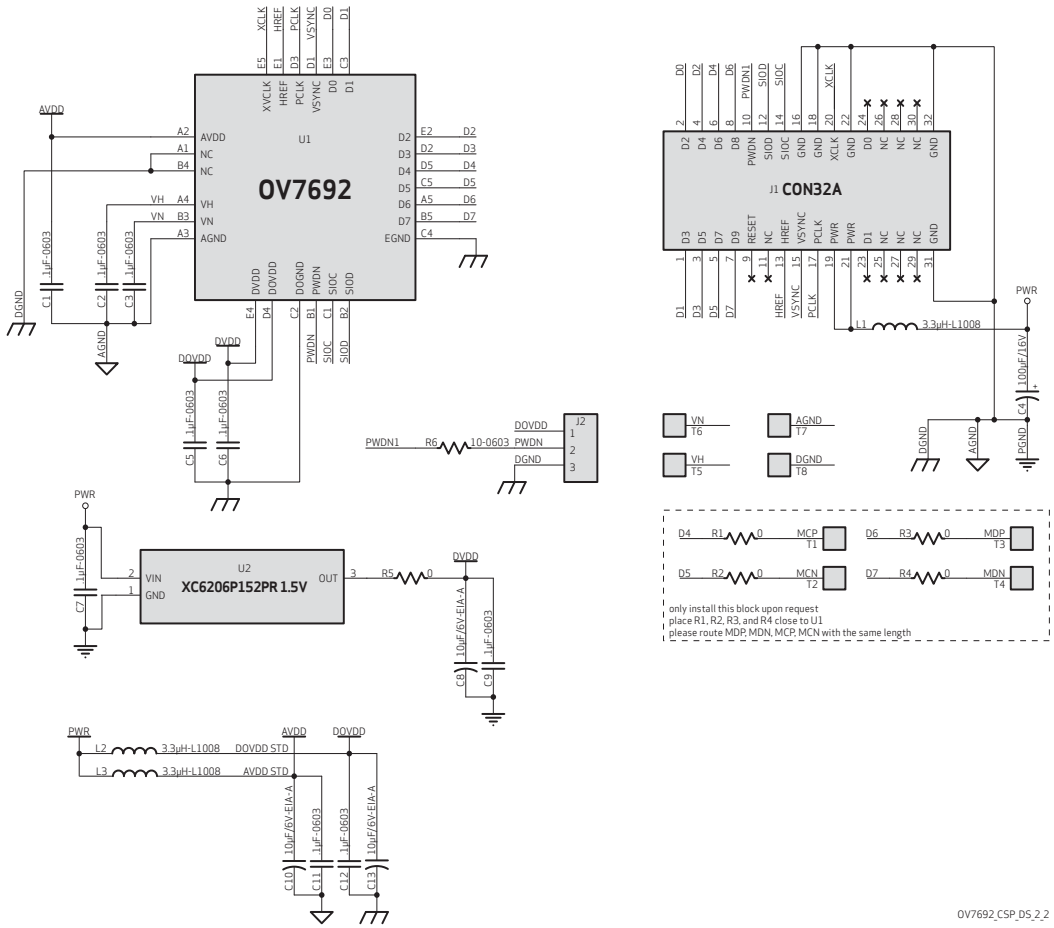


figure 2-2 reference design schematic



0V7692_CSP_DS_2_2

2.3 format and frame rate

table 2-1 format and frame rate

format	resolution	frame rate	scaling method	pixel clock	
				YUV	RAW
VGA	640 x 480	30 fps	full	24 MHz	12 MHz
CIF	352 x 288	30 fps	scaling down from VGA	24 MHz	n/a
QVGA	320 x 240	60 fps	sub sampling from VGA	12 MHz	6 MHz
QCIF	176 x 144	60 fps	scaling down from QVGA	12 MHz	n/a
QQVGA	160 x 120	60 fps	scaling down from QVGA	12 MHz	n/a
QQCIF	88 x 72	60 fps	scaling down from QVGA	12 MHz	n/a
any size		30 fps	windowing	24 MHz	12 MHz

2.4 I/O control

The OV7692 I/O pad function and driving capability can be easily adjusted. **table 2-2** lists the driving capability and function control registers of the I/O pads.

table 2-2 drive capability and direction control for I/O pads

function	register	R/W	description
output drive capability control	0x0E	RW	Bit[1:0]: Output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[7:0] I/O control	0x0C	RW	Bit[1]: Data output pin status selection 0: tri_state or output_low data output pins at power down, refer to **0x38**[3] 1: Data output pin hold at last status before power down
	0x38	RW	Bit[1:0]: Change status of data and clock output pins 0: tri_state at power down 1: Output low at power down
	0xB5	RW	Bit[5:4]: Data output pin of MIPI 11: tri_state MIPI output pins
Clock I/O control	0x0C	RW	Bit[2]: Clock output pin status selection 0: tri_state/output_low clock output pins at power down, refer to **0x38**[3] 1: Clock output pin hold at last status before power down

2.5 system clock control

The OV7692 PLL allows for an input clock frequency ranging between 6~27MHz or 54MHz, and has a maximum VCO frequency of 200MHz. MIPIClk is for the MIPI and SysClk is for the internal clock of the Image Signal Processing (ISP) block. The PLL can be bypassed by setting register 0x09[3] to 1.

2.6 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

The OV7692 SCCB supported clock rate is dependent on the input clock (XVCLK). **table 2-3** details the supported speeds.

table 2-3 SCCB support speeds

input clock (XVCLK)	SCCB clock
15 ≤ XVCLK ≤ 27 MHz	400 Kbps
10 ≤ XVCLK < 15 MHz	300 Kbps
6 ≤ XVCLK < 10 MHz	150 Kbps

2.7 power up sequence

The OV7692 sensor has a special power supply sequence (see **figure 2-3** and **table 2-4**). The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up. Manually applying a soft reset upon power up is recommended even though the on-chip power-up reset is included.

note Values listed in **figure 2-3** and **table 2-4** are temporary and may change. For further information about the power up sequence, contact your your local OmniVision representative.

figure 2-3 power up sequence

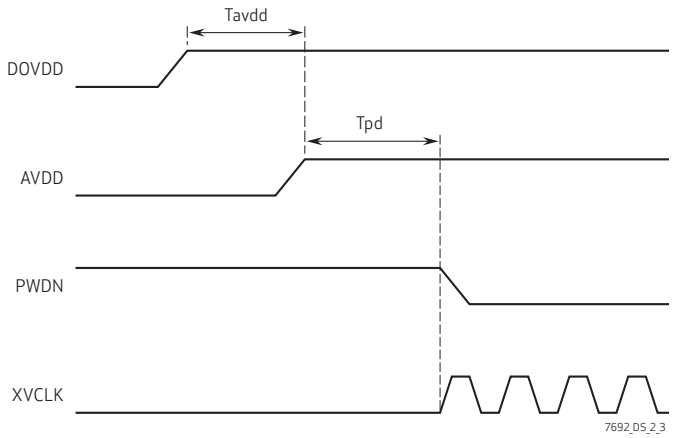


table 2-4 power up sequence specification

timing	min	max
Tavdd	> 0	10 ms
Tpd	1 ms	n/a

2.8 reset

The OV7692 clears all registers and resets them to their default values. When a software reset occurs by setting register 0x12[7] to high, it initiates through the SCCB interface.

2.9 hardware and software standby

Two suspend modes are available for the OV7692:

- hardware standby
- SCCB software standby

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV7692 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

3 block level description

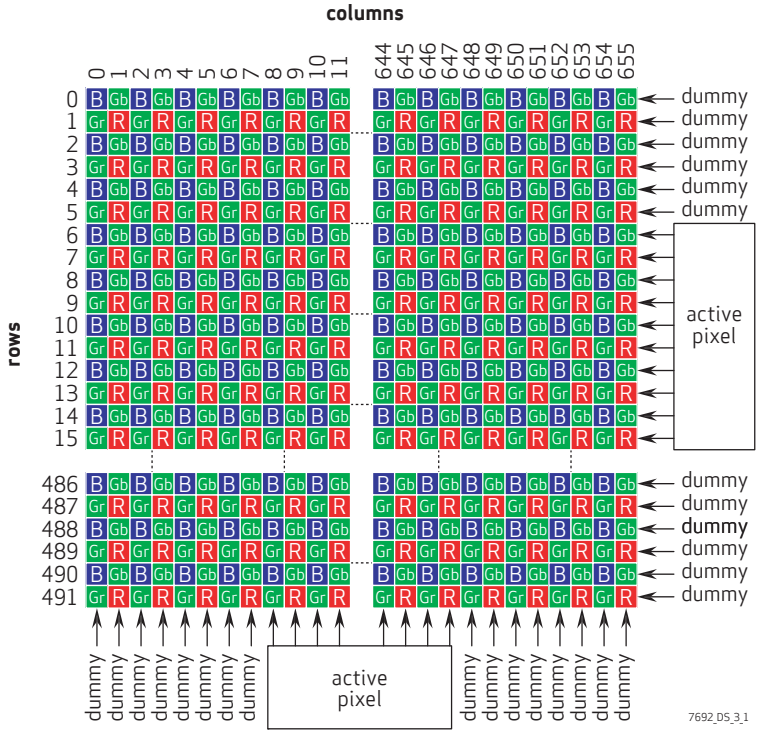
3.1 pixel array structure

The OV7692 sensor has an image array of 656 columns by 504 rows (330,624 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 330,624 pixels, 322,752 (656x492) are active pixels and can be output.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV7692 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

7692 DS 4 1

table 4-1 mirror and flip function control

function	register	description
mirror	0x0C	Bit[6]: mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip	0x0C	Bit[7]: flip ON/OFF select (see **table 4-2**) 0: flip OFF 1: flip ON

table 4-2 flip ON and flip OFF control settings

function	subsampling OFF 0x12[6] = 0	subsampling ON 0x12[6] = 1
flip ON	0x22[5:4] = 2'b00	0x22[5:4] = 2'b10
flip OFF	0x22[5:4] = 2'b00	0x22[5:4] = 2'b01

4.2 image windowing

An image windowing area is defined by four parameters, HS (horizontal start), HW (horizontal width), VS (vertical start), and VH (vertical height). By properly setting the parameters, any portion within the sense array size can be windowed as a visible area. This windowing is achieved by simply masking the pixels outside the windowing window; thus, it will not affect original timing.

figure 4-2 image windowing

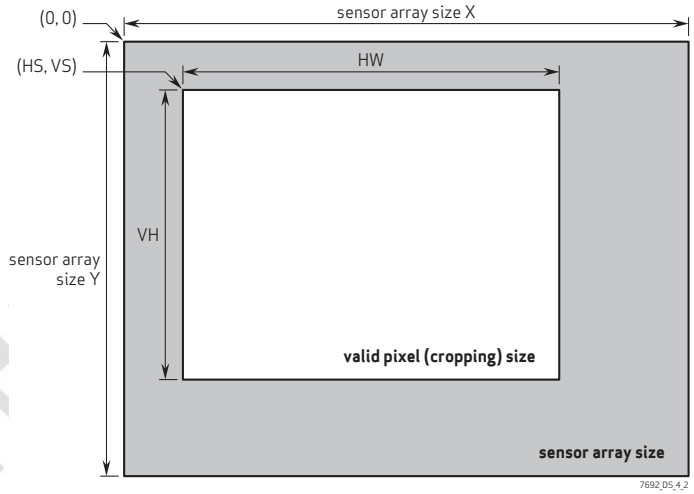


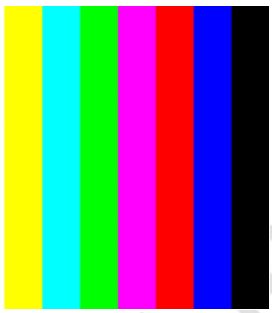
table 4-3 image windowing control functions

address	register name	default value	R/W	description
0x09	HS	0x00	RW	Bit[5:4]: HREF horizontal start point[9:8] high byte
0x17	HS	0x69	RW	Bit[7:0]: HREF horizontal start point[7:0] low byte
0x09	VS	0x00	RW	Bit[7:6]: HREF vertical start point[9:8] high byte
0x19	VS	0x0C	RW	Bit[7:0]: HREF vertical start point[7:0] high byte
0x16	HW	0x03	RW	Bit[6]: HREF horizontal offset[0]
0x18	HW	0xA4	RW	Bit[7:0]: HREF horizontal offset[8:1] high byte HW = {0x18, px16[4]} x 2
0x1A	VH	0x1A	RW	Bit[7:0]: HREF vertical offset[7:0] VH = [0x1A] x 2

4.3 test pattern

For testing purposes, the OV7692 offers one type of test pattern, color bar.

figure 4-3 test pattern



color bar

table 4-4 test pattern selection control

address	register name	default value	R/W	description
0x82	REG82	0x03	RW	Bit[3]: VBAR_EN 0: Test disable 1: Color bar enable

4.4 50/60Hz detection

4.4.1 overview

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50Hz or 60Hz light source so that the basic step of integration time can be determined. Contact your local OmniVision FAE for auto detection settings.

4.5 AEC/AGC algorithms

4.5.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from the SCCB interface. The related registers are in **table 4-5**.

table 4-5 AEC/AGC control functions

function	register address	description
AEC enable	0x13	Bit[0]: Automatic exposure control 0: manual 1: auto
AEC (exposure time)	{0x0F[7:0], 0x10[7:0]}	Exposure Time Control (unit = tline) AEC[15:0] = {0x0F[7:0],0x10[7:0]}
AGC enable	0x13	Bit[2]: Automatic gain control 0: manual 1: auto
AGC gain	{0x15[1:0], 0x00[7:0]}	Gain Control Gain[9:0] = {0x15[1:0], 0x00[7:0]} Gain = (1 + Gain[9]) x (1 + Gain[8]) x (1 + Gain[7]) x (1 + Gain[6]) x (1 + Gain[5]) x (1 +Gain[4]) x (1 + Gain[3:0]/16)
AEC/AGC fast mode	0x13	Bit[7]: AEC/AGC fast mode enable 0: disabled 1: enabled
WPT	0x24	AEC/AGC – Stable Operating Region (Upper Limit)
BPT	0x25	AEC/AGC – Stable Operating Region (Lower Limit)
VPT	0x26	AEC/AGC – Stable Operating Region Bit[7:4]: High nibble of upper limit of fast mode control zone Bit[3:0]: Low nibble of upper limit of fast mode control zone
YAVG	0x04	Frame Luminance Average Level (read only) Automatically updated based on the image output

4.5.2 average-based AEC/AGC

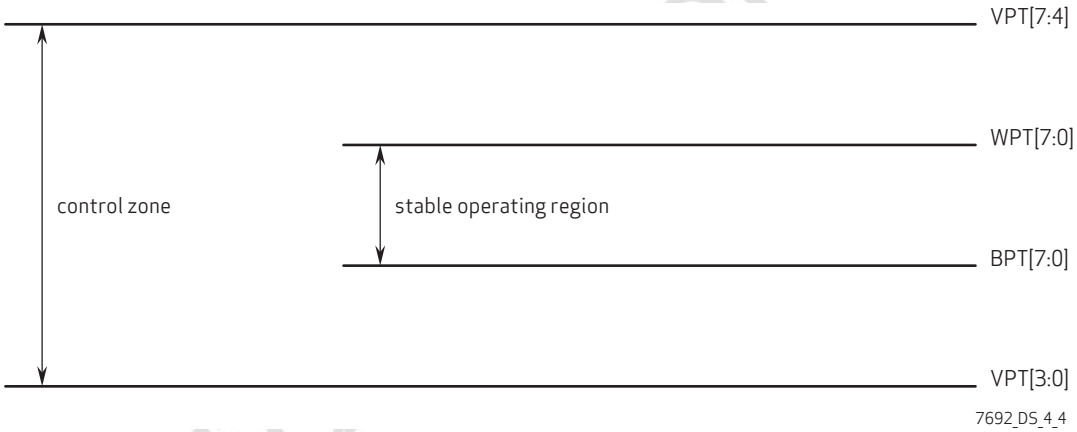
The average-based AEC controls image luminance using registers WPT (0x24) and BPT(0x25). In average-based mode, the value of register WPT(0x24) indicates the high threshold value and the value of register BPT(0x25) indicates the low threshold value. When the target image luminance average value YAVG(0x04) is within the range specified by registers WPT(0x24) and BPT(0x25), the AEC keeps the image exposure. When register YAVG(0x04) is greater than the value in register WPT(0x24), the AEC will decrease the image exposure. When register YAVG(0x04) is less than the value in register BPT(0x25), the AEC will increase the image exposure. Accordingly, the value in register WPT(0x24)

should be greater than the value in register BPT(0x25). The gap between the values of register WPT(0x24) and BPT(0x25) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers WPT(0x24) and BPT(0x25). AEC set to normal mode will allow for single-step increment or decrement in the image exposure to maintain the specified range. A value of 0 in register FASTEN(0x13[7]) will result in normal speed operation and a 1 will result in fast speed operation.

Register VPT(0x26) controls the fast AEC range. If the target image YAVG(0x04) is greater than VPT[7:4] x 16, AEC will decrease by half the current exposure time. If register YAVG(0x04) is less than VPT[3:0] x 16, AEC will increase to 2 times the current exposure time.

figure 4-4 average based AEC/AGC



4.5.3 banding filter

Generally, AC powered light sources usually has a frequency of 60Hz or 50Hz. When the sensor integration time is not an integer multiple to the light period, the image will flicker (horizontal banding). The banding filter will automatically detect current light frequency (when auto detection is on) and provides a rolling horizontal band eliminate function in auto exposure mode. The banding filter is deployed to filter out the banding effect caused by the 50/60 Hz lighting.

For a given operating frequency, band step can be expressed in terms of row timing.

In 50 or 60Hz flicker light, the exposure time must be multiple of the flicker interval to avoid band shown on the image. For 50Hz light, the exposure time must be

$$t_{Exposure} = N/100,$$

and for 60Hz light, the exposure time must be

$$t_{Exposure} = N/120,$$

where N is positive integer.

Since the exposure time, AEC[15:0] is based on row interval, it need to be preset on how many rows is equal to 1/100 second and 1/120 second. Banding filter registers, BD50st and BD60st, are used to set the number of rows of 1/100 and 1/120 second respectively. The banding filter can be calculated by where Maximum Exposure equals to the number of line per frame plus the number of dummy line.

$$\text{BD60st, 60Hz banding filter value} = \frac{1}{120 \times t_{\text{row interval}}} = \frac{\text{frame rate} \times \text{maximum exposure}}{120}$$

$$\text{BD50st, 50Hz banding filter value} = \frac{1}{100 \times t_{\text{row interval}}} = \frac{\text{frame rate} \times \text{maximum exposure}}{100}$$

The band steps for 50Hz and 60Hz light sources can be set in registers 0x50~0x52.

Under strong brightness condition, there is option to allow the exposure time to go below the minimum banding filter value (1/120 or 1/100) to prevent over exposure. When the option is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If option is disabled, the minimum integration time is one minimal band. The option can be set in register 0x13[4].

table 4-6 banding filter functions (sheet 1 of 2)

function	register address	description
banding filter enable	0x13	Bit[5]: Banding filter ON/OFF 0: Disabled 1: Enabled
banding filter option	0x13	Bit[4]: Below banding step value enable 0: Limit the minimum exposure time to 1/100 or 1/120 seconds under any light conditions when banding filter is enabled 1: Allow exposure time to be less than 1/100 or 1/120 seconds under strong light conditions when banding filter is enabled
banding filter mode	0x14	Bit[1]: Banding filter mode, effective when banding filter is enabled 0: Manual mode 1: Auto mode
banding filter manual mode	0x14	Bit[0]: Light source frequency manual selection 0: 60 Hz 1: 50 Hz

table 4-6 banding filter functions (sheet 2 of 2)

function	register address	description
banding filter step value (60Hz)	0x51	Bit[7:0]: BD60St Banding Filter step value for 60Hz light source (8 bits)
banding filter step value (50Hz)	0x50	Bit[7:0]: BD50St Banding Filter step value for 50Hz light source (8 bits)
maximum banding filter step (60Hz)	{0x20[6], 0x21[3:0]	Banding filter maximum allowable number of steps for 60Hz light source (5 bits) 0x20[6]: MSB 0x21[3:0]:LSBs
maximum banding filter step (50Hz)	{0x20[7], 0x21[7:4]}	Banding Filter maximum allowable number of steps for 50Hz light source (5 bits) 0x20[7]: MSB 0x21[7:4]:LSBs

4.6 black level calibration

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. There are three main functions of the BLC:

- combining two ADC data paths into one data path
- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all pixel values based on digital gain

table 4-7 black level calibration control functions

address	register name	default value	R/W	description
0x68	BLC8	0xB4	RW	Bit[3:0]: Target offset
0x69	BLC9	0x12	RW	Bit[1:0]: BLC enable = Bit[1] or Bit[0]

4.7 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

5 image sensor processor digital functions

5.1 ISP_TOP

The ISP_TOP includes all module enable signals, buffer power down control, top level control signals as well as ISP modules that require control bytes (WBC, UV_AVG, and YUV444to422).

- WBC: White Black pixel Canceling is used to detect and remove defect pixels.
- VarioPixel: This module is used to do 2:1 pixel sub sample in horizontal view. There are various ways to use VarioPixel function such as give out the average of 2 pixels, give out the first pixel and drop the second, or give out the second and drop the first.

table 5-1 ISP_TOP related registers (sheet 1 of 2)

sub register address	default value	R/W	description
0x80	0x7E	RW	Bit[7]: vario_en Bit[6]: cip_en Bit[5]: bc_en Bit[4]: wc_en Bit[3]: gamma_en Bit[2]: awb_gain_en Bit[1]: awb_en Bit[0]: lenc_en
0x81	0x41	RW	Bit[7:6]: Reserved Bit[5]: sde_en Bit[4]: uv_adj_en Bit[3]: scale_v_en Bit[2]: scale_h_en Bit[1]: uv_avg_en Bit[0]: Reserved
0x82	0x00	RW	Bit[7]: Bypass ISP Bit[6]: cen_global Bit[5]: Reserved Bit[4]: rblue_p 0: Internal Rblue is the same as ISP port 1: Inverse rblue inside ISP Bit[3]: bar_en Bit[2]: bar_opt_en 0: Color bar data is from vertical counter 1: Color bar data is constant Bit[1:0]: out_sel 00: Raw from WBC 01: Raw from CIP 1x: YUV422

table 5-1 ISP_TOP related registers (sheet 2 of 2)

sub register address	default value	R/W	description
0x83	0x00	RW	Bit[7]: bist_en_vfifo Bit[6]: bist_en_scale Bit[5]: bist_en_cip Bit[4]: bist_en_awb Bit[3]: mem_dec Bit[2]: pwdn_scale Bit[1]: pwdn_cip Bit[0]: pwdn_awb

5.2 ISP DCW, border cutting

This part includes the size registers for ISP input windowing, ISP output windowing, and Scaling input windowing. The ISP input windowing is designed to support digital zoom. The ISP output windowing and Scaling input windowing are both for cutting some border pixels or border lines which are not good enough due to algorithm limitation.

table 5-2 ISP_DCW, border cutting-related registers

sub register address	default value	R/W	description
0xC8	0x20	RW	Bit[1:0]: ih[9:8] High 2 bits of horizontal input size
0xC9	0x80	RW	Bit[7:0]: ih[7:0] Low 8 bits of horizontal input size
0xCA	0x01	RW	Bit[0]: iv[8] Ninth bit of vertical input size
0xCB	0xE0	RW	Bit[7:0]: iv[7:0] Low 8 bits of vertical input size
0xCC	0x02	RW	Bit[1:0]: oh[9:8] High 2 bits of horizontal output size
0xCD	0x80	RW	Bit[7:0]: oh[7:0] Low 8 bits of horizontal output size
0xCE	0x01	RW	Bit[0]: ov[8] Ninth bit of vertical output size
0xCF	0xE0	RW	Bit[7:0]: ov[7:0] Low 8 bits of vertical output size
0xD0	0x48	RW	Bit[7]: win_voff Bit[6:4]: Boundary offset Bit[3:0]: win_hoff

5.3 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image.

table 5-3 AWB-related registers (sheet 1 of 2)

sub register address	default value	R/W	description
0x8C	0x5D	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: g_en Bit[2]: awb_4x Bit[1]: one_zone Bit[0]: avg_all
0x8D	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x8E	0x12	RW	Bit[7]: awb_simple Bit[6:4]: stable_range Bit[3]: awb_bias_stat Bit[2:0]: local_limit
0x8F	0x11	RW	Bit[7:6]: count_area_sel Bit[5:4]: cnt_th Bit[3]: slp_4x Bit[2:0]: count_limit_ctrl
0x90	0x50	RW	Bit[7]: awb_rblue Bit[6]: awb2_sel Bit[5]: awb_preset Bit[4]: awb_simf Bit[3:2]: awb_win Bit[1]: awb_force1 Bit[0]: awb_freeze
0x91	0x01	RW	Bit[5]: aec_sel Bit[4]: calc_sel Bit[2]: awb_big_sel Bit[1]: slp_8x Bit[0]: awb_man_en
0x92	0x00	RW	Bit[7:0]: awb_ky
0x93	0x00	RW	Bit[7:0]: awb_kx
0x94	0x0F	RW	Bit[7:0]: awb_ec
0x95	0x0F	RW	Bit[7:0]: awb_fc
0x96	0xF0	RW	Bit[7:0]: value_top_limit
0x97	0x10	RW	Bit[7:0]: value_bot_limit
0x98	0x00	RW	Bit[7:0]: day_limit

table 5-3 AWB-related registers (sheet 2 of 2)

sub register address	default value	R/W	description
0x99	0x00	RW	Bit[7:0]: a_limit
0x9A	0x30	RW	Bit[7:0]: day_split
0x9B	0x30	RW	Bit[7:0]: a_split
0x9C	0xF0	RW	Bit[7:0]: red_limit
0x9D	0xF0	RW	Bit[7:0]: green_limit
0x9E	0xF0	RW	Bit[7:0]: blue_limit
0x9F	0xFF	RW	Bit[7:0]: awb_b_block
0xA0	0x40	RW	Bit[7:0]: awb_x0
0xA1	0x40	RW	Bit[7:0]: awb_y0
0xA2	0x0F	RW	Bit[7:0]: awb_s

5.4 gamma (GMA)

Gamma (GMA) converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

5.5 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

table 5-4 LENC related registers (sheet 1 of 2)

sub register address	default value	R/W	description
0x85	0x00	RW	Bit[7:5]: Reserved Bit[4]: LENC bias enable Bit[2]: hskip Bit[3]: vskip Bit[1]: sel_deltagain LENC output delta_gain Bit[0]: sel_r LENC output the radius from every pixel to LENC center has more priority than 0x85[1]
0x86	0x00	RW	Bit[7:0]: lc_radius

table 5-4 LENC related registers (sheet 2 of 2)

sub register address	default value	R/W	description
0x87	0x00	RW	Bit[7:0]: lc_xoffset
0x88	0x00	RW	Bit[7:0]: lc_yoffset
0x89	0x00	RW	Bit[7:0]: lc_rgain
0x8A	0x00	RW	Bit[7:0]: lc_ggain
0x8B	0x00	RW	Bit[7:0]: lc_bgain

5.6 color interpolation (CIP)

The color interpolation (CIP) functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

table 5-5 CIP, DNS and sharpen-related registers

sub register address	default value	R/W	description
0xB4	0x06	RW	Bit[5]: edge_mt_man_en Bit[4]: dns_th_man_en Bit[3:0]: edge_th
0xB5	0x08	RW	Bit[7:0]: dns_th_man
0xB6	0x04	RW	Bit[4:0]: edge_mt_man
0xB7	0x10	RW	Bit[7:0]: offset
0xB8	0x1E	RW	Bit[4:0]: base1
0xB9	0x02	RW	Bit[4:0]: base2
0xBA	0x09	RW	Bit[7]: Reserved Bit[6]: gain_sel_en Bit[5:4]: gain_sel 00: gain_4x is limited to 8 01: gain_4x is limited to 16 10: gain_4x is limited to 32 11: gain_4x is limited to 64 Bit[3:2]: dns_th_sel Bit[1:0]: edge_mt_range

5.7 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to cancel crosstalk and to convert images from the RGB domain to YUV domain.

table 5-6 CMX-related registers

sub register address	default value	R/W	description
0xBB	0x2C	RW	Bit[7:0]: m1
0xBC	0x24	RW	Bit[7:0]: m2
0xBD	0x08	RW	Bit[7:0]: m3
0xBE	0x14	RW	Bit[7:0]: m4
0xBF	0x24	RW	Bit[7:0]: m5
0xC0	0x38	RW	Bit[7:0]: m6
0xC1	0x1E	RW	Bit[7]: cmx_bias Bit[6]: m_db Bit[5:0]: m_sign
0xC2	0x00	RW	Bit[1]: vfirst Bit[0]: uv_cnv_opt 0: Average mode 1: Drop mode

5.8 UV adjust (UV_ADJ)

UV adjust (UV_ADJ) is used to reduce chrominance values in low light conditions to improve image quality. The higher AGC gain is, the lower the chrominance values. UV_ADJ has an automatic and manual mode.

5.9 special digital effects (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V using the Sat_u and Sat_v registers. Calculate Y using Y offset, Y gain, and Ybright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, reddish and other image effects which combine the effects already listed.

table 5-7 SDE related registers

sub register address	default value	R/W	description
0xD2	0x00	RW	Bit[7]: fixy_en Bit[6]: neg_en Bit[5]: gray_en Bit[4]: fixv_en Bit[3]: fixu_en Bit[2]: cont_en Bit[1]: sat_en Bit[0]: hue_en
0xD3	0x00	RW	Bit[7:0]: ybright
0xD4	0x20	RW	Bit[7:0]: ygain
0xD5	0x00	RW	Bit[7:0]: yoffset
0xD6	0x80	RW	Bit[7:0]: hue_cos
0xD7	0x00	RW	Bit[7:0]: hue_sin
0xD8	0x40	RW	Bit[7:0]: sat_u
0xD9	0x40	RW	Bit[7:0]: sat_v
0xDA	0x80	RW	Bit[7:0]: ureg
0xDB	0x80	RW	Bit[7:0]: vreg
0xDC	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: SgnSet Hue: sgn0=1, sgn1=0, sgn4=sgn5=0 => 0<theta< pi/2 sgn0=0, sgn1=1, sgn4=sgn5=0 => -pi/2<theta< 0 sgn0=1, sgn1=0, sgn4=sgn5=1 => pi/2<theta< pi sgn0=0, sgn1=1, sgn4=sgn5=1 => -pi<theta< -pi/2 YContrast : sign2 : YOffset sign3: YBrightness

6 image sensor output interface digital functions

6.1 system control

System control registers include clock, reset control, and PLL configure. Individual modules can be reset or clock gated by setting the appropriate registers.

table 6-1 system control related registers

address	register name	default value	R/W	description
0x12	REG12	0x00	RW	Bit[7]: Software reset
0x80	REG80	0x7E	RW	Reset for Individual Block (0: reset block; 1: enable block) Bit[7]: Reset VarioPixel™ Bit[6]: Reset CIP Bit[5]: Reset BC Bit[4]: Reset WC Bit[3]: Reset gamma Bit[2]: Reset AWB_gain Bit[1]: Reset AWB Bit[0]: Reset LENC
0x81	REG81	0x3F	RW	Reset for Individual Block (0: reset block; 1: enable block) Bit[5]: Reset SDE Bit[4]: Reset UV_adjust Bit[3]: Reset scale_v Bit[2]: Reset scale_h Bit[1]: Reset UV_avg Bit[0]: Reset CMX
0xDD	REGDD	0x1C	RW	Reset for Individual Block (0: reset block; 1: enable block) Bit[4:3]: Reset MIPI Bit[2]: Reset ISP

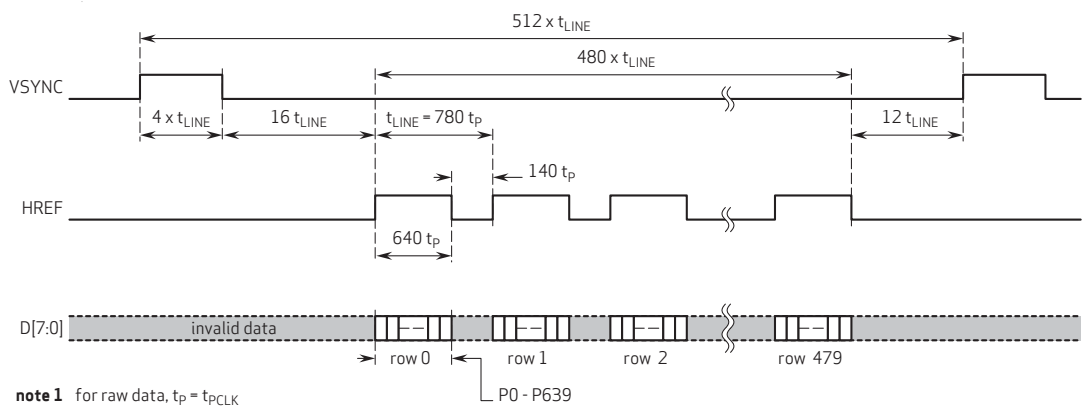
6.2 digital video port (DVP)

6.2.1 overview

The Digital Video Port (DVP) provides 8-bit parallel data output in all formats supported, and extended features including HSYNC mode and test pattern output.

6.2.2 VGA timing

figure 6-1 VGA timing diagram

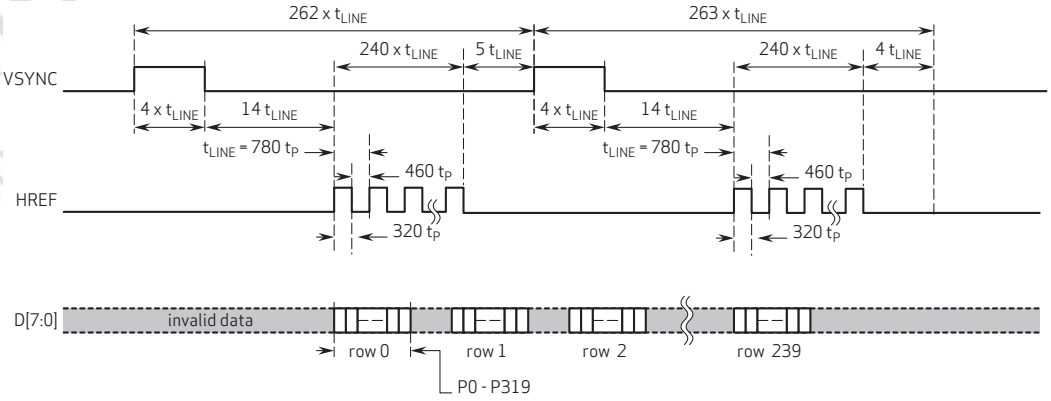


note 1 for raw data, $t_P = t_{PCLK}$

note 2 for YUV/RGB, $t_P = 2 \times t_{PCLK}$

7692_DS_6_1

figure 6-2 QVGA timing diagram



note 1 for YUV/RGB, $t_P = 2 \times t_{PCLK}$ (only to be used with YUV/RGB)

7692_DS_6_2

6.3 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and one bi-directional data lane solution for communication links between components inside a mobile device. The data lane has full support for HS (uni-direction) data transfer mode. Contact your local OmniVision FAE for more details.

7 register tables

The following tables provide descriptions of the device control registers contained in the OV7692. For all register enable/disable bits, enable = 1 and DISABLE = 0. The device slave addresses are 0x78 for write and 0x79 for read.

table 7-1 system control registers (sheet 1 of 22)

address	register name	default value	R/W	description
0x00	GAIN	0x00	RW	AGC Gain Control 10 bits (**REG15**[1:0] as MSB 2 bits) **REG15**[1:0]: digital gain Range 1x to 128x Gain = (Bit[9]+1) x (Bit[8]+1) x (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16)
0x01	BGAIN	0x40	RW	AWB Blue Gain Control Range: 0 to 4x([00] to [FF])
0x02	RGAIN	0x40	RW	AWB Red Gain Control Range: 0 to 4x([00] to [FF])
0x03	GGAIN	0x40	RW	AWB Green Gain Control Range: 0 to 4x([00] to [FF])
0x04	YAVG	–	R	Frame Average Level Automatically updated based on chip output format
0x05	BAVG	–	R	B Pixel Average (ISP) Automatically updated based on chip output format
0x06	RAVG	–	R	R Pixel Average (ISP) Automatically updated based on chip output format
0x07	GAVG	–	R	G Pixel Average (ISP) Automatically updated based on chip output format
0x08	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 2 of 22)

address	register name	default value	R/W	description
0x09	REG09	0x00	RW	Bit[7:6]: Vertical window start line control (MSB) (see **VSTART** (0x19) for LSBs) Bit[5:4]: Horizontal window start point control (MSB) (see 0x17 for LSBs) Bit[3]: Bypass PLL Bit[2]: Average selection 0: Use ISP output as data source 1: Use sensor output as data source Bit[1]: PLL_RST Manual reset PLL Bit[0]: ADCLK_A_low Disable ADCLK_A
0x0A	PIDH	0x76	R	Product ID Number MSB (Read only)
0x0B	PIDL	0x92	R	Product ID Number LSB (Read only)
0x0C	REG0C	0x16	RW	Bit[7]: Vertical flip Bit[6]: Horizontal mirror Bit[5]: BR swap when in RGB format Bit[4]: YU/YV swap when in YUV format Bit[3]: MLSB swap in DVP output Bit[2]: Clock output power-down pin status 0: Tri-state VSYNC, PCLK, HREF and CHSYNC pins upon power-down 1: VSYNC, PCLK and HREF hold Bit[1]: Data output pin status selection at power down 0: Tri-state data output pin at power-down 1: Data output pin hold at last status before power down Bit[0]: Reserved
0x0D	REG0D	0x44	RW	Bit[7]: Reserved Bit[6:4]: VS start point 000: Enable option to add dummy line before VSYNC 001~111: VSYNC option without dummy lines Bit[3]: Reserved Bit[2:0]: VS width

table 7-1 system control registers (sheet 3 of 22)

address	register name	default value	R/W	description
0x0E	REG0E	0x00	RW	Bit[7:4]: Reserved Bit[3]: Sleep mode enable 0: Normal mode 1: Sleep mode Bit[2]: Output data range selection 0: Full range 1: Data from [10] to [F0] (8 MSBs) Bit[1:0]: Output drive current select 00: 1x 01: 2x 10: 3x 11: 4x
0x0F	AECH	0x00	RW	MSBs of Automatic Exposure Control - AEC[15:8]
0x10	AECL	0x00	RW	LSBs of Automatic Exposure Control - AEC[7:0] Exposure time TEX = t_{LINE} × AEC[15:0] Note: The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period.
0x11	CLKRC	0x00	RW	Bit[7]: DPLLEN Internal frequency doubler of input clock ON/OFF selection (with **REG3E**[7] (0x3E)) 0: OFF 1: ON Bit[6]: Use external clock directly (at most div-2 available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) Range: [0 0000] to [1 1111]

table 7-1 system control registers (sheet 4 of 22)

address	register name	default value	R/W	description
0x12	REG12	0x00	RW	Bit[7]: System register reset 0: No change 1: Resets system Bit[6]: Skip mode enable Bit[5]: ITU656 protocol ON/OFF selection Bit[4]: Select sensor original raw data output Bit[3:2]: RGB output format control x0: Not used 01: RGB565 11: RGB444 Bit[1:0]: Output format control 00: YUV 01: Bayer RAW 10: RGB 11: Bayer RAW
0x13	REG13	0xE5	RW	Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - step size limit 0: Step size limited to vertical blank 1: Unlimited step size (current AEC value) Bit[5]: Banding filter ON/OFF Bit[4]: Enable AEC below banding value Bit[3]: Tp level exposure ON/OFF selection Bit[2]: AGC auto/manual control selection Bit[1]: AWB auto/manual control selection Bit[0]: Exposure auto/manual control selection

table 7-1 system control registers (sheet 5 of 22)

address	register name	default value	R/W	description
0x14	REG14	0x30	RW	Bit[7]: Field0 and Field1 have different frame length 0: Different frame length 1: Same frame length Bit[6:4]: Automatic gain ceiling Maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x Bit[3]: Reserved Bit[2]: Drop VSYNC output of corrupt frame Bit[1]: Manual 50/60 selection 0: Auto mode 1: Manual mode Bit[0]: Manually set banding with REG14[1] (0x14) 0: 60 Hz 1: 50 Hz

table 7-1 system control registers (sheet 6 of 22)

address	register name	default value	R/W	description
0x15	REG15	0x00	RW	Bit[7]: Auto frame rate control on/off selection Bit[6:4]: Auto frame rate max rate control 000: No reduction of frame rate 001: Max reduction to 1/2 frame rate 010: Max reduction to 1/3 frame rate 011: Max reduction to 1/4 frame rate 111: Max reduction to 1/8 frame rate Bit[3:2]: Auto frame rate active point control 00: Add frame when AGC reach 2x gain 01: Add frame when AGC reach 4x gain 10: Add frame when AGC reach 8x gain 11: Add frame when AGC reach 16x gain Bit[1:0]: Digital gain 00: No digital gain 01: 2x 10: Not applicable 11: 4x
0x16	REG16	0x03	RW	Bit[7]: Reserved Bit[6]: Horizontal sensor size[0] (see **HSIZE**[7:0] (0x18) for MSBs) Bit[5]: Roff1 Vertical window start line adjustment Bit[4]: Hoff1 Horizontal window start line adjustment Bit[3]: Reserved Bit[2]: Enable slowed PCLK for YUV size less that QVGA Bit[1:0]: Reserved
0x17	HSTART	0x69	RW	Horizontal Window Start Point Control (LSBs)
0x18	HSIZE	0xA4	RW	Horizontal Sensor Size[8:1] Actual horizontal size = 2 × {**HSIZE**[7:0], **REG16**[6]}
0x19	VSTART	0x0C	RW	Vertical Window Start Line Control (LSBs)
0x1A	VSIZE	0xF6	RW	Vertical Sensor Size 8 bits Actual vertical size = 2 × **VSIZE**[7:0]

table 7-1 system control registers (sheet 7 of 22)

address	register name	default value	R/W	description
0x1B	SHFT	0x19	RW	Pixel Shift
0x1C	MIDH	0x7F	R	Manufacturer ID Byte: High
0x1D	MIDL	0xA2	R	Manufacturer ID Byte: Low
0x1E	REG1E	0xB1	RW	Bit[7]: Reserved Bit[6]: CLK_CHG 0: Reserved 1: Freeze AEC/AGC and disable DropF Bit[5]: Ph1_arr_en 0: Keep Ph1_arr output to array low 1: No limit on Ph1_arr Bit[4]: BdcAEC 0: Reserved 1: Do AEC/AGC when alternating 50/60 Bit[3:2]: Reserved Bit[1]: AddLT1F Less than one frame dummy lines Bit[0]: EXPNG 0: Limit AEC step and disable the second precharge timing 1: No limit on AEC step and enable the second precharge timing
0x1F	LAEC	0x00	RW	tp level exposure control when exposure is less than one line (see **REG37**[5] (0x37) for manual mode)
0x20	REG20	0x00	RW	Bit[7]: MSB of banding filter maximum step for 50 Hz light source (4 LSBs are in **AECGM**[7:4] (0x21)) Bit[6]: MSB of banding filter maximum step for 60 Hz light source (4 LSBs are in **AECGM**[3:0] (0x21)) Bit[5:0]: Manual banding counter
0x21	AECGM	0x44	RW	Bit[7:4]: Banding filter maximum step for 50 Hz light source (see register **REG20**[7] (0x20) for MSB) Bit[3:0]: Banding filter maximum step for 60 Hz light source (see register **REG20**[6] (0x20) for MSB)

table 7-1 system control registers (sheet 8 of 22)

address	register name	default value	R/W	description
0x22~ 0x23	RSVD	–	–	Reserved
0x24	WPT	0x78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
0x25	BPT	0x68	RW	AGC/AEC - Stable Operating Region (Lower Limit)
0x26	VPT	0xD4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit of fast mode control zone Bit[3:0]: High nibble of lower limit of fast mode control zone
0x27	REG27	0x00	RW	Bit[7]: Black sun enable (digital part) Bit[6:4]: Vertical window position adjustment (for center average used) Bit[3]: Reserved Bit[2:0]: Horizontal window position adjustment (for center average used)
0x28	REG28	0x00	RW	Bit[7]: RNEG Output negative data Bit[6]: HGCHSW HREF changes to HSYNC Bit[5]: HSNEG HSYNC reverse Bit[4]: HRNEG HREF reverse Bit[3]: NOVS Bit[2]: VS_EDGE VSYNC option 0: VSYNC active on falling edge of PCLK 1: VSYNC active on rising edge of PCLK Bit[1]: VSNEG VSYNC negative Bit[0]: Reserved
0x29	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 9 of 22)

address	register name	default value	R/W	description
0x2A	EXHCL	0x30	RW	Bit[7]: Contrast center auto adjustment 0: Manual mode by setting REGD5[7:0] (0xD5) 1: Auto mode Bit[6:4]: Dummy pixel insert in horizontal direction 3 MSBs (see register EXHCH (0x2B) for LSBs) Bit[3:0]: Dummy line 4 MSBs
0x2B	EXHCH	0x0B	RW	Dummy Pixel Insert in Horizontal Direction 8 LSBs (see register EXHCL[6:4] (0x2A) for MSBs)
0x2C	DM_LN	0x00	RW	Dummy Line 8 LSBs (see register EXHCL[3:0] (0x2A) for MSBs)
0x2D	ADVFL	0x00	RW	Dummy Line Insert in Vertical Direction LSBs (1 bit equals 1 line) (see register ADVFH (0x2E) for MSBs)
0x2E	ADVFH	0x00	RW	Dummy Line Insert in Vertical Direction MSBs (1 bit equals 1 line) (see register ADVFL (0x2D) for LSBs)
0x2F	RSVD	–	–	Reserved
0x30	R_PLL0	0x04	RW	Bit[7:5]: DVP 3 LSBs PLL loop divider ratio: 32-DIVP[4:0] Bit[4:2]: Reserved Bit[1:0]: Pre-divider 00: /1 01: /1.5 10: /2 11: /3
0x31	R_PLL1	0x83	RW	Bit[7:6]: SELD5 System clock divider 00: /1 01: /1 10: /2 11: /2.5 Bit[5:2]: DIVS Divide VCO output ratio: 1/(DIVS+1) Bit[1:0]: DIVP 2 MSBs PLL loop divider (see REG09[3] (0x09) for bypass PLL) (see REGB4[3:0] (0xB4) (MIPI_bank) for MIPI clock divider)
0x32~ 0x35	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 10 of 22)

address	register name	default value	R/W	description
0x36	REG36	0x43	RW	Bit[7:3]: Reserved Bit[2]: Optical black window option 0: Full size 1: Skip mode Bit[1]: Do BLC at format change 0: Disable 1: Enable Bit[0]: Reserved
0x37	REG37	0x0C	RW	Bit[7:6]: Reserved Bit[5]: Enable manual less than one row exposure 0: Disable 1: Enable Bit[4]: PCLKO_D2 0: No divider 1: Output PCLK divided by 2 Bit[3]: PCLK_PAD (works with REG37[4] (0x37)) 0: PCLK is as the same as system clock 1: PCLK is double system clock Bit[2:0]: Reserved
0x38	3LSBs(ADC)	0x10	RW	Bit[7]: Input clock divider 0: Divided by 2 1: No divider Bit[6:4]: Stream OFF control VSYNC Y HREF PCLK 0xx: f f f f 100: k k k f 101: k k k k 11x: hz hz hz hz Note: f stand for free running hz stand for high impedance Bit[3]: Output low at power down 0: Disable 1: Enable Bit[2:1]: Reference compensation cap Bit[0]: Reserved
0x39	REG39	0x00	RW	Bit[7:5]: Reserved Bit[4]: Txlength Adjust gap in SA1 timing Bit[3:2]: Adjust HSYNC signal Bit[1:0]: Reserved
0x3A~ 0x3D	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 11 of 22)

address	register name	default value	R/W	description
0x3E	REG3E	0x20	RW	Bit[7]: Adjust input system clock Bit[6]: PCLK output gated 0: PCLK always output 1: PCLK output qualified by HREF Bit[5]: Get 1/2 or 1/4 of regular PCLK (used with **REG5E**[5:4] (0x5E)) Bit[4]: MIPI clock selection 0: When in RAW format 1: When in YUV/RGB format Bit[3:0]: Reserved
0x3F	REG3F	0x44	RW	Bit[7]: Reserved Bit[6]: Reverse PCLK 0: HREF goes high at PCLK rising edge 1: HREF goes high at PCLK falling edge Bit[5]: Reverse DSPclk Bit[4:0]: Reserved
0x40~ 0x4F	RSVD	–	–	Reserved
0x50	BD50ST	0x9A	RW	50Hz Banding AEC 8 bits
0x51	BD60ST	0x80	RW	60Hz Banding AEC 8 bits
0x52~ 0x59	RSVD	–	–	Reserved
0x5A	UV_CTR0	0x01	RW	Slope of UV Curve
0x5B	UV_CTR1	0xFF	RW	Bit[7:6]: UV adjustment gain high threshold control 2 LSBs (3 MSBs are in **UV_CTR2**[7:5] 0x5C)) Bit[5:0]: Y intercept point of UV curve
0x5C	UV_CTR2	0x1F	RW	Bit[7:5]: UV adjustment gain high threshold control 3 MSBs (2 LSBs are in **UV_CTR1**[7:6] (0x5B)) Bit[4:0]: Reserved

table 7-1 system control registers (sheet 12 of 22)

address	register name	default value	R/W	description
0x5D	UV_CTR3	0x00	RW	Bit[7:4]: UV adjustment gain low threshold control Bit[3]: AWB bias setting control 0: AWB bias set by BLC target 1: AWB bias set by REGE5[7:0] (0xE5) Bit[2]: Reserved Bit[1]: Center average selection 0: Choose whole image average value to system 1: Choose center 1/4 average value to system Bit[0]: Reserved
0x5E	REG5E	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: Divided PCLK Bit[3:2]: Reserved Bit[1:0]: PCLK delay option
0x5F~ 0x60	RSVD	–	–	Reserved
0x61	REG61	0x00	RW	Bit[7]: Reserved Bit[6]: Test pattern output.enable Bit[5:4]: Output select 00: 10-bit pattern 01: 10-bit pattern (model 2) 10: 8-bit pattern 11: 8-bit pattern (model 2) Bit[3:0]: Reserved
0x62	REG62	0x10	RW	Bit[7]: Debug mode only Bit[6]: AGC2x Do BLC Bit[5]: Always do BLC Bit[4:0]: Reserved
0x63	RST_CTRL	0x00	RW	Bit[7:5]: Reserved Bit[4]: Reset DSP Bit[3]: Reset SRAM of VFIFO Bit[2]: Reset PCLK domain in MIPI/VFIFO Bit[1]: Reserved Bit[0]: Reset SCLK domain in MIPI/VFIFO

table 7-1 system control registers (sheet 13 of 22)

address	register name	default value	R/W	description
0x64	VFIFO00	0x11	RW	Bit[7:3]: Indicate ratio of SCLK and PCLK 001: PCLK is double of SCLK 010: PCLK is the same as SCLK 100: PCLK is half of the SCLK Bit[2]: Enable manual mode of start size (see **VFIFO02** (0x66) for the value of start size) Bit[1:0]: Reserved
0x65	VFIFO01	0x00	RW	Bit[7]: Start size calculation trigger control 0: Begin of frame or end of each row 1: Begin of frame Bit[6:4]: Reserved Bit[3]: Start size subtle adjustment Bit[2:0]: Reserved
0x66	VFIFO02	0x00	RW	Indicate Start Size in Manual Mode (works with **VFIFO00**[2] (0x64))
0x67	VFIFO03	0x20	RW	Bit[7:4]: Reserved Bit[3:0]: Offset on start size
0x68	BLC8	0xB4	RW	Bit[7:6]: Reserved Bit[5:4]: BLC_R, BLC_B x0: Use R/Gr channel offset for all channels 01: Use B/Gb channel offset for all channels 11: Use all four channel offsets Bit[3:0]: Target offset
0x69	BLC9	0x12	RW	Bit[7]: Reserved Bit[6:3]: BLC window selection Bit[2]: Bypass BLC Bit[1:0]: BLC enable = Bit[1] || Bit[0]

table 7-1 system control registers (sheet 14 of 22)

address	register name	default value	R/W	description
0x6A	BLCA	0x00	RW	Bit[7]: Output BLC value select 0: Blue line 1: Red line Bit[6:5]: Output BLC value of channel select 00: G value 10: BR value x1: Target value Bit[4]: Use one BLC value for all channels Bit[3]: Reserved Bit[1:0]: BLC target offset adjustment with gain base selection 00: Base = 0 01: Base = 1 10: Base = 2 11: Base = 4 when x N, Target = BLC6[2:0]*4+ base * N/4
0x6B	BLCOUT	0x00	R	Readout BLC Values
0x6C	RSVD	–	–	Reserved
0x6D	5060_LUM2	–	R	Bit[7:4]: Reserved Bit[3:0]: 5060_luminance[19:16] MSBs
0x6E	5060_LUM1	–	R	Bit[7:0]: 5060_luminance[15:8]
0x6F	5060_LUM0	–	R	Bit[7:0]: 5060_luminance[7:0] LSBs
0x70	5060_0	0x00	RW	Bit[7:6]: Reserved Bit[5]: Threshold time divide 0: No division 1: Divide by 8 Bit[4]: Low light limit enable Bit[3]: Reversed sigma delta input Bit[2]: Band default 0: Set default as 60Hz 1: Set default as 50Hz Bit[1:0]: Threshold of time counter 00: 1s 01: 2s 10: 4s 11: 8s

table 7-1 system control registers (sheet 15 of 22)

address	register name	default value	R/W	description
0x71	5060_1	0x00	RW	Bit[7]: r_band_manual 0: Auto mode 1: Manual mode Bit[6]: Reset band statistics Bit[5]: Calculate sum automatic 0: Disable 1: Enable Bit[4]: Band counter enable judge band based on **5060_1**[3:0] (0x71) 0: Disable 1: Enable Bit [3:0]: Band counter Counter threshold for band change
0x72	5060_2	0x00	RW	Bit[7:6]: Low light limit definition 00: 128/600s 01: 2 x 128/600s 10: 3 x 128/600s Bit[5:0]: Threshold to detect whether it is in low light environment
0x73	5060_3	0x00	RW	Bit[7:0]: Threshold counter of low light
0x74	5060_4	0x20	RW	Bit[7:0]: Threshold for low sum value
0x75	5060_5	0x70	RW	Bit[7:0]: Threshold for high sum value
0x76	5060_6	0x00	RW	Bit[7:0]: Low threshold of light meter high 8 bits
0x77	5060_7	0x00	RW	Bit[7:0]: Low threshold of light meter low 8 bits
0x78	5060_8	0x01	RW	Bit[7:0]: High threshold of light meter high 8 bits
0x79	5060_9	0x2C	RW	Bit[7:0]: High threshold of light meter low 8 bits
0x7A	5060_A	0x4E	RW	Bit[7:0]: Clock period for sample number high 8 bits
0x7B	5060_B	0x1F	RW	Bit[7:0]: Clock period for sample number low 8 bits
0x7C	5060_C	0x00	RW	Indirect Register Address
0x7D	5060_D	0x00	RW	Indirect Register Value
0x7E	5060_E	0x00	RW	Bit[7:4]: 5060 bias current option Bit[3:0]: VSYNC start offset (available when 0x08[6:4] = 0)

table 7-1 system control registers (sheet 16 of 22)

address	register name	default value	R/W	description
0x7F	RSVD	–	–	Reserved
0x80	REG80	0x7E	RW	Bit[7]: vario_en Bit[6]: cip_en Bit[5]: bc_en Bit[4]: wc_en Bit[3]: gamma_en Bit[2]: awb_gain_en Bit[1]: awb_en Bit[0]: lenc_en
0x81	REG81	0x41	RW	Bit[7:6]: Reserved Bit[5]: sde_en Bit[4]: uv_adj_en Bit[3]: scale_v_en Bit[2]: scale_h_en Bit[1]: uv_avg_en Bit[0]: cmx_en
0x82	REG82	0x00	RW	Bit[7]: bypass ISP Bit[6]: cen_global Bit[5]: Reserved Bit[4]: rblue_p 0: Internal rblue is the same as ISP port 1: Inverse rblue inside ISP Bit[3]: bar_en Bit[2]: bar_opt_en 0: Color bar data is from vertical counter – YUV422 1: Color bar data is constant Bit[1]: out_sel 00: Raw from WBC 01: Raw from CIP 1x: YUV422
0x83	REG83	0x00	RW	Bit[7]: bist_en_vfifo Bit[6]: bist_en_scale Bit[5]: bist_en_cip Bit[4]: bist_en_awb Bit[3]: mem_dec Bit[2]: pwdn_scale Bit[1]: pwdn_cip Bit[0]: pwdn_awb
0x84	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 17 of 22)

address	register name	default value	R/W	description
0x85	REG85	0x00	RW	lc_ctrl[7:0] Bit[7:5]: Reserved Bit[4]: LENC bias enable Bit[3]: VSKIP Bit[2]: HSKIP Bit[1]: sel_deltagain LENC output delta_gain Bit[0]: sel_r LENC output the radius from every pixel to LENC center. Bit[0] has more priority than Bit[1]
0x86	REG86	0x00	RW	Bit[7:0]: lc_radius
0x87	REG87	0x00	RW	Bit[7:0]: lc_xoffset
0x88	REG88	0x00	RW	Bit[7:0]: lc_yoffset
0x89	REG89	0x00	RW	Bit[7:0]: lc_rgain
0x8A	REG8A	0x00	RW	Bit[7:0]: lc_ggain
0x8B	REG8B	0x00	RW	Bit[7:0]: lc_bgain
0x8C	REG8C	0x5D	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: g_en Bit[2]: awb_4x Bit[1]: one_zone Bit[0]: avg_all
0x8D	REG8D	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x8E	REG8E	0x12	RW	Bit[7]: awb_simple Bit[6:4]: stable_range Bit[3]: awb_bias_stat Bit[2:0]: local_limit
0x8F	REG8F	0x11	RW	Bit[7:6]: count_area_sel Bit[5:4]: cnt_th Bit[3]: slp_4x Bit[2:0]: count_limit_ctrl
0x90	REG90	0x50	RW	Bit[7]: awb_rblue Bit[6]: awb2_sel Bit[5]: awb_preset Bit[4]: awb_simf Bit[3:2]: awb_win Bit[1]: awb_force1 Bit[0]: awb_freeze

table 7-1 system control registers (sheet 18 of 22)

address	register name	default value	R/W	description
0x91	REG91	0x01	RW	Bit[7:6]: aec_sel Bit[5]: aec_sel Bit[4]: calc_sel Bit[2]: awb_big_sel Bit[1]: slp_8x Bit[0]: awb_man_en
0x92	REG92	0x00	RW	Bit[7:0]: awb_ky
0x93	REG93	0x00	RW	Bit[7:0]: awb_kx
0x94	REG94	0x0F	RW	Bit[7:0]: awb_ec
0x95	REG95	0x0F	RW	Bit[7:0]: awb_fc
0x96	REG96	0xF0	RW	Bit[7:0]: value_top_limit
0x97	REG97	0x10	RW	Bit[7:0]: value_bot_limit
0x98	REG98	0x00	RW	Bit[7:0]: day_limit
0x99	REG99	0x00	RW	Bit[7:0]: a_limit
0x9A	REG9A	0x30	RW	Bit[7:0]: day_split
0x9B	REG9B	0x30	RW	Bit[7:0]: a_split
0x9C	REG9C	0xF0	RW	Bit[7:0]: red_limit
0x9D	REG9D	0xF0	RW	Bit[7:0]: green_limit
0x9E	REG9E	0xF0	RW	Bit[7:0]: blue_limit
0x9F	REG9F	0xFF	RW	Bit[7:0]: awb_b_block
0xA0	REGA0	0x40	RW	Bit[7:0]: awb_x0
0xA1	REGA1	0x40	RW	Bit[7:0]: awb_y0
0xA2	REGA2	0x0F	RW	Bit[7:0]: awb_s
0xA3	REGA3	0x10	RW	YST1
0xA4	REGA4	0x12	RW	YST2
0xA5	REGA5	0x35	RW	YST3
0xA6	REGA6	0x5A	RW	YST4
0xA7	REGA7	0x69	RW	YST5
0xA8	REGA8	0x76	RW	YST6
0xA9	REGA9	0x80	RW	YST7
0xAA	REGAA	0x88	RW	YST8
0xAB	REGAB	0x8F	RW	YST9

table 7-1 system control registers (sheet 19 of 22)

address	register name	default value	R/W	description
0xAC	REGAC	0x96	RW	YST10
0xAD	REGAD	0xA3	RW	YST11
0xAE	REGAE	0xAF	RW	YST12
0xAF	REGAF	0xC4	RW	YST13
0xB0	REGB0	0xD7	RW	YST14
0xB1	REGB1	0xE8	RW	YST15
0xB2	REGB2	0x20	RW	YSLP15
0xB3	REGB3	0x00	RW	Bit[7:6]: Reserved Bit[5]: gma_bias enable Bit[4:0]: wbc_ctrl_2 Bit[4]: Threshold enable Bit[3:0]: Threshold
0xB4	REGB4	0x06	RW	Bit[5]: edge_mt_man_en Bit[4]: dns_th_man_en Bit[3:0]: edge_th
0xB5	REGB5	0x08	RW	Bit[7:0]: dns_th_man
0xB6	REGB6	0x04	RW	Bit[4:0]: edge_mt_man
0xB7	REGB7	0x10	RW	Bit[7:0]: Offset
0xB8	REGB8	0x1E	RW	Bit[7:5]: Base1 Bit[4:0]: Base1
0xB9	REGB9	0x02	RW	Bit[7:5]: Base2 Bit[4:0]: Base2
0xBA	REGBA	0x09	RW	Bit[7]: Reserved Bit[6]: gain_sel_en Bit[5:4]: gain_sel 00: gain_4x is limited to 8 01: gain_4x is limited to 16 10: gain_4x is limited to 32 11: gain_4x is limited to 64 Bit[3:2]: dns_th_sel Bit[1:0]: edge_mt_range
0xBB	REGBB	0x2C	RW	Bit[7:0]: m1
0xBC	REGBC	0x24	RW	Bit[7:0]: m2
0xBD	REGBD	0x08	RW	Bit[7:0]: m3
0xBE	REGBE	0x14	RW	Bit[7:0]: m4
0xBF	REGBF	0x24	RW	Bit[7:0]: m5

table 7-1 system control registers (sheet 20 of 22)

address	register name	default value	R/W	description
0xC0	REGC0	0x38	RW	Bit[7:0]: m6
0xC1	REGC1	0x1E	RW	Bit[7]: cmx_bias Bit[6]: m_db Bit[5:0]: m_sign
0xC2	REGC2	0x00	RW	Bit[7:2]: Reserved Bit[1]: vfirst Bit[0]: uv_cnv_opt 0: Average mode 1: Drop mode
0xC3	REGC3	0x80	RW	Bit[7]: win_sel Bit[6]: scale_man Bit[5]: h_round Bit[4]: h_drop Bit[3:2]: v_div_man Bit[1:0]: h_div_man
0xC4	REGC4	0x02	RW	Bit[7:3]: Not used Bit[2:0]: xsc_man[10:8]
0xC5	REGC5	0x00	RW	Bit[7:0]: xsc_man[7:0]
0xC6	REGC6	0x02	RW	Bit[7:3]: Not used Bit[2:0]: ysc_man[10:8]
0xC7	REGC7	0x00	RW	Bit[7:0]: ysc_man[7:0]
0xC8	REGC8	0x02	RW	Bit[7:2]: Not used Bit[1:0]: ih[9:8] High 2 bits of horizontal input size
0xC9	REGC9	0x80	RW	Bit[7:0]: ih[7:0] Low 8 bits of horizontal input size
0xCA	REGCA	0x01	RW	Bit[7:1]: Not used Bit[0]: iv[8] Ninth bit of vertical input size
0xCB	REGCB	0xE0	RW	Bit[7:0]: iv[7:0] Low 8 bits of vertical input size
0xCC	REGCC	0x02	RW	Bit[7:2]: Not used Bit[1:0]: oh[9:8] High 2 bits of horizontal output size
0xCD	REGCD	0x80	RW	Bit[7:0]: oh[7:0] Low 8 bits of horizontal output size

table 7-1 system control registers (sheet 21 of 22)

address	register name	default value	R/W	description
0xCE	REGCE	0x01	RW	Bit[7:1]: Not used Bit[0]: ov[8] Ninth bit of vertical output size
0xCF	REGCF	0xE0	RW	Bit[7:0]: ov[7:0] Low 8 bits of vertical output size
0xD0	REGD0	0x48	RW	Bit[7:0]: boundary offset Bit[3:0]: win_hoff Bit[7:4]: win_voff
0xD1	RSVD	–	–	Reserved
0xD2	REGD2	0x00	RW	Bit[7]: fixy_en Bit[6]: neg_en Bit[5]: gray_en Bit[4]: fixv_en Bit[3]: fixu_en Bit[2]: cont_En Bit[1]: sat_En Bit[0]: hue_En
0xD3	REGD3	0x00	RW	Bit[7:0]: ybright
0xD4	REGD4	0x20	RW	Bit[7:0]: ygain
0xD5	REGD5	0x00	RW	Bit[7:0]: yoffset
0xD6	REGD6	0x80	RW	Bit[7:0]: hue_cos
0xD7	REGD7	0x00	RW	Bit[7:0]: hue_sin
0xD8	REGD8	0x40	RW	Bit[7:0]: sat_u
0xD9	REGD9	0x40	RW	Bit[7:0]: sat_v
0xDA	REGDA	0x80	RW	Bit[7:0]: UREG
0xDB	REGDB	0x80	RW	Bit[7:0]: VREG
0xDC	REGDC	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: SgnSet Hue : sgn0=1, sgn1=0, sgn4=sgn5=0 => 0<theta< pi/2 sgn0=0, sgn1=1, sgn4=sgn5=0 => -pi/2<theta< 0 sgn0=1, sgn1=0, sgn4=sgn5=1 => pi/2<theta< pi sgn0=0, sgn1=1, sgn4=sgn5=1 => -pi<theta< -pi/2 YContrast : sign2 : YOffset sign3 : YBrightness

table 7-1 system control registers (sheet 22 of 22)

address	register name	default value	R/W	description
0xDD	REGDD	0x1C	RW	Bit[7]: snr_rst_ctrl2 Disable PCLK (MIPI) at SA1 Bit[6]: snr_rst_ctrl1 Disable SCLK (MIPI) at SA1 Bit[5]: snr_rst_ctrl0 Disable SCLK (DSP) at SA1 Bit[4]: gate_clk_ctrl2 0: Disable PCLK (MIPI) 1: Reserved Bit[3]: gate_clk_ctrl1 0: Disable SCLK (MIPI) 1: Reserved Bit[2]: gate_clk_ctrl0 0: Disable SCLK (DSP) 1: Reserved Bit[1:0]: BIST control
0xDE	RSVD	–	–	Reserved
0xDF	REGDF	0x11	RW	vario_sel[7:0] Bit[7:6]: VarioPixel mode for B Bit[5:4]: VarioPixel mode for Gb Bit[3:2]: VarioPixel mode for Gr Bit[1:0]: VarioPixel mode for R 00: Average mode 01: Select second pixel 1x: Select first pixel
0xE0	REGE0	0x00	RW	Bit[7:0]: reg_addr
0xE1	REGE1	–	R	Bit[7:0]: reg_dout
0xE2	AWBBIAS_MAN	0x00	RW	Bit[7:0]: AWB bias value for manual mode
0xE3~ 0xFE	RSVD	–	–	Reserved
0xFF	MIPI_BANK	0x00	RW	Bit[7:1]: MIPI register bank selection Bit[0]: MIPI register bank selection 0: Not selected 1: Selected (see table 7-2 for details)

table 7-2 MIPI bank registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x80	MIPI_CTRL00	0x04	RW	Bit[7]: mipi_hs_only 0: MIPI can support CD and ESCAPE mode 1: MIPI is always in high speed mode Bit[6]: ck_mark1_en 0: Reserved 1: Enable clock lane mark1 when resume Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Reserved Bit[2]: idle_sts 0: MIPI bus will be LP00 when there is no packet to transmit 1: MIPI bus will be LP11 when there is no packet to transmit Bit[1]: first_bit Change clk_lane first bit 0: Output 0x05 1: Output 0xAA Bit[0]: clk_lane_dis 0: Reserved 1: Manual set clock lane to low power mode

table 7-2 MIPI bank registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x81	MIPI_CTRL01	0x0F	RW	Bit[7]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[6]: spkt_dt_sel 0: Reserved 1: Use dt_spkt as short packet data Bit[5]: spkt_wc_sel 0: Use frame counter or line counter 1: Select spkt_wc_reg_o Bit[4]: ph_bit_order PH bit order for ECC 0: {DI[7:0], WC[7:0], WC[15:8]} 1: {DI[0:7], WC[0:7], WC[8:15]} Bit[3]: ph_byte_order PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: ph_byte_order2 PH byte order2 for ECC 0: Reserved 1: {WC,DI}, 0: {DI,WC} Bit[1]: mark1_en1 0: Reserved 1: After each rst release, lane1 should send mark1 for wkup_dly_o when mipi_sys_susp = 1 Bit[0]: Reserved

table 7-2 MIPI bank registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x82	MIPI_CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]

table 7-2 MIPI bank registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x83	MIPI_CTRL03	0x50	RW	Bit[7:6]: lp_glitch_nu 0: Use 2d of lp_in 1: Mask one SCLK cycle glitch of lp_in Bit[5:4]: cd_glitch_nu 0: Use 2d of lp_cd_in 1: Mask one SCLK cycle glitch of lp_cd_in Bit[3]: cd1_int_en 0: Disable CD plus of data lane1 1: Enable CD plus of data lane1 Bit[2]: Reserved Bit[1]: lp_cd1_en 0: Disable CD of data_lane1 from PHY 1: Enable CD of data_lane1 from PHY Bit[0]: Reserved

table 7-2 MIPI bank registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x84	MIPI_CTRL04	0x8D	RW	Bit[7]: wait_pkt_end 0: Reserved 1: Wait HS packet end when send UL command Bit[6]: tx_lsb_first 0: lp_tx and lp_rx high bit first 1: Low power tx low bit first Bit[5]: dir_recover_sel 0: Auto change to output only when TurnAround command 1: Auto change to output when LP11 and GPIO is output Bit[4]: mipi_reg_en 0: Disable MIPI_REG_P access registers, LP data will write to VFIFO 1: Enable MIPI_REG_P to access registers Bit[3]: inc_en 0: Reserved 1: mipi_reg_addr will auto increment by 1 Bit[2]: Reserved Bit[1]: wr_first_byte 0: Reserved 1: lp_rx will write first byte (command byte) to RAM Bit[0]: rd_ta_en 0: Reserved 1: Send turnaround command after sending register read data

table 7-2 MIPI bank registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x85	MIPI_CTRL05	0x10	RW	Bit[7]: lane_disable1 0: Reserved 1: Disable MIPI data lane1, lane1 will be LP00 Bit[6]: Reserved Bit[5]: lpx_p_sel 0: Auto calculate t_lpx_o in pclk2x domain, unit clk2x 1: Use lp_p_min[7:0] Bit[4]: lp_rx_intr_sel 0: Send lp_rx_intr_o at the first byte 1: Send lp_rx_intr_o at the end of receiving Bit[3]: cd_tst_sel 0: Reserved 1: Select PHY test pins Bit[2]: mipi_reg_mask 0: Reserved 1: Disable MIPI access SRB Bit[1:0]: Reserved
0x86	MIPI_CTRL06	0x08	RW	Bit[7:3]: Reserved Bit[2]: rst_rtn_en 0: Reserved 1: After reset, change to input to allow host RW registers Bit[1]: frame_end_en 0: Reserved 1: After frame end packet, change to input to allow host RW registers Bit[0]: line_end_en 0: Reserved 1: After line end packet, change to input to allow host RW registers
0x87	MIPI_CTRL07	0x53	RW	Bit[7:0]: Timeout register Timeout cycles for return ACK of register RW
0x88	MIPI_CTRL08	0x00	RW	Bit[7:0]: High byte of return ACK address
0x89	MIPI_CTRL09	0x00	RW	Bit[7:0]: Low byte of return ACK address
0x8A	MIPI_FCNT_MAX	0xFF	RW	High Byte of Max Frame Counter of Frame Sync Short Packet
0x8B	MIPI_FCNT_MAX	0xFF	RW	Low Byte of Max Frame Counter of Frame Sync Short Packet

table 7-2 MIPI bank registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x8C	MIPI_SPKT_WC_ REG	0x00	RW	High Byte of Manual Short Packet Word Counter
0x8D	MIPI_SPKT_WC_ REG	0x00	RW	Low Byte of Manual Short Packet Word Counter
0x8E	MIPI_CTRL14	0x2A	RW	Bit[7:6]: VC Virtual channel of MIPI Bit[5:0]: dt_man Manual data byte
0x8F	MIPI_DT_SPKT	0x00	RW	Manual Data Byte for Short Packet
0x90	UI_HS_ZERO _MIN MIPI_HS_ZERO_ MIN	0x14	RW	Bit[7:2]: Minimum UI value of hs_zero, unit UI Bit[1:0]: High byte of minimum value of hs_zero, unit ns
0x91	MIPI_HS_ZERO_ MIN	0x96	RW	Low byte of minimum value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x92	UI_HS_TRAIL _MIN MIPI_HS_TRAIL_ MIN	0x10	RW	Bit[7:2]: Minimum UI value of hs_trail, unit UI Bit[1:0]: High byte of minimum value of hs_trail, unit ns
0x93	MIPI_HS_TRAIL_ MIN	0x3C	RW	Bit[7:0]: Low byte of minimum value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x94	UI_CLK_ZERO _MIN MIPI_CLK_ ZERO_MIN	0x01	RW	Bit[7:2]: Minimum UI value of clk_zero, unit UI Bit[1:0]: High byte of minimum value of clk_zero
0x95	MIPI_CLK_ ZERO_MIN	0x86	RW	Low byte of minimum value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x96	UI_CLK_ PREPARE_MIN MIPI_CLK_ PREPARE_MIN	00	RW	Bit[7:2]: Minimum UI value of clk_prepare, unit UI Bit[1:0]: high byte of minimum value of clk_prepare, unit ns
0x97	MIPI_CLK_ PREPARE_MIN	0x3C	RW	Bit[7:0]: Low byte of minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o

table 7-2 MIPI bank registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x98	UI_CLK_POST_MIN MIPI_CLK_POST_MIN	0xD0	RW	Bit[7:2]: Minimum UI value of clk_post, unit UI Bit[1:0]: High byte of minimum value of clk_post, unit ns
0x99	MIPI_CLK_POST_MIN	0x56	RW	Low byte of minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x9A	UI_CLK_TRAIL_MIN MIPI_CLK_TRAIL_MIN	0x00	RW	Bit[7:2]: Minimum UI value of clk_trail, unit UI Bit[1:0]: High byte of minimum value of clk_trail, unit ns
0x9B	MIPI_CLK_TRAIL_MIN	0x3C	RW	Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x9C	UI_LPX_P_MIN MIPI_LPX_P_MIN	0x00	RW	Bit[7:2]: Minimum UI value of lpx_p(pclk2x domain), unit UI Bit[1:0]: High byte of minimum value of lpx_p, unit ns
0x9D	MIPI_LPX_P_MIN	0x32	RW	Low byte of minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x9E	UI_HS_PREPARE_MIN MIPI_HS_PREPARE_MIN	0x10	RW	Bit[7:2]: Minimum UI value of hs_prepare, unit UI Bit[1:0]: High byte of minimum value of hs_prepare, unit ns
0x9F	MIPI_HS_PREPARE_MIN	0x32	RW	Low byte of minimum value of hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0xA0	UI_HS_EXIT_MIN MIPI_HS_EXIT_MIN	0x00	RW	Bit[7:2]: Minimum UI value of hs_exit, unit UI Bit[1:0]: High byte of minimum value of hs_exit, unit ns
0xA1	MIPI_HS_EXIT_MIN	0x64	RW	Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0xA2	MIPI_REG_MIN	0x00	RW	Address range of MIPI RW registers is mipi_reg_min_o to mipi_reg_max_o
0xA3	MIPI_REG_MIN	0x00	RW	mipi_reg_min
0xA4	MIPI_REG_MAX	0xFF	RW	mipi_reg_max
0xA5	MIPI_REG_MAX	0xFF	RW	mipi_reg_max

table 7-2 MIPI bank registers (sheet 9 of 10)

address	register name	default value	R/W	description
0xA6	MIPI_WKUP_DLY	0x42	RW	Bit[7:6]: start_mode 00: Delay one line mode 01: Old mode, delay about 100 Tp 10: VHREF manual mode 11: Reserved Bit[5:0]: Wakeup delay for MIPI (MARK1 state)/2^12
0xA7	ADDR_BYTE MIPI_DIR_DLY	0x48	RW	Bit[7:6]: addr_byte Bit[5:0]: Change LP direction delay/2 after LP11
0xA8	MIPI_LP_GPIO	0x33	RW	Bit[7]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[6]: lp_dir_man1 0: Input 1: Output Bit[5]: lp_p1_o Bit[4]: lp_n1_o Bit[3:0]: Reserved
0xA9	MIPI_CTRL29	0x4F	RW	Bit[7:4]: t_lpx Unit: sclk cycle Bit[3:0]: t_clk_pre Unit: pclk2x cycle
0xAA	MIPI_T_TA_GO	0x10	RW	Unit: SCLK cycle
0xAB	MIPI_T_TA_SURE	0x06	RW	Unit: SCLK cycle
0xAC	MIPI_T_TA_GET	0x14	RW	Unit: SCLK cycle
0xAD	MIPI_CTRL2D START_OFFSET_ HIGH	0x00	RW	Bit[7:6]: wdata_byte Bit[5]: snr_pclk_div Bit[4:0]: High byte of start_offset
0xAE	START_OFFSET_ LOW	0x00	RW	Bit[7:0]: Low byte of start_offset
0xAF	CLIP_HIGH	0xF0	RW	Bit[7:4]: High byte of clip_max Bit[3:0]: High byte of clip_min
0xB0	CLIP_MAX_LOW	0xFF	RW	Bit[7:0]: Low byte of clip_max
0xB1	CLIP_MIN_LOW	0x00	RW	Bit[7:0]: High byte of clip_min
0xB2	TIMEOUT_NUM	0x00	RW	Bit[7:0]: Timeout number
0xB3	RSVD	–	–	Reserved

table 7-2 MIPI bank registers (sheet 10 of 10)

address	register name	default value	R/W	description
0xB4	MIPI_COM0	0x40	RW	Bit[7]: mipi_en 0: Disable 1: Enable Bit[6]: mipi_bit8 0: 10-bit mode 1: 8-bit mode Bit[5]: mipi_tst Bit[4:0]: mipi_pclk_div Divide PCLK in MIPI by 00: /1 01: /2 10: /3 11: /4
0xB5	R_MIPI0	0x70	RW	Bit[7:6]: pgm_lptx Driving strength of low speed transmitter Bit[5]: Power down MIPI Bit[4]: Power down MIPI low power transmitter Bit[3:2]: ICTL Bias current adjustment Bit[1:0]: LPH LP1_VOH value adjust
0xB6	R_MIPI1	0x00	RW	Bit[7:3]: Reserved Bit[2]: Halve bias current Bit[1:0]: Adjust high speed common mode voltage

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		260°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to 50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
I_{DD-A}	active (operating) current		17	22	mA
I_{DD-IO}			17	22	mA
$I_{DDS-SCCB}$	standby current		0.28	1.0	mA
$I_{DDS-PWDN}$			23	30	µA
digital inputs (typical conditions: AVDD = 2.8V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[a]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}[a]	SIOC and SIOD	1.26	1.8	2.3	V

a. based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	54	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

figure 8-1 SCCB interface timing

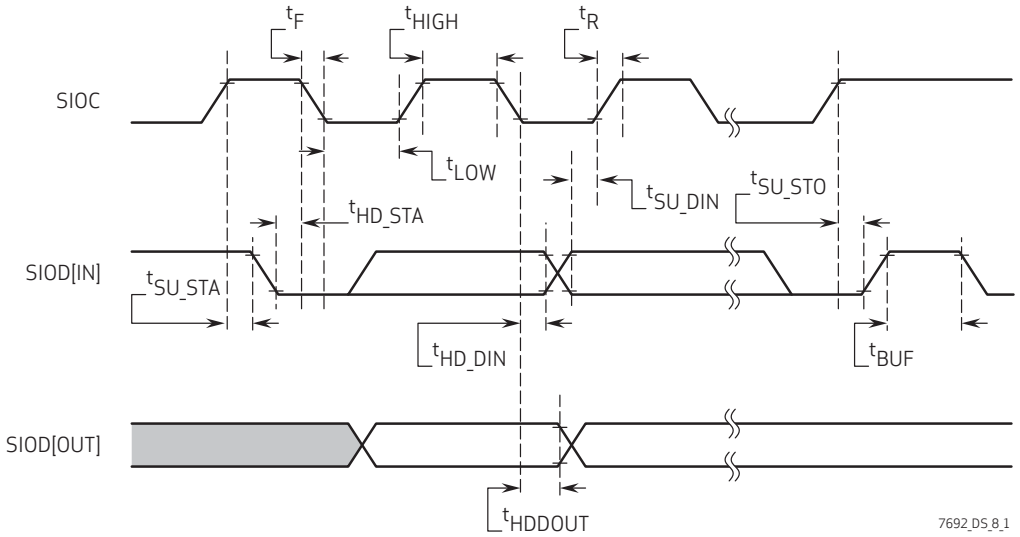


table 8-6 SCCB timing interface specifications[a]

symbol	typical SIOC clock frequency	SCCB standard mode (100 KHz)[b]		SCCB standard mode (400 KHz)[c]		unit
		min	max	min	max	
t_{HIGH}	SIOC clock high time	1156		259		ns
t_{LOW}	SIOC clock low time	2340		682		ns
t_{BUF}	bus free time before new start cycle	3960		874		ns
t_{HD_STA}	start of transmission hold time	341		83		ns
t_{SU_STA}	start of transmission setup time	0		0		ns
t_{SU_STO}	stop of transmission setup time	99.2		106		ns
t_{SUDIN}	input data setup time	476		209		ns
t_{HDDIN}	input data hold time	0		0		ns
t_{HDDOUT}	output data transmission hold time	1264		504		ns
t_R	SIOC clock rising time	1.76		1.5		ns
t_F	SIOC clock falling time	1.7		1.5		ns

a. see **Section 2.6,** SCCB interface for details on SCCB speed support

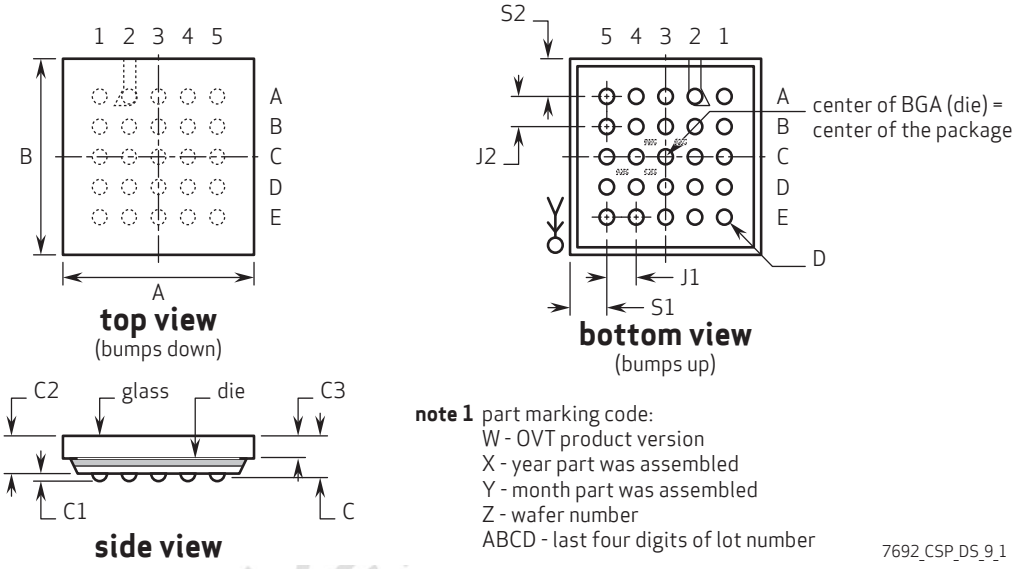
b. test results measured at XVCLK = 6MHz, DOVDD = 2.8V

c. test results measured at XVCLK = 27MHz, DOVDD=2.8V

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note 1 part marking code:
W - OVT product version
X - year part was assembled
Y - month part was assembled
Z - wafer number
ABCD - last four digits of lot number

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table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	2740	2765	2790	µm
package body dimension y	B	3104	3129	3154	µm
package height	C	690	750	810	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	620	665	µm
thickness of glass surface to wafer	C3	425	445	465	µm
ball diameter	D	220	250	280	µm
total pin count	N		25 (2 NC)		
pin count x-axis	N1		5		
pin count y-axis	N2		5		
pins pitch x-axis	J1		500		µm
pins pitch y-axis	J2		540		µm
edge-to-pin center distance analog x	S1	353	383	413	µm
edge-to-pin center distance analog y	S2	455	485	515	µm

9.2 IR reflow specifications

note
The OV7692 uses a lead free package.

figure 9-2 IR reflow ramp rate requirements

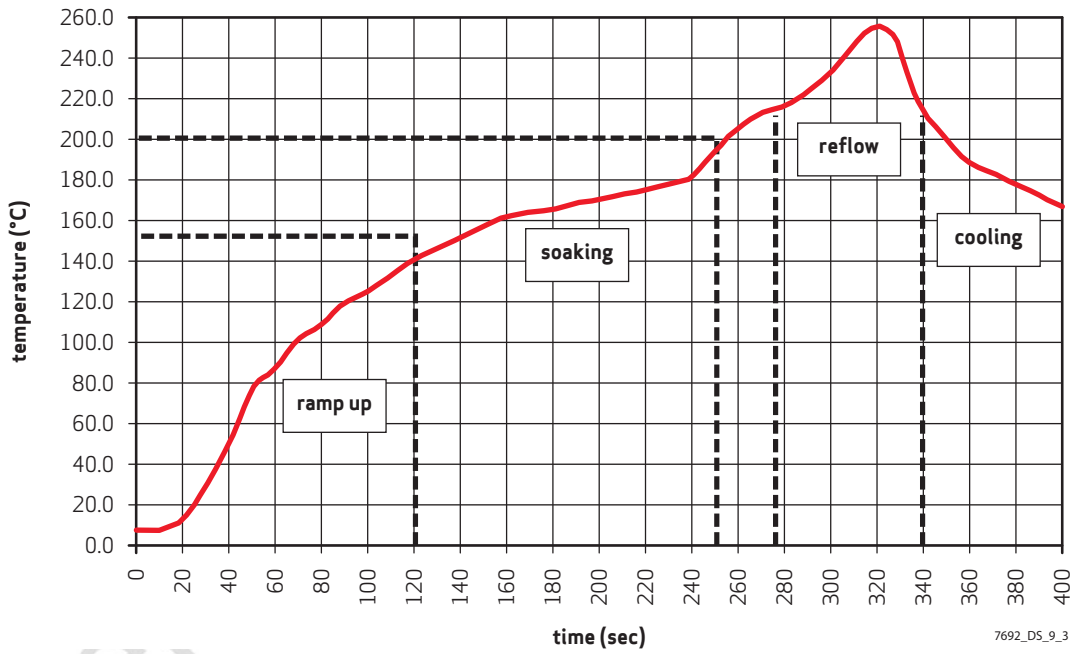


table 9-2 reflow conditions[a]

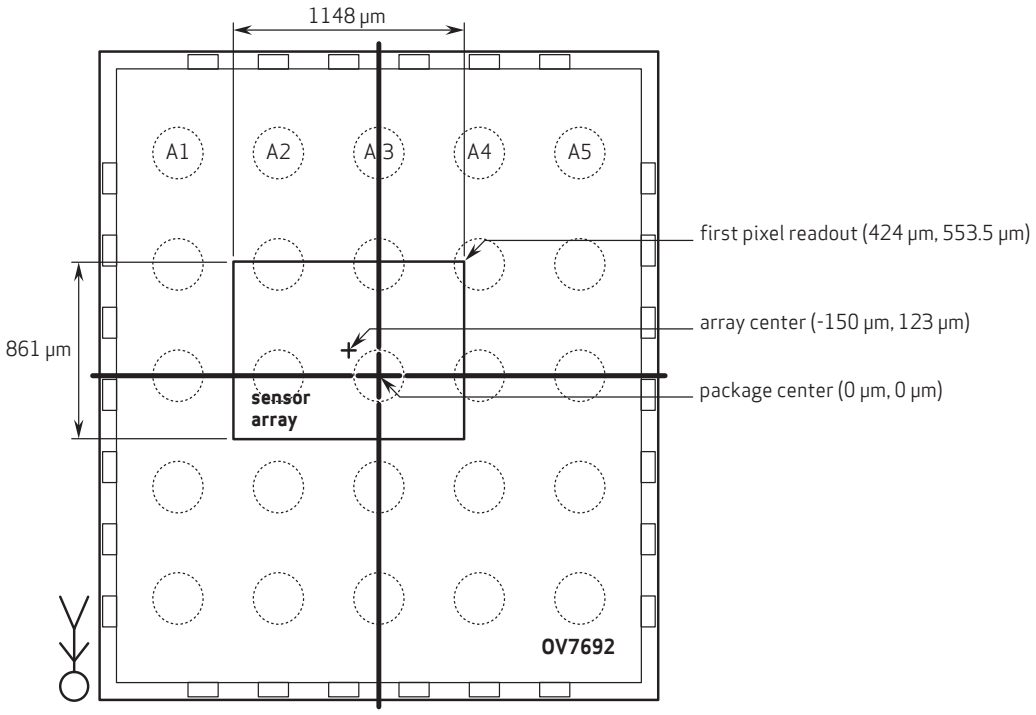
zone	description	exposure
ramp up	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
reflow	temperature higher than 217°C	30 ~ 120 seconds
peak	maximum temperature in SMT	260°C
cooling	cooling from 217°C to room temperature	temperature slope ≤ 6°C per second

a. maximum number of reflow cycles = 3

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 to A5 oriented down on the PCB.

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10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

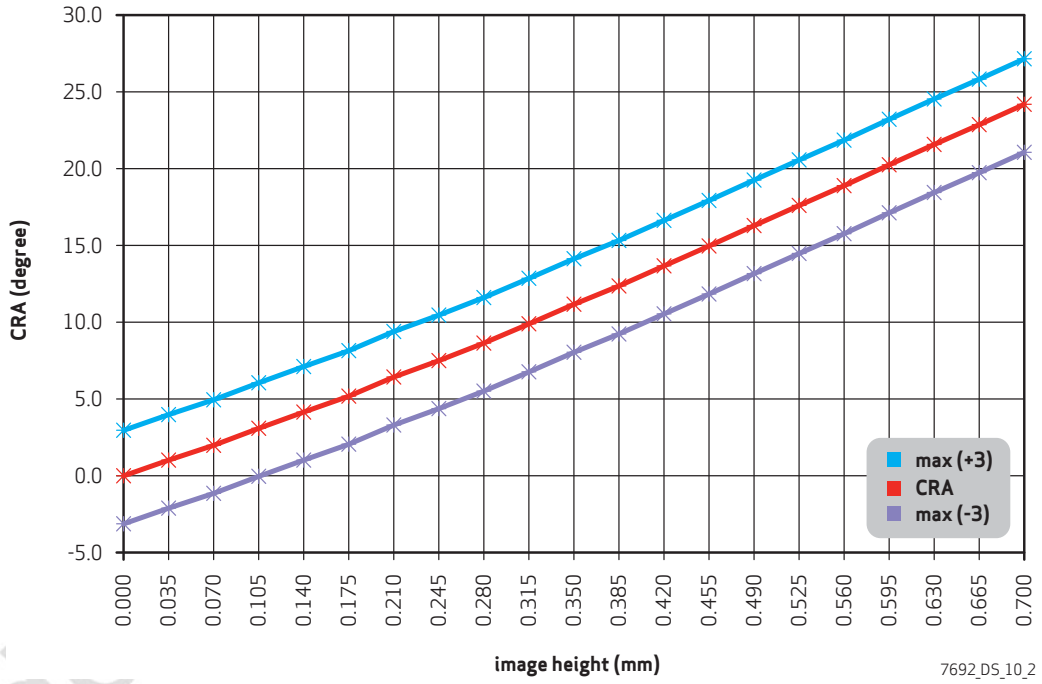

table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.035	1.0
0.1	0.07	2.0
0.15	0.105	3.1
0.2	0.140	4.2
0.25	0.175	5.2
0.3	0.210	6.4
0.35	0.245	7.5
0.4	0.280	8.7
0.45	0.315	9.9

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	0.350	11.2
0.55	0.385	12.4
0.6	0.420	13.7
0.65	0.455	15.0
0.7	0.490	16.3
0.75	0.525	17.6
0.8	0.560	18.9
0.85	0.595	20.3
0.9	0.630	21.6
0.95	0.665	22.9
1	0.700	24.2

revision history

version 1.0 12.02.2008

- initial release

version 1.1 02.20.2009

- updated section 2.6 SCCB interface table 2-3

version 1.11 03.03.2009

- updated information on the features page
- updated table 8-2 of chapter 8
- added table 8-5 and figure 8-1 of chapter 8

version 2.0 08.11.2009

- updated all references for Product Specification release

version 2.01 12.10.2010

- in the key specifications section, added "junction temperature" to temperature range and dark current
- in the key specifications section, updated S/N ratio to max S/N ratio and updated dynamic range: 66 dB to 66 dB @ 8x gain
- in the key specifications section, removed fixed pattern noise and well capacity
- in chapter 8, added "junction temperature" to table 8-2 functional temperature

the clear advantage™

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