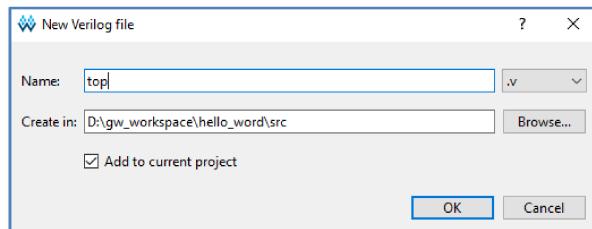
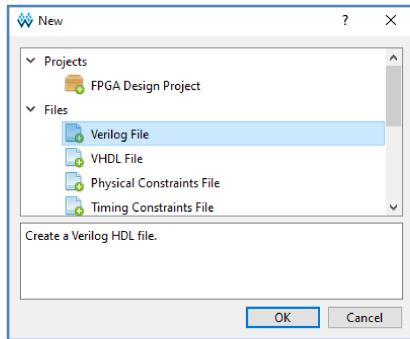




https://gowinsemi.com/en/support/download_eda/

The screenshot shows the GOWIN FPGA Designer interface with the following steps:

- File Menu:** Shows options like Open Example Project..., New... (selected), and Open...
 - New Dialog:** A modal window titled "New" for creating an "FPGA Design Project". It lists file types: Verilog File, VHDL File, Physical Constraints File, and Timing Constraints File. A note says: "Create a FPGA design project. You will be able to add or create RTL sources, run synthesis, place & route, and program your device." Buttons: OK, Cancel.
- Project Wizard - Project Name:** Step 1 of 3. Set Project Name to "hello_word", Create in "D:\gw_workspace", and checked "Use as default project location". Buttons: Next >, Cancel.
- Project Wizard - Select Device:** Step 2 of 3. Set Series to "GW1NR", Device to "Any", Package to "Any", Speed to "Any". Filtered results show "GW1NR" selected. Buttons: < Back, Next >, Cancel.
- Project Wizard - Summary:** Step 3 of 3. Summary of project settings:
 - Project:** Name: hello_word
Directory: D:\gw_workspace
Source Directory: D:\gw_workspace\hello_word\src
Implementation Directory: D:\gw_workspace\hello_word\impl
 - Device:** Part Number: GW1NR-LV9QN88PC6/IS
Series: GW1NR
Device: GW1NR-9C
Package: QFP88P
Speed: C6/ISButtons: < Back, Finish, Cancel.



```

module top (
    input wire button1,
    input wire button2,
    output wire [1:0] leds
);
    assign leds[0] = button1;
    assign leds[1] = button2;
endmodule

```

top.v

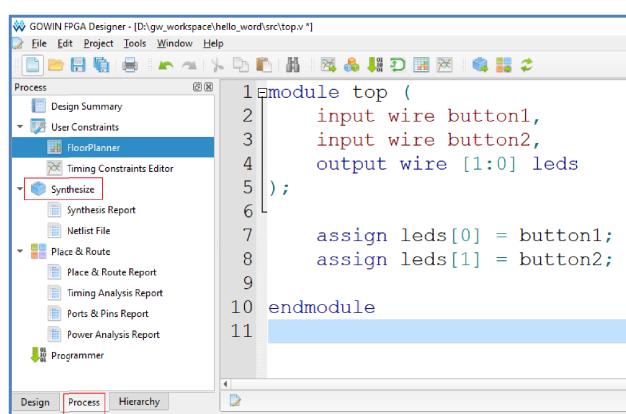
```

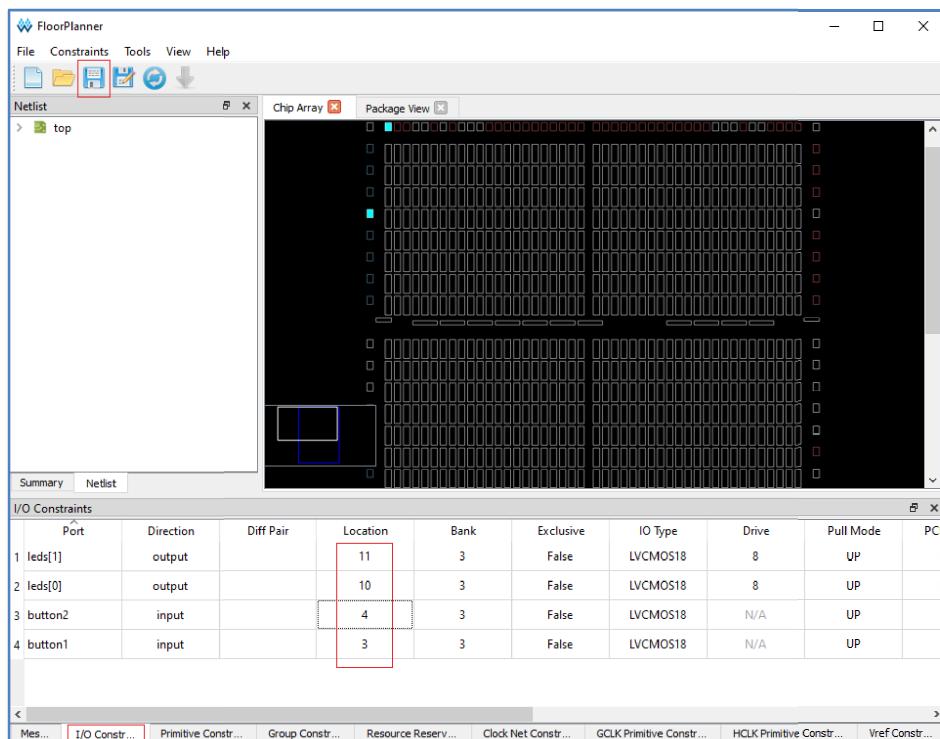
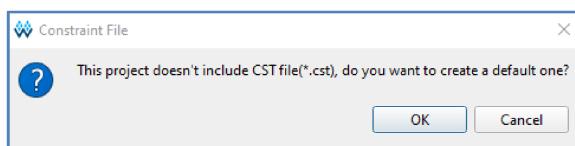
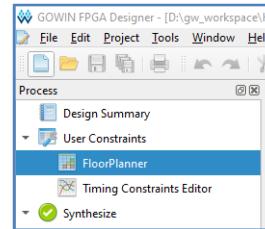
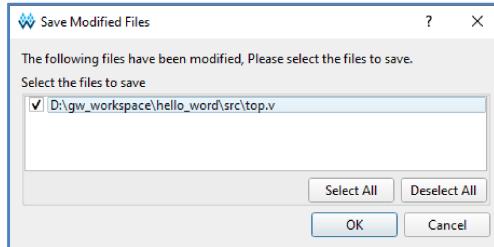
module top (
    input wire button1,
    input wire button2,
    output wire [1:0] leds
);

    assign leds[0] = button1;
    assign leds[1] = button2;

endmodule

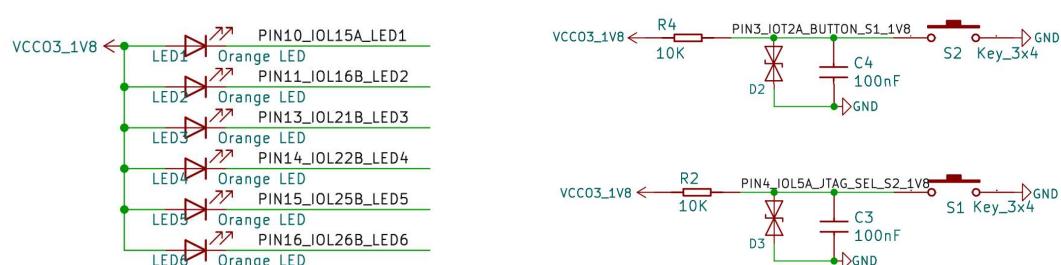
```





Hardware Schematic

<https://wiki.sipeed.com/hardware/en/tang/Tang-Nano-9K/Nano-9K.html>



```

1 IO_LOC "leds[1]" 11;
2 IO_PORT "leds[1]" IO_TYPE=LVC MOS18 PULL_MODE=UP DRIVE=8 BANK_VCCIO=1.8;
3 IO_LOC "leds[0]" 10;
4 IO_PORT "leds[0]" IO_TYPE=LVC MOS18 PULL_MODE=UP DRIVE=8 BANK_VCCIO=1.8;
5 IO_LOC "button2" 4;
6 IO_PORT "button2" IO_TYPE=LVC MOS18 PULL_MODE=UP BANK_VCCIO 1.8;
7 IO_LOC "button1" 3;
8 IO_PORT "button1" IO_TYPE=LVC MOS18 PULL_MODE=UP BANK_VCCIO=1.8;
9

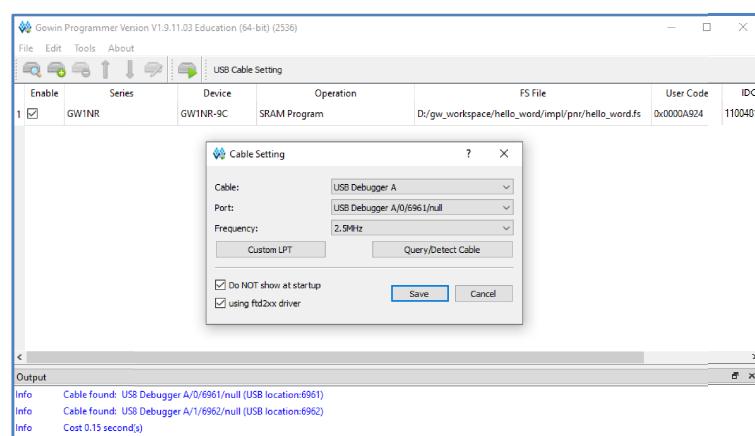
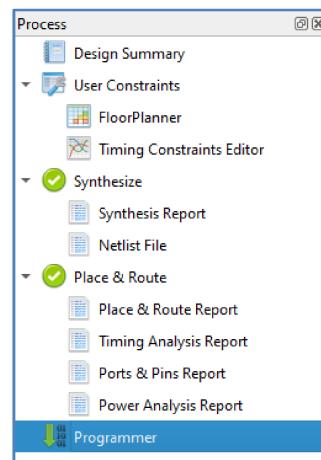
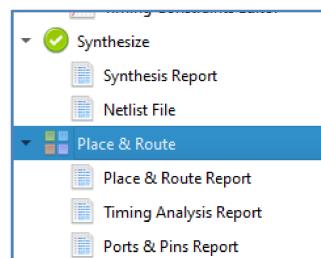
```

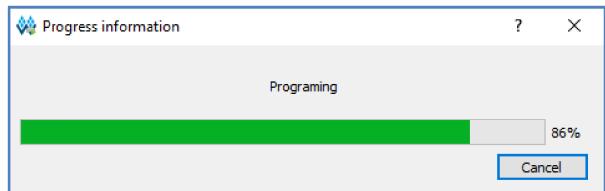
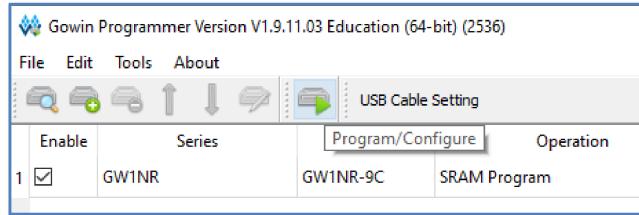
hello_word.cst

```

IO_LOC "leds[1]" 11;
IO_PORT "leds[1]" IO_TYPE=LVC MOS18 PULL_MODE=UP DRIVE=8 BANK_VCCIO=1.8;
IO_LOC "leds[0]" 10;
IO_PORT "leds[0]" IO_TYPE=LVC MOS18 PULL_MODE=UP DRIVE=8 BANK_VCCIO=1.8;
IO_LOC "button2" 4;
IO_PORT "button2" IO_TYPE=LVC MOS18 PULL_MODE=UP BANK_VCCIO=1.8;
IO_LOC "button1" 3;
IO_PORT "button1" IO_TYPE=LVC MOS18 PULL_MODE=UP BANK_VCCIO=1.8;

```





Tang Nano 9K

