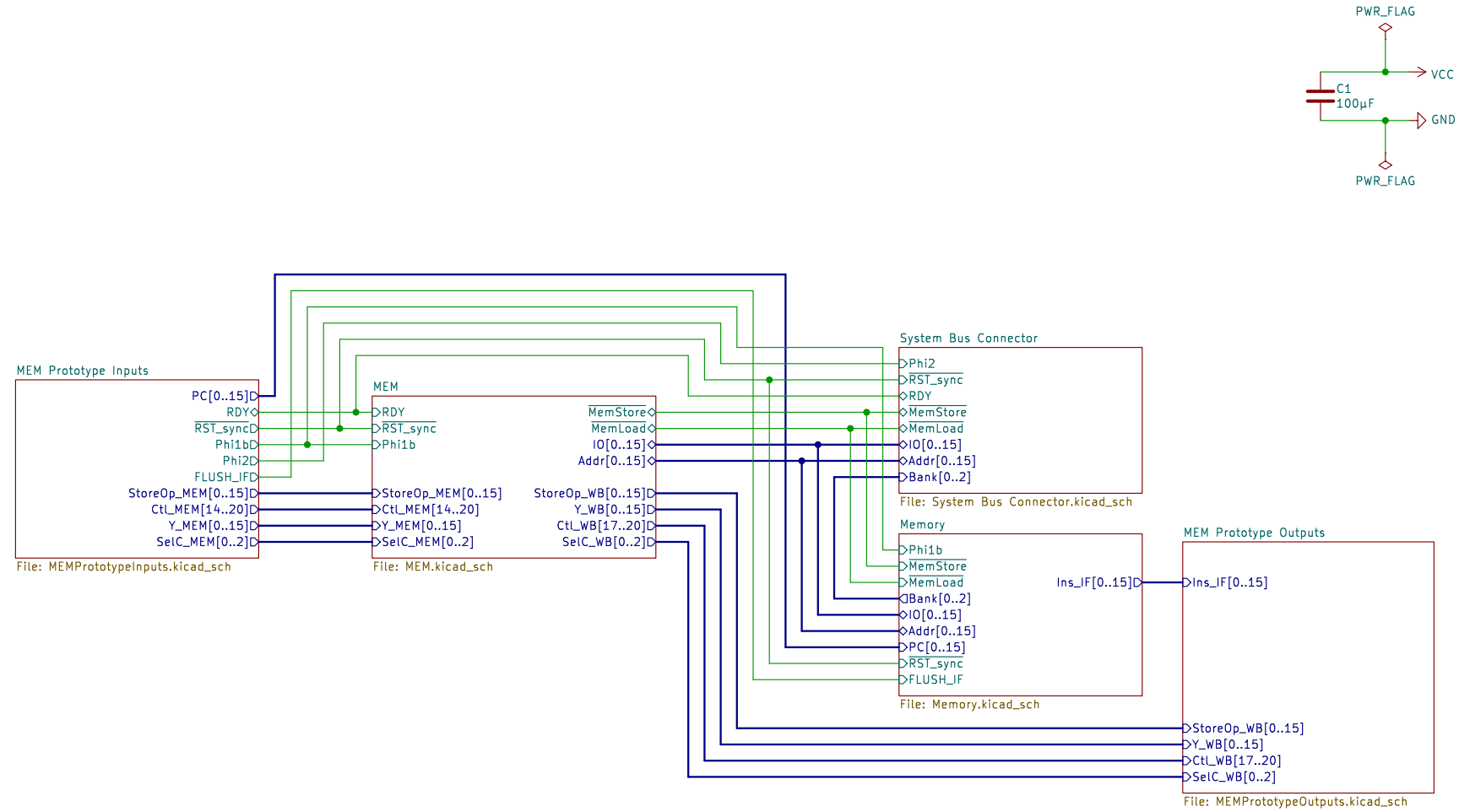
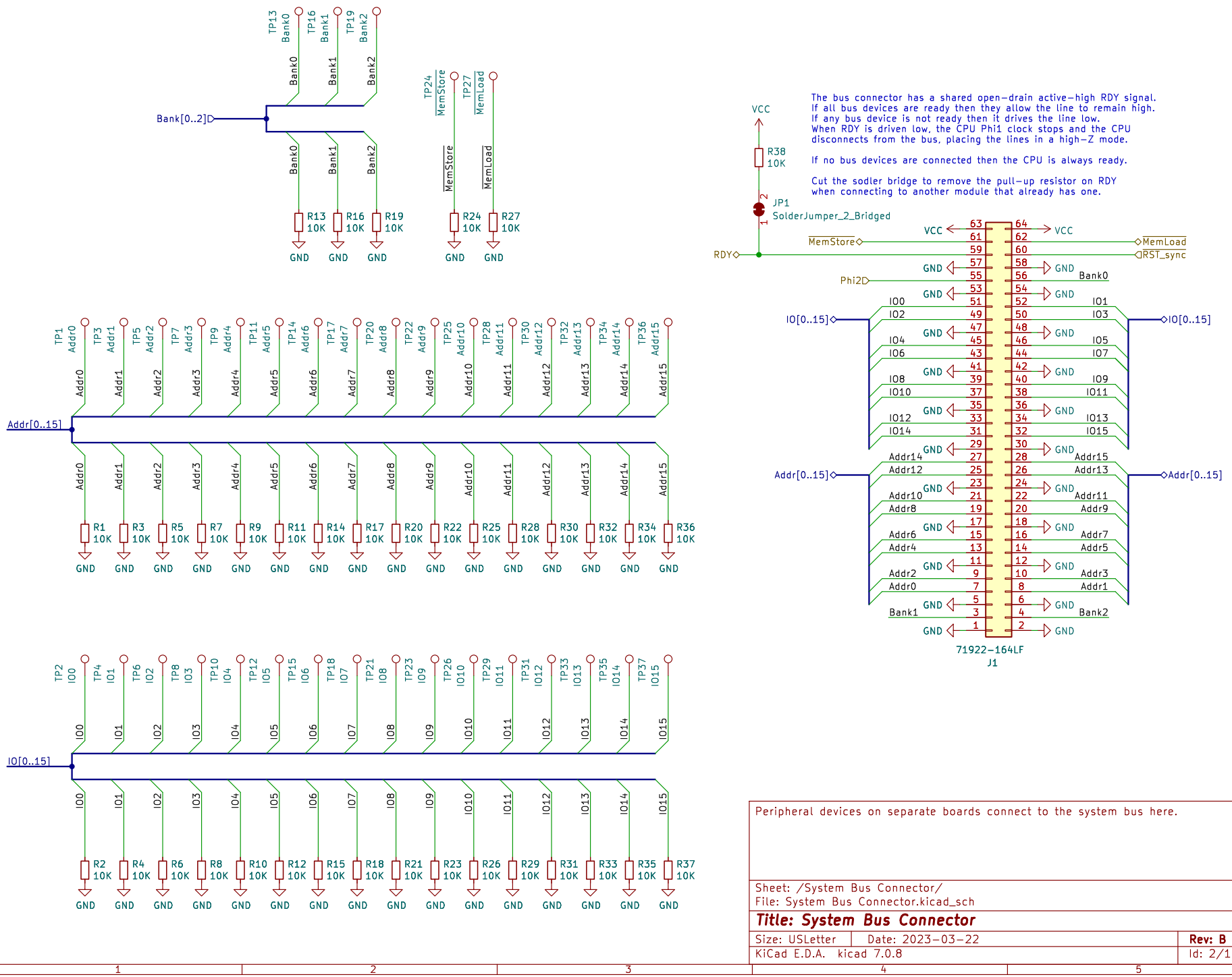


MEM Pipeline Stage and Computer Memory

Sheet: /
File: MEMModule.kicad_sch

Title: Turtle16: MEM, RAM, ROM

Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 1/14

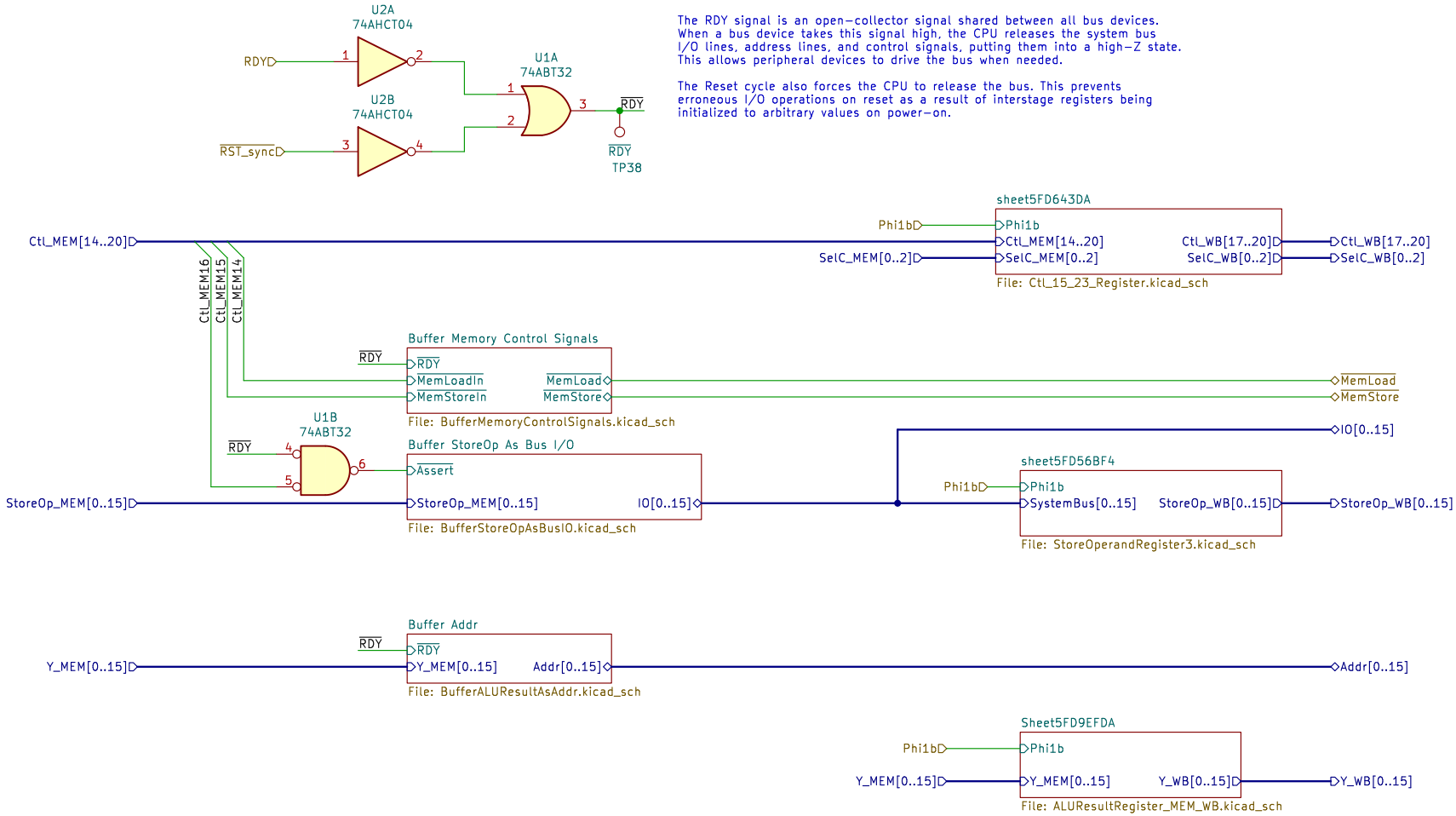


Peripheral devices on separate boards connect to the system bus here.

Sheet: /System Bus Connector/
File: System Bus Connector.kicad_sch

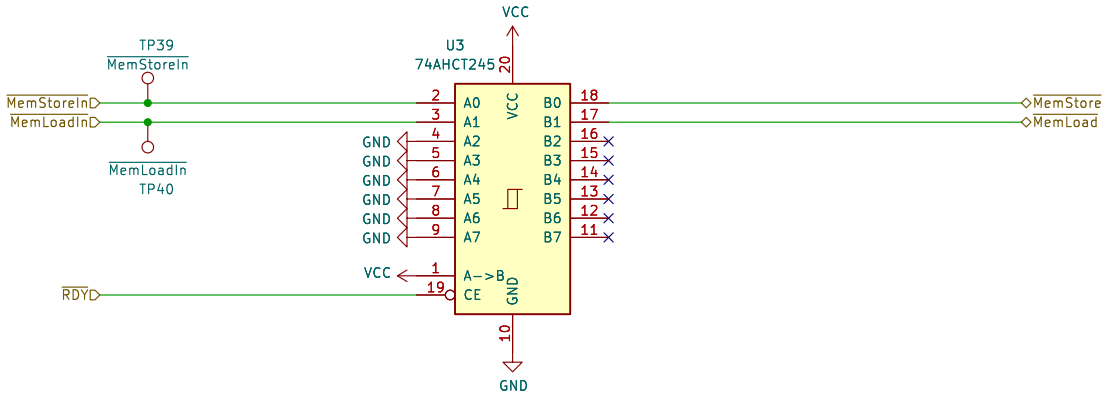
Title: System Bus Connector

Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 2/14



The MEM stage interfaces with memory and memory-mapped peripherals.
These devices connect to the main board via a connector described in another sheet.
Devices on the bus may take the open-collector ~RDY~ signal high to force the CPU to place bus lines into tristate and halt the Phi1 clock.

Sheet: /MEM/ File: MEM.kicad_sch		
Title: MEM		
Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 3/14

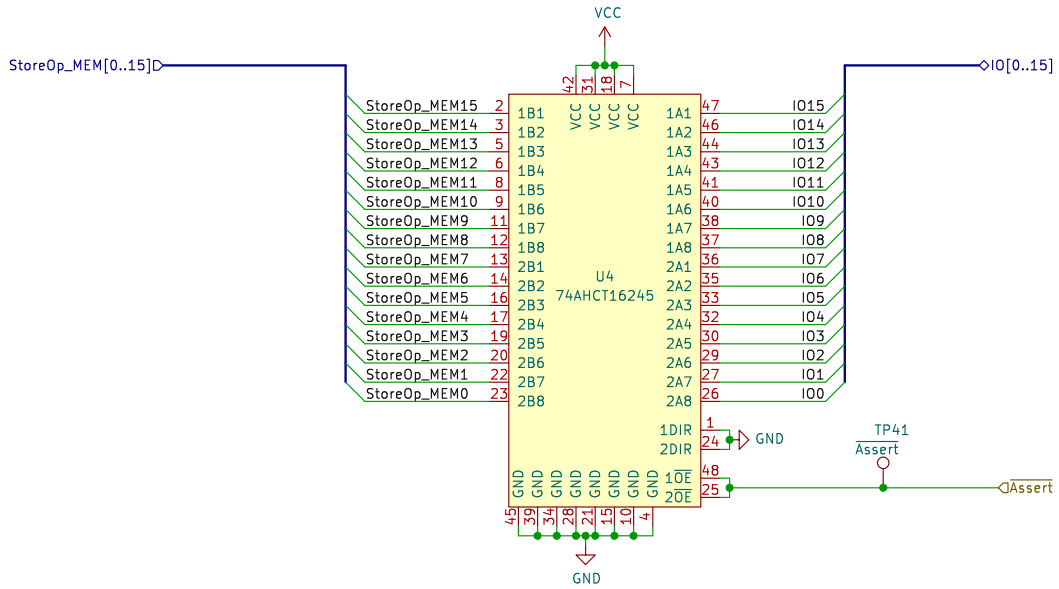


Sheet: /MEM/Buffer Memory Control Signals/
File: BufferMemoryControlSignals.kicad_sch

Title:

Size: USLetter | Date: 2023-03-22 | **Rev: B**

KiCad E.D.A. kicad 7.0.8 | Id: 4/14

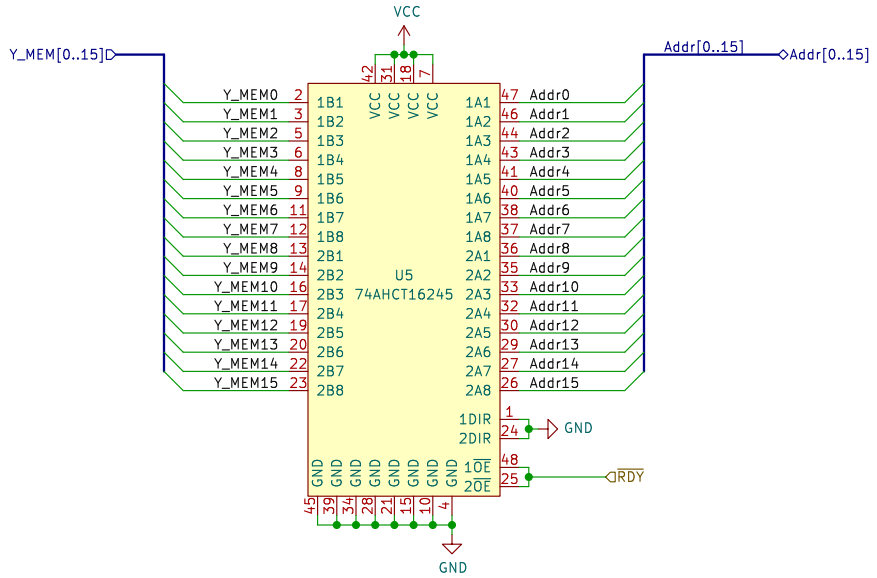


The store operand can be disconnected from the system memory bus via tristate outputs.
This allows peripheral devices to assert their own value to the bus during a Load.

Sheet: /MEM/Buffer StoreOp As Bus I/O/
File: BufferStoreOpAsBusIO.kicad_sch

Title: MEM: Buffer StoreOp

Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 5/14

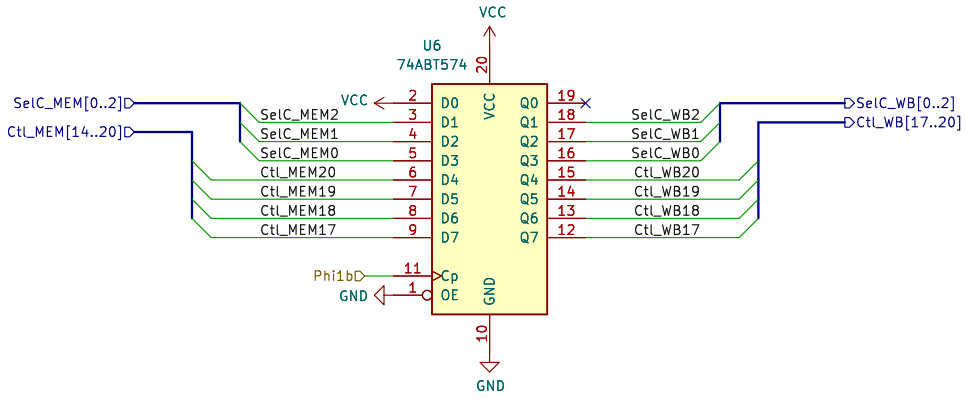


Buffer the effective address before it leaves the main board.

Sheet: /MEM/Buffer Addr/
File: BufferALUResultAsAddr.kicad_sch

Title: MEM: Buffer ALUResult

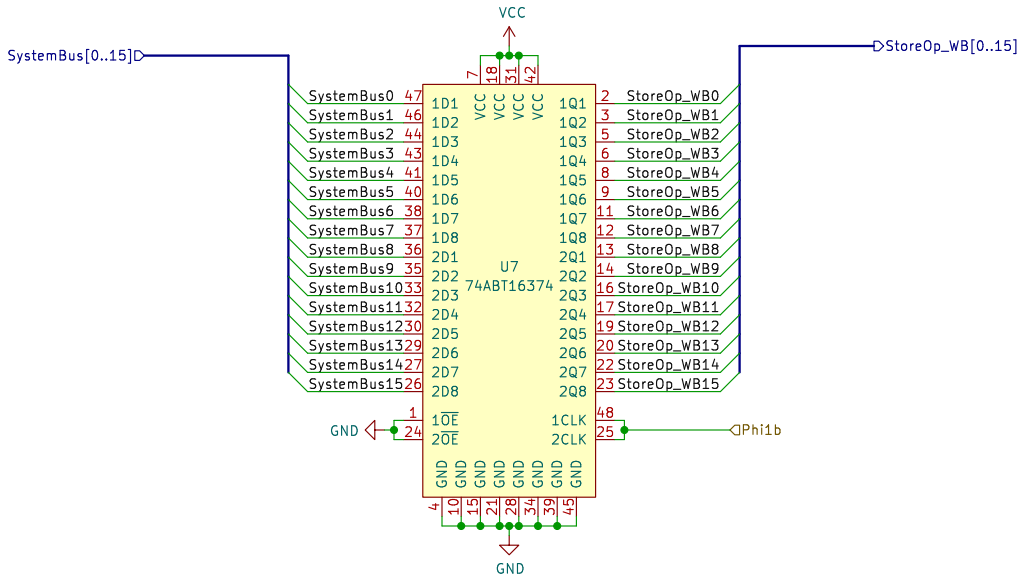
Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 6/14



Sheet: /MEM/sheet5FD643DA/
File: Ctl_15_23_Register.kicad_sch

Title: MEM/WB: Control Word Register

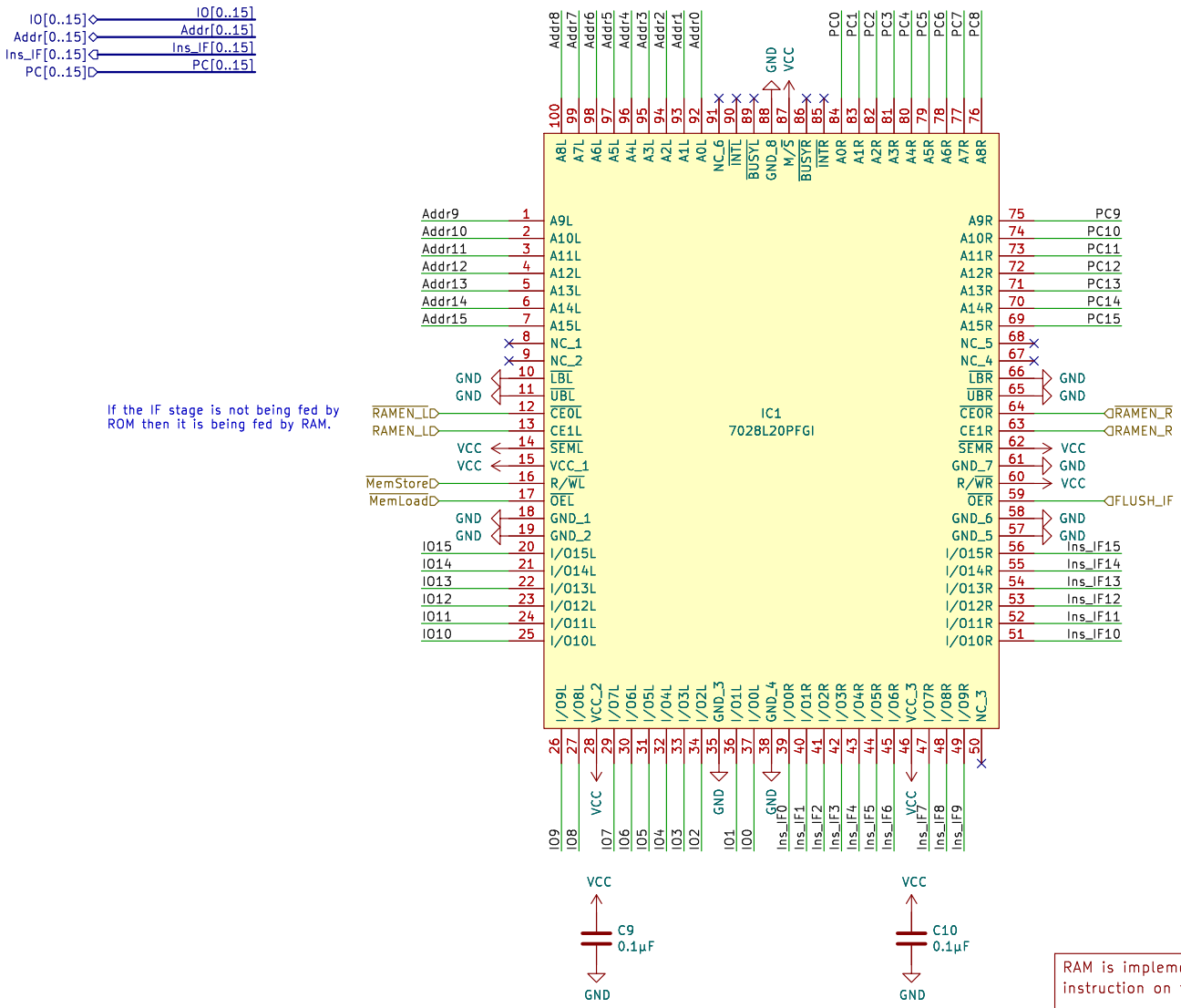
Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 7/14



Sheet: /MEM/sheet5FD56BF4/
File: StoreOperandRegister3.kicad_sch

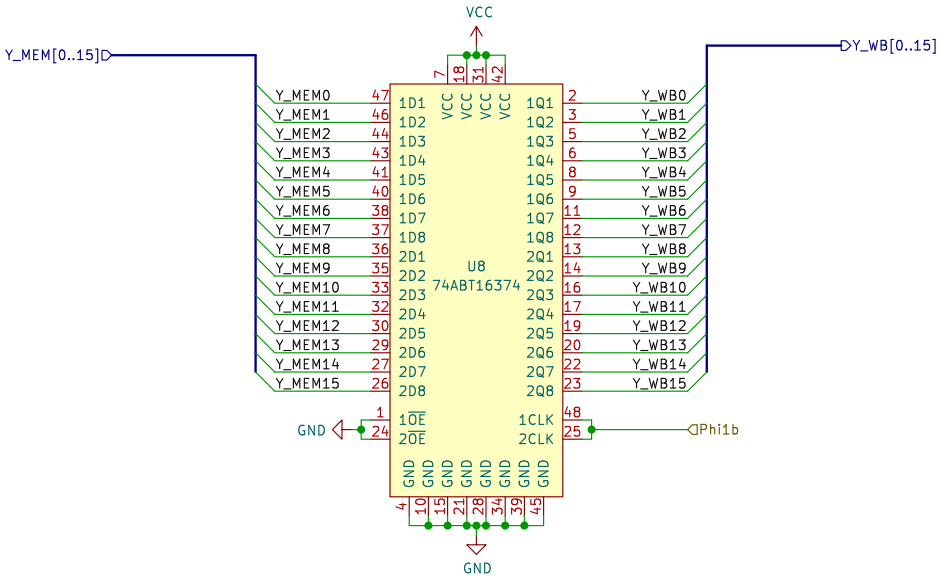
Title: MEM/WB: Store Operand Register

Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 8/14



RAM is implemented with a 64K x 16 dual port SRAM so that the IF stage can fetch an instruction on the second read port.

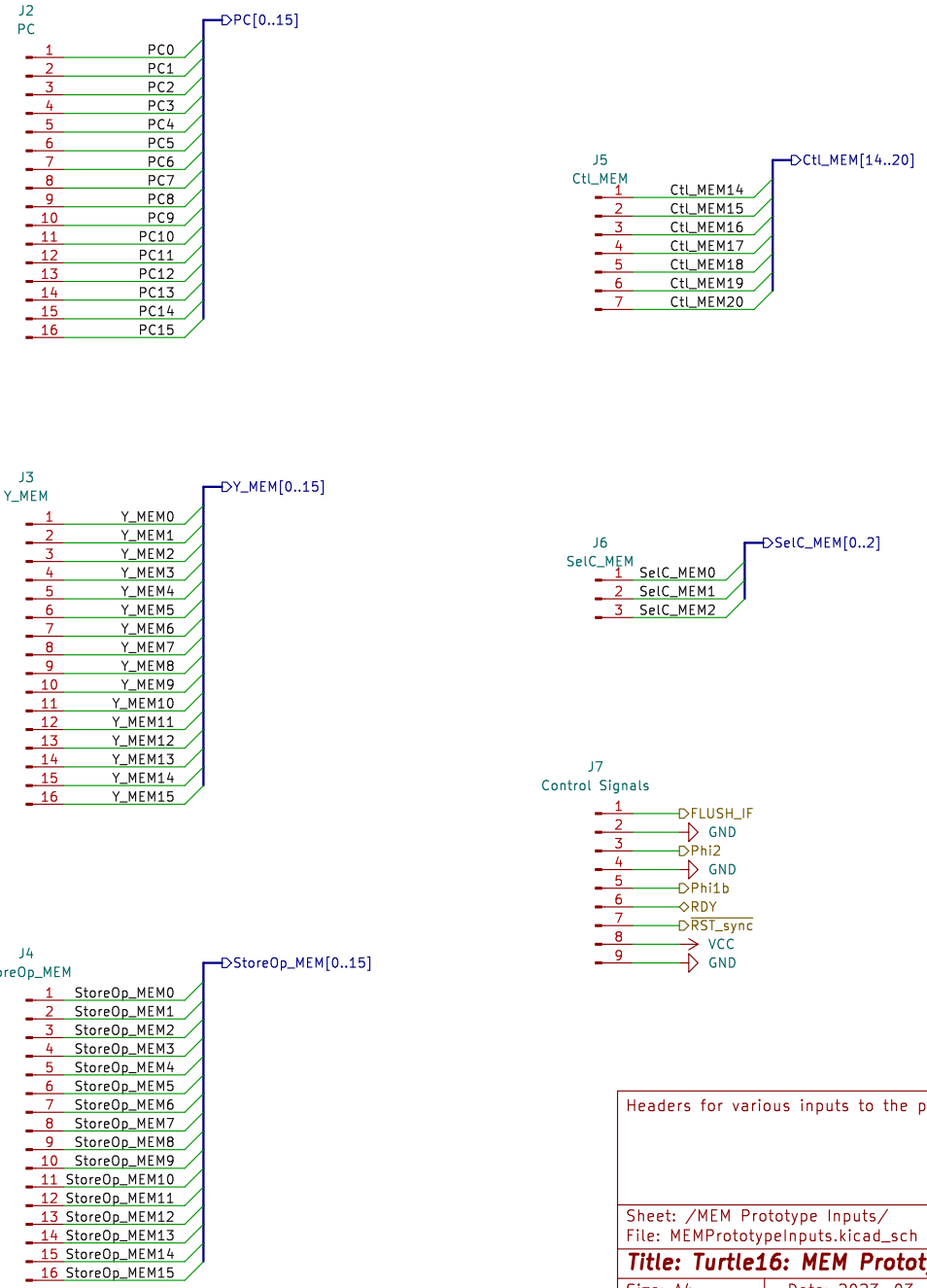
Sheet: /Memory/RAM/		
File: RAM.kicad_sch		
Title: Turtle16: RAM		
Size: A4	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 9/14



Sheet: /MEM/Sheet5FD9EFDA/
File: ALUResultRegister_MEM_WB.kicad_sch

Title: ALU Result Register MEM/WB

Size: USLetter	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 10/14

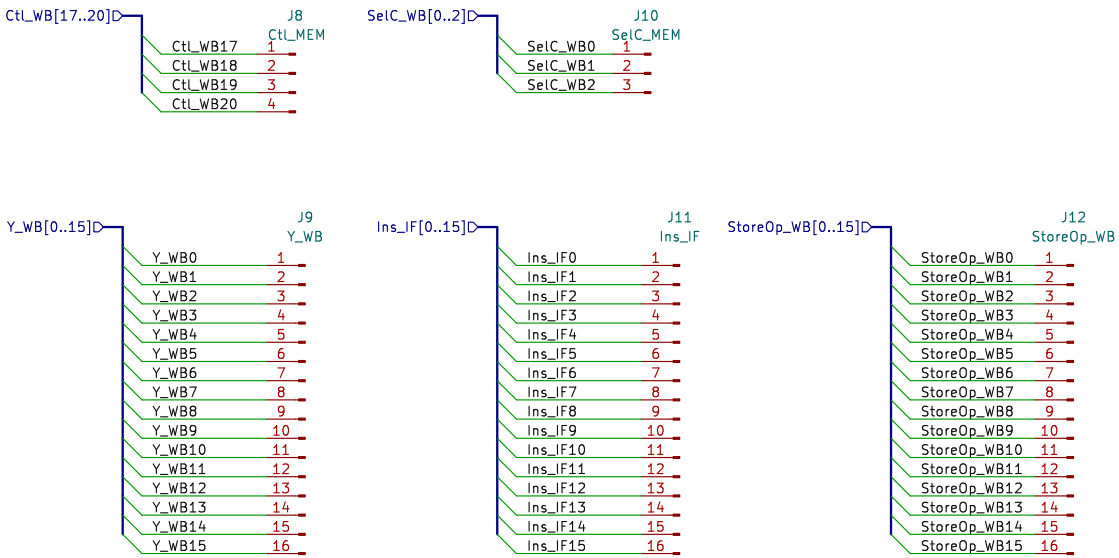


Headers for various inputs to the prototype board

Sheet: /MEM Prototype Inputs/
File: MEMPrototypeInputs.kicad_sch

Title: Turtle16: MEM Prototype Inputs

Size: A4	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 11/14



Headers for various outputs from the prototype board

Sheet: /MEM Prototype Outputs/
File: MEMPrototypeOutputs.kicad_sch

Title: Turtle16: MEM Prototype Outputs

Size: A4	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 12/14

IO[0..15]
Addr[0..15]
Ins_IF[0..15]
PC[0..15]
Bank[0..2]

The Bank register resets to zero when the computer resets. Set the bank register by writing a word to address zero.

When the bank register is zero, the instruction fetch unit is fed by ROM. (The PLD asserts ~~ROMEN~~.)

Otherwise, the instruction fetch unit is fed by one side of the dual port RAM IC. This allows the computer to be reprogrammed at run time.

The PLD allows some other combinations of memory address and bank to be mapped to RAM during load/store over the memory bus. This mapping may be reprogrammed later to accomodate new devices added to the bus. If there are no other devices on the bus then a good default mapping would be to map all banks and memory ranges to RAM.

ROM
PC[0..15]
FLUSH_IF
RAMEN_L
PC[0..15]
FLUSH_IF
RAMEN_L
Ins_IF[0..15]
Ins_IF[0..15]
File: ROM.kicad_sch

RAM
IO[0..15]
Addr[0..15]
PC[0..15]
FLUSH_IF
MemStore
MemLoad
RAMEN_L
RAMEN_L
RAMEN_R
RAMEN_R
IO[0..15]
Addr[0..15]
PC[0..15]
FLUSH_IF
MemStore
MemLoad
RAMEN_L
RAMEN_L
RAMEN_R
RAMEN_R
Ins_IF[0..15]
Ins_IF[0..15]
File: RAM.kicad_sch

VCC
C13
0.1µF
GND

U9
ATF22V10C
Addr0 1 IN/CLK
Addr1 2 IN
Addr2 3 IN
Addr3 4 IN
Addr4 5 IN
Addr5 6 IN
Addr6 7 IN
Addr7 8 IN
Addr8 9 IN
Addr9 10 IN
Addr10 11 IN
24 VCC
I/O 23 RAMEN_L
I/O 22 RAMEN_R
I/O 21
I/O 20 Bank2
I/O 19 Bank1
I/O 18 Bank0
I/O 17 Addr15
I/O 16 Addr14
I/O 15 Addr13
I/O 14 Addr12
I/O 13 Addr11
GND 12
IN/OE

VCC
C12
0.1µF
GND

U10
CD74HC173PWR
IO0 14 D0
IO1 13 D1
IO2 12 D2
IO3 11 D3
16 VCC
Q0 3 Bank0
Q1 4 Bank1
Q2 5 Bank2
Q3 6
GND 1 Oe1
2 Oe2
9 E1
10 E2
Phi1b 7 Cp
RST_sync 15 Mr
GND 8

U2C
74AHCT04
RAMEN_L 5
6 RAMEN_L

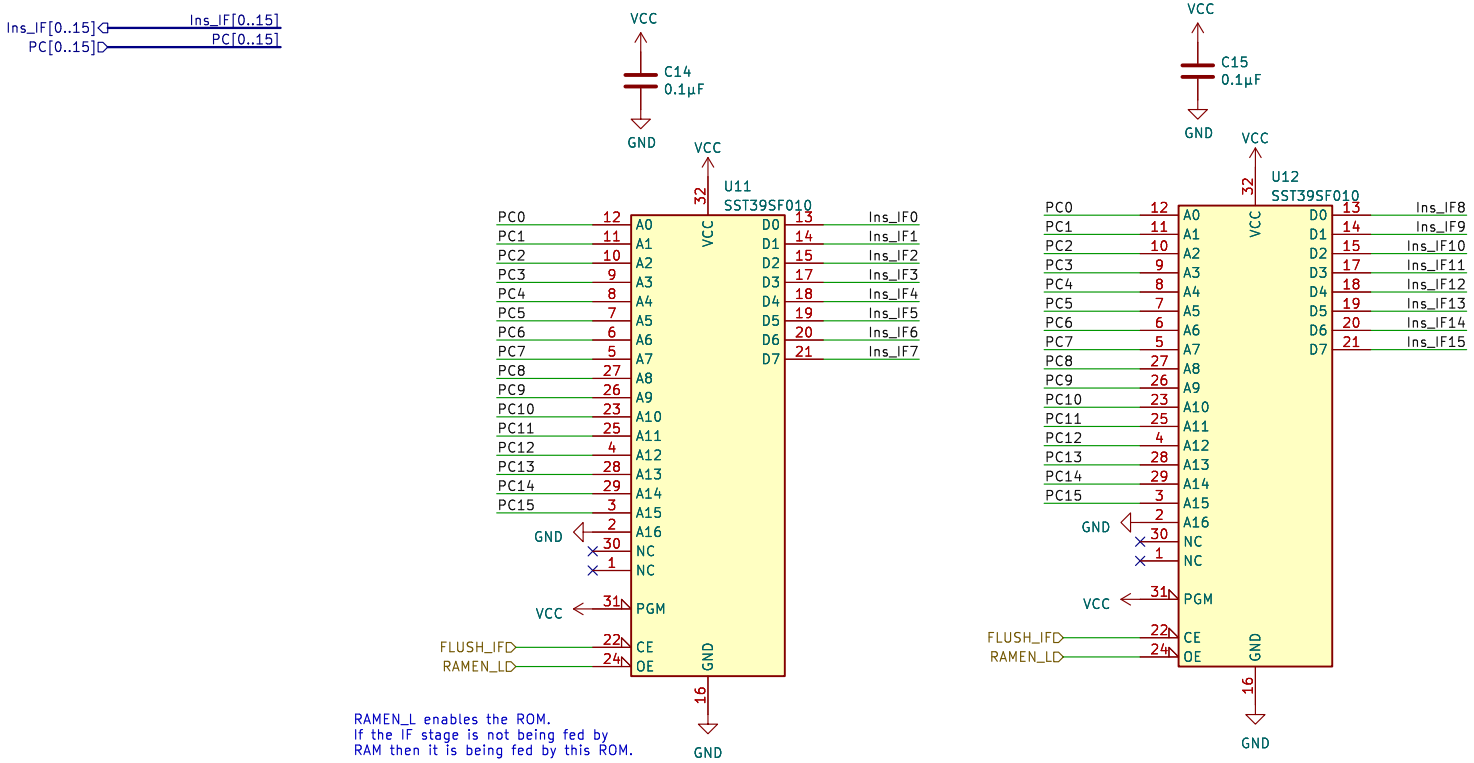
U2D
74AHCT04
RAMEN_R 9
8 RAMEN_R

TP42
TestPoint TP43
RAMEN_L
RAMEN_L
TestPoint TP44
TestPoint TP45
RAMEN_R
RAMEN_R
TestPoint

Sheet: /Memory/
File: Memory.kicad_sch

Title:

Size: A4	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 13/14



Sheet: /Memory/ROM/		
File: ROM.kicad_sch		
Title:		
Size: A4	Date: 2023-03-22	**Rev: B**
KiCad E.D.A. kicad 7.0.8		Id: 14/14