Sheet: Register XY

File: Register XY.sch

Sheet: Register A

File: Register A.sch

Sheet: Clock

File: Clock.sch

Sheet: Program Counter

File: Program Counter.sch

Sheet: Register B

File: Register B.sch

Sheet: Power-on Reset

File: Power-on Reset.sch

Sheet: Link Register

File: Link Register.sch

Sheet: ALU

File: ALU.sch

Sheet: Data RAM

File: Data RAM.sch

Sheet: Instruction Fetch

File: Instruction Fetch.sch

Sheet: Shifter

File: Shifter.sch

Sheet: Register D

File: Register D.sch

Sheet: Instruction Decode

File: Instruction Decode.sch

Sheet: Bus Display

File: Bus Display.sch

Sheet: Expansion

File: Expansion.sch

Sheet: Execute

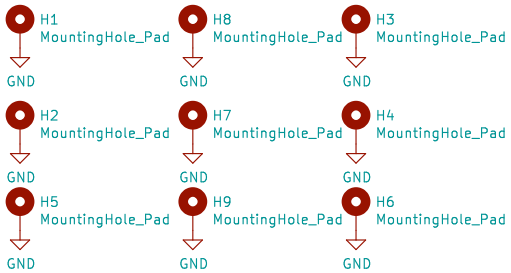
File: Execute.sch

Sheet: Power Supply

File: PowerSupply.sch

Sheet: Register K

File: Register K.sch

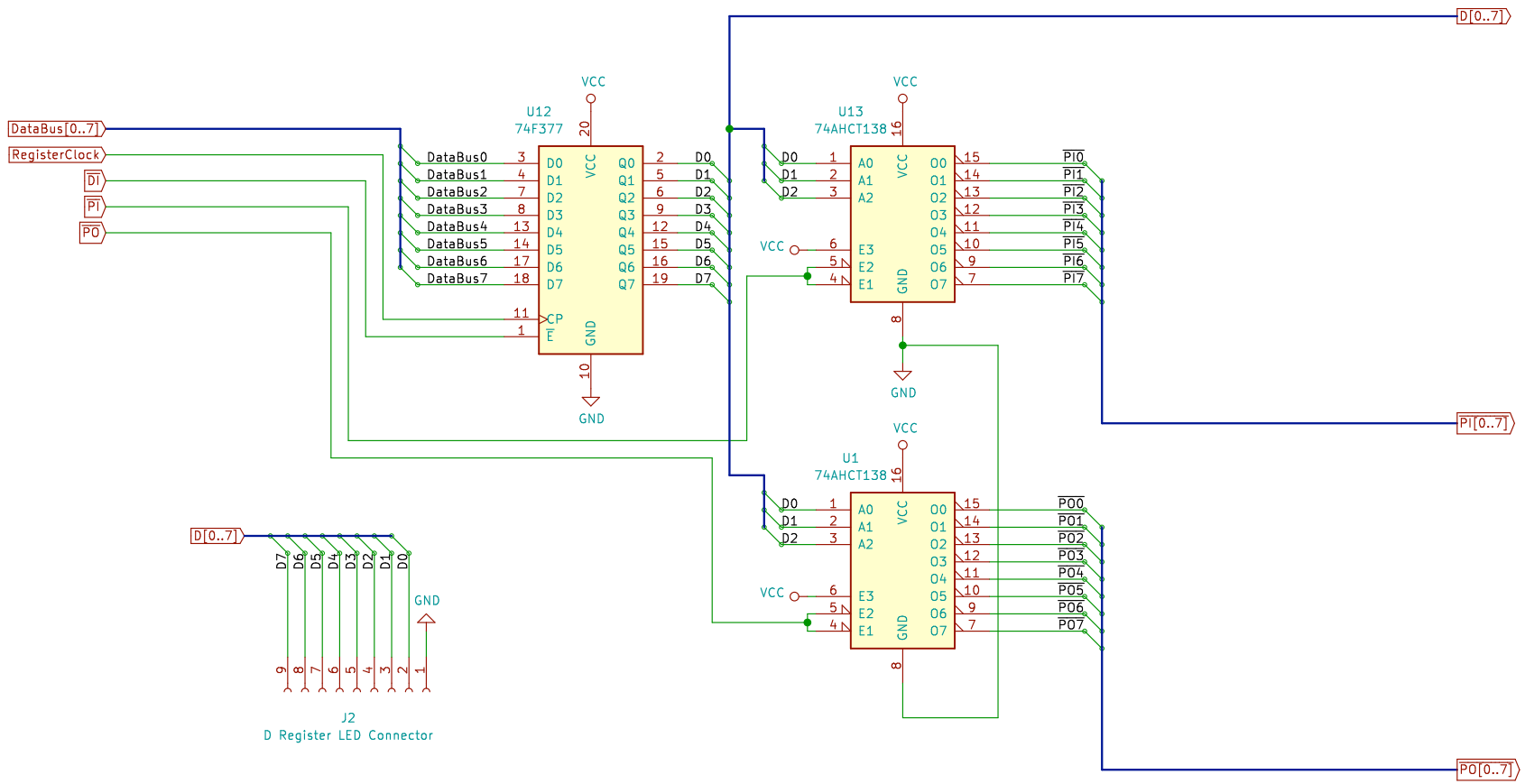


TTL microcomputer built from 74xx series logic chips.

Sheet: /
File: MainBoard.sch

Title: TurtleTTL: Main Board

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 1/23

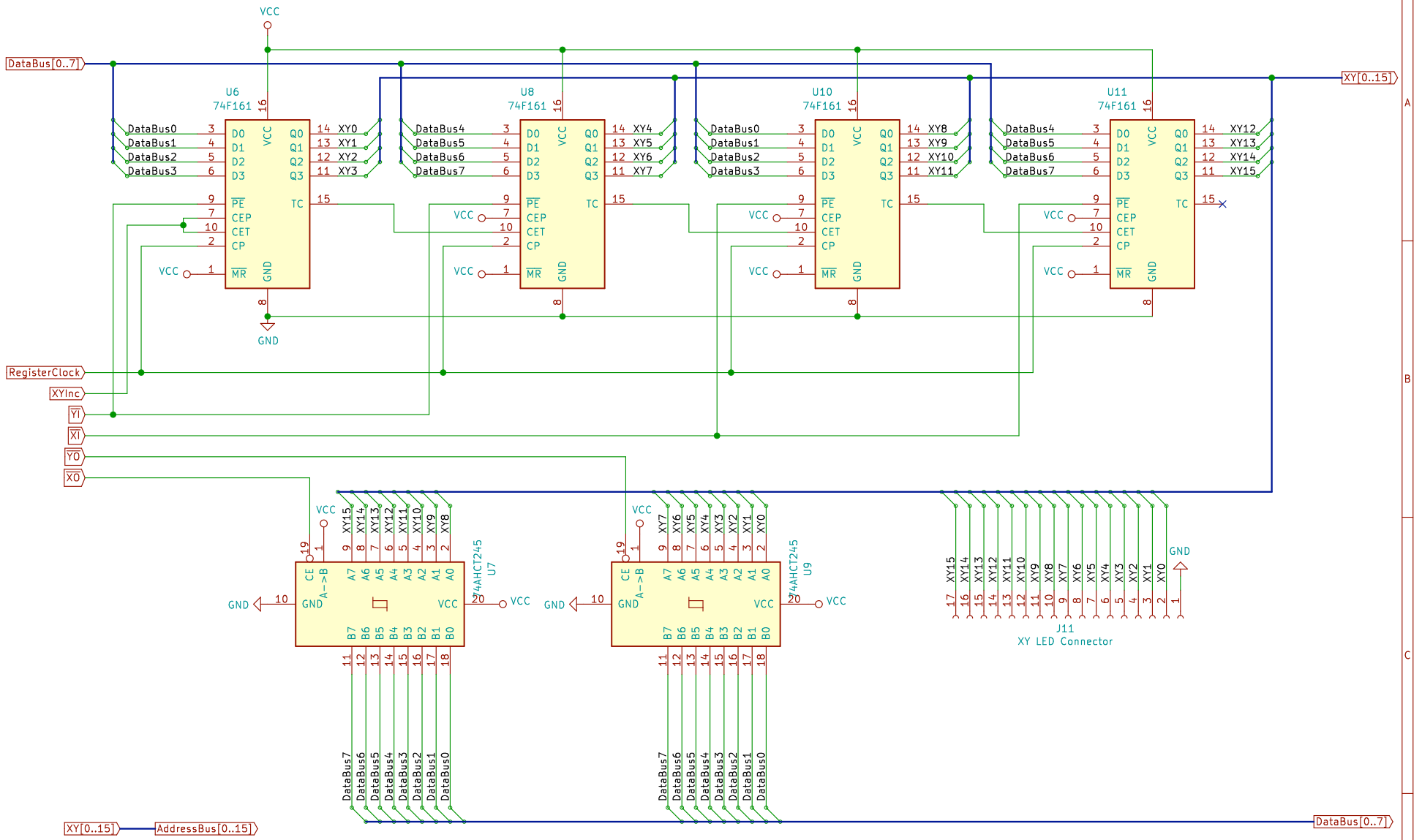


Register D controls the device select lines for peripherals and memory.

Sheet: /Register D/
File: Register D.sch

Title: Register D

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 2/23

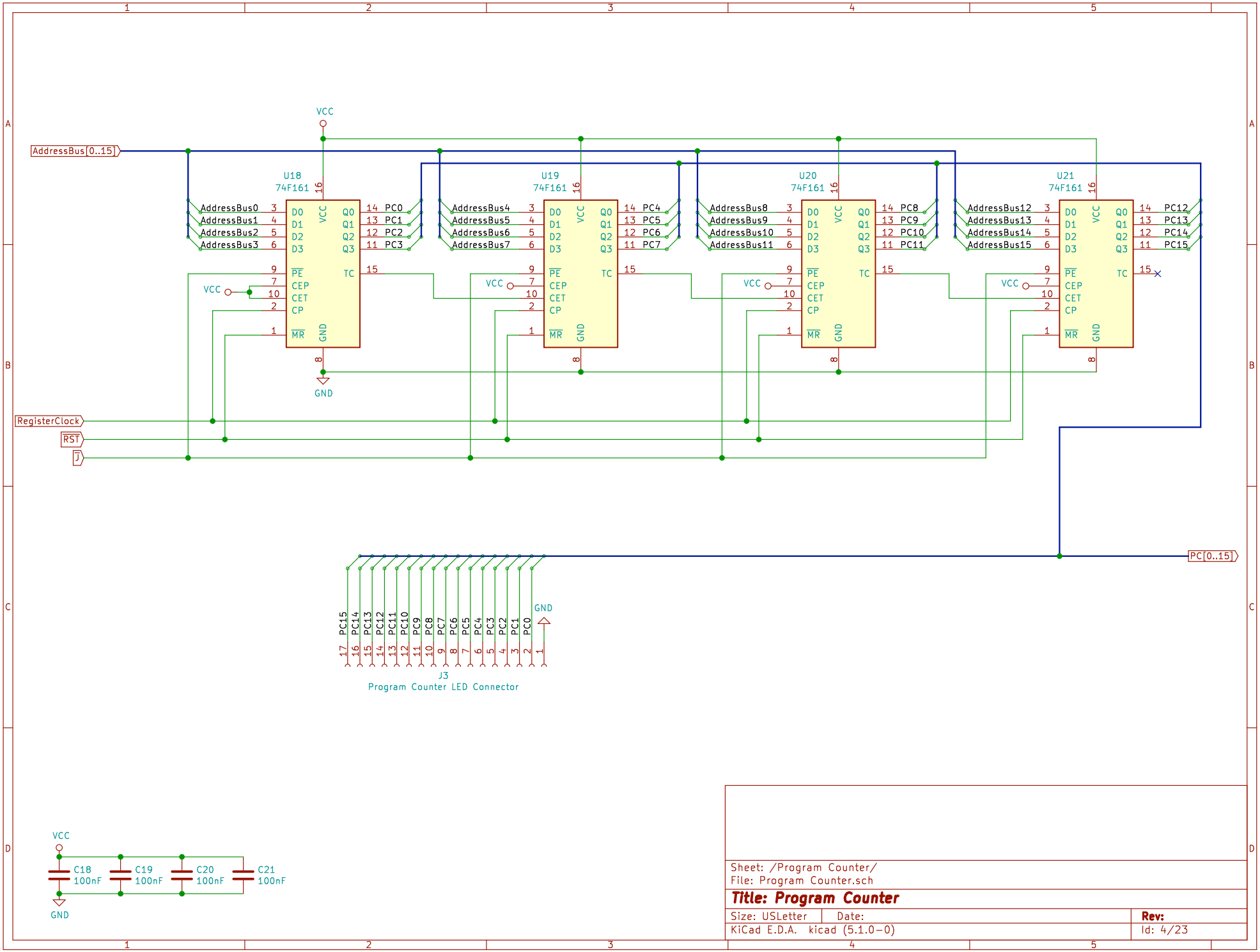


The XY register pair sets the value on the sixteen-bit Address Bus.

Sheet: /Register XY/
File: Register XY.sch

Title: Registers X and Y

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 3/23



Sheet: /Program Counter/
File: Program Counter.sch

Title: Program Counter

Size: USLetter | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.0-0) | Id: 4/23

Sheet: PC/IF

File: PC_IF.sch

Sheet: Instruction ROM

File: Instruction ROM.sch

Sheet: Instruction RAM

File: Instruction RAM.sch

Sheet: Instruction Register

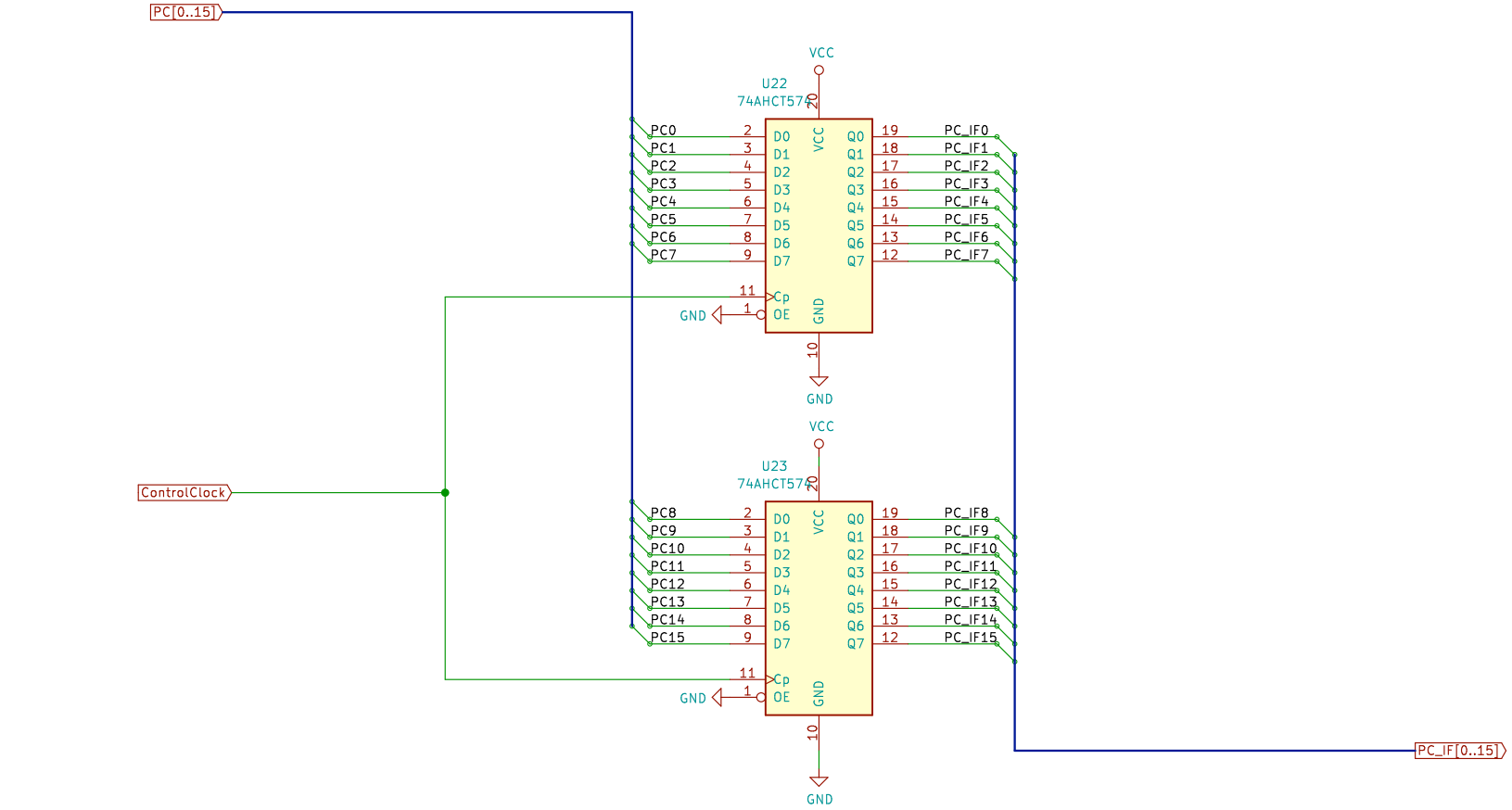
File: Instruction Register.sch

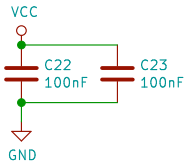
Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

Title: Instruction Fetch

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 5/23



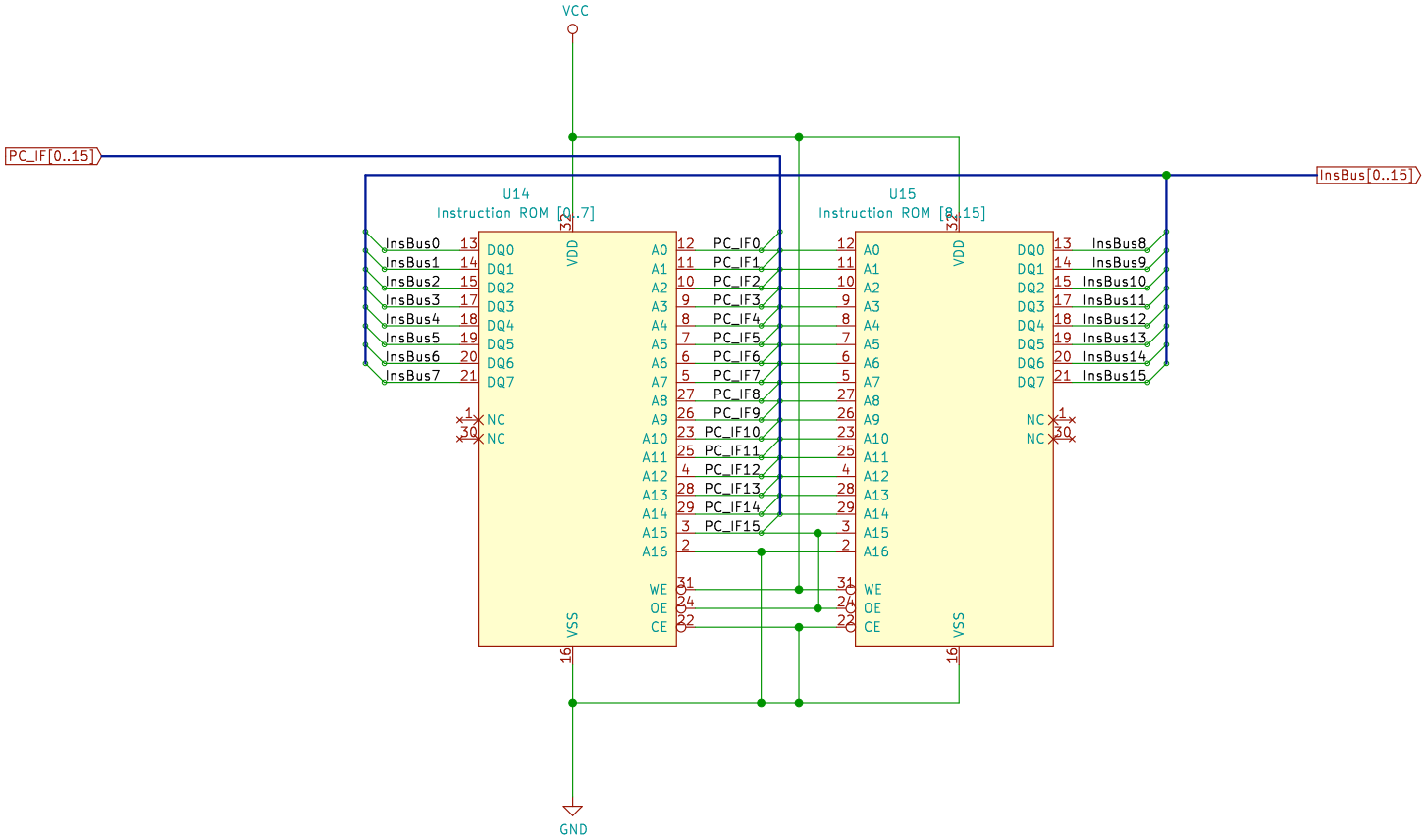


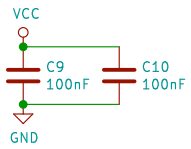
The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /Instruction Fetch/PC/IF/
File: PC_IF.sch

Title: PC/IF

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 6/23



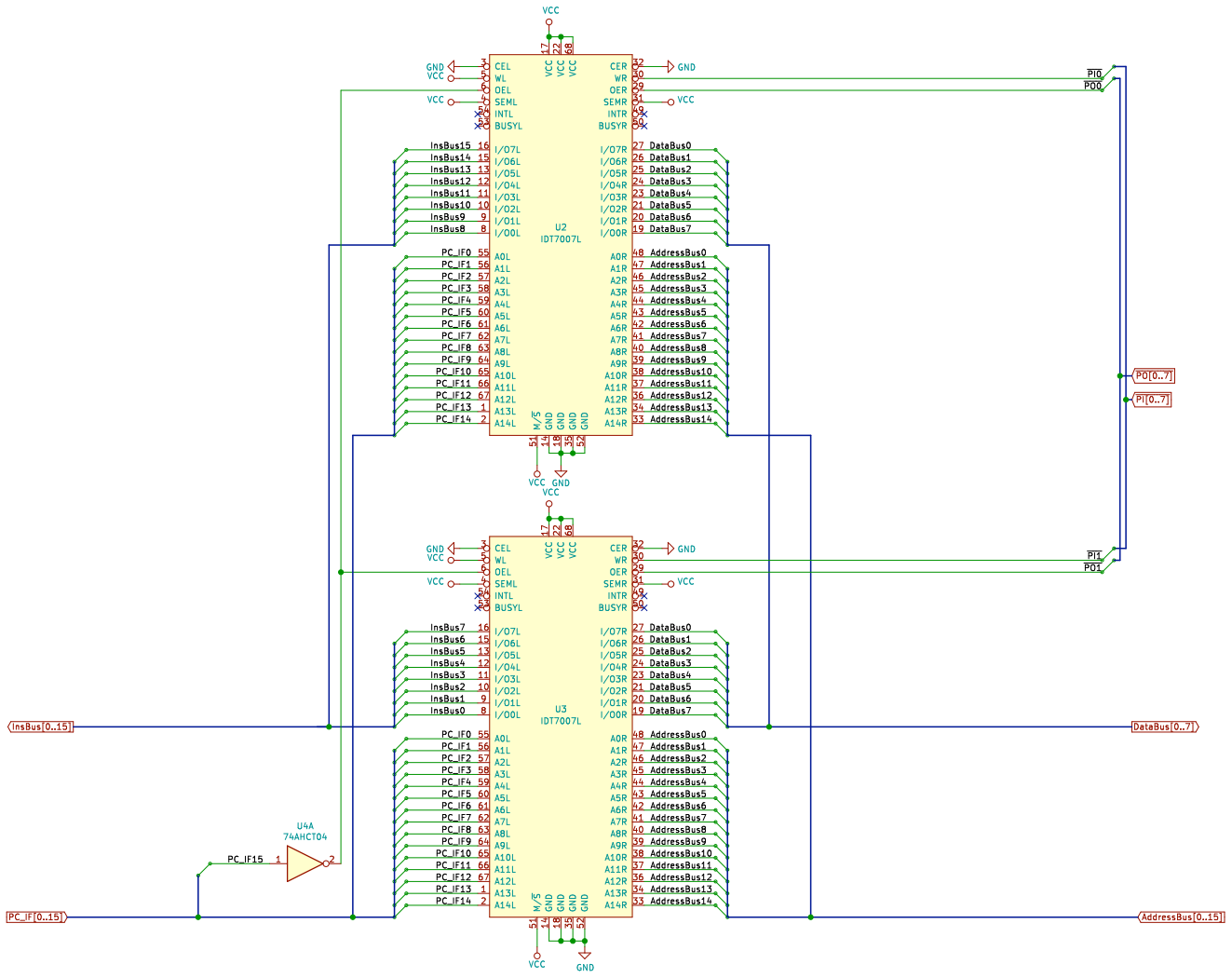


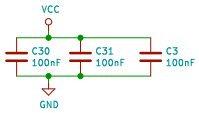
Instruction ROM is located on a daughter board.
This schematic describes the connectors by attach it to the main board.

Sheet: /Instruction Fetch/Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 7/23



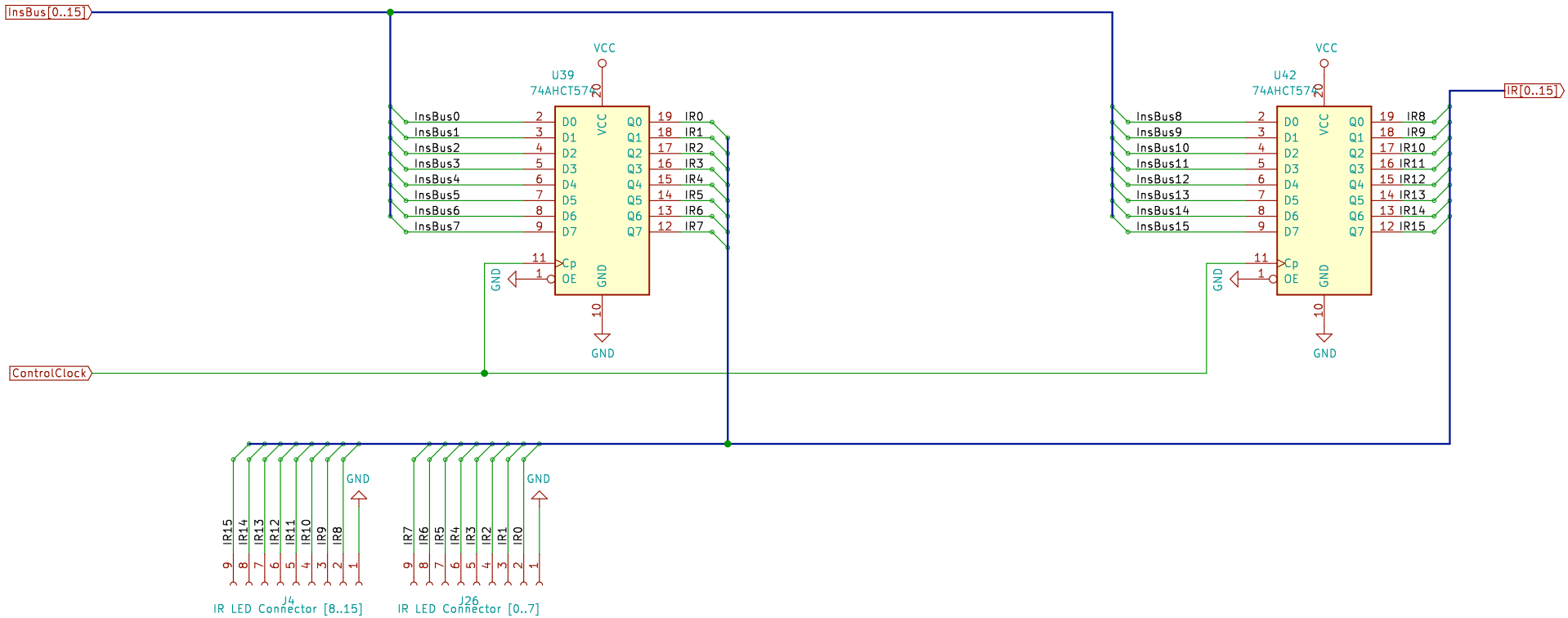


The Instruction RAM module allows a portion of Instruction Memory to be accessed from the data bus.

Sheet: /Instruction Fetch/Instruction RAM/
File: Instruction RAM.sch

Title: Instruction RAM

Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 8/23

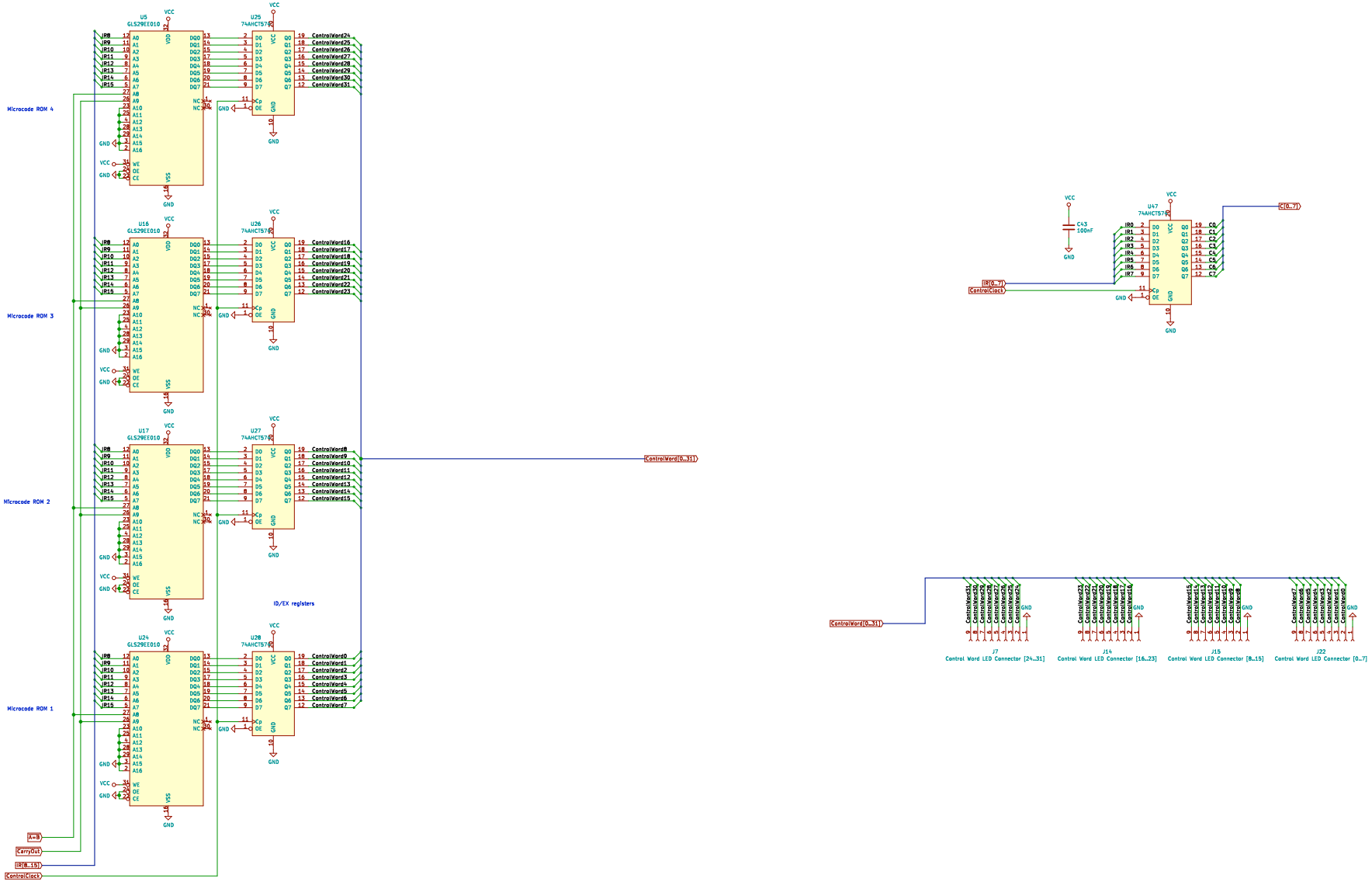


The Instruction Register receives input from either Instruction ROM or Instruction RAM.

Sheet: /Instruction Fetch/Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 9/23

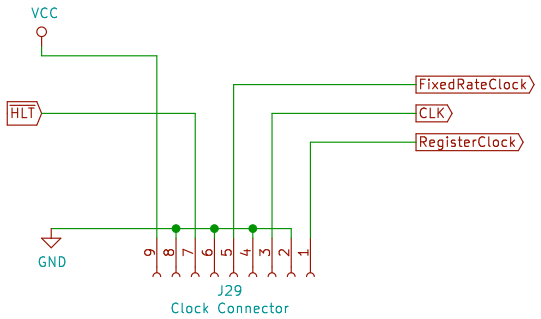


The instruction Decoder decodes an eight bit opcode into a 32-bit control word.

Sheet: /Instruction Decode/
File: Instruction Decode.sch

Title: Instruction Decode

Size: A2	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		id: 10/23

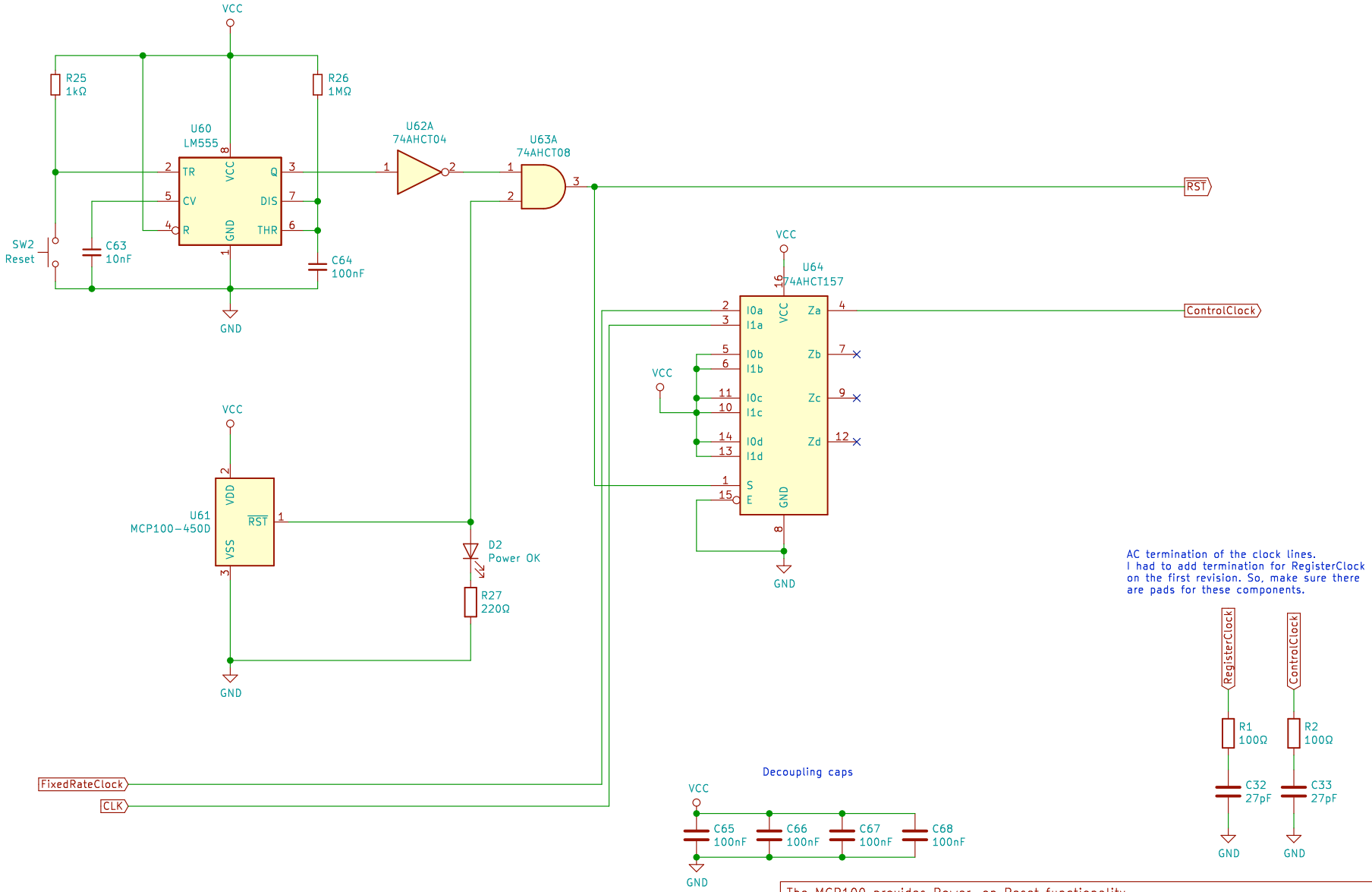


The clock module is located on an external board.

Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 11/23

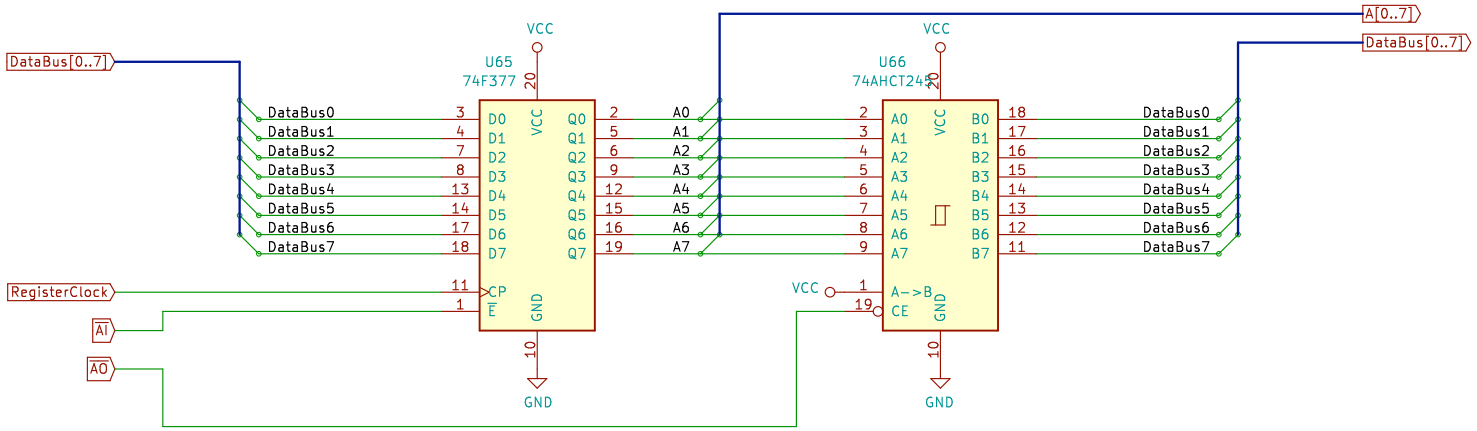


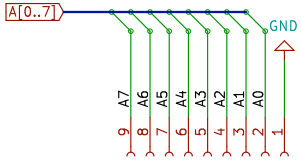
The MCP100 provides Power-on Reset functionality.
A button is also provided to manually reset the machine.
During reset, the control clock is pulsed repeatedly to flush the pipeline.

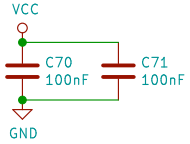
Sheet: /Power-on Reset/
File: Power-on Reset.sch

Title: Power-on Reset

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 12/23





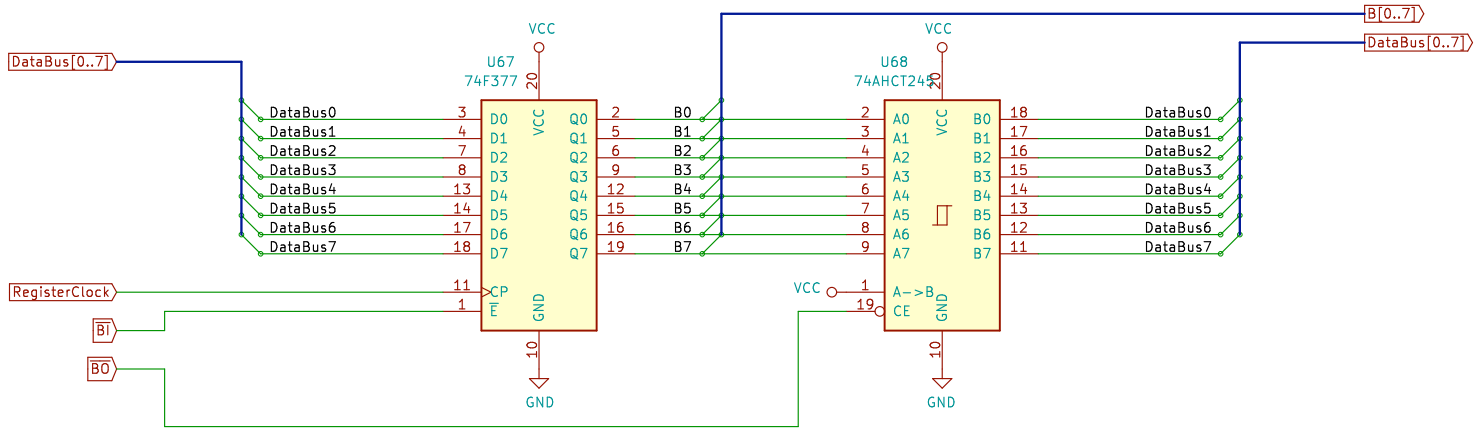


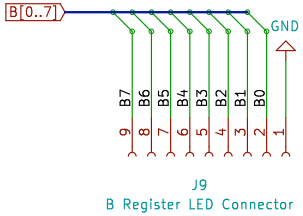
Register A is wired to the ALU's A operand.

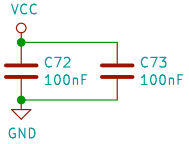
Sheet: /Register A/
File: Register A.sch

Title: Register A

Size: A | Date: | **Rev:**
KiCad E.D.A. kicad (5.1.0-0) | Id: 13/23





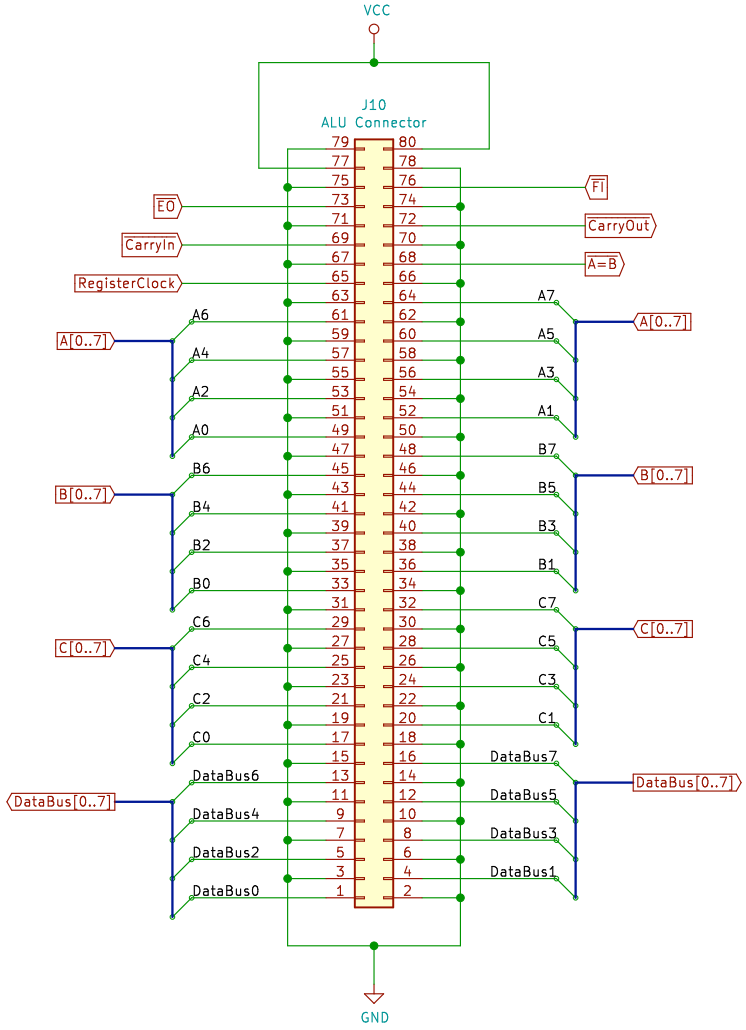


Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

Title: Register B

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 14/23

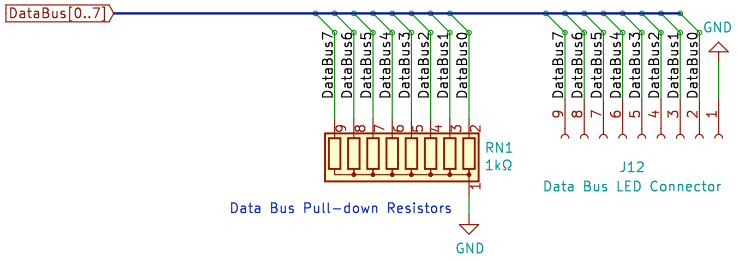


The ALU is located on an external card.
The ALU operands are directly wired to the A and B registers.
The bits of the constant register provide the ALU control signals.

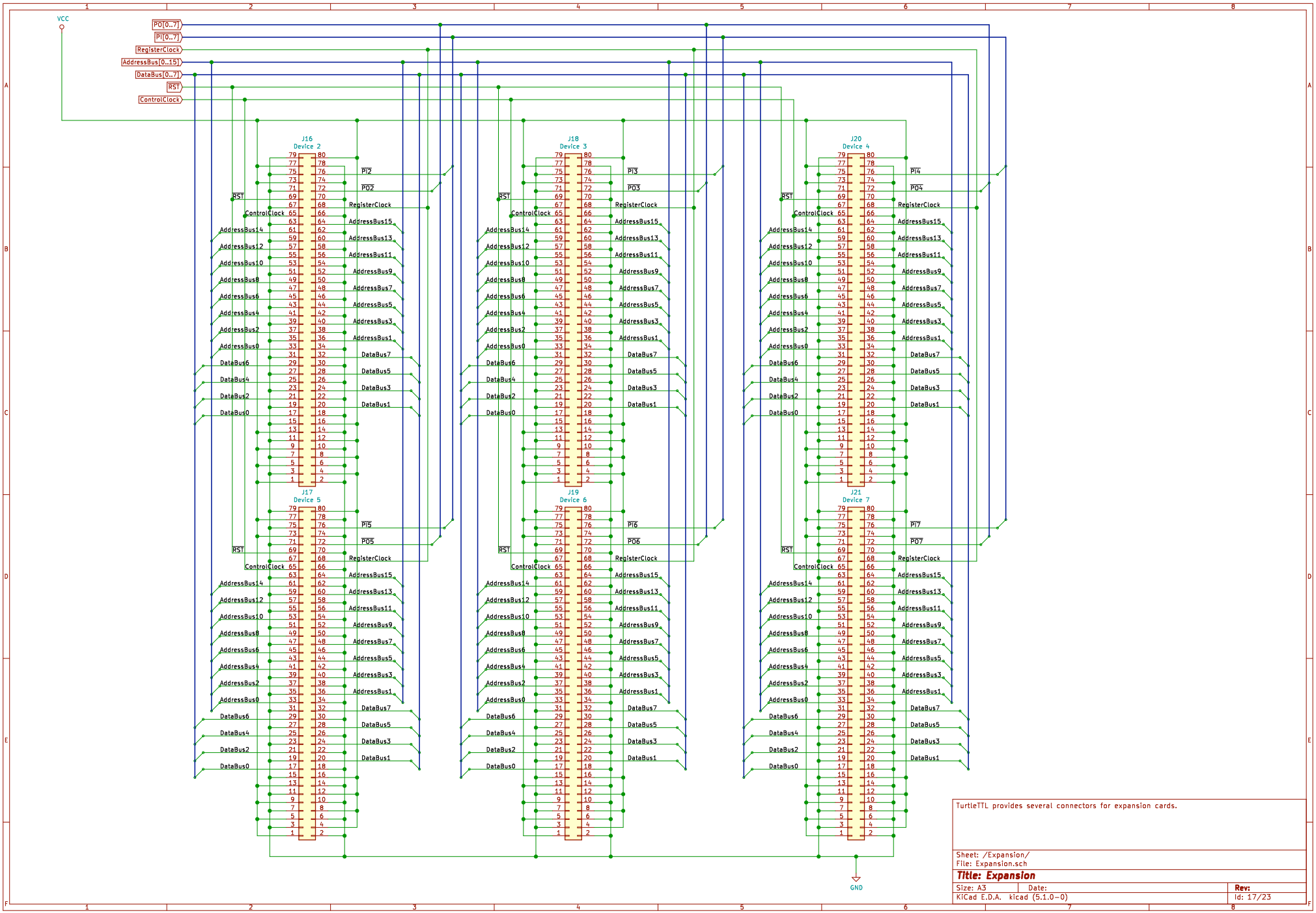
Sheet: /ALU/
File: ALU.sch

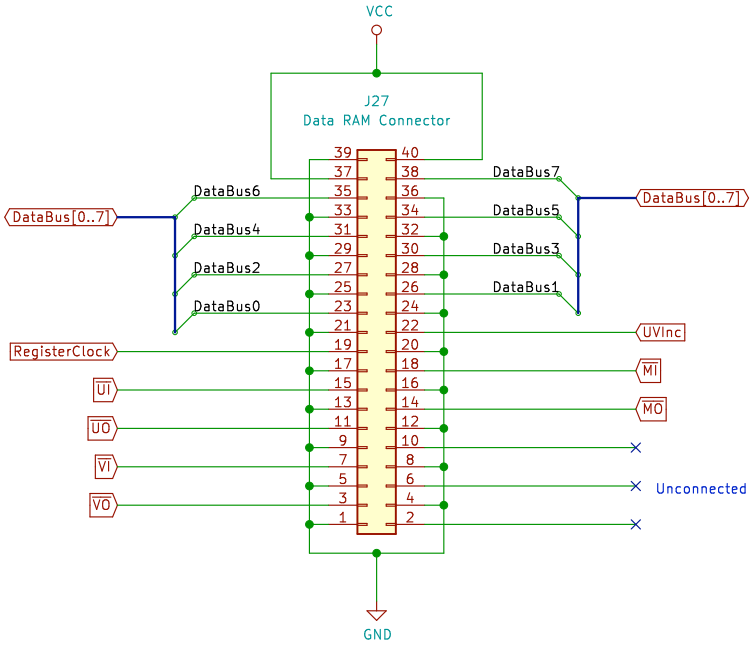
Title: ALU

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 15/23



Sheet: /Bus Display/		
File: Bus Display.sch		
Title: Bus Display		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 16/23


VCC
PO[0..7]
PI[0..7]
RegisterClock
AddressBus[0..15]
DataBus[0..7]
RST
ControlClock
J16
Device 2
J17
Device 5
J18
Device 3
J19
Device 6
J20
Device 4
J21
Device 7
PI2
PO2
PI5
PO5
PI3
PO3
PI6
PO6
PI4
PO4
PI7
PO7
GND
TurtleTTL provides several connectors for expansion cards.
Sheet: /Expansion/
File: Expansion.sch
Title: Expansion
Size: A3
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 17/23

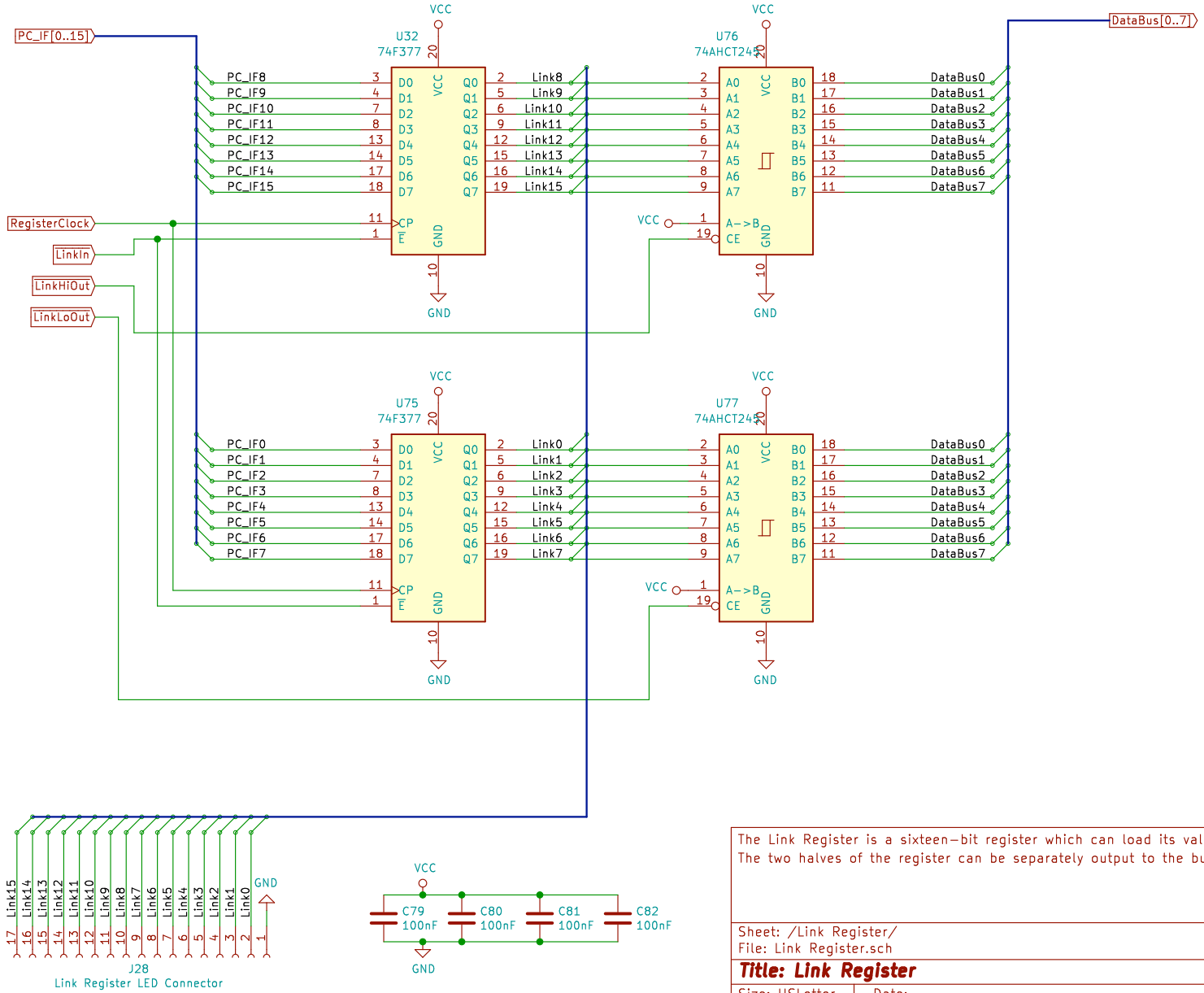


The Data RAM and its address registers are located on an external card.

Sheet: /Data RAM/
File: Data RAM.sch

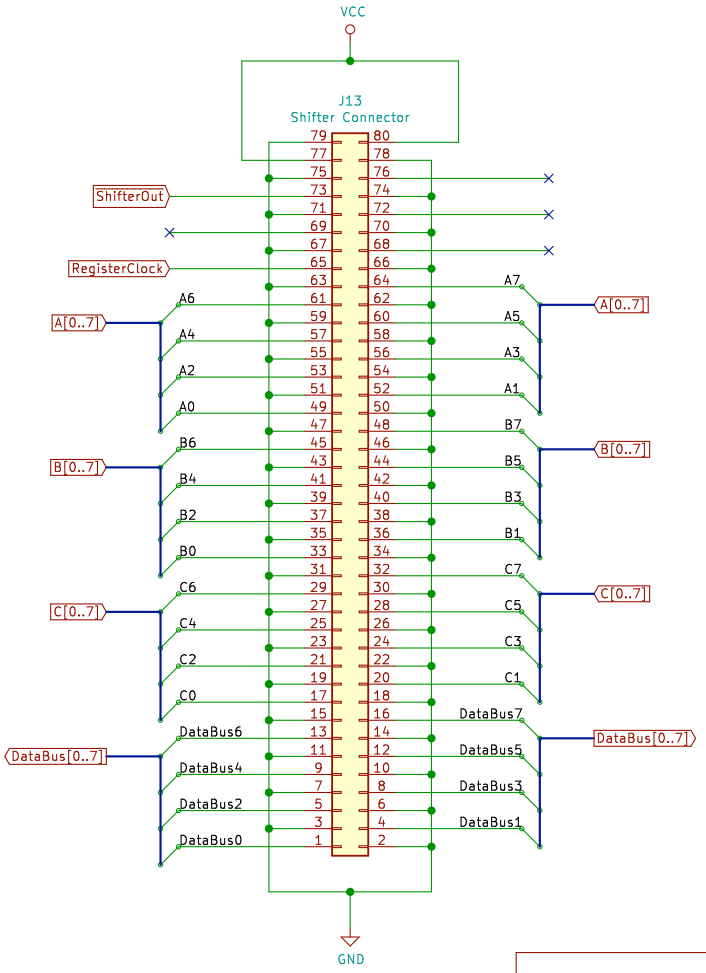
Title: Data RAM

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 18/23



The Link Register is a sixteen-bit register which can load its value from PC.
The two halves of the register can be separately output to the bus.

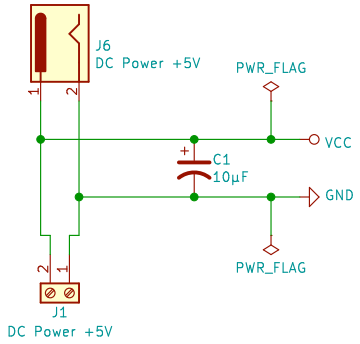
Sheet: /Link Register/	
File: Link Register.sch	
Title: Link Register	
Size: USLetter Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)	Id: 19/23



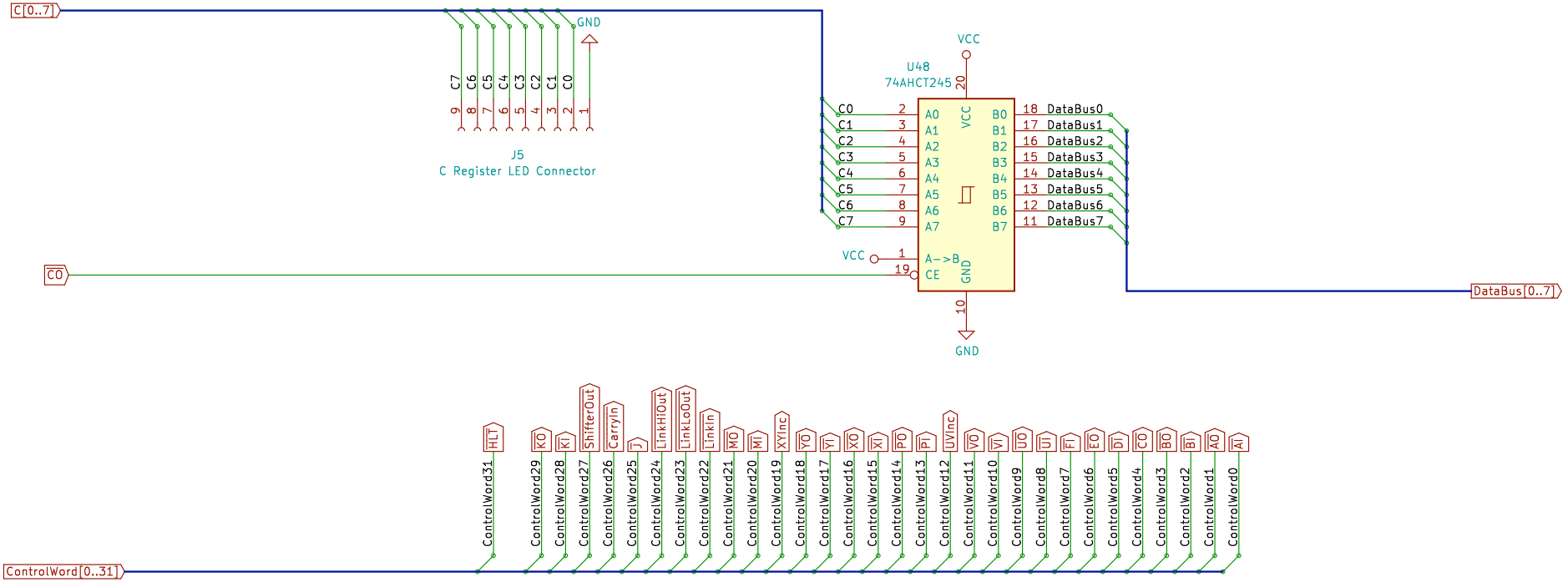
Sheet: /Shifter/
File: Shifter.sch

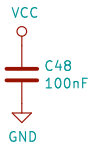
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 20/23



Sheet: /Power Supply/ File: PowerSupply.sch		
Title: Power Supply		
Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 21/23



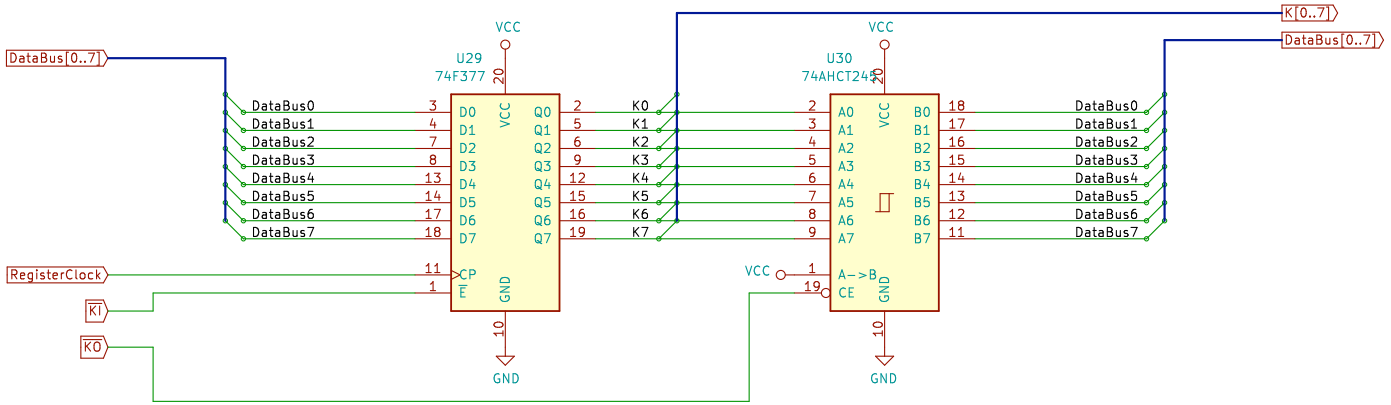


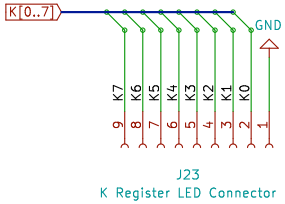
The lower eight bits of the instruction register can be expressed onto the data bus as a constant value.

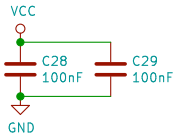
Sheet: /Execute/
File: Execute.sch

Title: Execute

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 22/23







Eight-bit general-purpose register "K"

Sheet: /Register K/
File: Register K.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 23/23