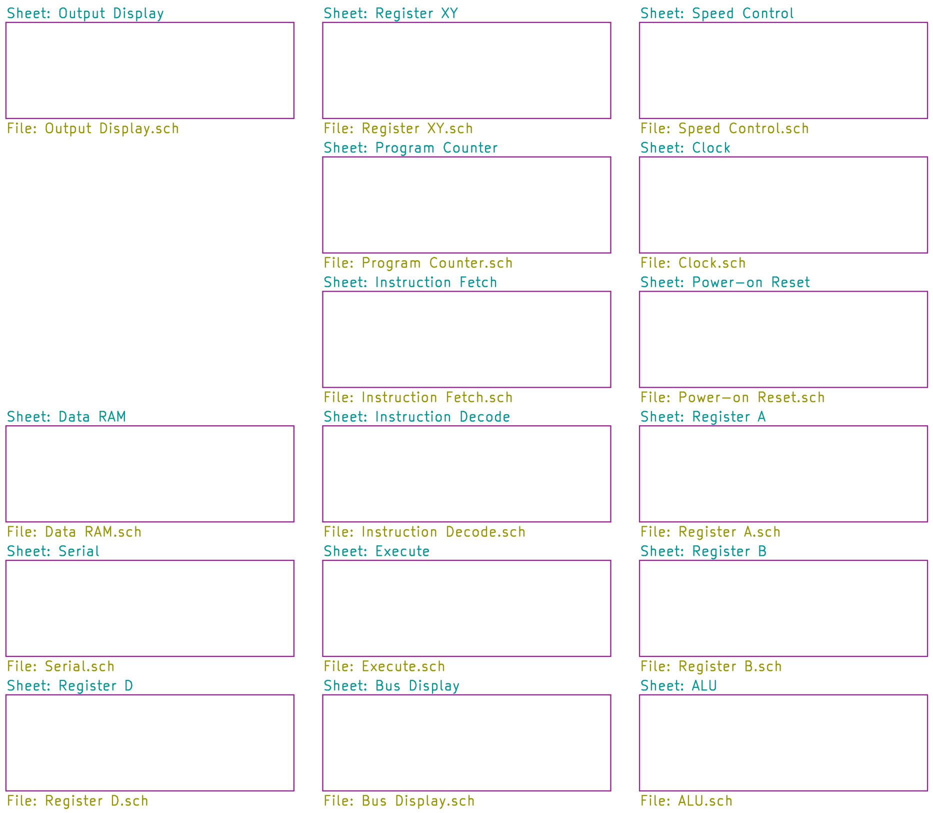
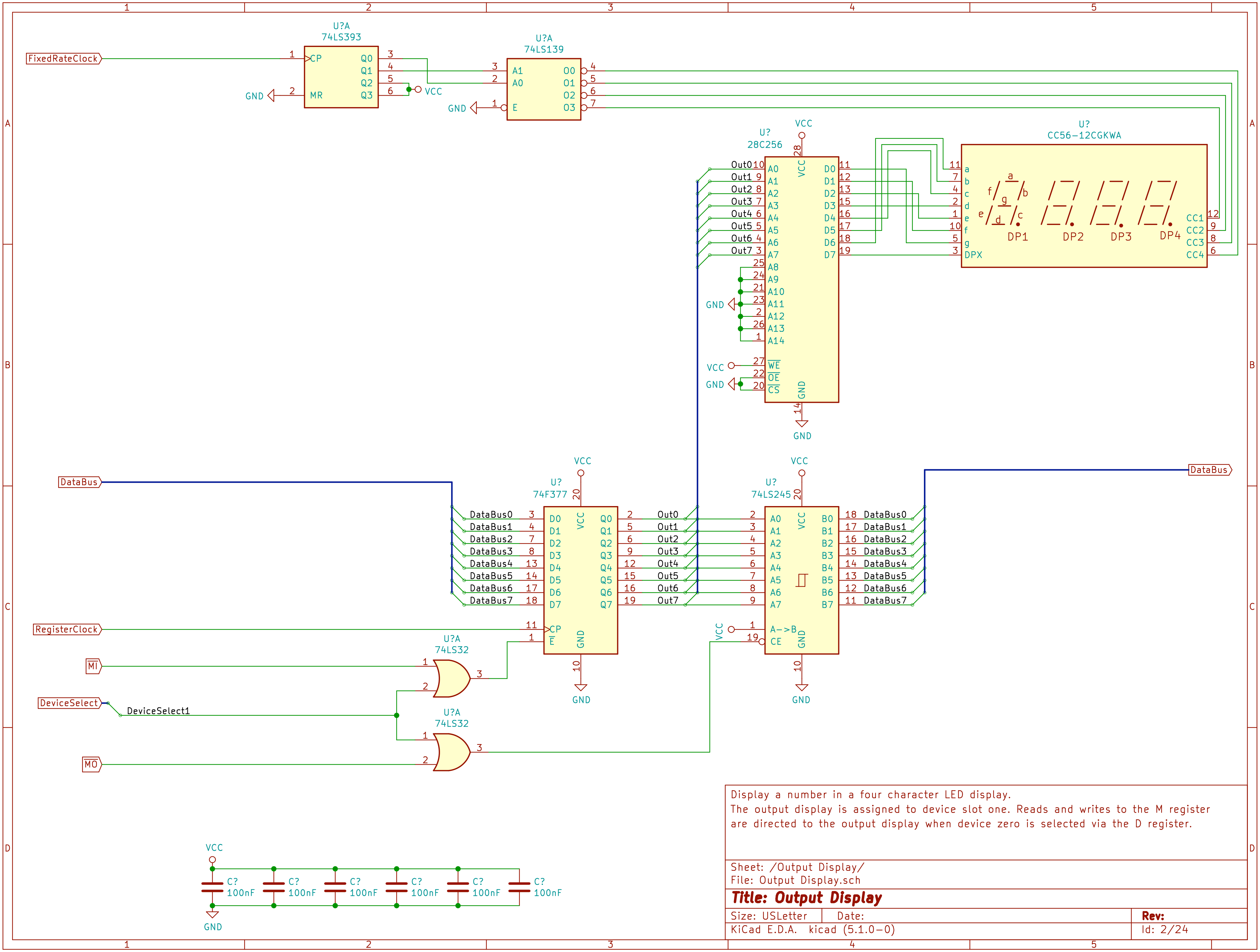


TTL microcomputer built from 74xx series logic chips.

Sheet: /
File: TurtleTTL.sch

Title: Turtle TTL

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0–0)		Id: 1/24

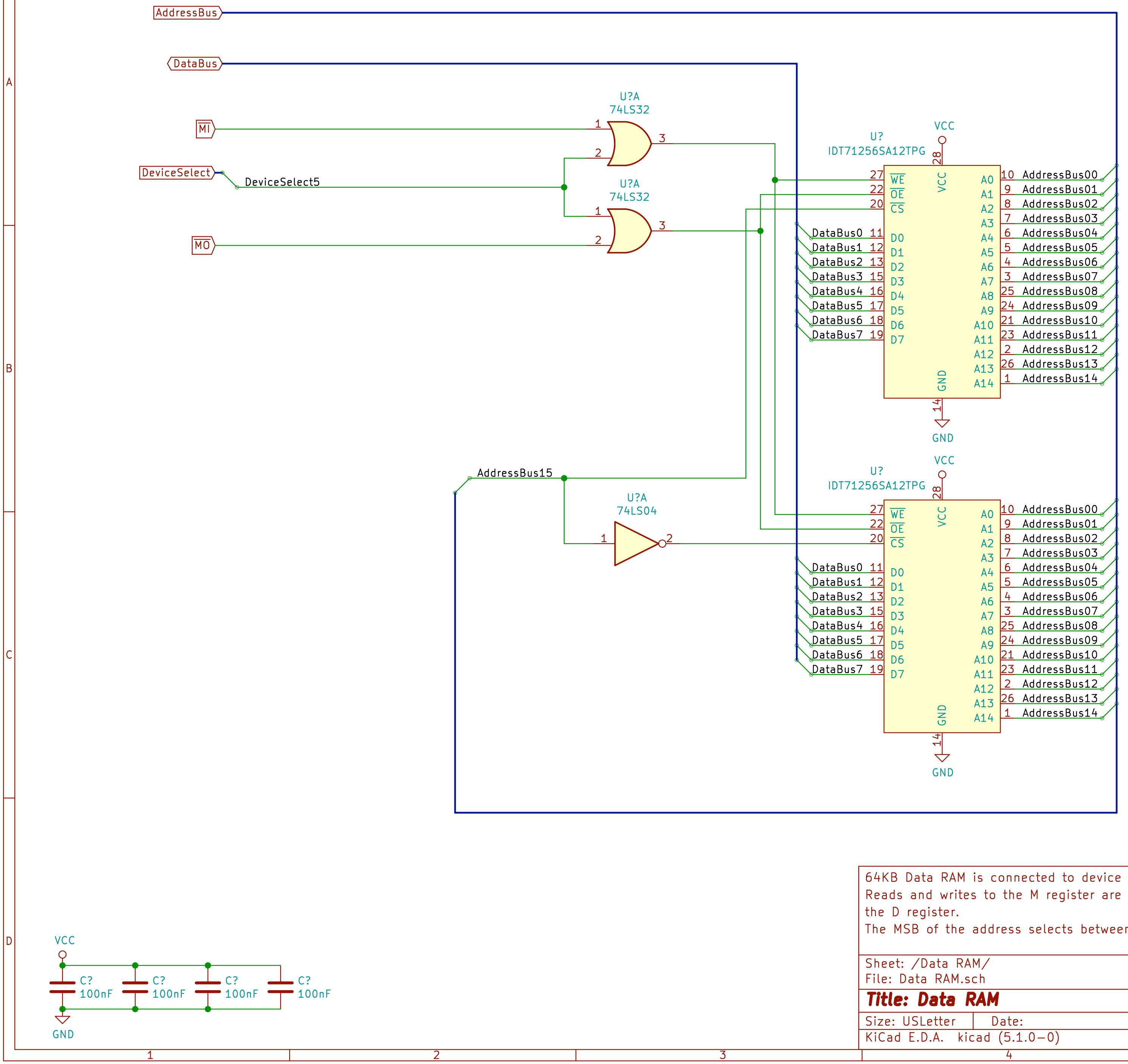


Display a number in a four character LED display.
The output display is assigned to device slot one. Reads and writes to the M register are directed to the output display when device zero is selected via the D register.

Sheet: /Output Display/
File: Output Display.sch

Title: Output Display

Size: USLetter Date: Rev:
KiCad E.D.A. kicad (5.1.0–0) Id: 2/24

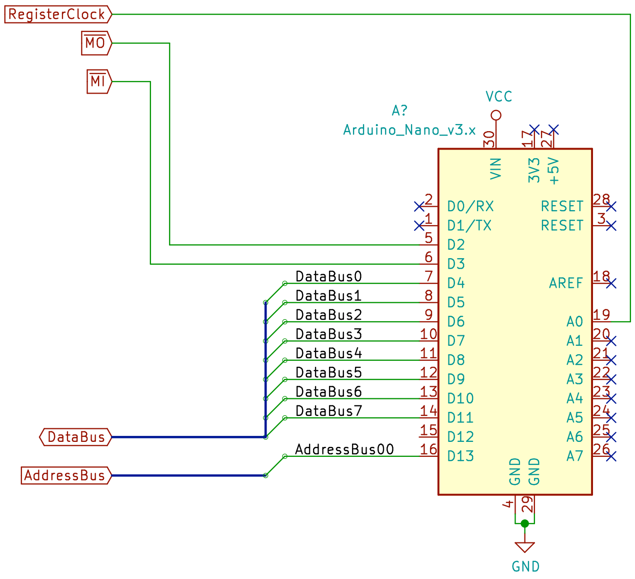


64KB Data RAM is connected to device slot five.
Reads and writes to the M register are directed to Data RAM when device 5 is selected via the D register.
The MSB of the address selects between two 32KB SRAM ICs.

Sheet: /Data RAM/
File: Data RAM.sch

Title: Data RAM

Size: USLetter Date: Rev:
KiCad E.D.A. kicad (5.1.0-0) Id: 3/24

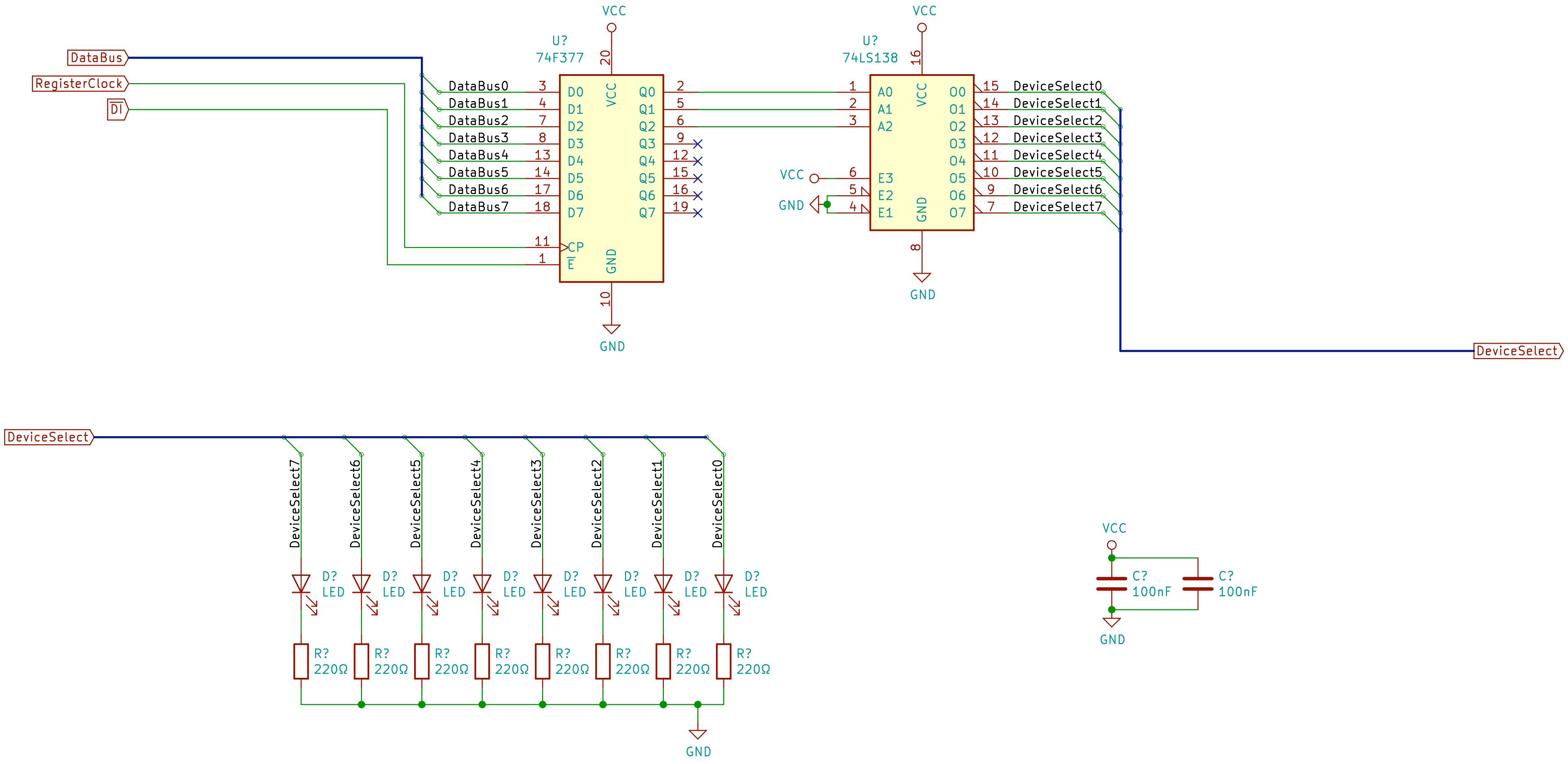


An Arduino Nano serves as a serial interface module.

Sheet: /Serial/
File: Serial.sch

Title: Serial I/O

Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 4/24

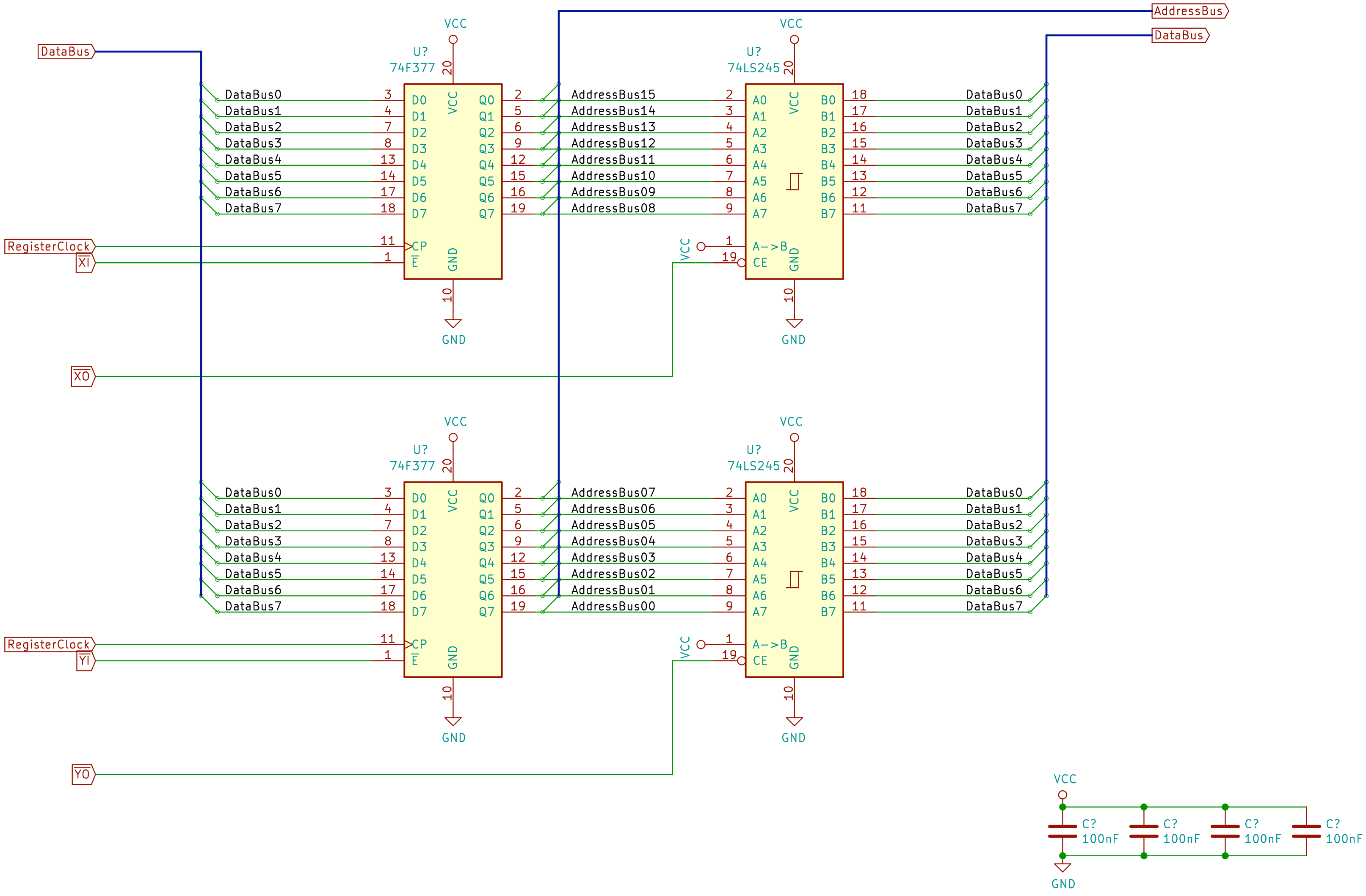


Register D controls the device select lines for peripherals and memory.

Sheet: /Register D/
File: Register D.sch

Title: Register D

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 5/24



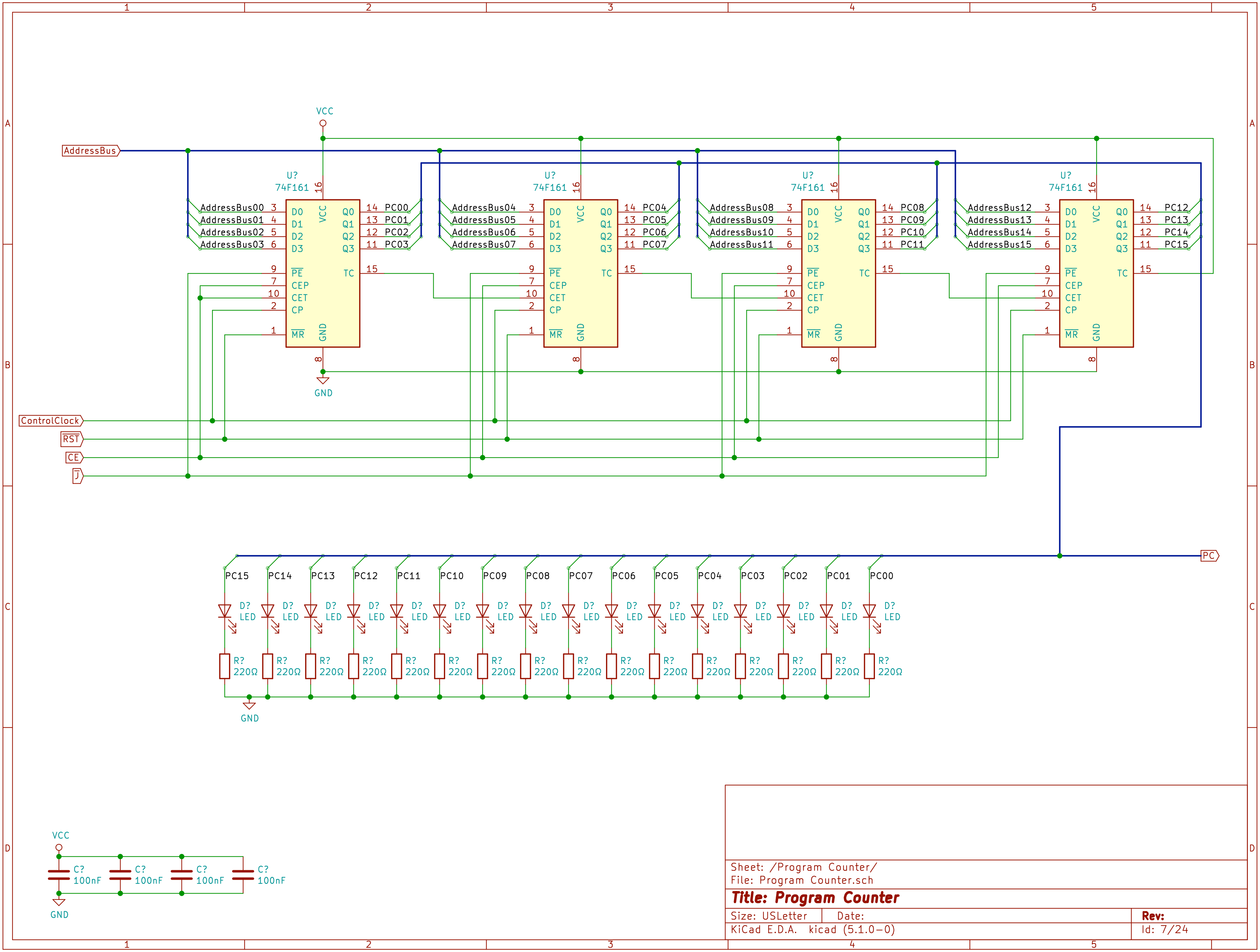
The XY register pair sets the value on the sixteen-bit Address Bus.

Sheet: /Register XY/
File: Register XY.sch

Title: Registers X and Y

Size: USLetter Date: Rev:

KiCad E.D.A. kicad (5.1.0-0) Id: 6/24

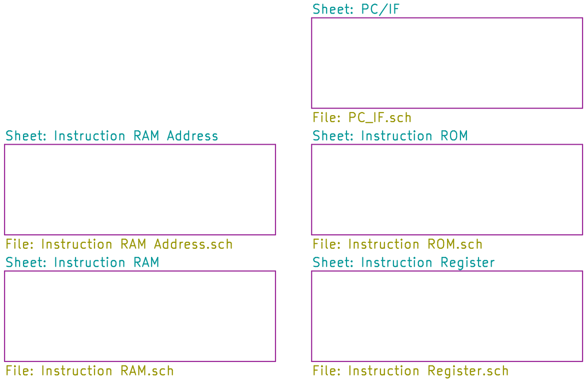


Sheet: /Program Counter/
File: Program Counter.sch

Title: Program Counter

Size: USLetter Date: Rev:

KiCad E.D.A. kicad (5.1.0-0) Id: 7/24



Sheet: PC/IF
File: PC_IF.sch

Sheet: Instruction RAM Address
File: Instruction RAM Address.sch

Sheet: Instruction ROM
File: Instruction ROM.sch

Sheet: Instruction RAM
File: Instruction RAM.sch

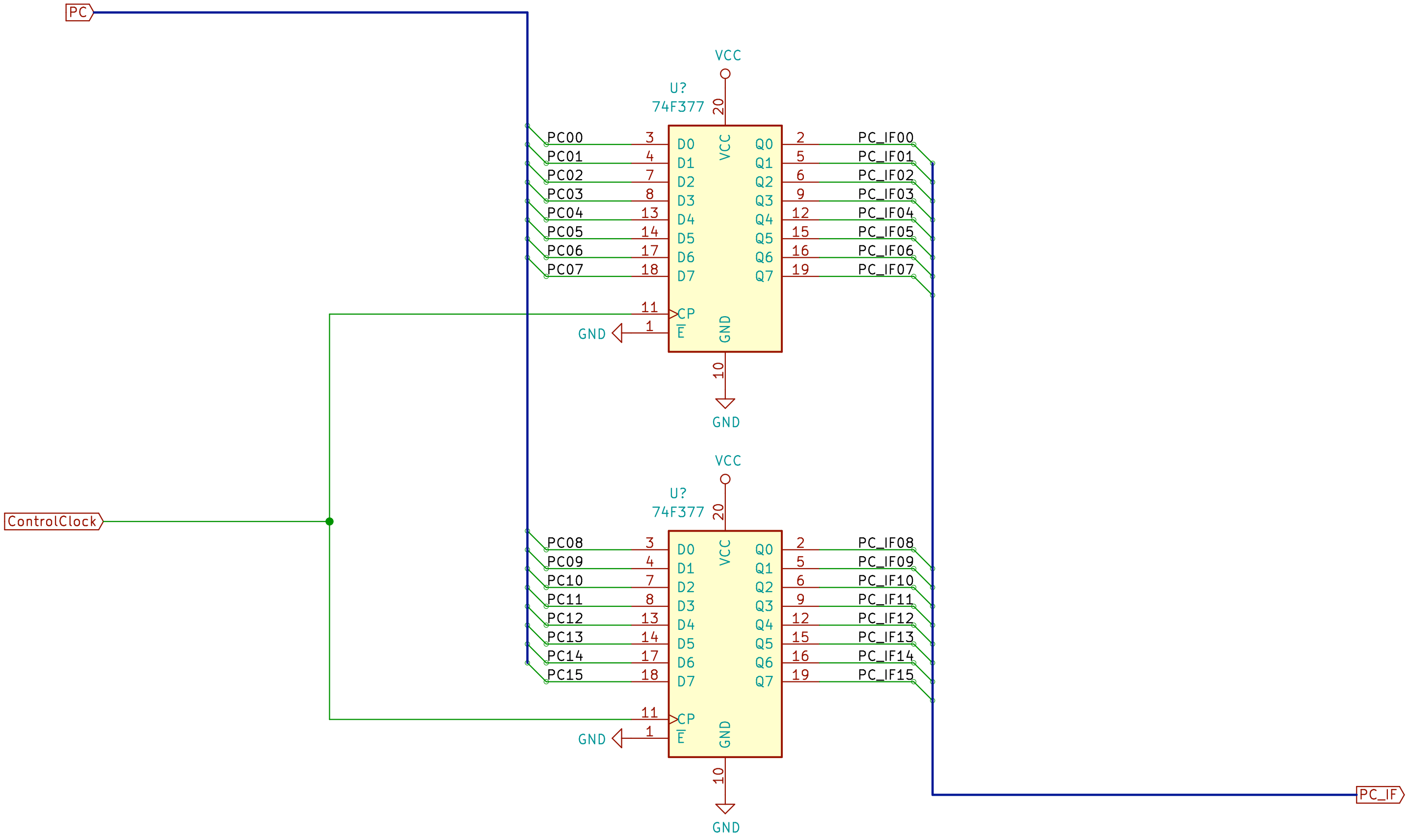
Sheet: Instruction Register
File: Instruction Register.sch

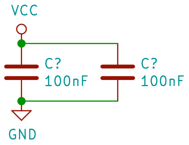
Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

Title: Instruction Fetch

Size: A4 Date: **Rev:**
KiCad E.D.A. kicad (5.1.0-0) Id: 8/24



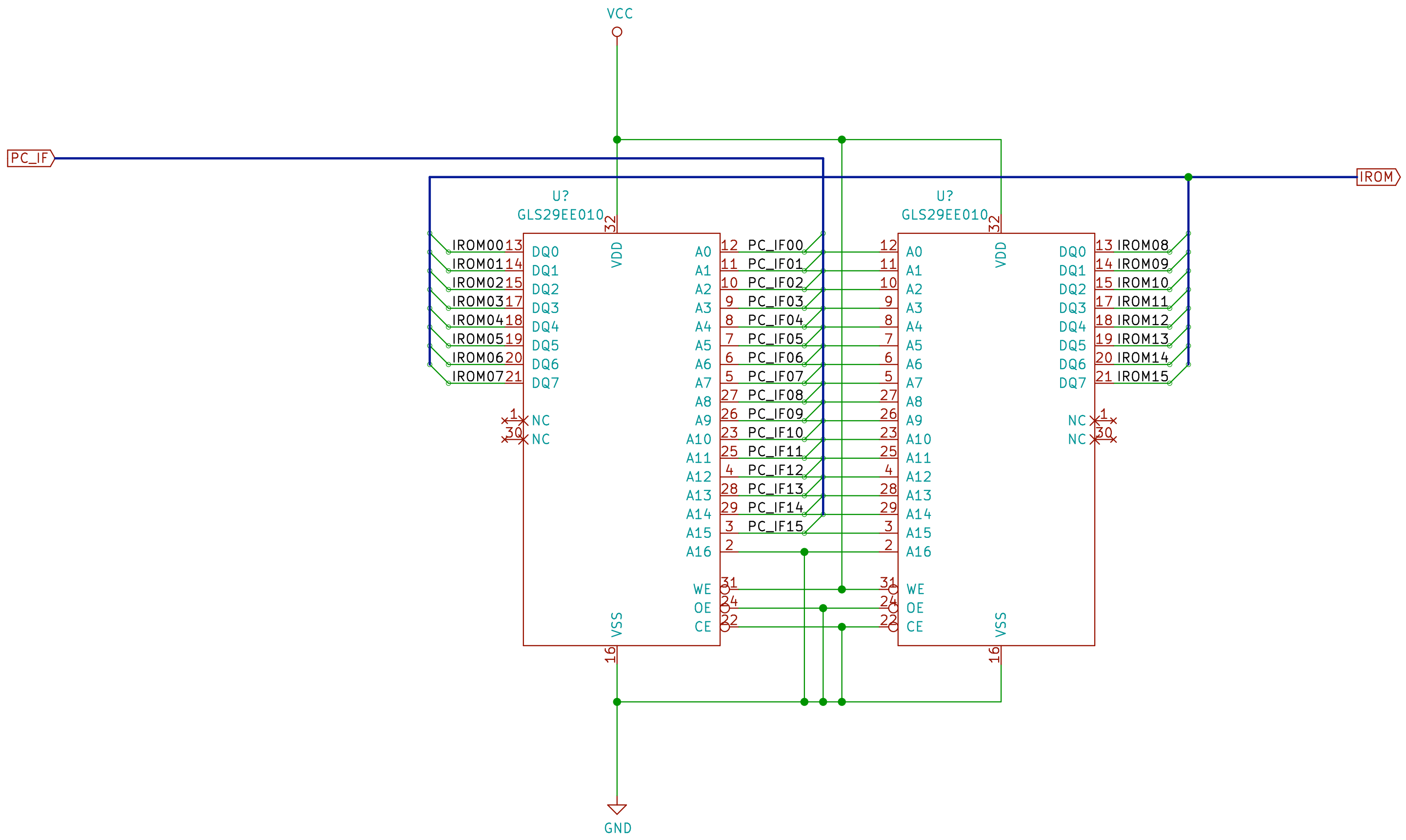


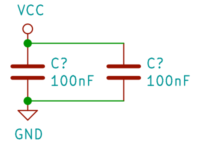
The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /Instruction Fetch/PC/IF/
File: PC_IF.sch

Title: PC/IF

Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 9/24



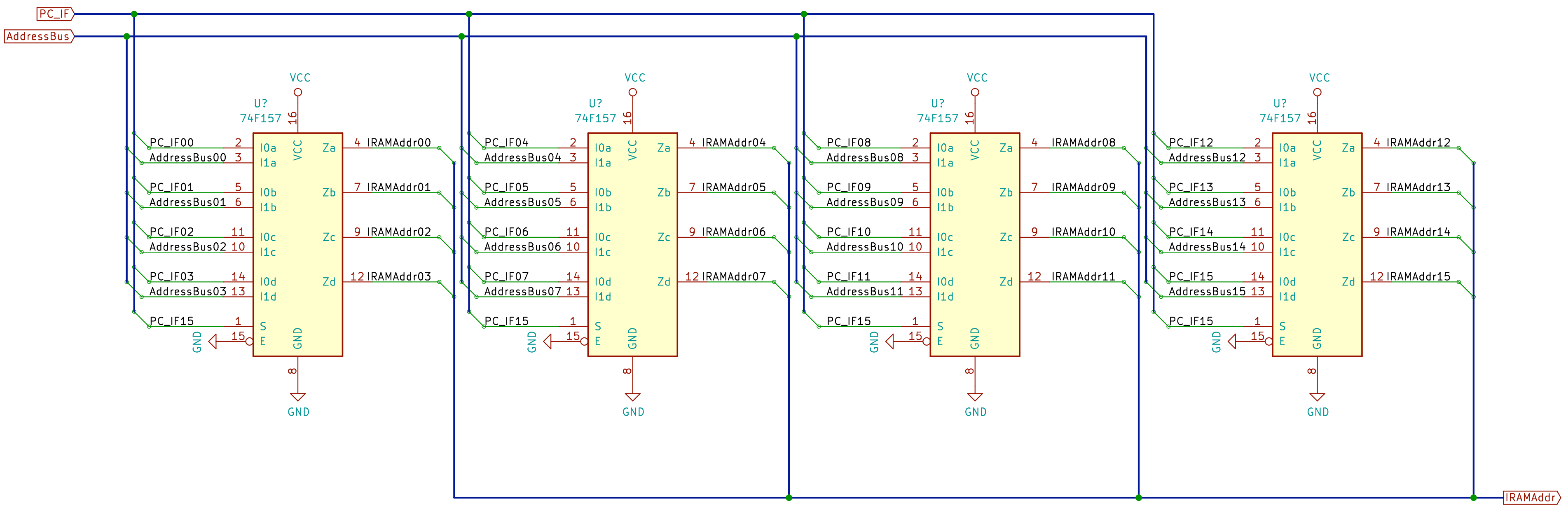


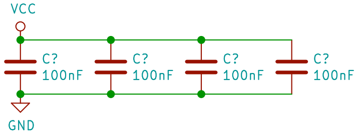
16-bit instructions are read from ROM at the address specified by the Program Counter.

Sheet: /Instruction Fetch/Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 10/24



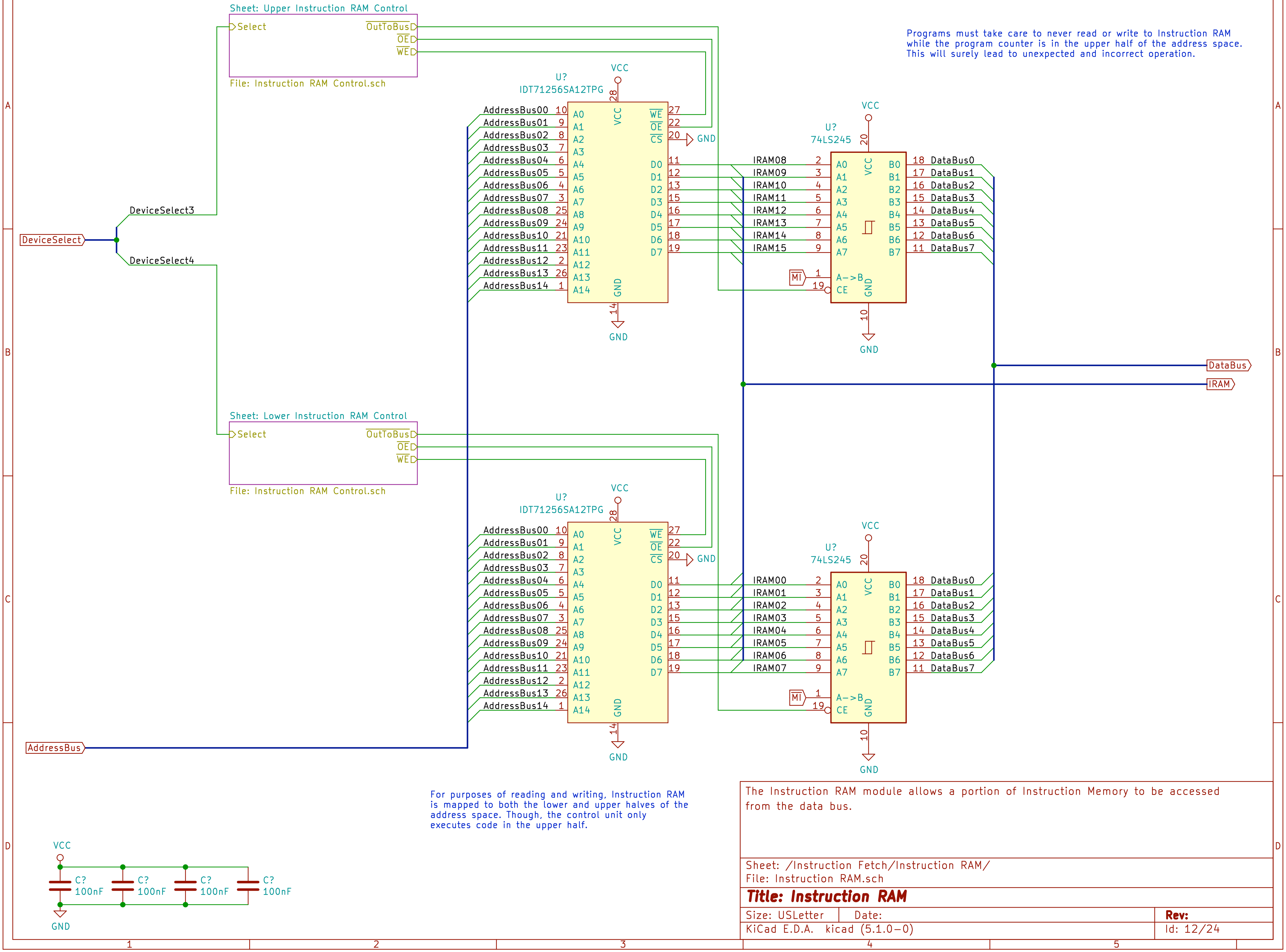


Instruction RAM uses an address from either the program counter or the address bus.
If the program counter is in the upper 32KB of the address space then use the program counter as we're running in Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM Address/
File: Instruction RAM Address.sch

Title: Instruction RAM Address

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 11/24



Programs must take care to never read or write to Instruction RAM while the program counter is in the upper half of the address space. This will surely lead to unexpected and incorrect operation.

For purposes of reading and writing, Instruction RAM is mapped to both the lower and upper halves of the address space. Though, the control unit only executes code in the upper half.

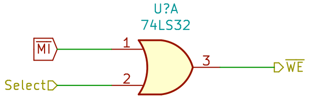
The Instruction RAM module allows a portion of Instruction Memory to be accessed from the data bus.

Sheet: /Instruction Fetch/Instruction RAM/
File: Instruction RAM.sch

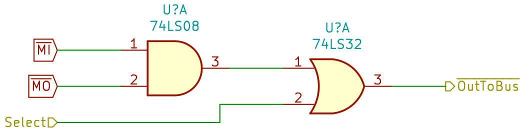
Title: Instruction RAM

Size: USLetter | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.0-0) | Id: 12/24

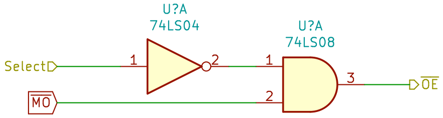


Only write to the Instruction SRAM when the MI signal is active and the appropriate plane of Instruction RAM is selected.



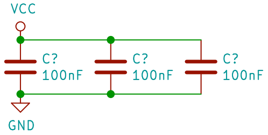
The bus transceiver should connect the Instruction SRAM to the Data Bus when the plane is selected and wither MO or MI is active.

The direction of the bus transceiver must also be set appropriately. This is done elsewhere.



Always output from Instruction SRAM when the plane of Instruction RAM is deselected. This allows RAM to be read for use in IF.

Else, if the plane is selected then only read from SRAM when the MO signal is active.

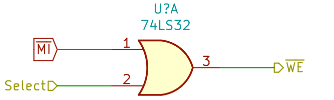


Logic for the control signals which drive Instruction RAM.

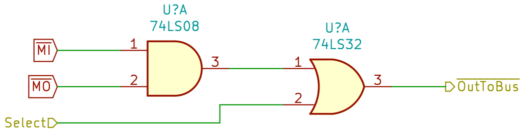
Sheet: /Instruction Fetch/Instruction RAM/Lower Instruction RAM Control/
File: Instruction RAM Control.sch

Title: Instruction RAM Control Logic

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 13/24

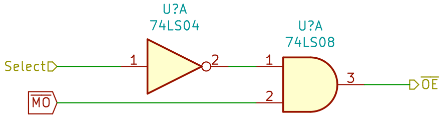


Only write to the Instruction SRAM when
the MI signal is active and the appropriate
plane of Instruction RAM is selected.



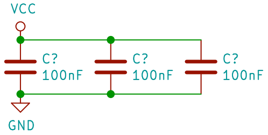
The bus transceiver should connect the
Instruction SRAM to the Data Bus when
the plane is selected and wither MO or MI
is active.

The direction of the bus transceiver must
also be set appropriately. This is done
elsewhere.



Always output from Instruction SRAM when
the plane of Instruction RAM is deselected.
This allows RAM to be read for use in IF.

Else, if the plane is selected then only read
from SRAM when the MO signal is active.



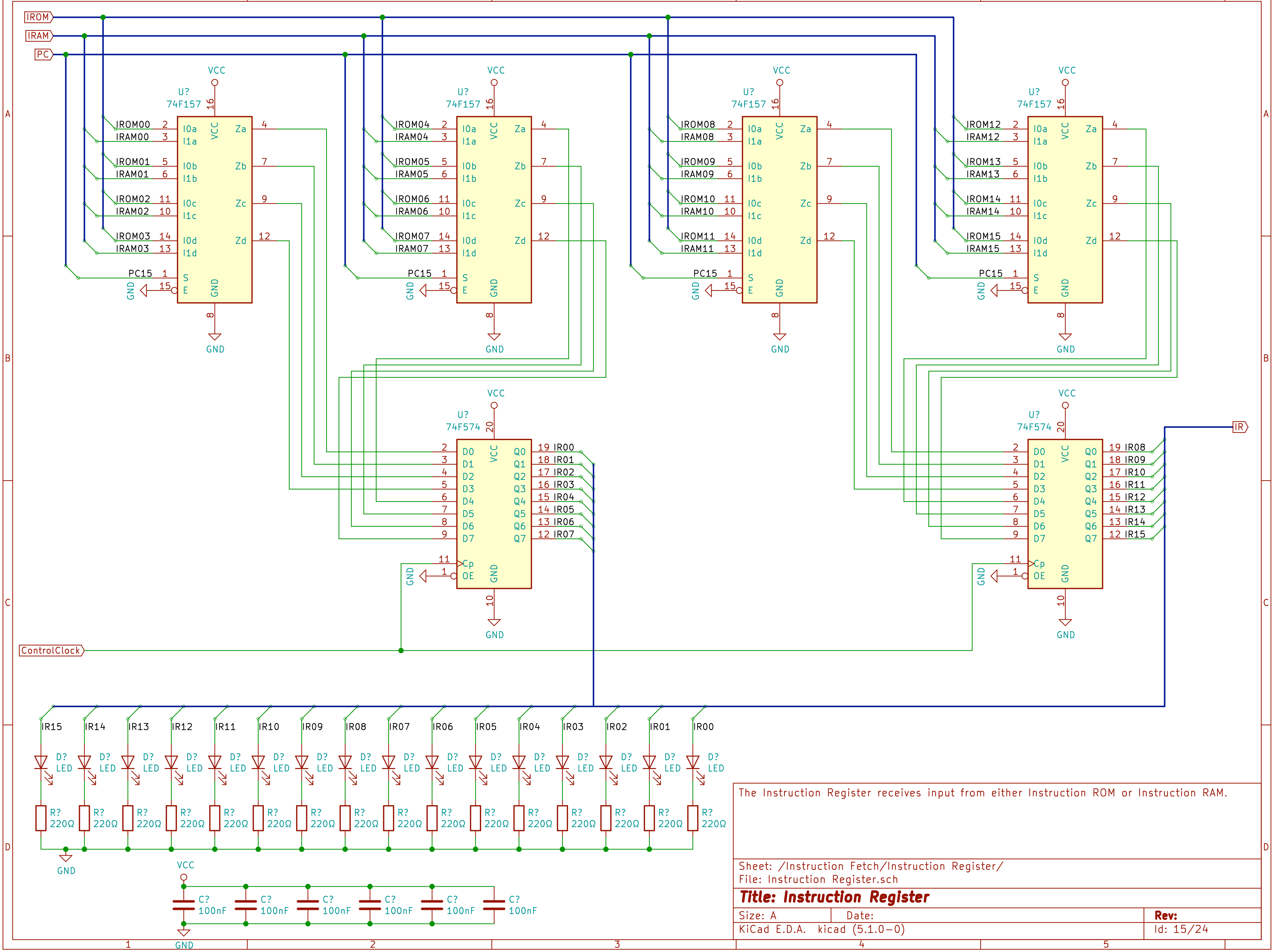
Logic for the control signals which drive Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM/Upper Instruction RAM Control/
File: Instruction RAM Control.sch

Title: Instruction RAM Control Logic

Size: A4 Date: **Rev:**

KiCad E.D.A. kicad (5.1.0-0) Id: 14/24

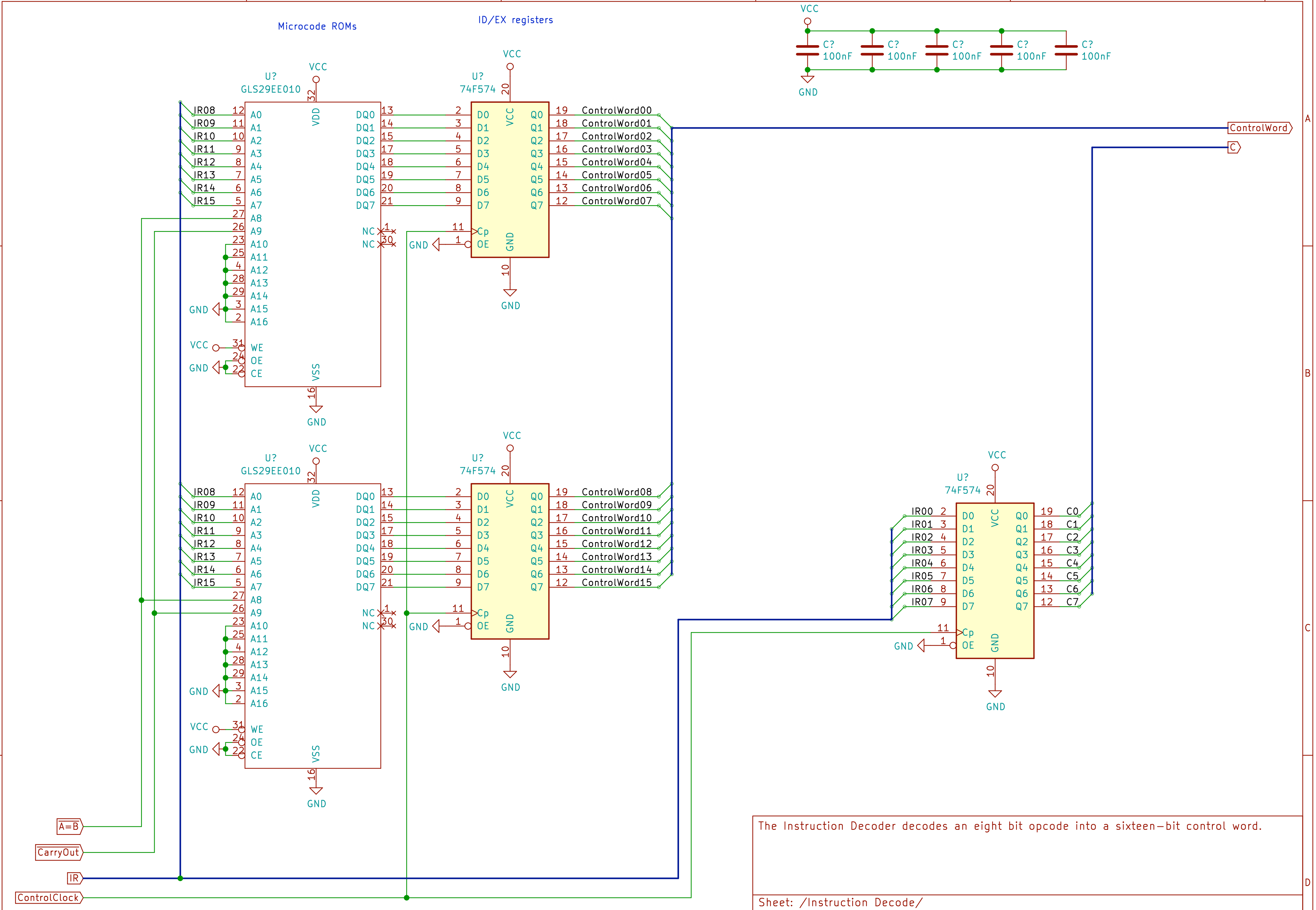


The Instruction Register receives input from either Instruction ROM or Instruction RAM.

Sheet: /Instruction Fetch/Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 15/24

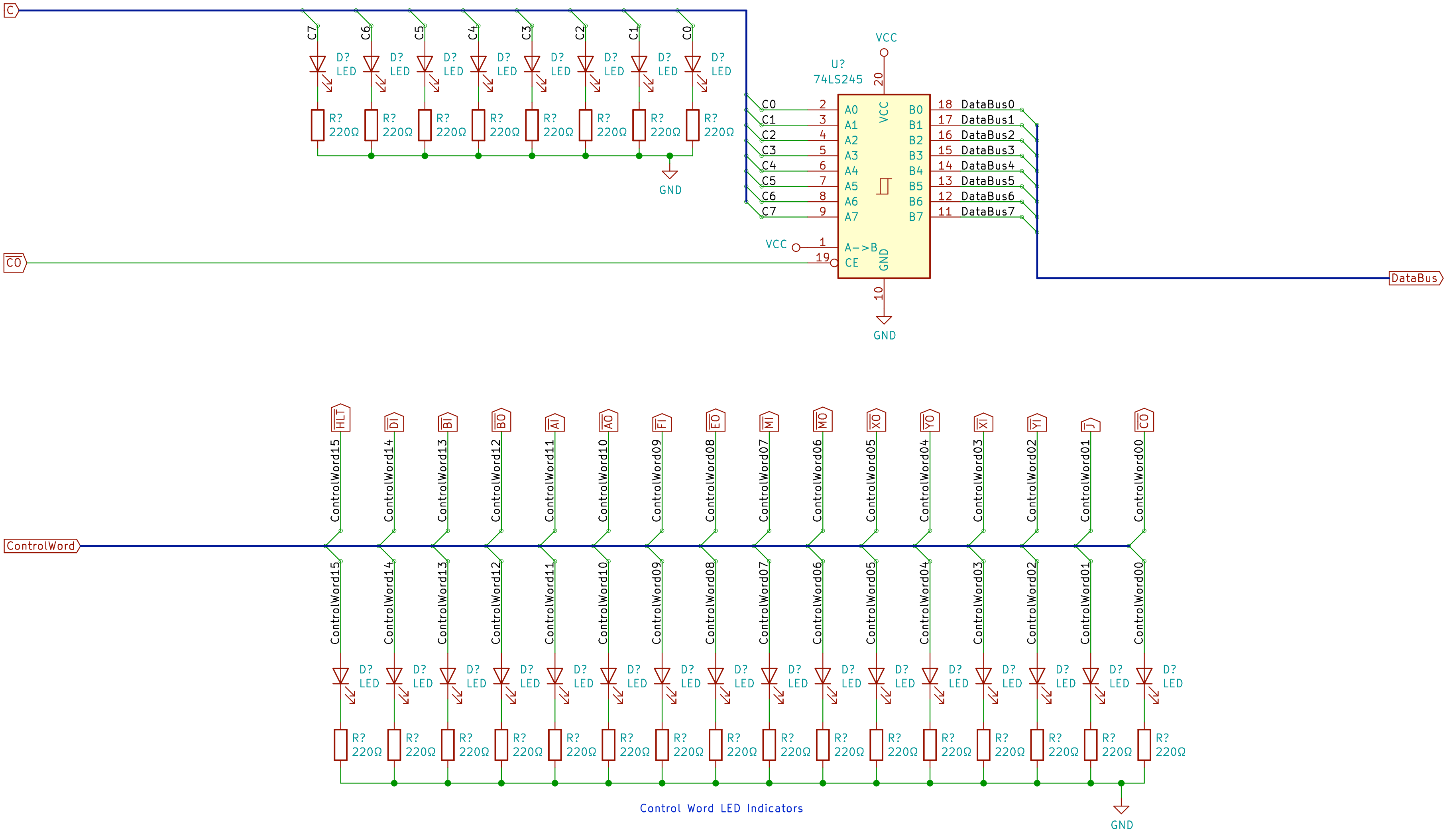


The Instruction Decoder decodes an eight bit opcode into a sixteen-bit control word.

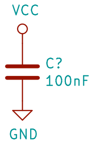
Sheet: /Instruction Decode/
File: Instruction Decode.sch

Title: Instruction Decode

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 16/24



Control Word LED Indicators

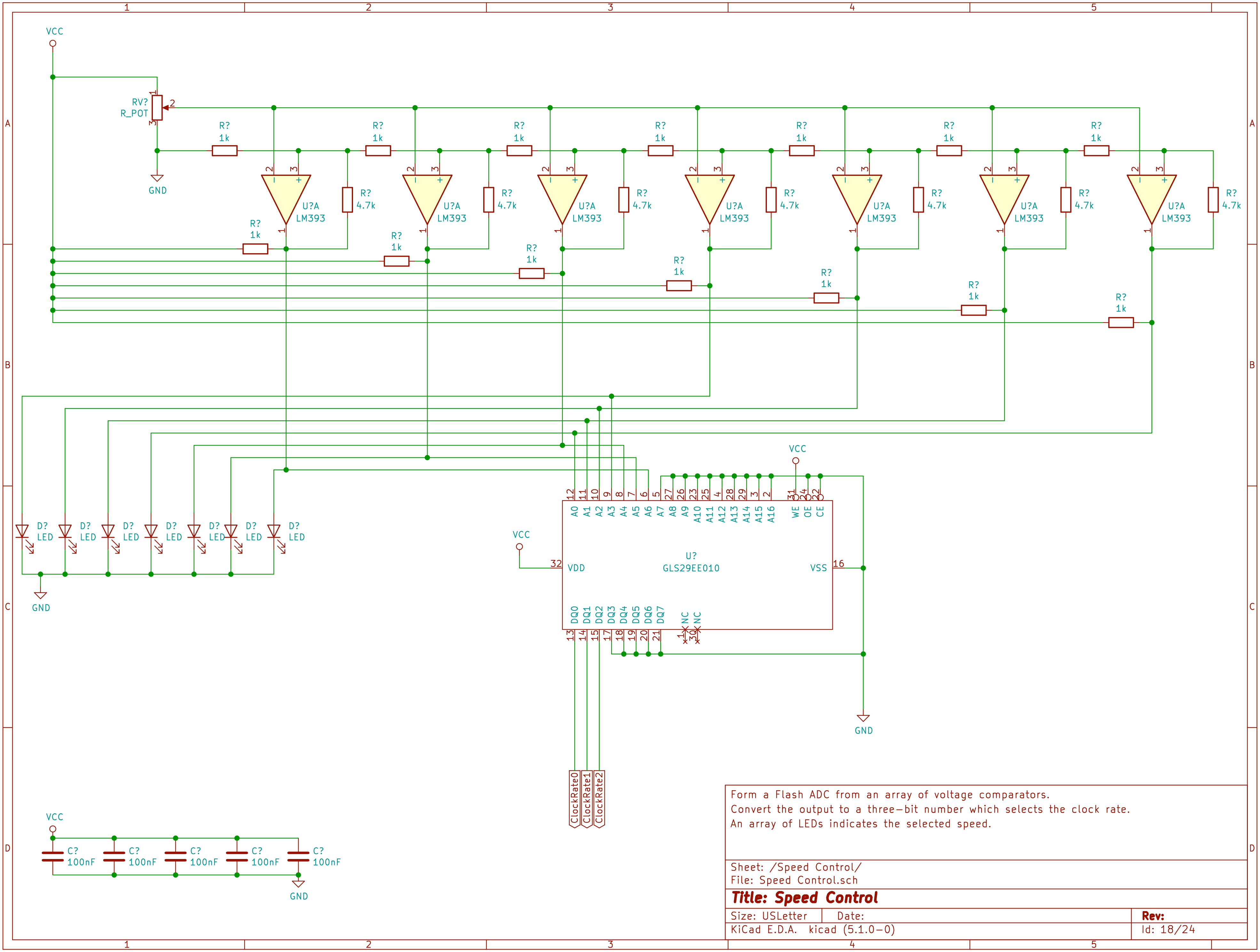


The lower eight bits of the instruction register can be expressed onto the data bus as a constant value.

Sheet: /Execute/
File: Execute.sch

Title: Execute

Size: A   Date: **Rev:**
KiCad E.D.A. kicad (5.1.0-0)   Id: 17/24

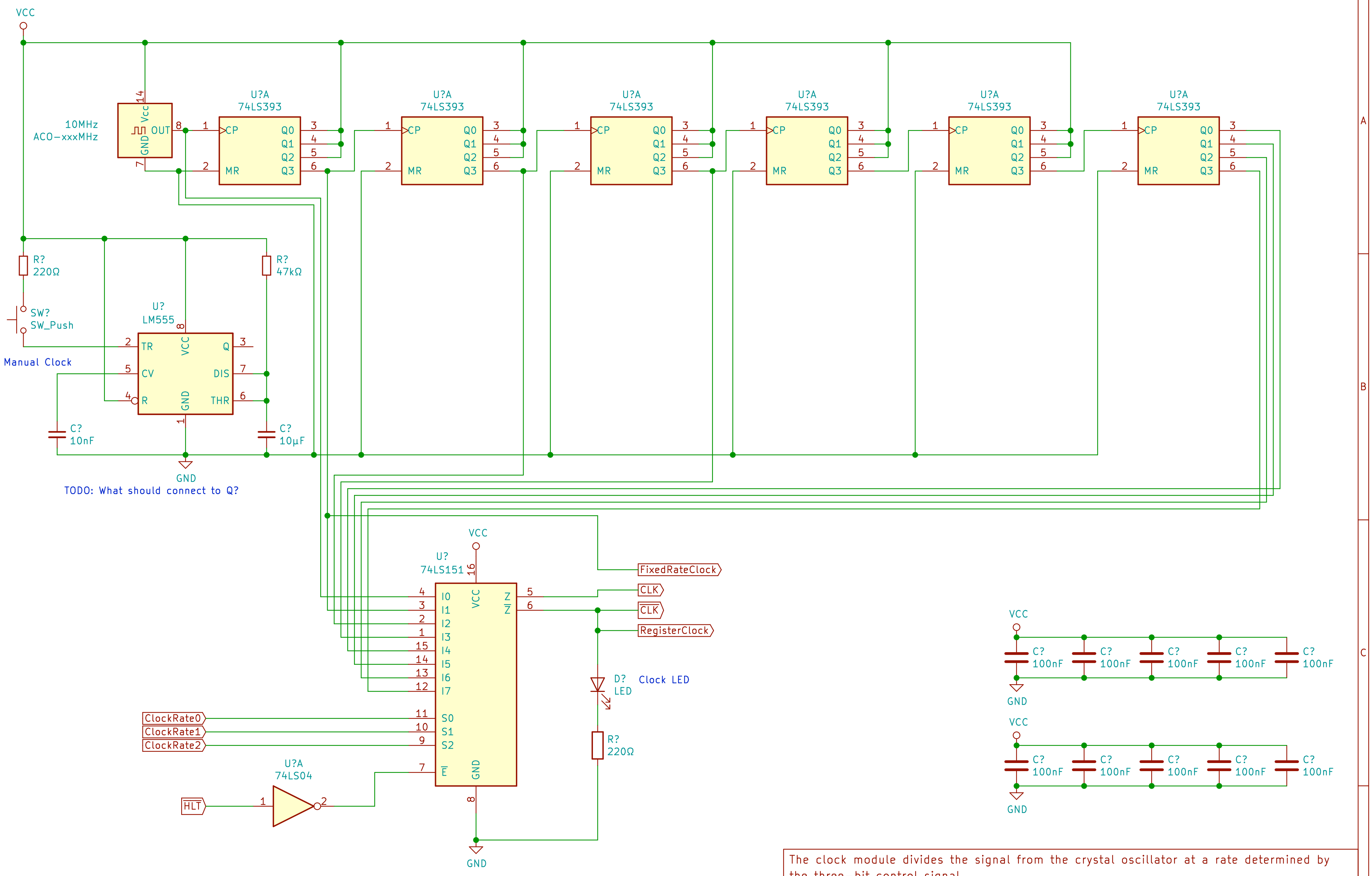


Form a Flash ADC from an array of voltage comparators.
Convert the output to a three-bit number which selects the clock rate.
An array of LEDs indicates the selected speed.

Sheet: /Speed Control/
File: Speed Control.sch

Title: Speed Control

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 18/24



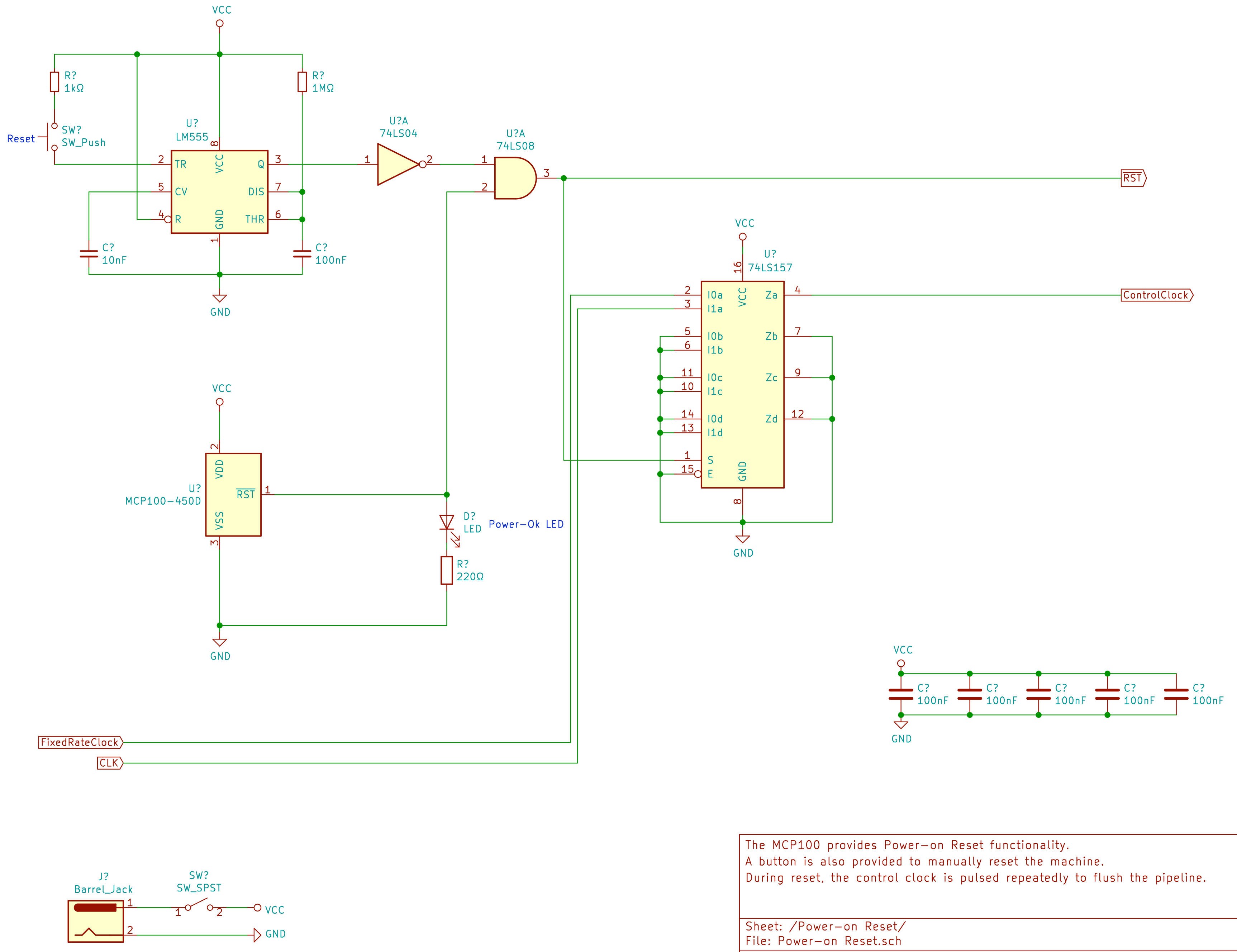
The clock module divides the signal from the crystal oscillator at a rate determined by the three-bit control signal.

Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: A Date: **Rev:**

KiCad E.D.A. kicad (5.1.0-0) Id: 19/24

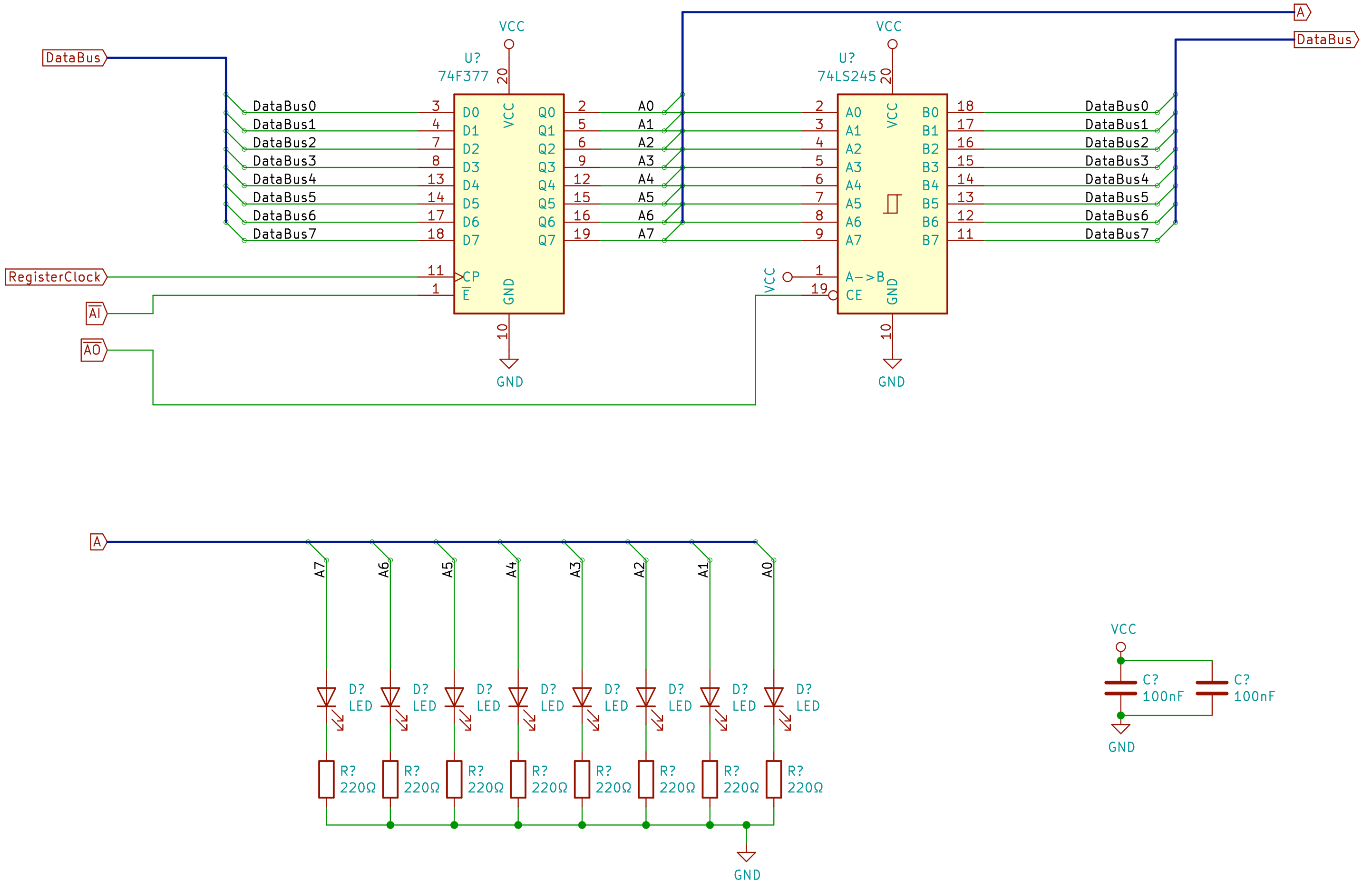


The MCP100 provides Power−on Reset functionality.
A button is also provided to manually reset the machine.
During reset, the control clock is pulsed repeatedly to flush the pipeline.

Sheet: /Power−on Reset/
File: Power−on Reset.sch

Title: Power−on Reset

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0−0)		Id: 20/24

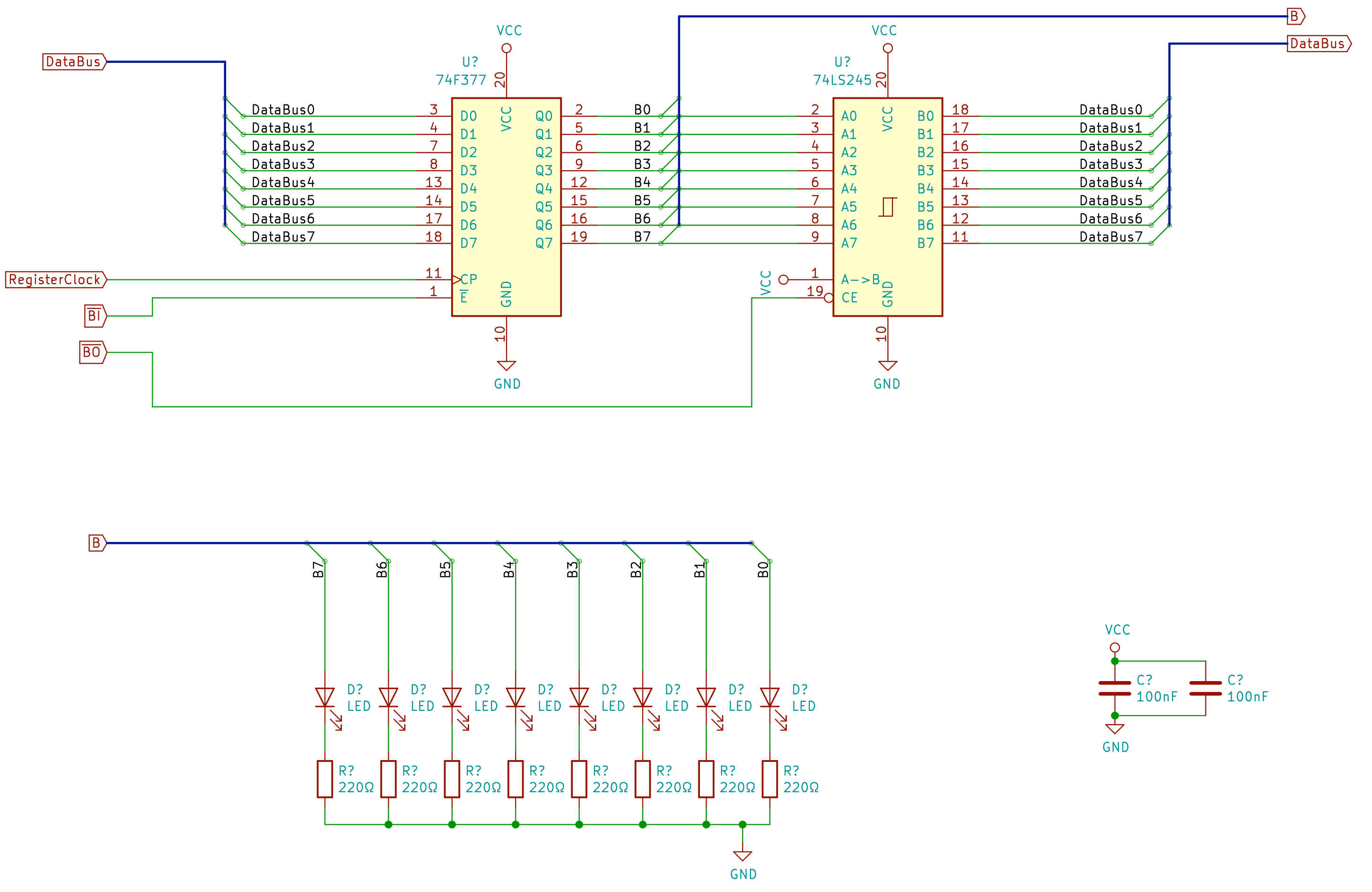


Register A is wired to the ALU's A operand.

Sheet: /Register A/
File: Register A.sch

Title: Register A

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 21/24

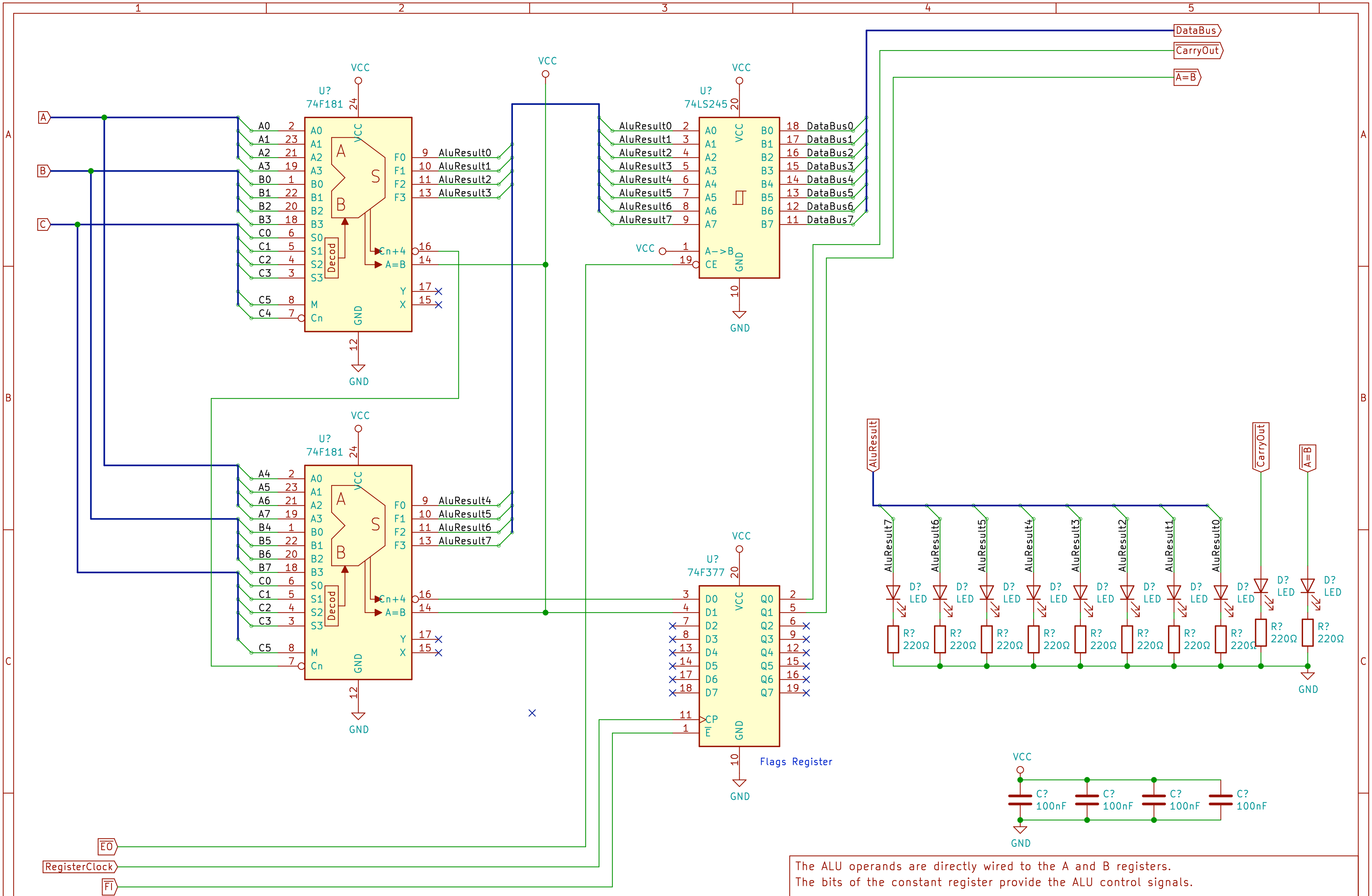


Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

Title: Register B

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 22/24

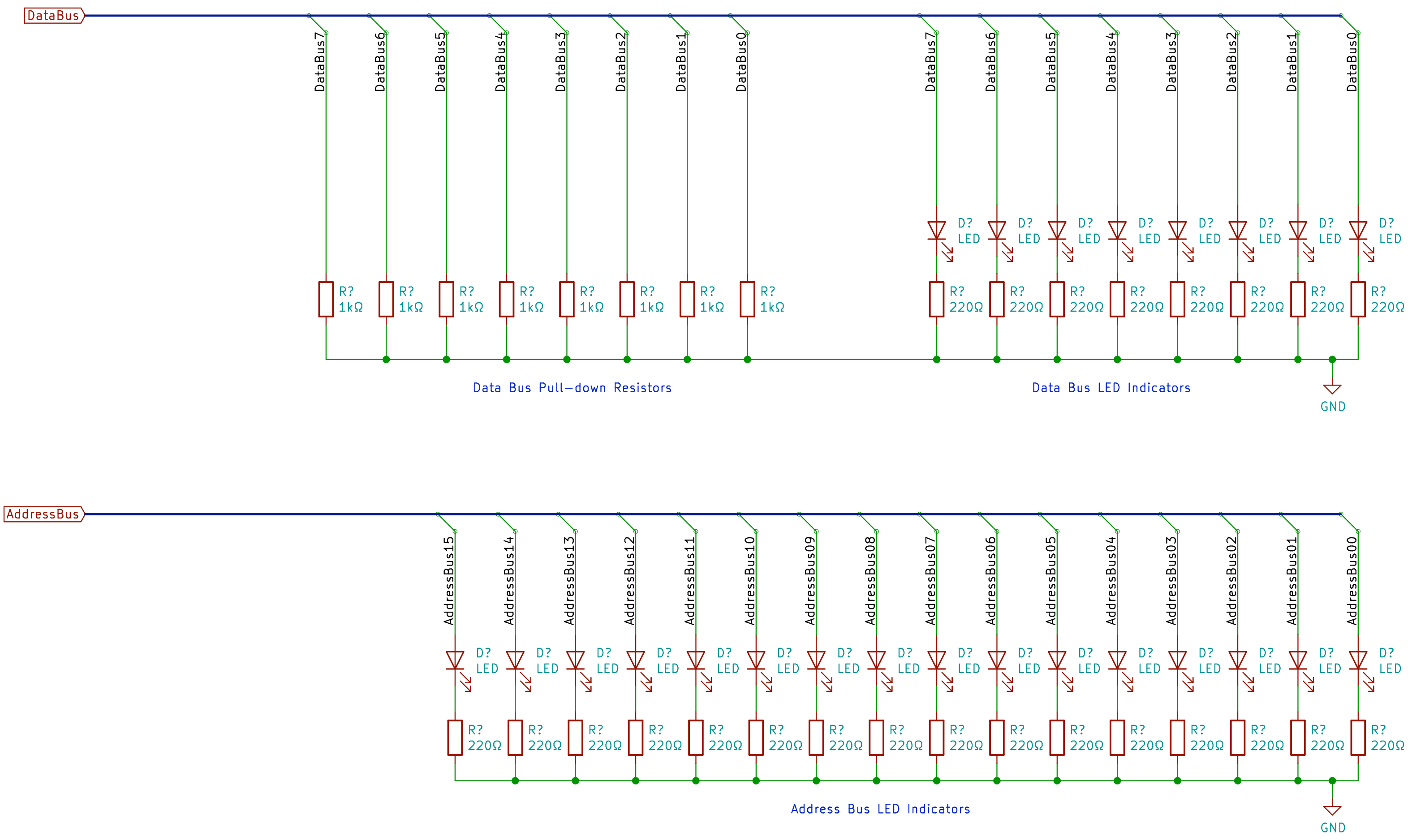


The ALU operands are directly wired to the A and B registers.
The bits of the constant register provide the ALU control signals.

Sheet: /ALU/
File: ALU.sch

Title: ALU

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 23/24



Sheet: /Bus Display/
File: Bus Display.sch

Title: Bus Display

Size: A Date: **Rev:**
KiCad E.D.A. kicad (5.1.0−0) Id: 24/24