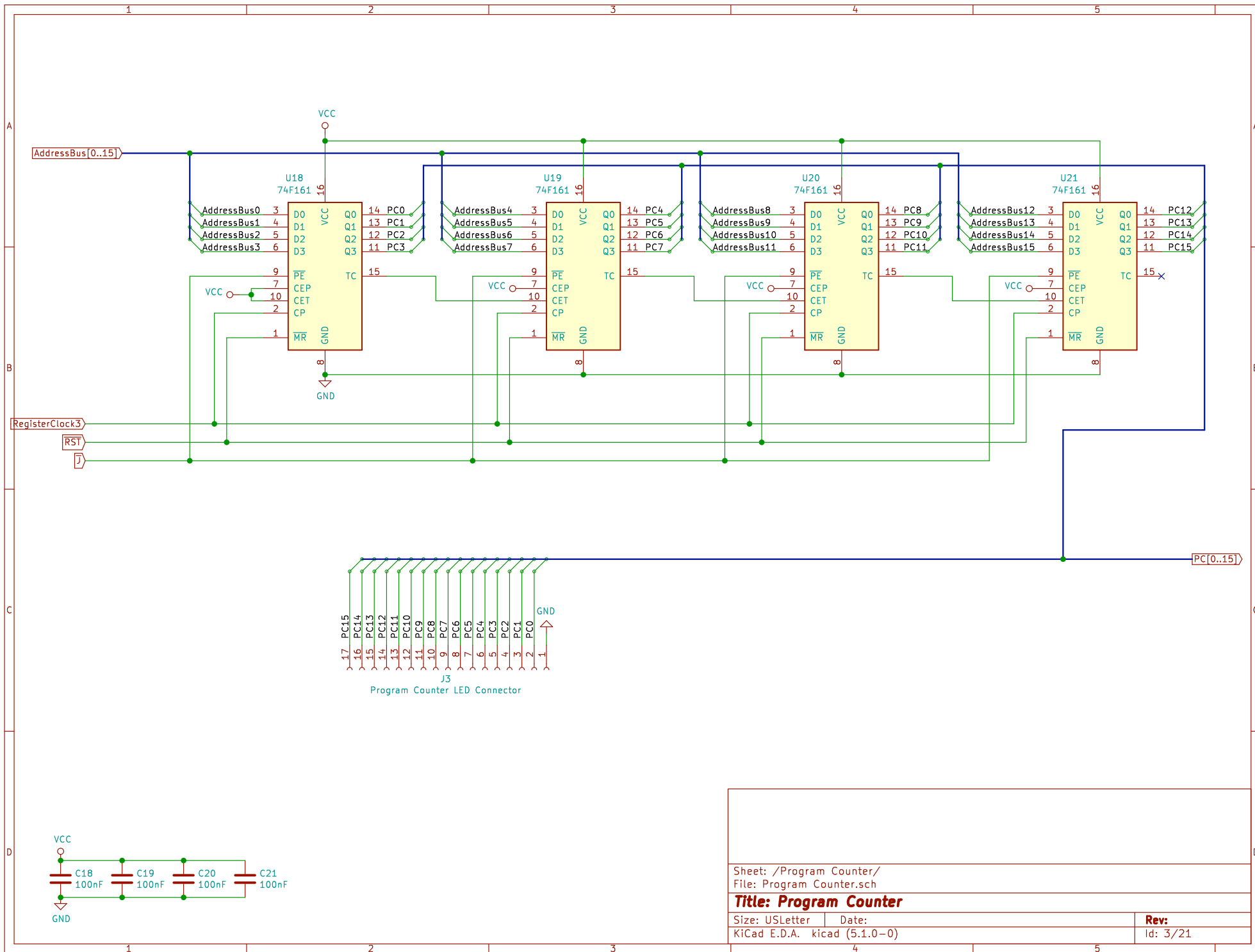


Register D controls the device select lines for peripherals and memory.		
Sheet: /Register D/ File: Register D.sch		
Title: Register D		
Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 2/21



Sheet: /Program Counter/
File: Program Counter.sch

Title: Program Counter

Size: USLetter Date:
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1	2	3	4	5	6
A					A
B					B
C					C
D					D
1	2	3	4	5	6

Sheet: PC/IF



File: PC_IF.sch

Sheet: Instruction ROM



File: Instruction ROM.sch

Sheet: Instruction RAM



File: Instruction RAM.sch

Sheet: Instruction Register



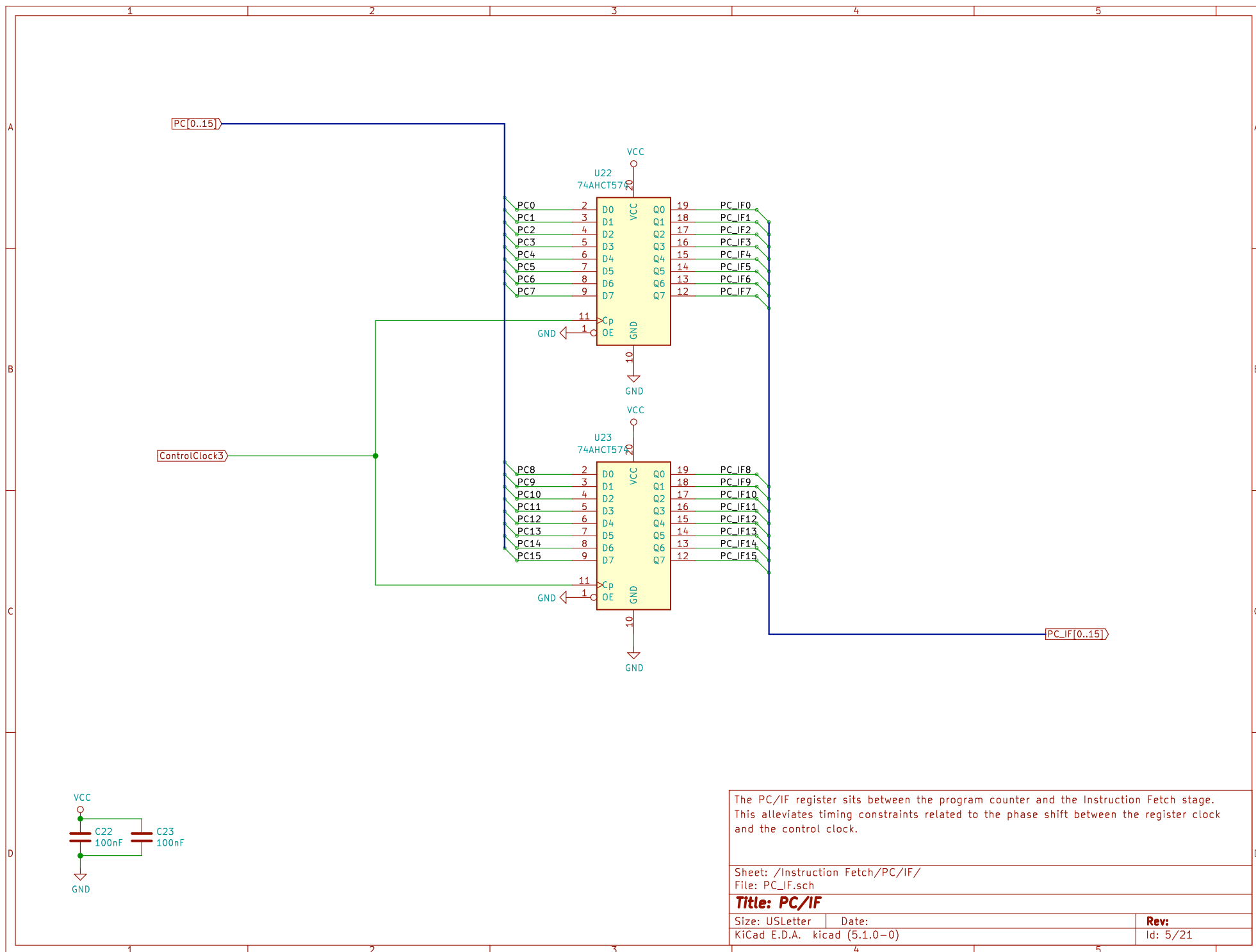
File: Instruction Register.sch

Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

Title: Instruction Fetch

Size: A4	Date:	Rev:
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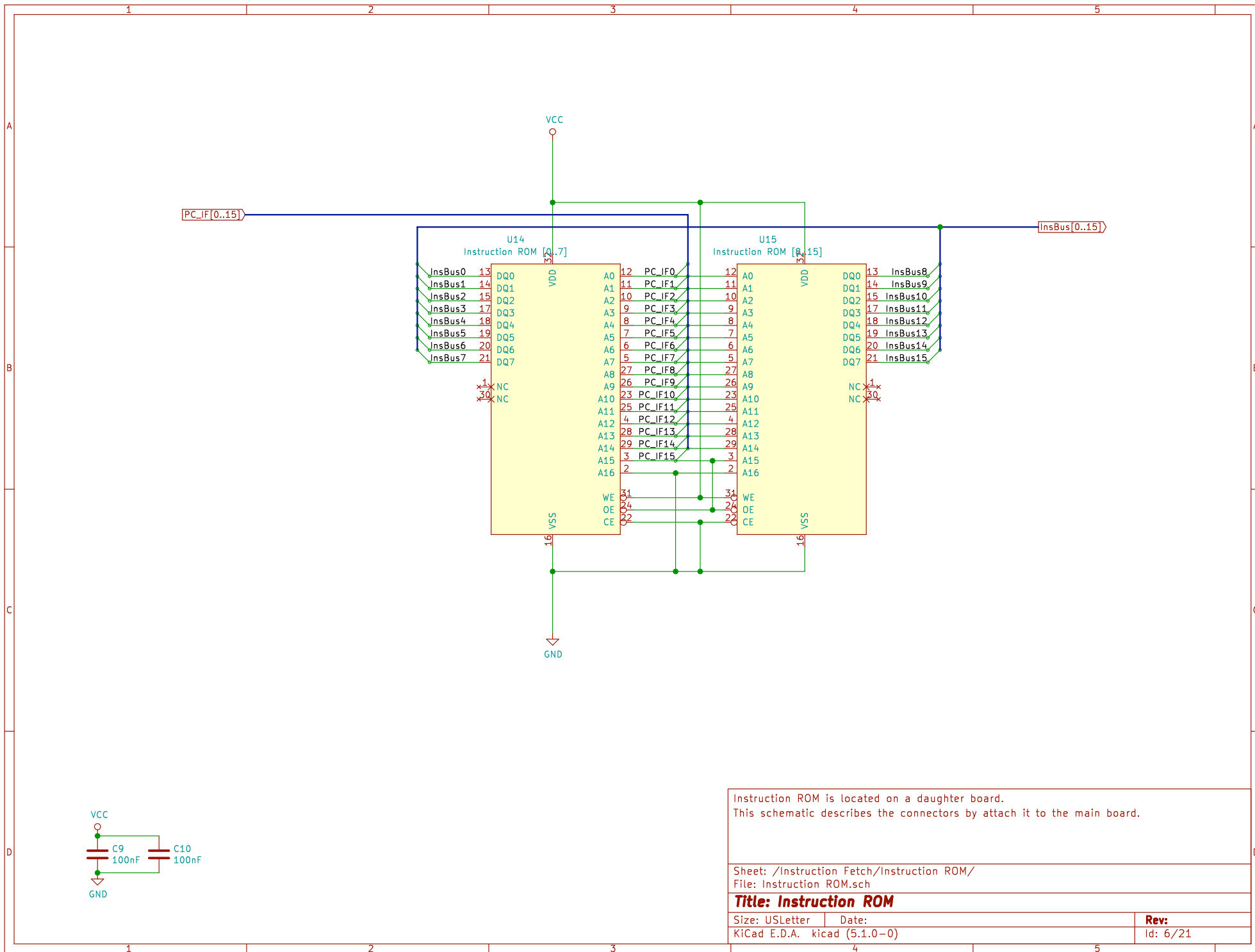
The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /Instruction Fetch/PC/IF/
File: PC_IF.sch

Title: PC/IF

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
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Instruction ROM is located on a daughter board.
This schematic describes the connectors to attach it to the main board.

Sheet: /Instruction Fetch/Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

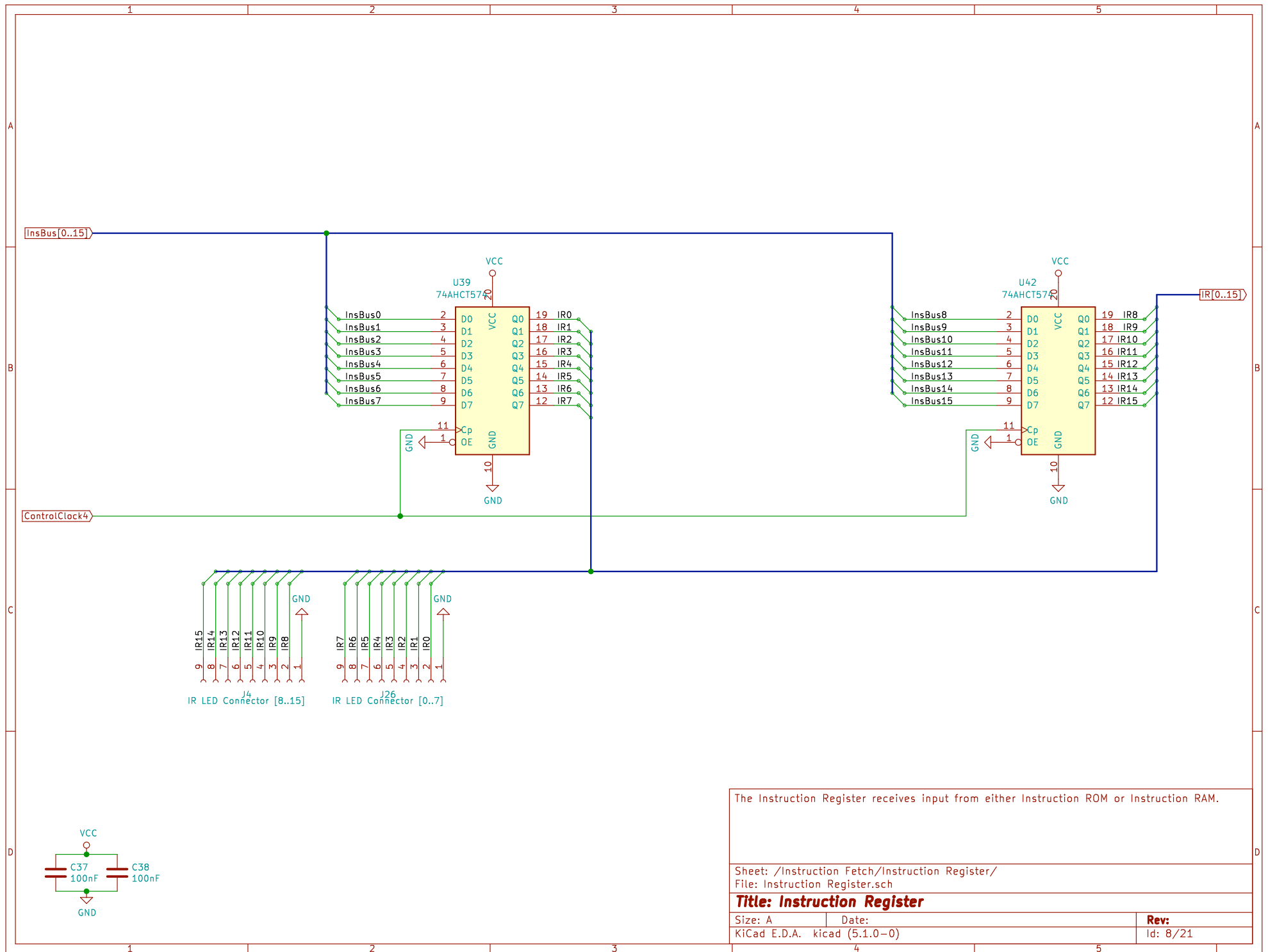
Size: USLetter

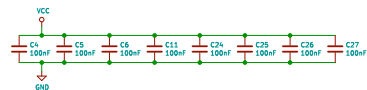
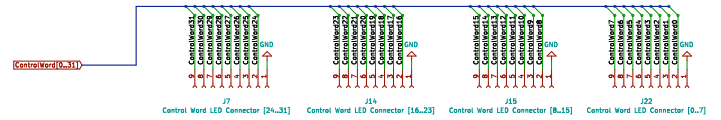
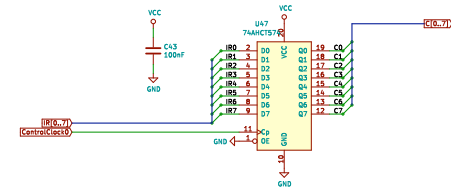
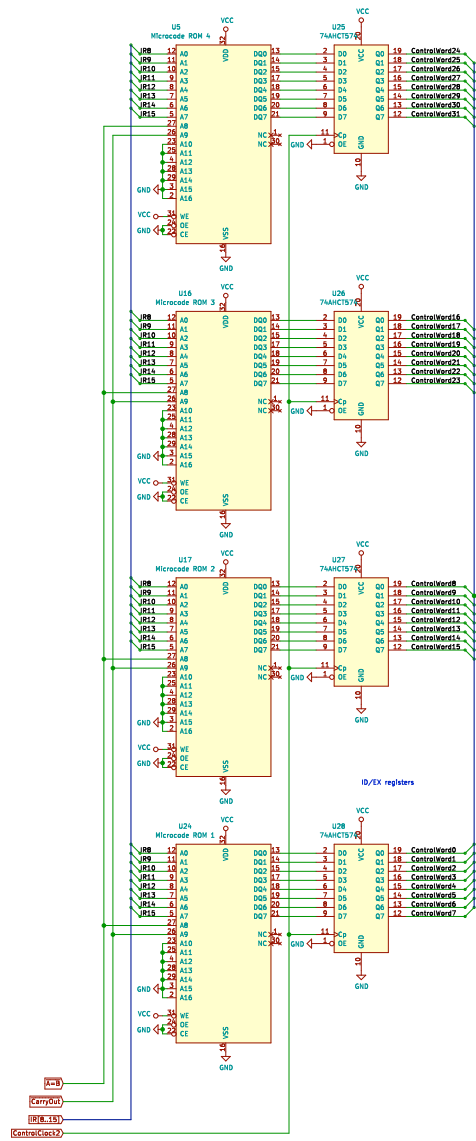
Date:

KiCad E.D.A. kicad (5.1.0-0)

Rev:

Id: 6/21





The Instruction Decoder decodes an eight bit opcode into a 32-bit control word.

Sheet: /Instruction Decoder/

File: Instruction Decoder.kicad

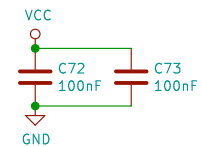
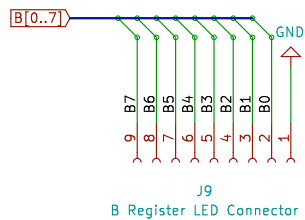
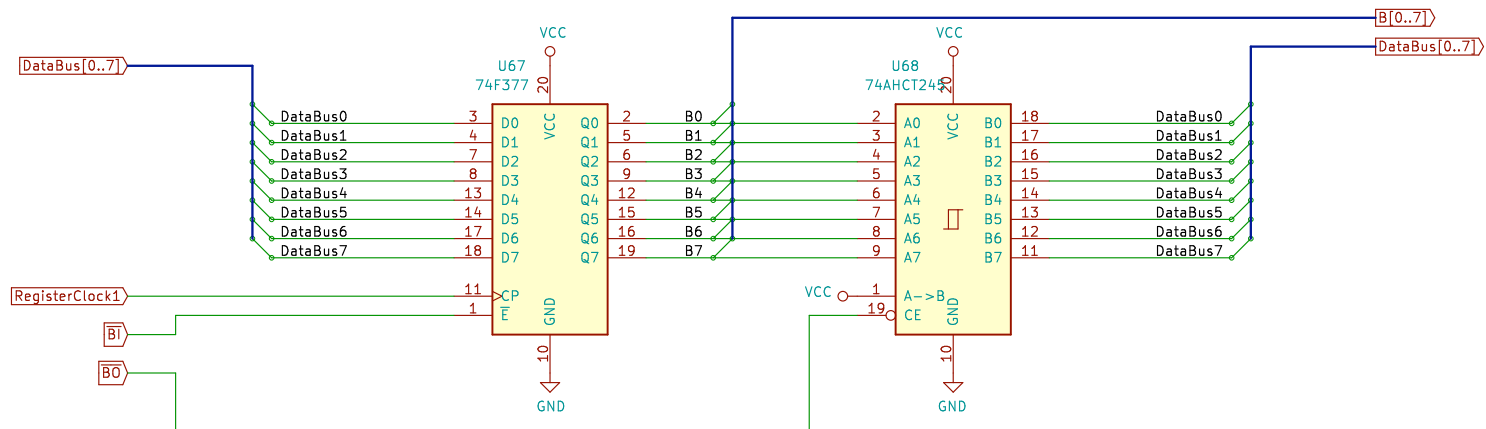
Title: Instruction Decode

Size: A2

KiCad E.D.A. KiCad (5.1.0-0)

Date: 16/9/21

Rev: 1



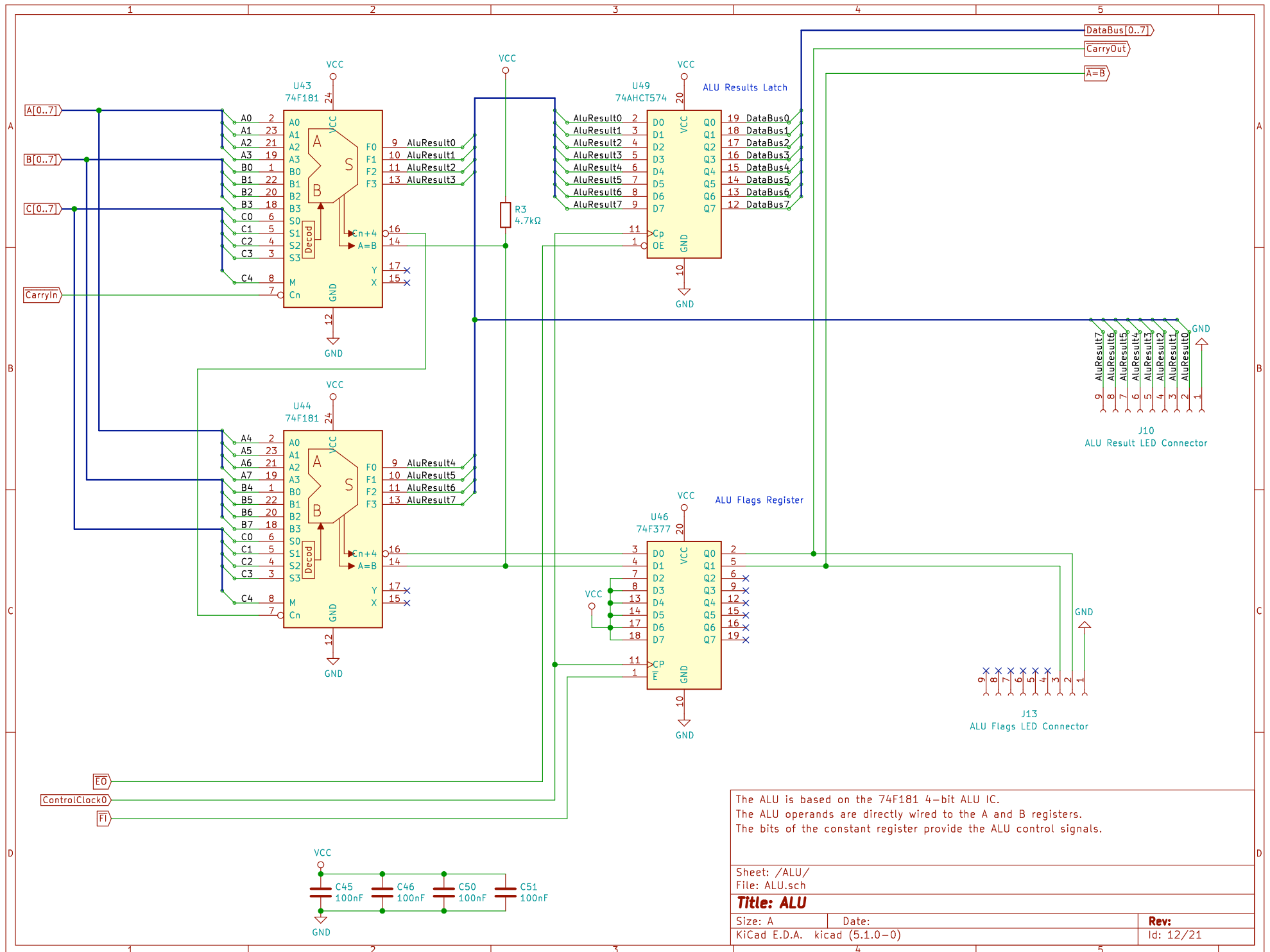
Register B is wired to the ALU's B operand.

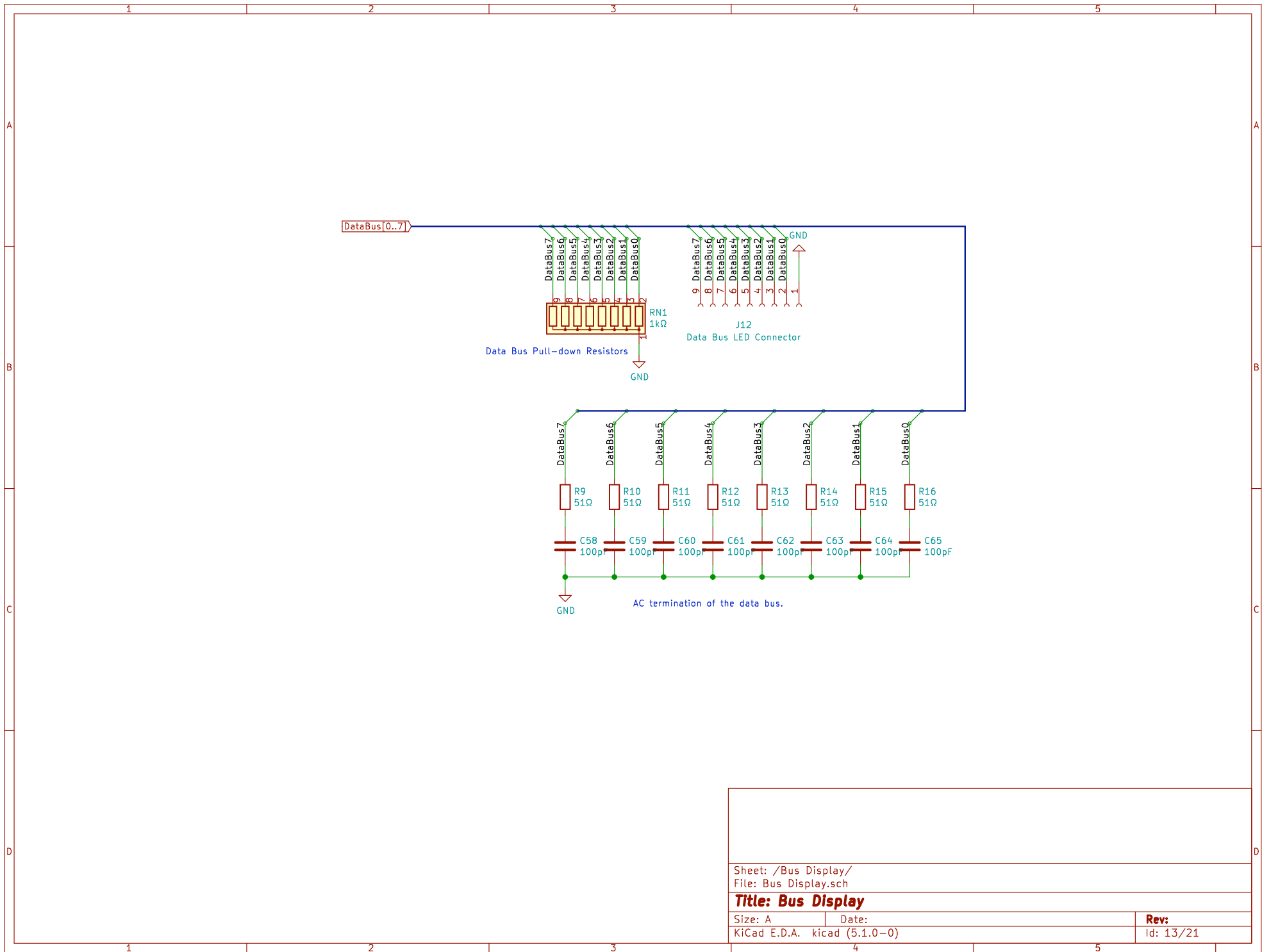
Sheet: /Register B/
File: Register B.sch

Title: Register B

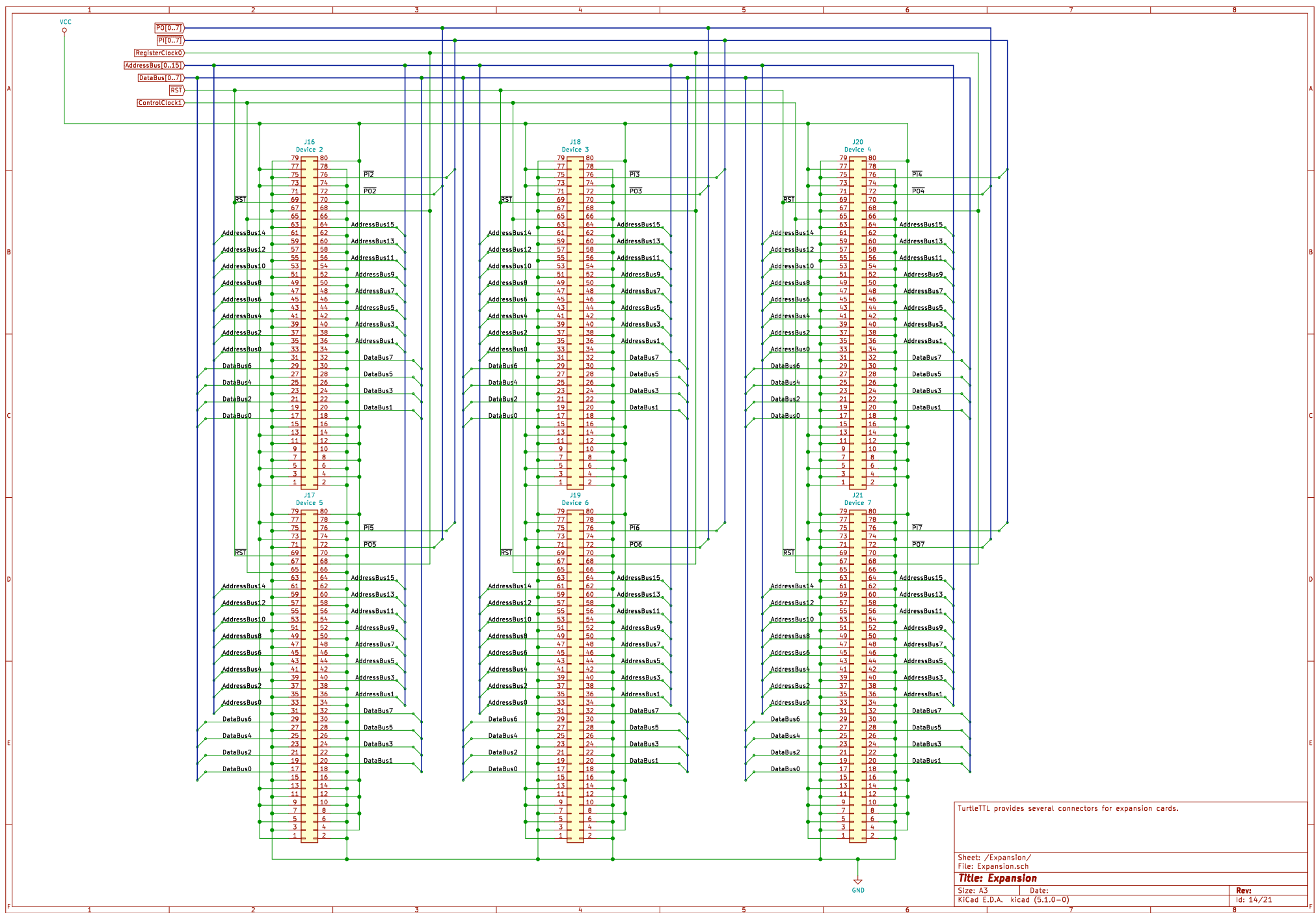
Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 11/21





Sheet: /Bus Display/ File: Bus Display.sch		
Title: Bus Display		
Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 13/21

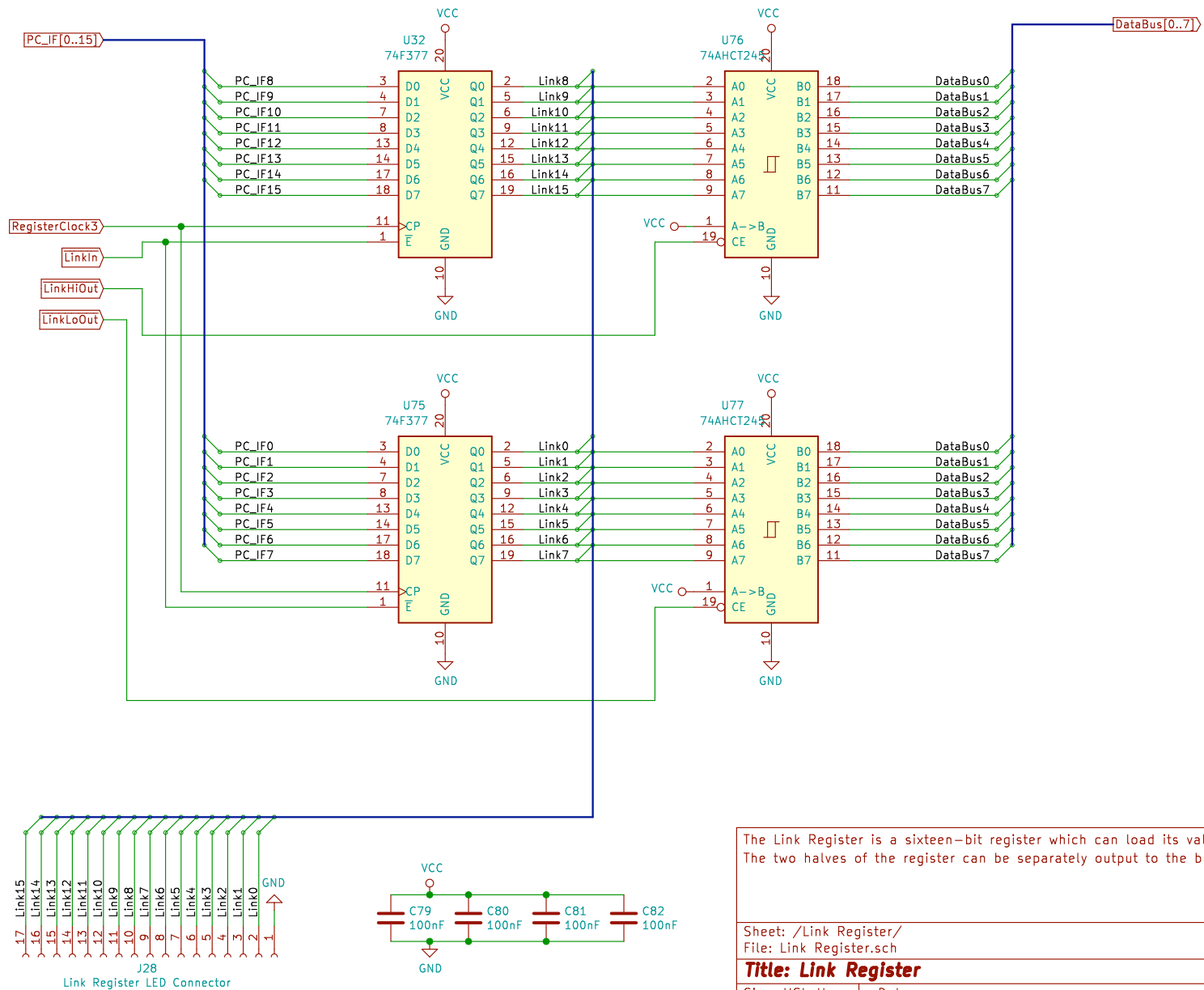


TurtleTTL provides several connectors for expansion cards.

Sheet: /Expansion/
File: Expansion.sch

Title: Expansion

Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 14/21



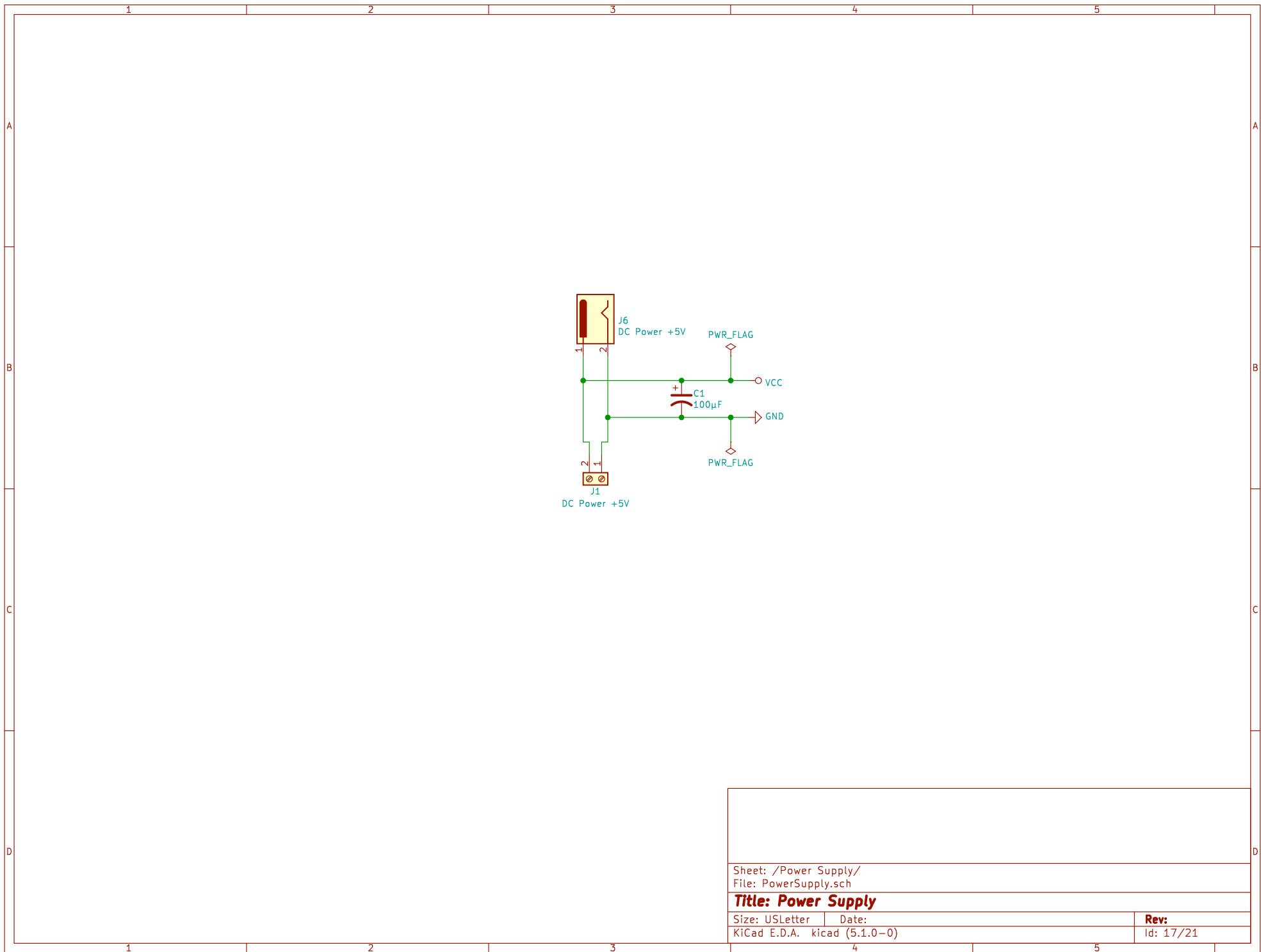
The Link Register is a sixteen-bit register which can load its value from PC. The two halves of the register can be separately output to the bus.

Sheet: /Link Register/
File: Link Register.sch

Title: Link Register

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 16/21



Sheet: /Power Supply/ File: PowerSupply.sch		
Title: Power Supply		
Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 17/21

