Sheet: Output Display

File: Output Display.sch

Sheet: Register XY

File: Register XY.sch

Sheet: Speed Control

File: Speed Control.sch

Sheet: Program Counter

File: Program Counter.sch

Sheet: Clock

File: Clock.sch

Sheet: PC/IF

File: PC_IF.sch

Sheet: Power-on Reset

File: Power-on Reset.sch

Sheet: Instruction RAM

File: Instruction RAM.sch

Sheet: Instruction ROM

File: Instruction ROM.sch

Sheet: Register A

File: Register A.sch

Sheet: Data RAM

File: Data RAM.sch

Sheet: Instruction Register

File: Instruction Register.sch

Sheet: Register B

File: Register B.sch

Sheet: Instruction Decoder

File: Instruction Decoder.sch

Sheet: ALU

File: ALU.sch

Sheet: Execute

File: Execute.sch

Sheet: Bus Display

File: Bus Display.sch

Sheet: Register D

File: Register D.sch

Sheet: Control Word Display

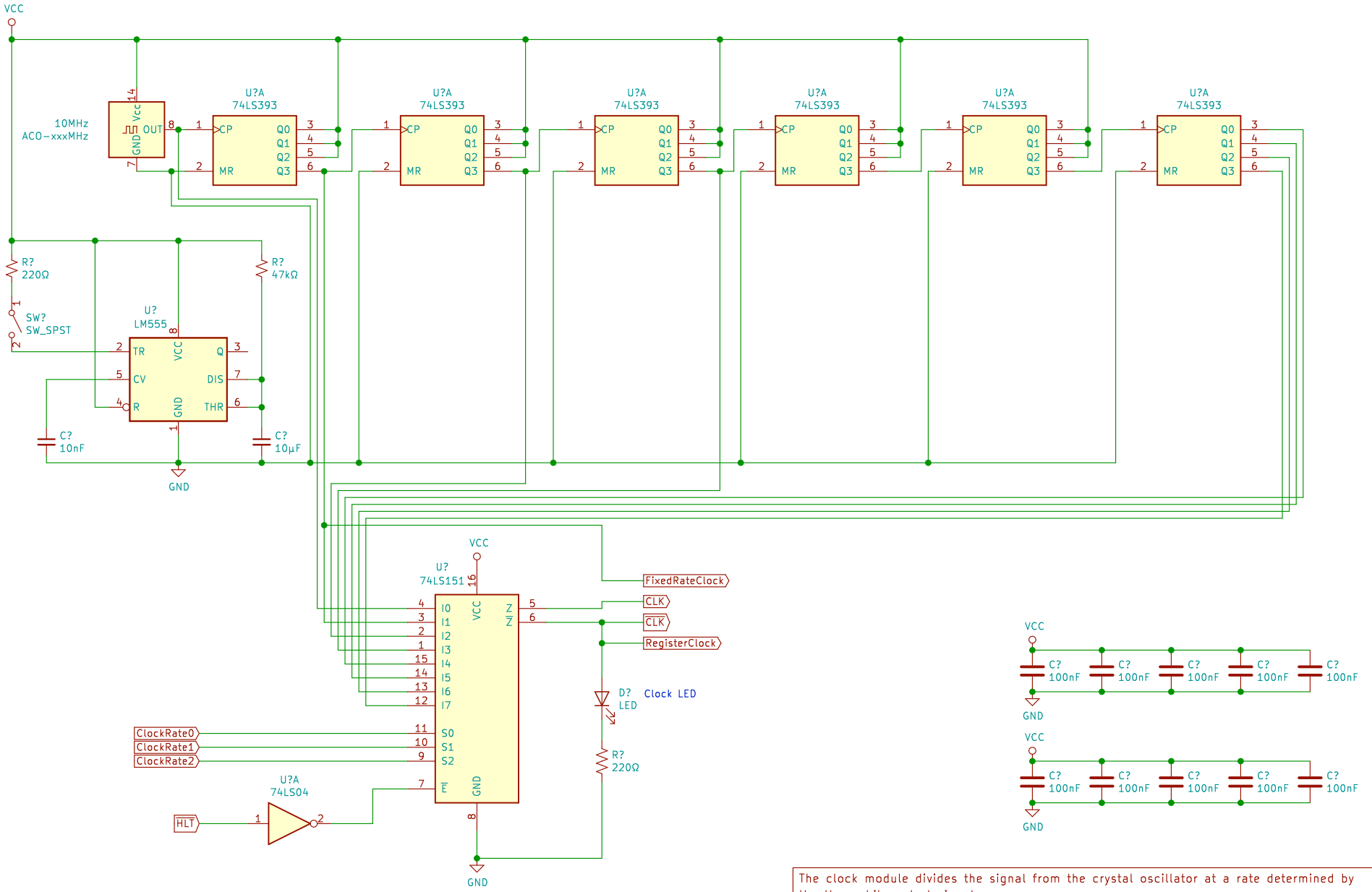
File: Control Word Display.sch

TTL microcomputer built from 74xx series logic chips.

Sheet: /
File: TurtleTTL.sch

Title: Turtle TTL

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 1/20



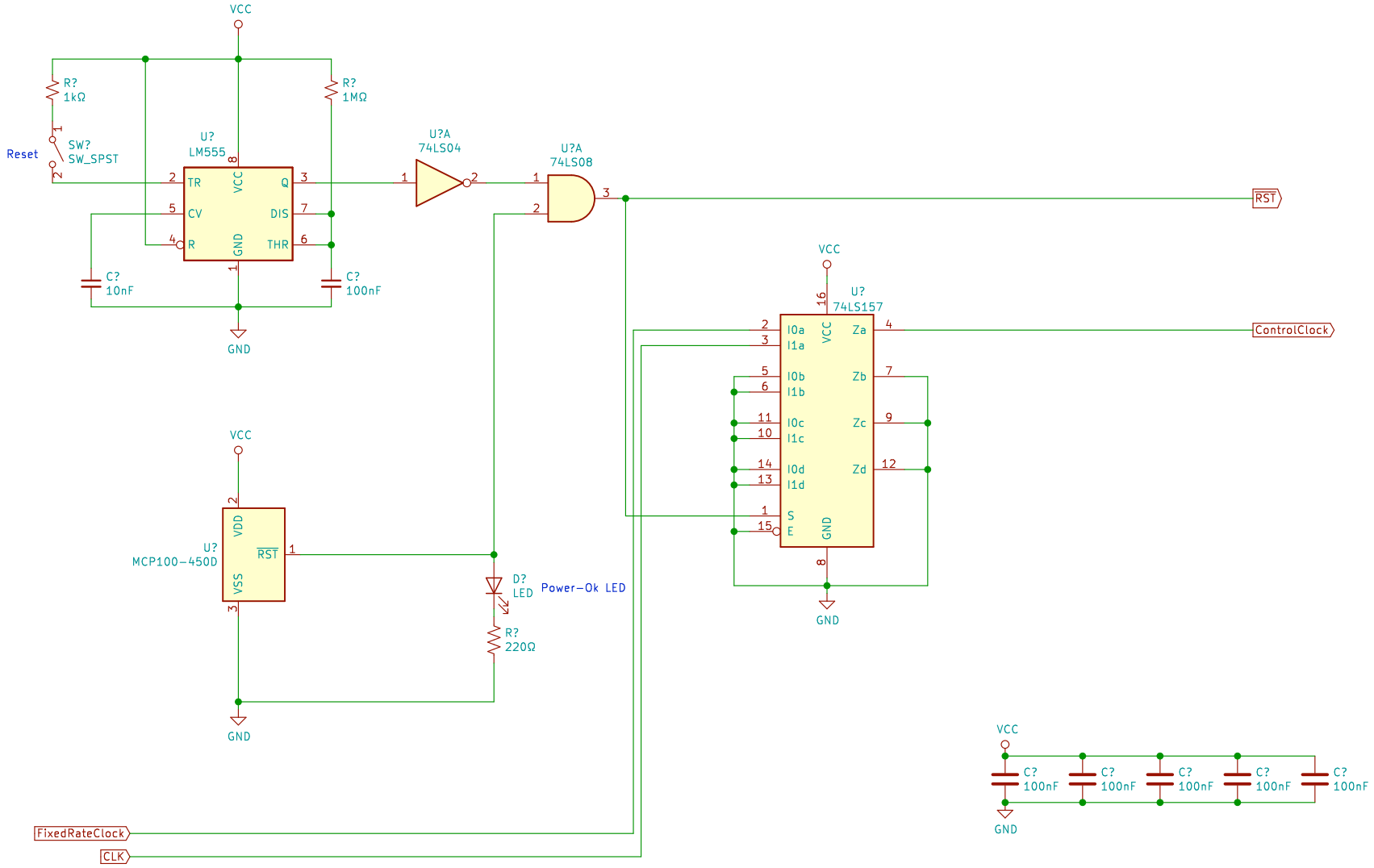
The clock module divides the signal from the crystal oscillator at a rate determined by the three-bit control signal.

Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: A | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.0-0) | Id: 2/20

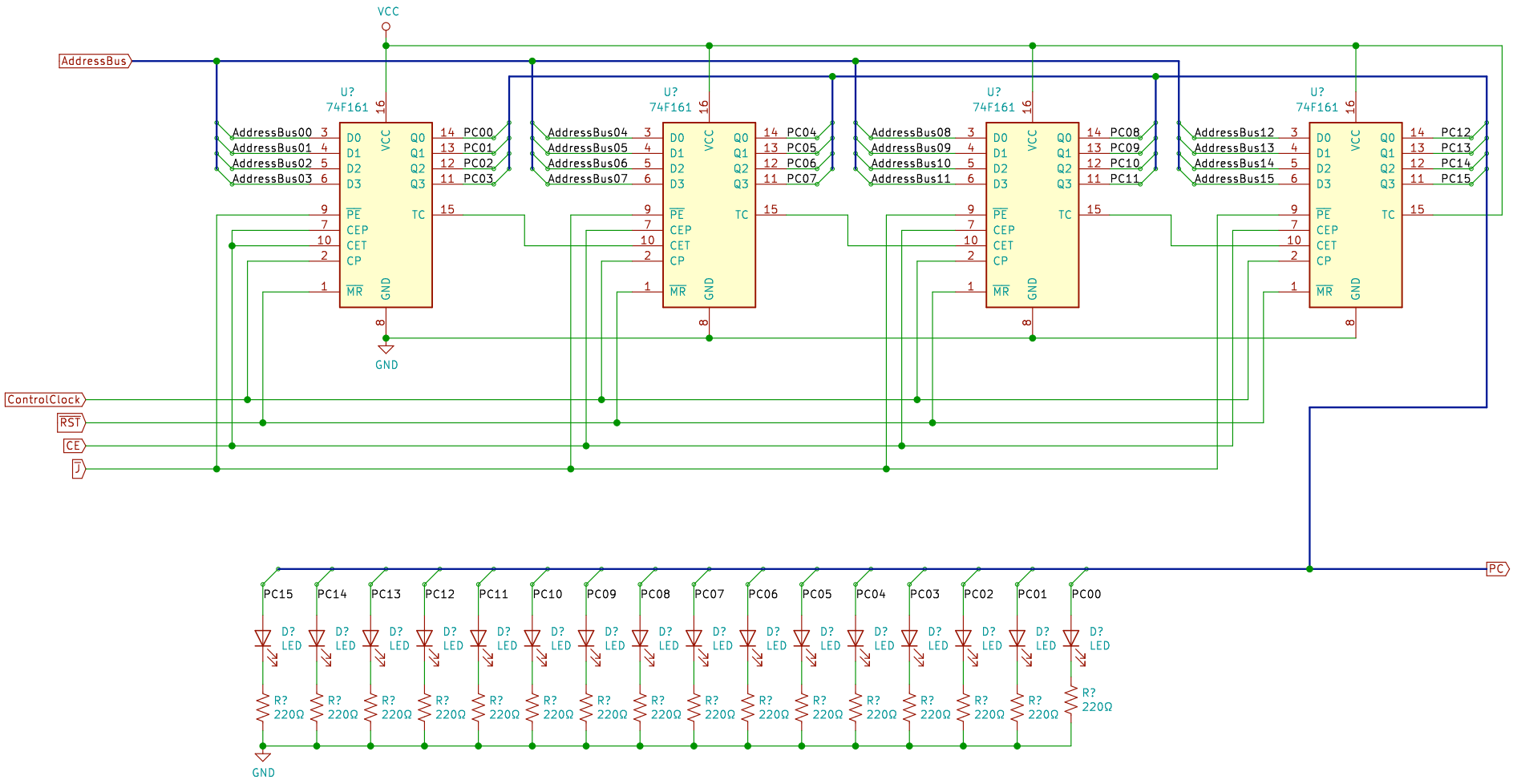


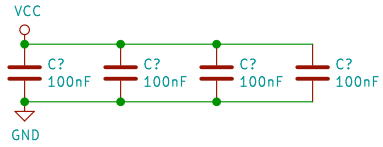
The MCP100 provides Power-on Reset functionality.
A button is also provided to manually reset the machine.
During reset, the control clock is pulsed repeatedly to flush the pipeline.

Sheet: /Power-on Reset/
File: Power-on Reset.sch

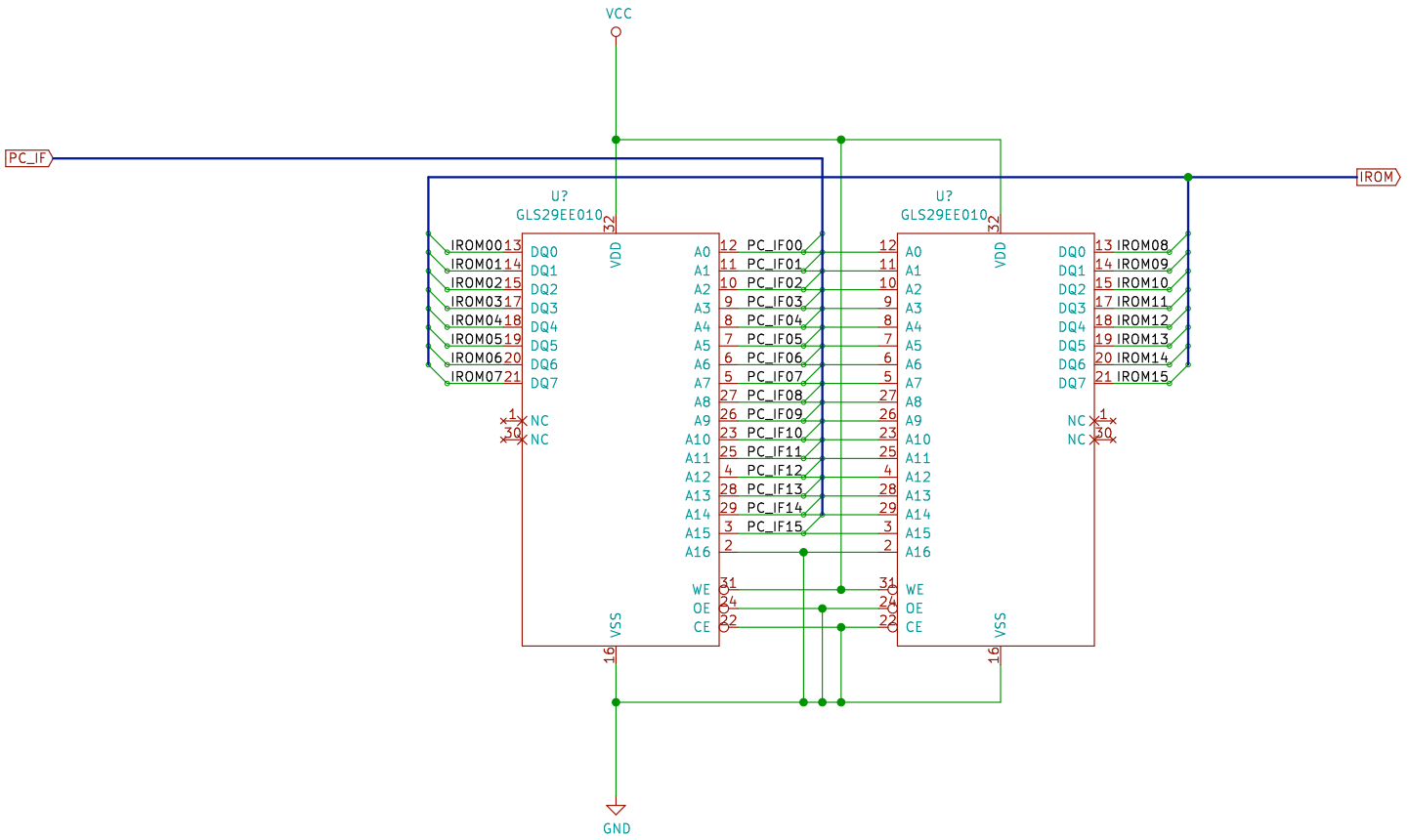
Title: Power-on Reset

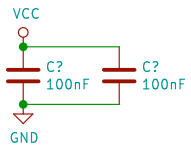
Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 3/20





Sheet: /Program Counter/	
File: Program Counter.sch	
Title: Program Counter	
Size: A	Date:
KiCad E.D.A. kicad (5.1.0-0)	Id: 4/20





16-bit instructions are read from ROM at the address specified by the Program Counter.

Sheet: /Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 5/20

Sheet: /Instruction RAM/
File: Instruction RAM.sch

Title: Instruction RAM

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 6/20

Sheet: /Instruction Decoder/
File: Instruction Decoder.sch

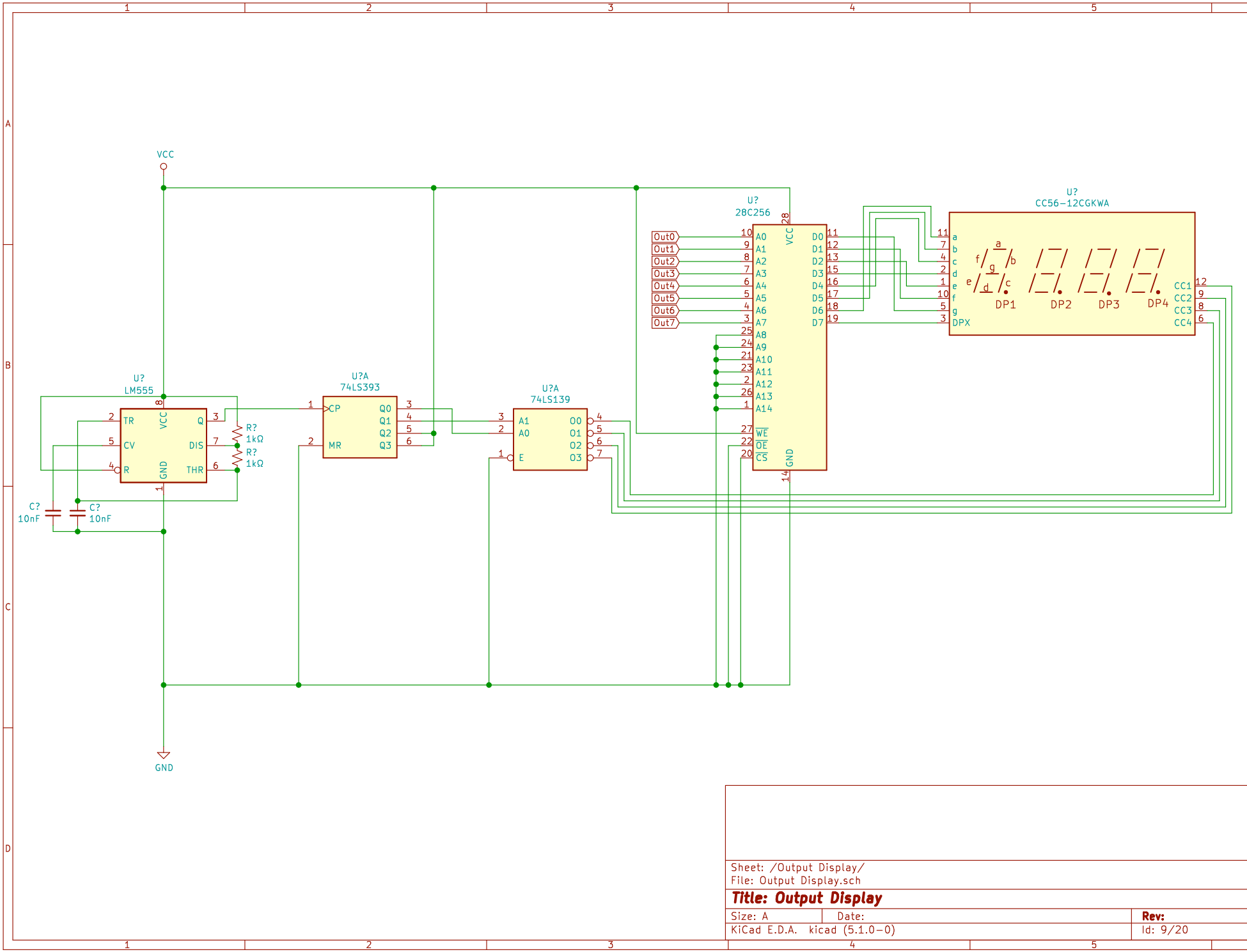
Title: Instruction Decoder

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 7/20

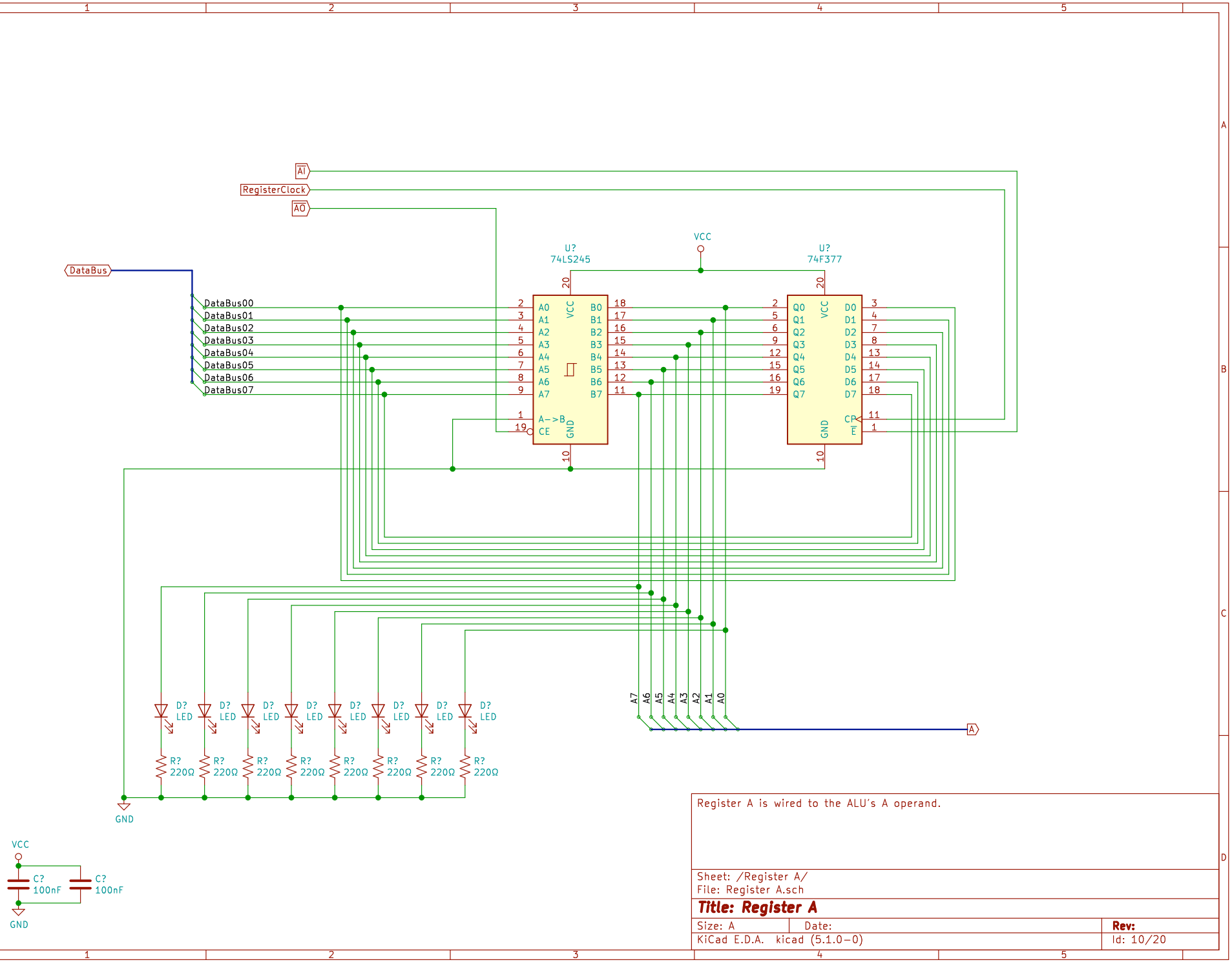
Sheet: /Execute/
File: Execute.sch

Title: Execute

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 8/20



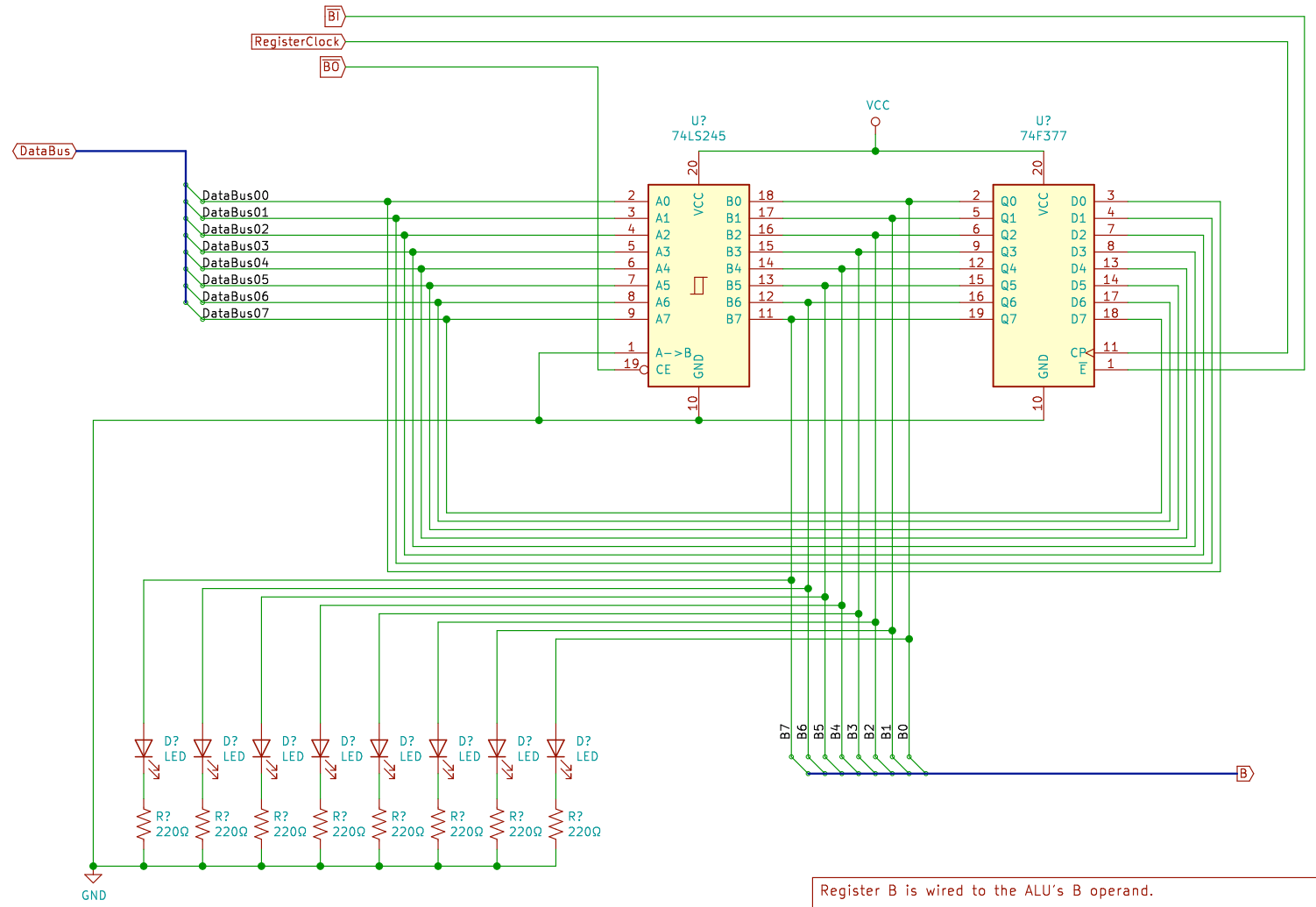
Sheet: /Output Display/	
File: Output Display.sch	
Title: Output Display	
Size: A	Date:
KiCad E.D.A. kicad (5.1.0-0)	Rev: Id: 9/20

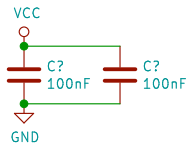

AI
RegisterClock
AO
DataBus
DataBus00
DataBus01
DataBus02
DataBus03
DataBus04
DataBus05
DataBus06
DataBus07
U?
74LS245
A0
A1
A2
A3
A4
A5
A6
A7
A->B
CE
VCC
GND
B0
B1
B2
B3
B4
B5
B6
B7
U?
74F377
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
D0
D1
D2
D3
D4
D5
D6
D7
CP
D?
LED
R?
220Ω
A7
A6
A5
A4
A3
A2
A1
A0
A
C?
100nF
Register A is wired to the ALU's A operand.
Sheet: /Register A/
File: Register A.sch
Title: Register A
Size: A
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 10/20

Sheet: /ALU/
File: ALU.sch

Title: ALU

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 11/20





Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

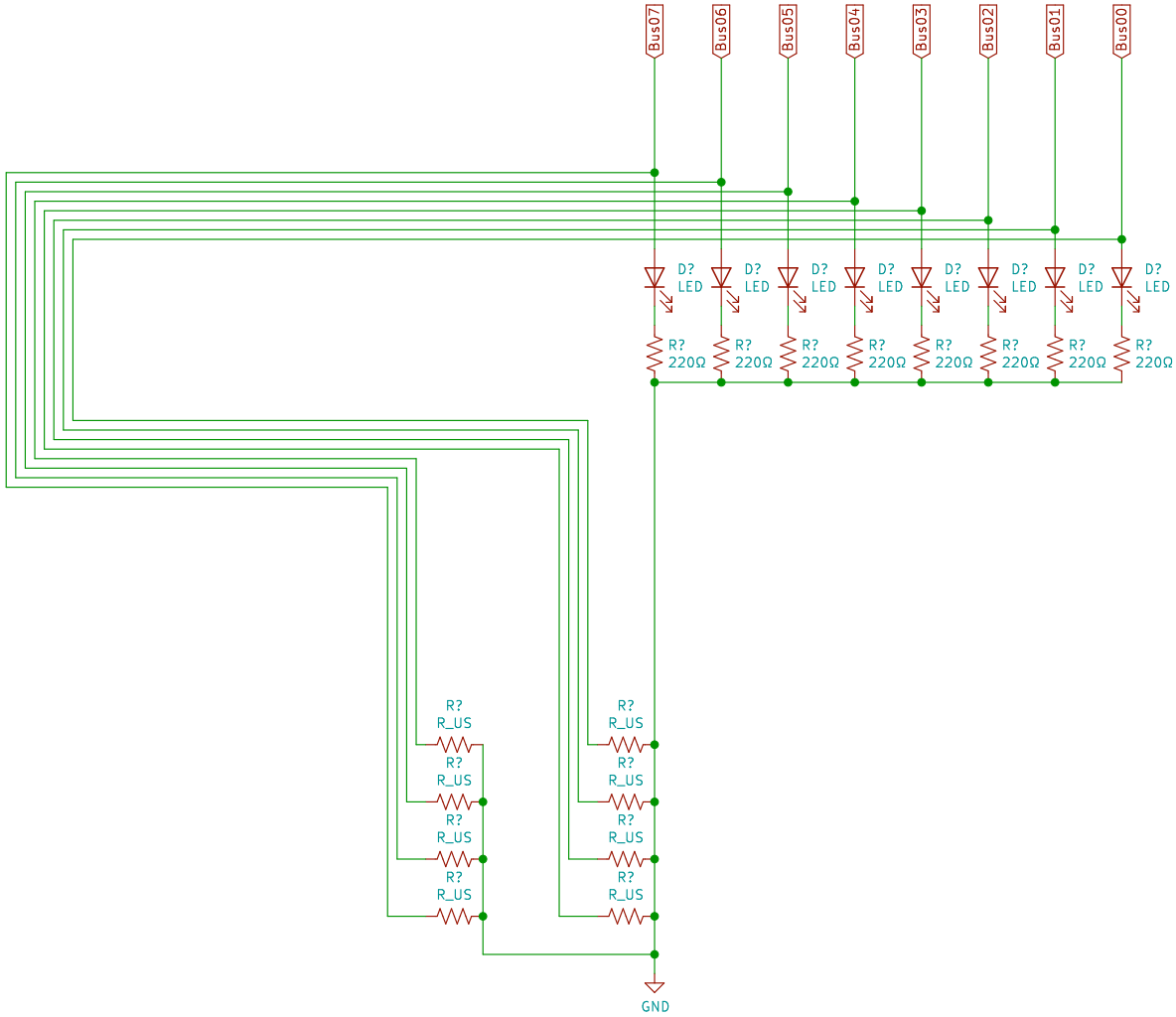
Title: Register B

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 12/20

Sheet: /Data RAM/
File: Data RAM.sch

Title: Data RAM

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 13/20

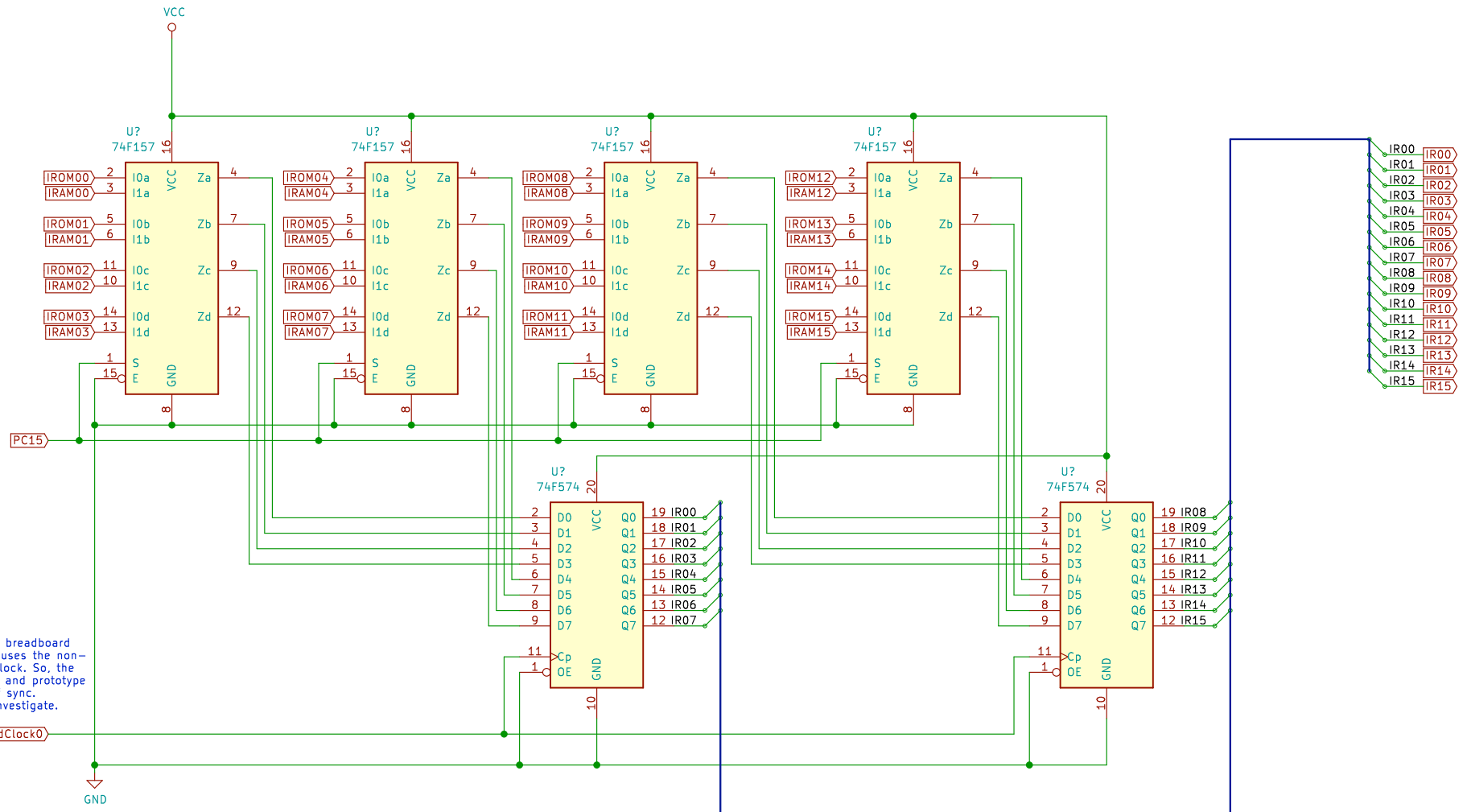


Sheet: /Bus Display/		
File: Bus Display.sch		
Title: Bus Display		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 14/20

Sheet: /Control Word Display/
File: Control Word Display.sch

Title: Control Word Display

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 15/20

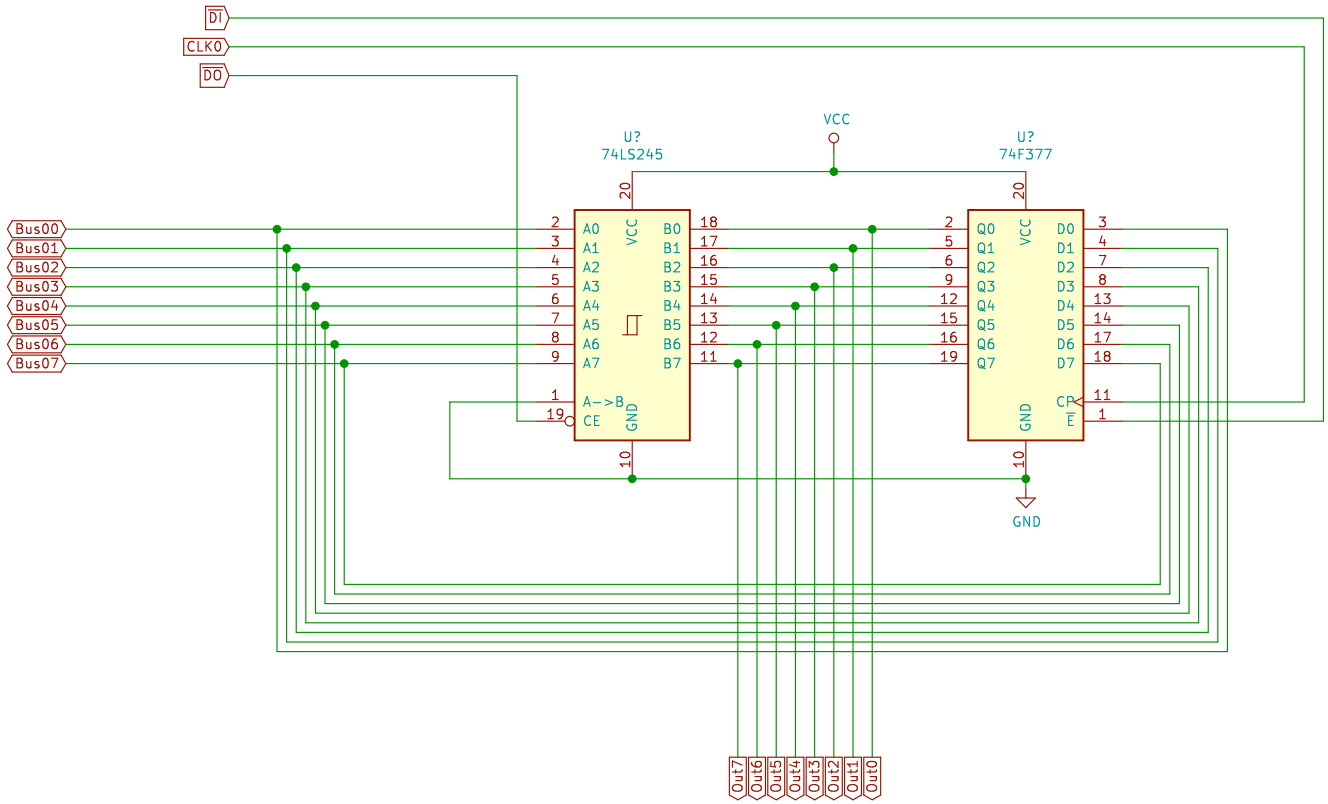


The Instruction Register receives input from either Instruction ROM or Instruction RAM.

Sheet: /Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 16/20

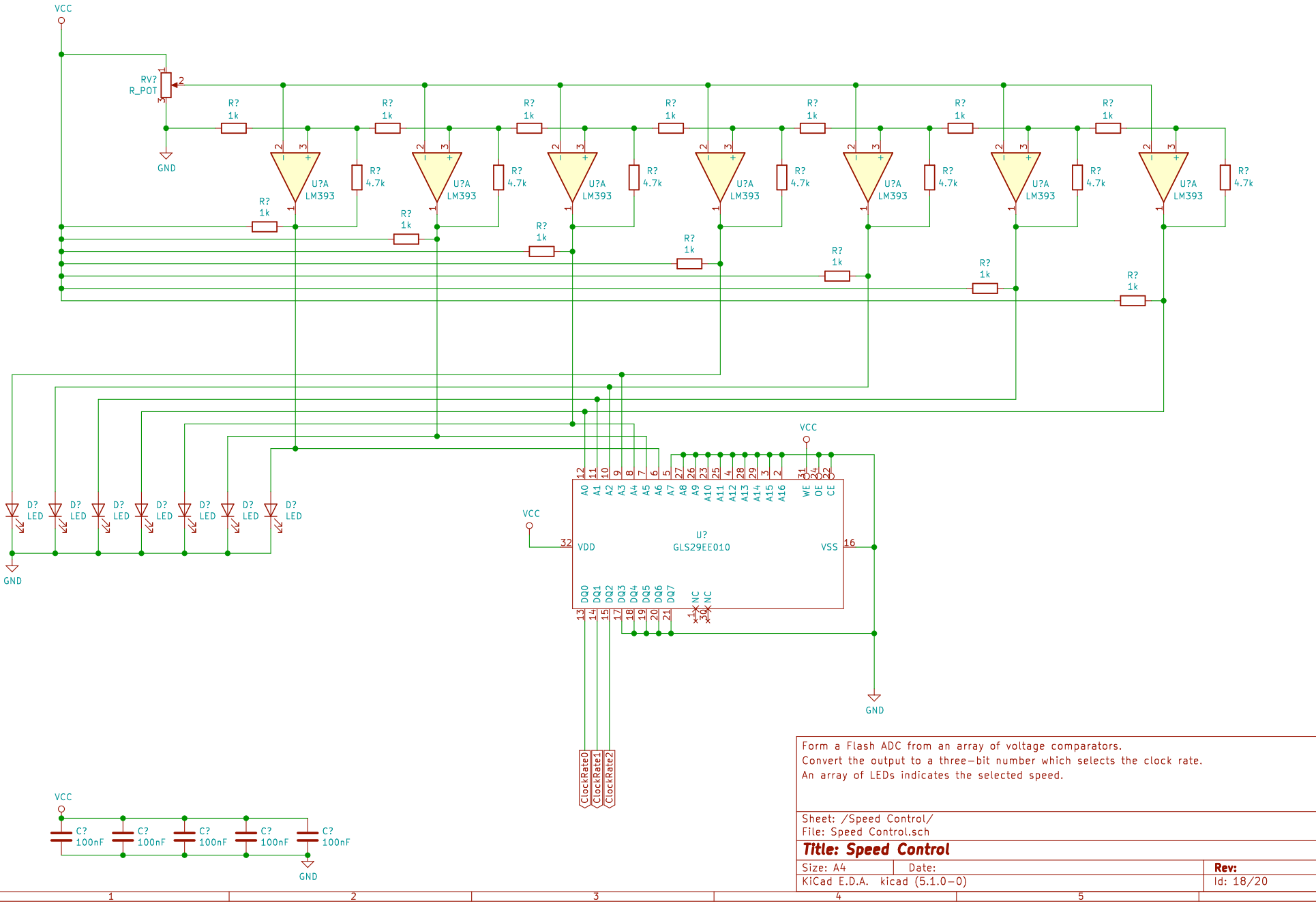


Register D is wired directly to the Output Display Module.

Sheet: /Register D/
File: Register D.sch

Title: Register D

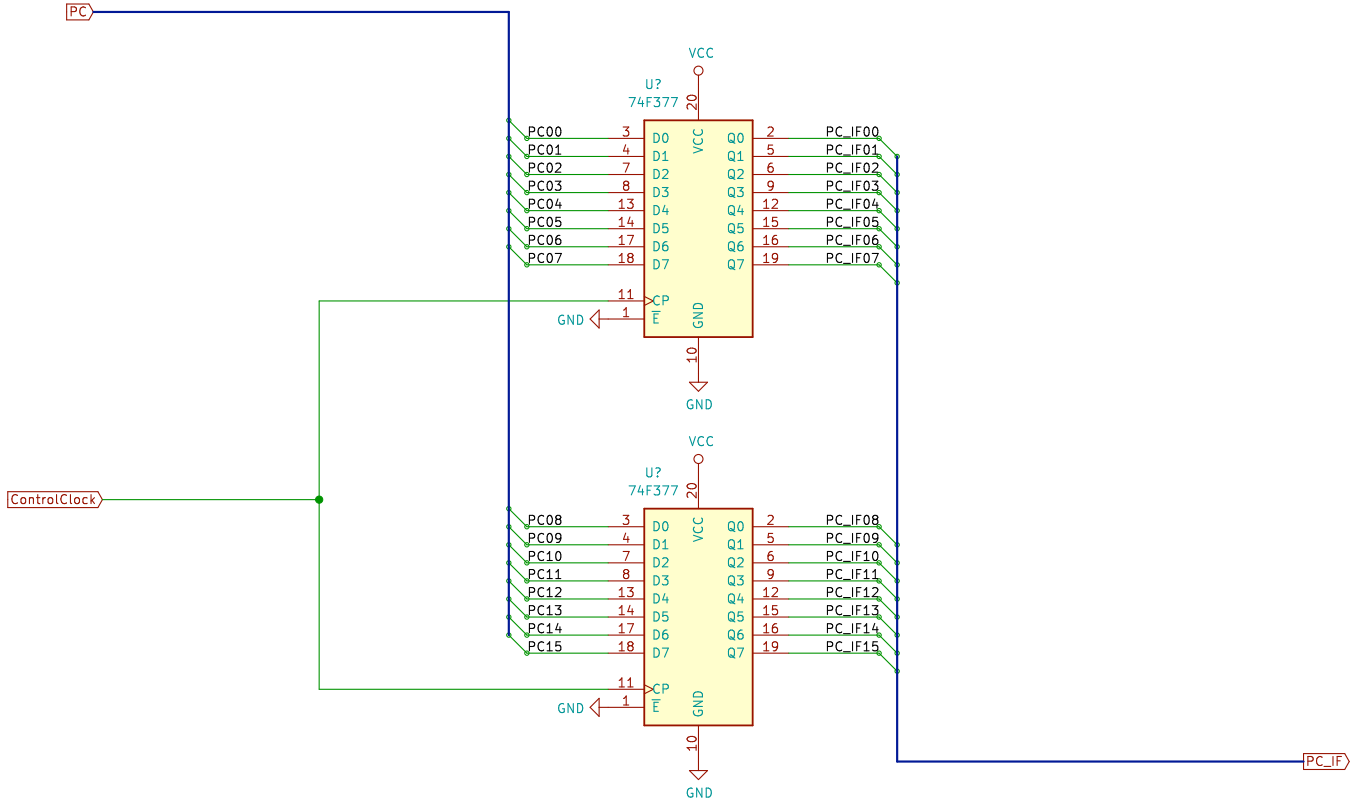
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 17/20

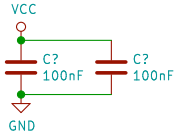

VCC
RV?
R_POT
GND
R?
1k
4.7k
U?A
LM393
D?
LED
U?
GLS29EE010
VDD
VSS
WE
OE
CE
NC
C?
100nF
ClockRate0
ClockRate1
ClockRate2
Form a Flash ADC from an array of voltage comparators.
Convert the output to a three-bit number which selects the clock rate.
An array of LEDs indicates the selected speed.
Sheet: /Speed Control/
File: Speed Control.sch
Title: Speed Control
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 18/20

Sheet: /Register XY/
File: Register XY.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 19/20





The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /PC/IF/
File: PC_IF.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 20/20