Sheet: Register XY

File: Register XY.sch

Sheet: Register A

File: Register A.sch

Sheet: Bus Display

File: Bus Display.sch

Sheet: Register UV

File: Register UV.sch

Sheet: Program Counter

File: Program Counter.sch

Sheet: Register B

File: Register B.sch

Sheet: Speed Control

File: Speed Control.sch

Sheet: Data RAM

File: Data RAM.sch

Sheet: Link Register

File: Link Register.sch

Sheet: ALU

File: ALU.sch

Sheet: Clock

File: Clock.sch

Sheet: Instruction Fetch

File: Instruction Fetch.sch

Sheet: Register D

File: Register D.sch

Sheet: Power-on Reset

File: Power-on Reset.sch

Sheet: Instruction Decode

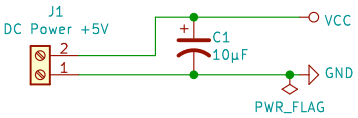
File: Instruction Decode.sch

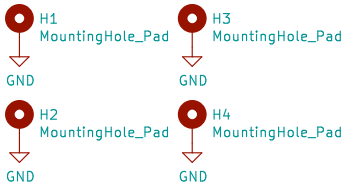
Sheet: Expansion

File: Expansion.sch

Sheet: Execute

File: Execute.sch



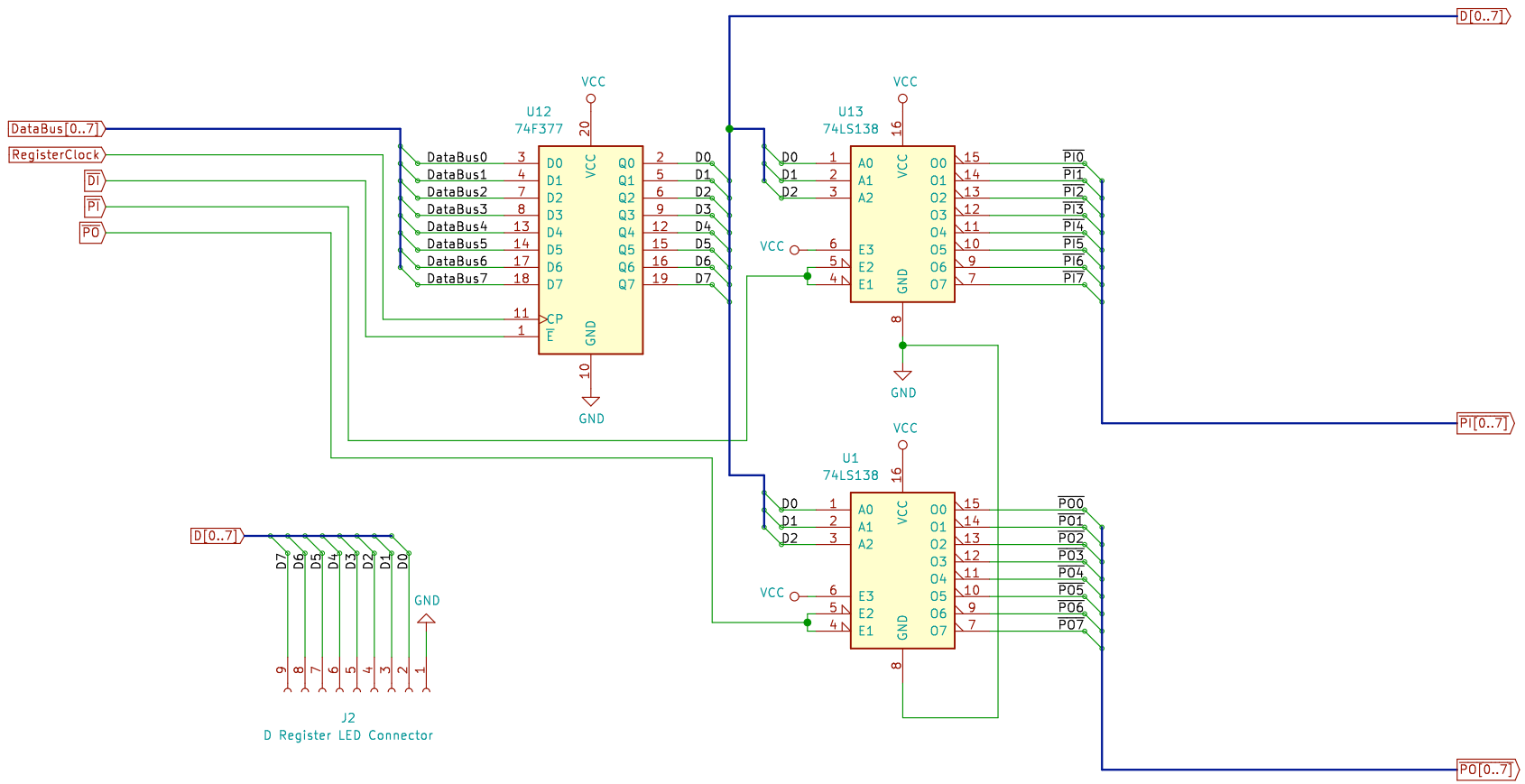


TTL microcomputer built from 74xx series logic chips.

Sheet: /
File: MainBoard.sch

Title: TurtleTTL: Main Board

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 1/23

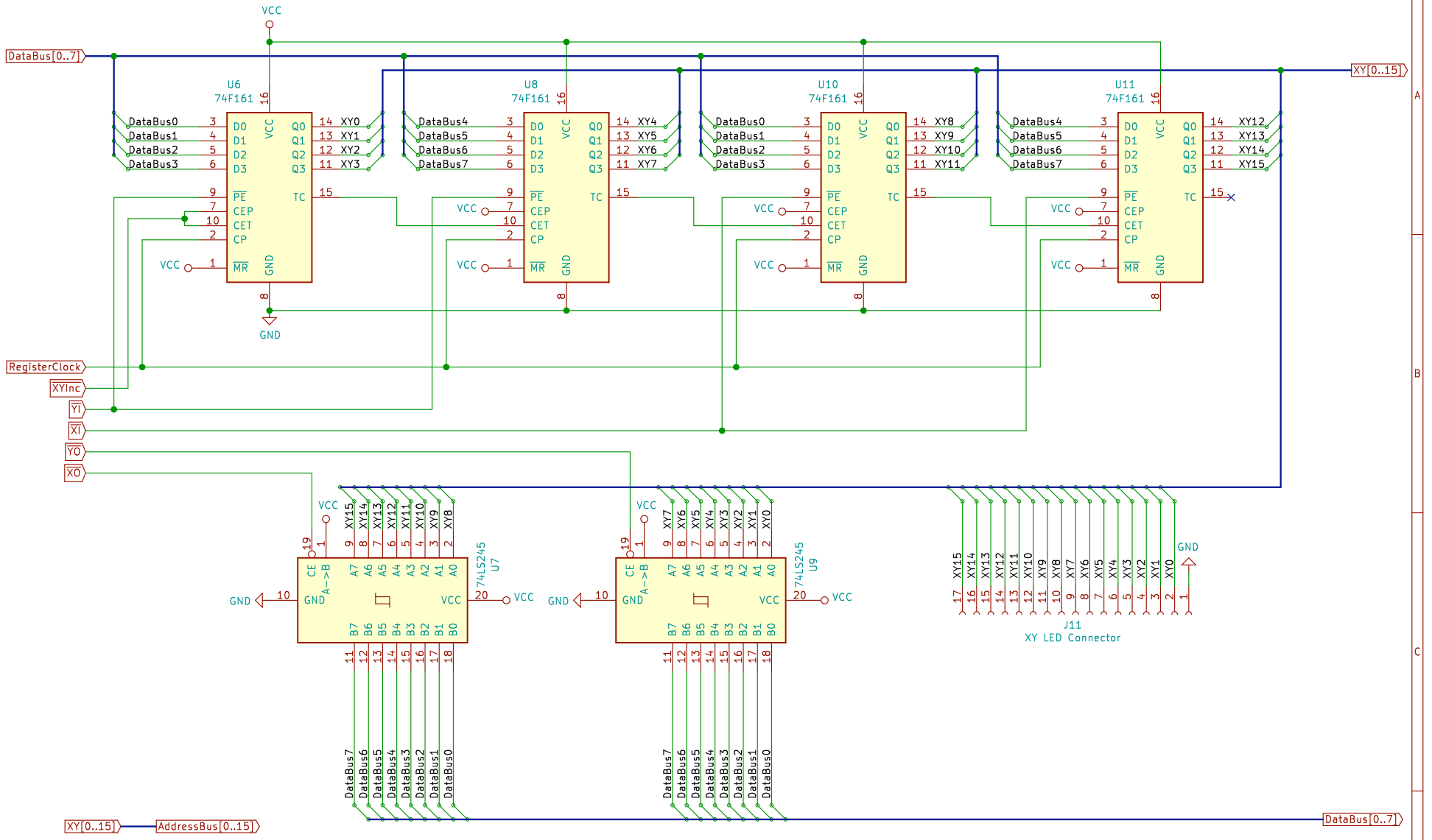


Register D controls the device select lines for peripherals and memory.

Sheet: /Register D/
File: Register D.sch

Title: Register D

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 2/23

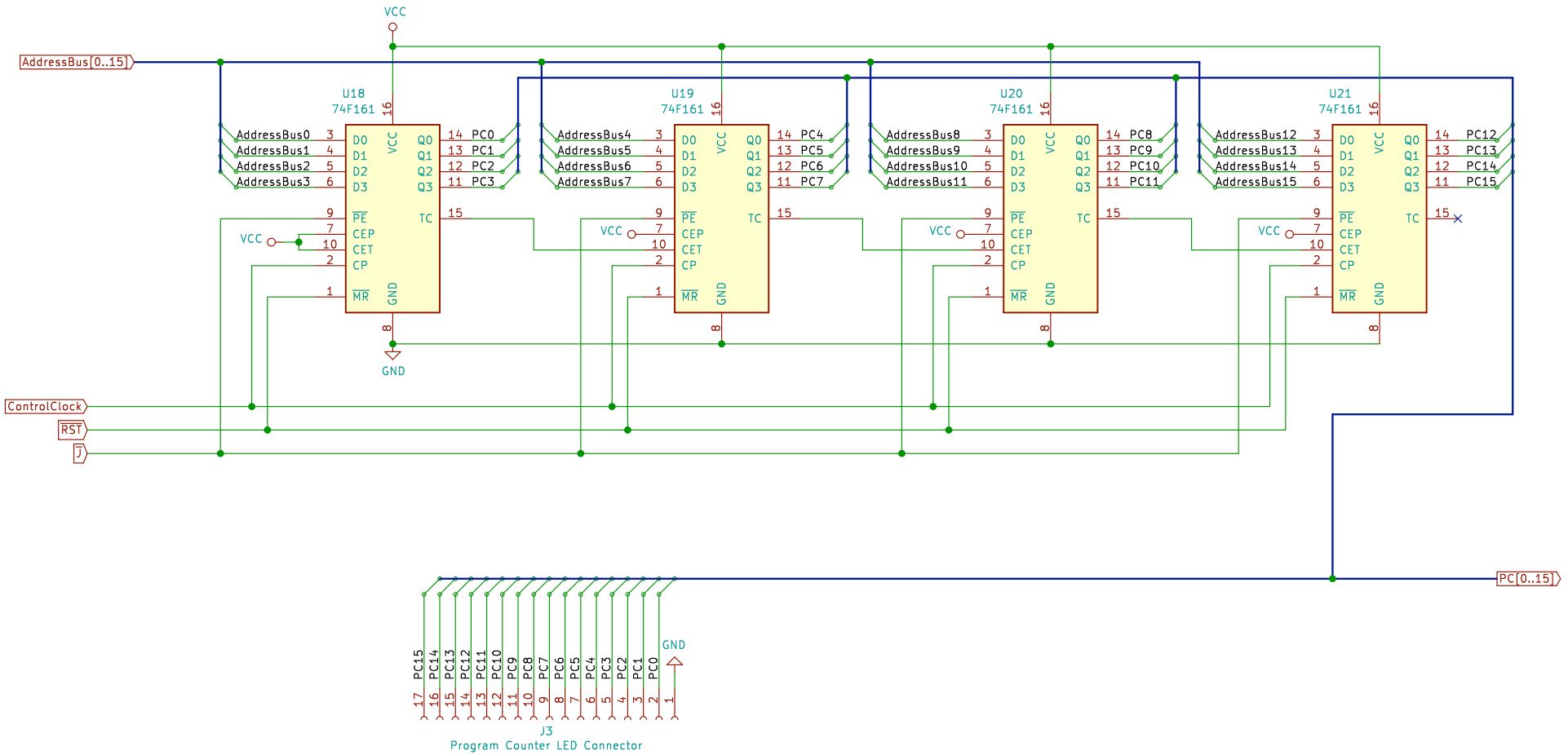


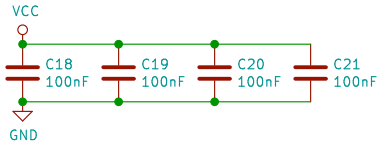
The XY register pair sets the value on the sixteen-bit Address Bus.

Sheet: /Register XY/
File: Register XY.sch

Title: Registers X and Y

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 3/23





Sheet: /Program Counter/	
File: Program Counter.sch	
Title: Program Counter	
Size: USLetter Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)	Id: 4/23

Sheet: PC/IF

File: PC_IF.sch

Sheet: Instruction RAM Address

File: Instruction RAM Address.sch

Sheet: Instruction ROM

File: Instruction ROM.sch

Sheet: Instruction RAM

File: Instruction RAM.sch

Sheet: Instruction Register

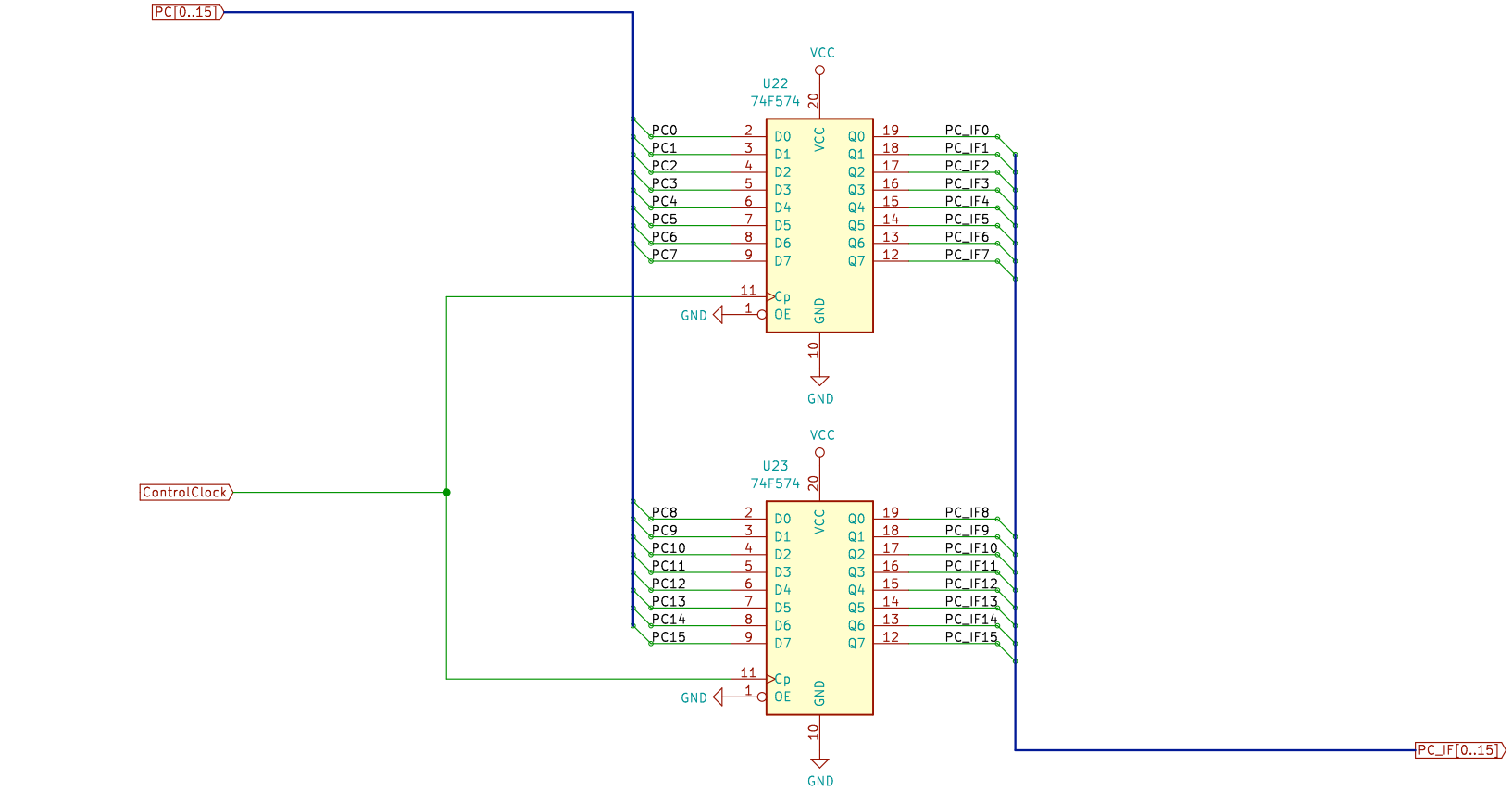
File: Instruction Register.sch

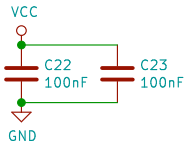
Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

Title: Instruction Fetch

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 5/23



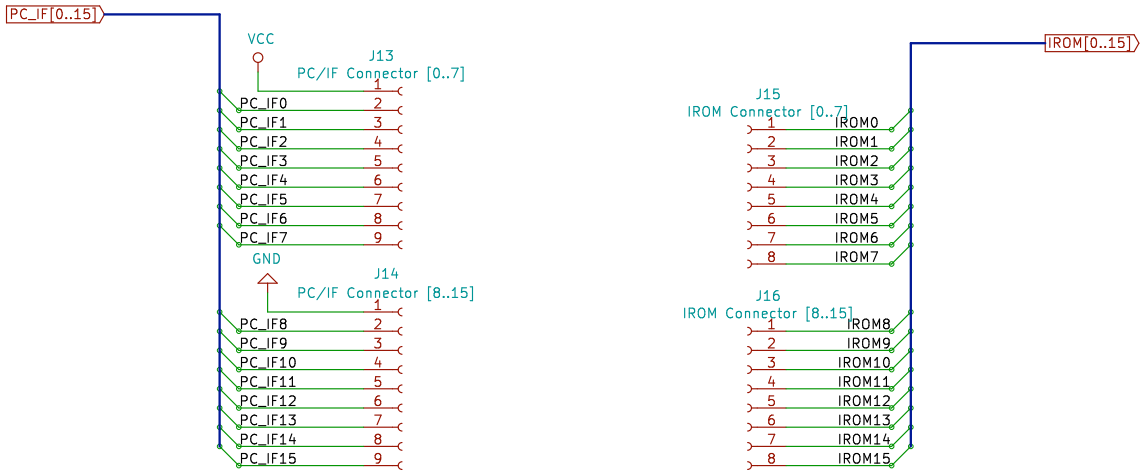


The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /Instruction Fetch/PC/IF/
File: PC_IF.sch

Title: PC/IF

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 6/23

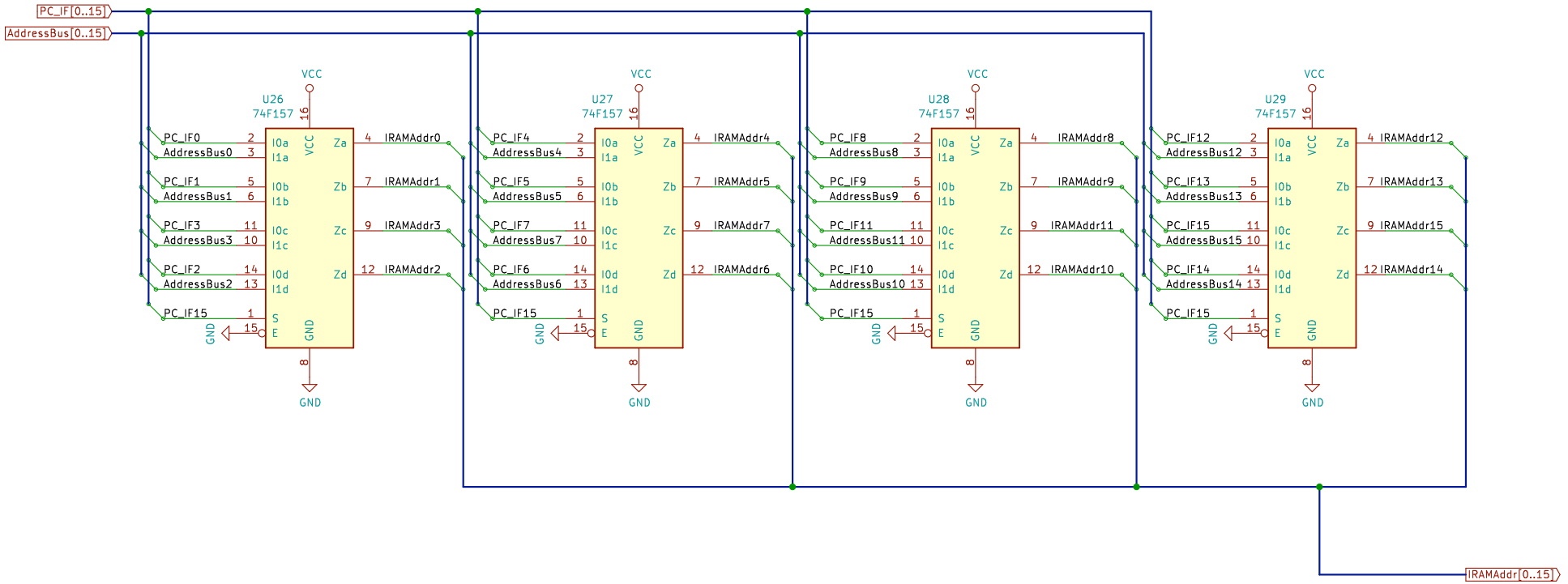


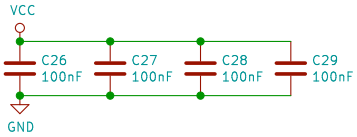
Instruction ROM is located on a daughter board.
This schematic describes the connectors by attach it to the main board.

Sheet: /Instruction Fetch/Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 7/23



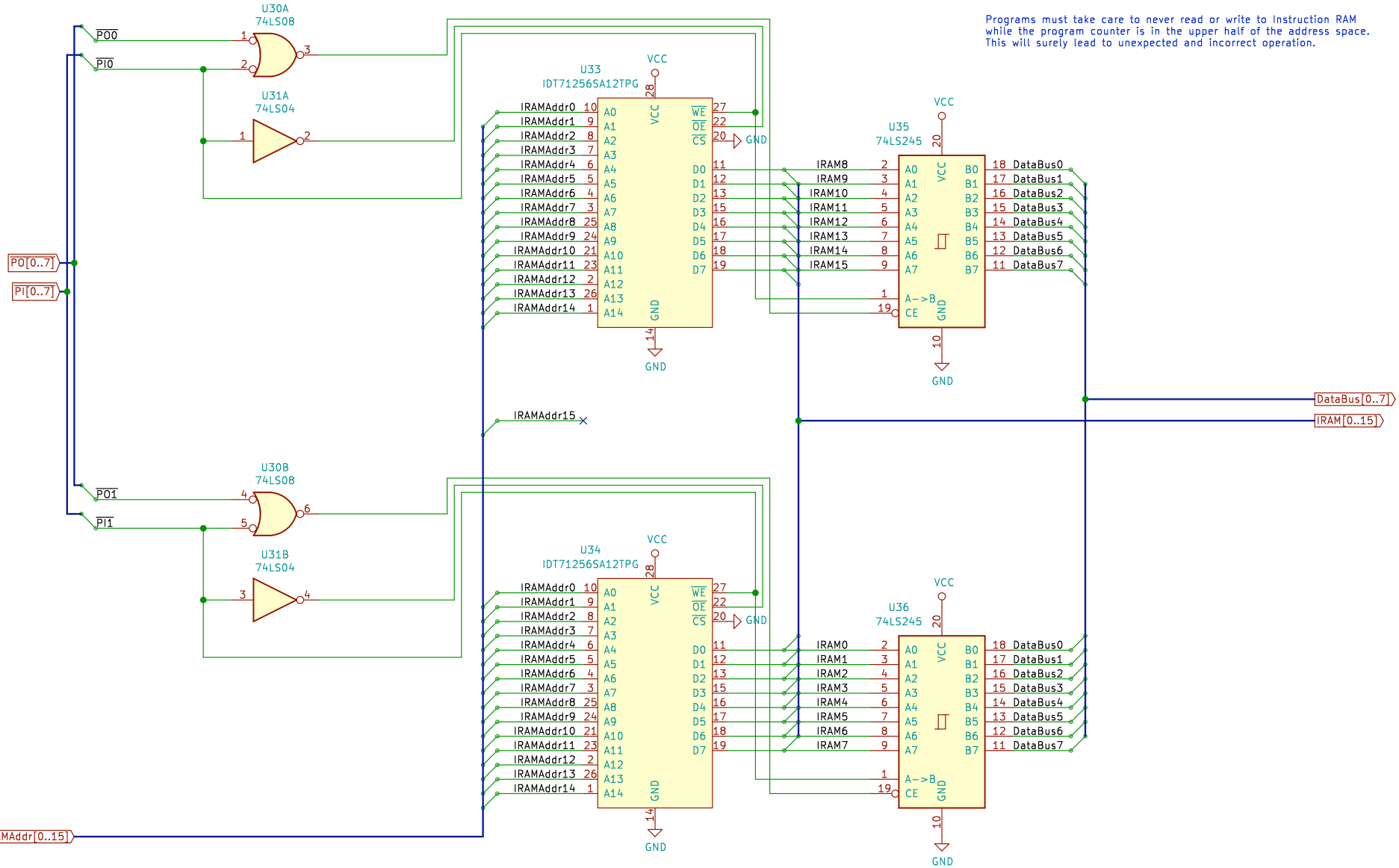


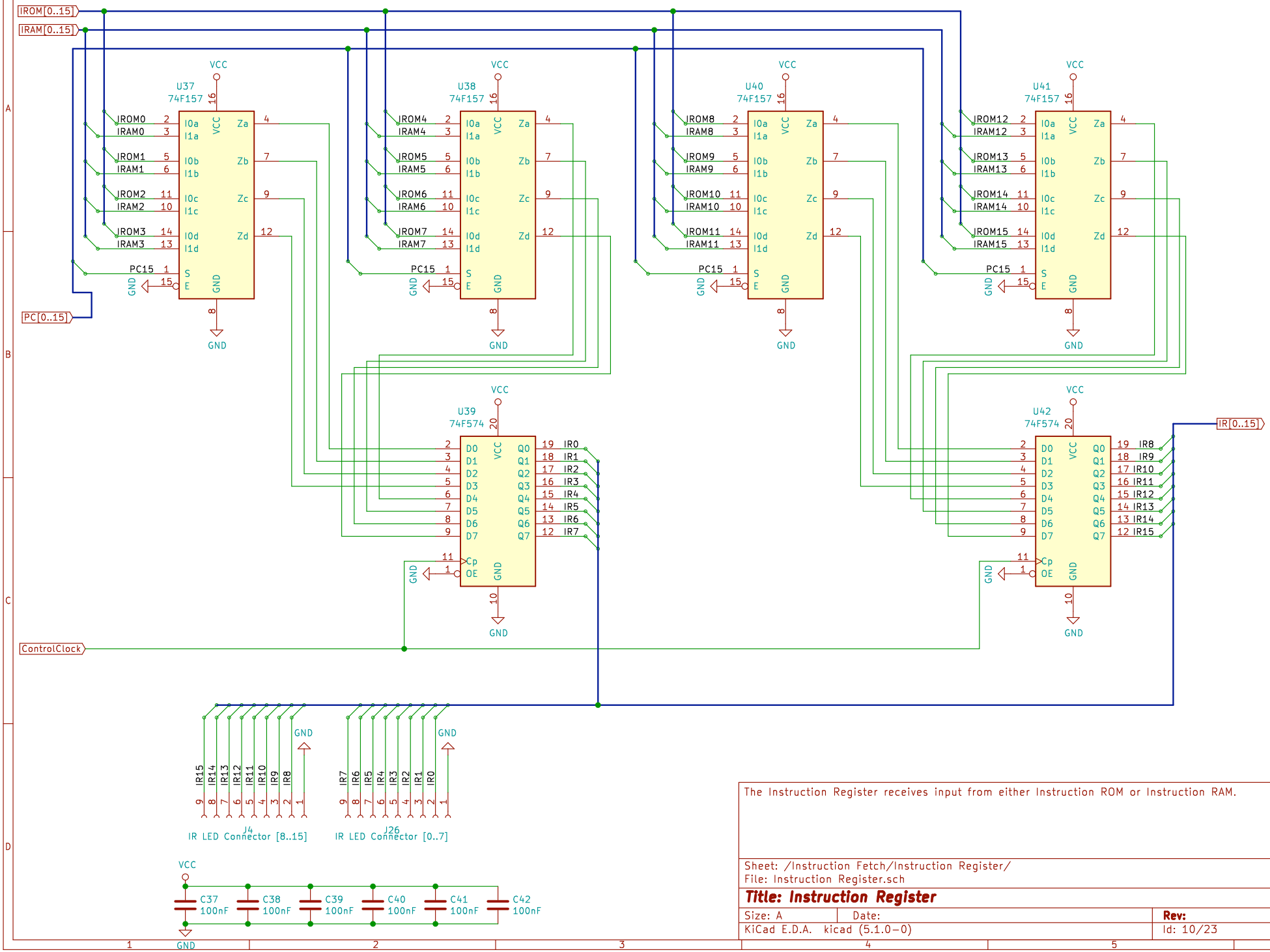
Instruction RAM uses an address from either the program counter or the address bus.
If the program counter is in the upper 32KB of the address space then use the program counter as we're running in Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM Address/
File: Instruction RAM Address.sch

Title: Instruction RAM Address

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 8/23


Programs must take care to never read or write to Instruction RAM while the program counter is in the upper half of the address space. This will surely lead to unexpected and incorrect operation.
U30A
74LS08
U31A
74LS04
U30B
74LS08
U31B
74LS04
PO0
PI0
PO1
PI1
PO[0..7]
PI[0..7]
U33
IDT71256SA12TPG
U34
IDT71256SA12TPG
IRAMAddr0
IRAMAddr1
IRAMAddr2
IRAMAddr3
IRAMAddr4
IRAMAddr5
IRAMAddr6
IRAMAddr7
IRAMAddr8
IRAMAddr9
IRAMAddr10
IRAMAddr11
IRAMAddr12
IRAMAddr13
IRAMAddr14
IRAMAddr15
IRAMAddr[0..15]
U35
74LS245
U36
74LS245
IRAM8
IRAM9
IRAM10
IRAM11
IRAM12
IRAM13
IRAM14
IRAM15
IRAM0
IRAM1
IRAM2
IRAM3
IRAM4
IRAM5
IRAM6
IRAM7
DataBus0
DataBus1
DataBus2
DataBus3
DataBus4
DataBus5
DataBus6
DataBus7
DataBus[0..7]
IRAM[0..15]
VCC
GND
C30 100nF
C31 100nF
C32 100nF
C33 100nF
C34 100nF
C35 100nF
For purposes of reading and writing, Instruction RAM is mapped to both the lower and upper halves of the address space. Though, the control unit only executes code in the upper half.
The Instruction RAM module allows a portion of Instruction Memory to be accessed from the data bus.
Sheet: /Instruction Fetch/Instruction RAM/
File: Instruction RAM.sch
Title: Instruction RAM
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 9/23

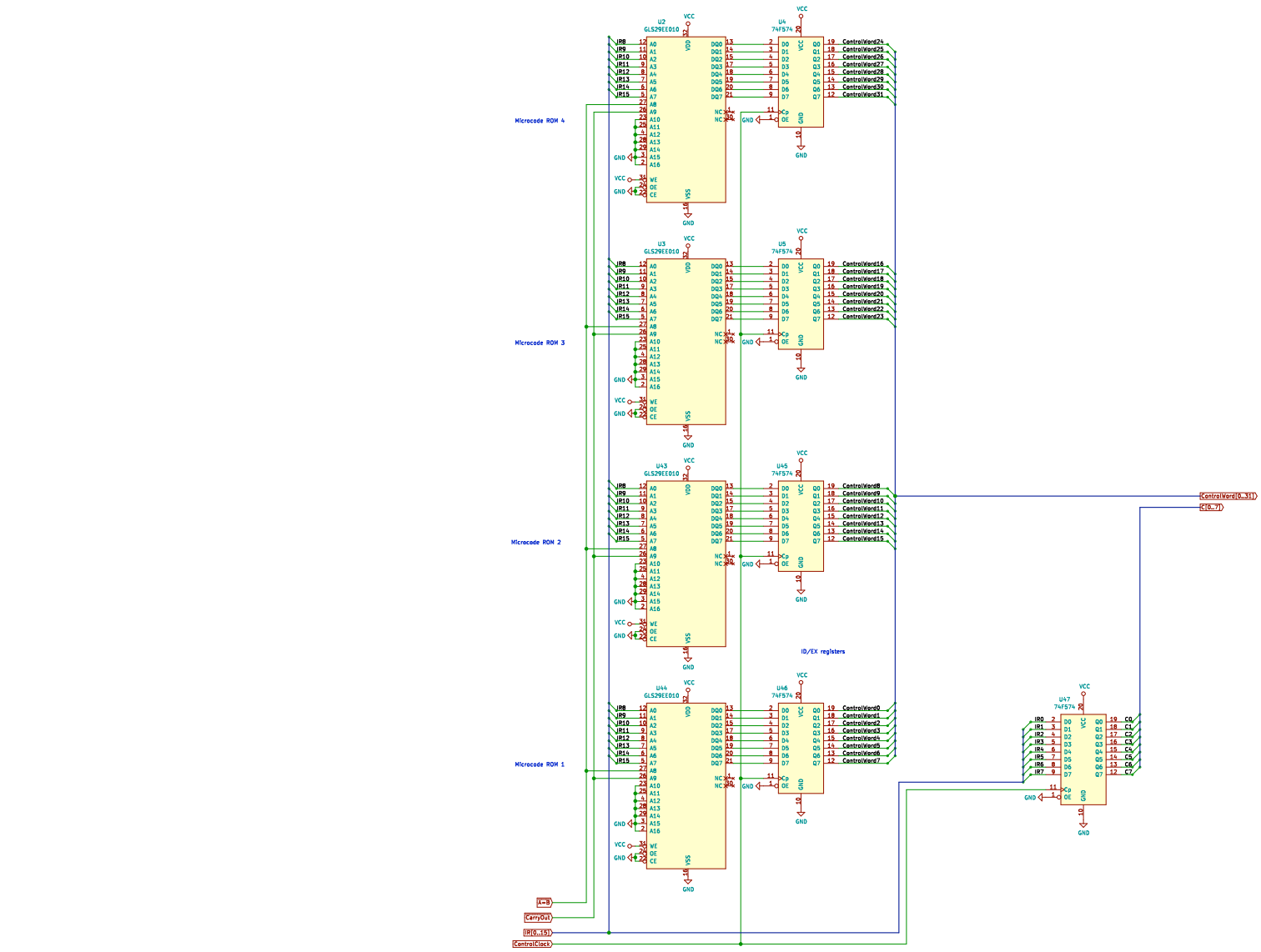


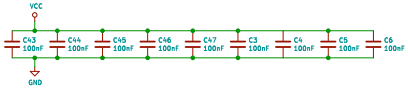
The Instruction Register receives input from either Instruction ROM or Instruction RAM.

Sheet: /Instruction Fetch/Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 10/23



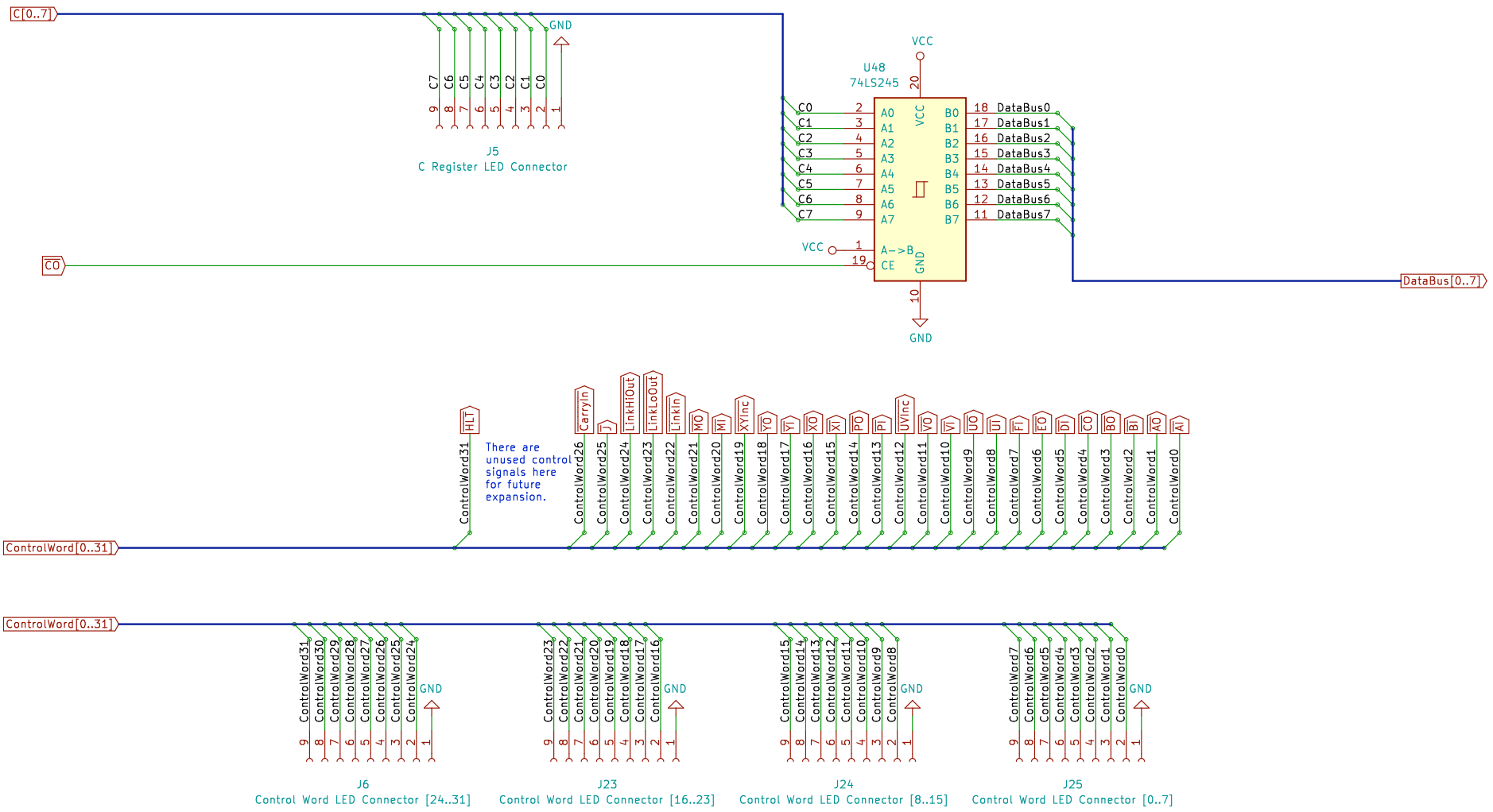


The instruction Decoder decodes an eight bit opcode into a sixteen-bit control word.

Sheet: /Instruction Decode/
File: Instruction Decode.sch

Title: Instruction Decode

Size: A2	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 11/23

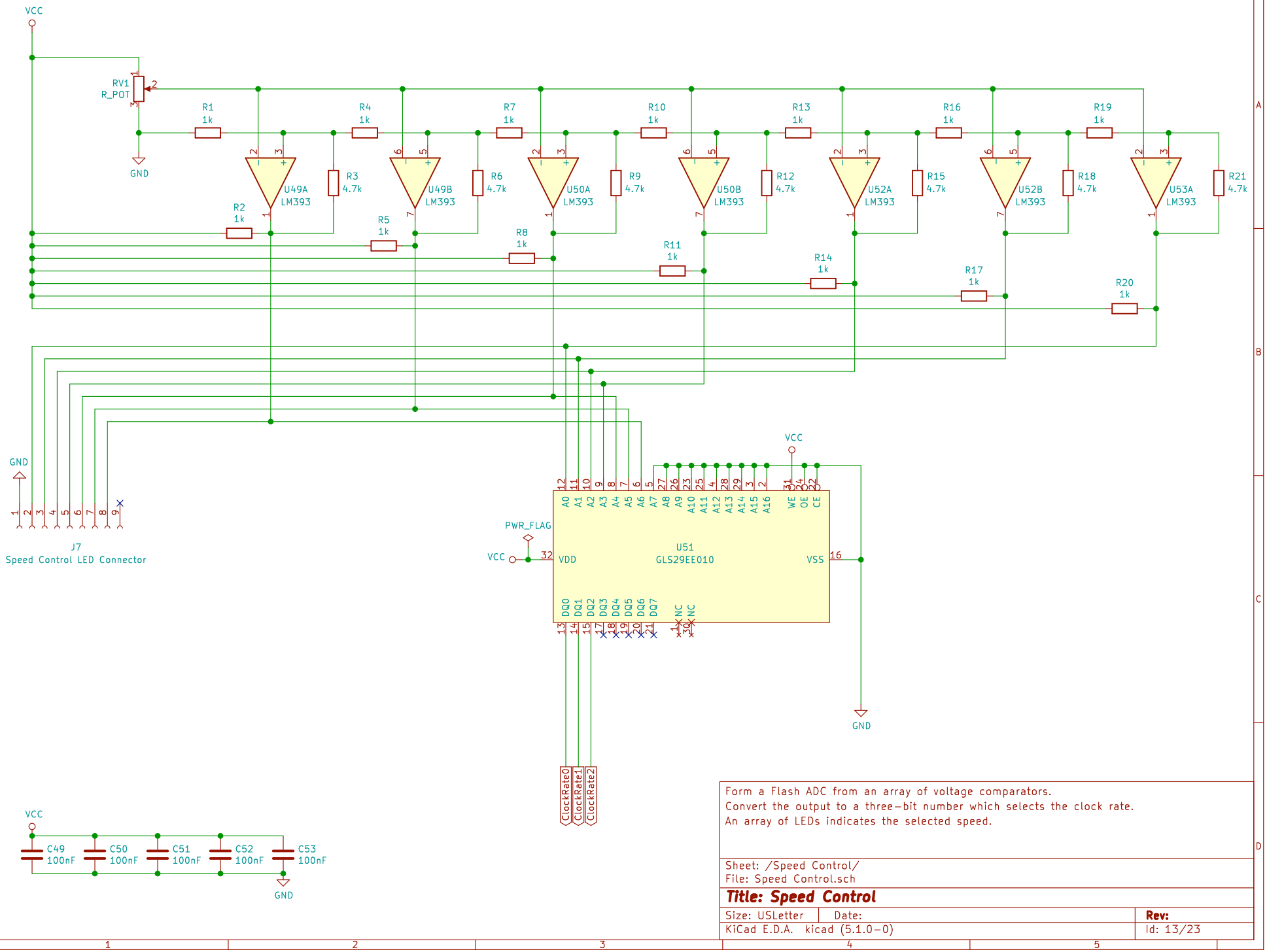


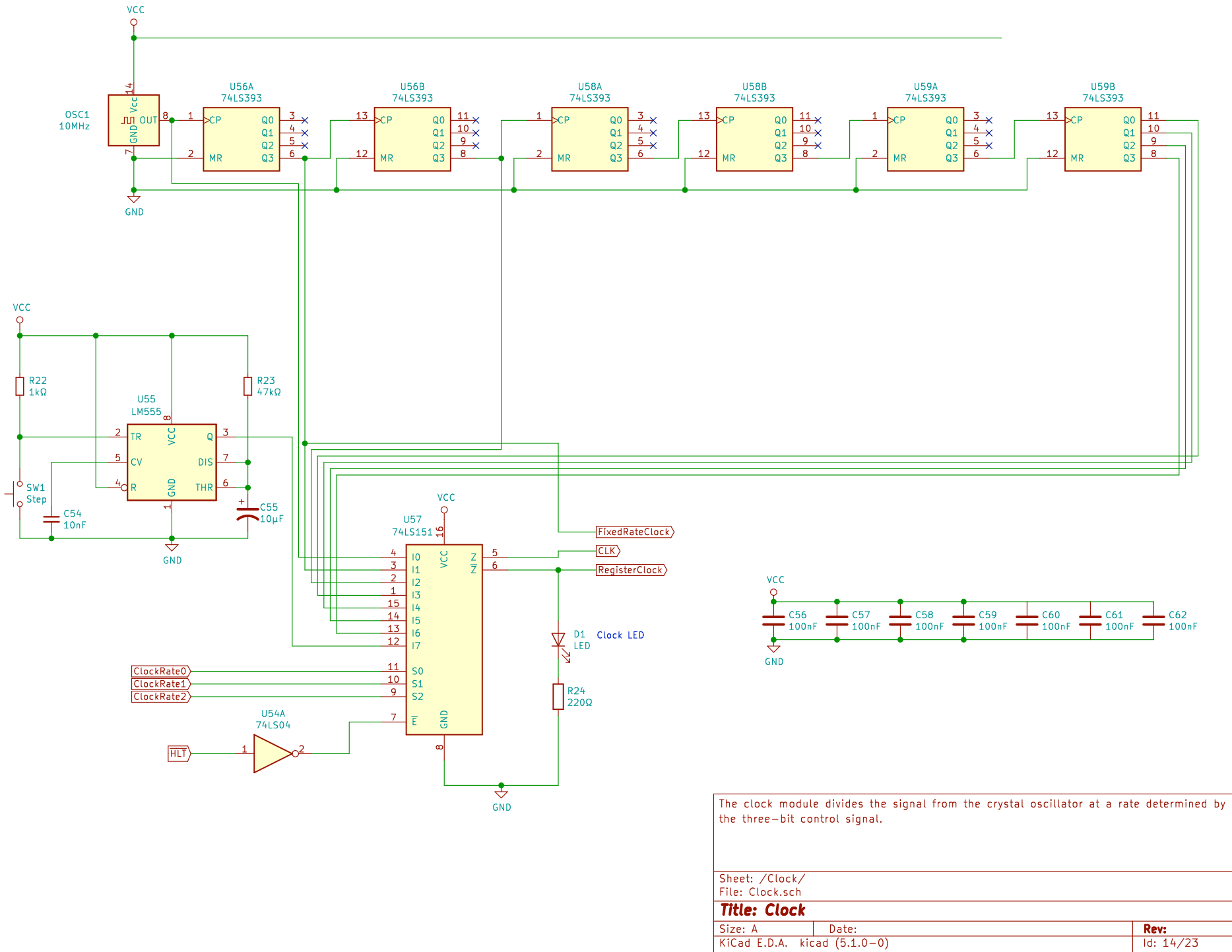
The lower eight bits of the instruction register can be expressed onto the data bus as a constant value.

Sheet: /Execute/
File: Execute.sch

Title: Execute

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 12/23


VCC
RV1
R_POT
GND
R1 1k
R2 1k
R3 4.7k
R4 1k
R5 1k
R6 4.7k
R7 1k
R8 1k
R9 4.7k
R10 1k
R11 1k
R12 4.7k
R13 1k
R14 1k
R15 4.7k
R16 1k
R17 1k
R18 4.7k
R19 1k
R20 1k
R21 4.7k
U49A LM393
U49B LM393
U50A LM393
U50B LM393
U52A LM393
U52B LM393
U53A LM393
J7
Speed Control LED Connector
PWR_FLAG
U51
GLS29EE010
VDD
VSS
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
WE OE CE
NC NC
ClockRate0
ClockRate1
ClockRate2
C49 100nF
C50 100nF
C51 100nF
C52 100nF
C53 100nF
Form a Flash ADC from an array of voltage comparators.
Convert the output to a three-bit number which selects the clock rate.
An array of LEDs indicates the selected speed.
Sheet: /Speed Control/
File: Speed Control.sch
Title: Speed Control
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 13/23



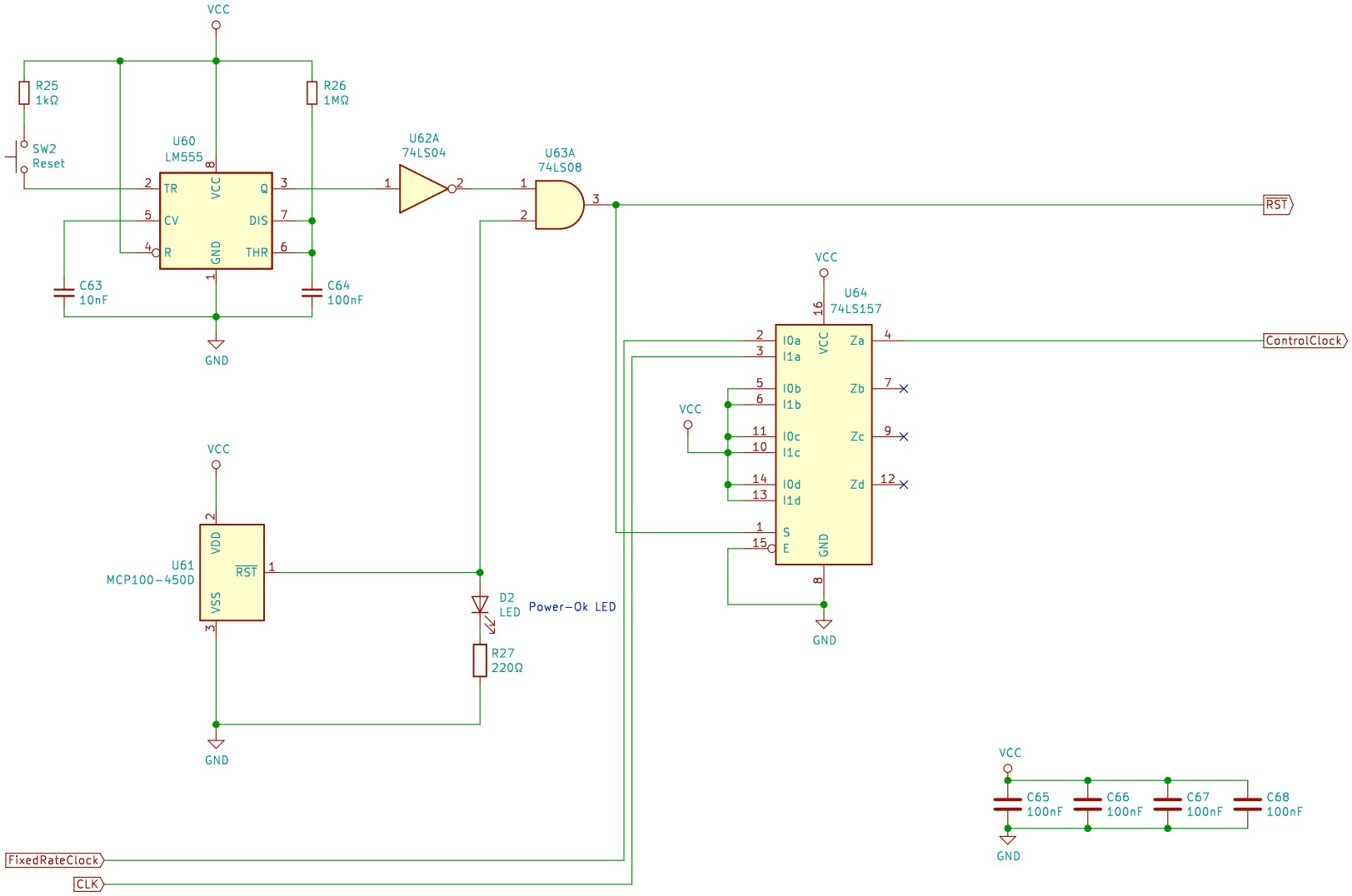
The clock module divides the signal from the crystal oscillator at a rate determined by the three-bit control signal.

Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: A | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.0-0) | Id: 14/23

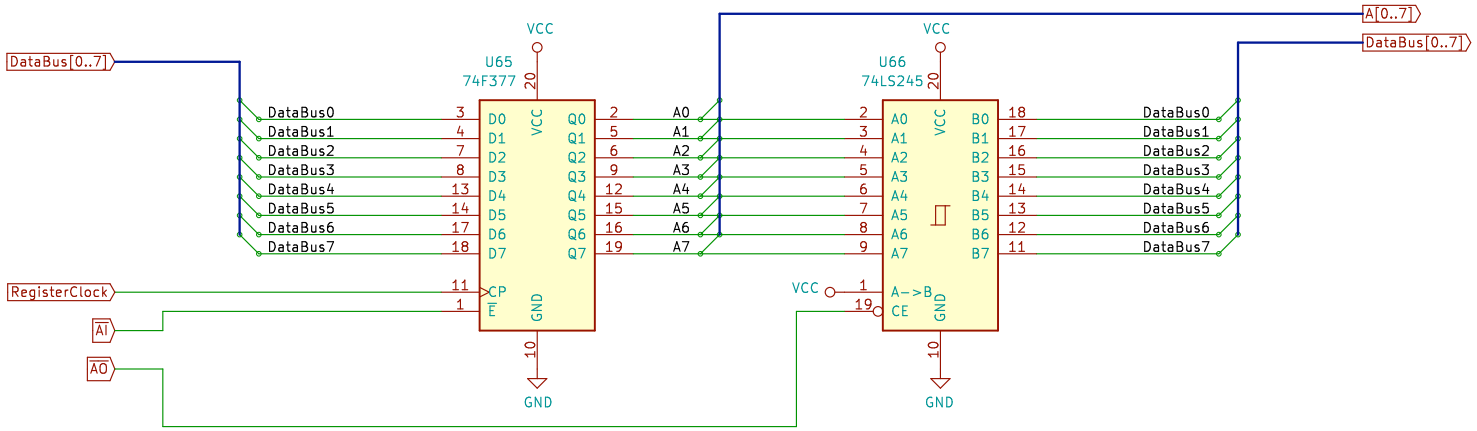


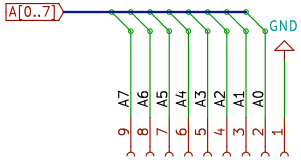
The MCP100 provides Power-on Reset functionality.
A button is also provided to manually reset the machine.
During reset, the control clock is pulsed repeatedly to flush the pipeline.

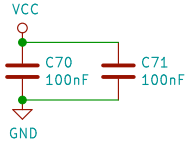
Sheet: /Power-on Reset/
File: Power-on Reset.sch

Title: Power-on Reset

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 15/23





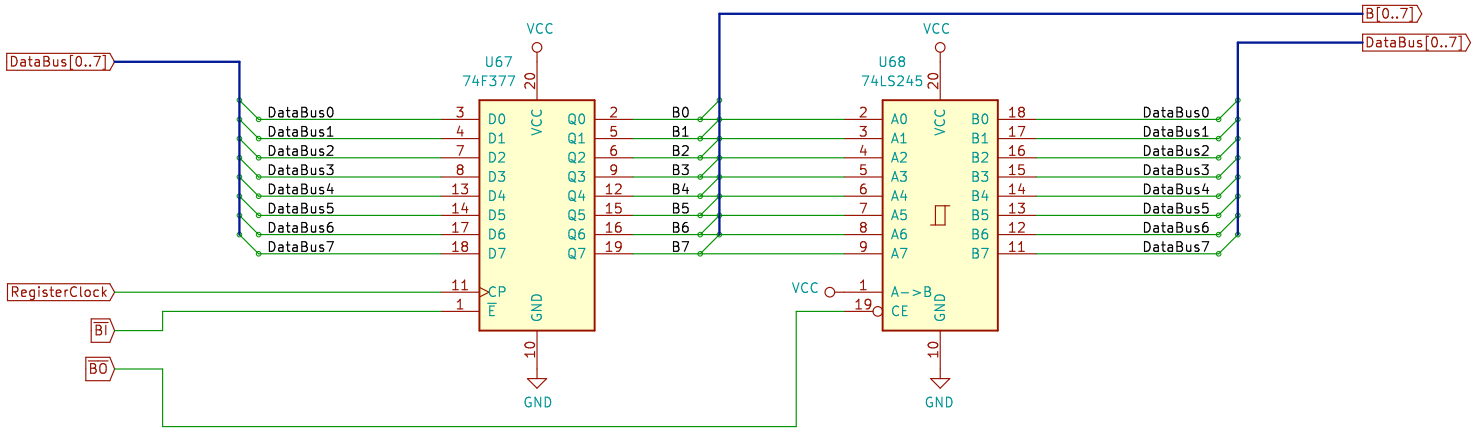


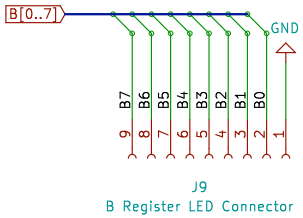
Register A is wired to the ALU's A operand.

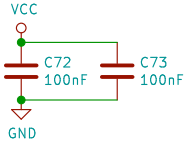
Sheet: /Register A/
File: Register A.sch

Title: Register A

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 16/23





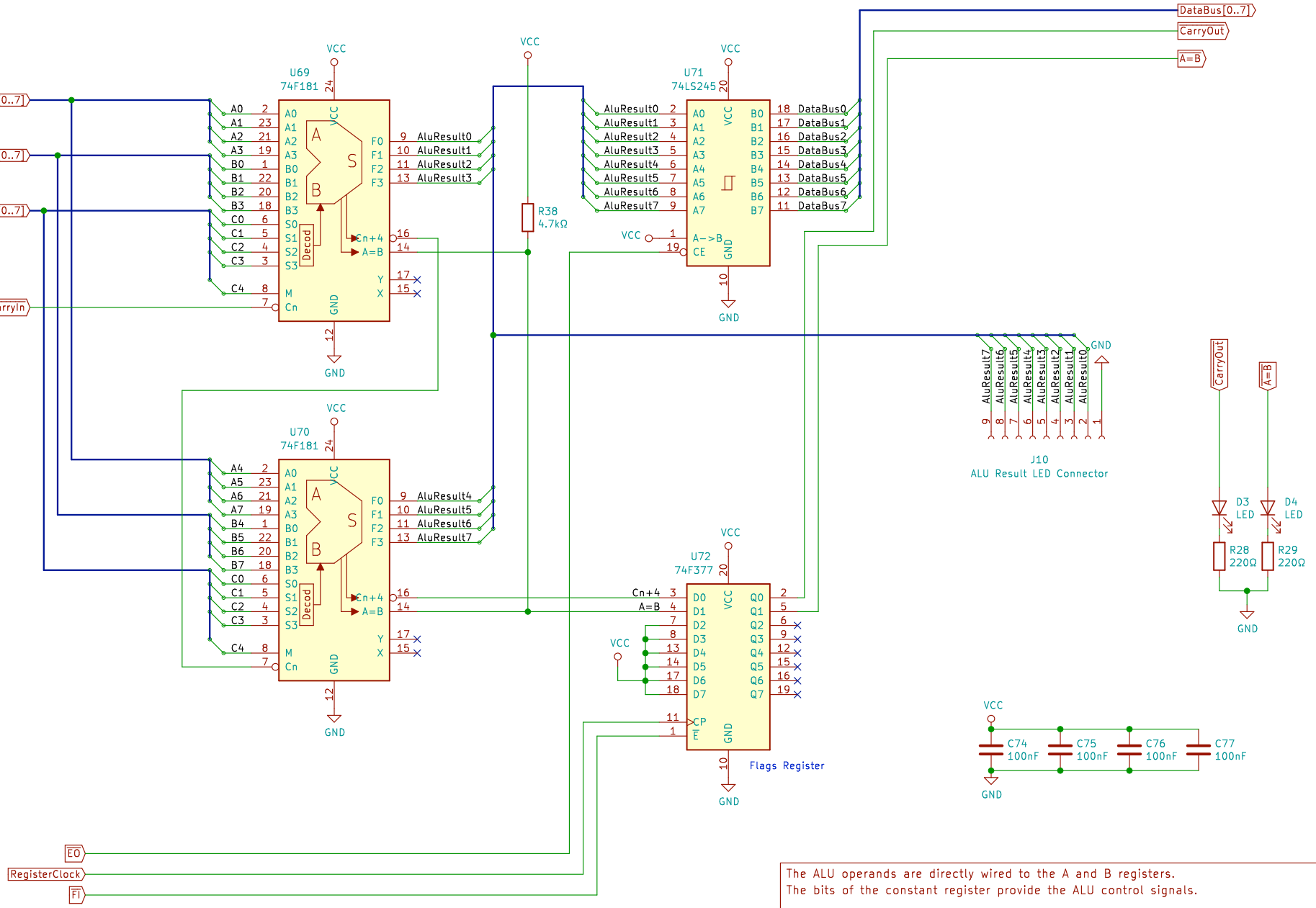


Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

Title: Register B

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 17/23

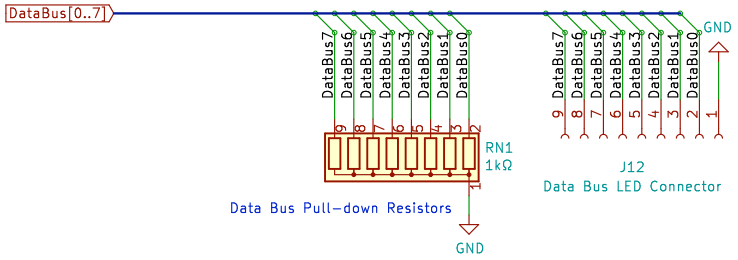


The ALU operands are directly wired to the A and B registers.
The bits of the constant register provide the ALU control signals.

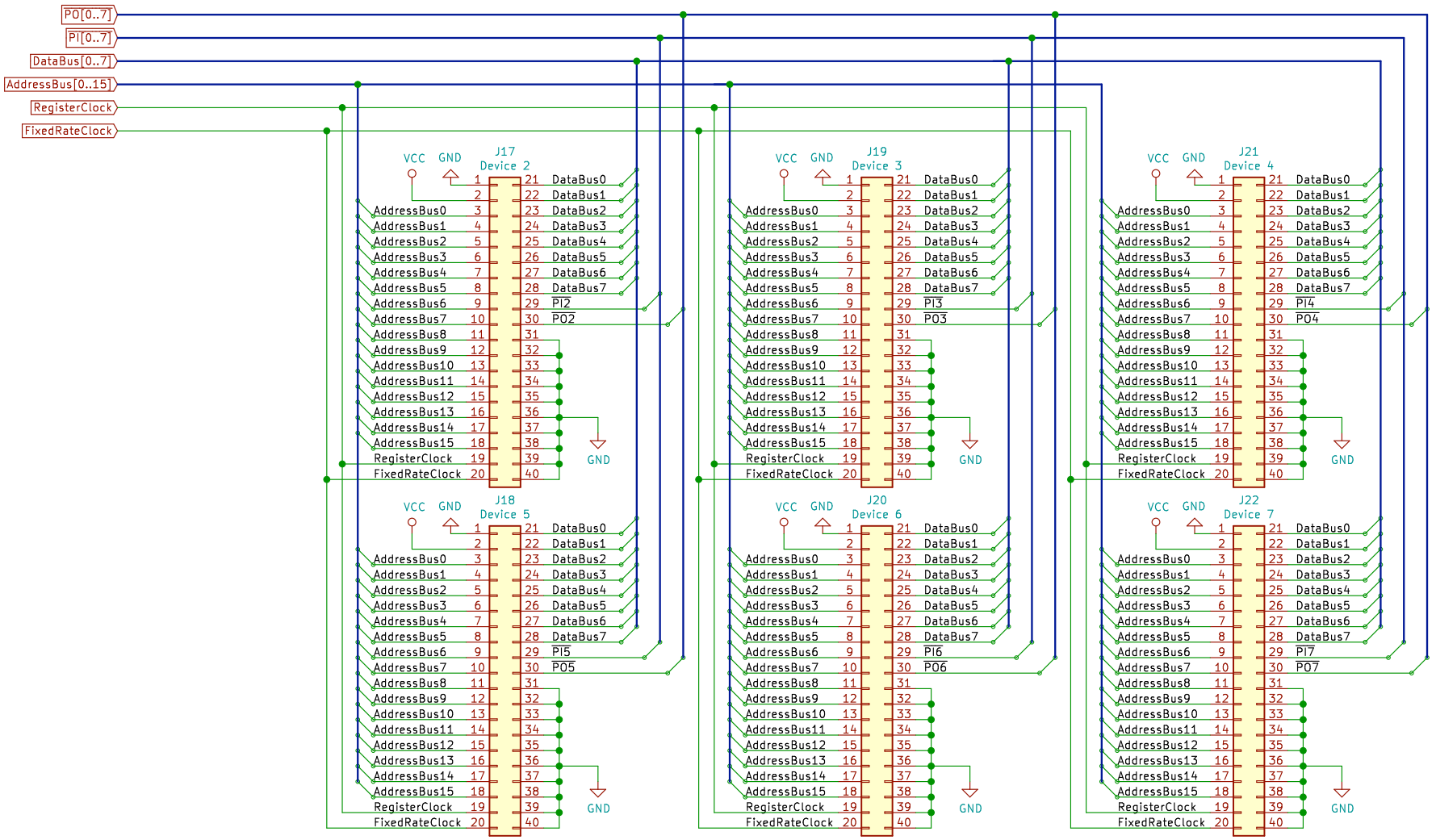
Sheet: /ALU/
File: ALU.sch

Title: ALU

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 18/23



Sheet: /Bus Display/		
File: Bus Display.sch		
Title: Bus Display		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 19/23

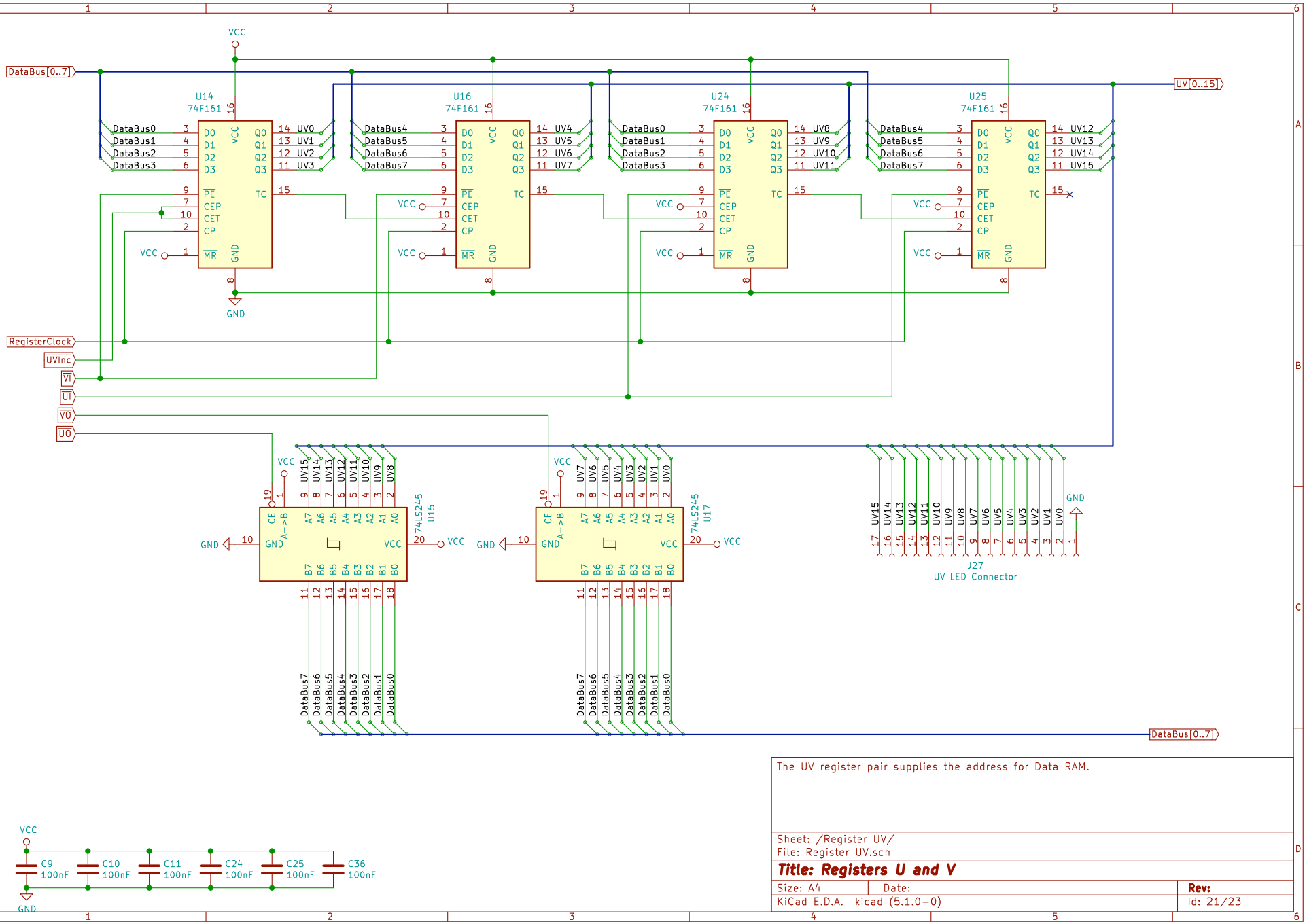


TurtleTTL provides several connectors for expansion cards.

Sheet: /Expansion/
File: Expansion.sch

Title: Expansion

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 20/23

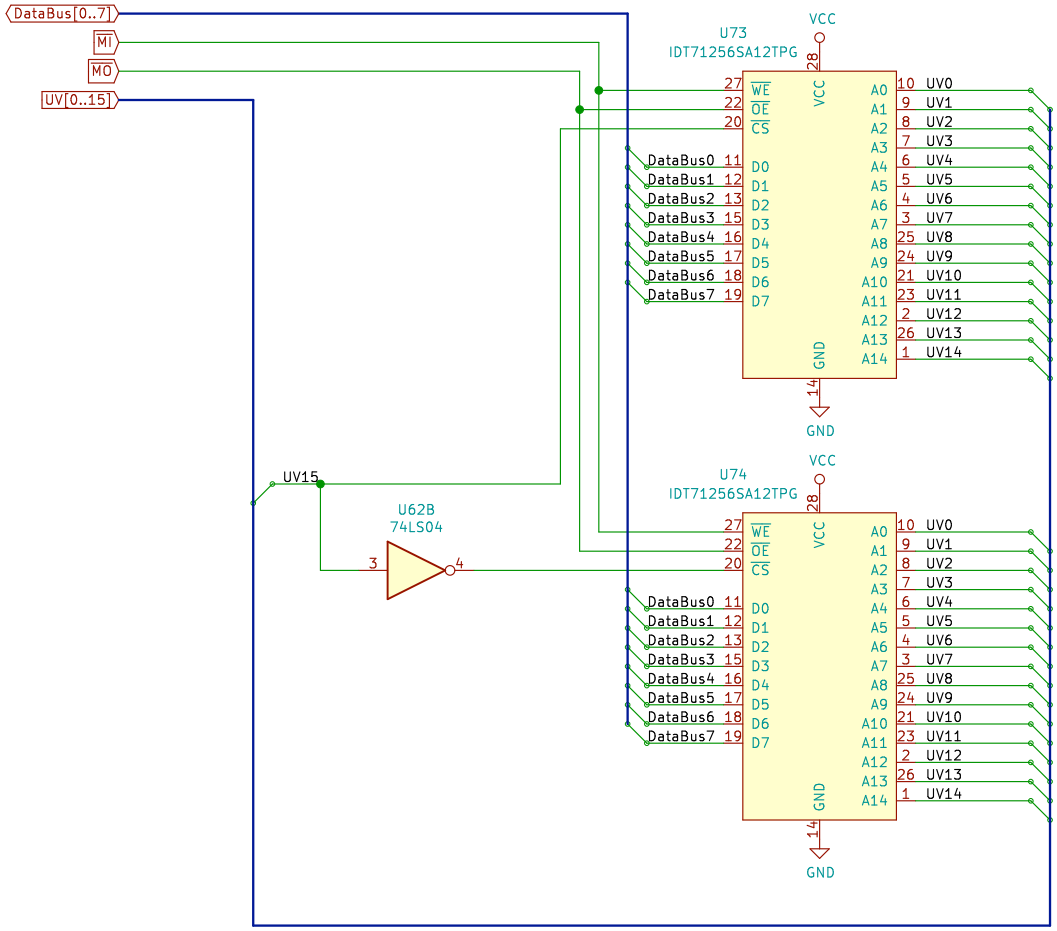


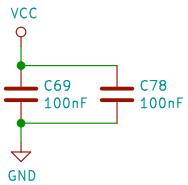
The UV register pair supplies the address for Data RAM.

Sheet: /Register UV/
File: Register UV.sch

Title: Registers U and V

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 21/23





64KB Data RAM

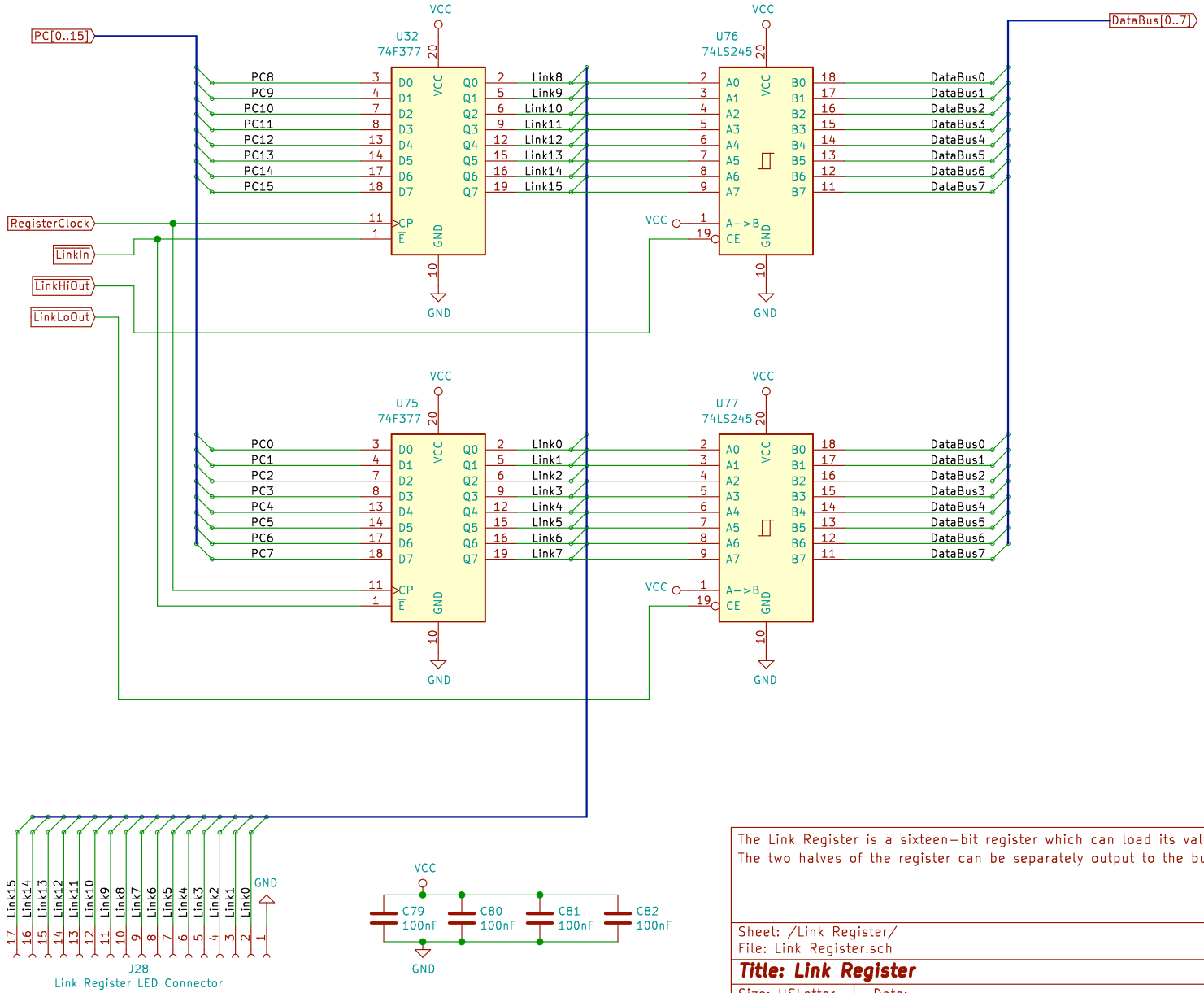
The MSB of the address selects between two 32KB SRAM ICs.

Sheet: /Data RAM/

File: Data RAM.sch

Title: Data RAM

Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 22/23



The Link Register is a sixteen-bit register which can load its value from PC.
The two halves of the register can be separately output to the bus.

Sheet: /Link Register/	
File: Link Register.sch	
Title: Link Register	
Size: USLetter Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)	Id: 23/23