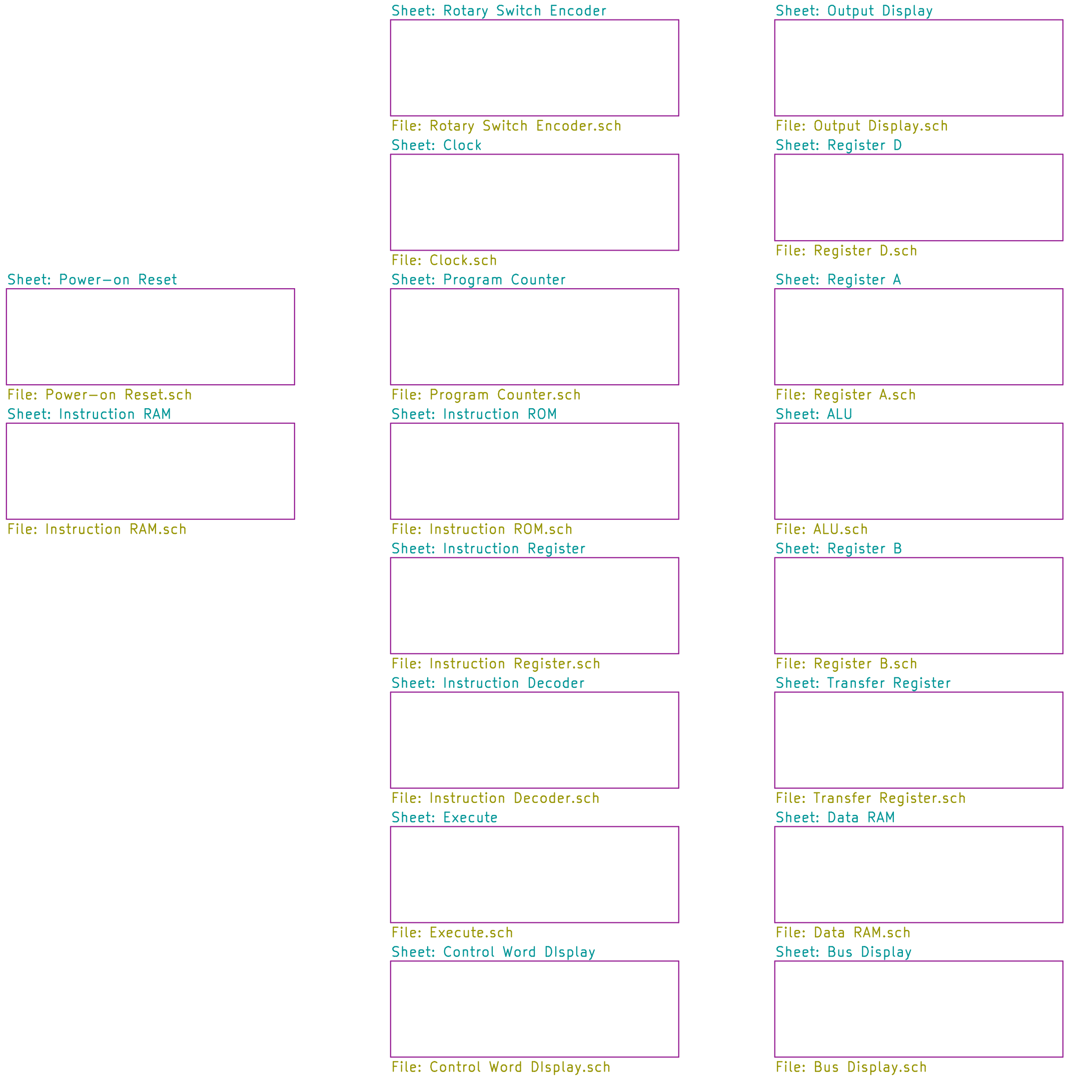
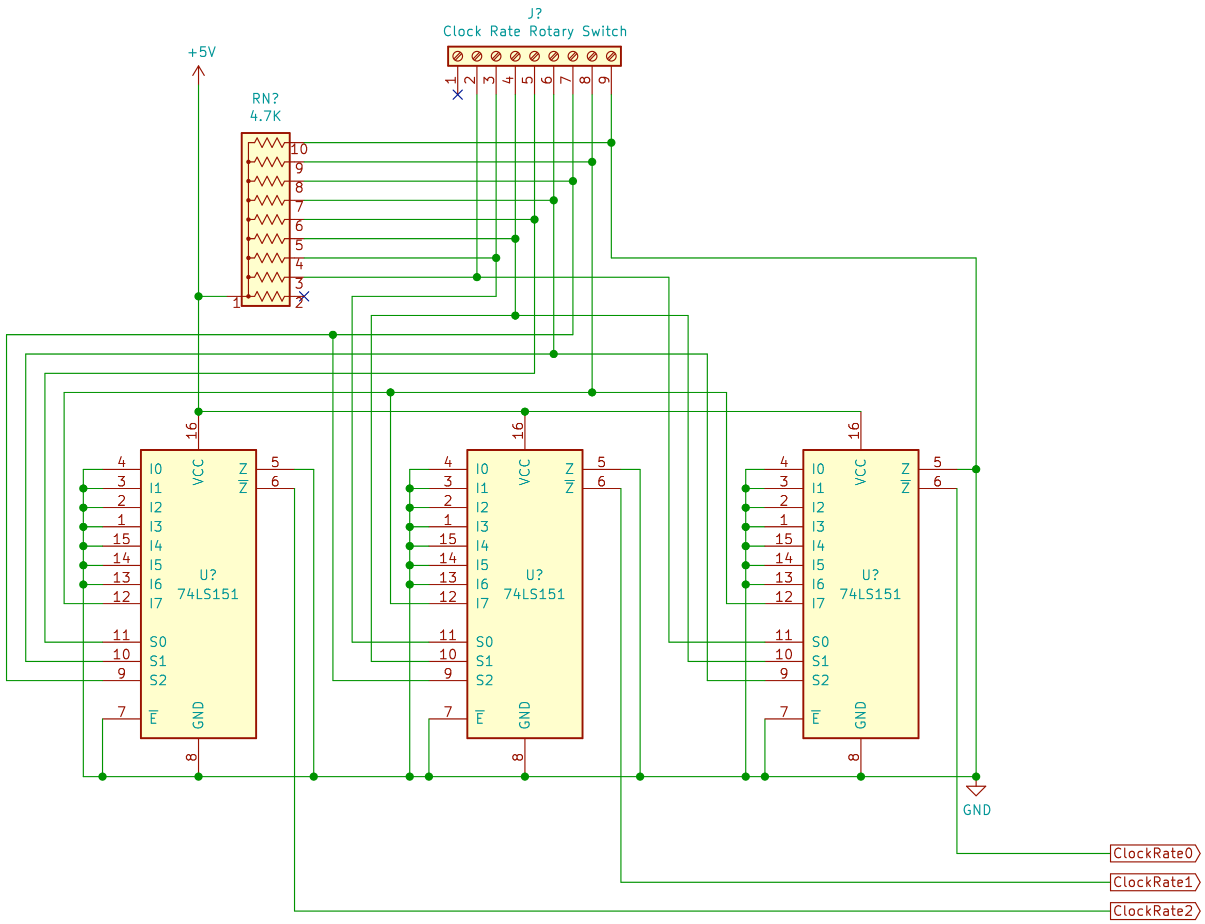

Sheet: Rotary Switch Encoder
File: Rotary Switch Encoder.sch
Sheet: Output Display
File: Output Display.sch
Sheet: Clock
File: Clock.sch
Sheet: Register D
File: Register D.sch
Sheet: Power–on Reset
File: Power–on Reset.sch
Sheet: Program Counter
File: Program Counter.sch
Sheet: Register A
File: Register A.sch
Sheet: Instruction RAM
File: Instruction RAM.sch
Sheet: Instruction ROM
File: Instruction ROM.sch
Sheet: ALU
File: ALU.sch
Sheet: Instruction Register
File: Instruction Register.sch
Sheet: Register B
File: Register B.sch
Sheet: Instruction Decoder
File: Instruction Decoder.sch
Sheet: Transfer Register
File: Transfer Register.sch
Sheet: Execute
File: Execute.sch
Sheet: Data RAM
File: Data RAM.sch
Sheet: Control Word DIsplay
File: Control Word DIsplay.sch
Sheet: Bus Display
File: Bus Display.sch

Sheet: /
File: Firenze.sch

Title: Firenze

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0–0)
Id: 1/19

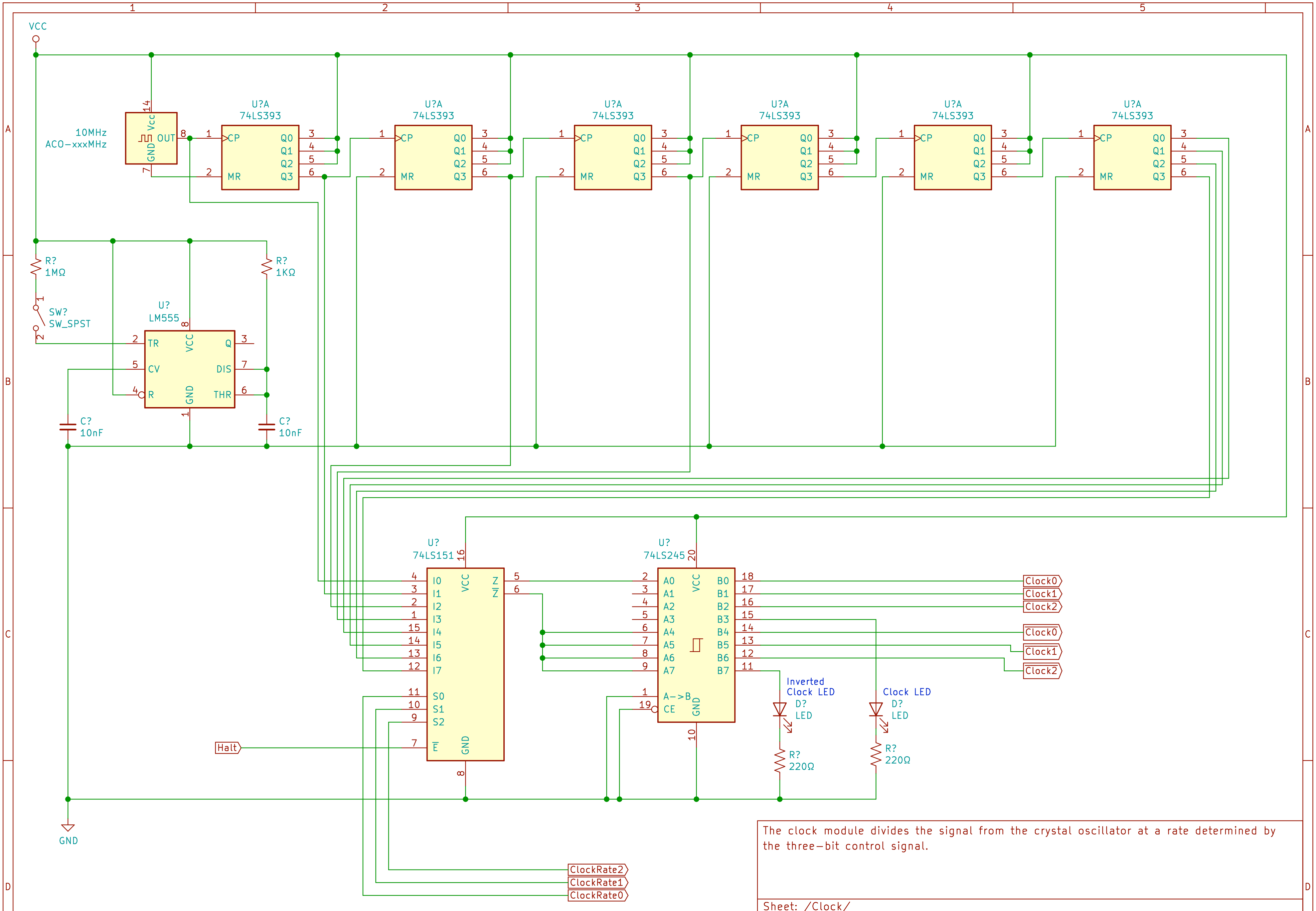

J?
Clock Rate Rotary Switch
1 2 3 4 5 6 7 8 9
+5V
RN?
4.7K
1 2 3 4 5 6 7 8 9 10
U?
74LS151
I0 I1 I2 I3 I4 I5 I6 I7
S0 S1 S2
E
VCC
GND
Z
Z
U?
74LS151
U?
74LS151
GND
ClockRate0
ClockRate1
ClockRate2

The clock rate rotary switch (connected via a screw terminal) is wired to three 74LS151 chips to translate the switch position to a three-bit value to control the clock rate.

Sheet: /Rotary Switch Encoder/
File: Rotary Switch Encoder.sch

Title: Rotary Switch Encoder

Size: USLetter Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 2/19

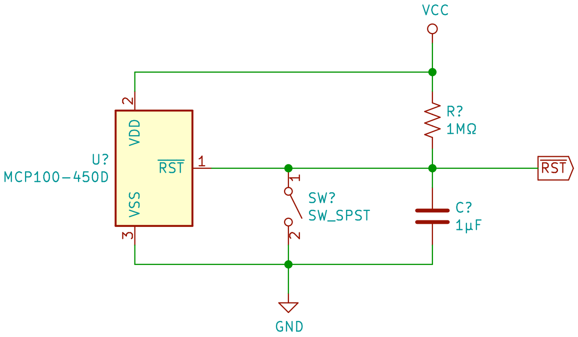

1
2
3
4
5
A
B
C
D
VCC
10MHz
ACO−xxxMHz
14
Vcc
OUT
8
GND
7
U?A
74LS393
1
CP
2
MR
Q0
Q1
Q2
Q3
3
4
5
6
R?
1MΩ
SW?
SW_SPST
1
2
U?
LM555
8
TR
VCC
Q
3
5
CV
DIS
7
4
R
GND
THR
6
1
R?
1KΩ
C?
10nF
C?
10nF
U?
74LS151
16
4
I0
VCC
Z
5
3
I1
Z̄
6
2
I2
1
I3
15
I4
14
I5
13
I6
12
I7
11
S0
10
S1
9
S2
Halt
7
Ē
GND
8
U?
74LS245
20
2
A0
VCC
B0
18
3
A1
B1
17
4
A2
B2
16
5
A3
B3
15
6
A4
B4
14
7
A5
B5
13
8
A6
B6
12
9
A7
B7
11
1
A−>B
19
CE
GND
10
Clock0
Clock1
Clock2
Clock0
Clock1
Clock2
Inverted
Clock LED
D?
LED
Clock LED
D?
LED
R?
220Ω
R?
220Ω
GND
ClockRate2
ClockRate1
ClockRate0

The clock module divides the signal from the crystal oscillator at a rate determined by the three−bit control signal.

Sheet: /Clock/
File: Clock.sch

Title: Clock

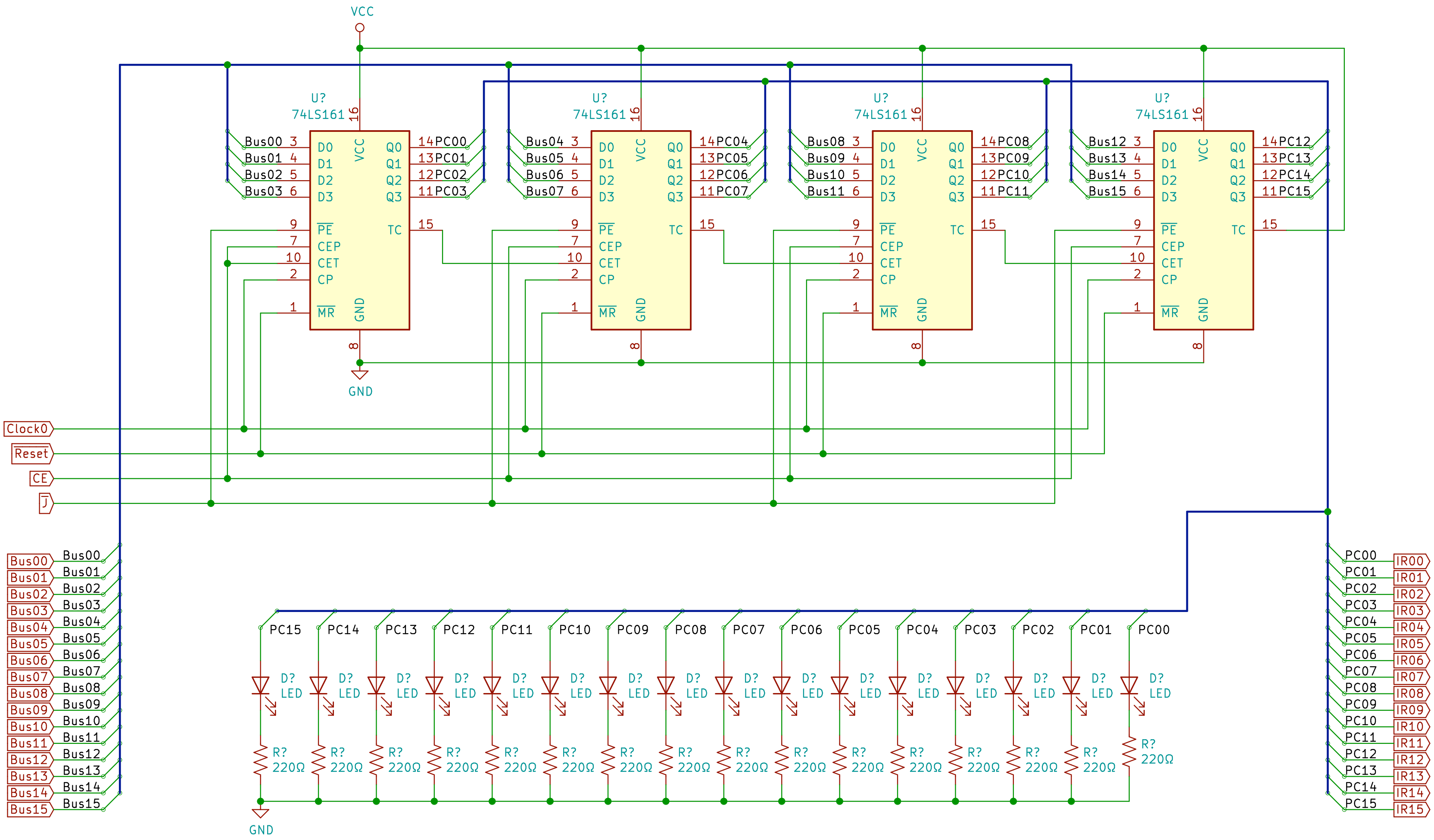
Size: A	Date:	**Rev:**
KiCad E.D.A. eeschema (5.1.0−0)		Id: 3/19


VCC
R?
1MΩ
U?
MCP100-450D
2
VDD
RST
1
VSS
3
SW?
SW_SPST
1
2
C?
1µF
RST
GND

Sheet: /Power-on Reset/
File: Power-on Reset.sch

Title: Power-on Reset

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 4/19



VCC
U?
74LS161
16
D0
D1
D2
D3
VCC
Q0
Q1
Q2
Q3
PE
CEP
CET
CP
TC
MR
GND
8
Bus00 3
Bus01 4
Bus02 5
Bus03 6
14PC00
13PC01
12PC02
11PC03
Bus04 3
Bus05 4
Bus06 5
Bus07 6
14PC04
13PC05
12PC06
11PC07
Bus08 3
Bus09 4
Bus10 5
Bus11 6
14PC08
13PC09
12PC10
11PC11
Bus12 3
Bus13 4
Bus14 5
Bus15 6
14PC12
13PC13
12PC14
11PC15
9
7
10
2
1
15
GND
Clock0
Reset
CE
J
Bus00
Bus01
Bus02
Bus03
Bus04
Bus05
Bus06
Bus07
Bus08
Bus09
Bus10
Bus11
Bus12
Bus13
Bus14
Bus15
PC15
PC14
PC13
PC12
PC11
PC10
PC09
PC08
PC07
PC06
PC05
PC04
PC03
PC02
PC01
PC00
D?
LED
R?
220Ω
PC00
PC01
PC02
PC03
PC04
PC05
PC06
PC07
PC08
PC09
PC10
PC11
PC12
PC13
PC14
PC15
IR00
IR01
IR02
IR03
IR04
IR05
IR06
IR07
IR08
IR09
IR10
IR11
IR12
IR13
IR14
IR15

Sheet: /Program Counter/
File: Program Counter.sch

Title: Program Counter

Size: A Date: **Rev:**

KiCad E.D.A. eeschema (5.1.0-0) Id: 5/19

Sheet: /Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 6/19

Sheet: /Instruction RAM/
File: Instruction RAM.sch

Title: Instruction RAM

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 7/19

Sheet: /Instruction Decoder/
File: Instruction Decoder.sch

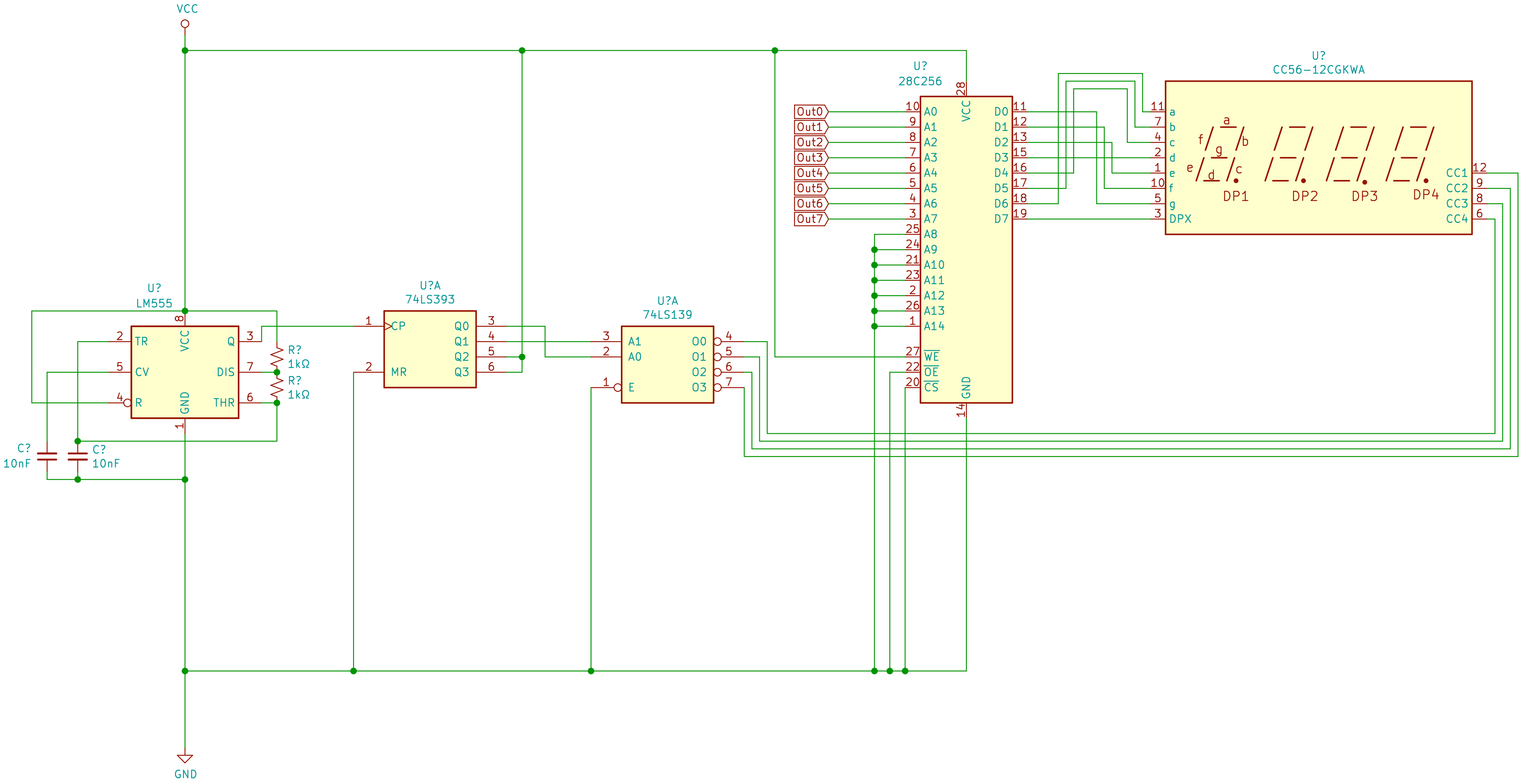
Title: Instruction Decoder

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 8/19

Sheet: /Execute/
File: Execute.sch

Title: Execute

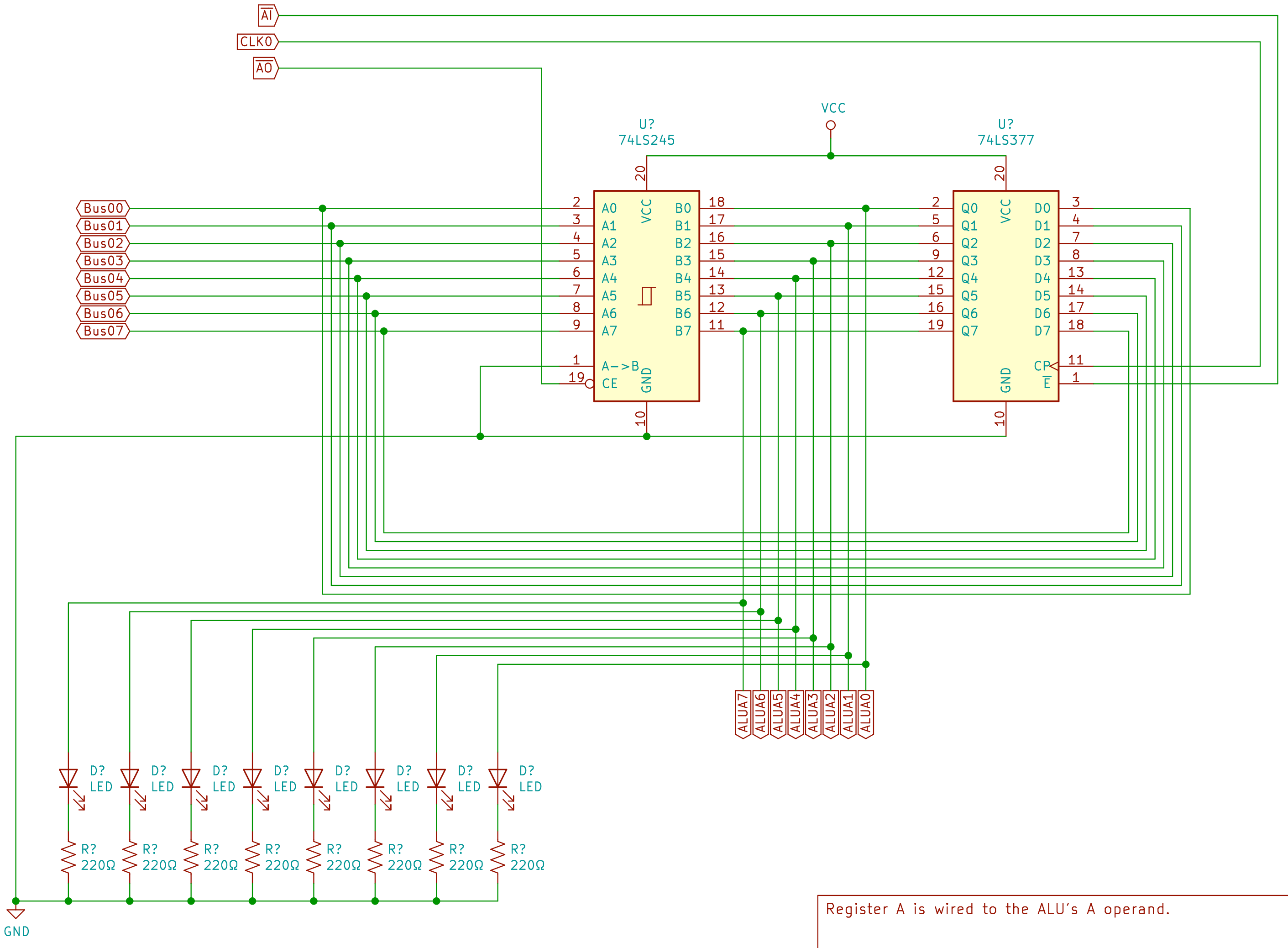
Size: A Date: **Rev:**
KiCad E.D.A. eeschema (5.1.0-0) Id: 9/19


VCC
U?
LM555
TR
CV
R
VCC
GND
Q
DIS
THR
R?
1kΩ
R?
1kΩ
C?
10nF
C?
10nF
GND
U?A
74LS393
CP
MR
Q0
Q1
Q2
Q3
U?A
74LS139
A1
A0
E
O0
O1
O2
O3
U?
28C256
Out0
Out1
Out2
Out3
Out4
Out5
Out6
Out7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
WE
OE
CS
VCC
GND
D0
D1
D2
D3
D4
D5
D6
D7
U?
CC56-12CGKWA
a
b
c
d
e
f
g
DPX
DP1
DP2
DP3
DP4
CC1
CC2
CC3
CC4

Sheet: /Output Display/
File: Output Display.sch

Title: Output Display

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 10/19


AI
CLK0
AO
Bus00
Bus01
Bus02
Bus03
Bus04
Bus05
Bus06
Bus07
VCC
U?
74LS245
U?
74LS377
20
A0
A1
A2
A3
A4
A5
A6
A7
A->B
CE
B0
B1
B2
B3
B4
B5
B6
B7
VCC
GND
10
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
D0
D1
D2
D3
D4
D5
D6
D7
CP
E
ALUA7
ALUA6
ALUA5
ALUA4
ALUA3
ALUA2
ALUA1
ALUA0
D?
LED
R?
220Ω
GND

Register A is wired to the ALU's A operand.

Sheet: /Register A/
File: Register A.sch

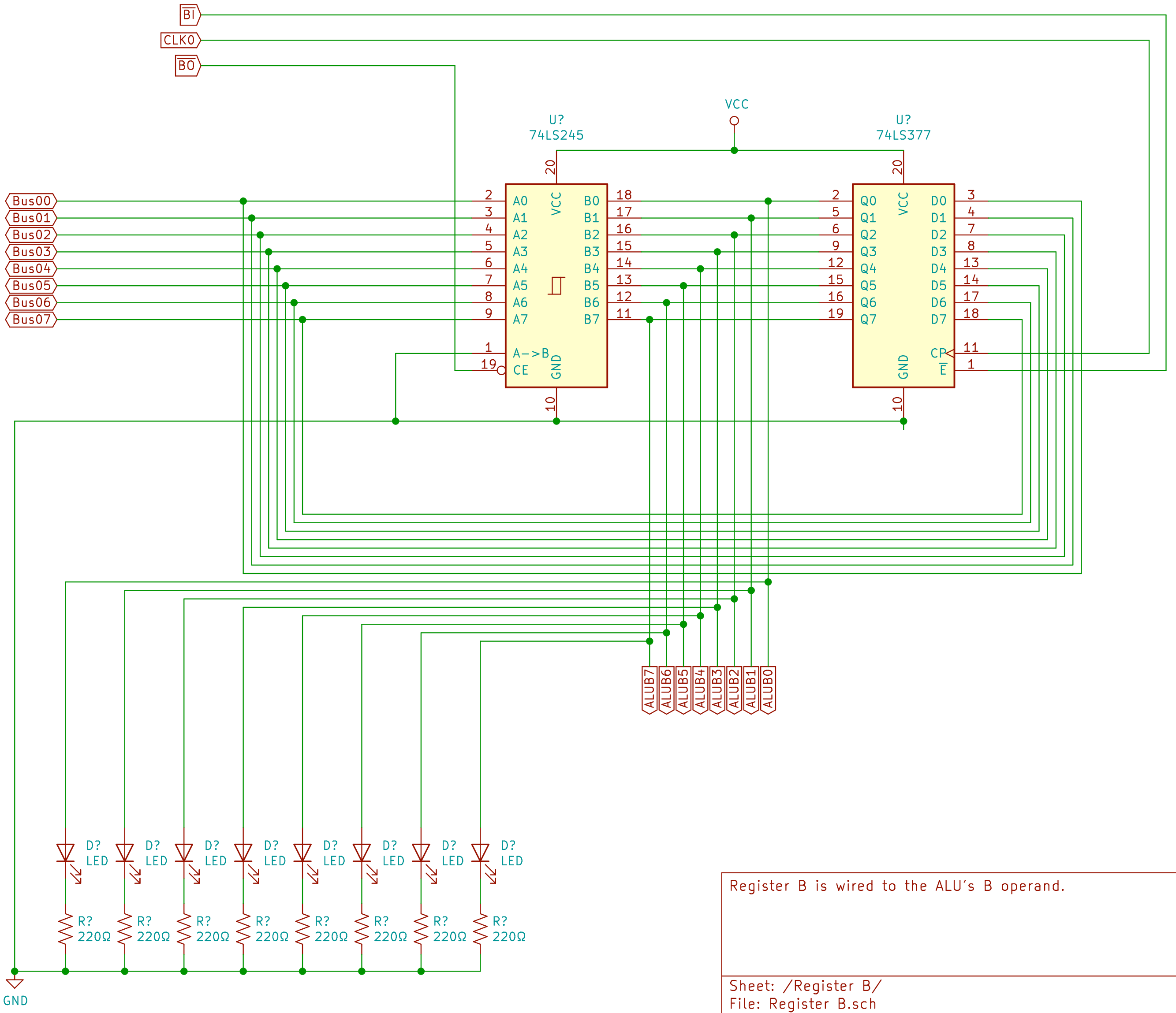
Title: Register A

Size: A	Date:	**Rev:**
KiCad E.D.A. eeschema (5.1.0-0)		Id: 11/19

Sheet: /ALU/
File: ALU.sch

Title: ALU

Size: A	Date:	**Rev:**
KiCad E.D.A. eeschema (5.1.0-0)		Id: 12/19


BI
CLKO
BO
VCC
U?
74LS245
U?
74LS377
Bus00
Bus01
Bus02
Bus03
Bus04
Bus05
Bus06
Bus07
A0
A1
A2
A3
A4
A5
A6
A7
A->B
CE
VCC
GND
B0
B1
B2
B3
B4
B5
B6
B7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
D0
D1
D2
D3
D4
D5
D6
D7
CP
E
20
10
ALUB7
ALUB6
ALUB5
ALUB4
ALUB3
ALUB2
ALUB1
ALUB0
D?
LED
R?
220Ω
GND

Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

Title: Register B

Size: A Date: **Rev:**
KiCad E.D.A. eeschema (5.1.0-0) Id: 13/19

Sheet: /Transfer Register/
File: Transfer Register.sch

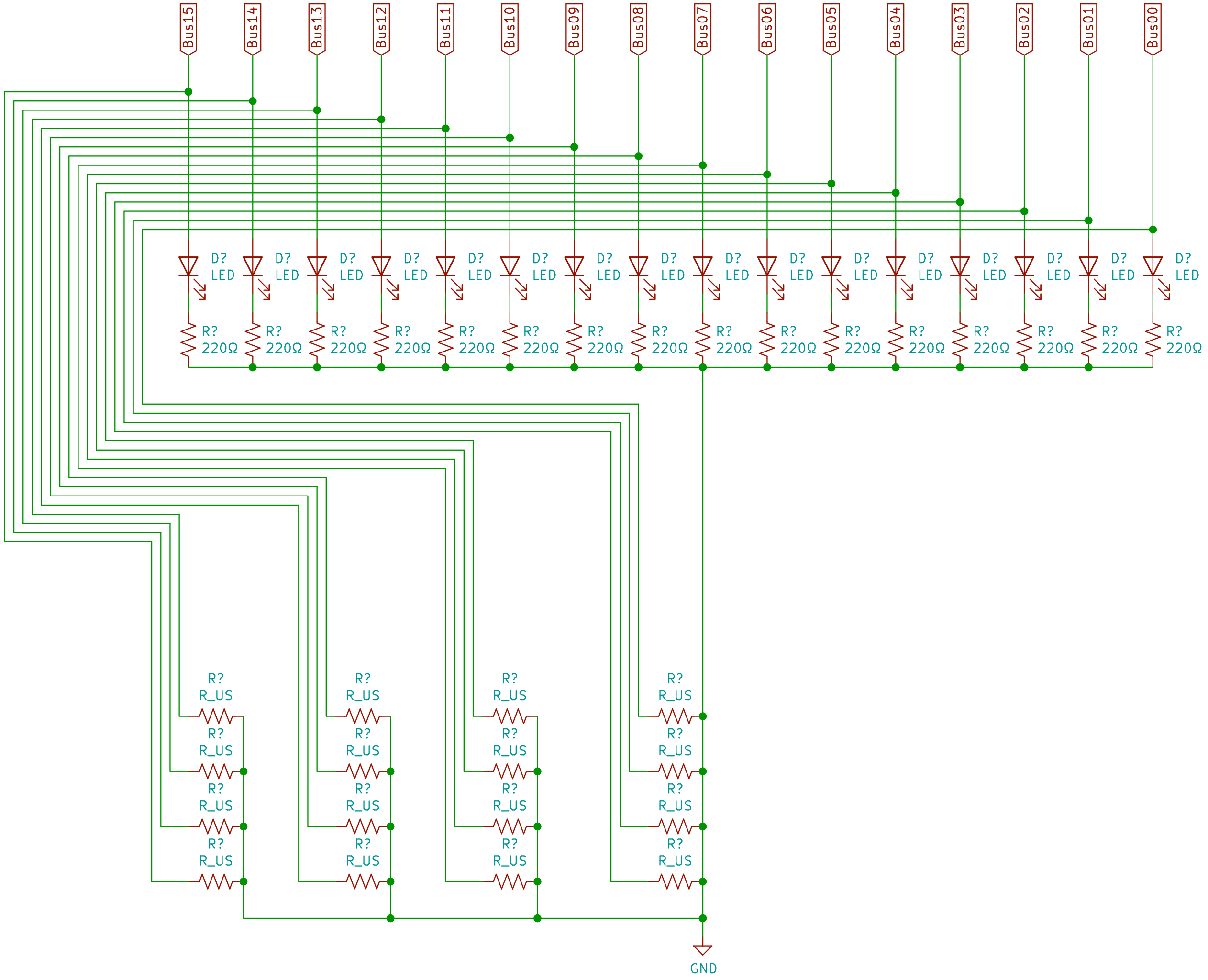
Title: Transfer Register

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 14/19

Sheet: /Data RAM/
File: Data RAM.sch

Title: Data RAM

Size: A	Date:	**Rev:**
KiCad E.D.A. eeschema (5.1.0-0)		Id: 15/19


Bus15
Bus14
Bus13
Bus12
Bus11
Bus10
Bus09
Bus08
Bus07
Bus06
Bus05
Bus04
Bus03
Bus02
Bus01
Bus00
D?
LED
R?
220Ω
R?
R_US
GND

Sheet: /Bus Display/
File: Bus Display.sch

Title: Bus Display

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 16/19

Sheet: /Control Word DIsplay/
File: Control Word DIsplay.sch

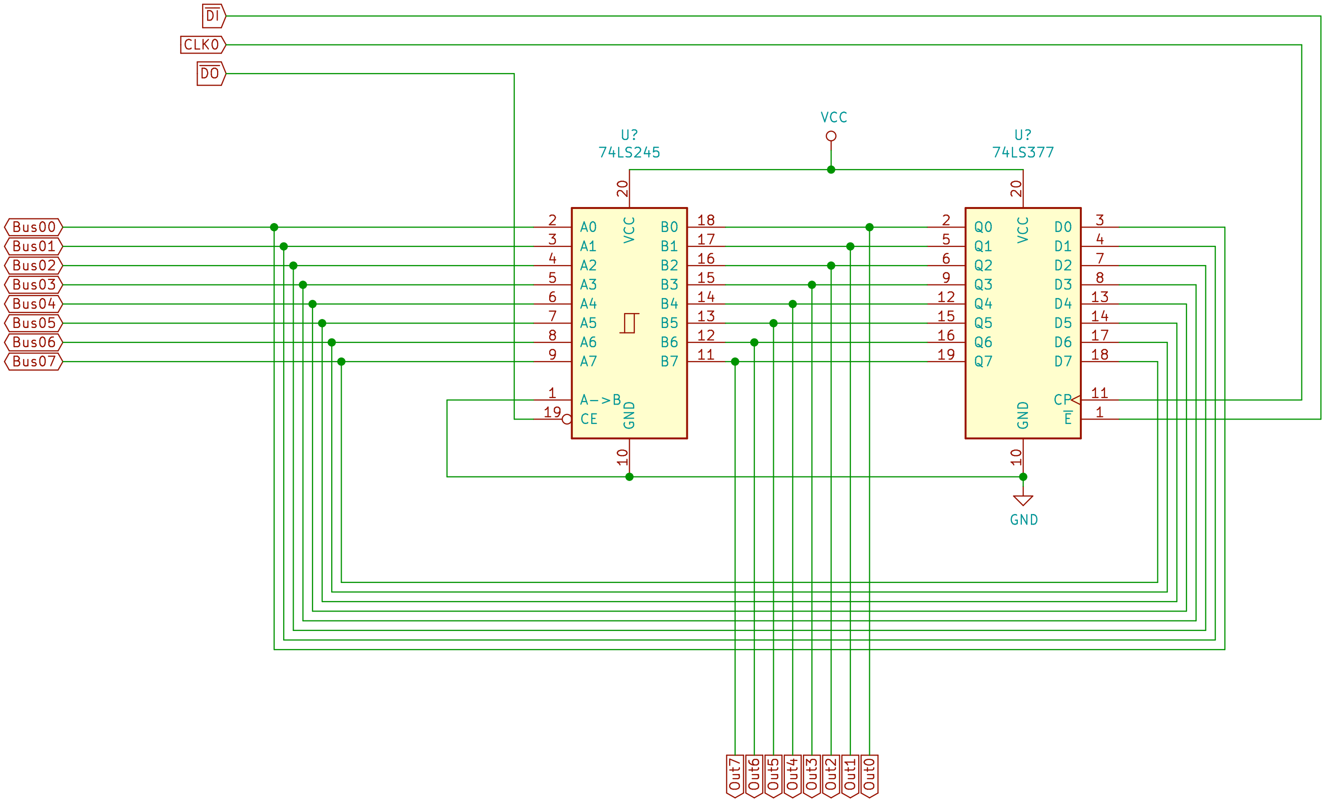
Title: Control Word Display

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 17/19

Sheet: /Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 18/19


DI
CLKO
DO
Bus00
Bus01
Bus02
Bus03
Bus04
Bus05
Bus06
Bus07
U?
74LS245
VCC
U?
74LS377
20
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
A->B
CE
VCC
GND
10
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
D0 D1 D2 D3 D4 D5 D6 D7
CP
E
GND
Out7
Out6
Out5
Out4
Out3
Out2
Out1
Out0

Register D is wired directly to the Output Display Module.

Sheet: /Register D/
File: Register D.sch

Title: Register D

Size: A
Date:
Rev:
KiCad E.D.A. eeschema (5.1.0-0)
Id: 19/19