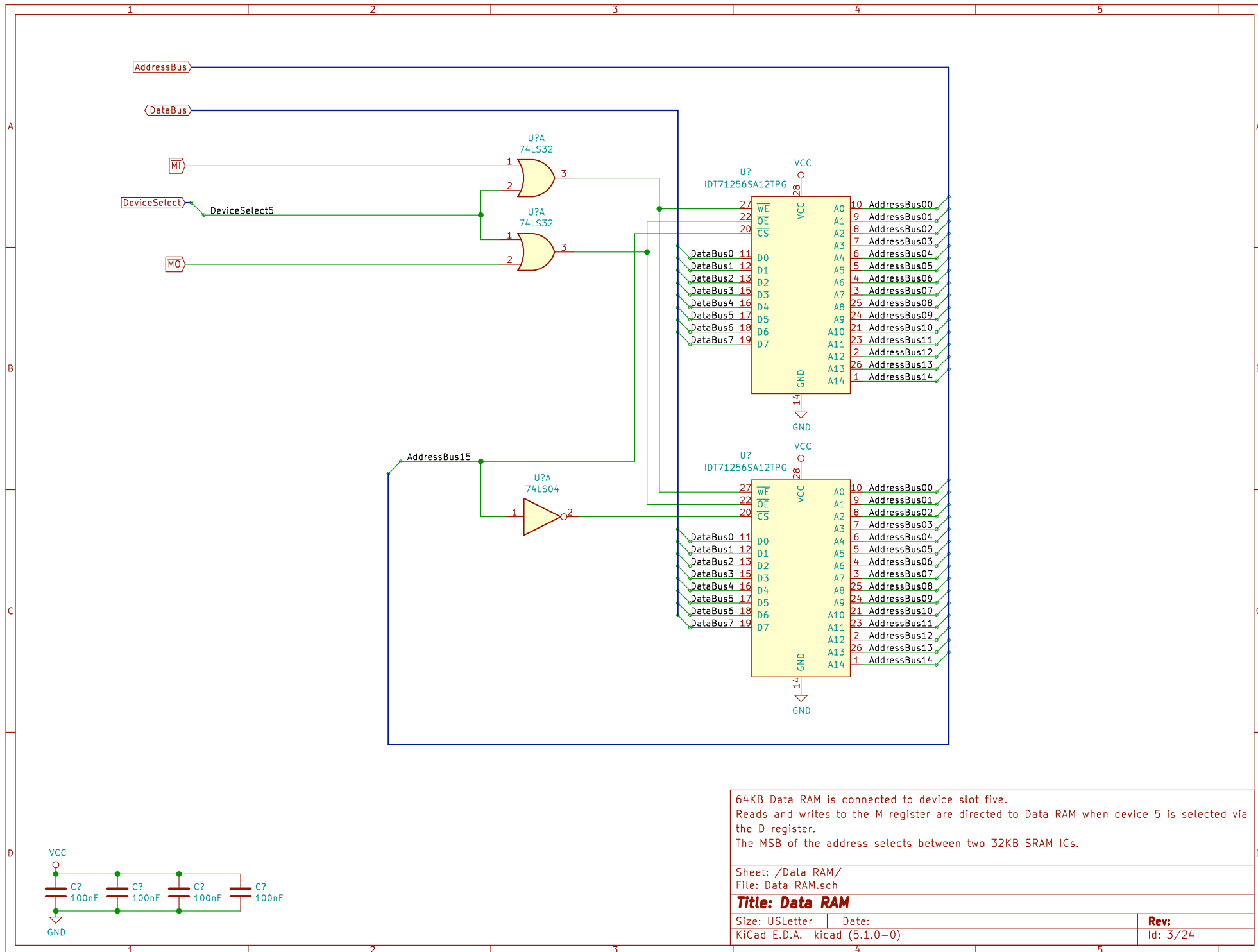


	1	2	3	4	5	
A		Sheet: Output Display File: Output Display.sch	Sheet: Register XY File: Register XY.sch Sheet: Program Counter	Sheet: Speed Control File: Speed Control.sch Sheet: Clock		A
B		Sheet: Data RAM File: Data RAM.sch Sheet: Serial	File: Program Counter.sch Sheet: Instruction Fetch	File: Clock.sch Sheet: Power-on Reset		B
C		File: Serial.sch Sheet: Register D	File: Instruction Fetch.sch Sheet: Instruction Decode	File: Power-on Reset.sch Sheet: Register A		C
		File: Register D.sch	File: Instruction Decode.sch Sheet: Execute	File: Register A.sch Sheet: Register B		
			File: Execute.sch Sheet: Bus Display	File: Register B.sch Sheet: ALU		
			File: Bus Display.sch	File: ALU.sch		
D						D
	1	2	3	4	5	

TTL microcomputer built from 74xx series logic chips.

Sheet: /	
File: TurtleTTL.sch	
Title: Turtle TTL	
Size: A	Date:
KiCad E.D.A. kicad (5.1.0-0)	
Rev:	
Id: 1/24	



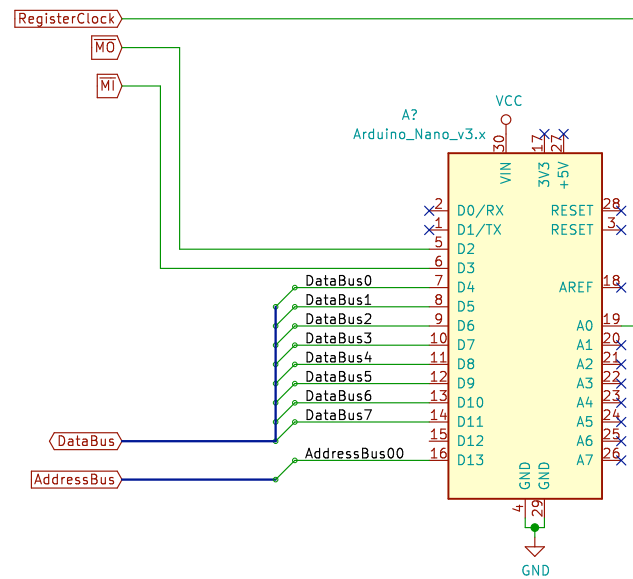
64KB Data RAM is connected to device slot five.
 Reads and writes to the M register are directed to Data RAM when device 5 is selected via the D register.
 The MSB of the address selects between two 32KB SRAM ICs.

Sheet: /Data RAM/
 File: Data RAM.sch

Title: Data RAM

Size: USLetter Date:
 KiCad E.D.A. kicad (5.1.0-0)

Rev:
 Id: 3/24



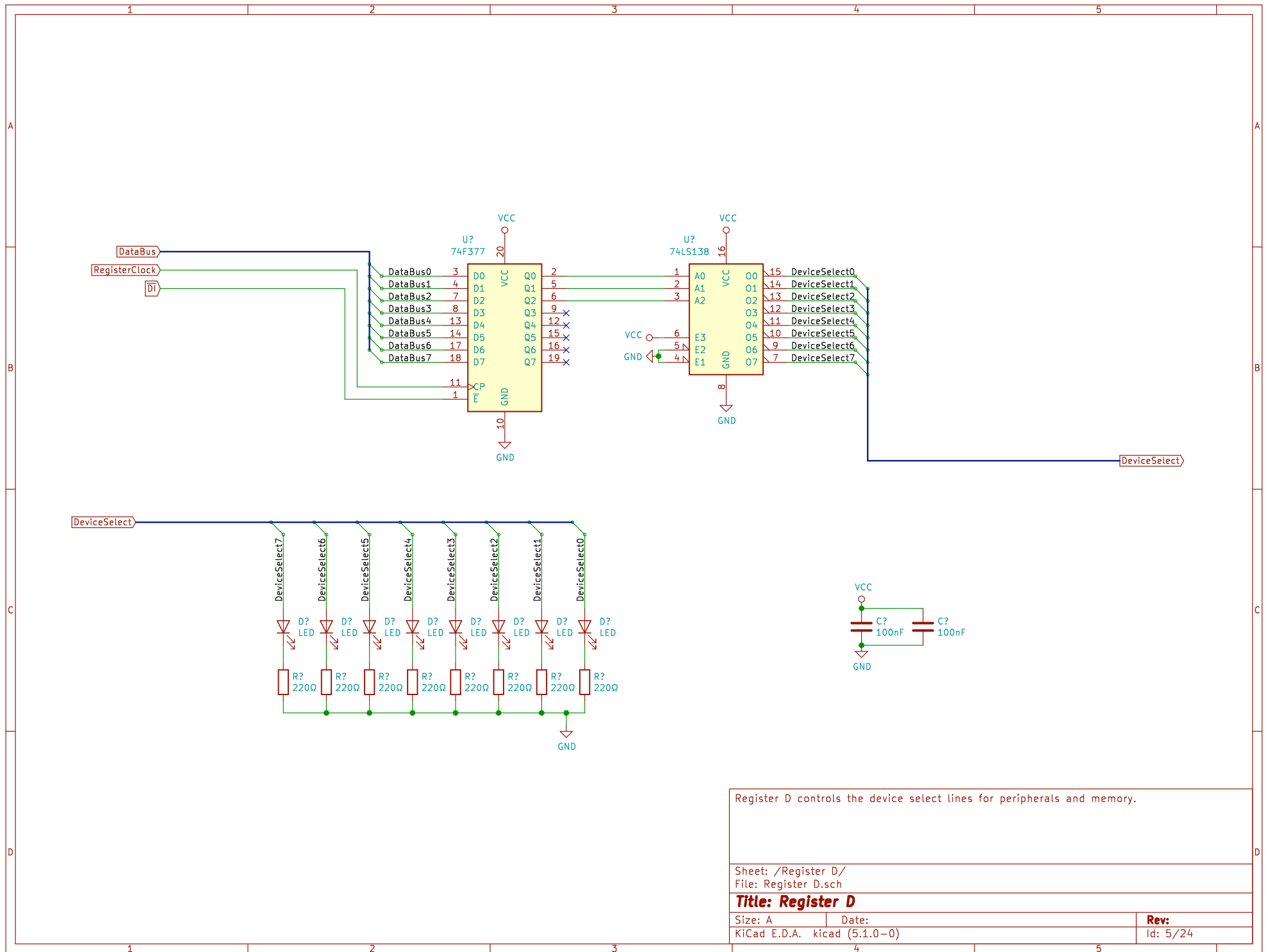
An Arduino Nano serves as a serial interface module.

Sheet: /Serial/
File: Serial.sch

Title: Serial I/O

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 4/24



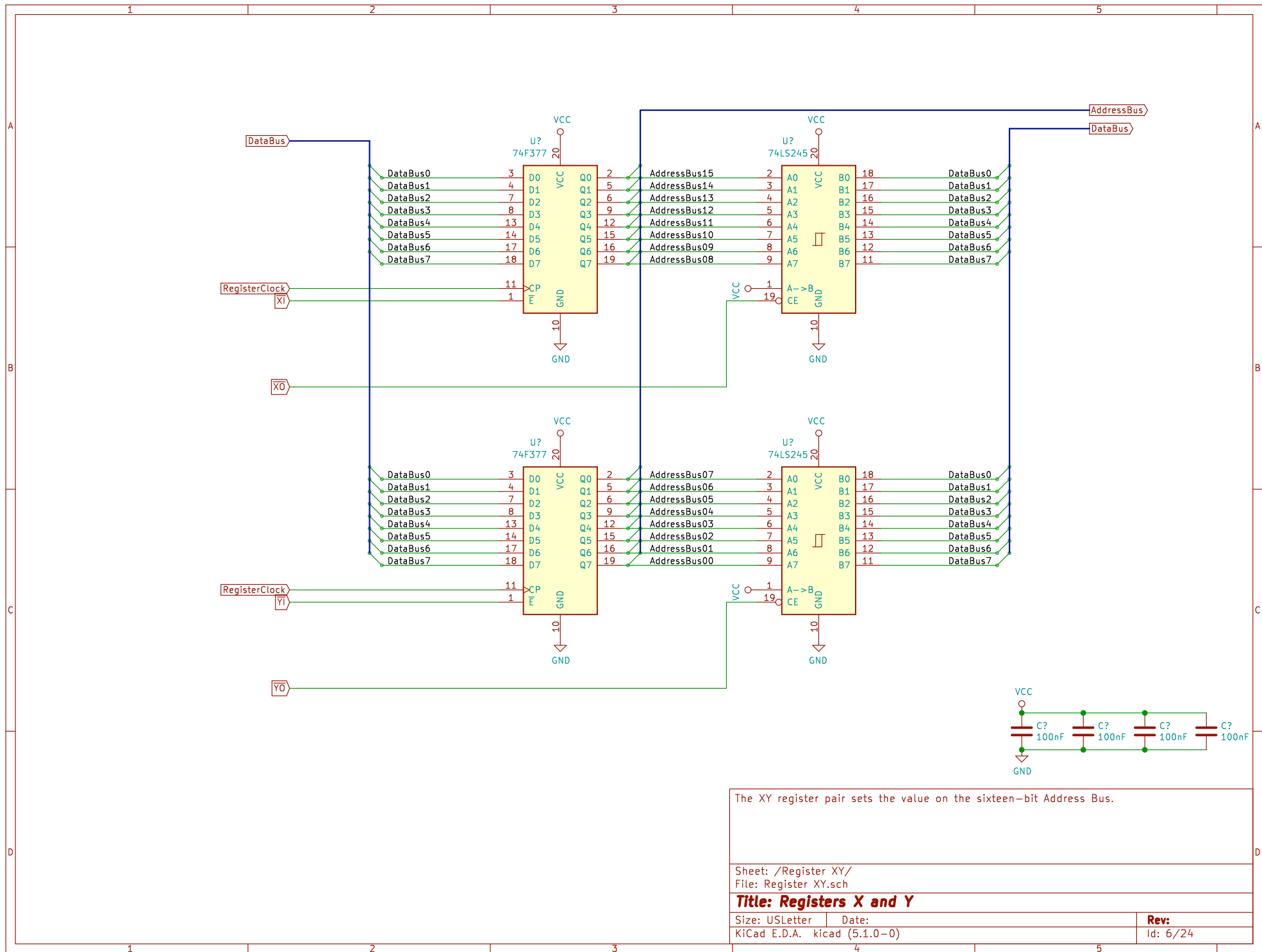
Register D controls the device select lines for peripherals and memory.

Sheet: /Register D/
File: Register D.sch

Title: Register D

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 5/24

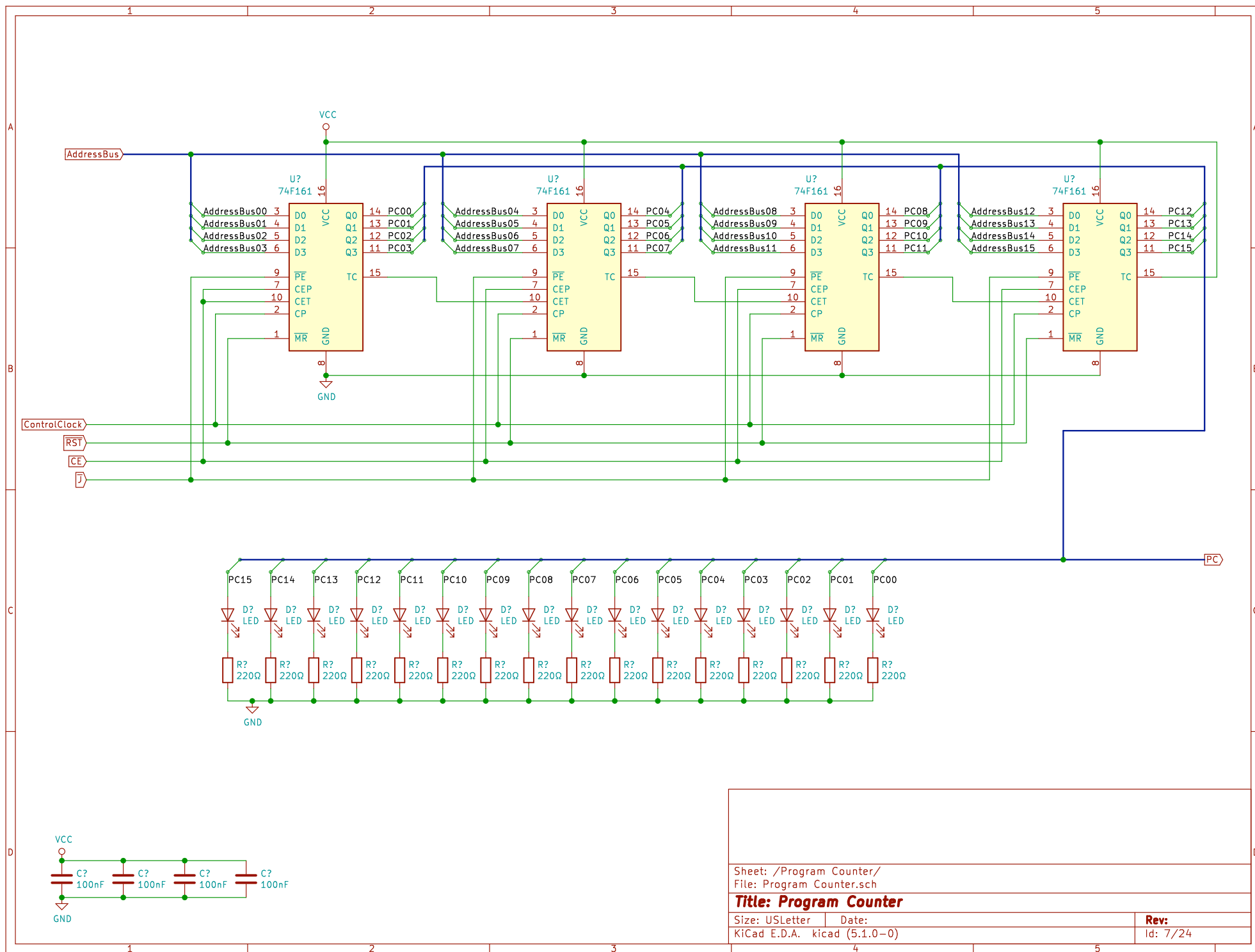


The XY register pair sets the value on the sixteen-bit Address Bus.

Sheet: /Register XY/
File: Register XY.sch

Title: Registers X and Y

Size: USLetter	Date:
KiCad E.D.A. kicad (5.1.0-0)	Rev: Id: 6/24



Sheet: /Program Counter/
File: Program Counter.sch

Title: Program Counter

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 7/24

1	2	3	4	5	6
A					A
B					B
C					C
D					D
1	2	3	4	5	6

Sheet: PC/IF

File: PC_IF.sch
Sheet: Instruction ROM

Sheet: Instruction RAM Address

File: Instruction RAM Address.sch
Sheet: Instruction RAM

File: Instruction ROM.sch
Sheet: Instruction Register

File: Instruction RAM.sch

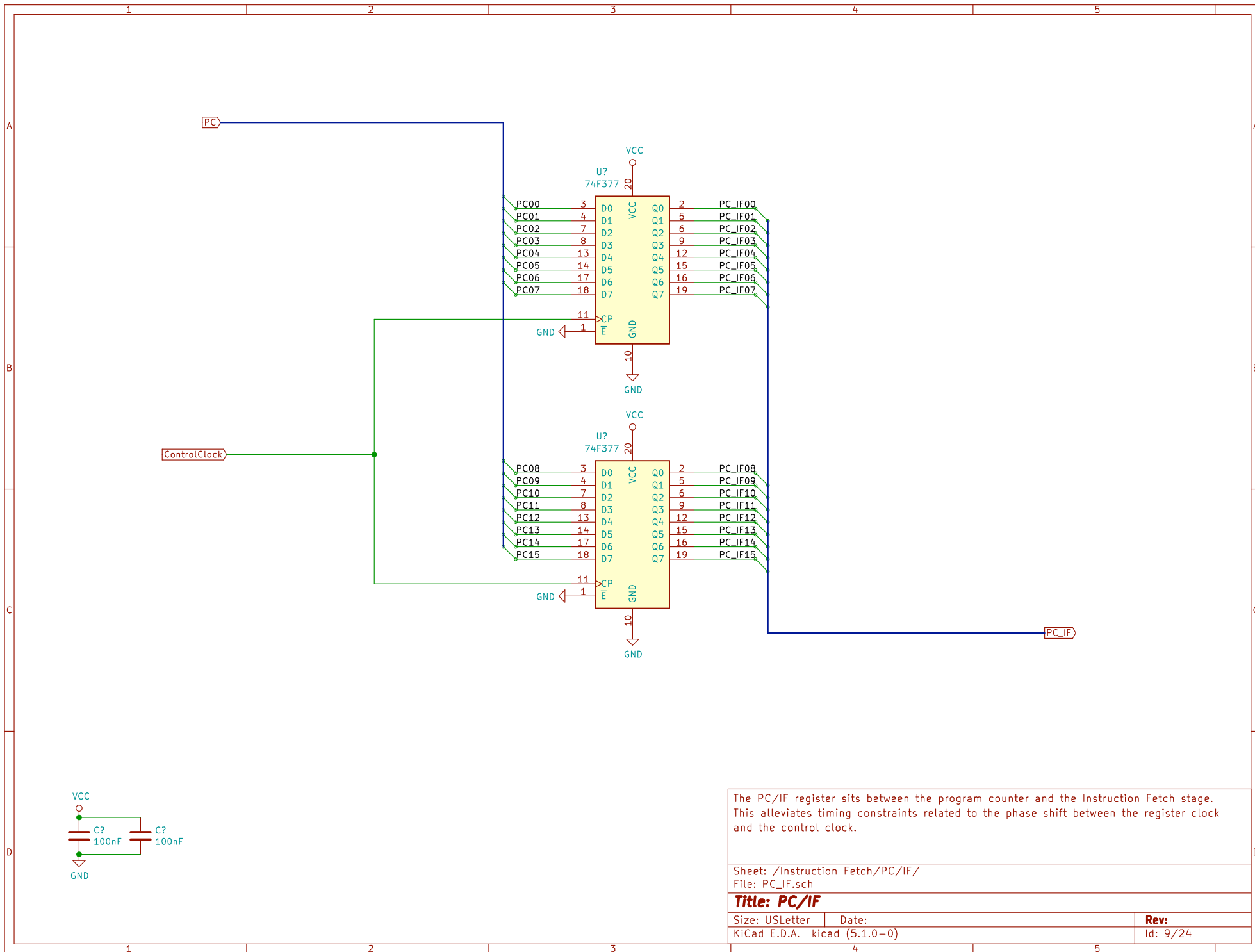
File: Instruction Register.sch

Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

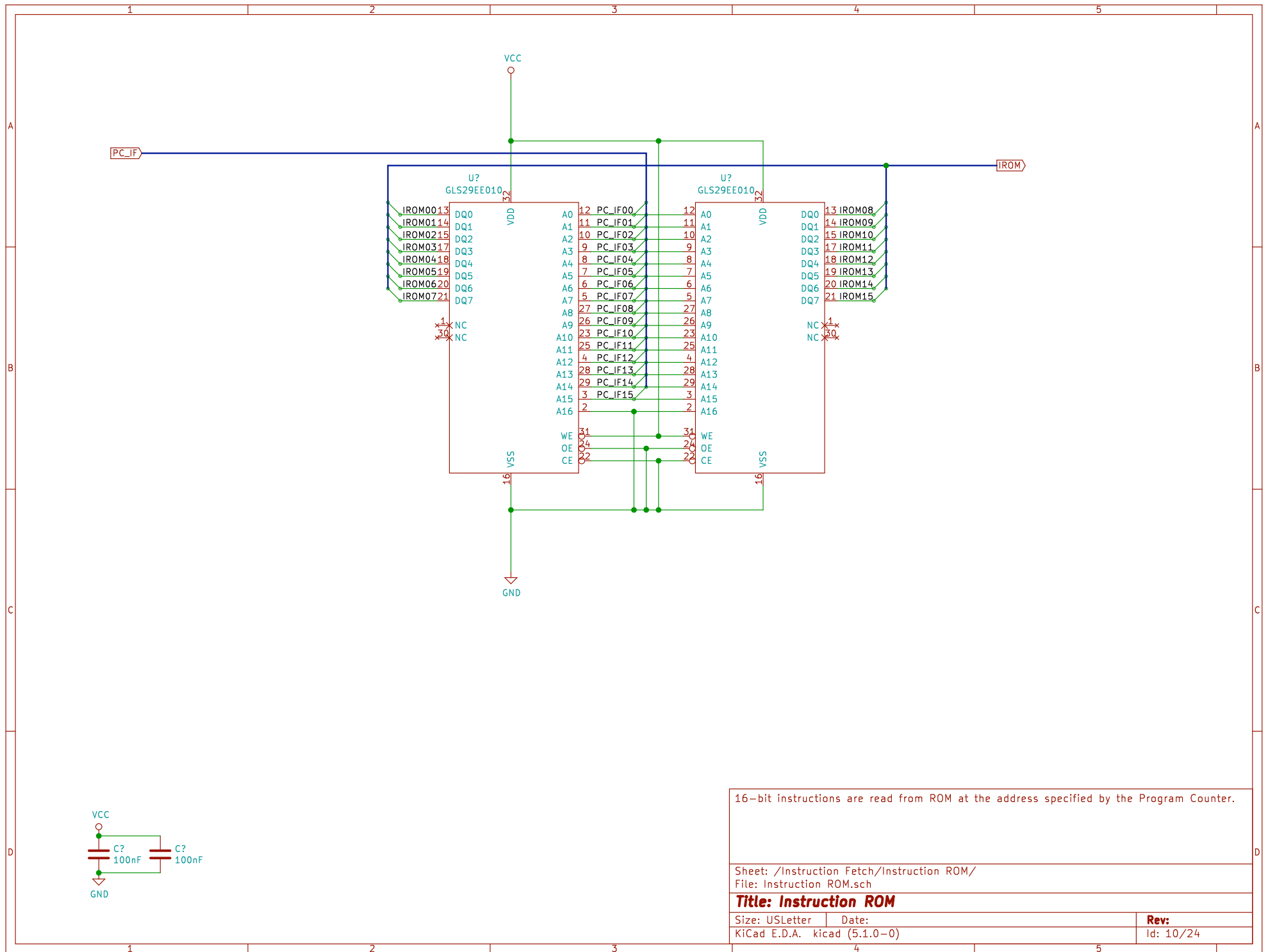
Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

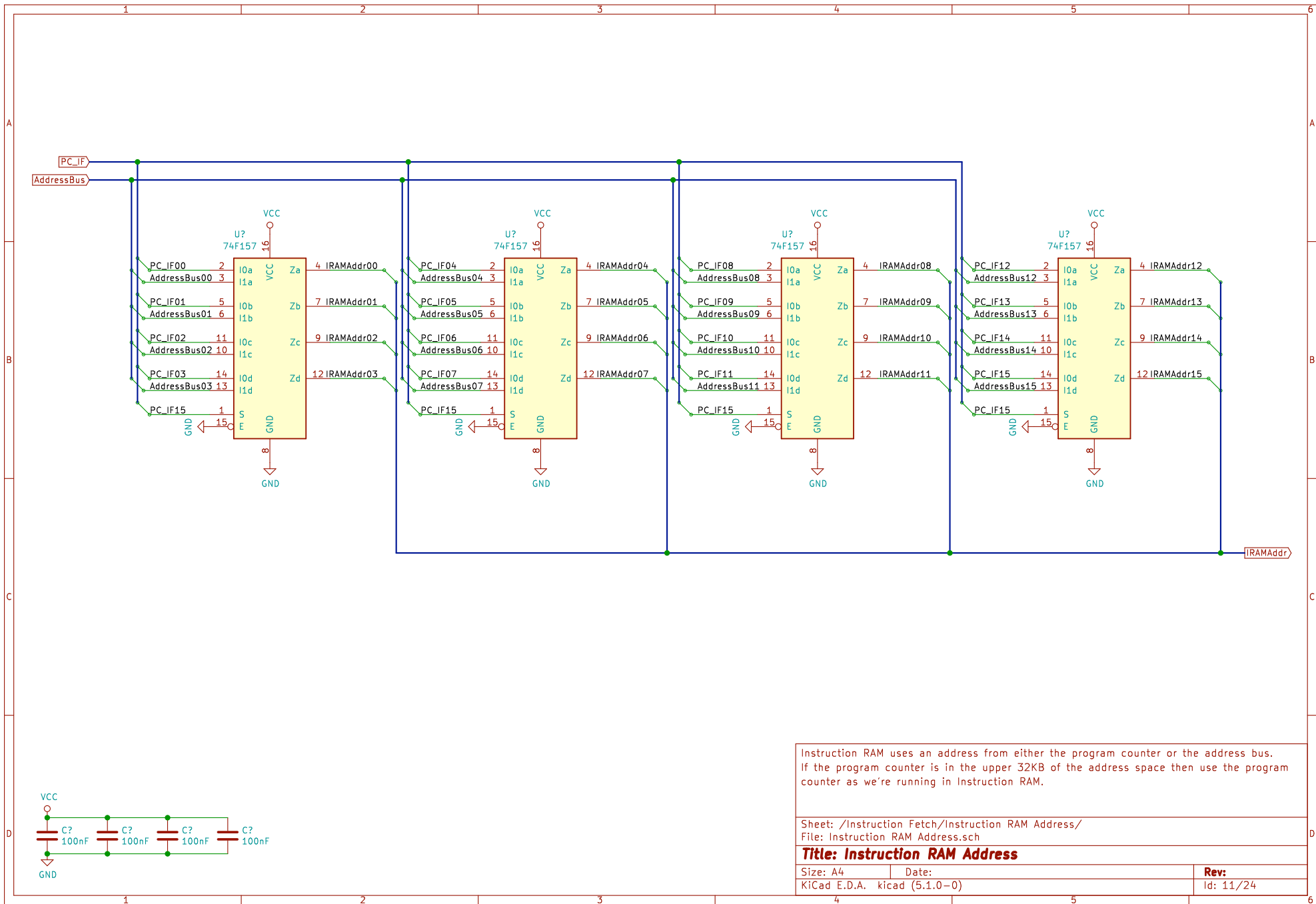
Title: Instruction Fetch

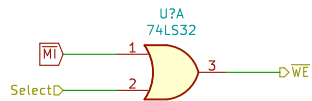
Size: A4	Date:	Rev:
KiCad E.D.A. - kicad (5.1.0-0)		Id: 8/24



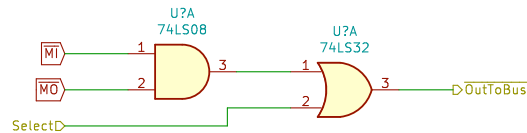
<p>The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.</p>	
<p>Sheet: /Instruction Fetch/PC/IF/ File: PC_IF.sch</p>	
<p>Title: PC/IF</p>	
Size: USLetter	Date:
KiCad E.D.A. kicad (5.1.0-0)	Rev: Id: 9/24





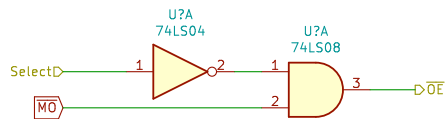


Only write to the Instruction SRAM when the MI signal is active and the appropriate plane of Instruction RAM is selected.



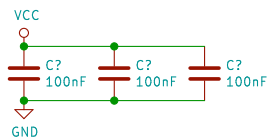
The bus transceiver should connect the Instruction SRAM to the Data Bus when the plane is selected and wither MO or MI is active.

The direction of the bus transceiver must also be set appropriately. This is done elsewhere.



Always output from Instruction SRAM when the plane of Instruction RAM is deselected. This allows RAM to be read for use in iF.

Else, if the plane is selected then only read from SRAM when the MO signal is active.

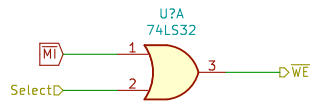


Logic for the control signals which drive Instruction RAM.

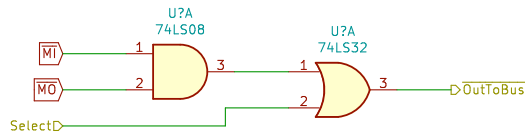
Sheet: /Instruction Fetch/Instruction RAM/Lower Instruction RAM Control/
File: Instruction RAM Control.sch

Title: Instruction RAM Control Logic

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 13/24

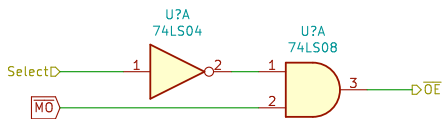


Only write to the Instruction SRAM when the MI signal is active and the appropriate plane of Instruction RAM is selected.



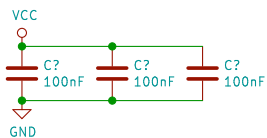
The bus transceiver should connect the Instruction SRAM to the Data Bus when the plane is selected and wither MO or MI is active.

The direction of the bus transceiver must also be set appropriately. This is done elsewhere.



Always output from Instruction SRAM when the plane of Instruction RAM is deselected. This allows RAM to be read for use in iF.

Else, if the plane is selected then only read from SRAM when the MO signal is active.



Logic for the control signals which drive Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM/Upper Instruction RAM Control/
File: Instruction RAM Control.sch

Title: Instruction RAM Control Logic

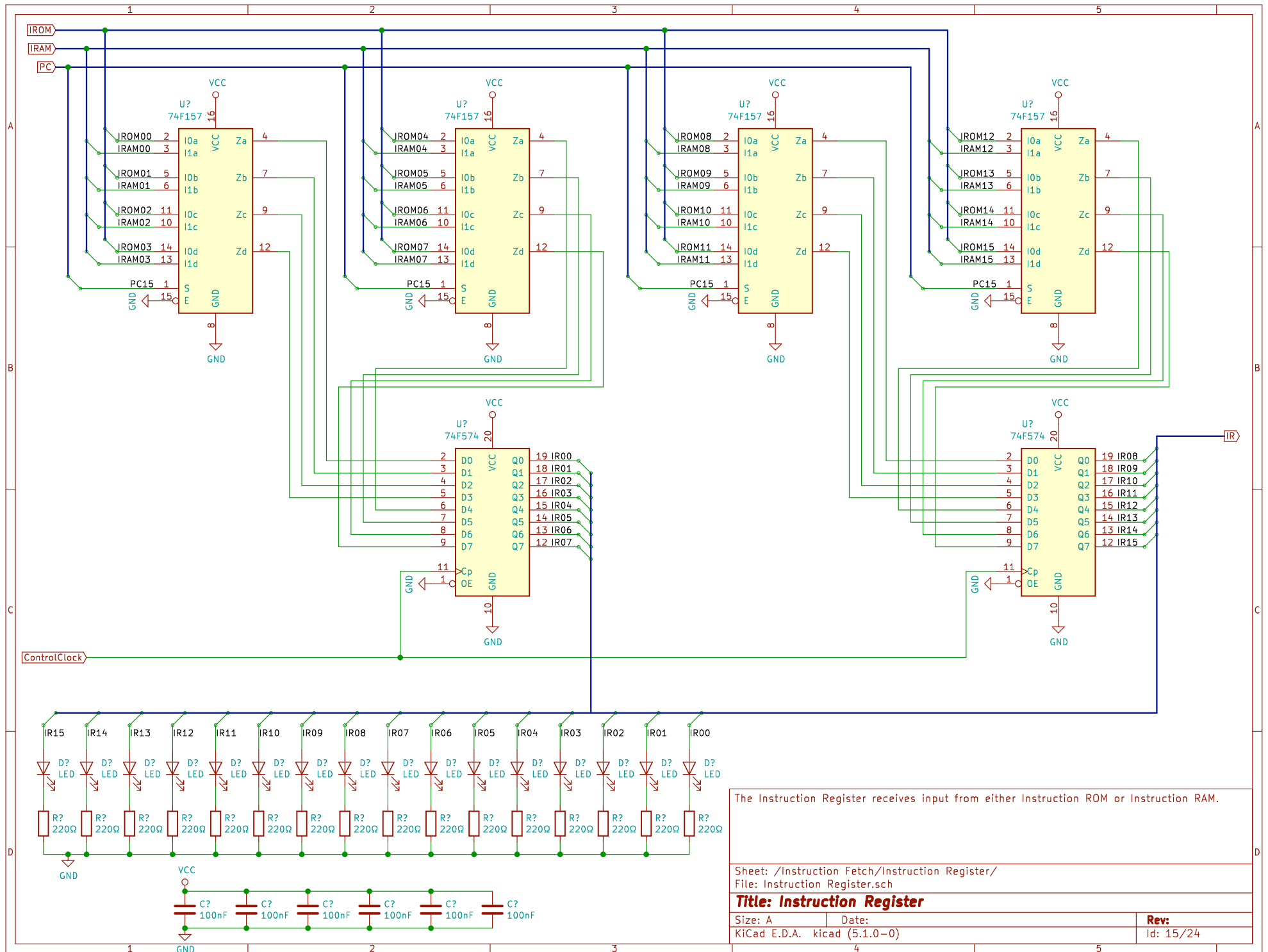
Size: A4

Date:

Rev:

KiCad E.D.A. kicad (5.1.0-0)

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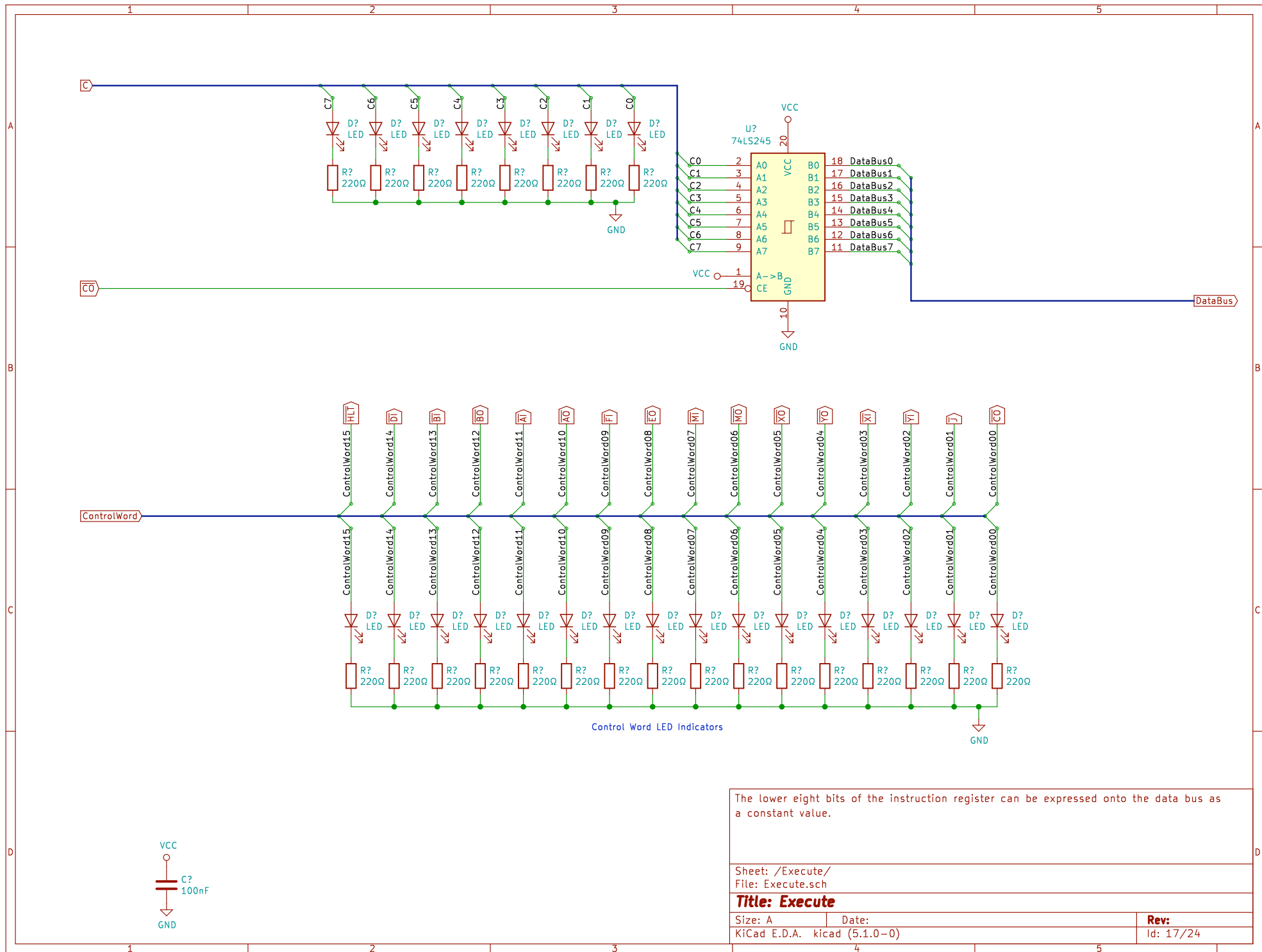
The Instruction Register receives input from either Instruction ROM or Instruction RAM.

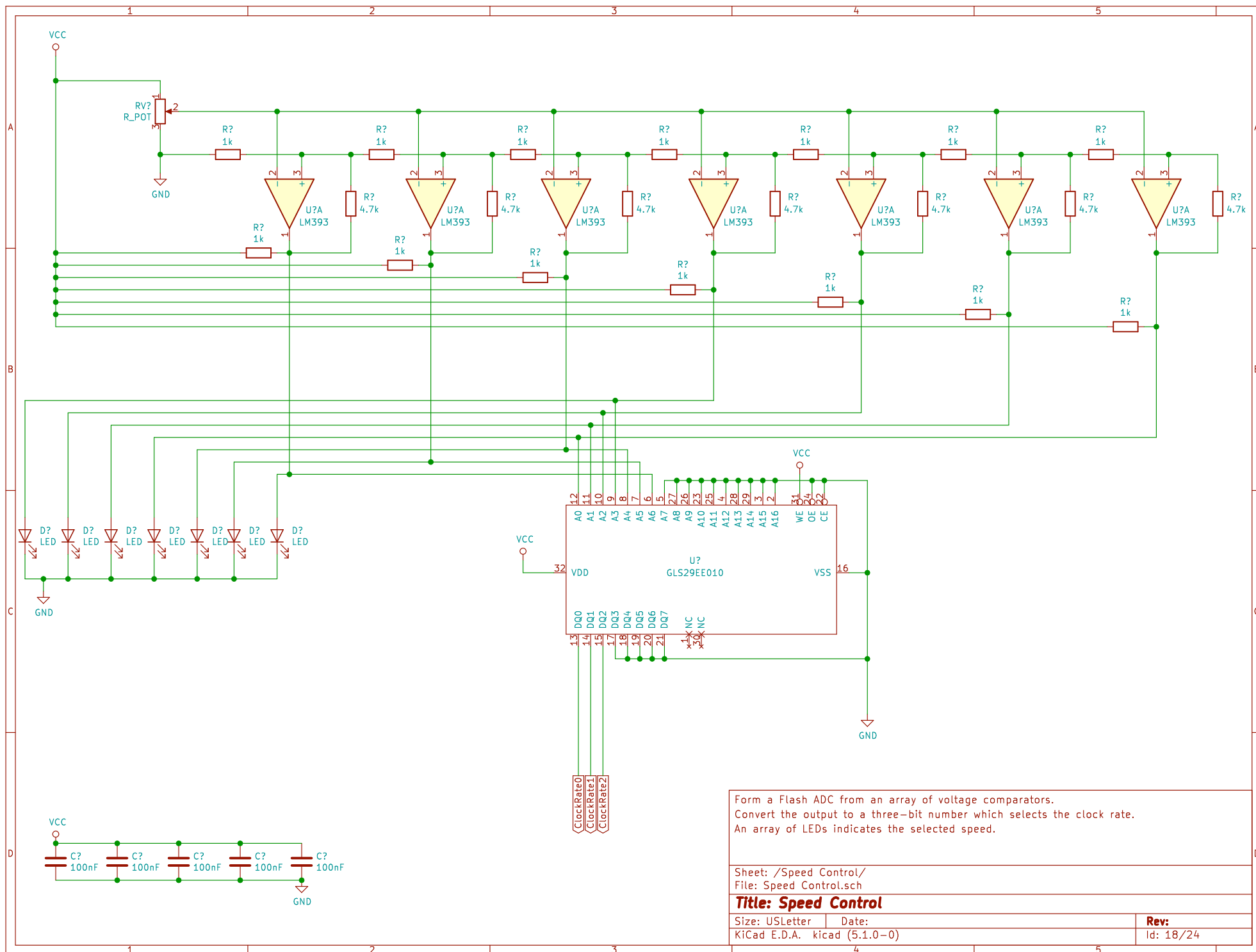
Sheet: /Instruction Fetch/Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 15/24





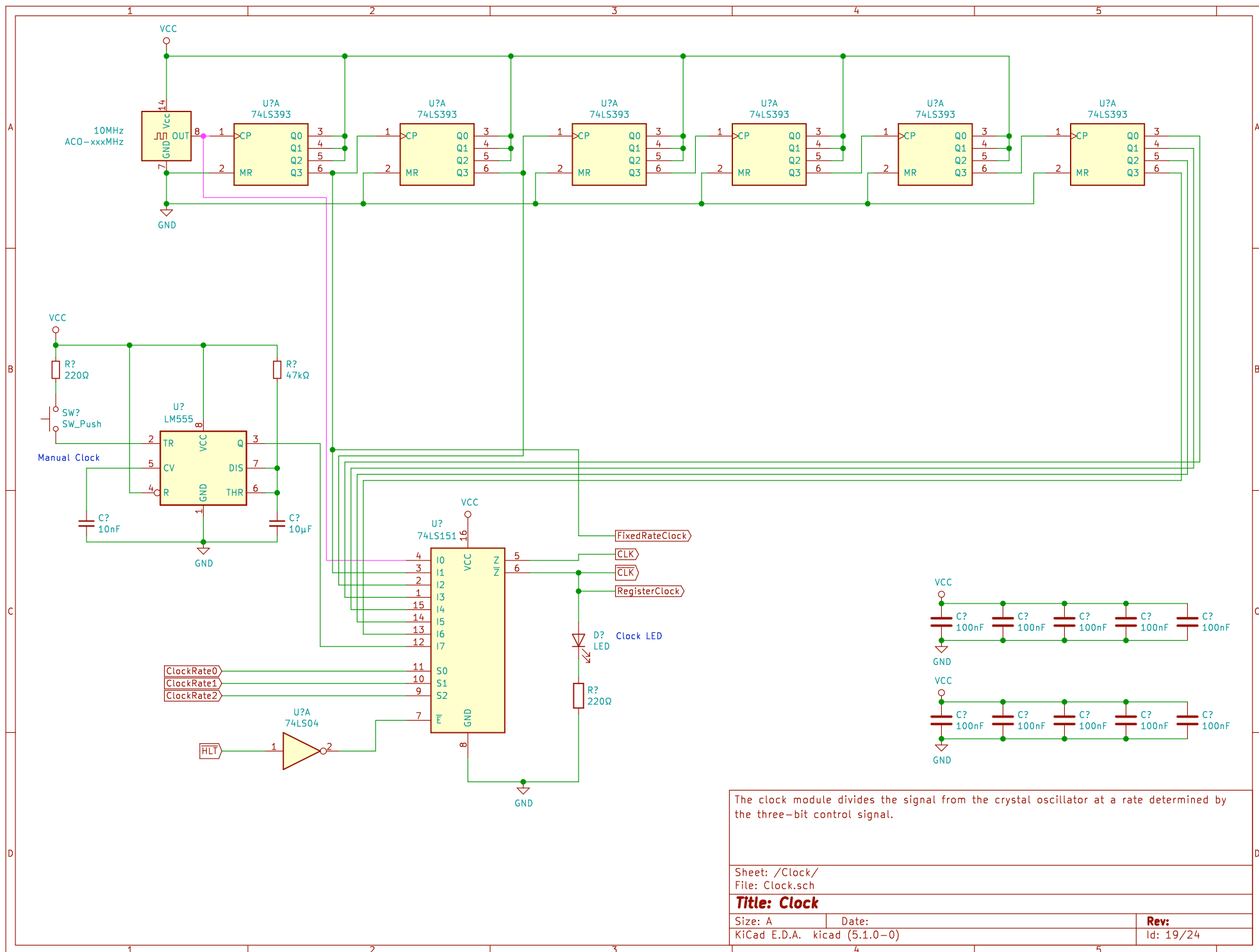
Form a Flash ADC from an array of voltage comparators.
Convert the output to a three-bit number which selects the clock rate.
An array of LEDs indicates the selected speed.

Sheet: /Speed Control/
File: Speed Control.sch

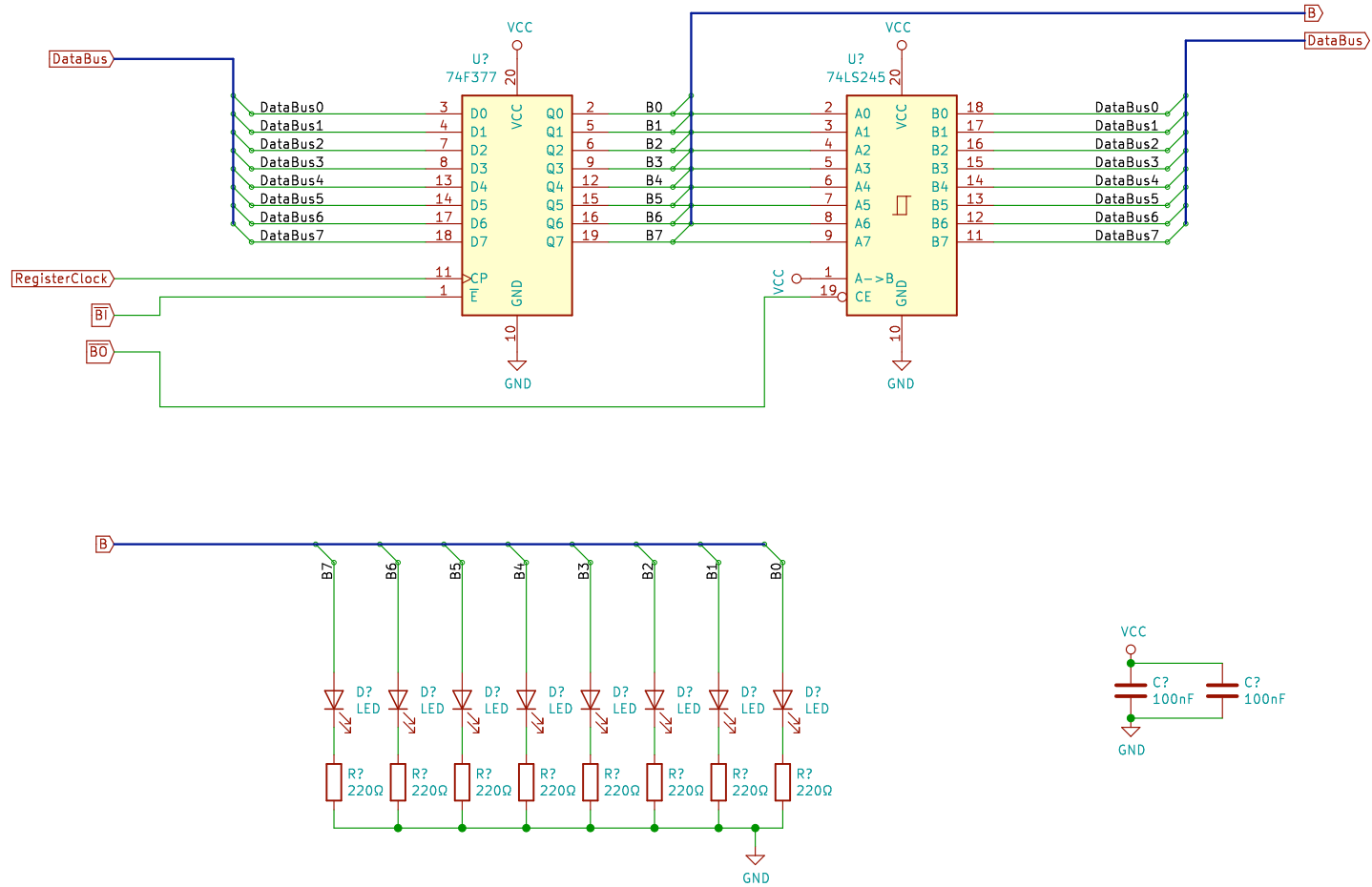
Title: Speed Control

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 18/24



Rev: 1.0
Id: 21/24



Register B is wired to the ALU's B operand.		
Sheet: /Register B/ File: Register B.sch		
Title: Register B		
Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 22/24

