Sheet: Output Display

File: Output Display.sch

Sheet: Register XY

File: Register XY.sch

Sheet: Speed Control

File: Speed Control.sch

Sheet: Program Counter

File: Program Counter.sch

Sheet: Clock

File: Clock.sch

Sheet: Instruction Fetch

File: Instruction Fetch.sch

Sheet: Power-on Reset

File: Power-on Reset.sch

Sheet: Data RAM

File: Data RAM.sch

Sheet: Instruction Decode

File: Instruction Decode.sch

Sheet: Register A

File: Register A.sch

Sheet: Serial

File: Serial.sch

Sheet: Execute

File: Execute.sch

Sheet: Register B

File: Register B.sch

Sheet: Register D

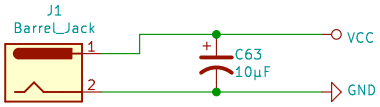
File: Register D.sch

Sheet: Bus Display

File: Bus Display.sch

Sheet: ALU

File: ALU.sch

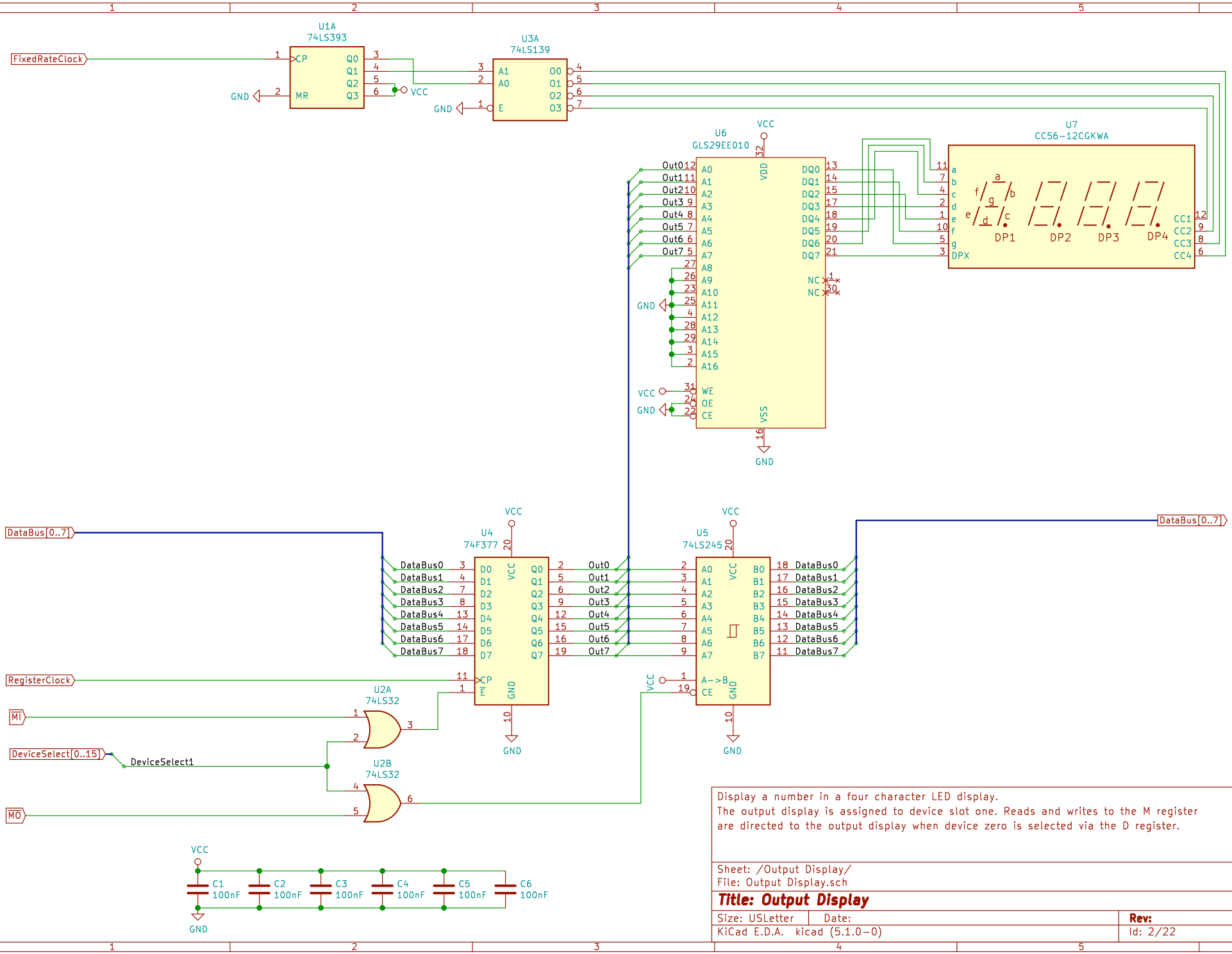


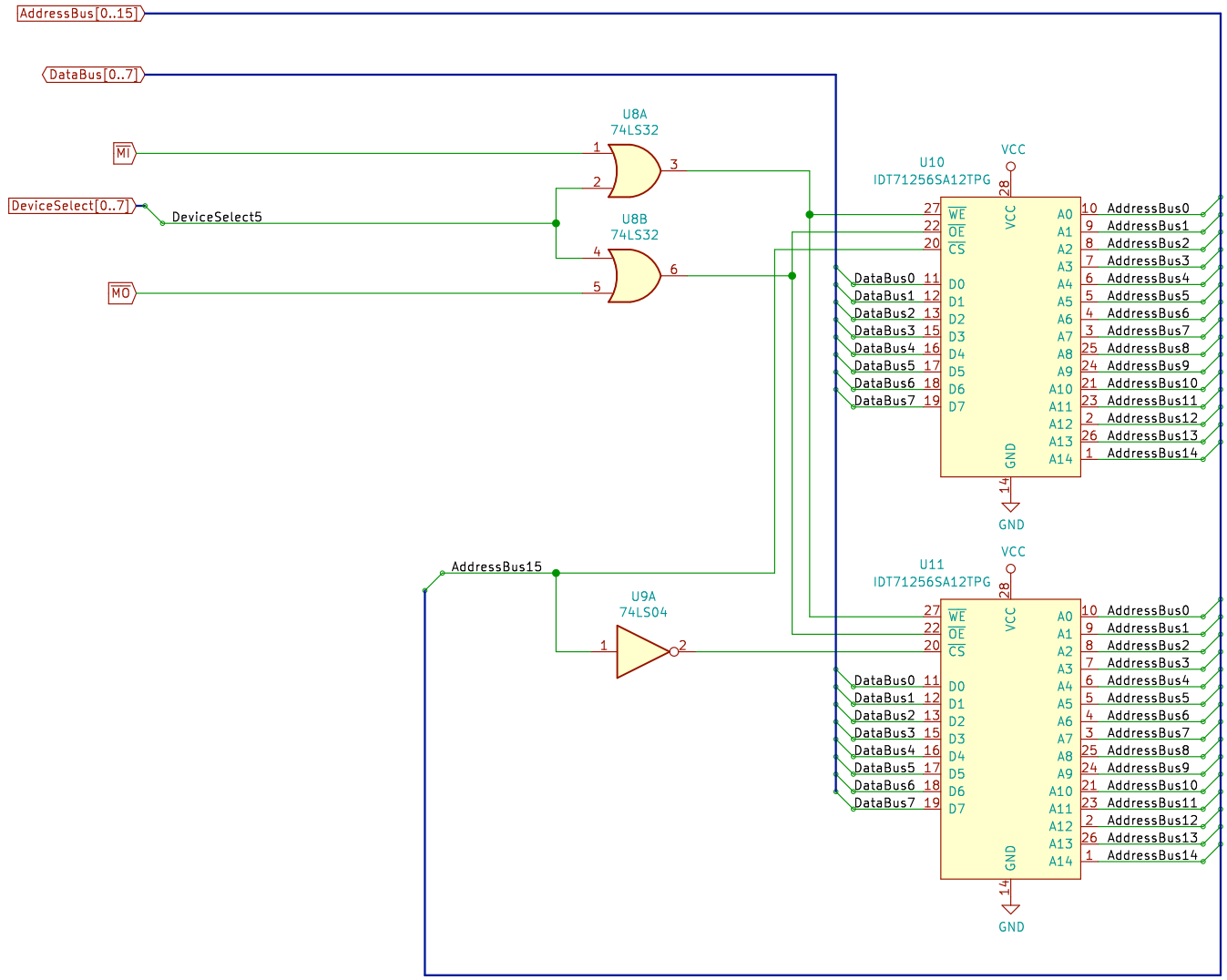
TTL microcomputer built from 74xx series logic chips.

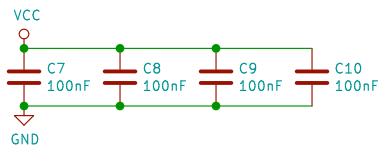
Sheet: /
File: TurtleTTL.sch

Title: Turtle TTL

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 1/22


U1A
74LS393
FixedRateClock
CP
MR
Q0
Q1
Q2
Q3
GND
VCC
U3A
74LS139
A1
A0
E
O0
O1
O2
O3
U6
GLS29EE010
VDD
VSS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
WE
OE
CE
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
NC
Out0
Out1
Out2
Out3
Out4
Out5
Out6
Out7
U7
CC56-12CGKWA
a
b
c
d
e
f
g
DP
DP1
DP2
DP3
DP4
CC1
CC2
CC3
CC4
DataBus[0..7]
U4
74F377
U5
74LS245
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
DataBus0
DataBus1
DataBus2
DataBus3
DataBus4
DataBus5
DataBus6
DataBus7
A->B
B0
B1
B2
B3
B4
B5
B6
B7
RegisterClock
MI
MO
DeviceSelect[0..15]
DeviceSelect1
U2A
74LS32
U2B
74LS32
C1
100nF
C2
100nF
C3
100nF
C4
100nF
C5
100nF
C6
100nF
Display a number in a four character LED display.
The output display is assigned to device slot one. Reads and writes to the M register are directed to the output display when device zero is selected via the D register.
Sheet: /Output Display/
File: Output Display.sch
Title: Output Display
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 2/22



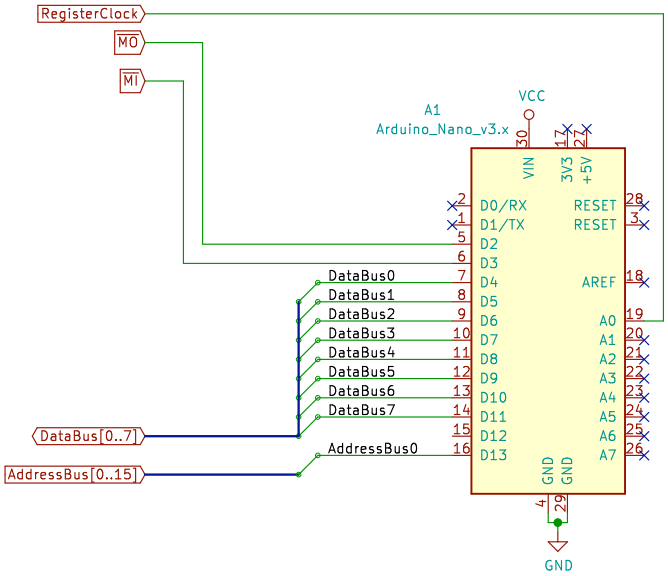


64KB Data RAM is connected to device slot five.
Reads and writes to the M register are directed to Data RAM when device 5 is selected via the D register.
The MSB of the address selects between two 32KB SRAM ICs.

Sheet: /Data RAM/
File: Data RAM.sch

Title: Data RAM

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 3/22

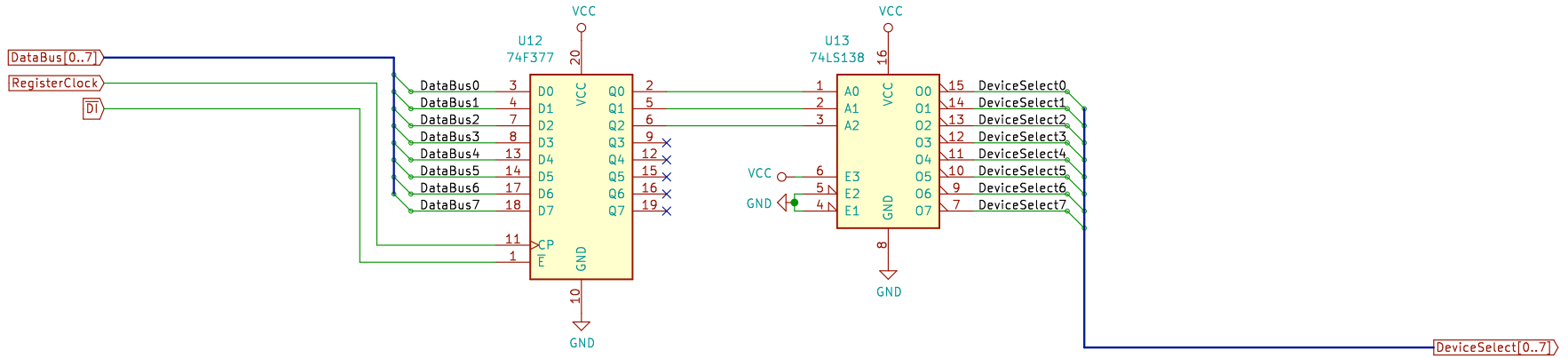


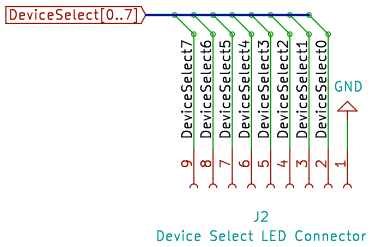
An Arduino Nano serves as a serial interface module.

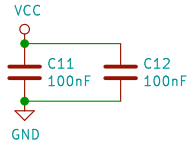
Sheet: /Serial/
File: Serial.sch

Title: Serial I/O

Size: USLetter | Date: | **Rev:**
KiCad E.D.A. kicad (5.1.0-0) | Id: 4/22





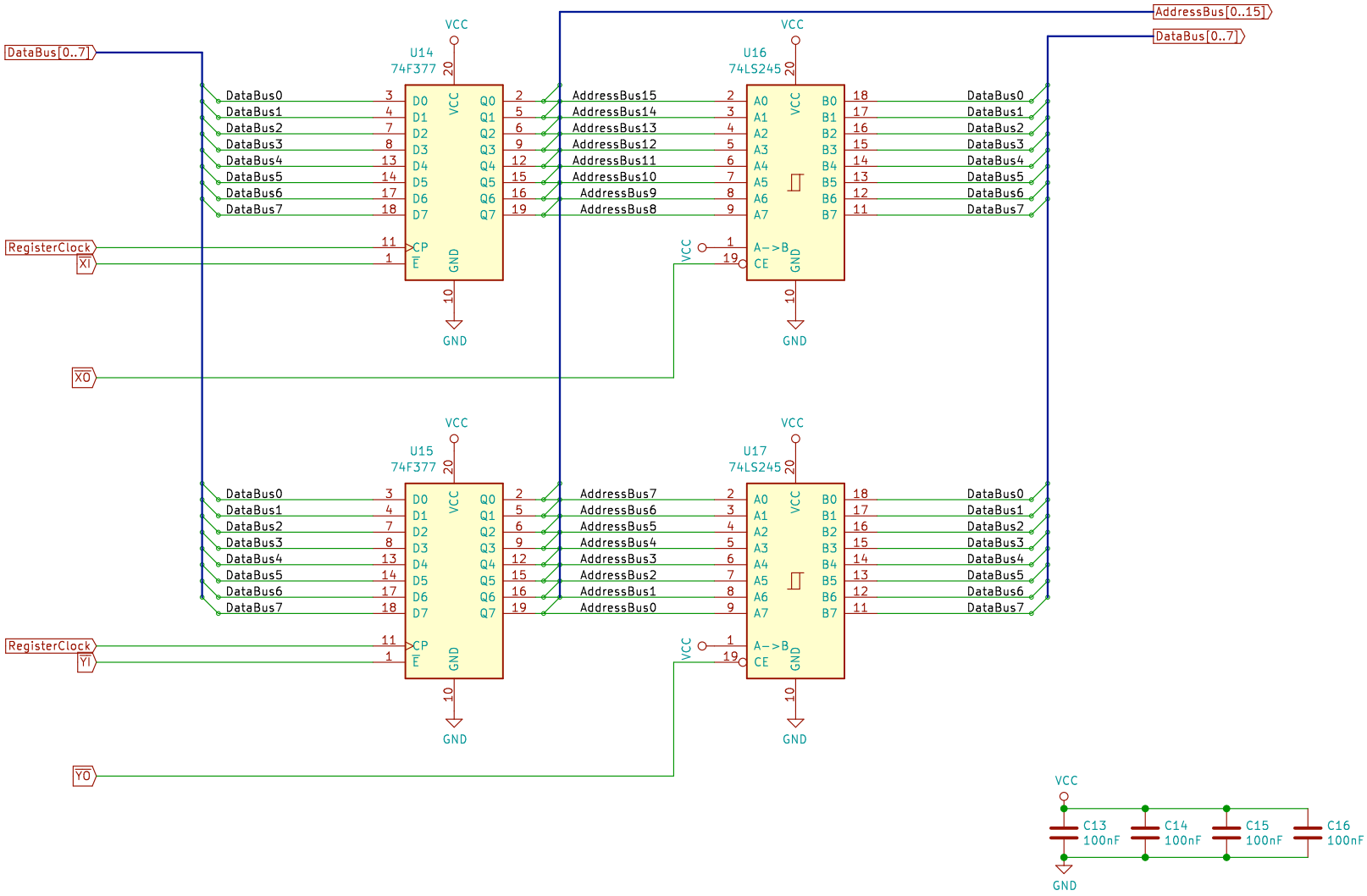


Register D controls the device select lines for peripherals and memory.

Sheet: /Register D/
File: Register D.sch

Title: Register D

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 5/22

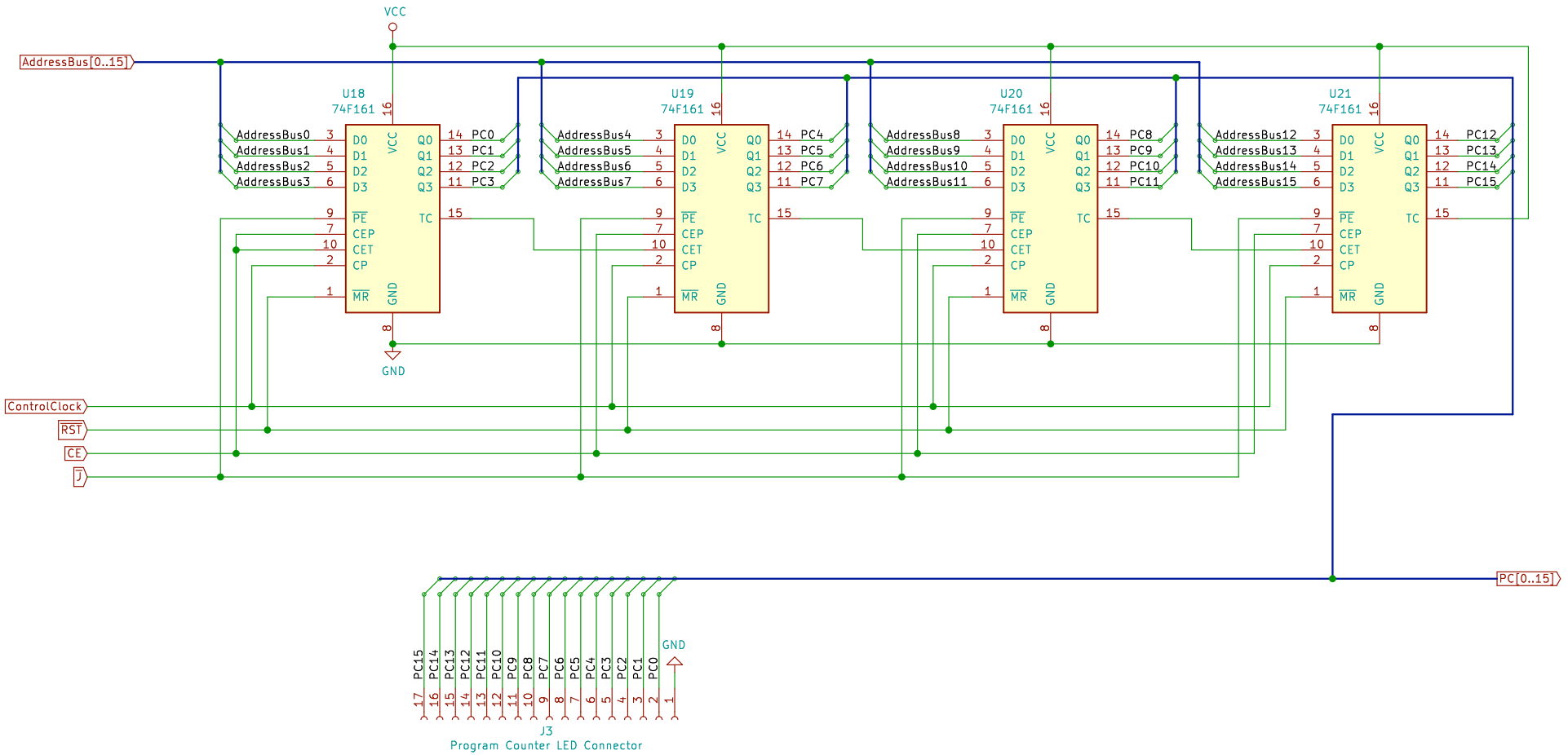


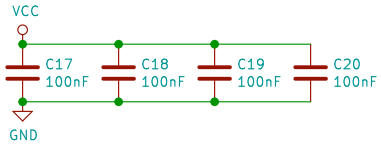
The XY register pair sets the value on the sixteen-bit Address Bus.

Sheet: /Register XY/
File: Register XY.sch

Title: Registers X and Y

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 6/22





Sheet: /Program Counter/	
File: Program Counter.sch	
Title: Program Counter	
Size: USLetter Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)	Id: 7/22

Sheet: PC/IF

File: PC_IF.sch

Sheet: Instruction RAM Address

File: Instruction RAM Address.sch

Sheet: Instruction ROM

File: Instruction ROM.sch

Sheet: Instruction RAM

File: Instruction RAM.sch

Sheet: Instruction Register

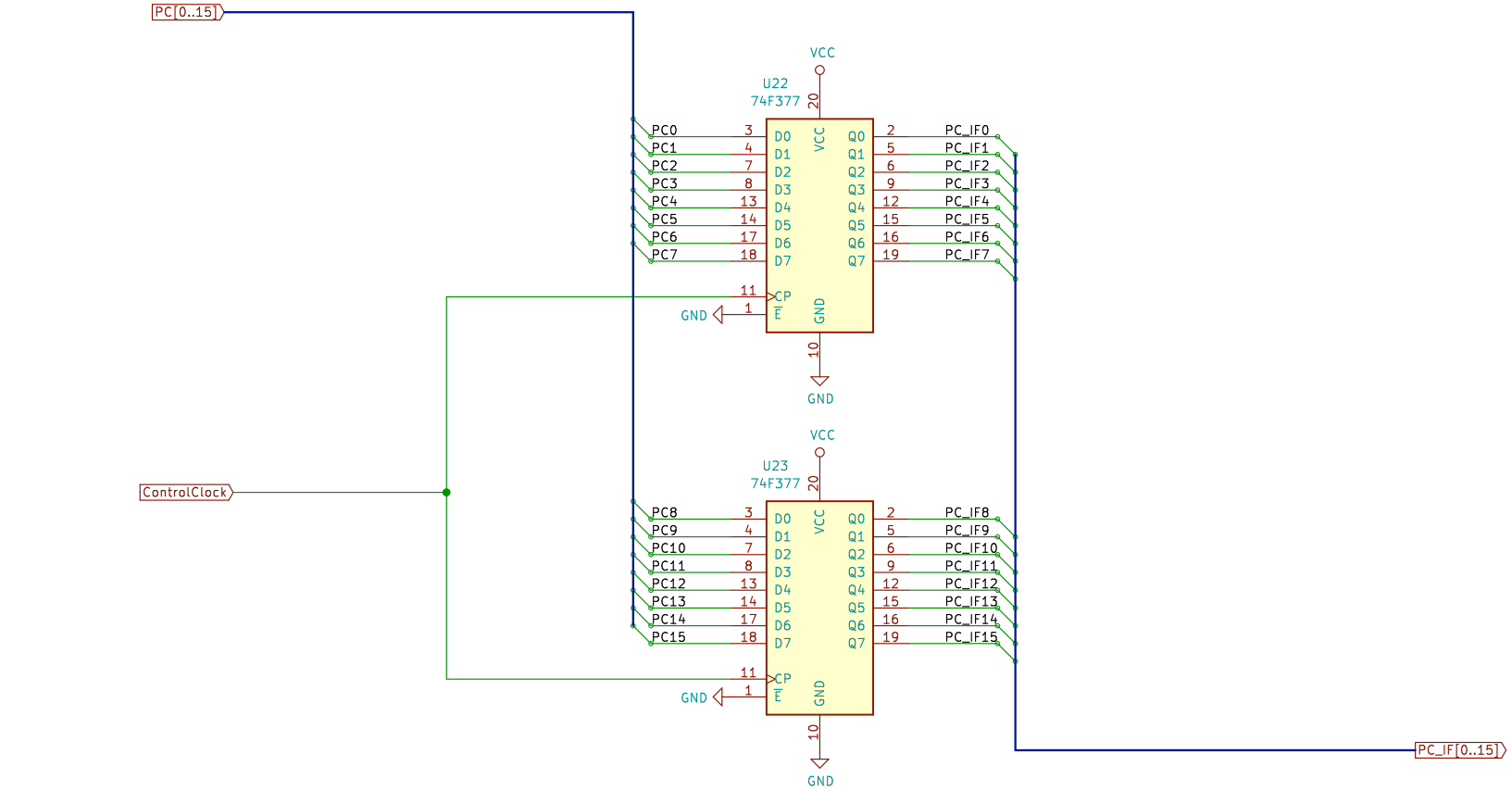
File: Instruction Register.sch

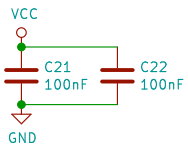
Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

Title: Instruction Fetch

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 8/22



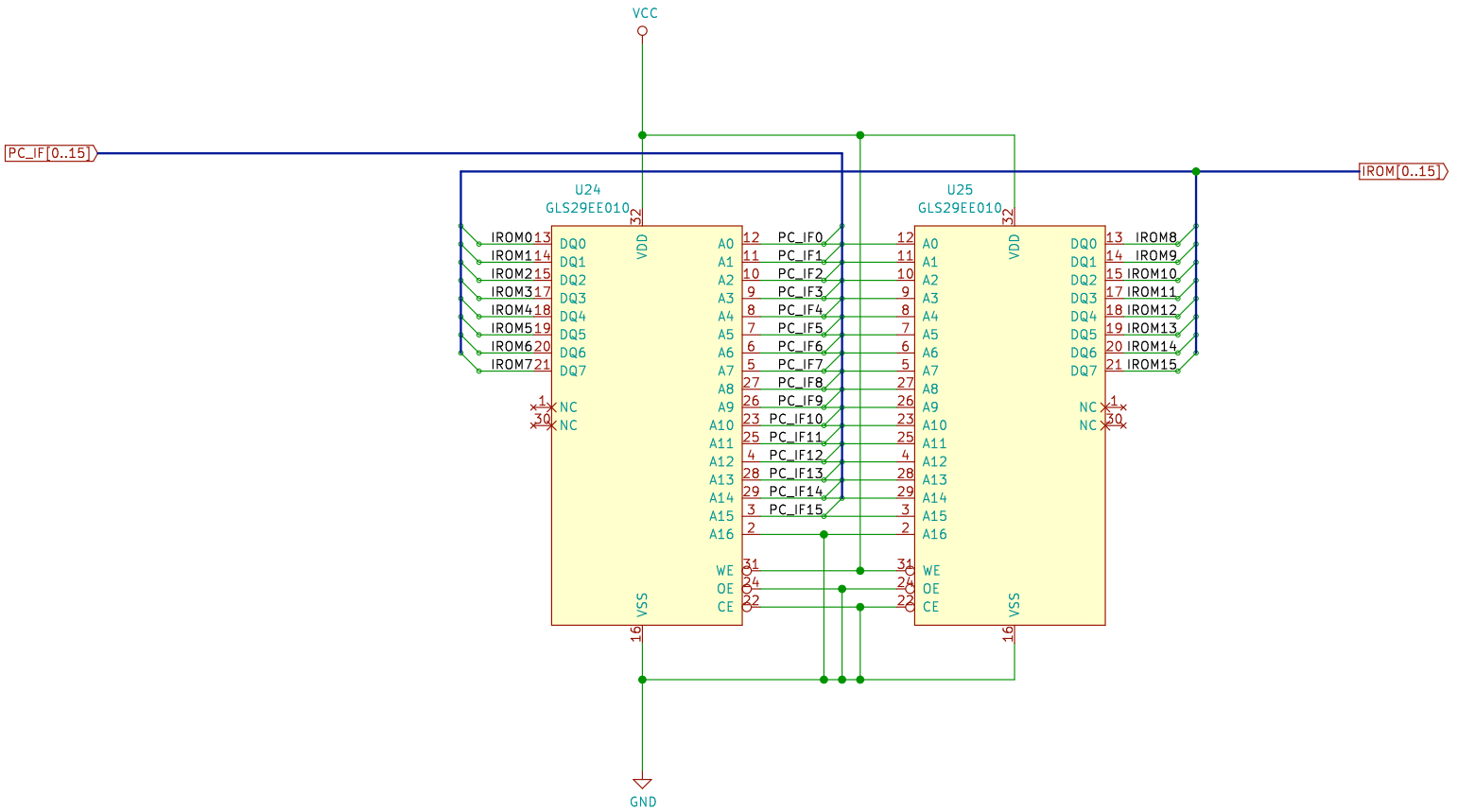


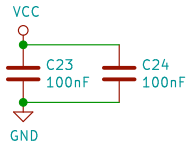
The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /Instruction Fetch/PC/IF/
File: PC_IF.sch

Title: PC/IF

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 9/22



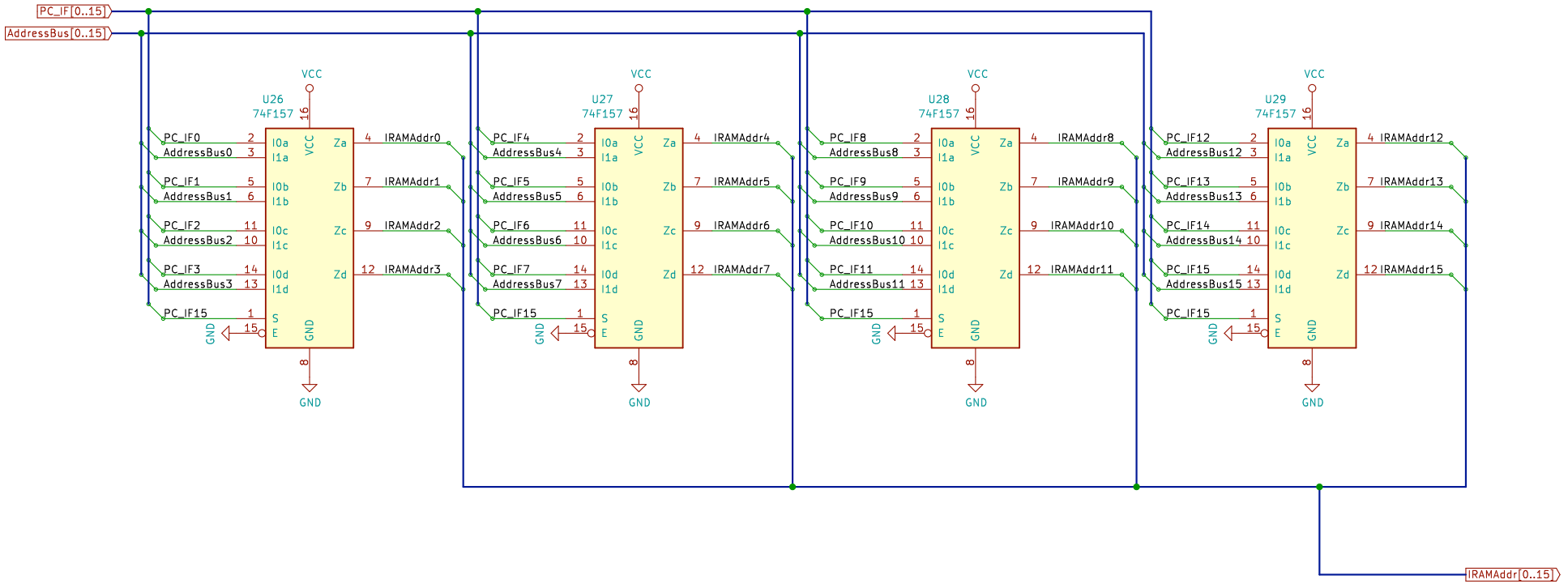


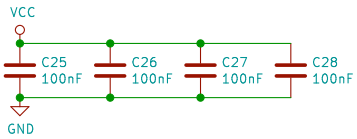
16-bit instructions are read from ROM at the address specified by the Program Counter.

Sheet: /Instruction Fetch/Instruction ROM/
File: Instruction ROM.sch

Title: Instruction ROM

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 10/22



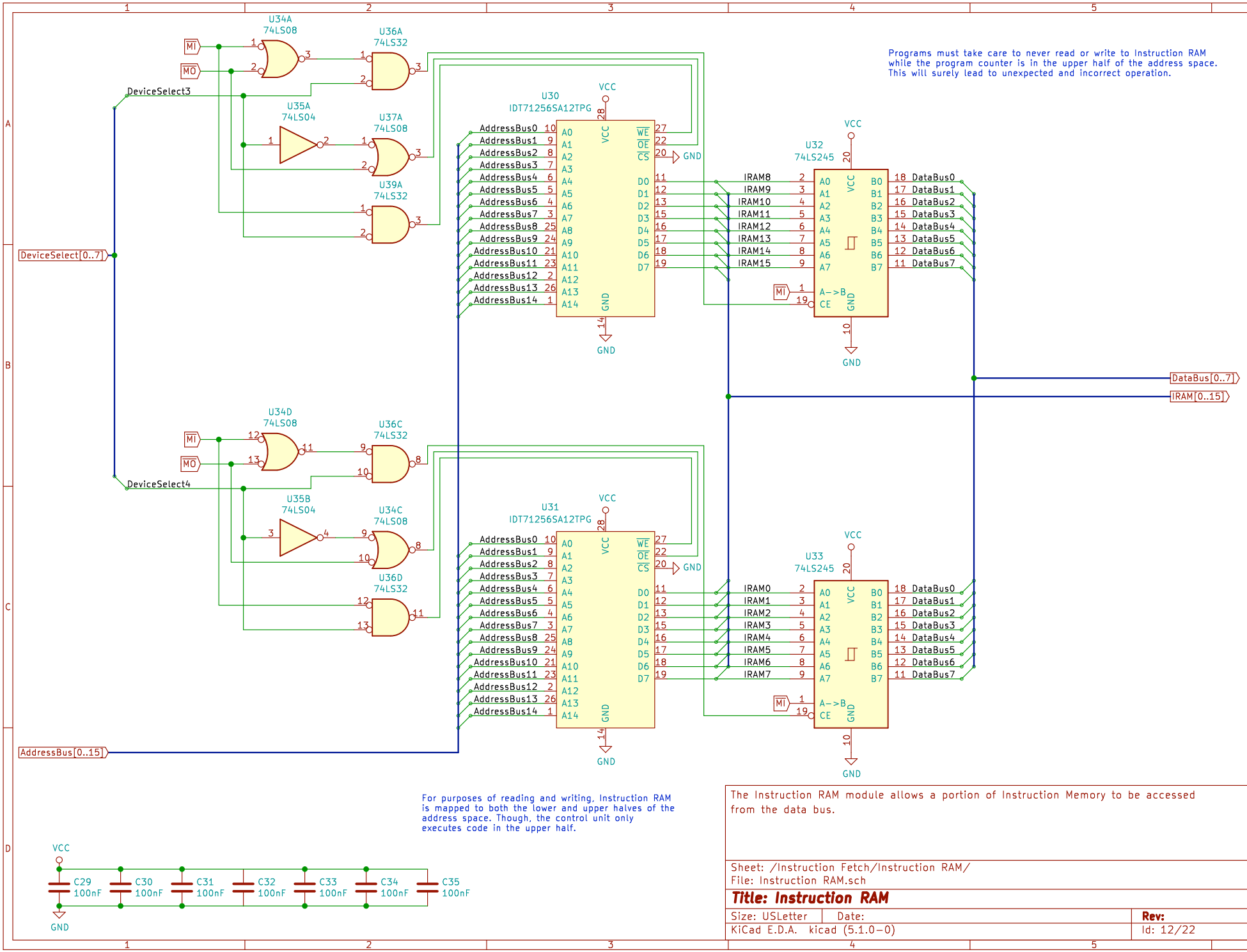


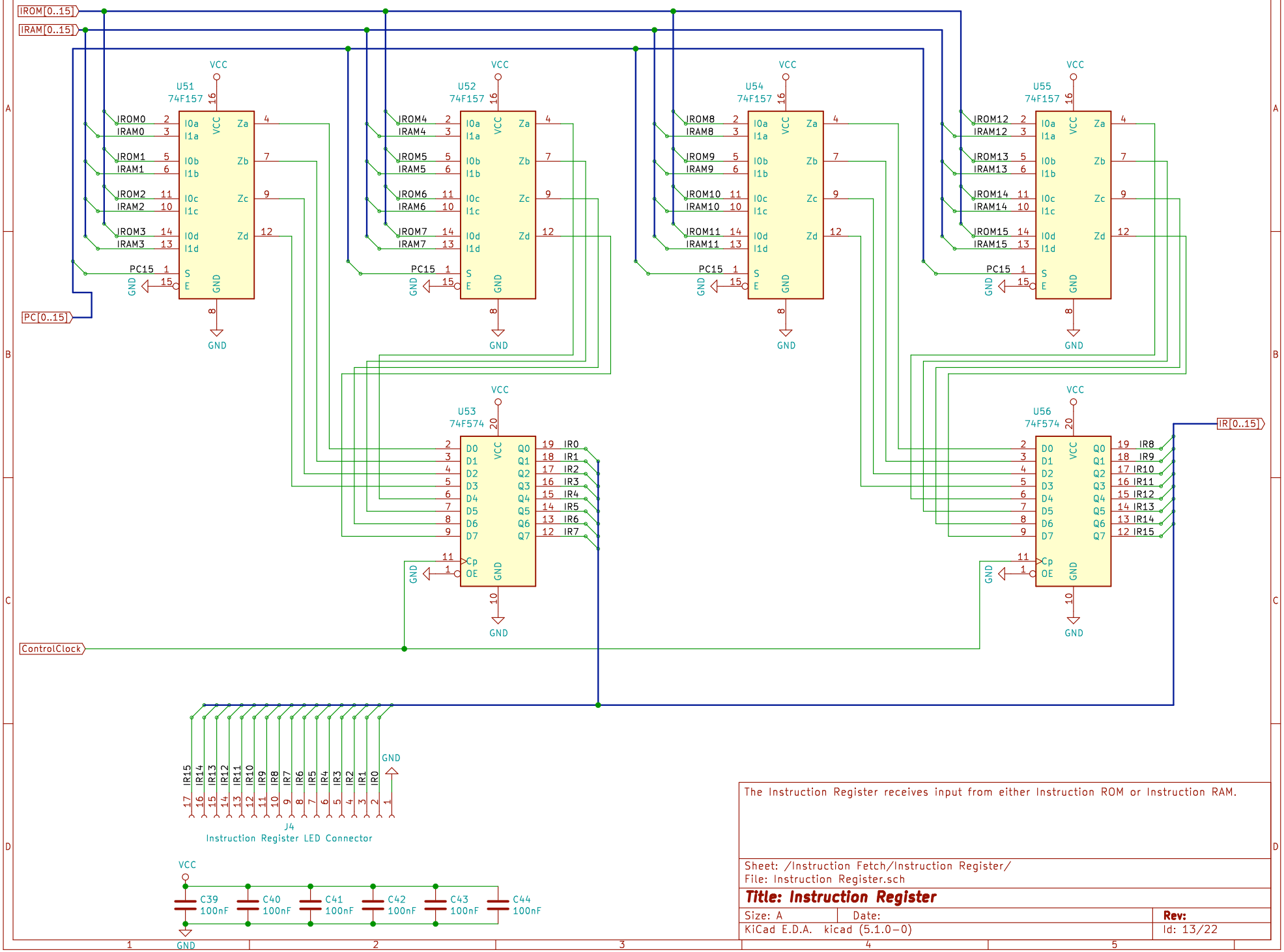
Instruction RAM uses an address from either the program counter or the address bus.
If the program counter is in the upper 32KB of the address space then use the program counter as we're running in Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM Address/
File: Instruction RAM Address.sch

Title: Instruction RAM Address

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 11/22


Programs must take care to never read or write to Instruction RAM while the program counter is in the upper half of the address space. This will surely lead to unexpected and incorrect operation.
U34A 74LS08
U36A 74LS32
U35A 74LS04
U37A 74LS08
U39A 74LS32
U34D 74LS08
U36C 74LS32
U35B 74LS04
U34C 74LS08
U36D 74LS32
MI
MO
DeviceSelect3
DeviceSelect4
DeviceSelect[0..7]
U30 IDT71256SA12TPG
U31 IDT71256SA12TPG
AddressBus0
AddressBus1
AddressBus2
AddressBus3
AddressBus4
AddressBus5
AddressBus6
AddressBus7
AddressBus8
AddressBus9
AddressBus10
AddressBus11
AddressBus12
AddressBus13
AddressBus14
AddressBus[0..15]
VCC
GND
U32 74LS245
U33 74LS245
IRAM8
IRAM9
IRAM10
IRAM11
IRAM12
IRAM13
IRAM14
IRAM15
IRAM0
IRAM1
IRAM2
IRAM3
IRAM4
IRAM5
IRAM6
IRAM7
DataBus0
DataBus1
DataBus2
DataBus3
DataBus4
DataBus5
DataBus6
DataBus7
DataBus[0..7]
IRAM[0..15]
A->B
For purposes of reading and writing, Instruction RAM is mapped to both the lower and upper halves of the address space. Though, the control unit only executes code in the upper half.
C29 100nF
C30 100nF
C31 100nF
C32 100nF
C33 100nF
C34 100nF
C35 100nF
The Instruction RAM module allows a portion of Instruction Memory to be accessed from the data bus.
Sheet: /Instruction Fetch/Instruction RAM/
File: Instruction RAM.sch
Title: Instruction RAM
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 12/22

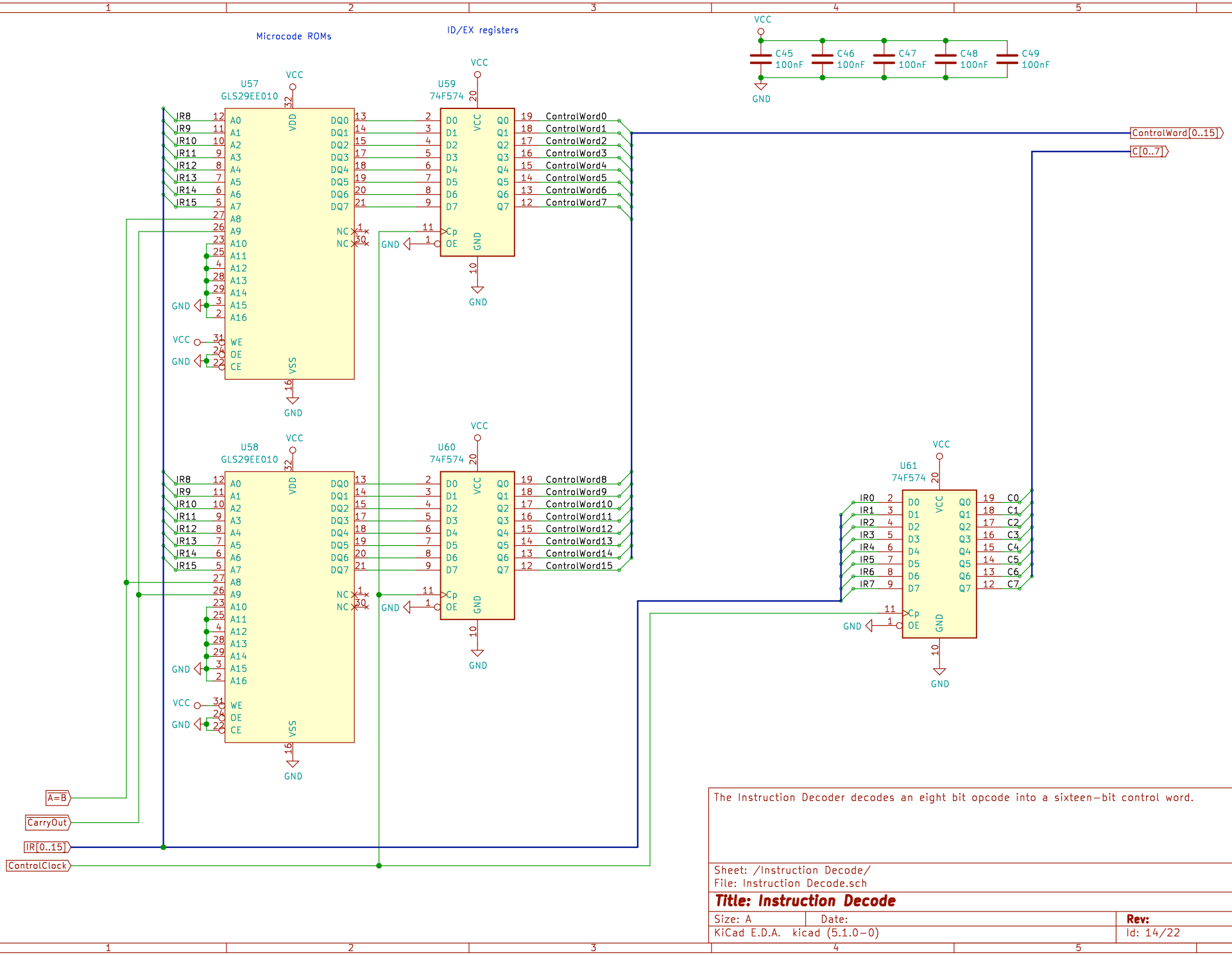


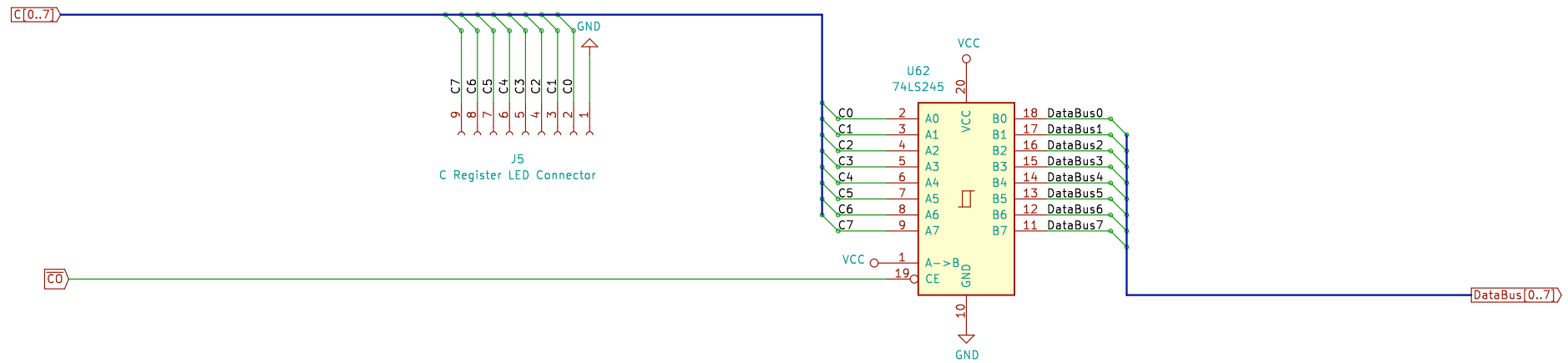
The Instruction Register receives input from either Instruction ROM or Instruction RAM.

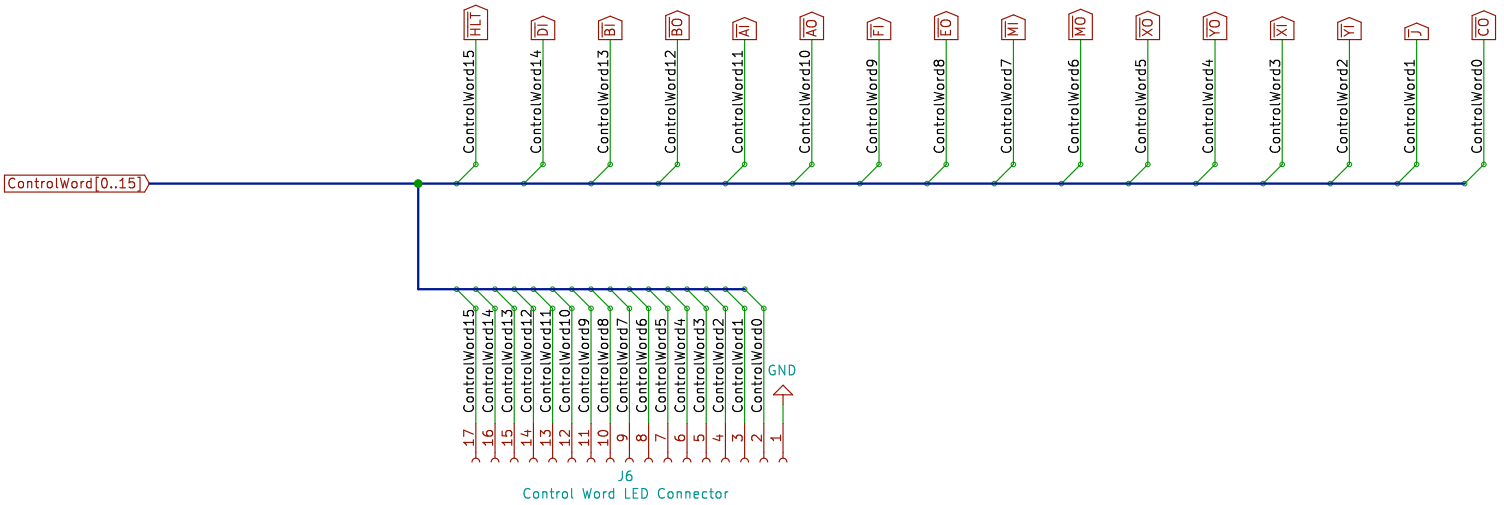
Sheet: /Instruction Fetch/Instruction Register/
File: Instruction Register.sch

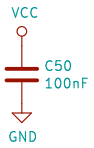
Title: Instruction Register

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 13/22


Microcode ROMs
ID/EX registers
U57
GLS29EE010
U58
GLS29EE010
U59
74F574
U60
74F574
U61
74F574
C45 100nF
C46 100nF
C47 100nF
C48 100nF
C49 100nF
VCC
GND
ControlWord0
ControlWord1
ControlWord2
ControlWord3
ControlWord4
ControlWord5
ControlWord6
ControlWord7
ControlWord8
ControlWord9
ControlWord10
ControlWord11
ControlWord12
ControlWord13
ControlWord14
ControlWord15
ControlWord[0..15]
C[0..7]
A=B
CarryOut
IR[0..15]
ControlClock
The Instruction Decoder decodes an eight bit opcode into a sixteen-bit control word.
Sheet: /Instruction Decode/
File: Instruction Decode.sch
Title: Instruction Decode
Size: A
Date:
Rev:
KiCad E.D.A. kicad (5.1.0-0)
Id: 14/22





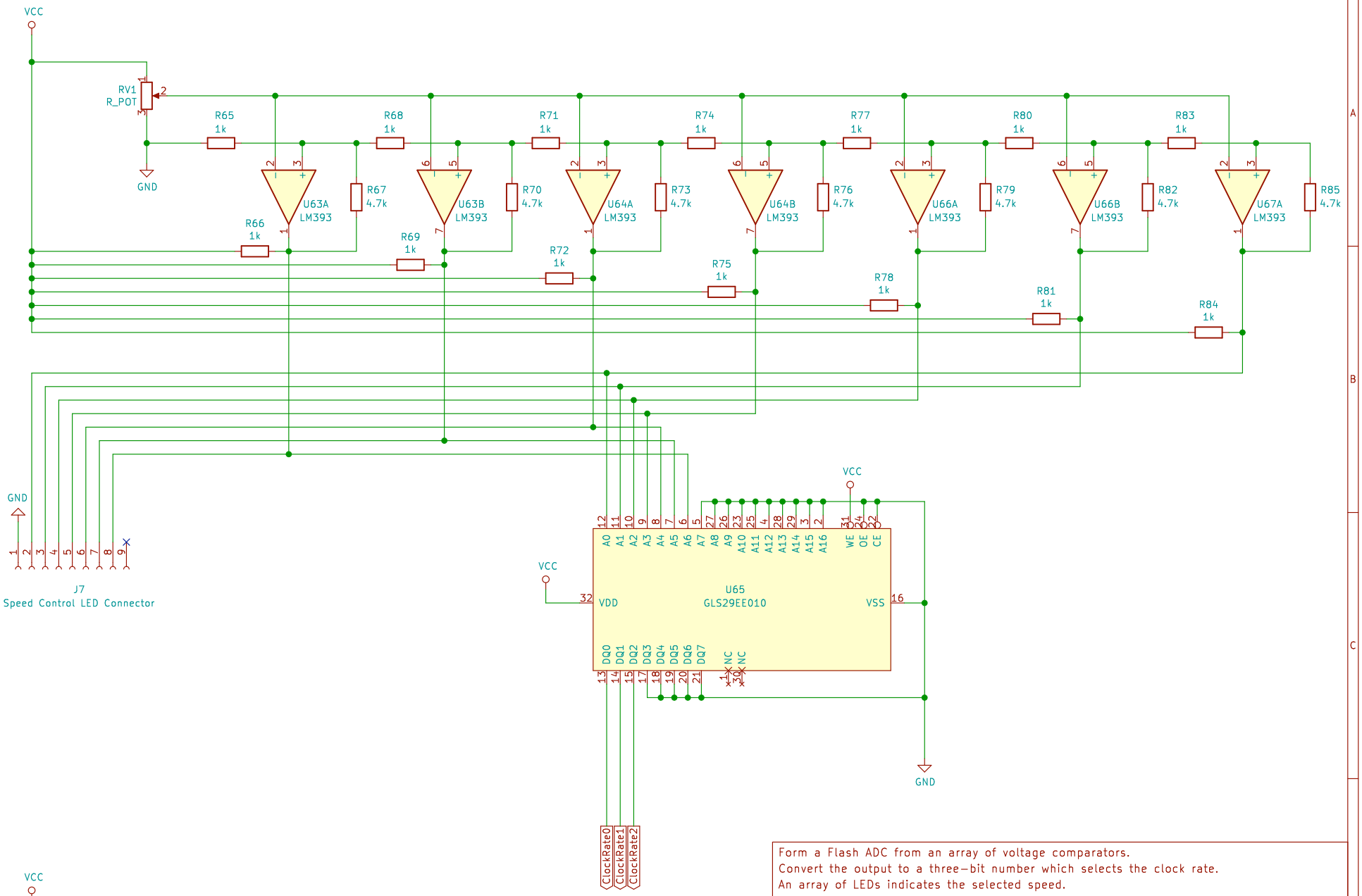


The lower eight bits of the instruction register can be expressed onto the data bus as a constant value.

Sheet: /Execute/
File: Execute.sch

Title: Execute

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 15/22

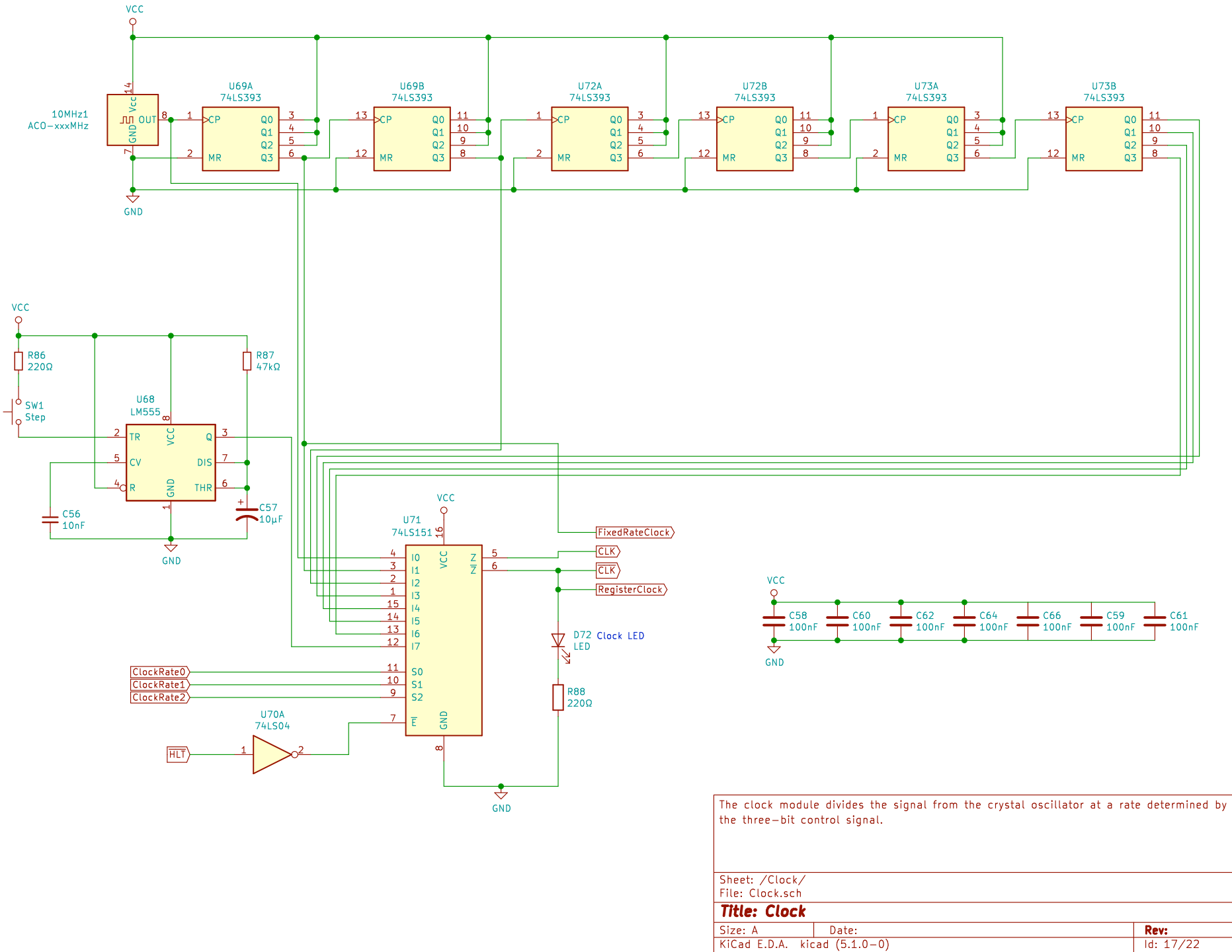


Form a Flash ADC from an array of voltage comparators.
Convert the output to a three-bit number which selects the clock rate.
An array of LEDs indicates the selected speed.

Sheet: /Speed Control/
File: Speed Control.sch

Title: Speed Control

Size: USLetter | Date: | **Rev:**
KiCad E.D.A. kicad (5.1.0-0) | Id: 16/22



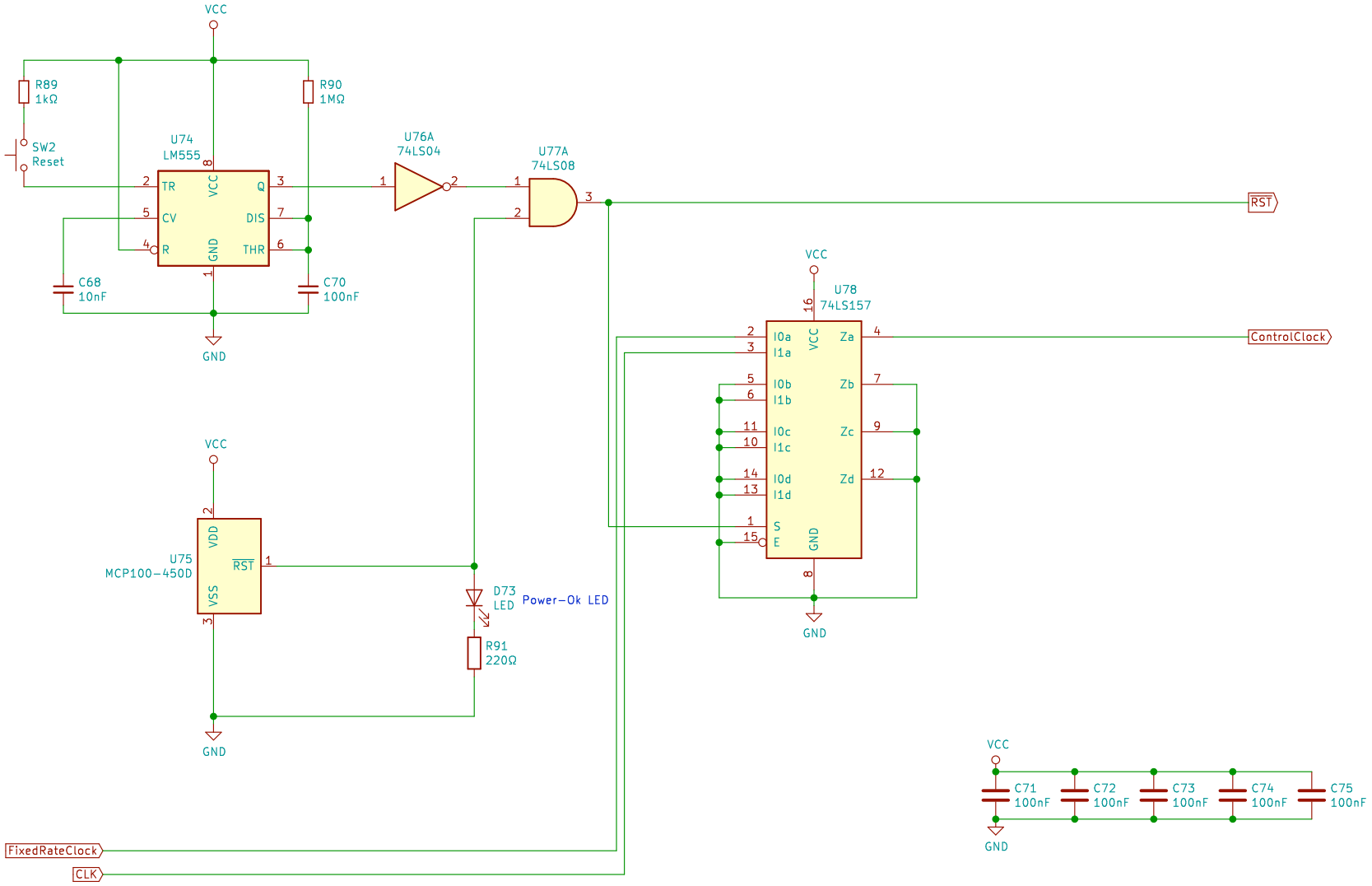
The clock module divides the signal from the crystal oscillator at a rate determined by the three-bit control signal.

Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: A | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.0-0) | Id: 17/22

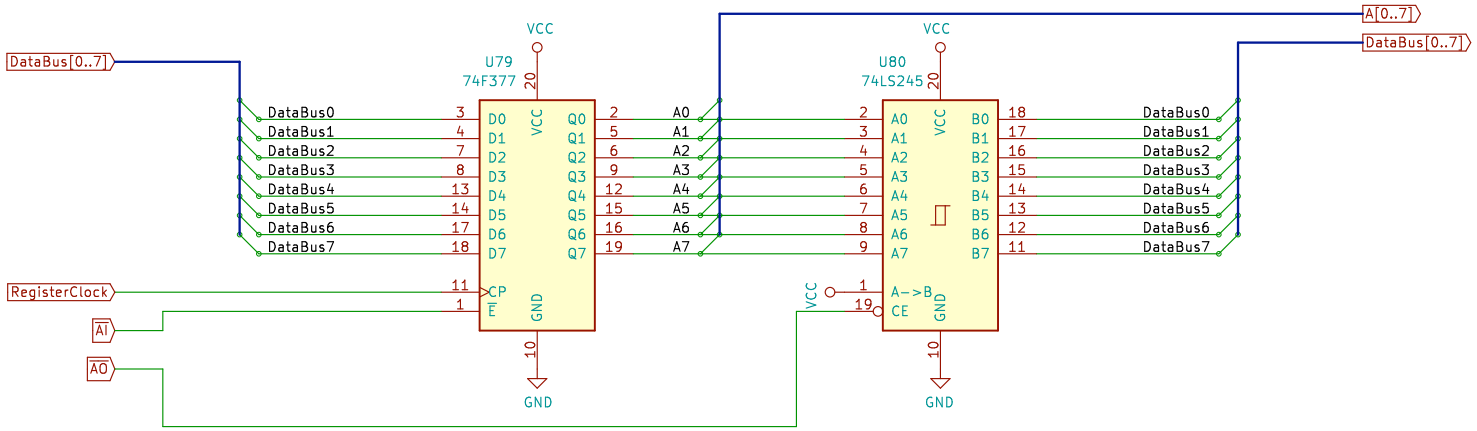


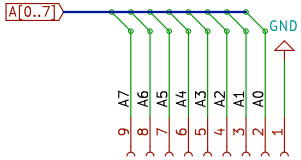
The MCP100 provides Power-on Reset functionality.
A button is also provided to manually reset the machine.
During reset, the control clock is pulsed repeatedly to flush the pipeline.

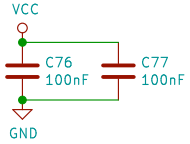
Sheet: /Power-on Reset/
File: Power-on Reset.sch

Title: Power-on Reset

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 18/22





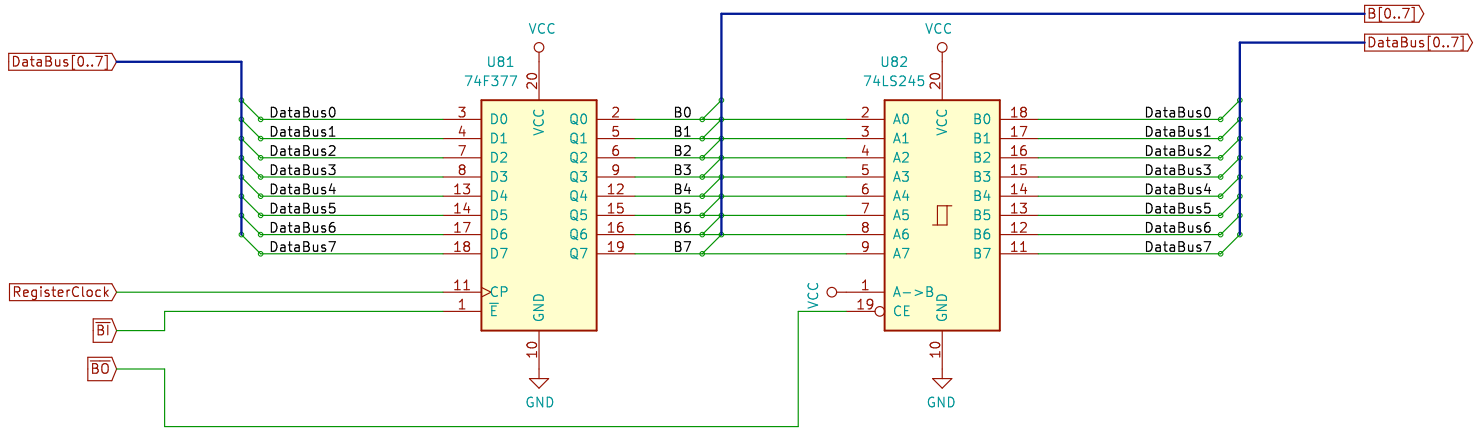


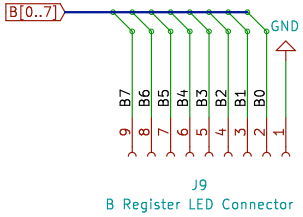
Register A is wired to the ALU's A operand.

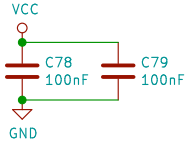
Sheet: /Register A/
File: Register A.sch

Title: Register A

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 19/22





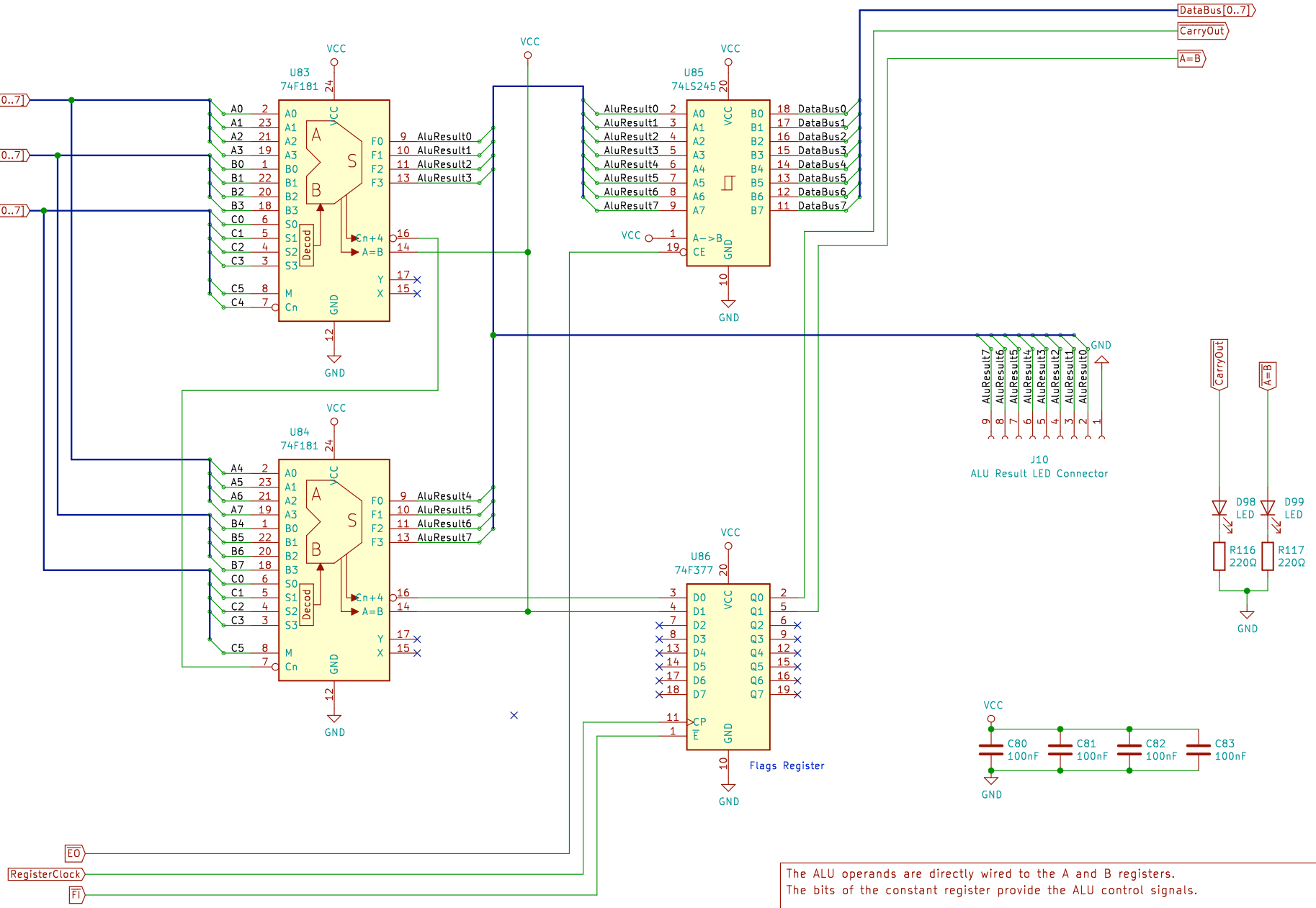


Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

Title: Register B

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.0-0)		Id: 20/22

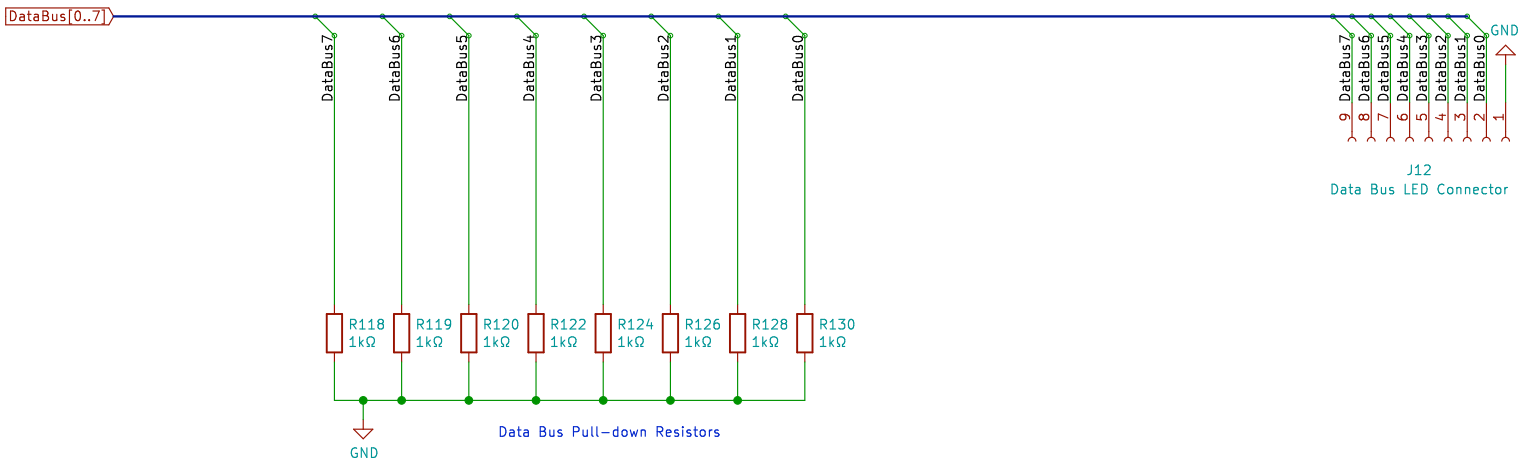


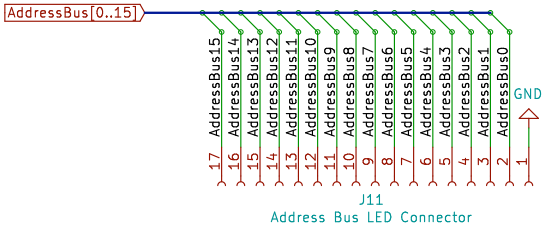
The ALU operands are directly wired to the A and B registers.
The bits of the constant register provide the ALU control signals.

Sheet: /ALU/
File: ALU.sch

Title: ALU

Size: A	Date:	Rev:
KiCad E.D.A. kicad (5.1.0-0)		Id: 21/22





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Title: Bus Display

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KiCad E.D.A. kicad (5.1.0-0)		Id: 22/22