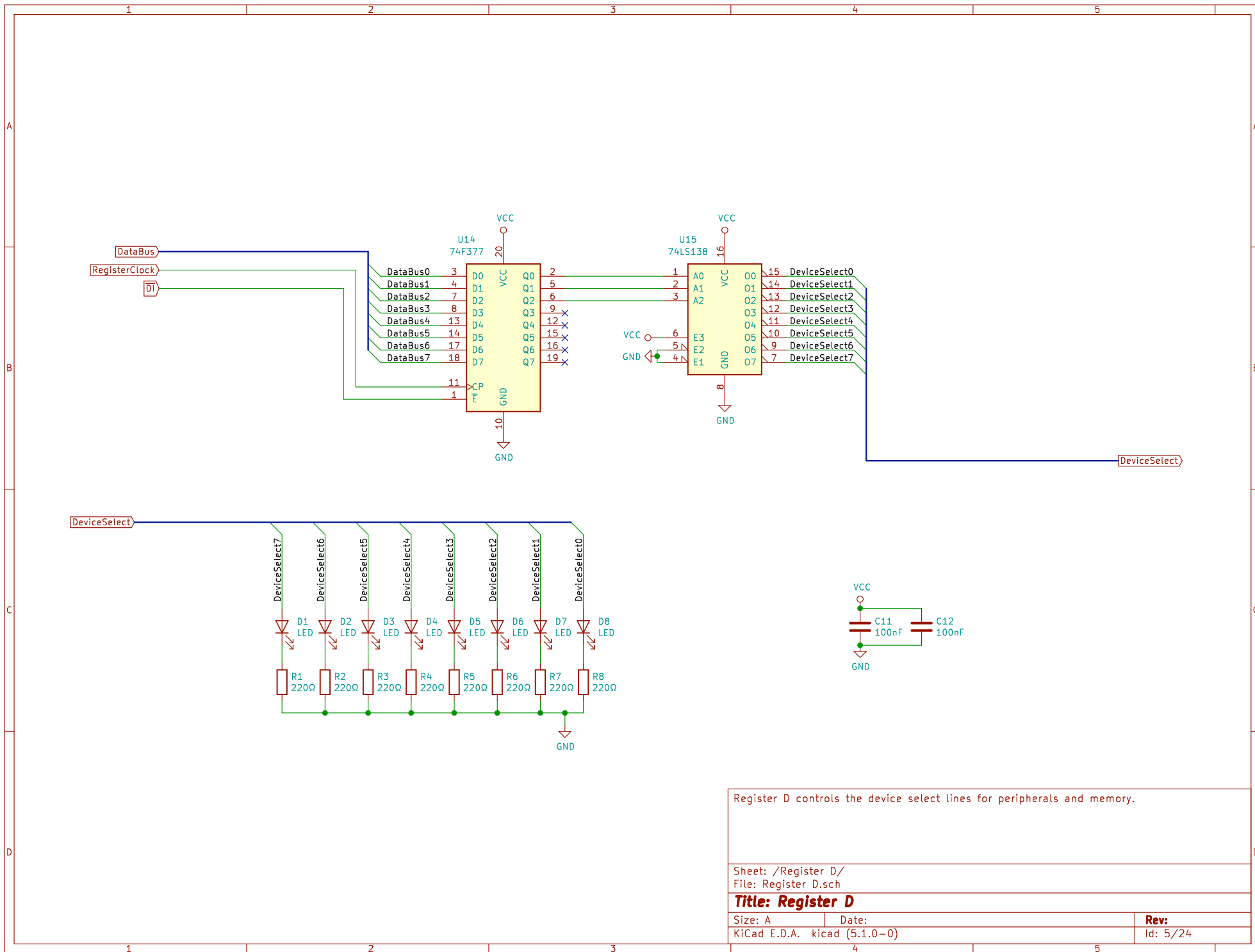
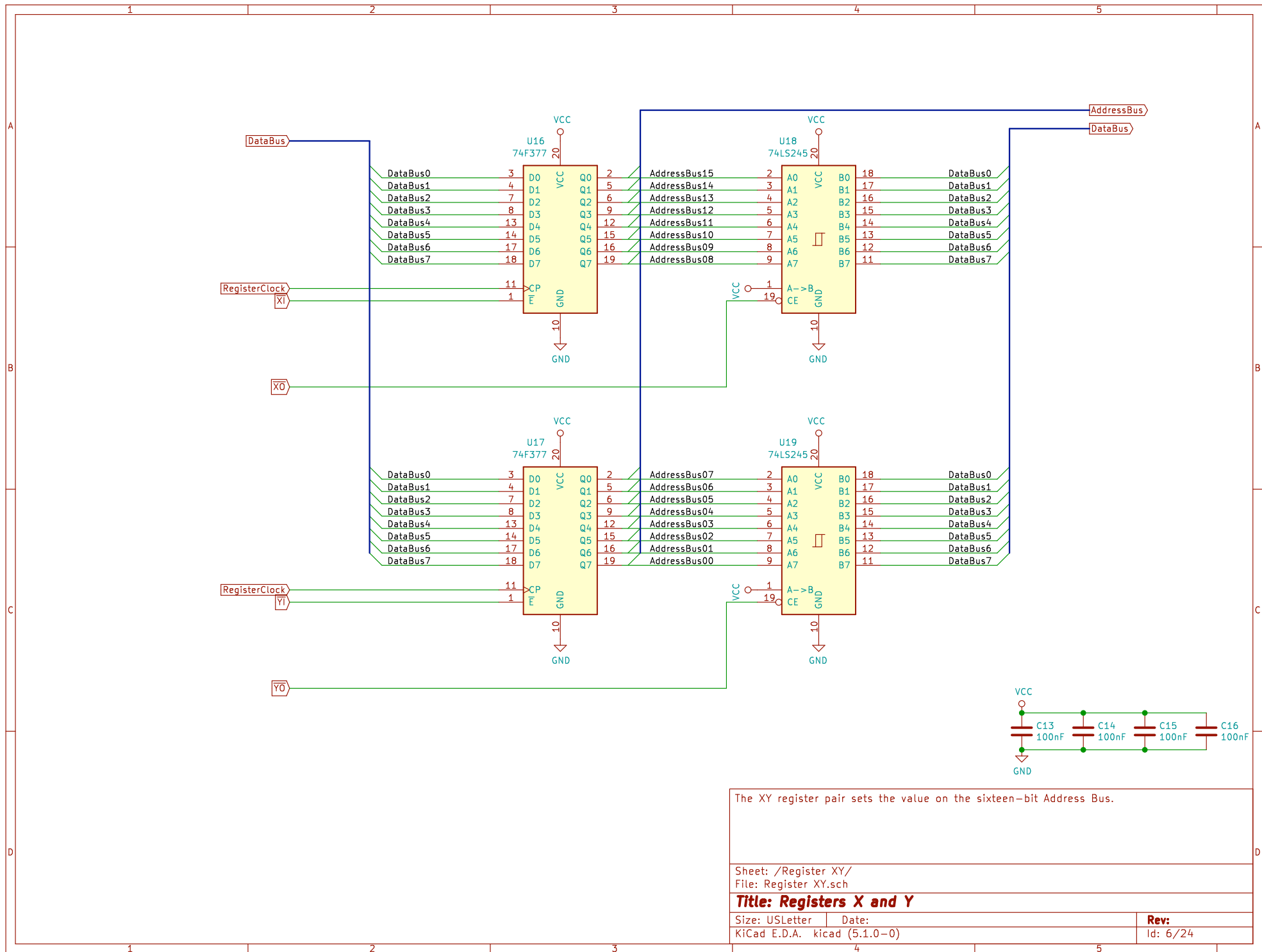
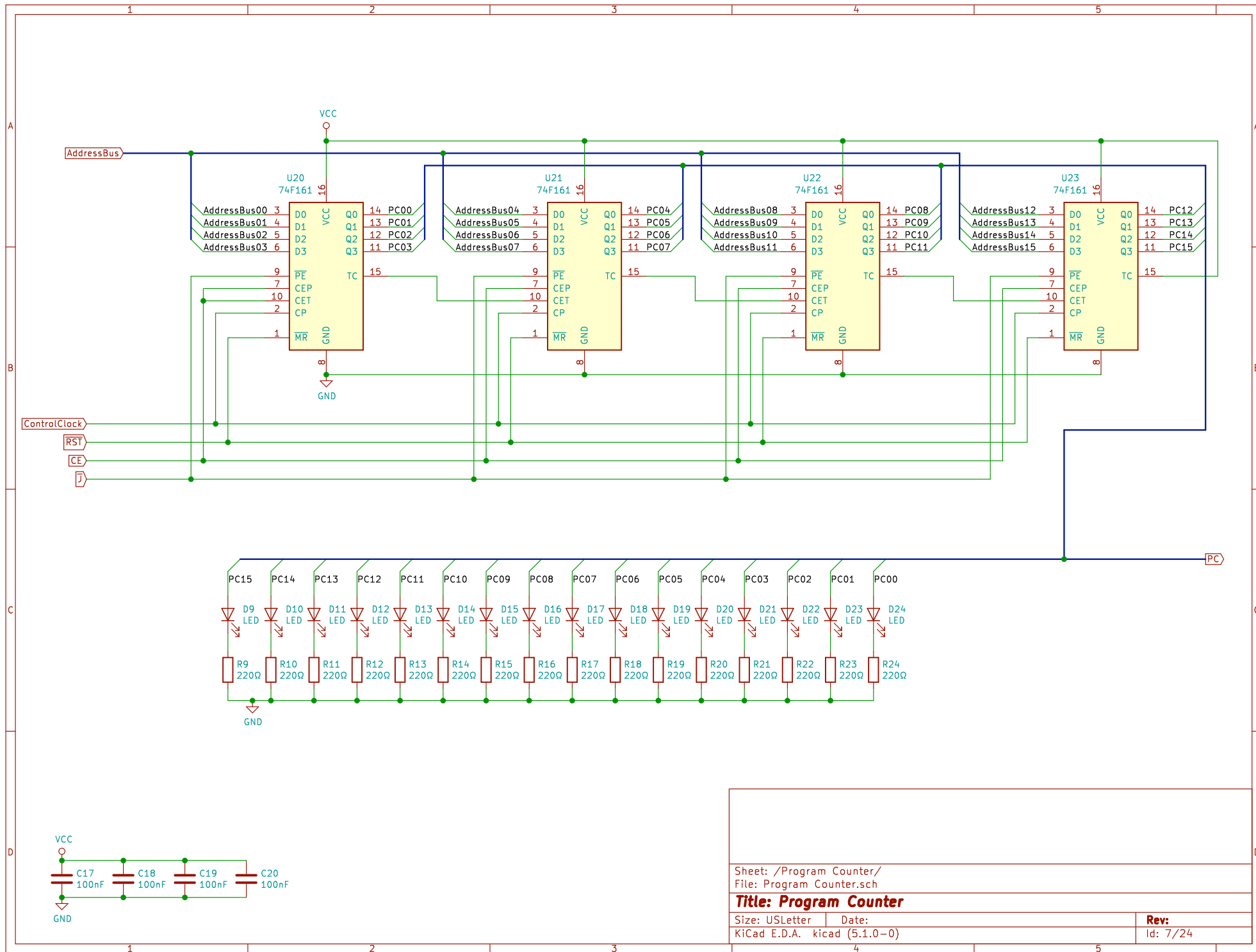


An Arduino Nano serves as a serial interface module.	
Sheet: /Serial/ File: Serial.sch	
Title: Serial I/O	
Size: USLetter	Date:
KiCad E.D.A. kicad (5.1.0-0)	Rev: Id: 4/24







Sheet: /Program Counter/
File: Program Counter.sch

Title: Program Counter

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 7/24

1	2	3	4	5	6
A					A
B					B
C					C
D					D
1	2	3	4	5	6

Sheet: PC/IF

File: PC_IF.sch
Sheet: Instruction ROM

Sheet: Instruction RAM Address

File: Instruction RAM Address.sch
Sheet: Instruction RAM

File: Instruction ROM.sch
Sheet: Instruction Register

File: Instruction RAM.sch

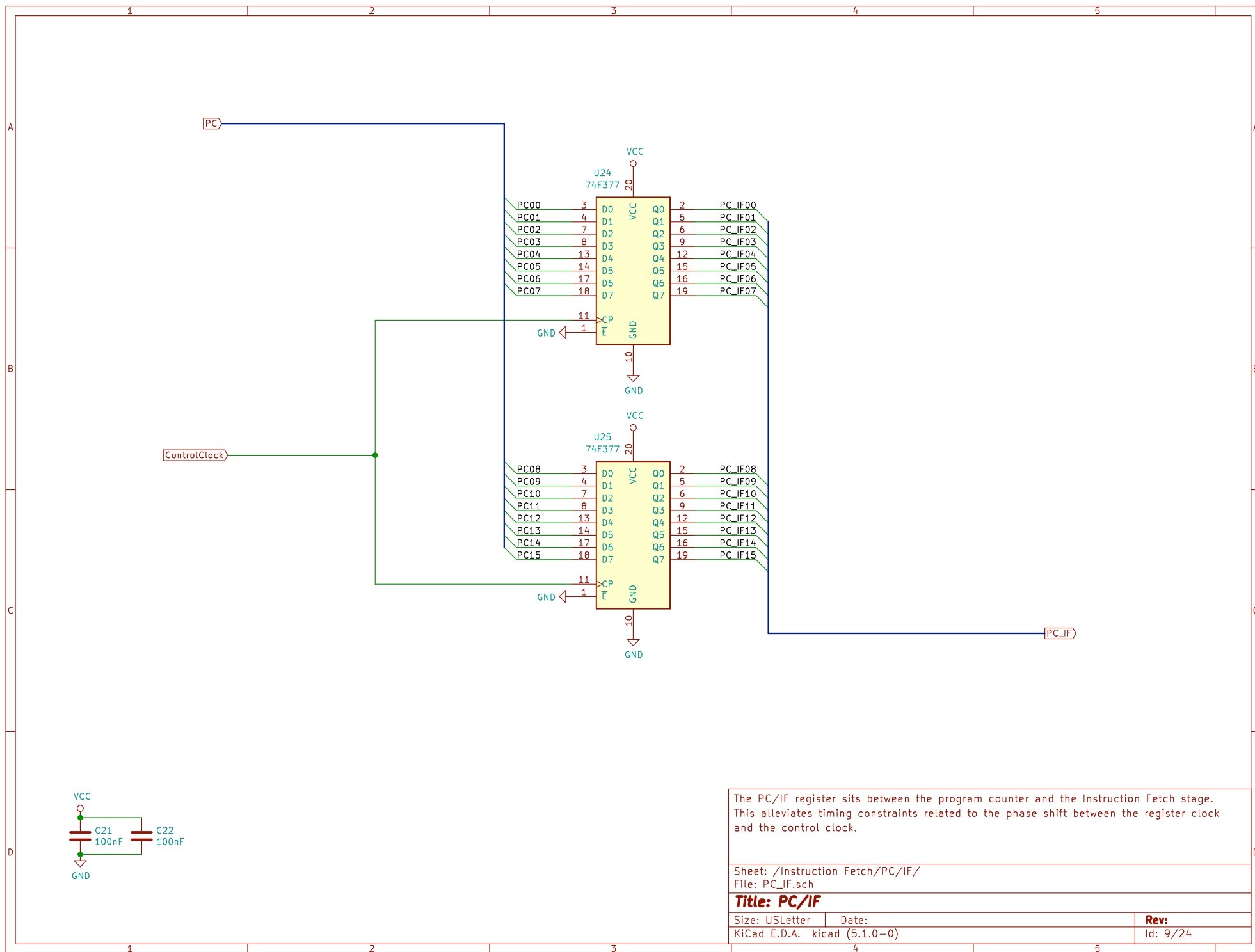
File: Instruction Register.sch

Instructions can be fetched from either Instruction ROM or Instruction RAM.
The lower 32KB of the address space is mapped to ROM, the remainder to RAM.

Sheet: /Instruction Fetch/
File: Instruction Fetch.sch

Title: Instruction Fetch

Size: A4	Date:	Rev:
KiCad E.D.A. - kicad (5.1.0-0)		Id: 8/24



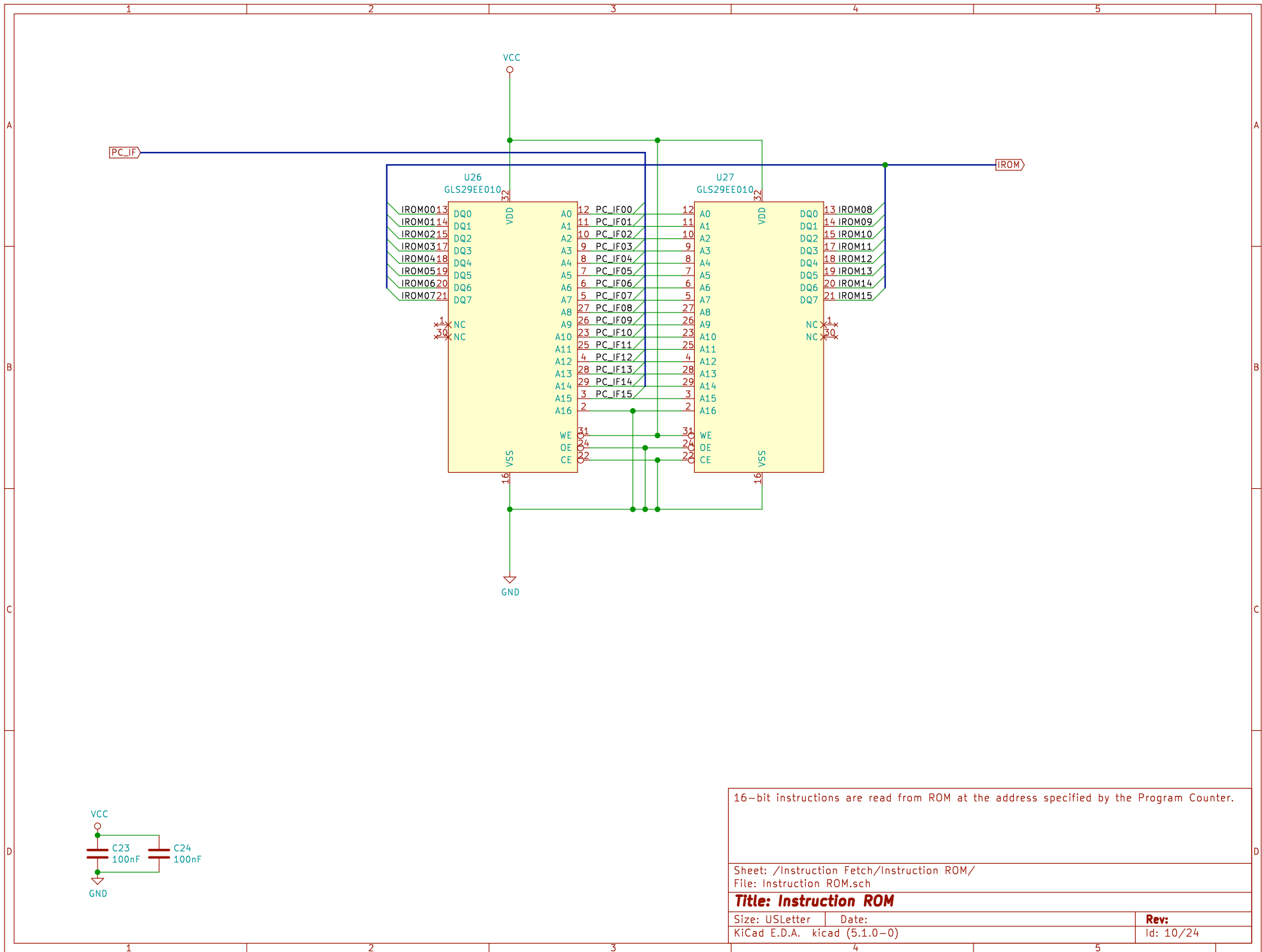
The PC/IF register sits between the program counter and the Instruction Fetch stage. This alleviates timing constraints related to the phase shift between the register clock and the control clock.

Sheet: /Instruction Fetch/PC/IF/
File: PC_IF.sch

Title: PC/IF

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
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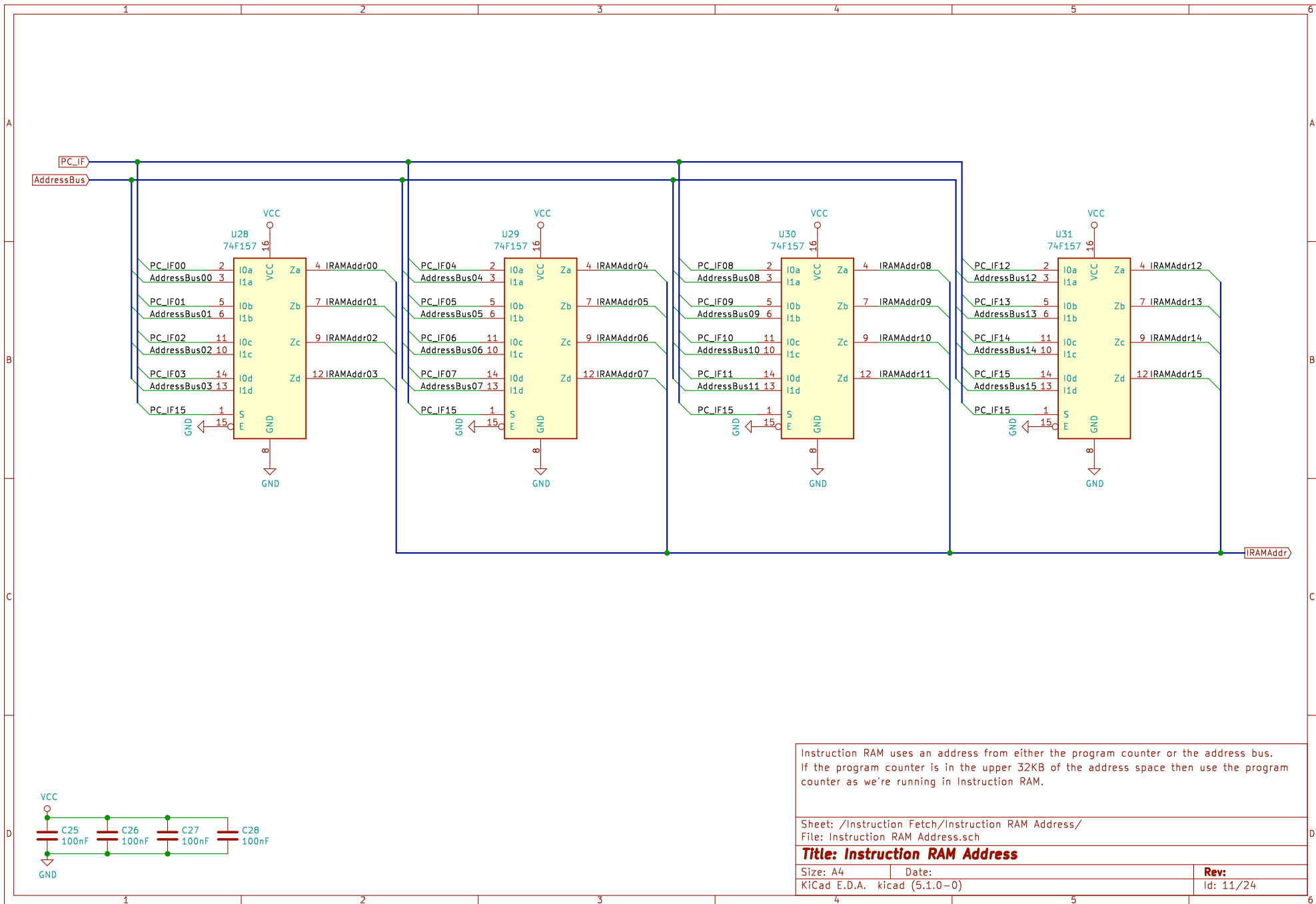
16-bit instructions are read from ROM at the address specified by the Program Counter.

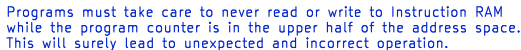
Sheet: /Instruction Fetch/Instruction ROM/
File: Instruction ROM.sch

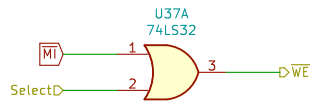
Title: Instruction ROM

Size: USLetter Date:
KiCad E.D.A. kicad (5.1.0-0)

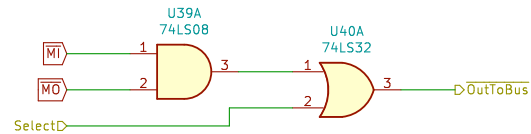
Rev:
Id: 10/24





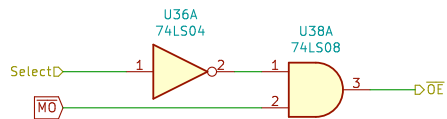


Only write to the Instruction SRAM when the MI signal is active and the appropriate plane of Instruction RAM is selected.



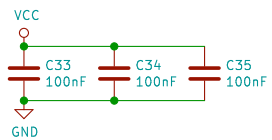
The bus transceiver should connect the Instruction SRAM to the Data Bus when the plane is selected and wither MO or MI is active.

The direction of the bus transceiver must also be set appropriately. This is done elsewhere.



Always output from Instruction SRAM when the plane of Instruction RAM is deselected. This allows RAM to be read for use in IF.

Else, if the plane is selected then only read from SRAM when the MO signal is active.



Logic for the control signals which drive Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM/Lower Instruction RAM Control/
File: Instruction RAM Control.sch

Title: Instruction RAM Control Logic

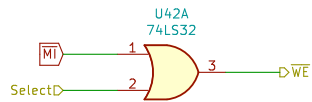
Size: A4

Date:

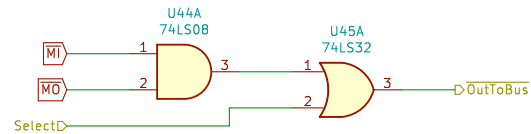
Rev:

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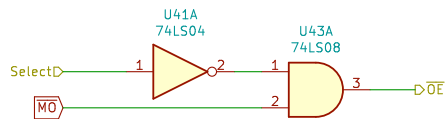


Only write to the Instruction SRAM when the MI signal is active and the appropriate plane of Instruction RAM is selected.



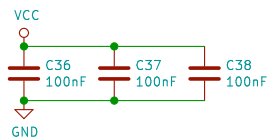
The bus transceiver should connect the Instruction SRAM to the Data Bus when the plane is selected and wither MO or MI is active.

The direction of the bus transceiver must also be set appropriately. This is done elsewhere.



Always output from Instruction SRAM when the plane of Instruction RAM is deselected. This allows RAM to be read for use in IF.

Else, if the plane is selected then only read from SRAM when the MO signal is active.



Logic for the control signals which drive Instruction RAM.

Sheet: /Instruction Fetch/Instruction RAM/Upper Instruction RAM Control/
File: Instruction RAM Control.sch

Title: Instruction RAM Control Logic

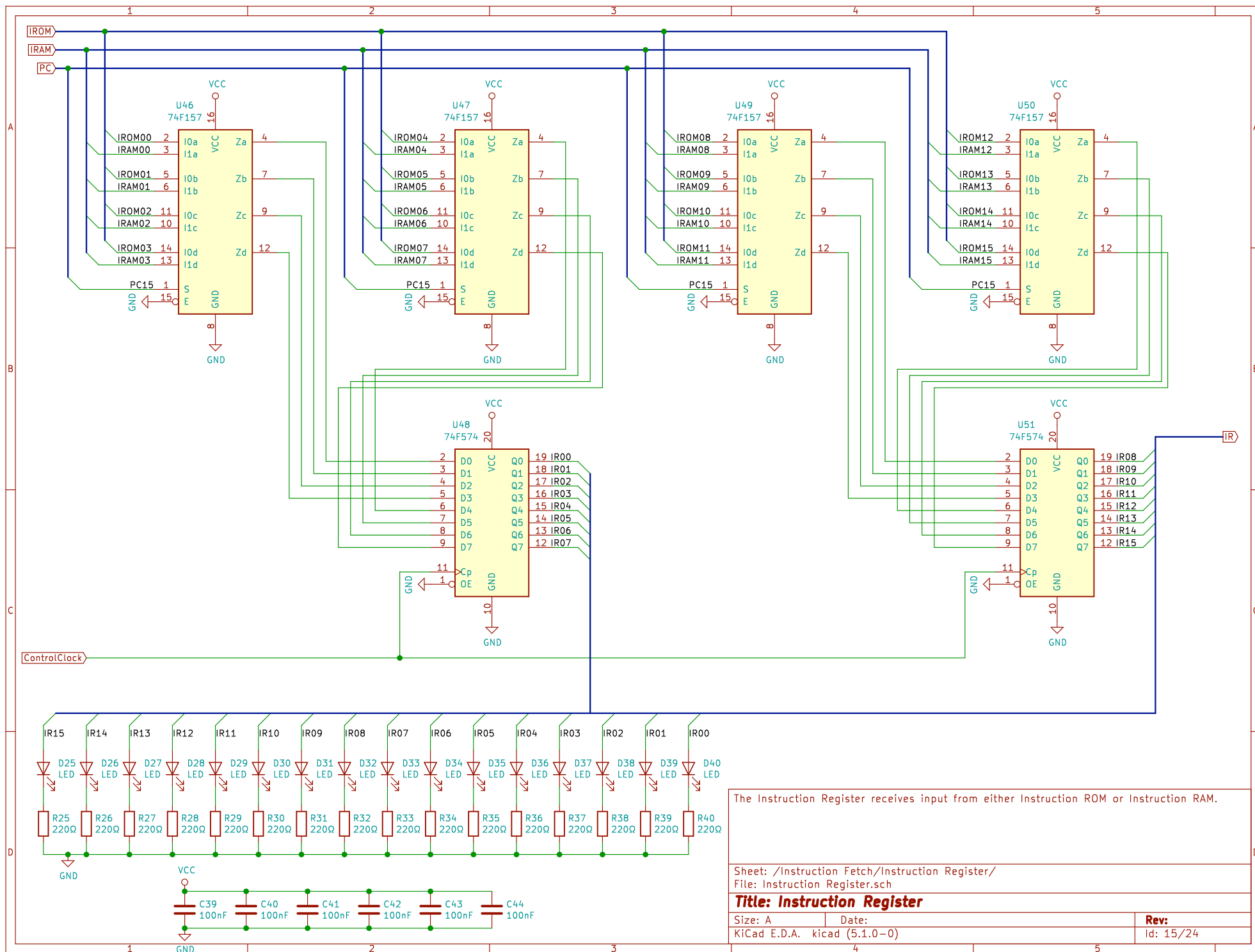
Size: A4

Date:

Rev:

KiCad E.D.A. kicad (5.1.0-0)

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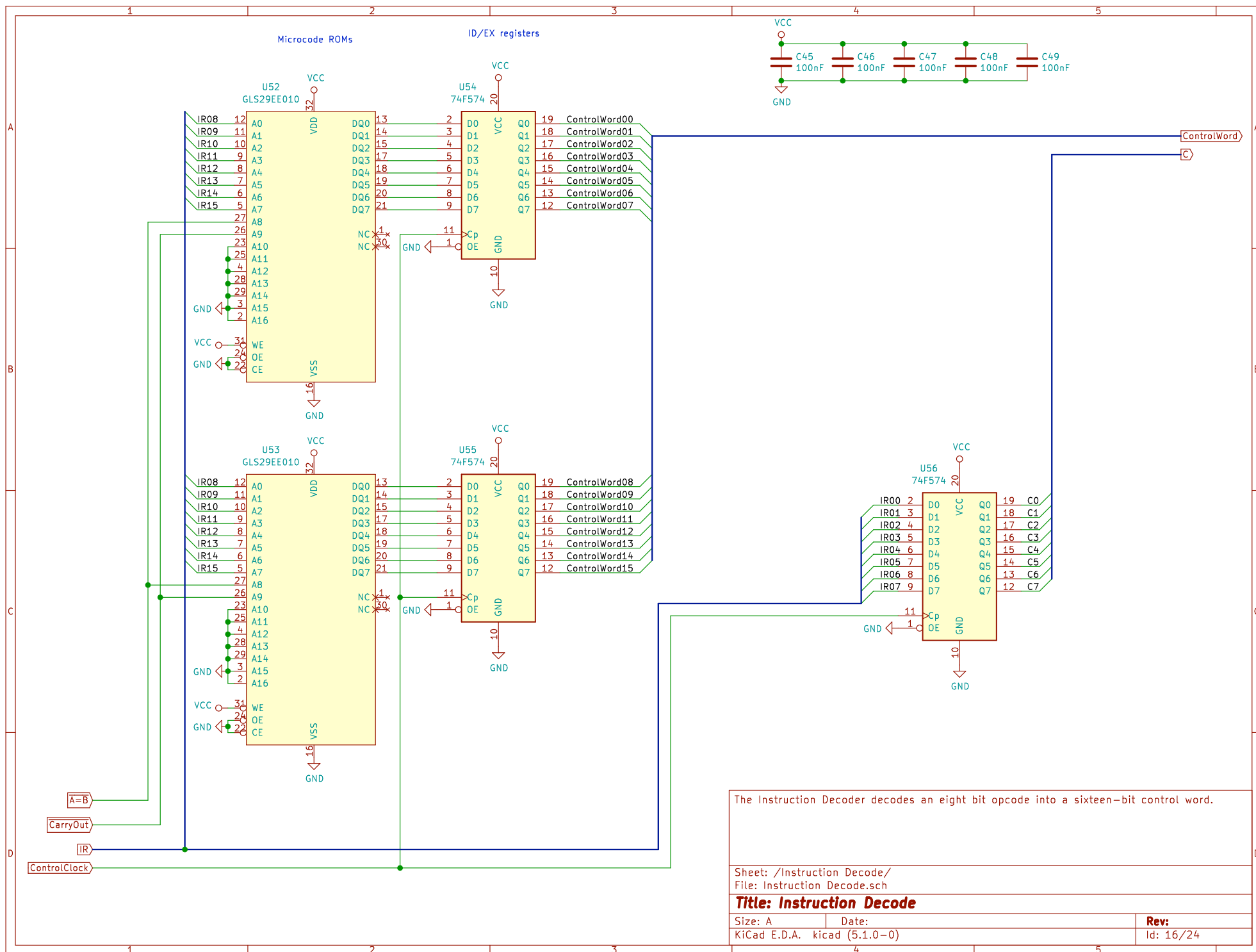
The Instruction Register receives input from either Instruction ROM or Instruction RAM.

Sheet: /Instruction Fetch/Instruction Register/
File: Instruction Register.sch

Title: Instruction Register

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 15/24



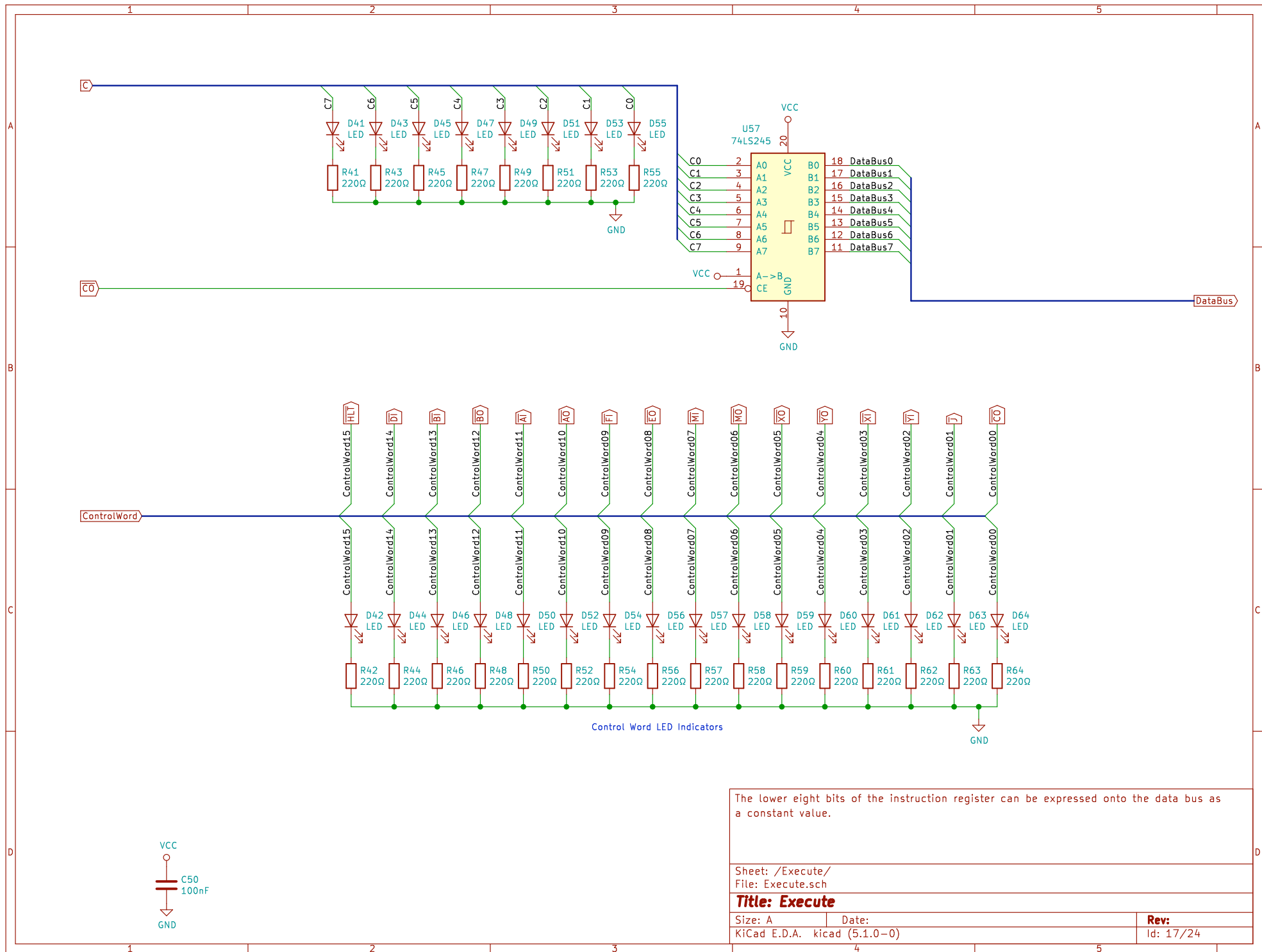
The Instruction Decoder decodes an eight bit opcode into a sixteen-bit control word.

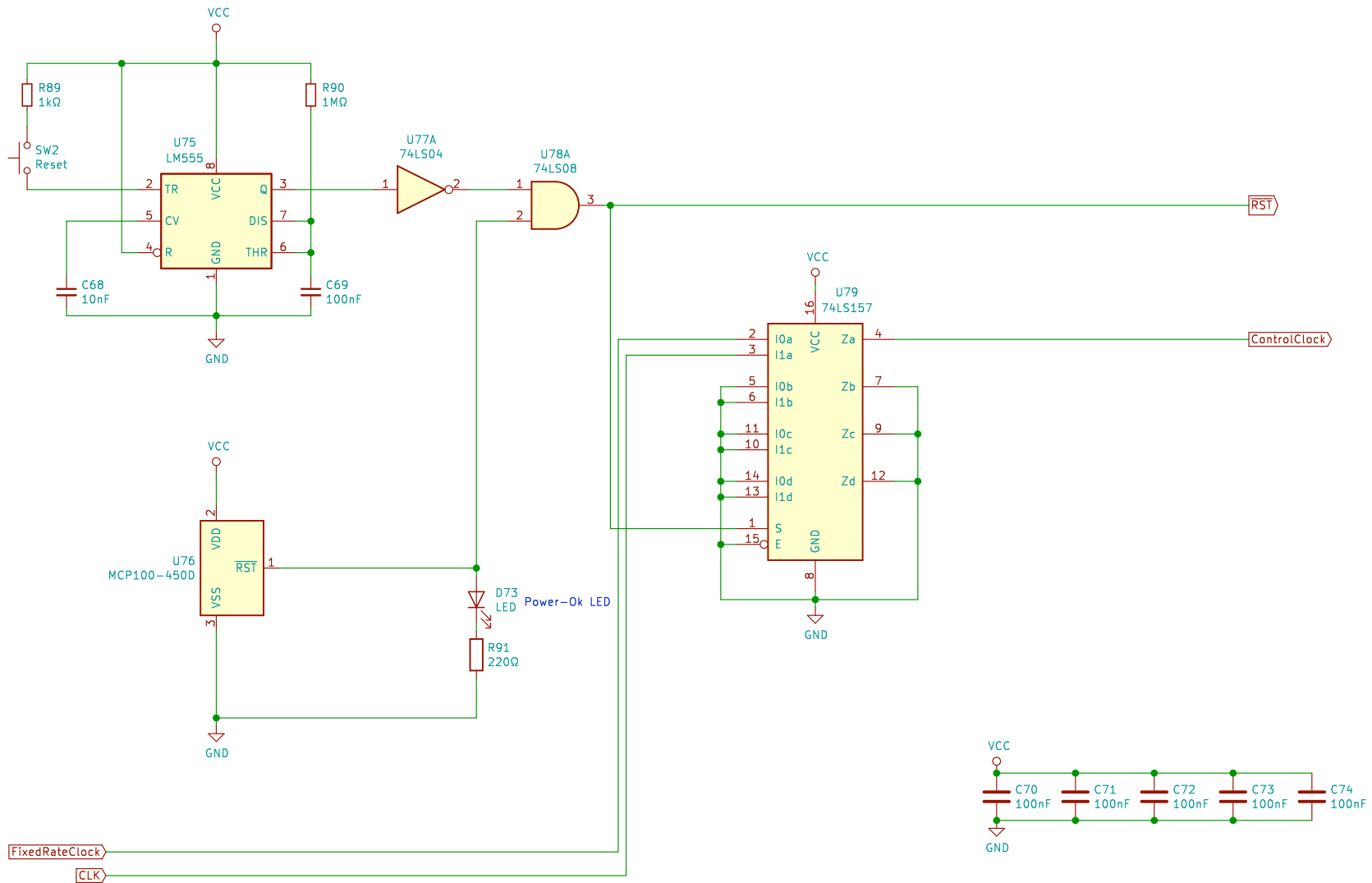
Sheet: /Instruction Decode/
File: Instruction Decode.sch

Title: Instruction Decode

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 16/24





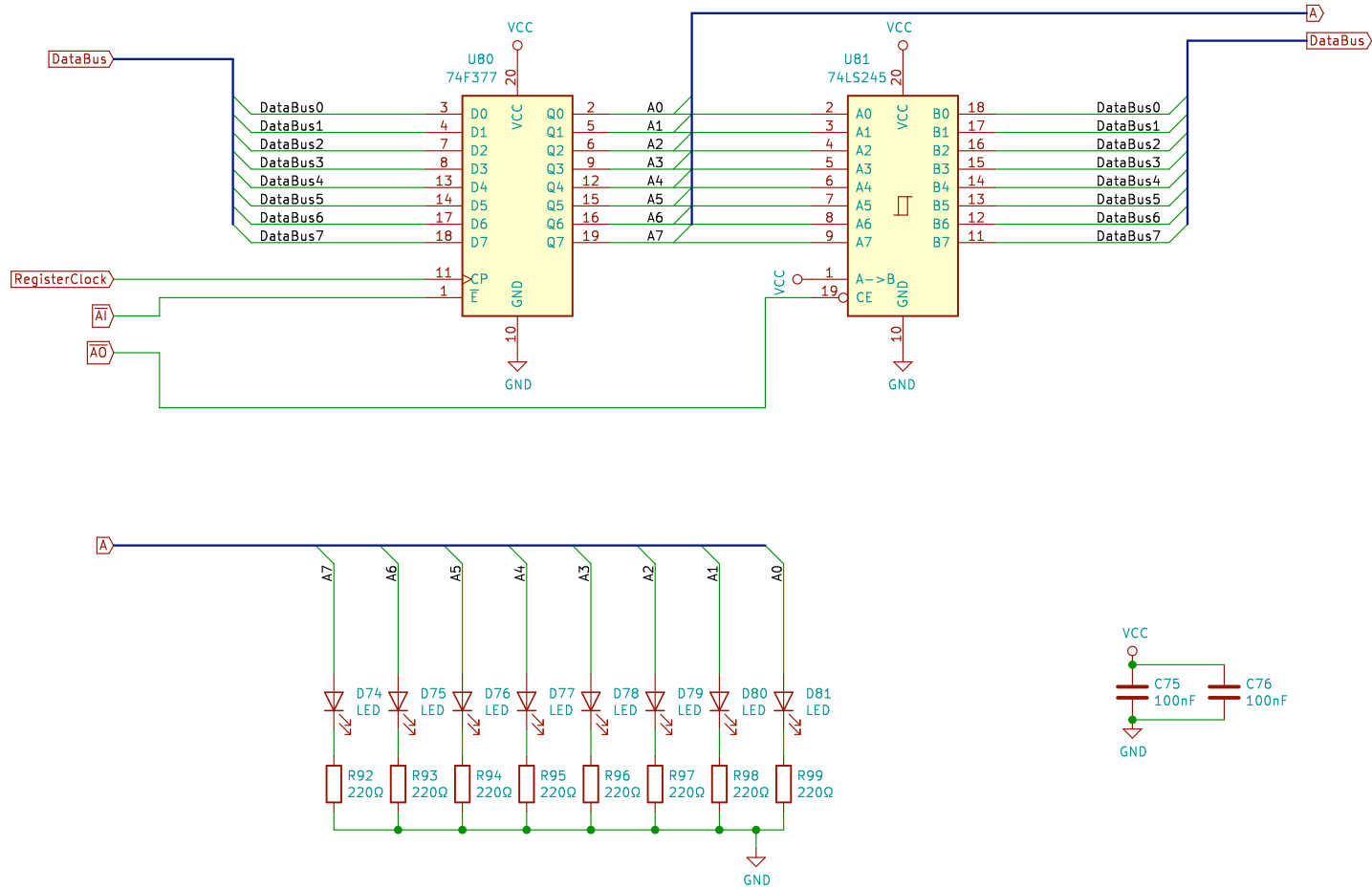
The MCP100 provides Power-on Reset functionality.
A button is also provided to manually reset the machine.
During reset, the control clock is pulsed repeatedly to flush the pipeline.

Sheet: /Power-on Reset/
File: Power-on Reset.sch

Title: Power-on Reset

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 20/24



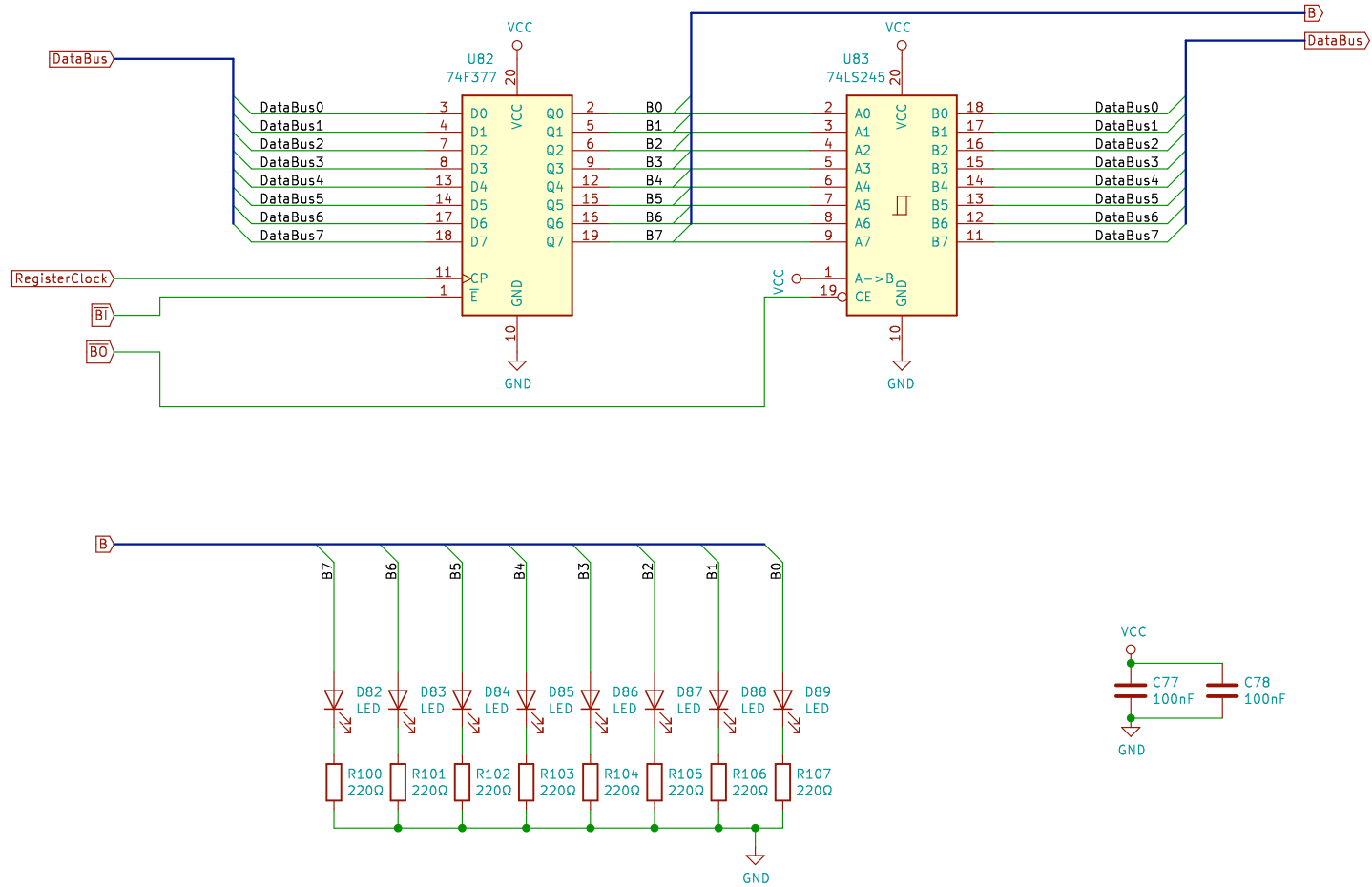
Register A is wired to the ALU's A operand.

Sheet: /Register A/
File: Register A.sch

Title: Register A

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 21/24



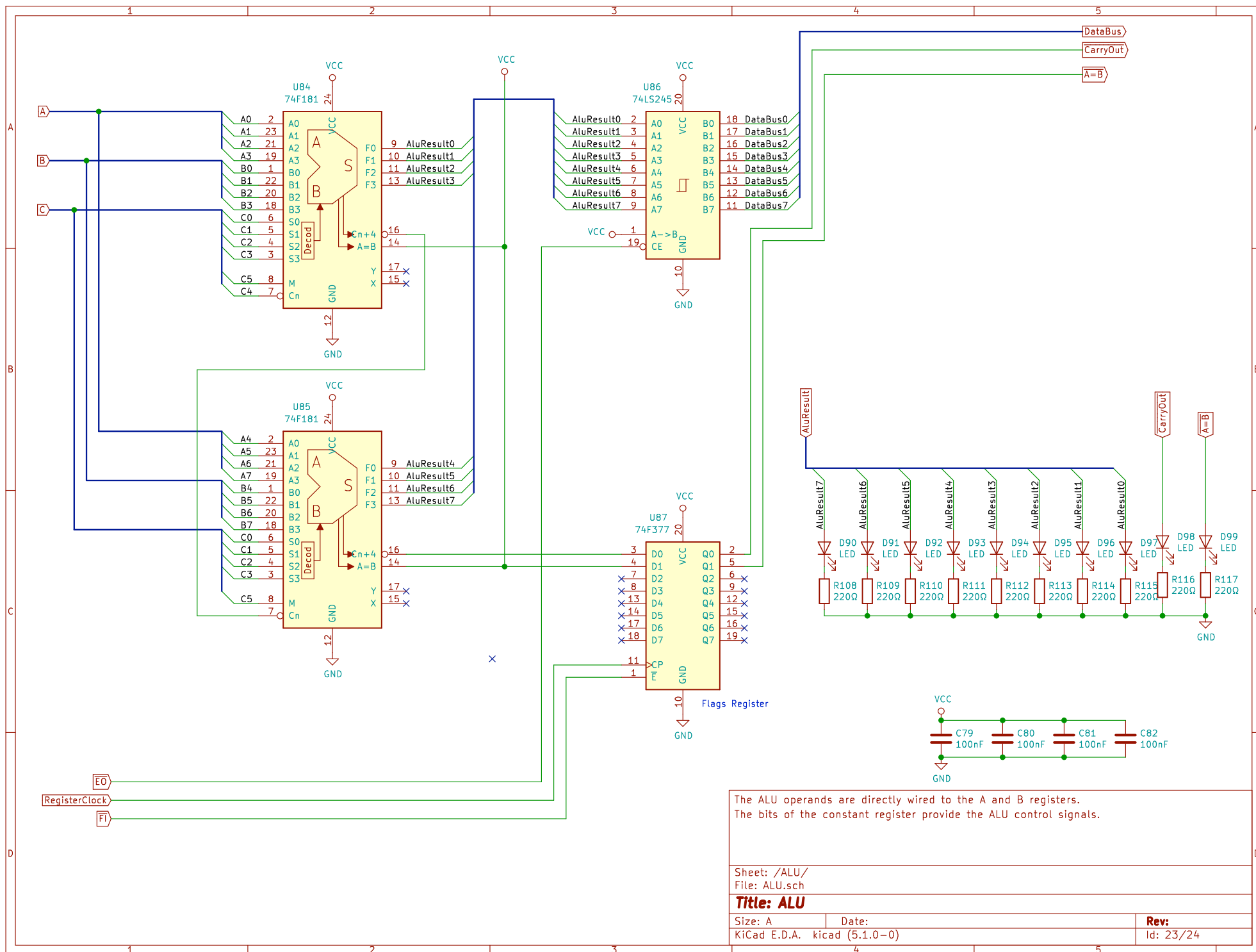
Register B is wired to the ALU's B operand.

Sheet: /Register B/
File: Register B.sch

Title: Register B

Size: A Date:
KiCad E.D.A. kicad (5.1.0-0)

Rev:
Id: 22/24



The ALU operands are directly wired to the A and B registers. The bits of the constant register provide the ALU control signals.	
Sheet: /ALU/ File: ALU.sch	
Title: ALU	
Size: A	Date:
KiCad E.D.A. kicad (5.1.0-0)	Rev: Id: 23/24

