Analysis of CMOS 2 power supply problem

Apr 3 2024

Background

Monday, April 1 2024

- While troubleshooting Formatter filesystem and umbi connection, we heard (from Mario on PLC) that the Exp current was 0.7 A after power application. This was consistent.
- Later on Monday, without Formatter working, we tried commanding CMOS 2 power on using the direct GSE to Housekeeping connection. We saw no change in current (from 0.7 A) and assumed CMOS 2 was not turning on. We were able to excite changes in current (with expected magnitude) by commanding the Housekeeping board to power on CMOS 1 and Timepix. At that point we powered off the system, to avoid risks related to the power anomaly.

Friday, March 29 2024

- NSROC put the integrated payload on the cart with big wheels and rolled outside for GPS/Iridium tests. During these tests, the Exp. power was turned on, but subsystems (detectors) were not turned on. After the rollout test, Exp. was mounted on the rail.
- During the rollout, the Exp. drew 0.7 A when powered on. This indicates CMOS 2 was powered on for the test.
- Detail:
    - Test started with transmitter on, drawing 1.22 A from TM2 bus.
    - After Exp. bus powered on by NSROC, 2.08 A from TM2 bus.
    - Diff is 0.86, which is expected for Formatter + CMOS 2 boot up.

Wednesday, March 27 2024

- Sequence tests were conducted in the PAB.

run1, sequence test 1, all-fire

- CMOS 2 was powered normally during run1 (sequence 1, all fire).
    - Evidence: started pcap recording on GSE computer at 2:24 pm. The first telemetry packet (destination 224.1.1.118:9999) arrives at 2:39 pm from CMOS 1, after the power-on command is sent to both CMOSes.
- During this test, there was a battery voltage drop of 1.2 V. Thanasi add power plots after get data from Garrett.
    - From notes from NSROC engineers, the TM2/Exp battery pack dropped 1.2 V when switching to internal power during this test. The test continued successfully after that point. CMOS 2 was powered on at this point. The switch to internal power occurred at 3:10:10 pm local time.
    - A CMOS 2 packet was received at 3:10:11 pm, and CMOS 2 data continued to be received for the rest of the test.

run2, sequence test 2, no-fire

- CMOS 2 appears to be powered with Exp. power during run2 (sequence 2, no fire).
    - First CMOS 2 packet received at 4:36 pm. This is before I indicate in the notes that CMOS 2 is turned on. More detail on timing:
    - 4:36 pm Exp power on (this is reflected in the notes, and we get the first MDNS packets from 192.168.1.8 in the pcap at this time). Granular:
        - 4:36:44 pm get first packet (MDNS) with ip.src == 192.168.1.8. Indicates Formatter has finished boot at this time.
        - 4:36:50 pm get first packet heading to 192.168.1.100. Indicates main formatter software has started at this time.
        - 4:36:54 pm get first UDP packet with header indicating CMOS 2 source. CMOS 2 must be booted at this time.
        - 4:43:49 pm powered on and received first packet from CMOS 1.

sequence test 3, power backup

- The last test of the day was the power backup sequence, which is very short. We did not turn on Exp. subsystems or record Exp. data for this test, but we believe CMOS 2 turned on with the Exp. during this test.
    - Need to check current record from this test. Mario has notes.

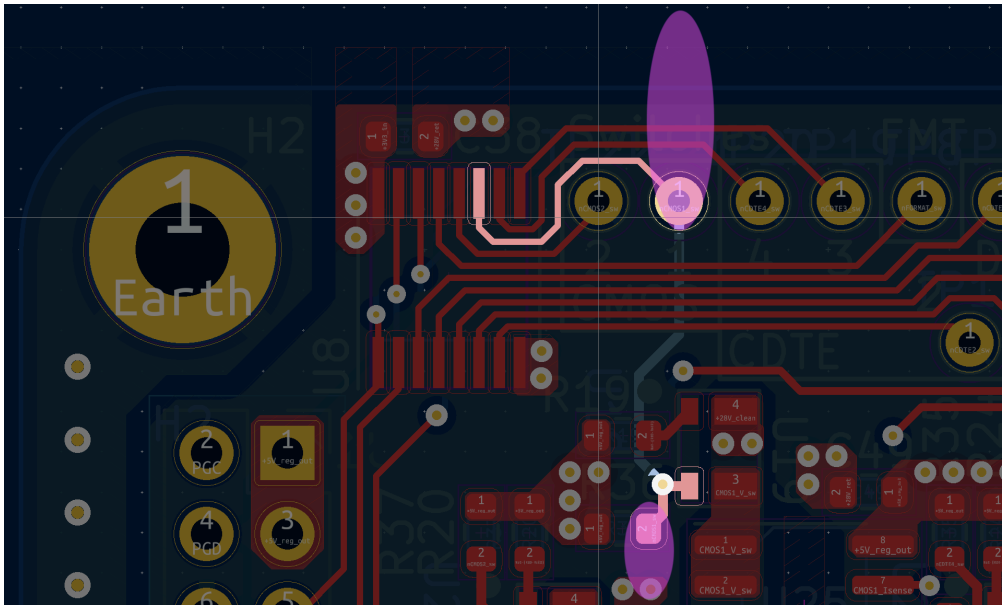
Possible causes

Wait. In everything that follows, I am looking at traces labeled "CMOS1" on the Power board. In the flight integration, the Power board output pins labeled "CMOS2" got harnessed to CMOS 1, and vice versa. So we need to look at signals labeled "CMOS1" on the power board.

`nCMOS1_sw` shorts

This signal controls the gate of an optically isolated MOSFET. Tying it to GND will cause power delivery.

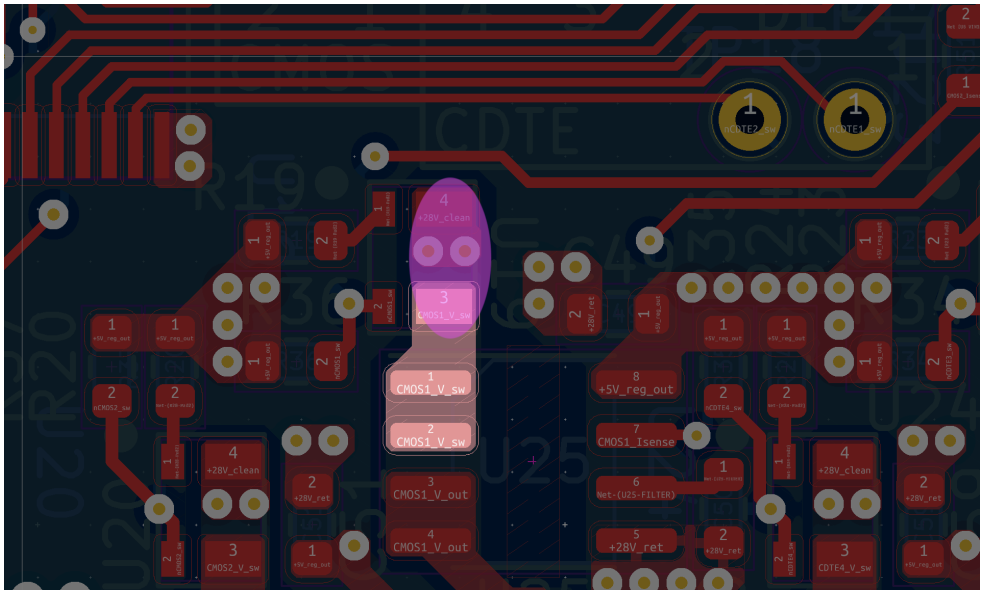
The signal `nCMOS1_sw` is covered in epoxy on the MAX7317 chip leg. There are two other possible short sites for this trace. The upper site would need to contact the box, either by wearing through Kapton located between the PCB and the box shelf, or via FOD at least 150 mil long, jumping the testpoint to the box.



The lower site could be caused by FOD ~70 mil long, but the placement appears quite unstable (between caps or pads of two 0603 components). I would be surprised if, e.g., a conductive fiber settled and stayed in this location.

`CMOS1_V_sw` shorts

This is the power line to CMOS 2 after the optically isolated MOSFET that turns it on/off, and before it passes through a Hall effect current sensor.



One possibility is for the opto-isolated MOSFET to fail closed. I don't know what failure modes to expect from this MOSFET. I would expect significant overvoltage (>60 V) or overcurrent (>3 A) would be needed to damage the part in this way.

Another possibility is for FOD to settle alongside the MOSFET, shorting pad 4 to pad 3 (jumping `+28V_clean` directly into `CMOS1_V_sw`). This is directly in the current path to CMOS 2, so we would need FOD that forms a stable connection carrying ~0.4 A, 28 V. That sounds unlikely to me.

A short between `+28V_clean` and `CMOS1_V_sw`

This would mean +28 V goes directly out to CMOS 2 all the time, first passing through the Hall effect current sensor.

A short between `nFORMAT_sw` and `nCMOS1_sw`

- These signals are on the power board.
- They are pulled low to turn on Formatter/CMOS 2.
- The Formatter is pulled low by default (always on). The pullup is a relatively strong 680 Ω resistor.
- The CMOS 2 enable line is pulled up (to 5V) by default using a weak 10 kΩ pullup resistor (same as all other detector systems).
- If a short is present between these two signals, the Formatter pulling down would win, and CMOS 2 would turn on.
- The chip (MAX7317) driving these signals (`nFORMAT_sw` and `nCMOS2_sw`) is controlled via SPI communication from the Housekeeping microcontroller.
- The MAX7317 outputs are open-drain.
- The MAX7317 port P9 controls the Formatter. The MAX7317 port P8 controls CMOS 2. These are adjacent pins (12 and 13) on the package.
- In the flight power board build, it appears R26 and R14 are both populated.

Table:
(Italicized rows are nominal power-on states with and without a short between MAX7317 P9 and P8).

Short	MAX P9	MAX P8	nFORMAT_sw	nCMOS2_sw	Formatter	CMOS 2
Absent	*open*	*open*	*5V*	*5V*	*On*	*Off*
Absent	open	closed	5V	GND	On	On
Absent	closed	open	GND	5V	Off	Off
Absent	closed	closed	GND	GND	Off	On
Present	*open*	*open*	*5V*	*5V*	*On*	*Off*
Present	open	closed				
Present	closed	open				
Present	closed	closed				

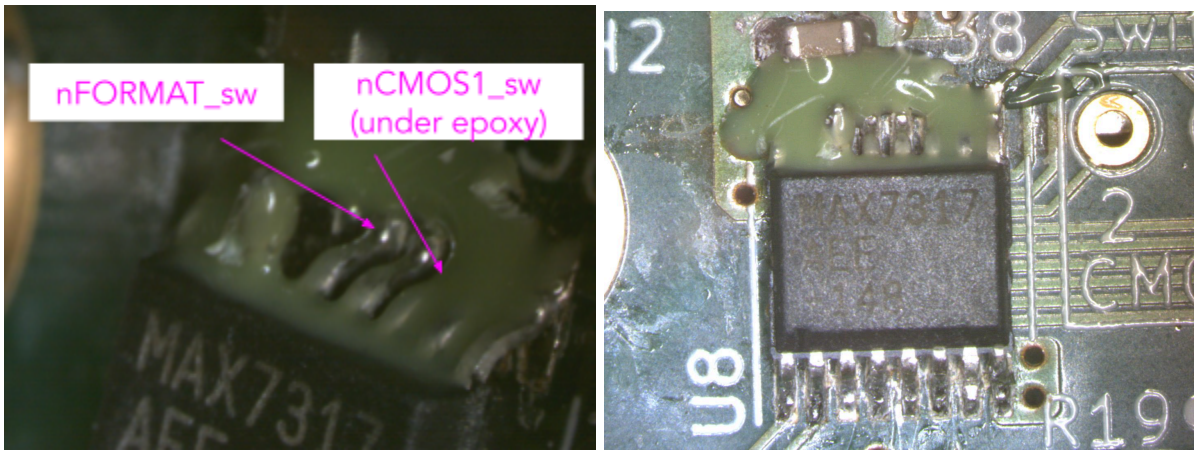
From the above, this sounds really unlikely. Also realized that CMOS 2 is the wrong signal on the PCB, we should be checking CMOS 1.

See run2 and run3 from Apr 3 testing. I believe this test rules out this failure mode.

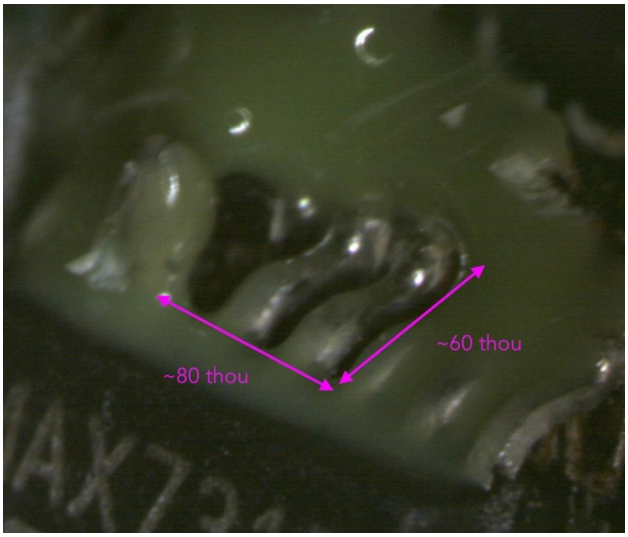
Aside for Housekeeping implementation detail:

- If the HK microcontroller receives the command 0x03 0x09 0x01 (cycle Formatter power), it is handled as a special case, which does:
    1. Set 0x00 to the MAX7317 output register
    2. Wait 1 ms
    3. Set 0x01 to the MAX7317 output register
- This does:
    1. Take the `nFORMAT_sw` signal from floating—but (effectively) pulled to ground through the opto-isolated MOSFET's LED + 680 Ω current limiter—into an open-drain state. In this case, both sides of the LED will be at `GND`, and the MOSFET will have no drain to the Formatter.
    2. Wait 1 ms
    3. Put `nFORMAT_sw` back into a floating state, so the opto LED anode will see pullup to 5 V again.

Board photos



The Formatter and CMOS 2 enable pins are the two visible pins on the left photo. These were taken prior to the flight vibe test at SSL.



The above photo has rough dimensions of exposed area annotated. A conductive object would need to have size <80 thou, or a radius of curvature <80 thou at the point it contacts the chip in order to cause a short. And come in at the right angle, settle stably (through launch and shipment), etc.

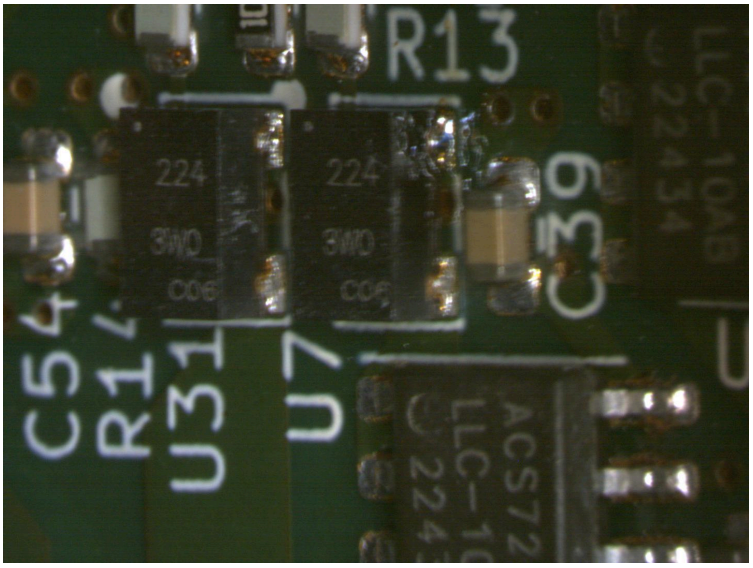
G3VM-61WR failure modes

A possibility is failure (into a S-D short) of the opto-isolated MOSFET that controls power output to CMOS 2.

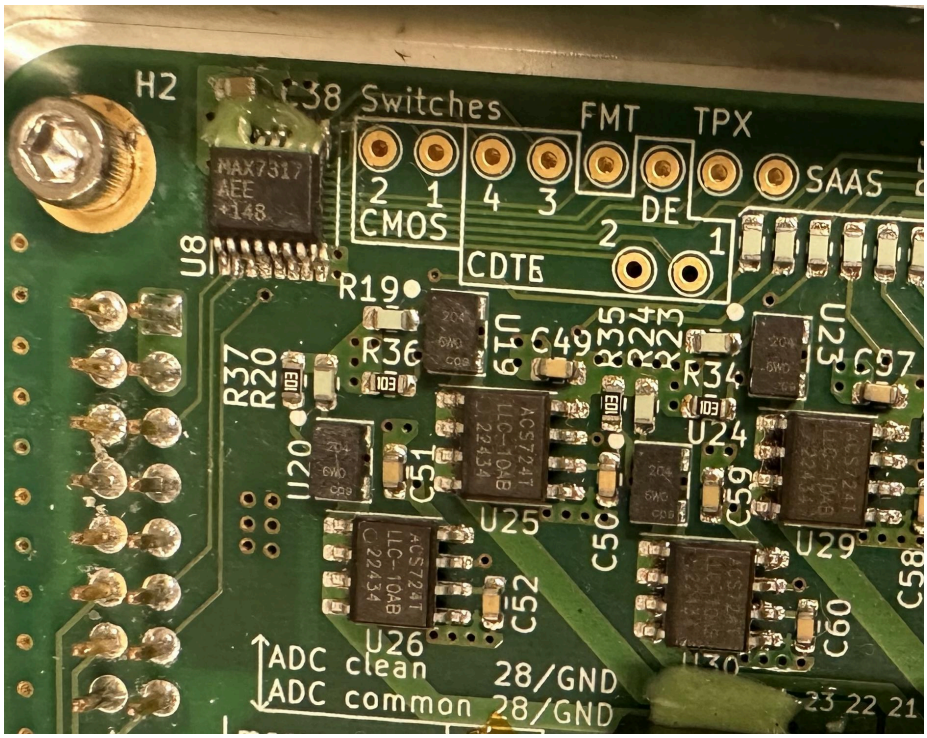
This is the MOSFET. We are using the -61WR variant for CMOS 2, which has higher voltage rating (60 V) but lower current rating (3 A) than the -31WR variant, which we are using for Formatter, DE, etc. I checked the company's Precautions document for their MOSFETs, found no usable information about failure.

The correct variant of the part is indeed populated on the board, this was visually verified post-flight.

- From board photos, the -31WR variant has cap markings 224 / 3W0 / C06:



- From the datasheet, the marking "3W0" is consistent with the -31WR variant.
- Here is the 28 V side of the board:



- Looks like the cap is marked something like 204 / 6W0 / C09
- From the datasheet, the marking "6W0" is consistent with the -61WR variant.
- So we don't have the wrong MOSFET in place.

Latchup? Would expect it to clear after power cycle. Need some current or voltage pulse on each power-on to excite.

G3VM-61(WR) on-die failures

Sep 23, 2024. In preparation for receiving power board back in MN.

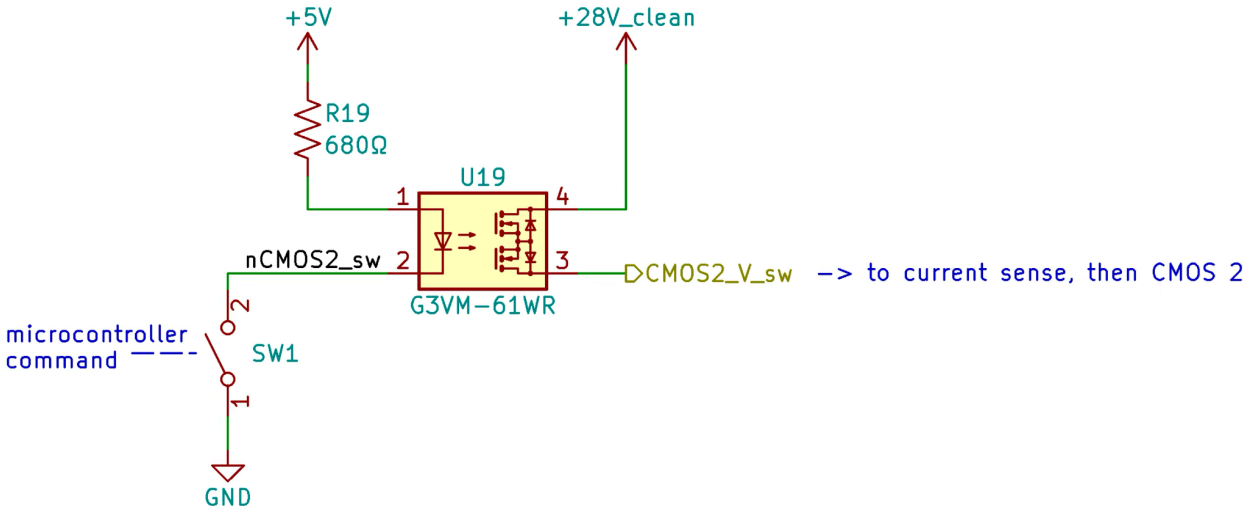
Omron provides a list of precautions for their MOSFET relay products. The G3VM-61(WR) has an LED with InGaAs chemistry.

Some thoughts:

- Failure could be a fused short of the LED (always on), or a drain-source short of the MOSFET. Should be able to tell which one simply by lifting the chip and probing the pins.
- Decapping the chip may lead give use the same information. Could we learn anything about the failure mechanism by decapping? Or just failure mde?
    - Decapping service: reach out to MN Nano Center (in PAN), see if they have capability.

LED failure by circuit design

A generic output switch on the power board has this design:



For the CMOS 2 switch, the G3VM-61WR variant is used instead, but the ballast resistor is the same. The current through the LED is

$$I = \frac{V - V_{fwd}}{R}$$

Using the measured value of the 5 V line (5.35 V) and an LED forward voltage of 1.22 V (from the datasheet), the current is 6 mA. This is larger than the minimum turn-on current of the LED, and much smaller than the maximum allowable current through the LED (30 mA).

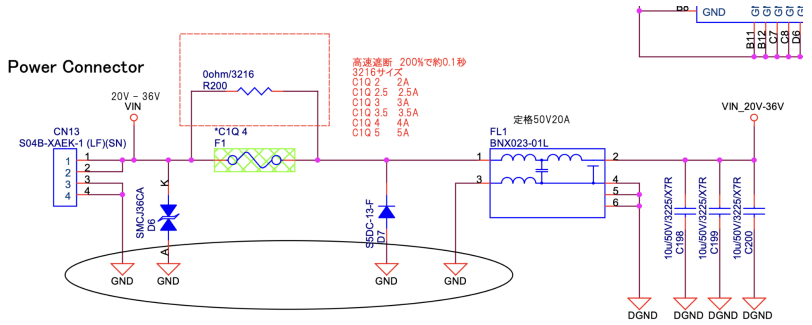
Looking up this forward current value in the Omron the precautions plots, they expect an operating life above 10^7 hours for a 0.1% component failure rate (1 in 1000 parts fail).

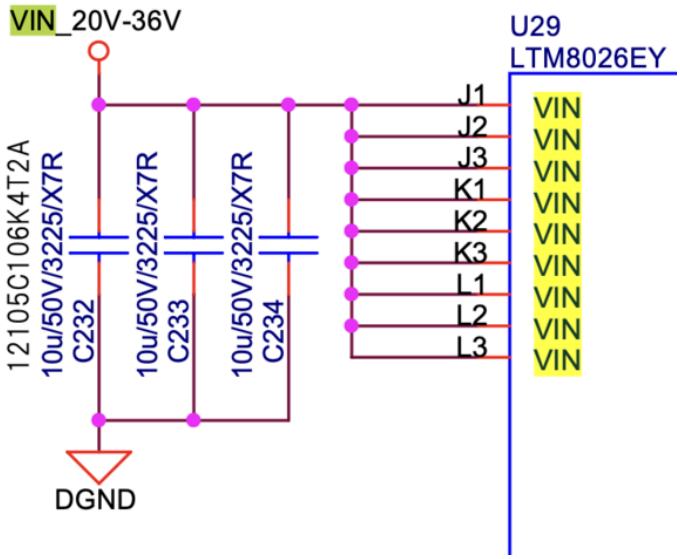
So we are well within the design range for the LED. With board in-hand, check ballast resistor value.

Overcurrent on inrush

The G3VM-61(WR) is rated for 3 A continuous output current, and 9 A pulse current (duration ~10 ms). Is it possible the 9 A pulse limit was exceeded during a turn-on transient?

Here are two clippings of CMOS input power line (VIN_20V-36V):



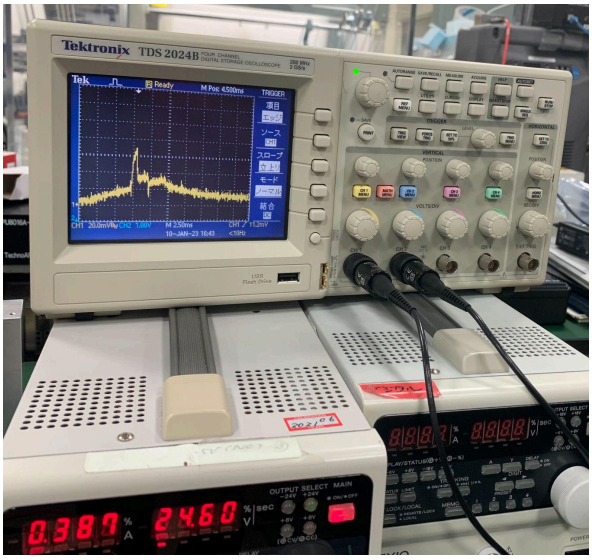


The total input capacitance visible here is ~60 µF. The BNX023-01L input filter used has series resistance ~0.5 mΩ. The D-S resistance (R_on) of the G3VM-61(WR) is 40-60 mΩ at operating temperature. I estimate the BNX023-01L to have ~27 nH inductance from the plot of its frequency response. Plugging all these into an RLC circuit simulation, I get a step response that is definitely overdamped. There is no ringing above 28 V. To excite any ringing with these parameters, parasitic inductances >130 µH would be needed.

A plot of the loaded CMOS 1 (normally functioning) output indicates a rise time of ~1 ms. This implies inrush < 1.5 A for a load capacitance of ~60 µF, far below any absolute limits of the SSR.

Also, CMOS 1 has been turned on and off hundreds of times, in many different ambient conditions, without issue.

On Jan 10 2023, I conducted an inrush current test with a bench supply EM CMOS board. Inrush was measured by probing the voltage across a 0.05 Ω, 0.1% resistor in series with the load. That produced this plot:



in which the voltage drop across the ballast resistor rises ~60 mV, giving a peak inrush current of 1.2 A. So it seems the design analysis is close to actual system performance.

So at first glance inrush issues *also* seem unlikely.

Post-flight lab work

Timeline of work

Oct 7 2024

We opened the power board enclosure, took photos, visually inspected, and performed basic multimeter tests to compare the faulty CMOS 2 channel to its functioning, but otherwise identical CMOS 1 counterpart.

- Probed out the LED (gate) side of the G3VM-61(WR) for CMOS 2 and compared to CMOS 1. Both are identical (in V_fwd, absolute voltages, etc) in both powered and unpowered conditions. So we rule out failure of the LED side of the SSR.
- In an unpowered configuration, the resistance across pins 3 and 4 of the faulty SSR (output legs) is 380 kΩ. Compare to the functioning counterpart, which probes fully open circuit across those pins.
- With 28.00 V applied to input (pin 4) of the faulty SSR and no output load, we see 27.6 V on the output side (a drop of 0.4 V across the channel).
    - This drop does not change at all when command CMOS 2 "on" (driving the LED).
    - The unloaded, faulty SSR shows no difference on a thermal camera from a functioning SSR.

Oct 9 2024

We loaded the CMOS 2 and CMOS 1 outputs with 90 Ω power resistor (~0.3 A load). This is close to the steady-state CMOS device current consumption. First we checked the CMOS 1 (nominal) channel under load, with 28.00 V input:

- Output voltage is 27.95 V.
- No noticeable heating of the G3VM-61(WR) for this channel with a thermal camera.

Then we loaded the faulty CMOS 2 channel with the same 90 Ω power resistors (removed from CMOS 1 output):

- Output voltage is 27.16 V (more drop than the unloaded case, which was 27.6 V).
- Significant heating of the faulty G3VM-61(WR) to ~50 °C.

Oct 10 2024

- There was a rattling noise when shaking the power board yesterday. Unscrewed it from housing. This was just stacking spacers in the HK/power interboard header shaking. They are fully captive thermoplastic (integral to the Samtec header) and shook the same way before flight. No risk.

Next steps

Recap:

- Failure occurred during or immediately after Sequence Test 1 (all-fire) in Poker, on March 27 2024. Symptoms were visible by start of Sequence Test 2.

- During Sequence Test 1, there was a battery failure that resulted in a 1.2 V drop on the 28 V input line from the bus. This occurred while switching to internal power.
    - If this failure induced significant transients on the 28 V line, those may explain the observed behavior.
    - I don't know how this switchover is done, or what the transients look like.

Redesign

For FOXSI-5, we should justify a redesign (or lack thereof) of this system. Without understanding the underlying failure mechanism it is hard to justify a design choice. Some options:

1. Choose a different SSR/FET with even higher current/voltage rating.
2. Add inline current limiting.
3. Add TVS diodes.
4. Add more input capacitance.