



DIGITAL LOGIC

CHAPTER FOUR: Sequential Logic Circuits (Part II)

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4.3 Clock Signals and Clocked Flip Flops

4.3.1 Introduction

- Clock Waveforms: A clock signal is a **rectangular pulse** train or a **square wave**. A clock waveform can have many shapes as shown below:

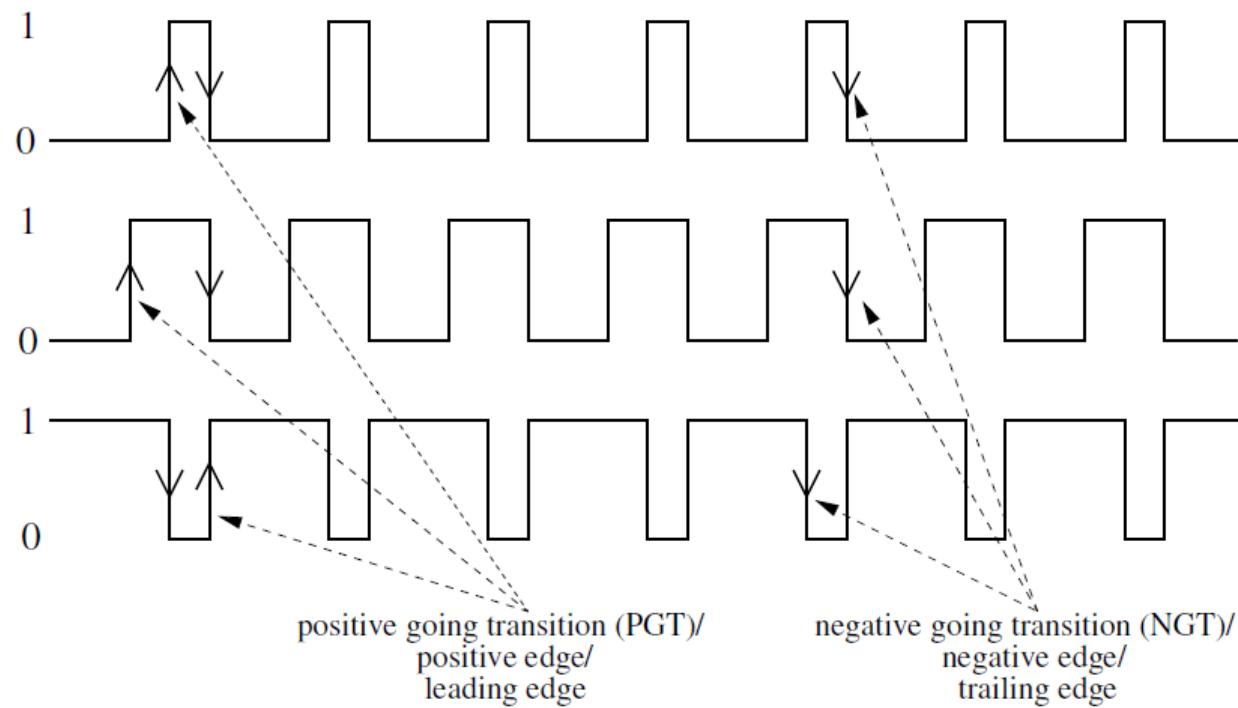


Figure 4.9: Clock waveforms

4.3 Clock Signals and Clocked Flip Flops

* Duty Cycle:

For a clock waveform,

$$\text{Duty Cycle} = \frac{T_{\text{HIGH}}}{T_{\text{HIGH}} + T_{\text{LOW}}} \cdot 100 \%$$

- Where T_{HIGH} is the time the waveform is at logic level 1 and T_{LOW} is the time the waveform is at logic level 0.

* Synchronous and Asynchronous Operation:

- Digital systems can operate either synchronously or asynchronously.
- **Asynchronous operation:** Outputs of a logic circuit **change any time** **when** one or more of the **inputs change**. This kind of circuits are **difficult to troubleshoot** since the outputs can change at any time.
- **Synchronous operation:** Outputs can only **change at specific instants of time**, these instants **determined by the clock**.

Types of Clocked Flip-Flops:

- i. Level driven flip-flops
- ii. Master-slave flip flops
- iii. Edge-triggered flip-flops
- The first two types are no longer used in modern digital systems, but are covered here for completeness of this course.

4.3.2 Level – Driven Flip Flops

- A Level-driven flip-flop is one where **one level** of the clock **enables** the data inputs to affect the state of the flip-flop, whereas the **other level disables** the data inputs from affecting the state of the flip-flop. This type of flip-flop is illustrated using a JK flip-flop as illustrated next:

4.3.2 Level – Driven Flip Flops

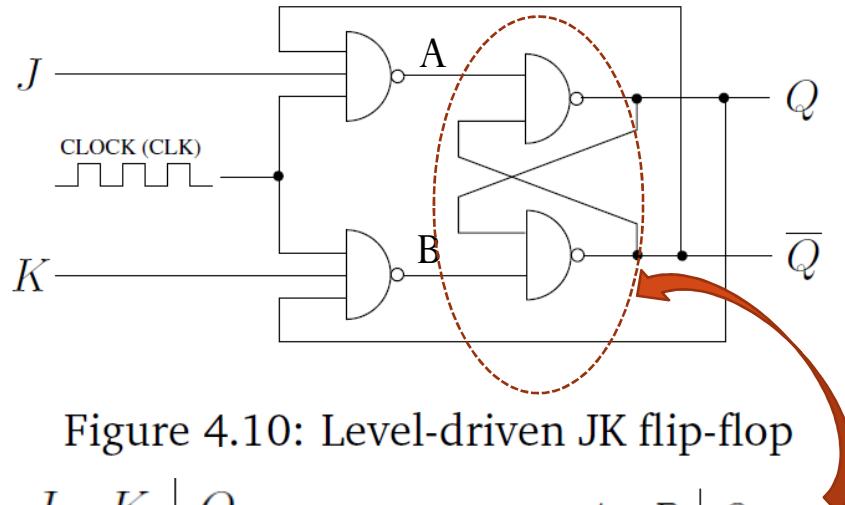


Figure 4.10: Level-driven JK flip-flop

J	K	Q_{n+1}	A	B	Q_{n+1}
0	0	Q_n	0	0	Disallowed as it causes $Q = \bar{Q} = 1$
0	1	0	0	1	1
1	0	1	1	0	0
1	1	\bar{Q}_n	1	1	Q_n - 'remembers' previous state (Memory State)

- From Figure 4.10 above, we can see that **when the CLK signal is at logic level 0**, $A = B = 1$. From the truth-table of the NAND gate latch, we can see that the flip-flop will be in the memory state, hence the inputs **J and K will not have any effect on the outputs Q and \bar{Q}** .

4.3.2 Level – Driven Flip Flops

- We can conclude that the inputs J and K are disabled from affecting the state of the flip-flop when **CLK = 0**.
- When the CLK signal is HIGH, $A = \overline{J} \cdot \overline{Q}$ and $B = \overline{K} \cdot Q$. (**the NAND gate outputs A and B shall be determined by $J \cdot \overline{Q}$ and $K \cdot Q$**) The next state of the flip-flop is determined by the inputs J and K.
- This implies that when CLK = 1, the flip-flop inputs (**J and K**) are enabled to **affect the state of the flip-flop**.
- In such cases, we say that the **enabling** level of the clock is HIGH (i.e. Logic 1).
- Figure 4.11 below shows the symbols for level driven JK flip-flops:

4.3.2 Level – Driven Flip Flops

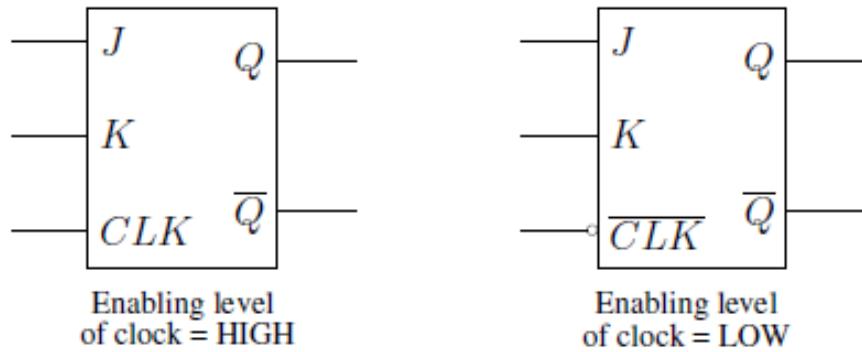


Figure 4.11: Symbols of level-driven JK flip-flops

Exercise

Draw the circuit diagrams for level-driven SET-RESET flip-flop, D flip-flop and the T flip-flop and explain their operation.

4.3.3 The Master-Slave Flip-Flop

- The block diagram for the master rest flip flop is as shown below:

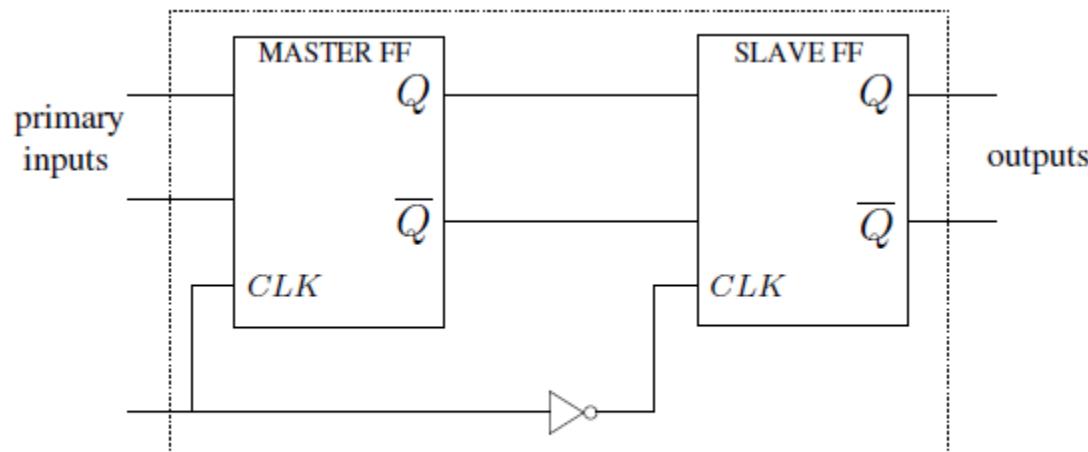


Figure 4.12: A master-slave flip-flop

- Assume that the basic flip-flops are enabled by the HIGH level of the clock:

4.3.3 The Master-Slave Flip-Flop

- **CLK = HIGH** Primary inputs are **enabled** to determine the next state of the Master flip-flop. Clock input to the Slave flip-flop is LOW so that the **Slave inputs are disabled** from affecting the state of the Slave flip-flop.
- **CLK = LOW** Primary inputs are **disabled** from affecting the state of the Master flip-flop. Clock input to the Slave flip-flop is HIGH so that the Master's outputs are transferred to the Slave flip-flop to determine the next state of the Slave flip-flop.
- Figure 4.13 next shows a JK Master-Slave flip-flop:

4.3.3 The Master-Slave Flip-Flop

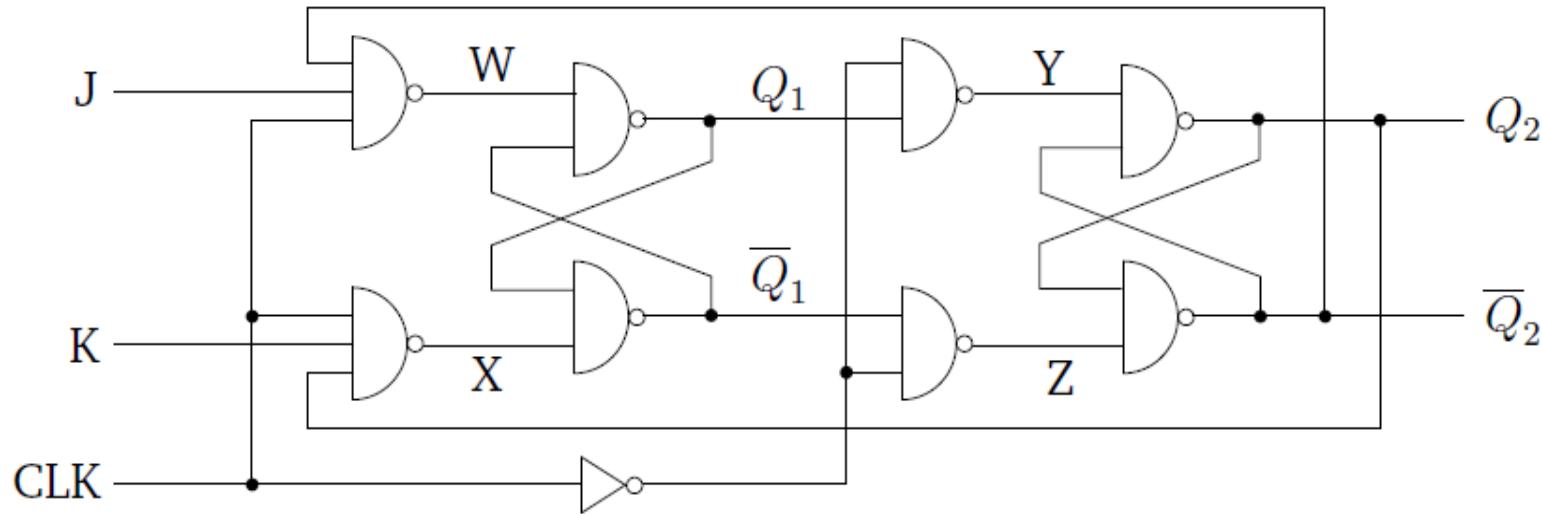


Figure 4.13: JK Master-Slave flip-flop

$CLK = 1$: $W = \overline{(J\bar{Q})}$ and $X = \overline{(KQ)}$, hence the primary inputs J and K determine the next state of the Master flip-flop. At the same time, $Y = Z = 1$ hence the slave flip-flop cannot change state when $CLK = 1$.

$CLK = 0$: $W = X = 1$ hence the Master flip-flop cannot change states. At the same time, $Y = \bar{Q}_1$ and $Z = Q_1$ hence the outputs of the Master are transferred to the Slave flip-flop to determine the next output of the Master-Slave flip-flop.

4.3.3 The Master-Slave Flip-Flop

- The operation of the Master-Slave flip-flop can be summarized as shown in Figure 4.14:

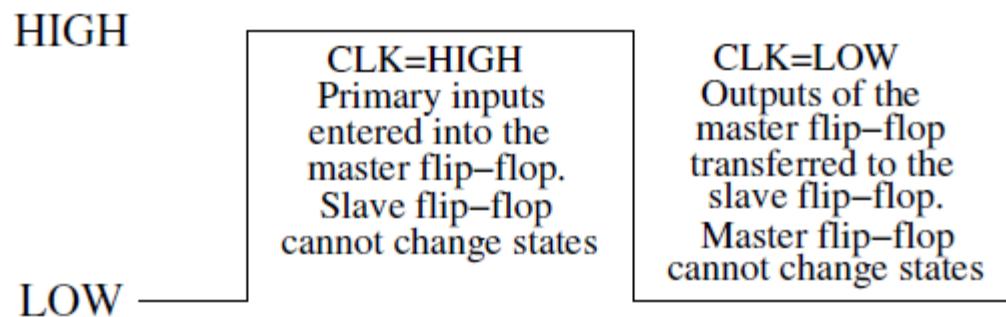


Figure 4.14: Response of a Master-Slave flip-flop to clock signal

4.3.4 Edge triggered Flip-Flops

- Edge triggered flip-flops are those that only change state **during the clock transitions** (HIGH to LOW or LOW to HIGH).
- The flip-flops that change state during the HIGH to LOW transitions of the clock (negative going transitions) are known as **negative edge triggered** flip-flops, while those that change state at the LOW to HIGH transitions of the clock are known as **positive edge triggered** flip-flops.
- Note that there are no flip-flops **that trigger on both the positive and the negative** going transitions of the clock.
- Figure 4.16 shows the logic symbol for a positive edge triggered JK flip-flop:

4.3.4 Edge triggered Flip-Flops

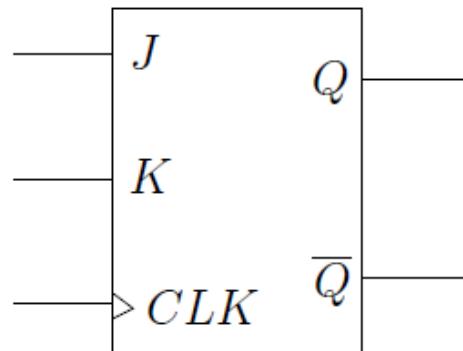


Figure 4.16: Symbol of a positive-edge-triggered JK flip-flop

- The corresponding truth table is as shown below:

<i>J</i>	<i>K</i>	<i>CLK</i>	<i>Q_{n+1}</i>
0	0		<i>Q_n</i>
0	1		0
1	0		1
1	1		\bar{Q}_n

4.3.4 Edge triggered Flip-Flops

Figure 4.17 shows the logic symbol for a negative edge triggered JK flip-flop:

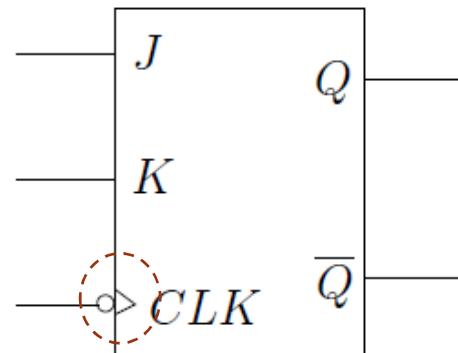


Figure 4.17: Symbol of a negative-edge-triggered JK flip-flop

The corresponding truth table is as below:

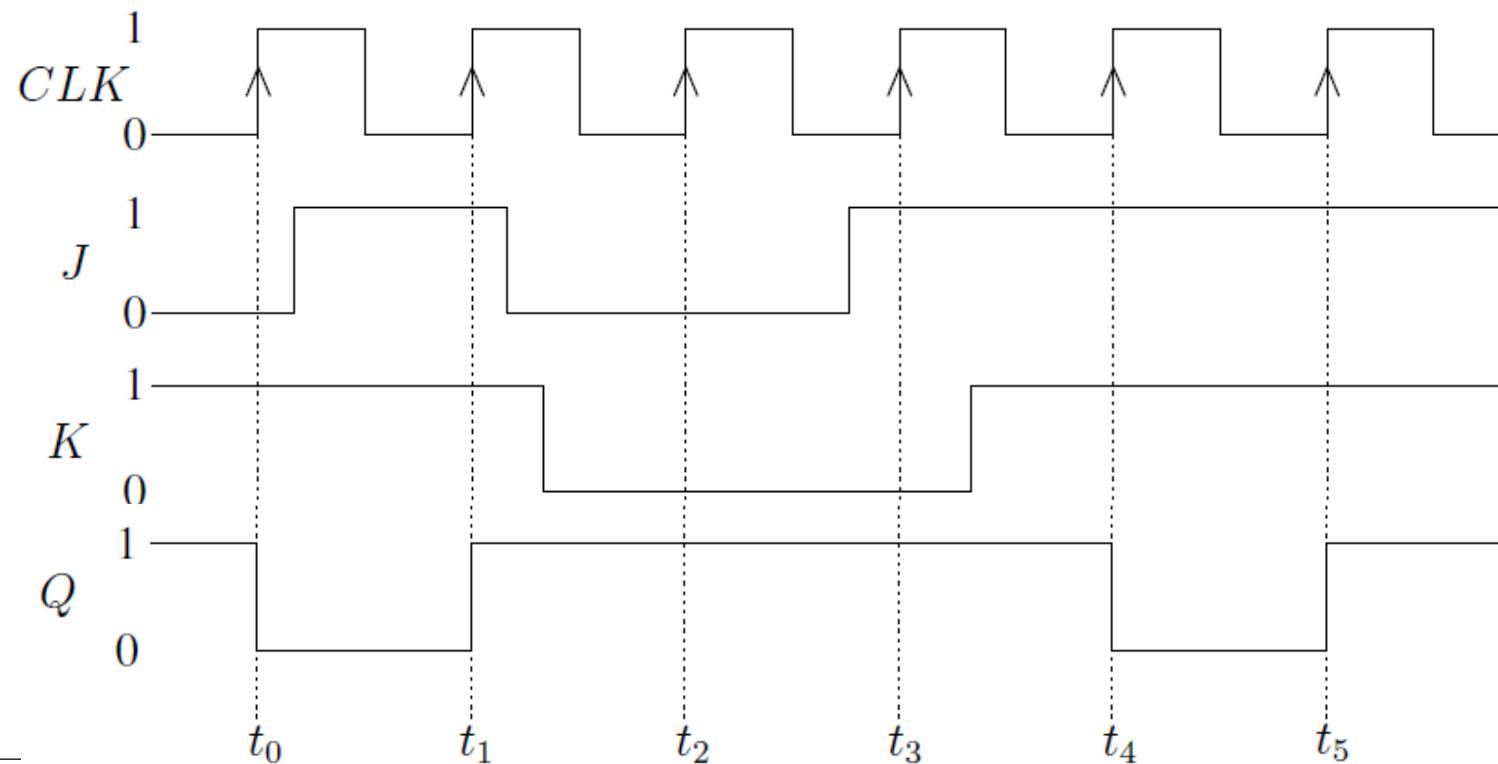
The corresponding truth-table is shown below:

<i>J</i>	<i>K</i>	<i>CLK</i>	Q_{n+1}
0	0	↓	Q_n
0	1	↓	0
1	0	↓	1
1	1	↓	\bar{Q}_n

4.3.4 Edge triggered Flip-Flops

Exercise

- Figure 4.18 shows a clock waveform and inputs J and K applied to a positive-edge triggered JK flip-flop. Using the truth-table for a positive edge triggered JK flip-flop, explain what happens at t_0, t_1, t_2, t_3, t_4 and t_5 to justify the output waveform shown for Q. (Assume that the initial state of Q is HIGH).



4.3.5 Asynchronous Inputs

- The flip-flop inputs we have talked about so far (J,K, D, SET, RESET, T) are known as **synchronous inputs**. This is because the effect of these inputs to the flip-flop output is synchronized with the clock.
- There are other types of inputs known as **asynchronous inputs**. Asynchronous inputs operate independently of the clock input.
- There are two asynchronous inputs in a flip-flop, the PRESET (sometimes referred to as SET) and CLEAR (sometimes referred to as RESET).
- The PRESET input is used to **set the state** of the flip-flop **to 1** ($Q = 1$) **regardless of the state of the synchronous inputs and the clock**, while the **CLEAR** input is used to **reset the flip-flop** ($Q = 0$).
- These inputs are usually active-LOW as illustrated next:

4.3.5 Asynchronous Inputs

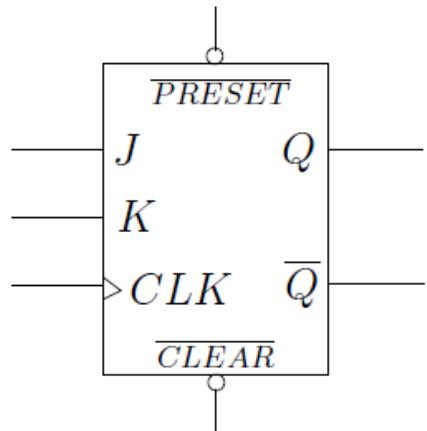


Figure 4.19: JK flip-flop with asynchronous inputs

- The truth-table corresponding to this flip-flop is shown below:

<i>PRESET</i>	<i>CLEAR</i>	<i>Flip – flop response</i>
1	1	Responds to J, K and CLK (synchronous operation)
1	0	Flip-Flop RESET ($Q = 0$)
0	1	Flip-Flop SET ($Q = 1$)
0	0	Not used (= Setting and Resetting at the same time)

4.5 Flip-Flop Excitation Tables Derivation

Recall: The **truth table** for an SR flip flop is as shown below:

<i>SET</i>	<i>RESET</i>	<i>Q_{n+1}</i>
0	0	<i>Q_n</i> - 'remembers' previous state (Memory State)
0	1	0 - Flip-Flop RESET
1	0	1 - Flip-Flop SET
1	1	Disallowed as it causes $Q = \bar{Q} = 1$

This can be expanded to give the **characteristic table** as shown:

<i>S</i>	<i>R</i>	<i>Q_n</i>	<i>Q_{n+1}</i>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Disallowed
1	1	1	Disallowed

4.5 Flip-Flop Excitation Tables Derivation

- The SR flip flop *excitation table is derived as below:

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

*What is an excitation table? A table that gives the inputs required for a given combination of present state Q_n and next state Q_{n+1}

4.5 Flip-Flop Excitation Tables Derivation

Recall: The **truth table** for a D flip flop is as shown below:

D	Q_{n+1}
0	0
1	1

This can be expanded to give the **characteristic table** as shown:

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

4.5 Flip-Flop Excitation Tables Derivation

- The D flip flop ***excitation table** is derived from the characteristic table as below:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

***What is an excitation table?** A table that gives the inputs required for a given combination of present state Q_n and next state Q_{n+1}

4.5 Flip-Flop Excitation Tables Derivation

Recall: The **truth table** for a T flip flop is as shown below:

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

This can be expanded to give the **characteristic table** as shown:

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

4.5 Flip-Flop Excitation Tables Derivation

- The T flip flop ***excitation table** is derived from the characteristic table as below:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

***What is an excitation table?** A table that gives the inputs required for a given combination of present state Q_n and next state Q_{n+1}

4.5 Flip-Flop Excitation Tables Derivation

Recall: The **truth table** for an JK flip flop is as shown below:

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

This can be expanded to give the **characteristic table** as shown:

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

4.5 Flip-Flop Excitation Tables Derivation

- The JK flip flop *excitation table is derived as below:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

*What is an excitation table? A table that gives the inputs required for a given combination of present state Q_n and next state Q_{n+1}

4.6 Derivation of One Flip-Flop Function From Another

The procedure:

1. Construct the **state transition table** for the required flip-flop function.
2. Determine the combination of inputs of the flip-flop being used that gives the same transition (this is done with the help of the flip-flop excitation tables derived in the previous section).
3. Determine the relationship between the required inputs and the available flip-flop inputs.
4. Construct the circuit.

4.6 Derivation of One Flip-Flop Function From Another

Example 1:

- Realize a JK flip-flop function using a SET-RESET (SR) flip-flop.

REQUIRED FUNCTION				FLIP FLOP BEING USED	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

4.5 Flip-Flop Excitation Tables

- The K-maps for S and R are shown below:

		$\bar{J}K$	$\bar{J}K$	JK	$J\bar{K}$	
		\bar{Q}	0	0	1	1
Q	\bar{Q}	X	0	0	X	
	Q	X	0	0	X	

S

		$\bar{J}K$	$\bar{J}K$	JK	$J\bar{K}$	
		\bar{Q}	X	X	0	0
Q	\bar{Q}	0	1	1	0	
	Q	X	0	0	X	

R

- From the K-maps, we can see that:

$$S = J\bar{Q} \text{ and } R = KQ$$

4.3 Clock Signals and Clocked Flip Flops

- The circuit can now be represented as:

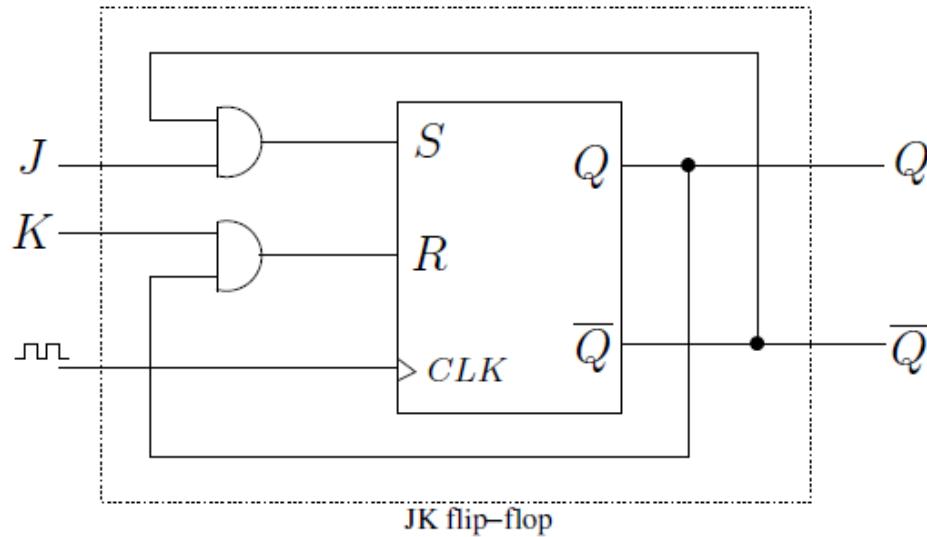


Figure 4.21: Realizing a JK flip-flop function from an SR flip-flop

4.6 Derivation of One Flip-Flop Function From Another

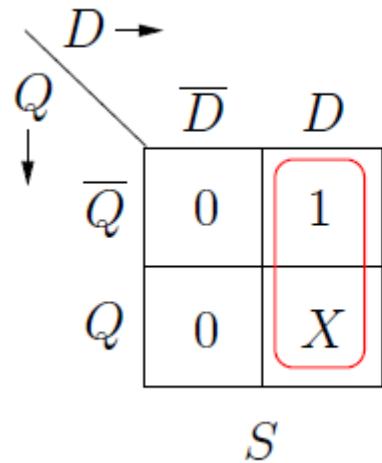
Example 2:

- Realize a D flip-flop function using a SET-RESET (SR) flip-flop.

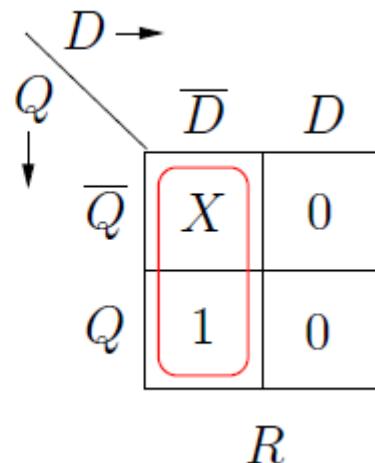
REQUIRED FUNCTION			FLIP FLOP BEING USED	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

4.5 Flip-Flop Excitation Tables

- The K-maps for S and R are shown below:



S



R

- From the K-maps, we can see that:

$$S = D \text{ and } R = \bar{D}$$

4.3 Clock Signals and Clocked Flip Flops

- The circuit can now be represented as:

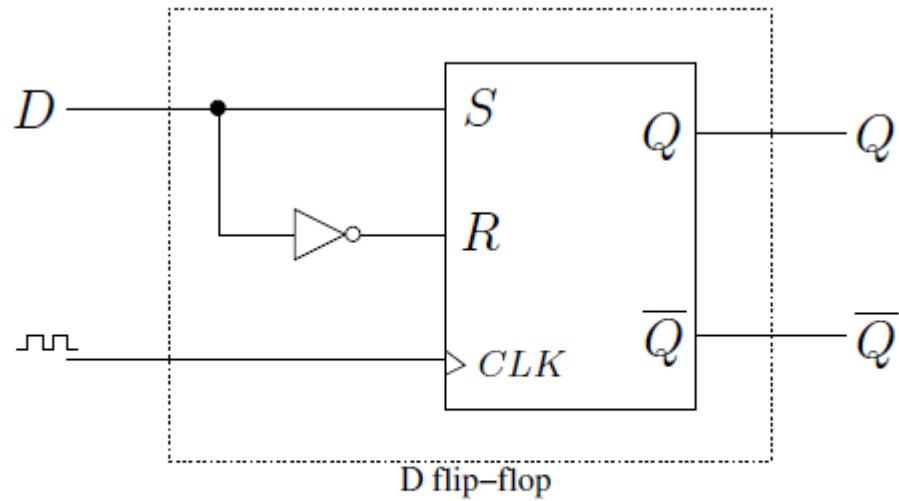


Figure 4.23: Realizing a D flip-flop function from an SR flip-flop

4.6 Derivation of One Flip-Flop Function From Another

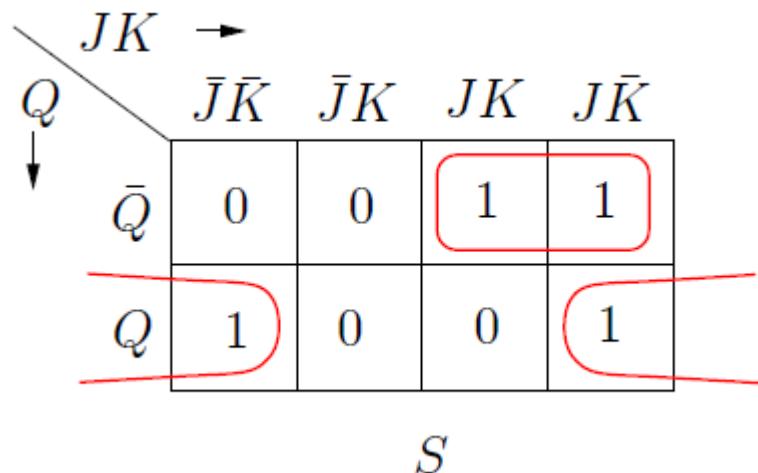
Example 3:

- Realize a JK flip-flop function using a D Flip-flop.

REQUIRED FUNCTION				FLIP FLOP BEING USED
J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

4.5 Flip-Flop Excitation Tables

- The K-maps for D is as shown below:



- From the K-maps, we can see that:

$$D = J\bar{Q} + \bar{K}Q$$

4.3 Clock Signals and Clocked Flip Flops

- The circuit can now be represented as:

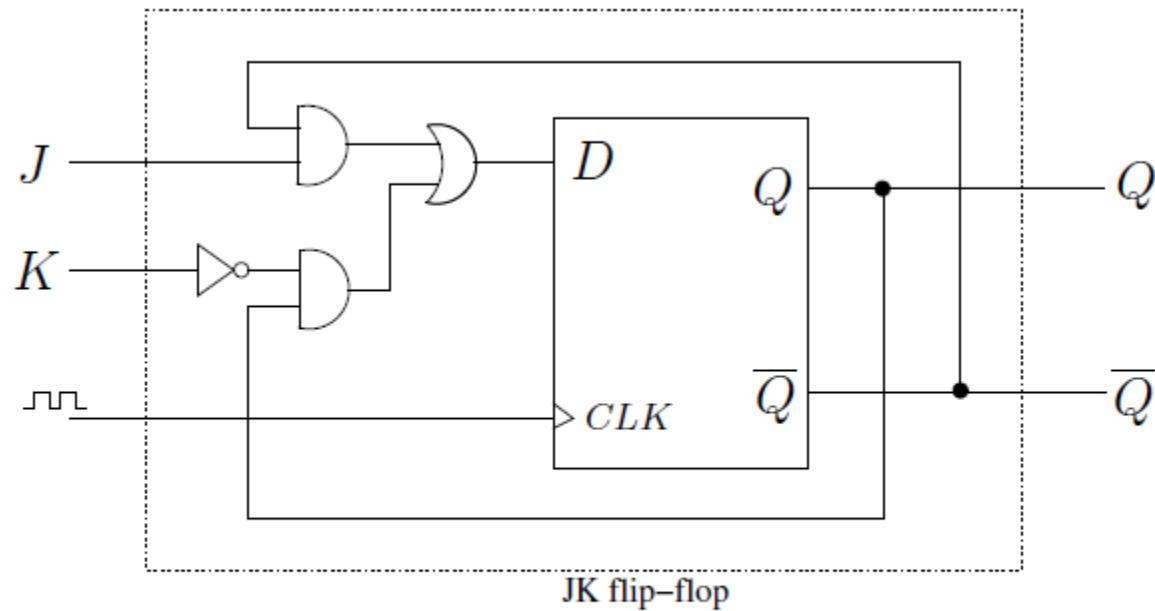


Figure 4.25: Realizing a JK flip-flop function from an D flip-flop



End of session



Questions....?