Command	ras_n	cas_n	we_n
No Operation (NOP)	H	H	H
Active	L	H	H
Read	H	L	H
Write	H	L	L
Burst Terminate	H	H	L
Recharge	L	H	L
Autorefresh	L	L	H
Load mode Register	L	L	L

INITIALIZATION

SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and the clock is stable, the SDRAM requires a 100 µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100 µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

durante 100us=#cycles solo command=NOP=HHH

Once the 100 µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state. Once in the idle state, two AUTO REFRESH cycles must be performed. After two refresh cycles are complete, SDRAM ready for mode register programming. Because the mode registers will power up in unknown state, it should be loaded prior to applying any operational command.

despues de 100us=#cycles y NOP se ejecuto, RECHARGE=LHL

despues de Recharged=idle, x2 AUTOREFRESH=LLH