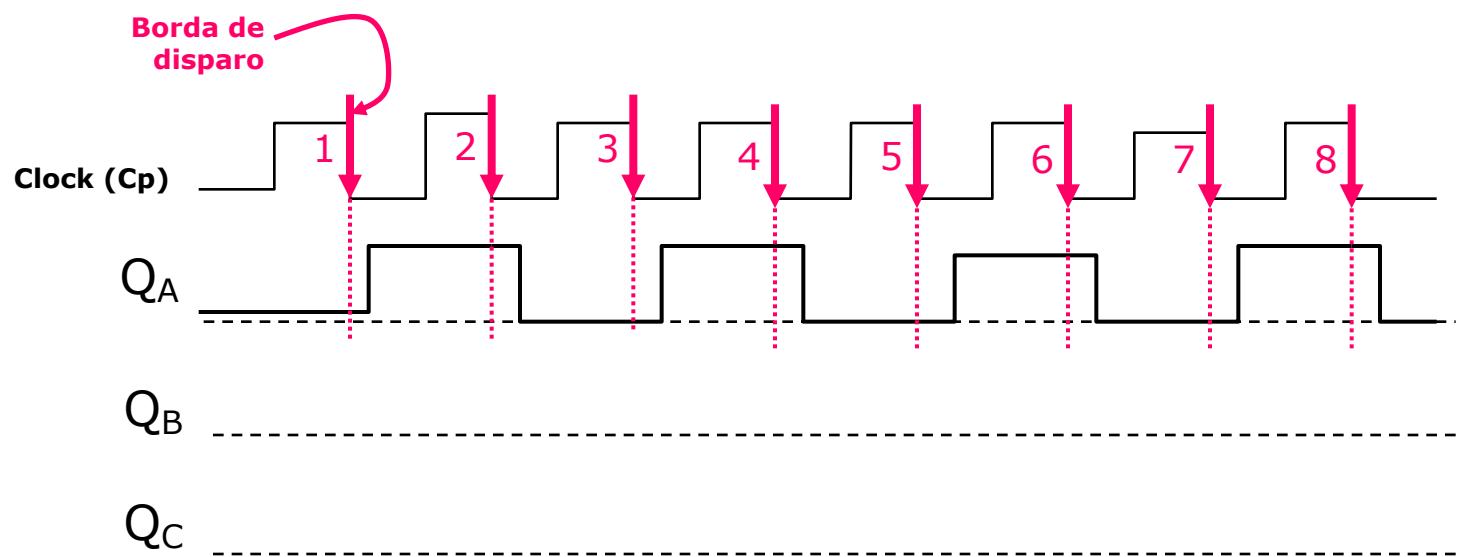
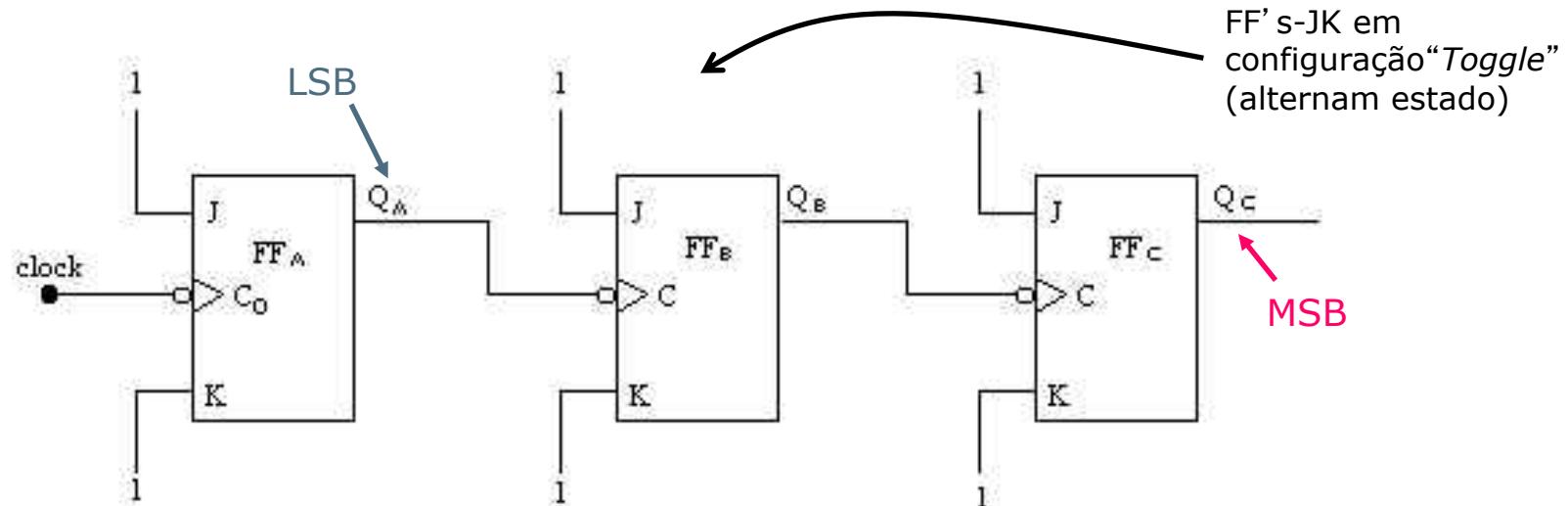


Contadores assíncronos

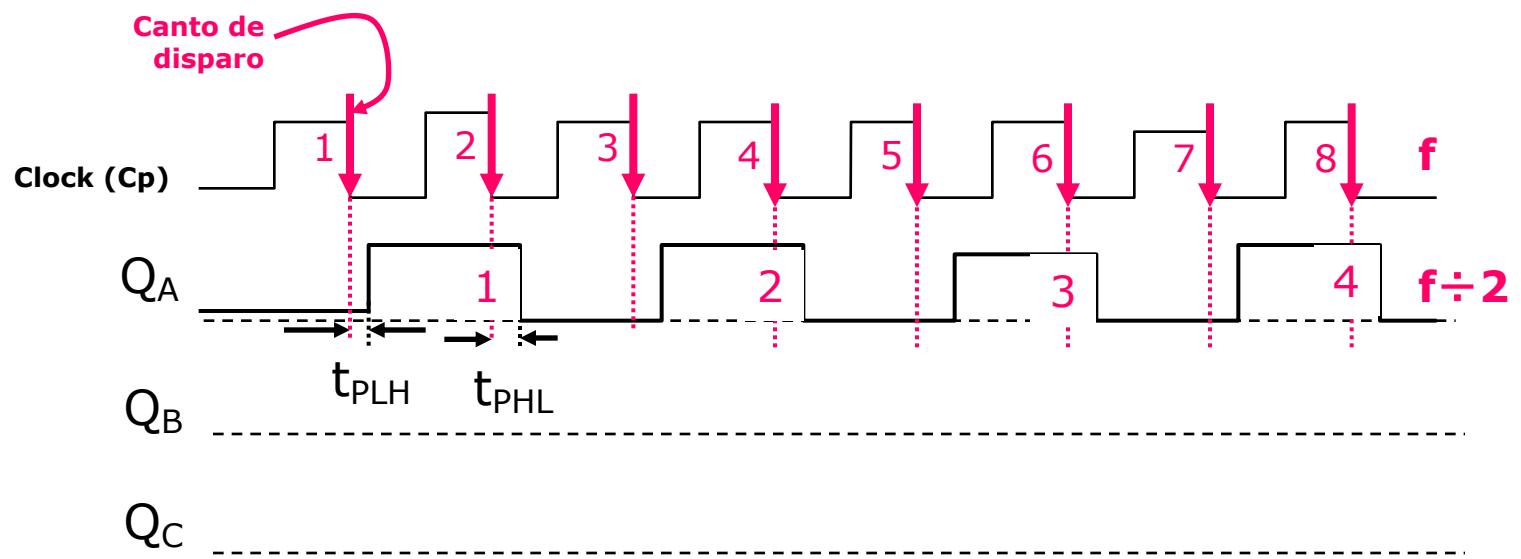
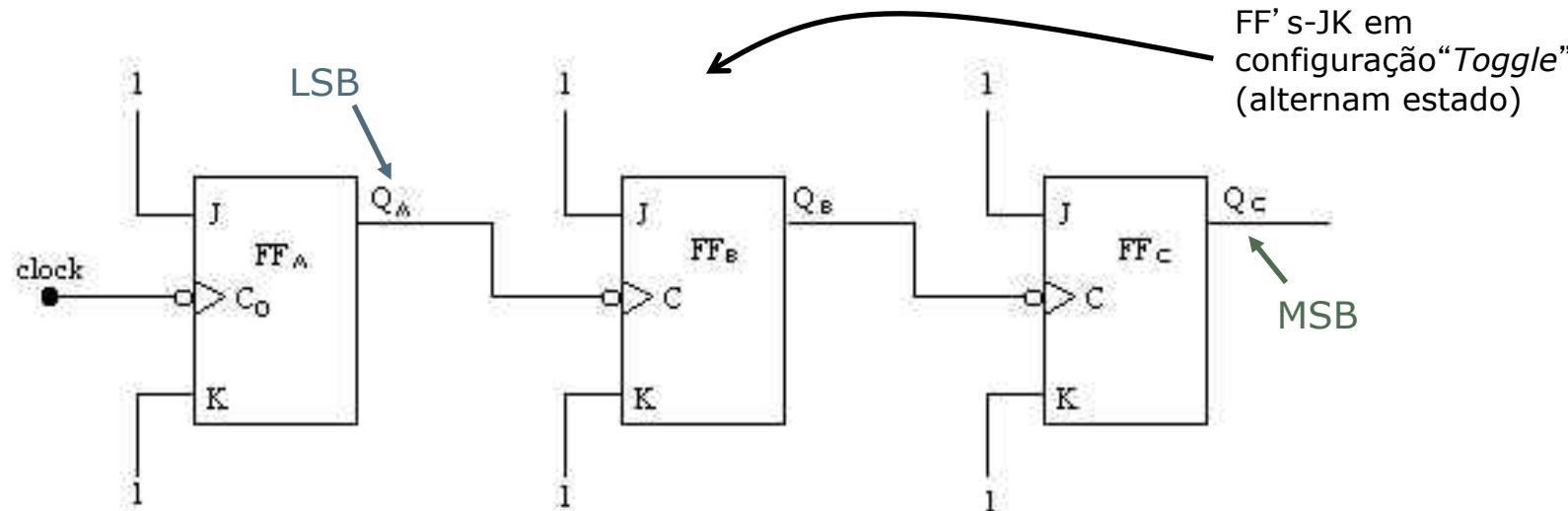
Circuitos Digitais II
Prof. Fernando Passold



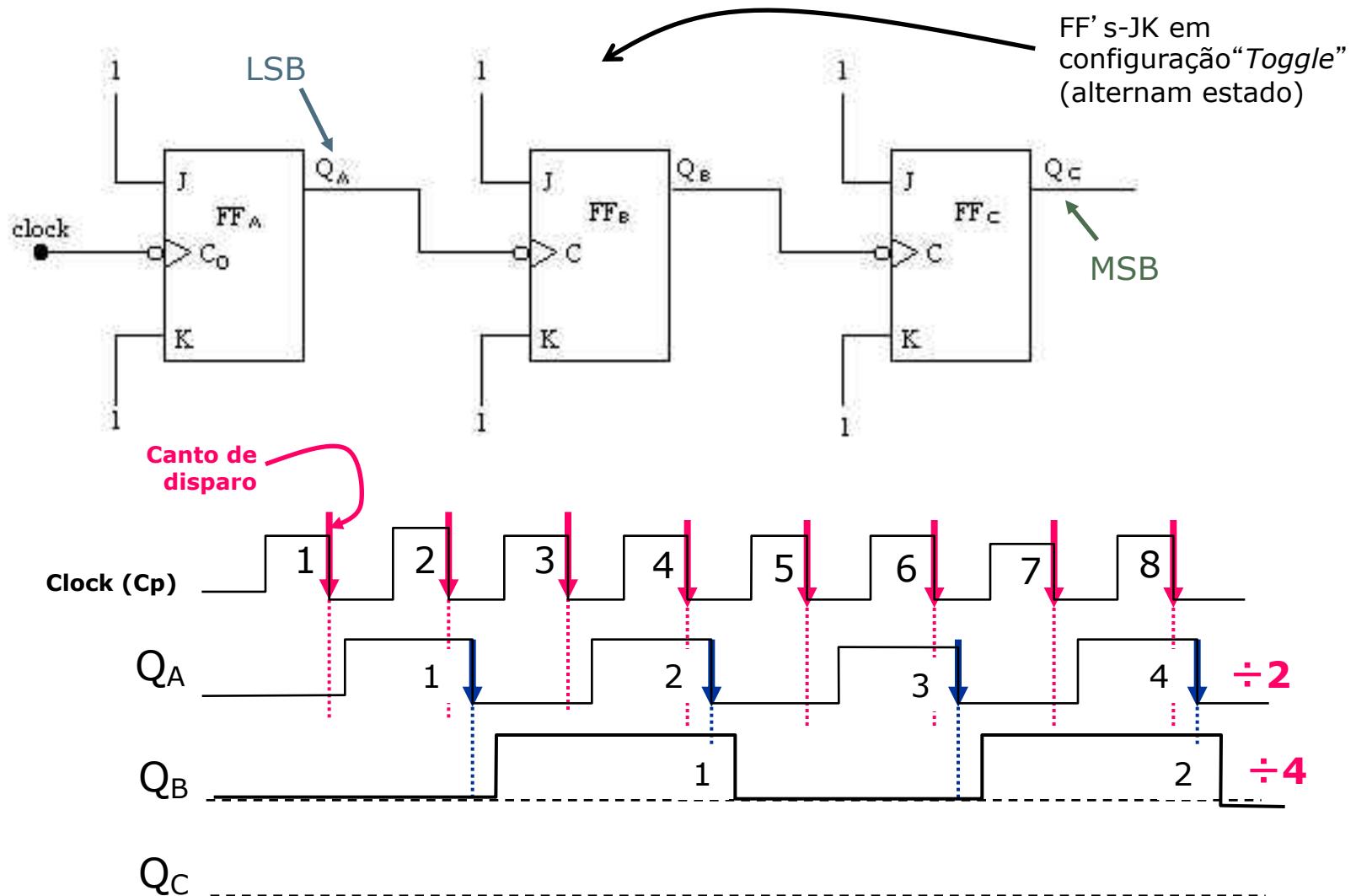
Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



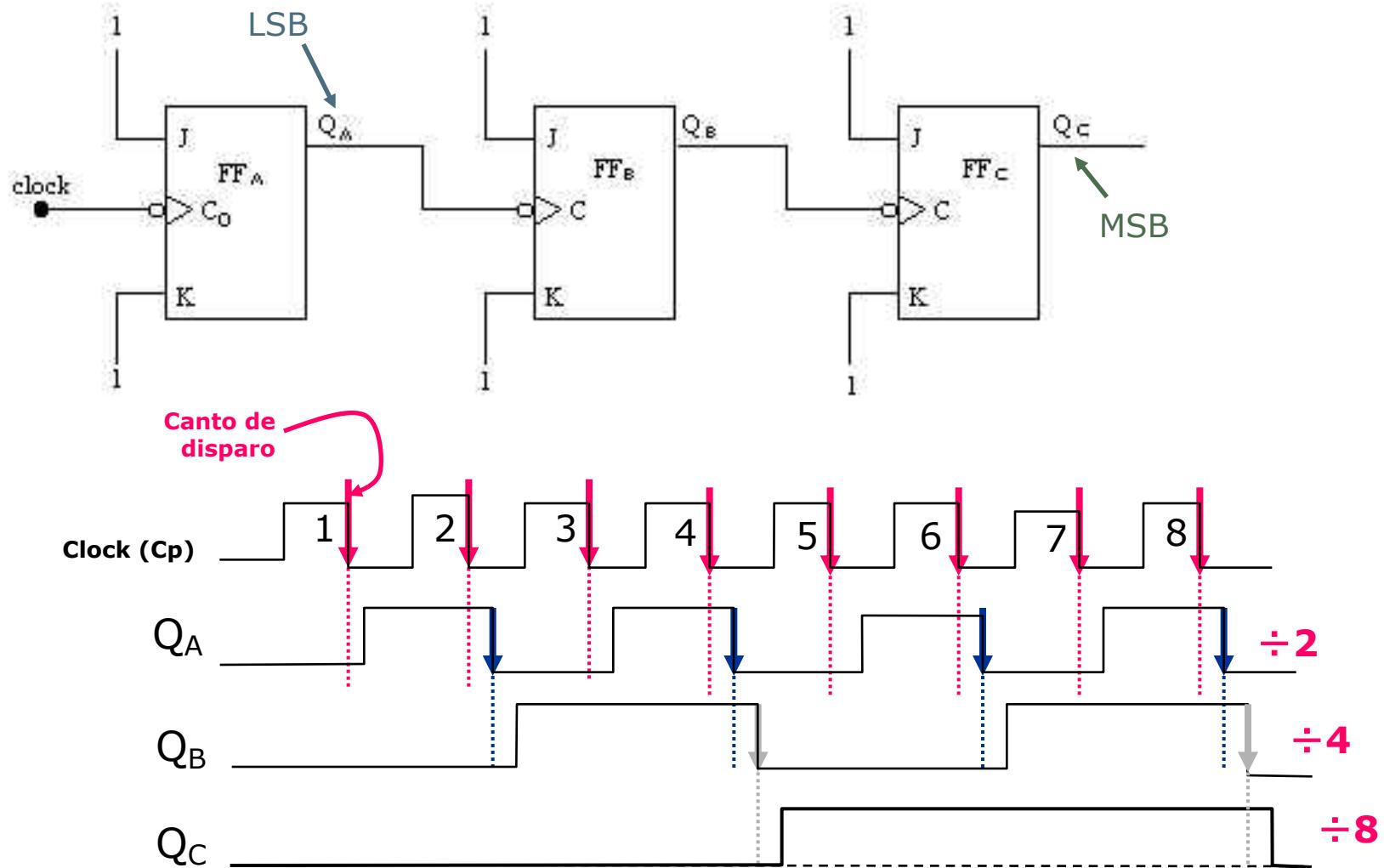
Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



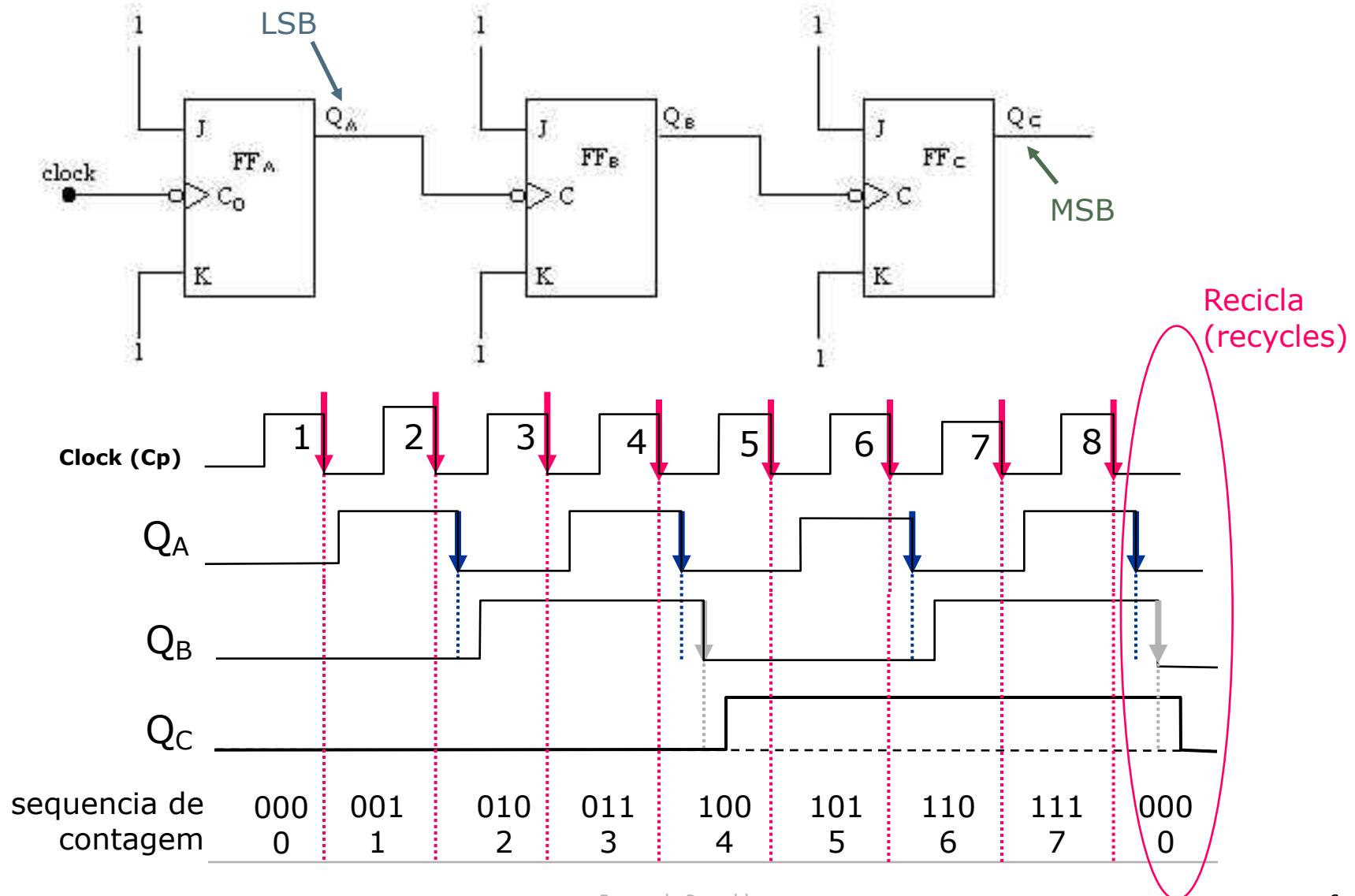
Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



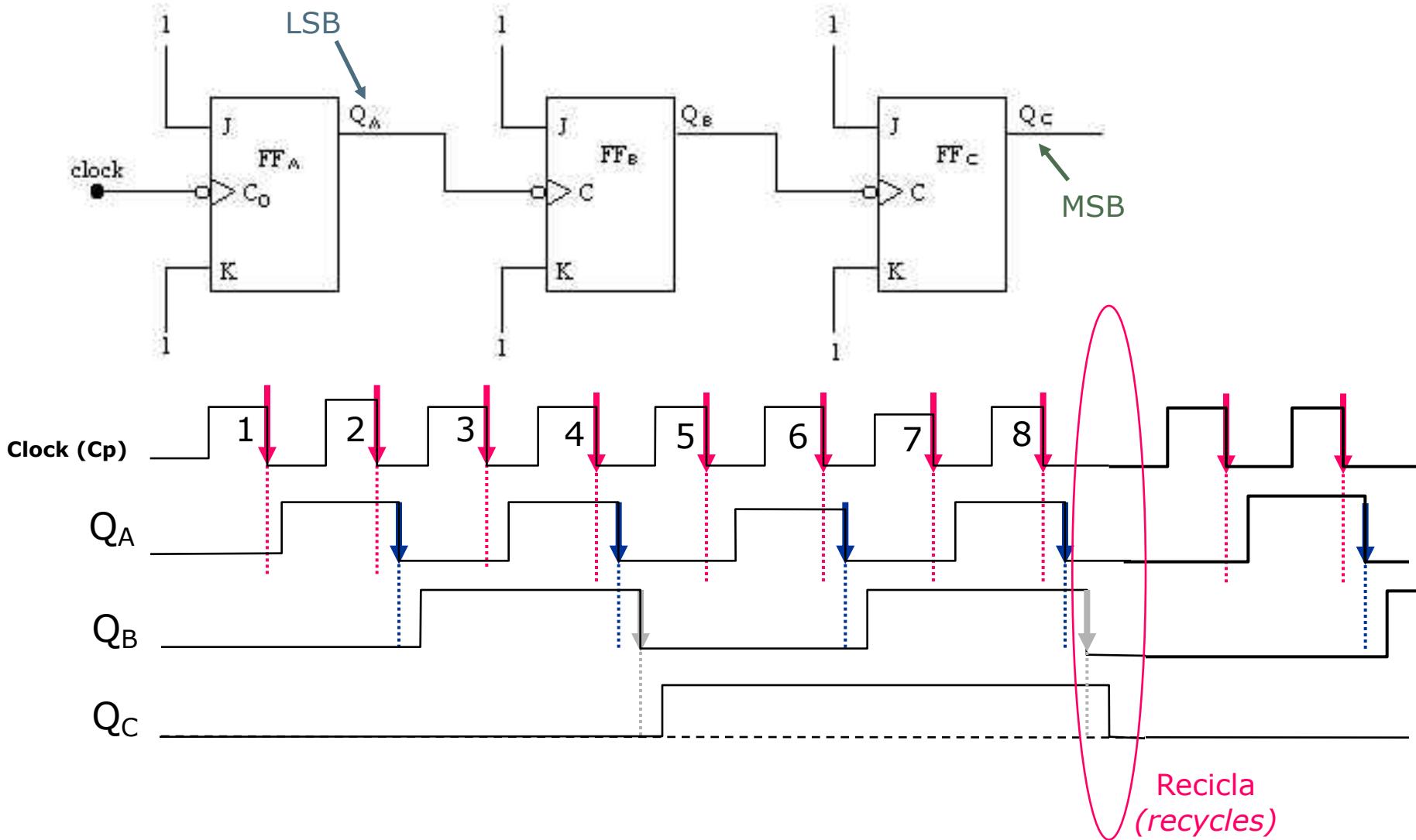
Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



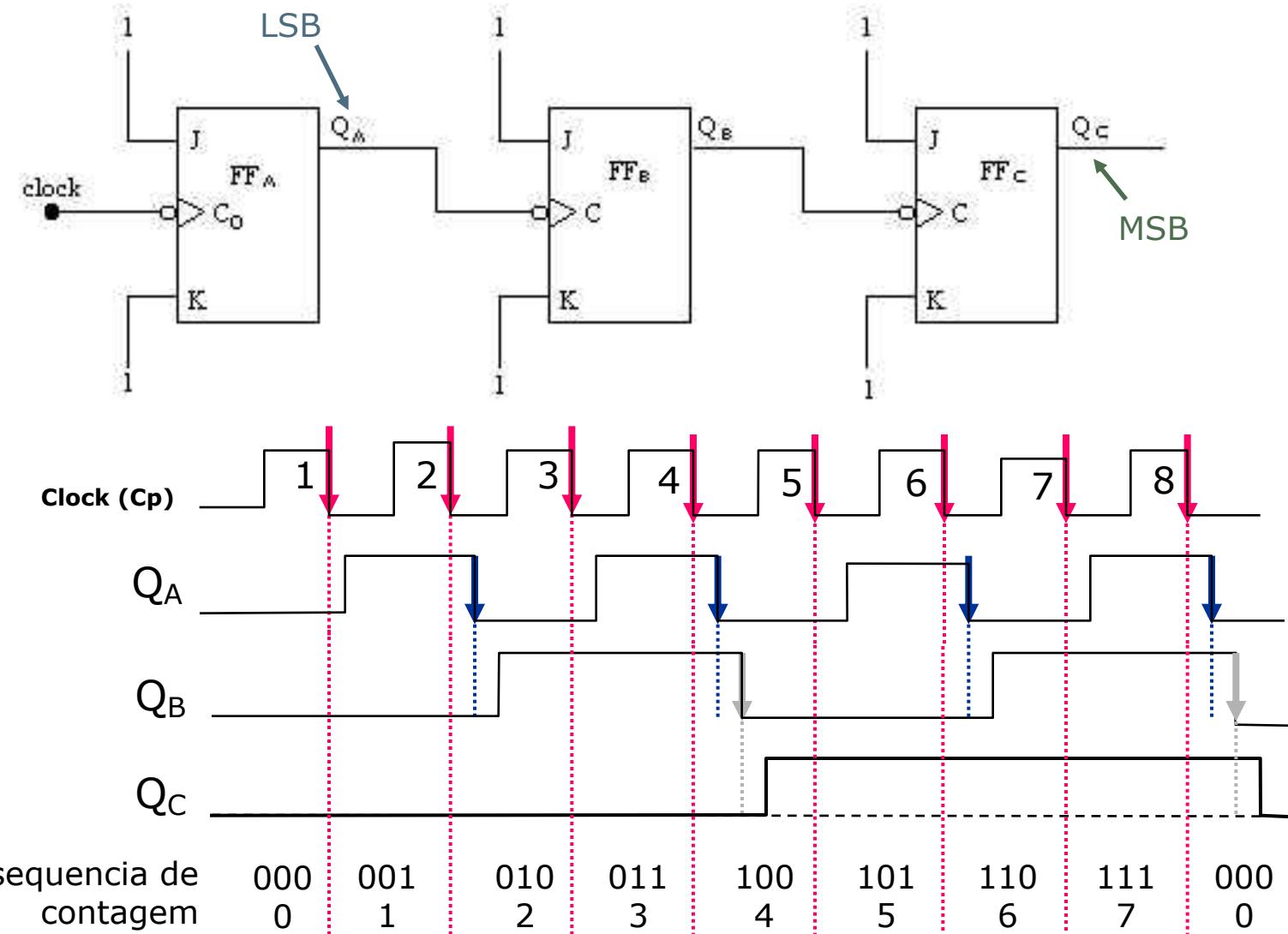
Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



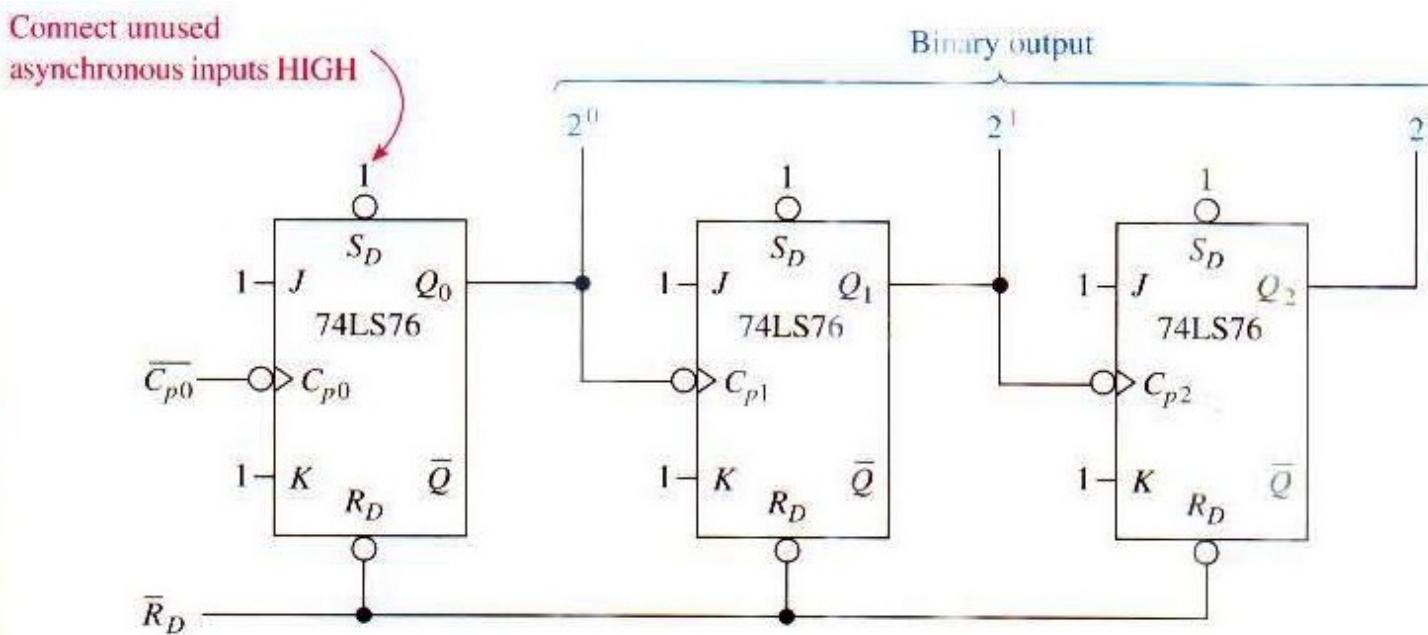
Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



“Ripple Counter” (Contador Assíncrono):



Common Misconception

Because counters are drawn left-to-right, the **LSB of the binary output appears on the left**, which is the **opposite of what we are used to**.

Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3): conta de 0 até 7:

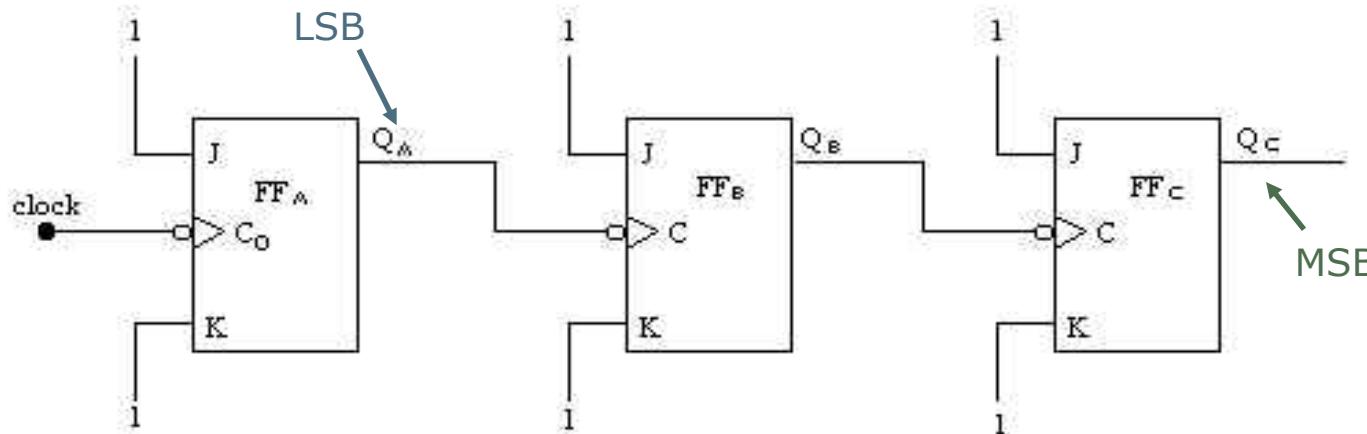
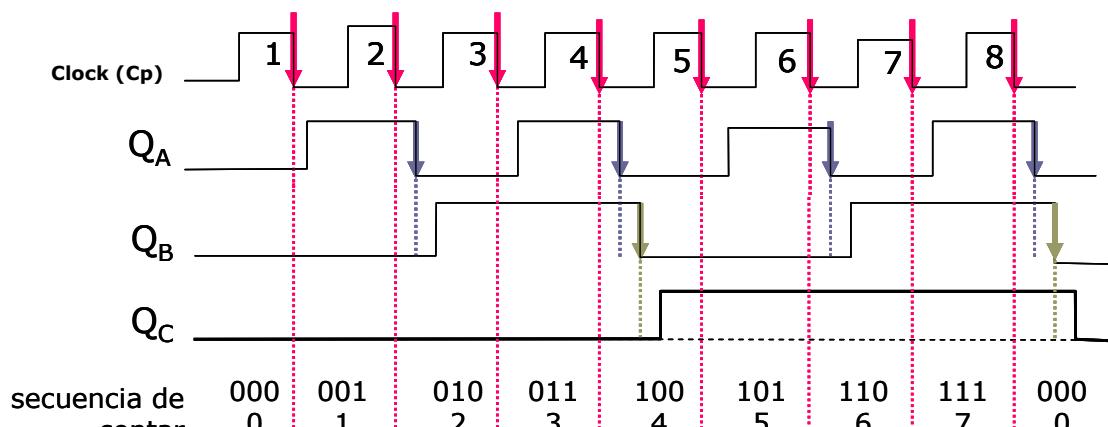


Tabela de Contagem:

Pulso de Clock (Inicialmente)	Qc	Qb	Qa	Conta
	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7
8	0	0	0	0
9	0	0	1	1
:	:	:	:	:



Recicla
(recycle)

Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3): conta de 0 até 7:

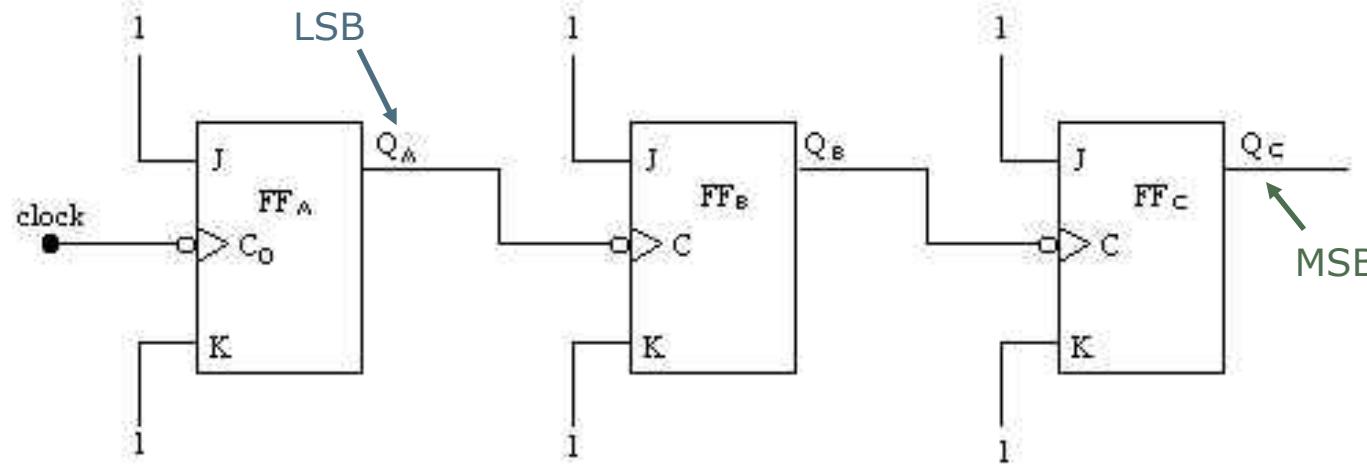
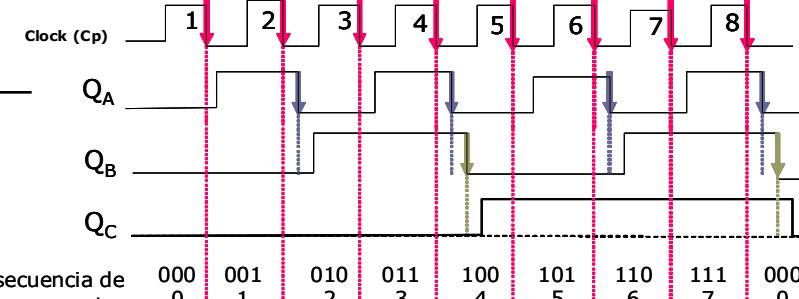
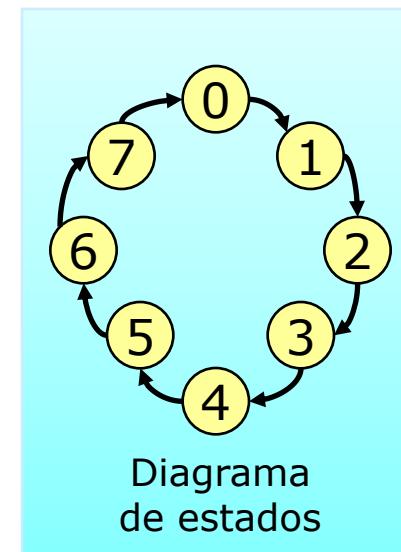


Tabela de Contagem:

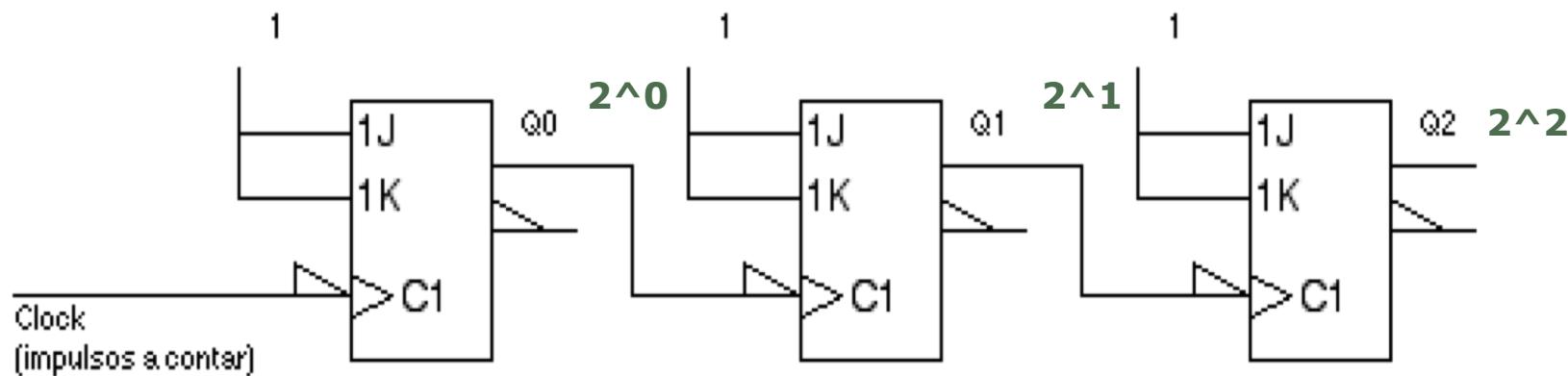
Pulso de Clock (Inicialmente)	Qc	Qb	Qa	Conta
	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7
8	0	0	0	0
9	0	0	1	1
:	:	:	:	:



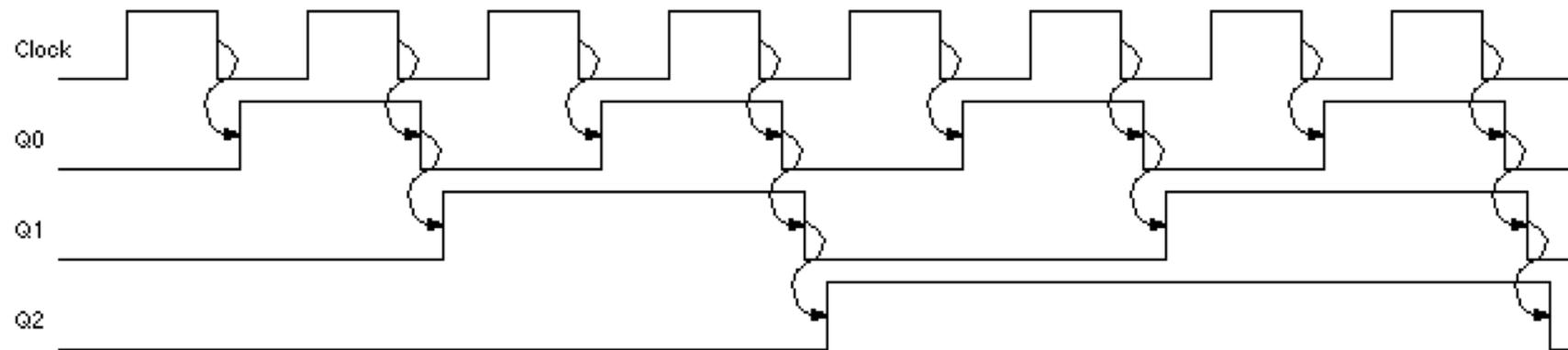
Recicla
(recycle)



Exemplo 1) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:

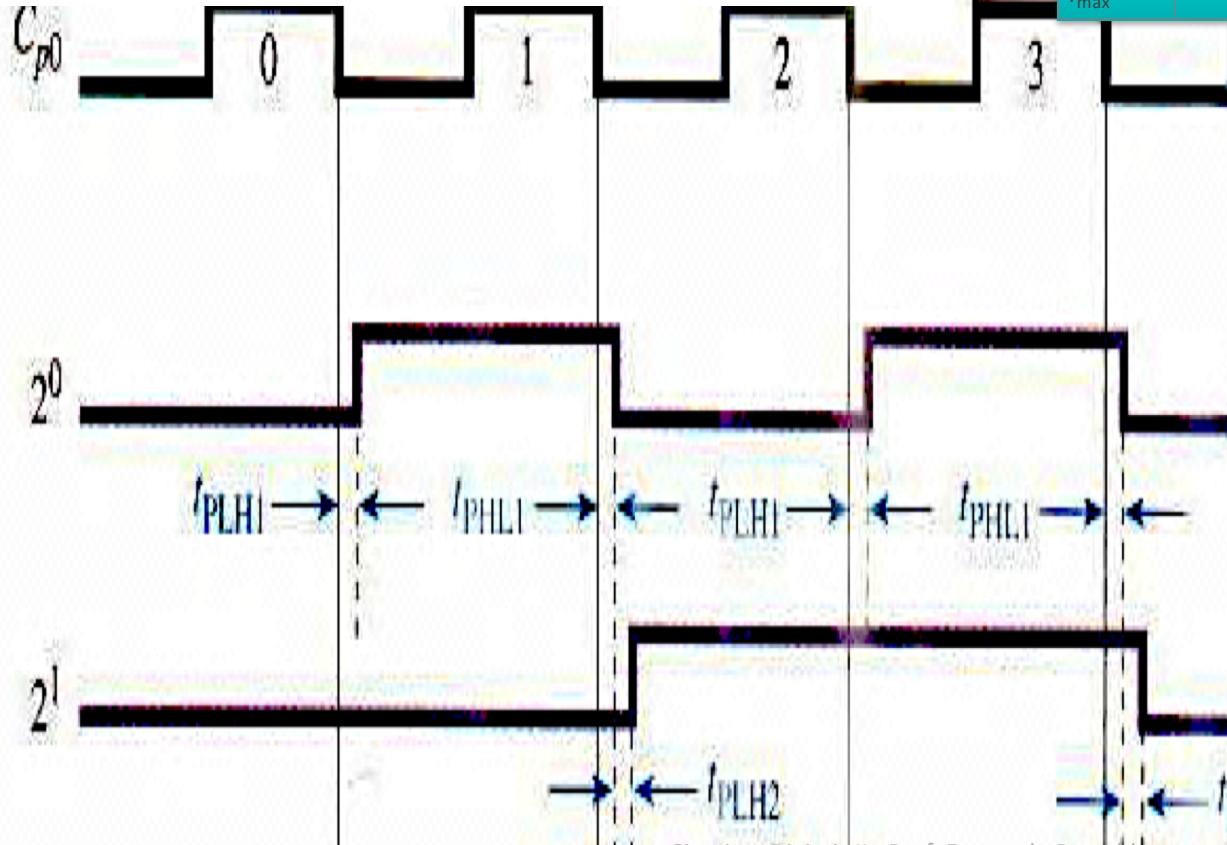
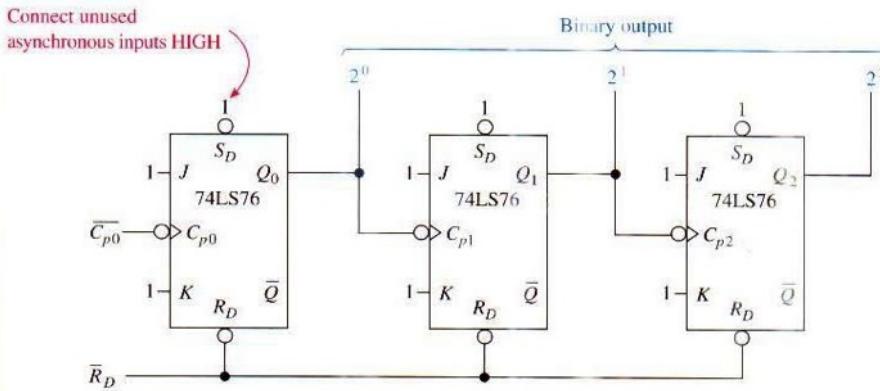


Outra forma de considerar o atraso de propagação dos FFs:



Este símbolo indica que a transição é uma consequência da anterior.

“Ripple Counter” Effects (Efeitos do Contador Assíncrono):

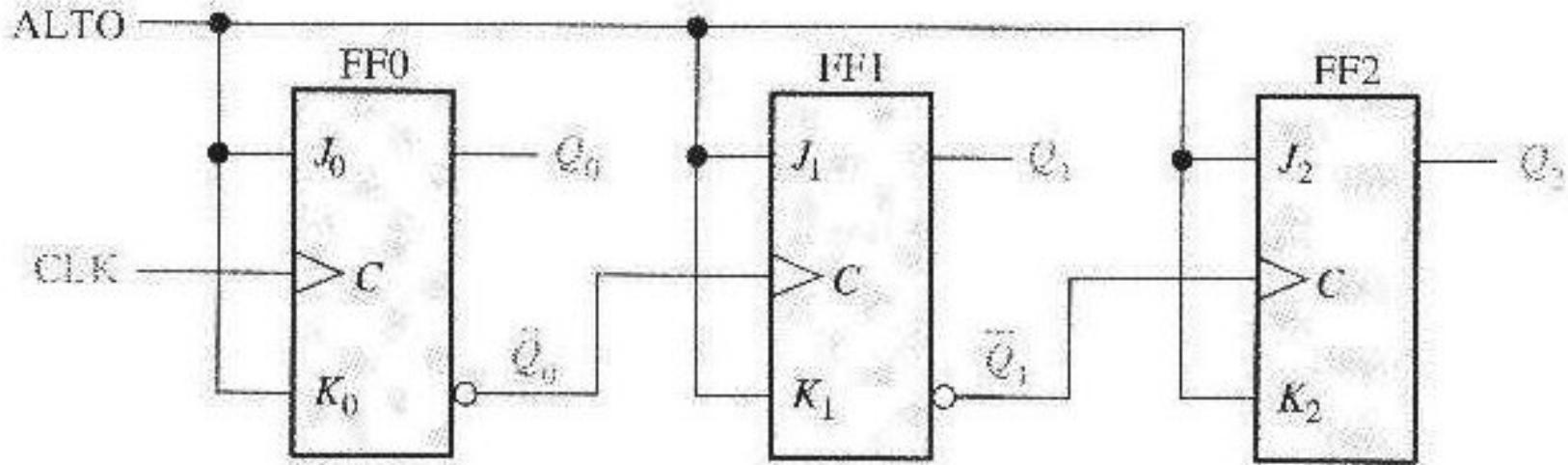


Exemplo para um circuito real:
Dados: p/ 74LS76

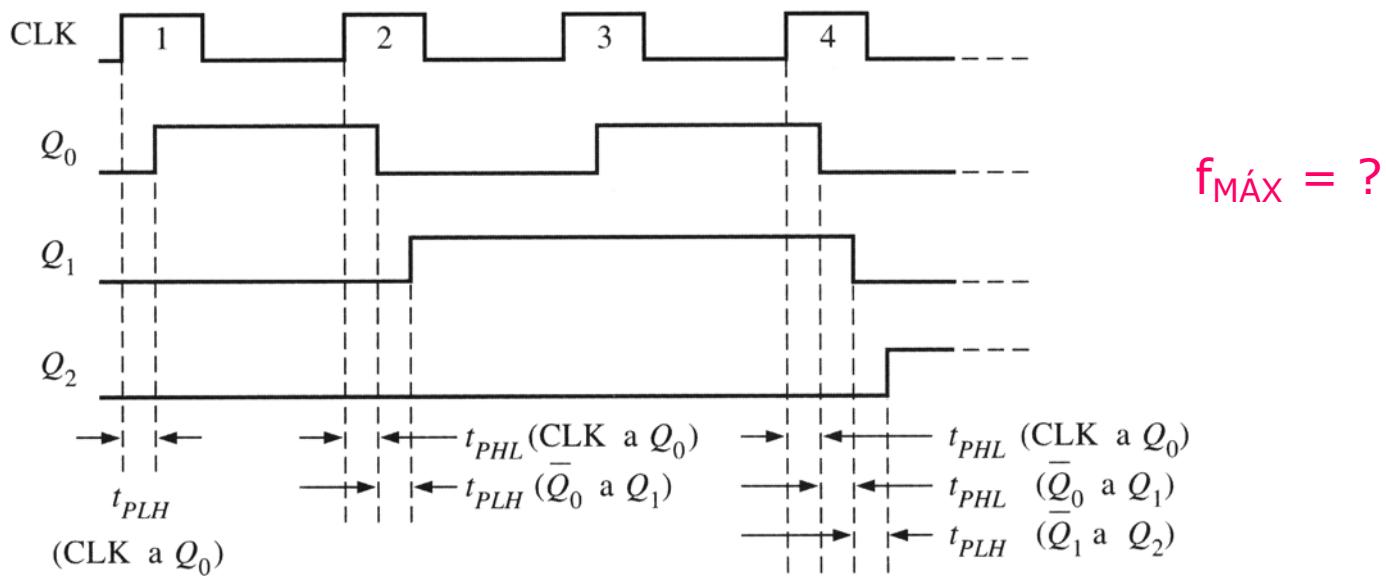
		Typ	Max	Min	Unit
t_{PLH}	Clock, Clear, Set to Output	15	20		ns
t_s	Setup Time			20	ns
t_h	Hold Time			0	ns
f_{max}			45	30	MHz

Detalhes:
Influência
Atrasos de
Propagação
(➡ Freq)

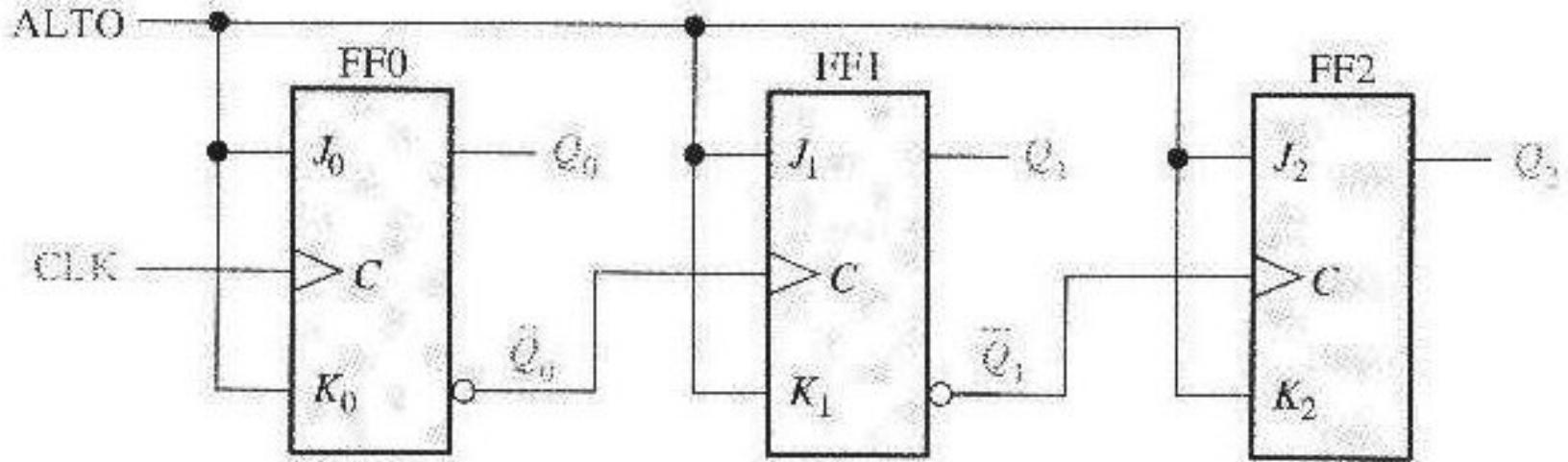
Exemplo 2) Outro contador asíncrono:



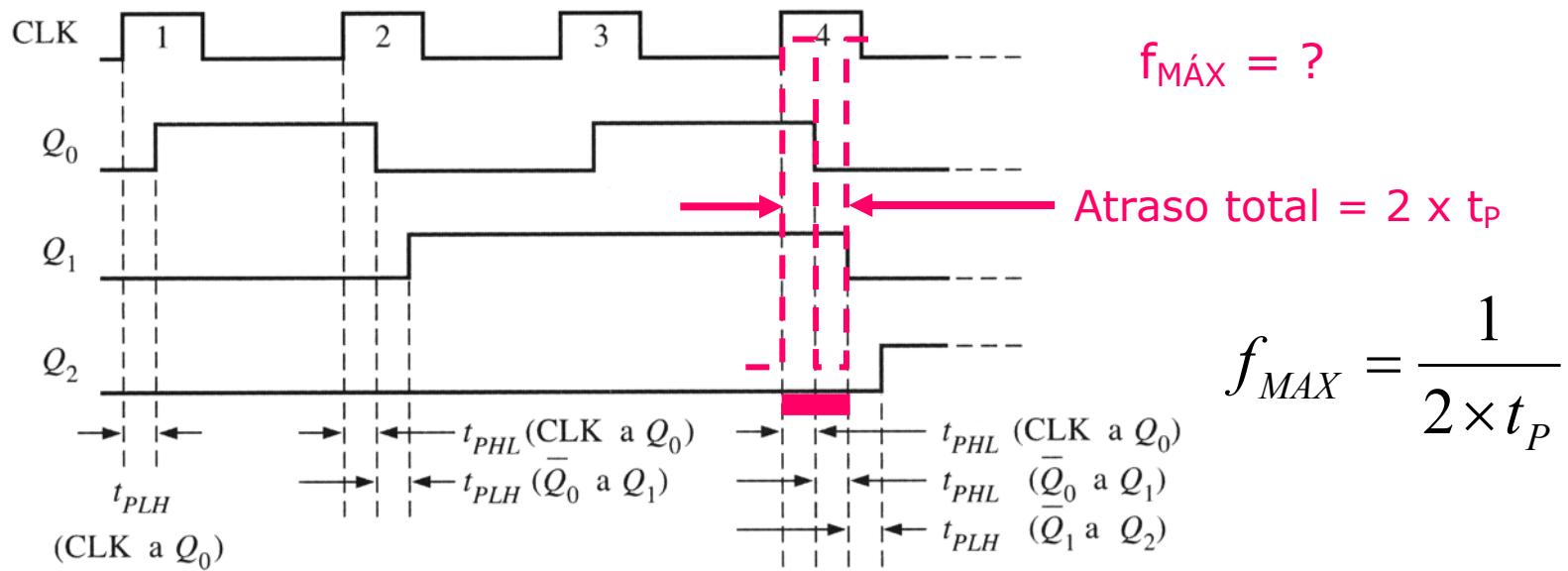
Atenção: notar que os FF's são ativados por borda de subida do sinal de *clock*.



Exemplo 2) Outro contador asíncrono:

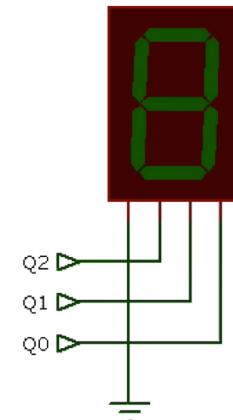
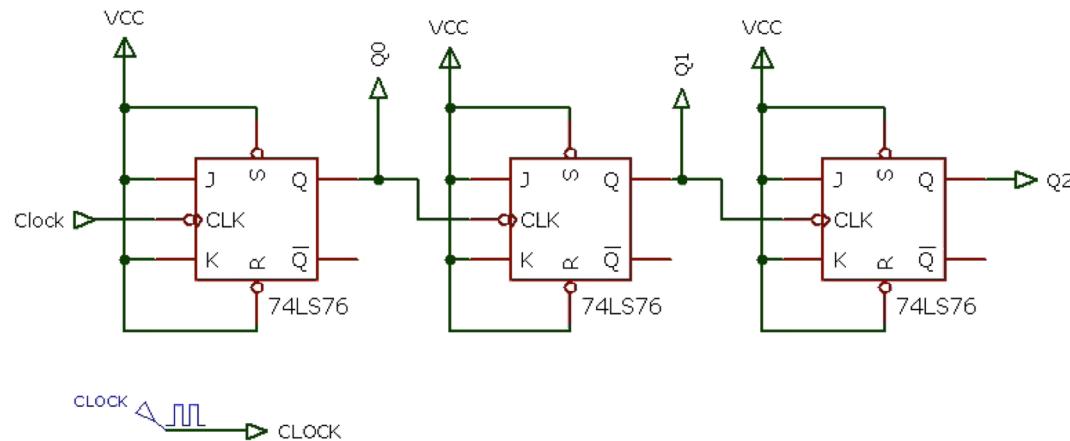


Atenção: notar que os FF's são ativados por borda de subida do sinal de *clock*.

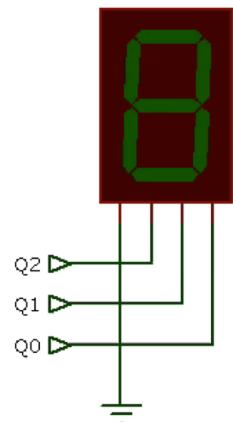
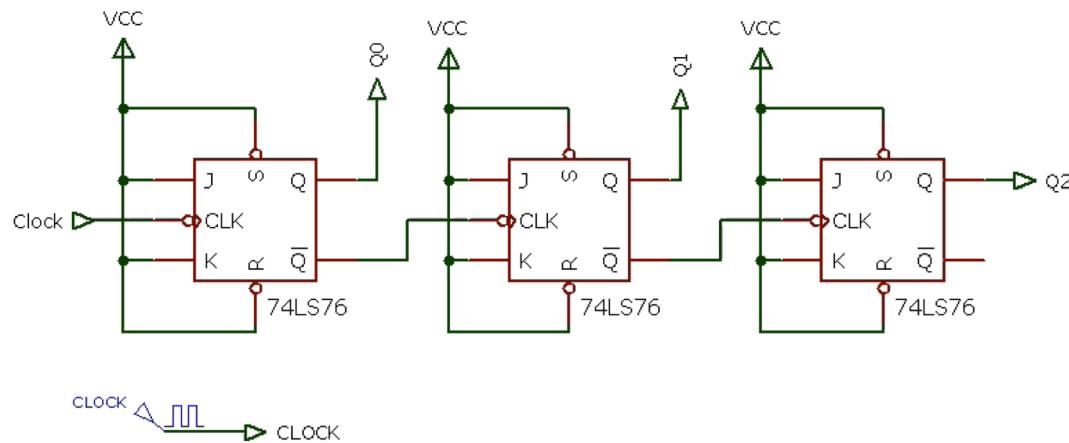


Exemplo Contadores Assíncronos:

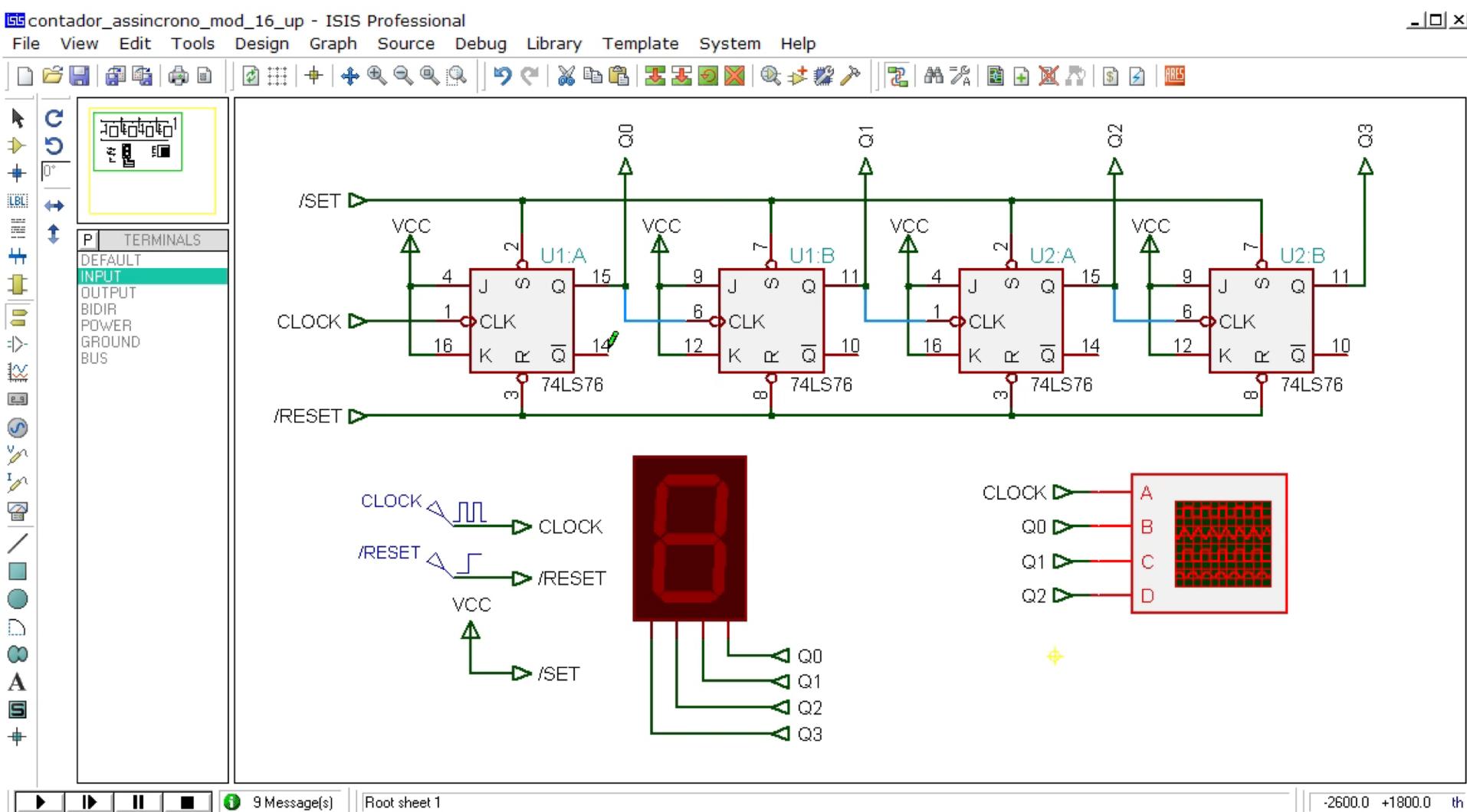
Crescente ↗



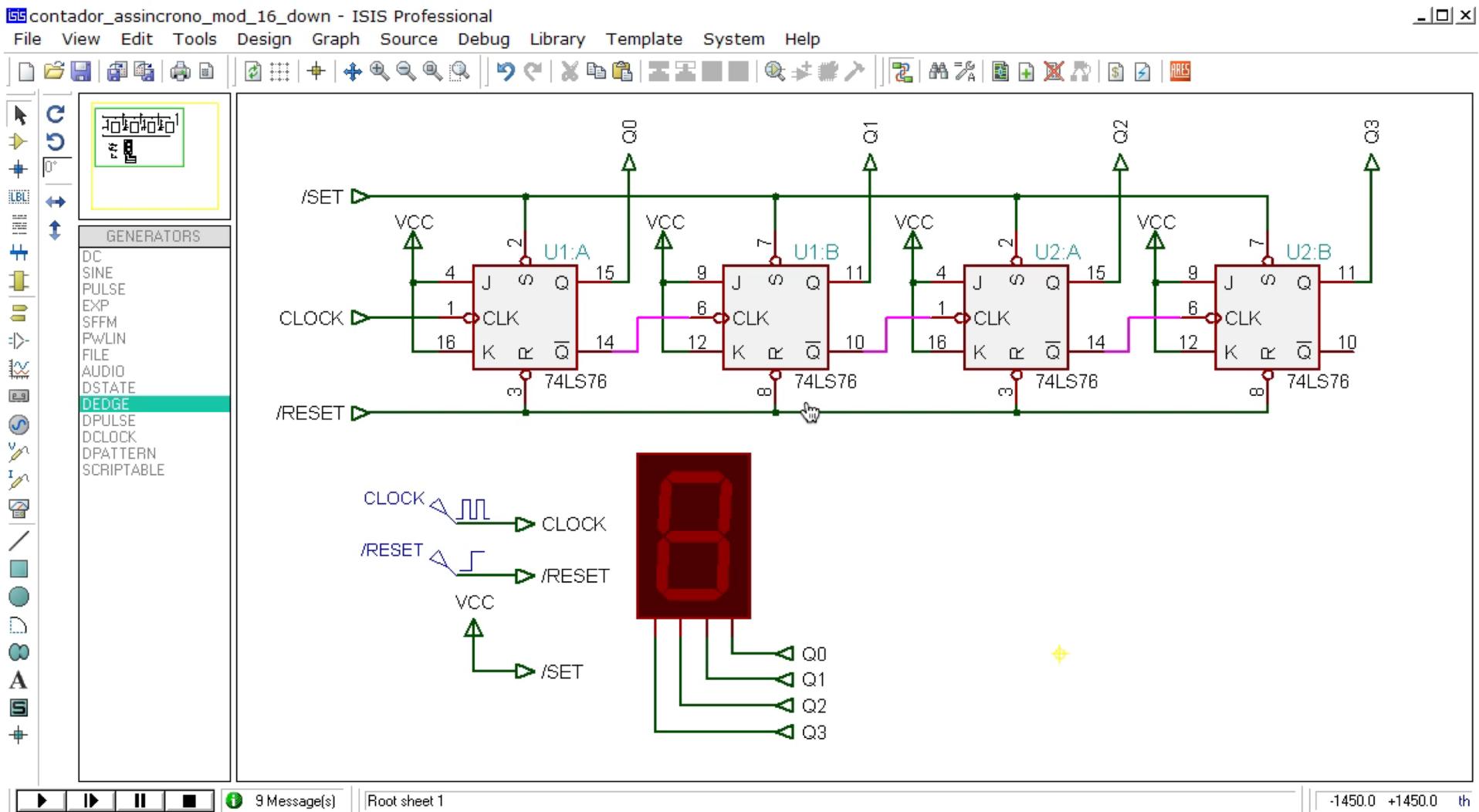
Decrescente ↘



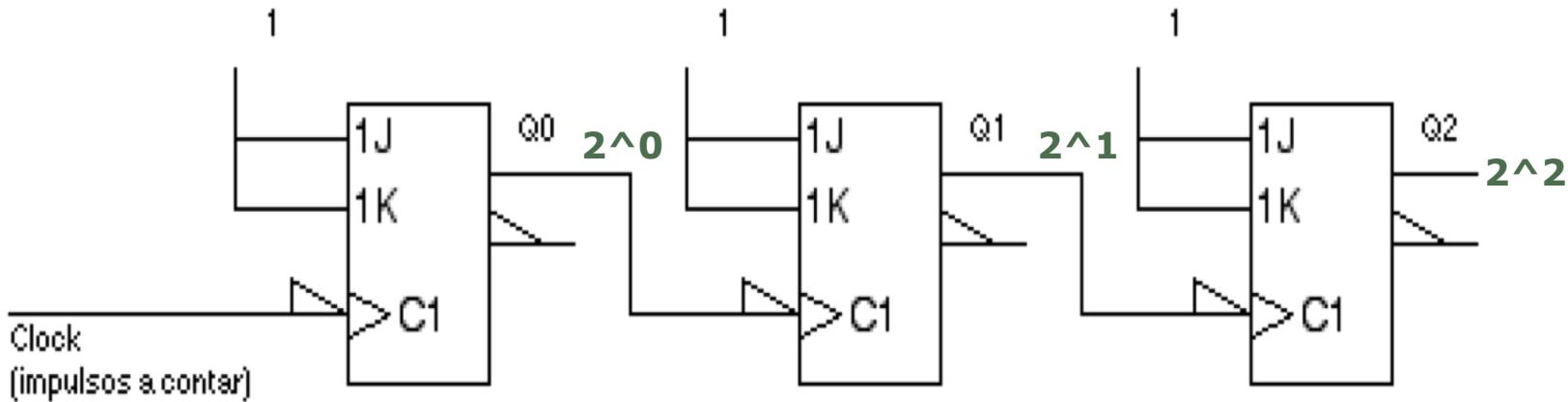
Contador assíncrono MOD-16 crescente:



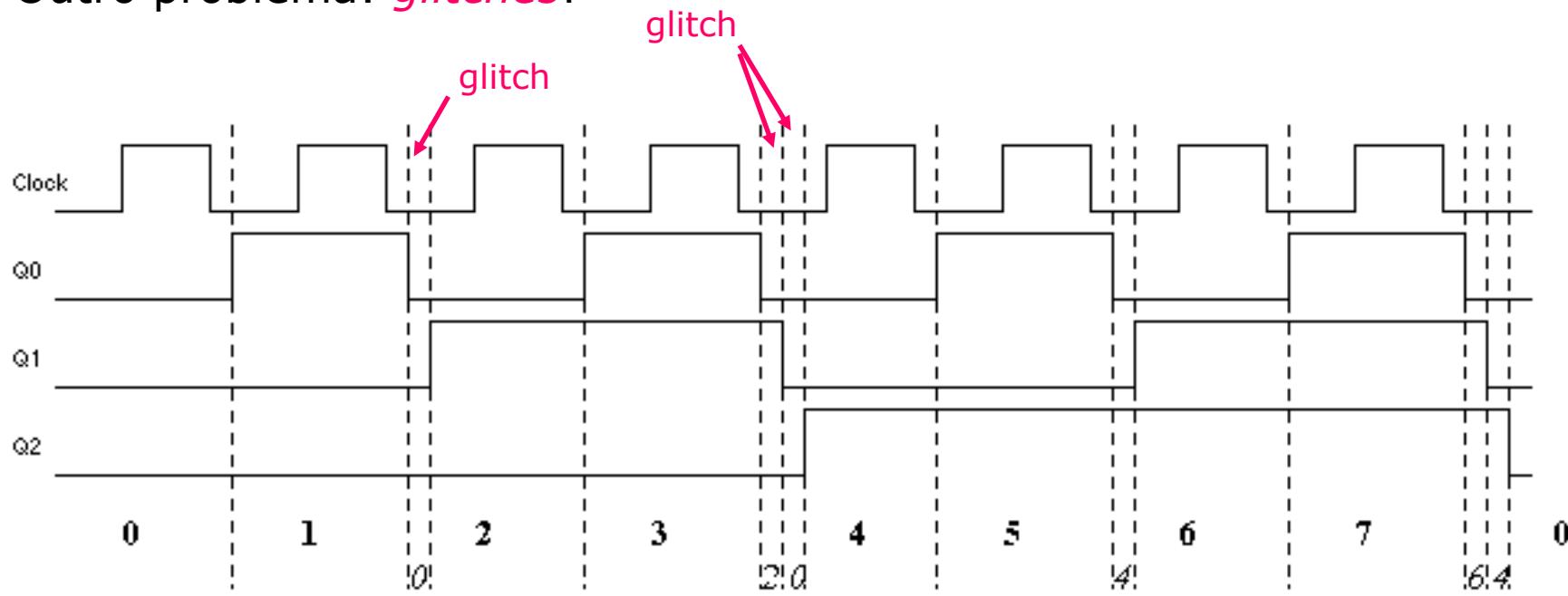
Contador assíncrono MOD-16 decrescente:



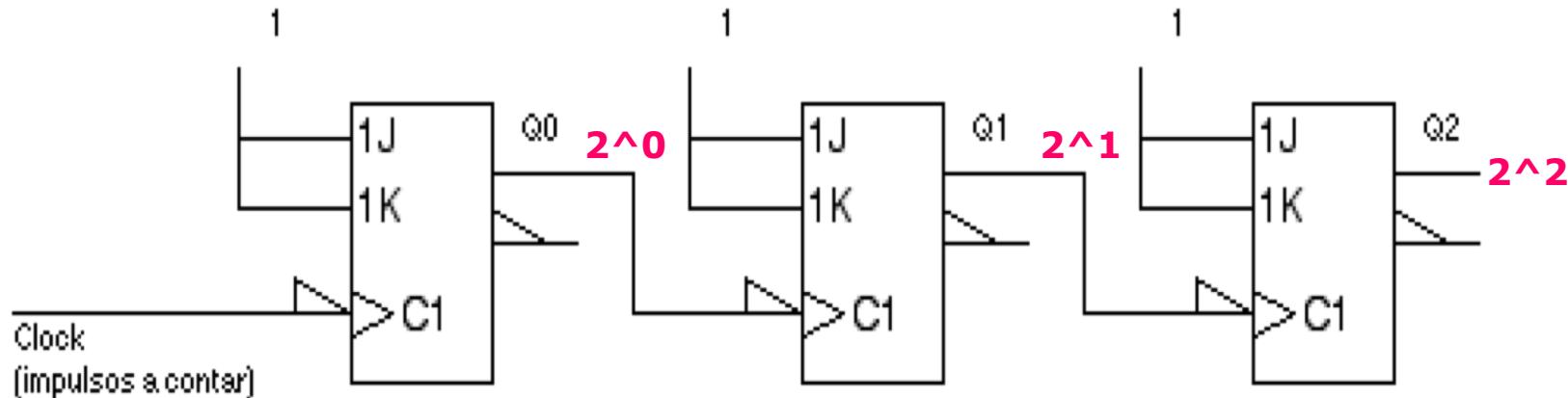
Exemplo 3) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



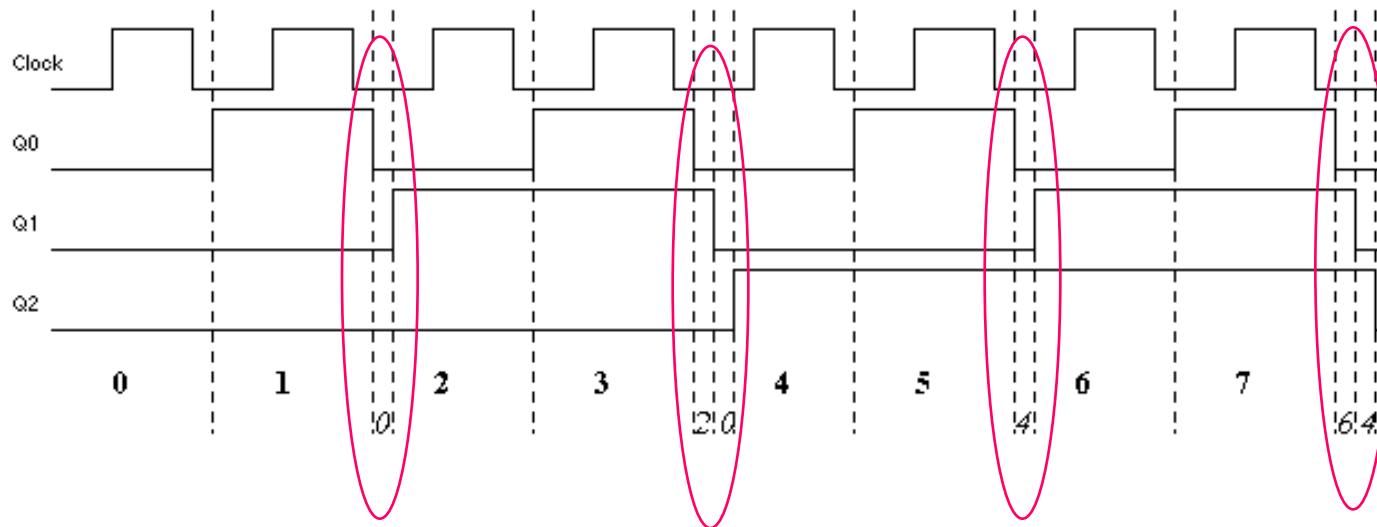
Outro problema: *glitches!*



Exemplo 3) Contador assíncrono crescente de módulo 8 (2^3):
conta de 0 até 7:



Outro problema: *glitches!*



Glitches: Estados de contagem transitórios.

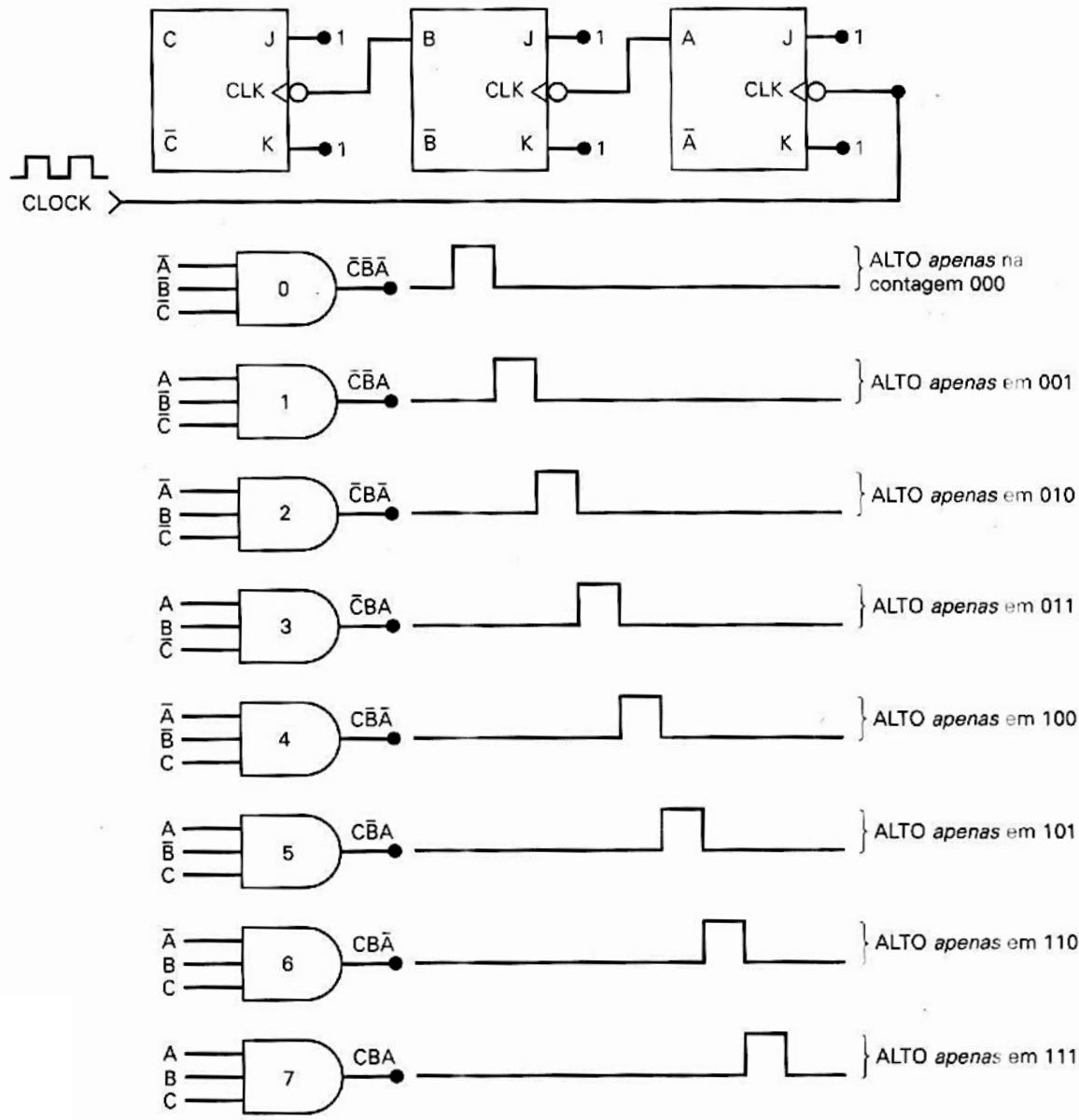
Tabela de Contagem:

Clock	Qc	Qb	Qa	Contagem
0	0	0	0	0
1	0	0	1	1
2	0	0	0	0
2	0	1	0	2
3	0	1	1	3
4	0	1	0	2
4	0	0	0	0
4	1	0	0	4
5	1	0	1	5
6	1	0	0	4
6	1	1	0	6
7	1	1	1	7
8	0	0	0	0
9	0	0	1	1
:	:	:	:	:

Inconvenientes (desvantagens) de um círcuito contador assíncrono:

Suponha que a saída deste contador seja decodificada.

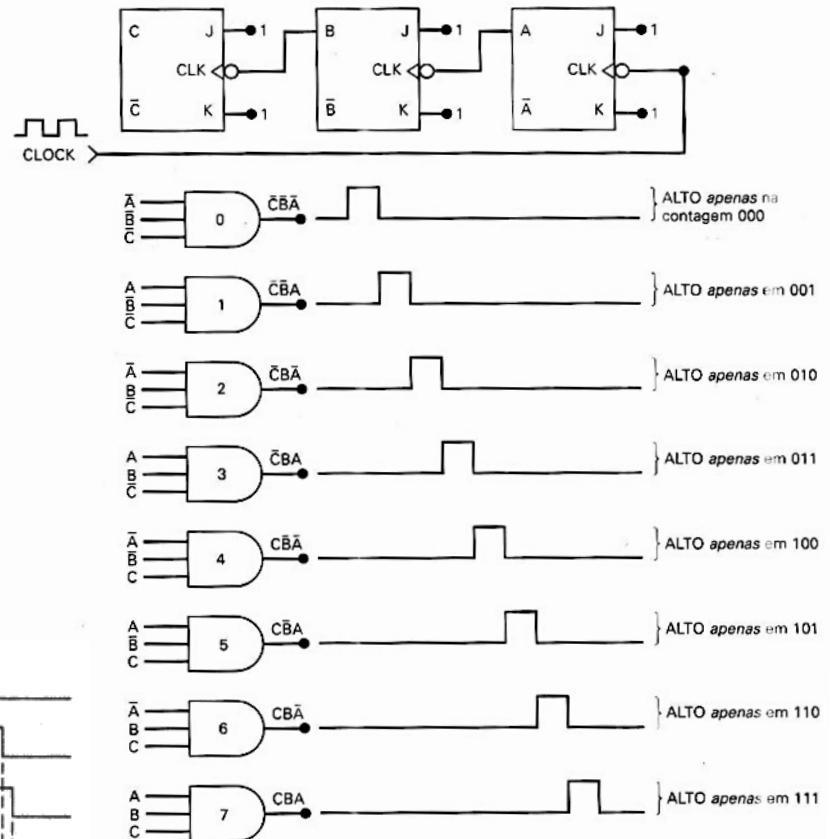
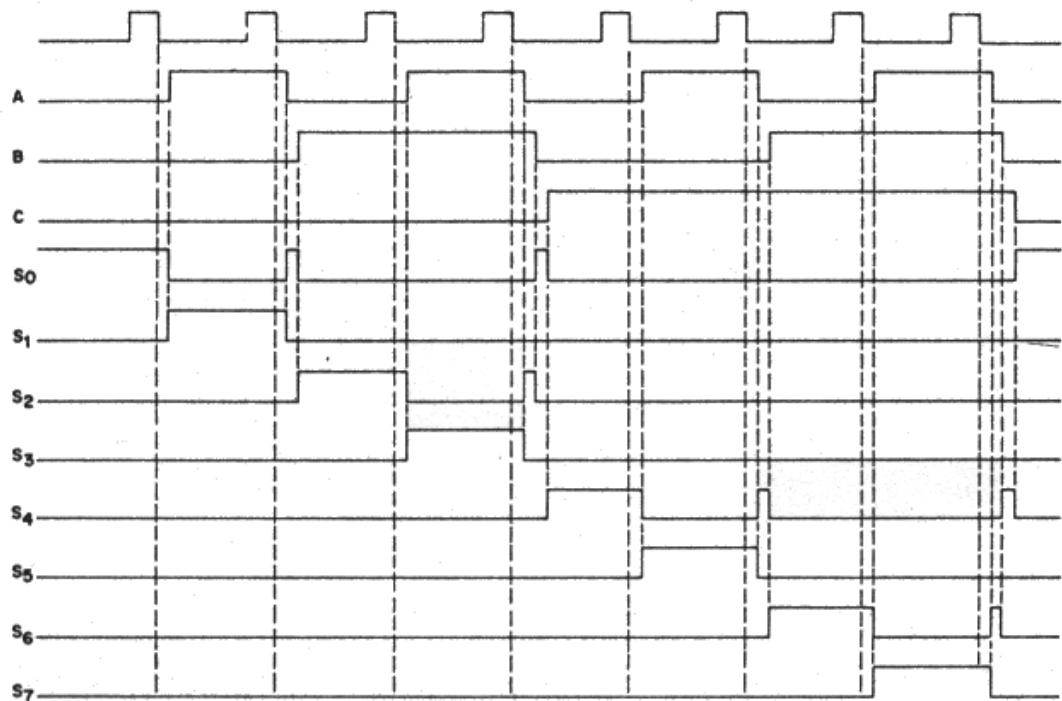
Haverá problemas....



Inconvenientes (desvantagens) de um círcuito contador assíncrono:

Suponha que a saída deste contador seja decodificada.

Haverá problemas....



Inconvenientes (desvantagens) de um círcuito contador assíncrono:

Clock	Qc	Qb	Qa	Contagem
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	0	1	0	2
4	0	0	0	0
4	1	0	0	4
5	1	0	1	5
6	1	0	0	4
6	1	1	0	6
7	1	1	1	7
8	0	0	0	0
9	0	0	1	1
:	:	:	:	:

Suponha que a saída deste contador seja decodificada.

Haverá problemas....

Note que este circuito gera pulsos de decodificação falsos – “glitches” (figura 4.20).

Solução?

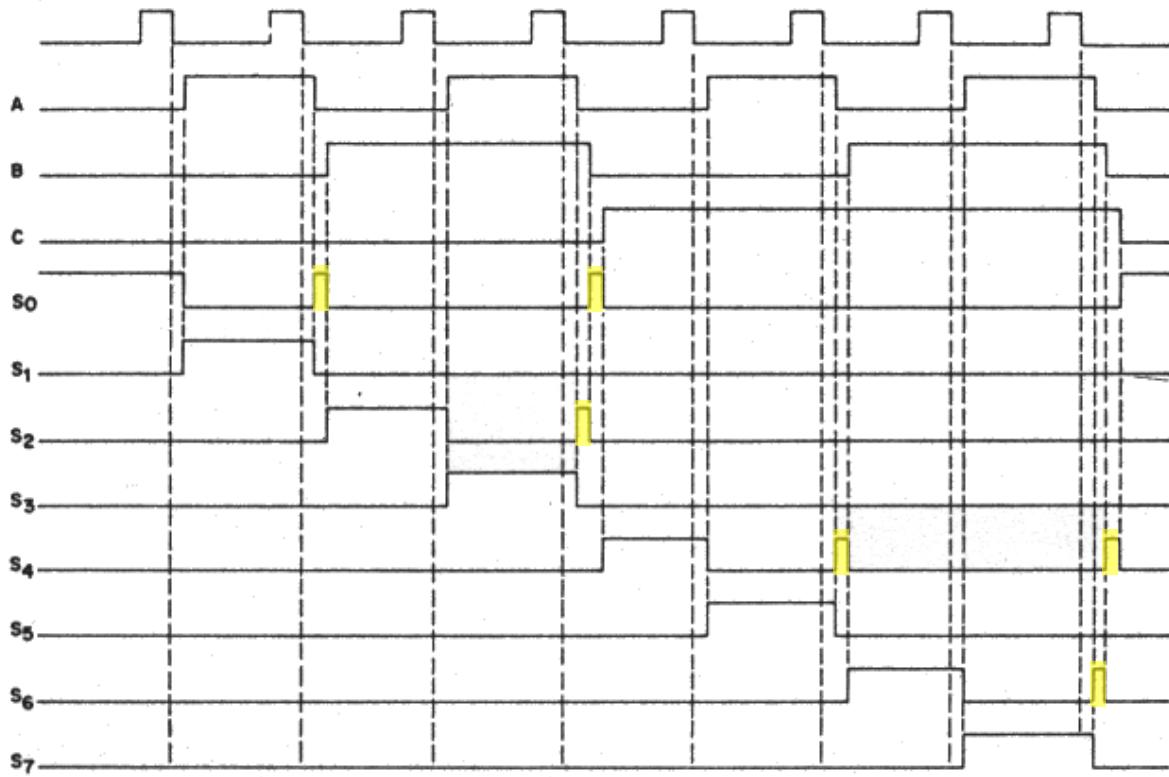
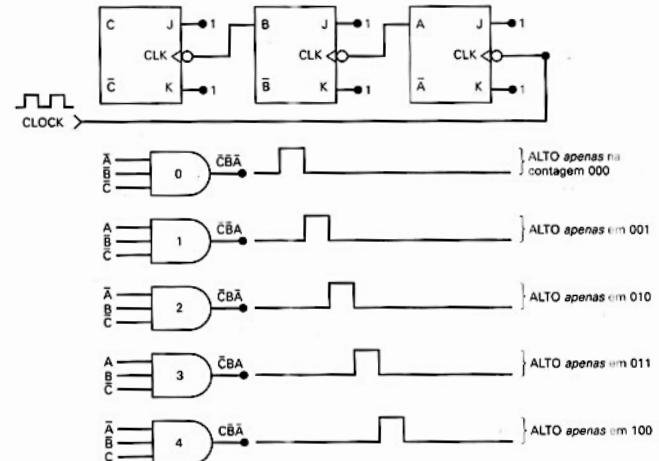


Figura 4.20

Inconvenientes (desvantagens) de um círcuito contador assíncrono:

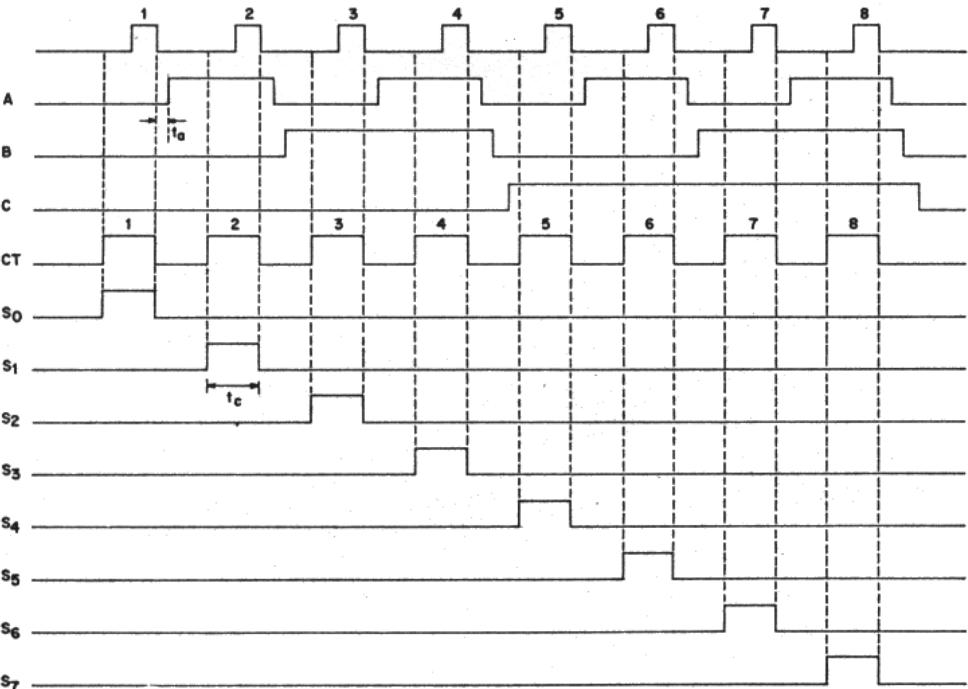
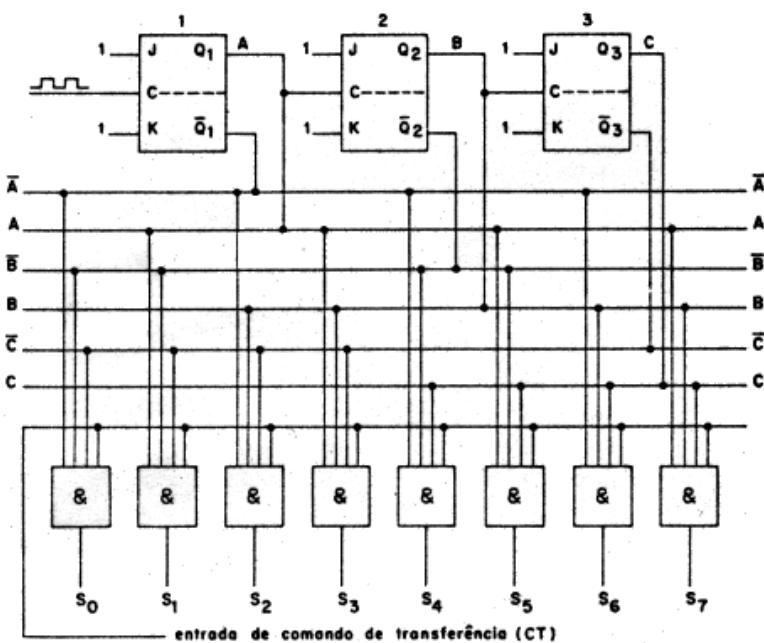
Suponha que a saída deste contador seja decodificada.

Haverá problemas....

Note que este circuito gera pulsos de decodificação falsos – “glitches” (figura 4.20).

Solução:

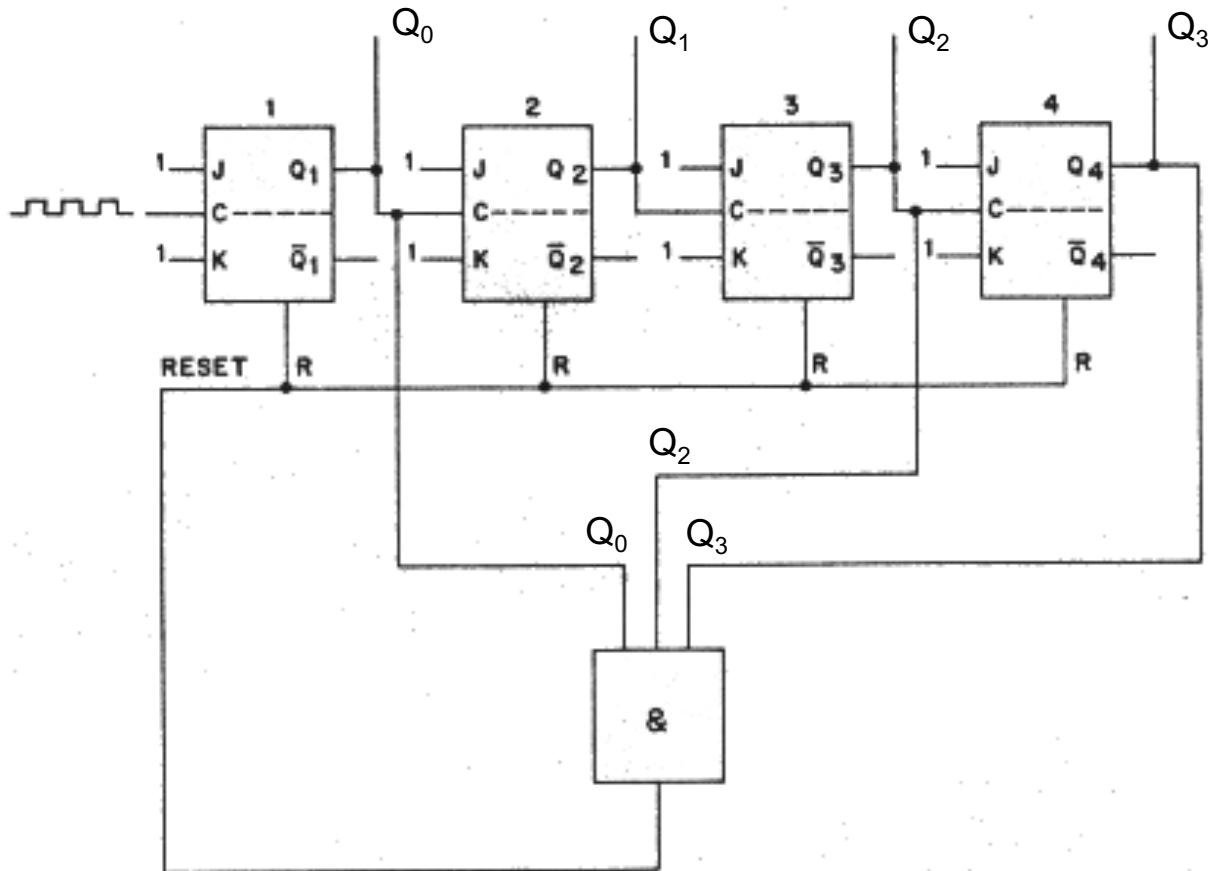
Agregar o sinal “CT” (Comando de Transferência), possivelmente em sincronismo com sinal de clock..



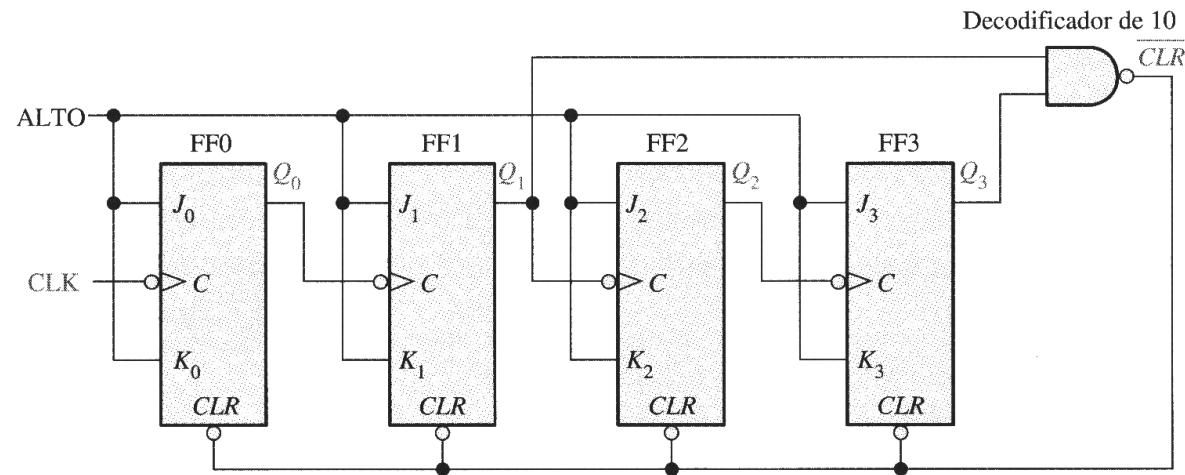
Exemplo:
Contador assíncrono
modulo-13

Note:

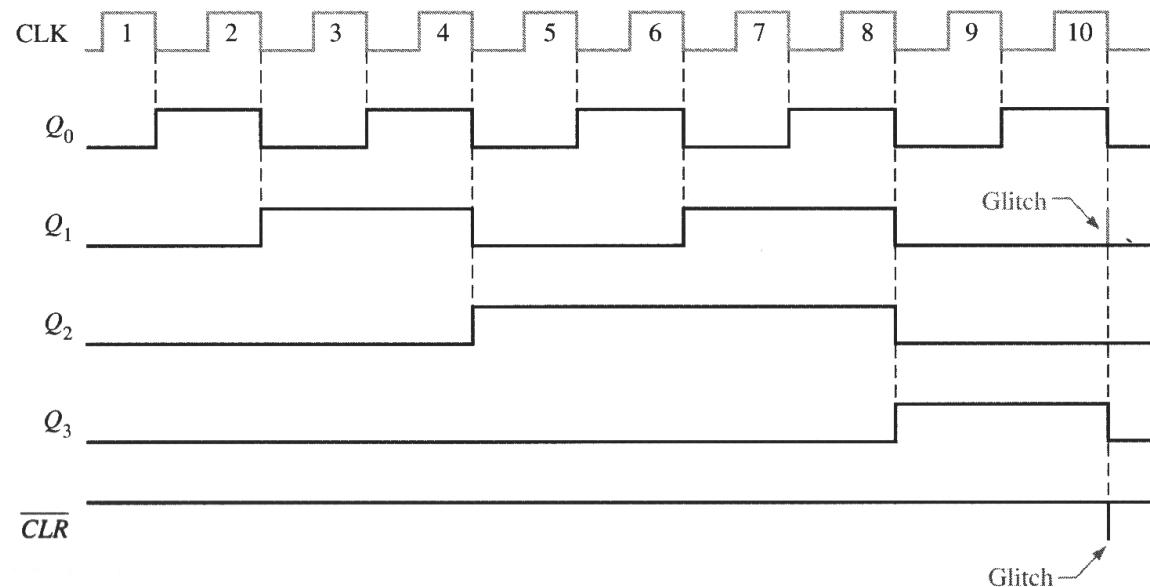
$$13_{(10)} = \begin{matrix} Q_3 & Q_2 & Q_1 & Q_0 \\ 1 & 1 & 0 & 1 \end{matrix}_{(2)}$$



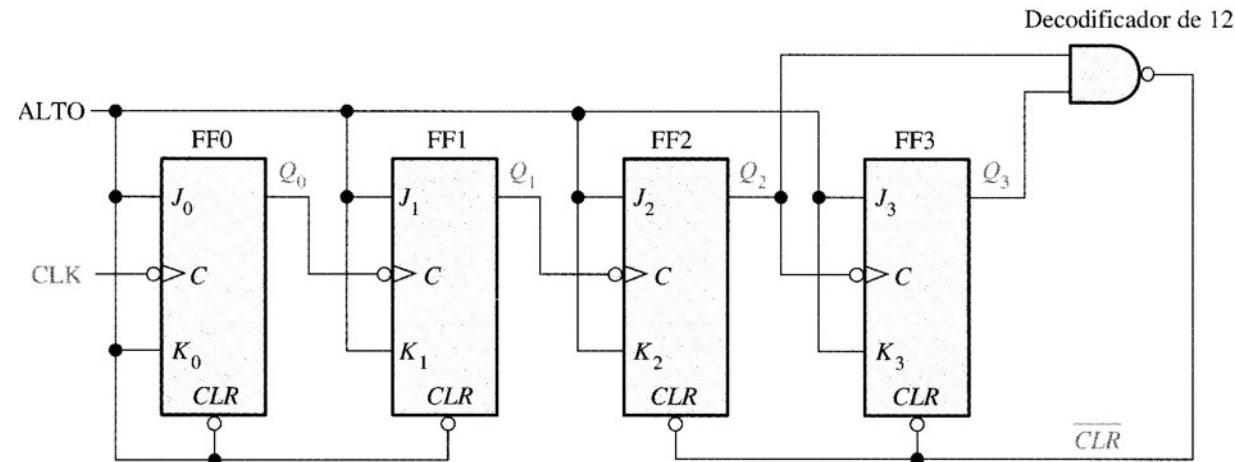
Exemplo 4) contador assíncrono módulo 10:



Note:
 $10_{(10)} = 1010_{(2)}$

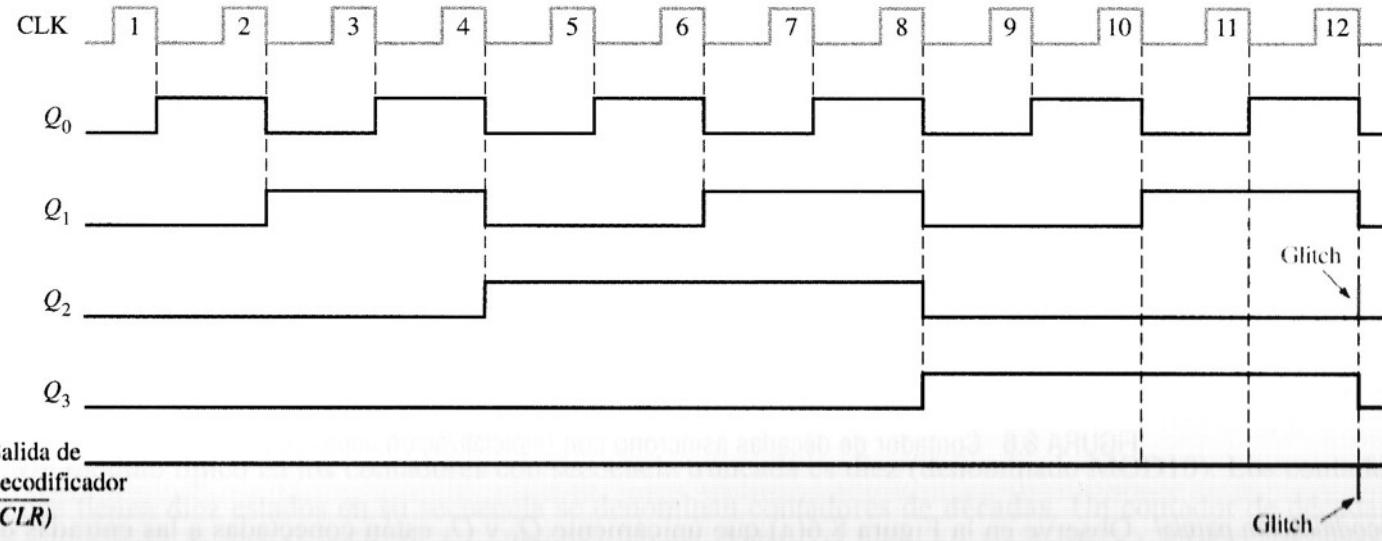


Exemplo 5) Contador assíncrono módulo 12:

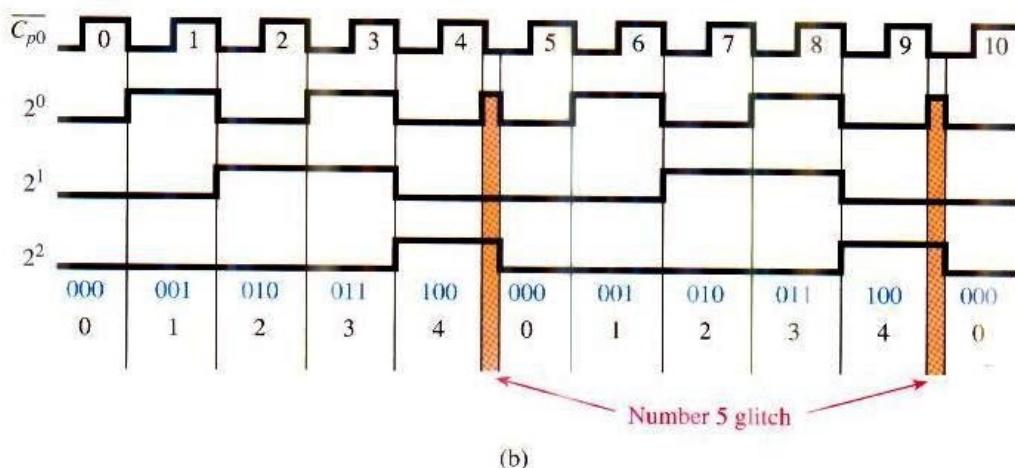
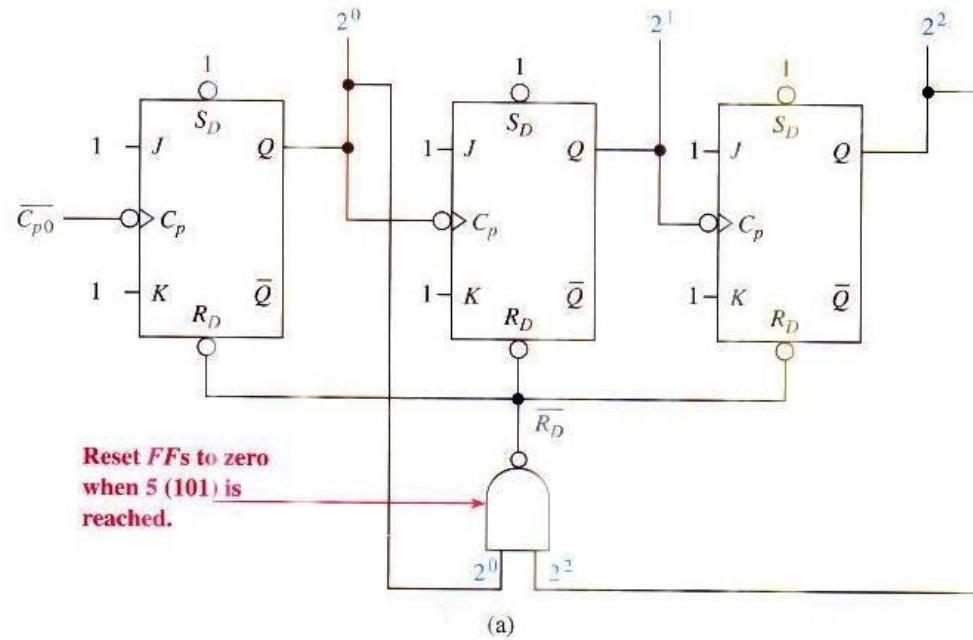


Note:
 $12_{(10)} = 1100_{(2)}$

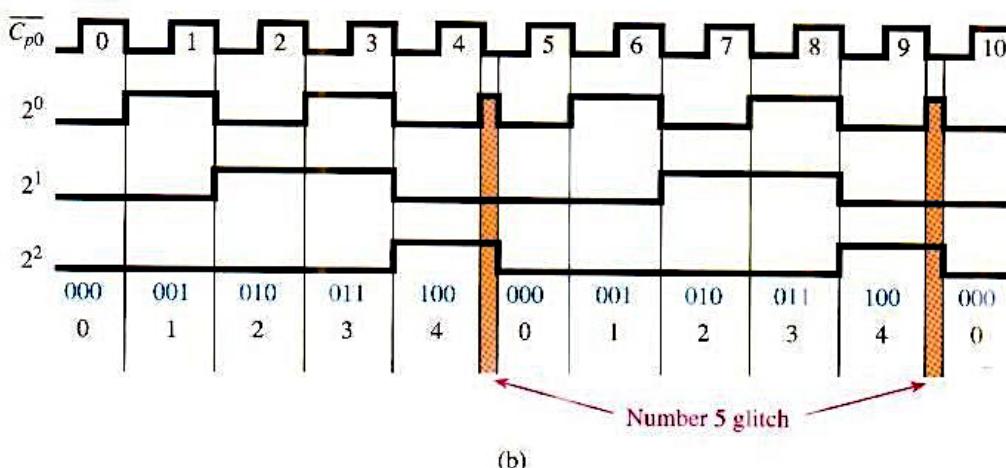
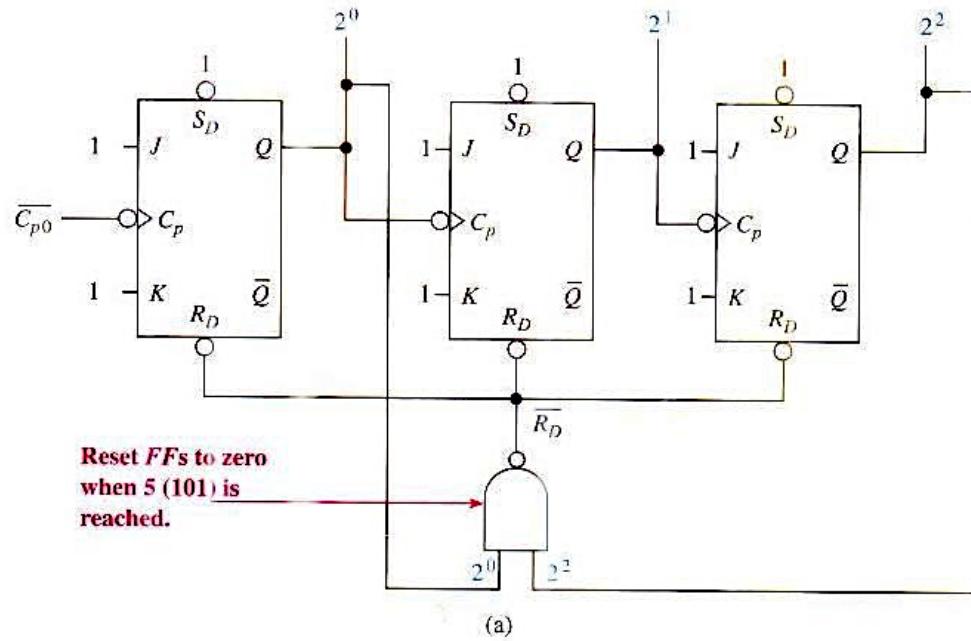
a)



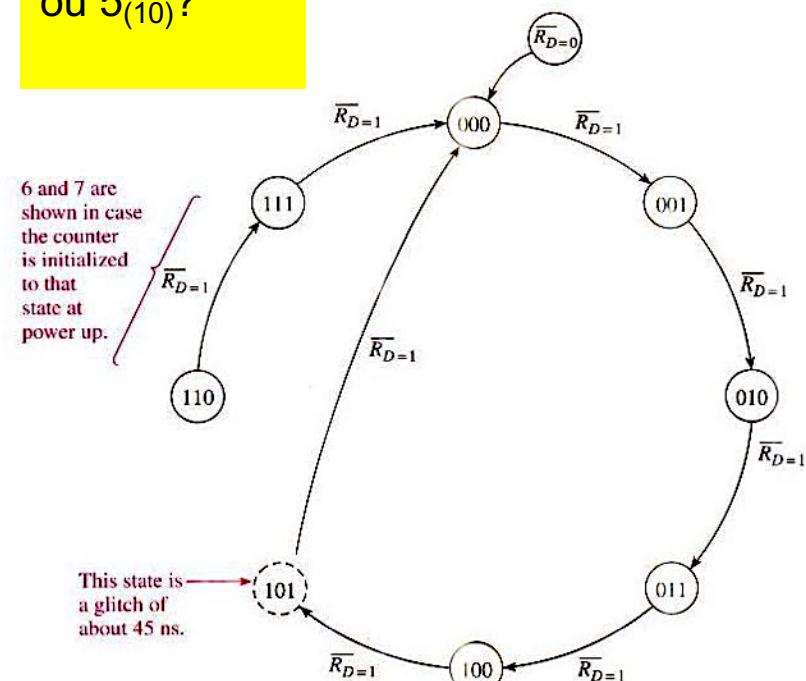
Exemplo 6: Contador Assíncrono de módulo-5



Exemplo 6: Contador Assíncrono de módulo-5

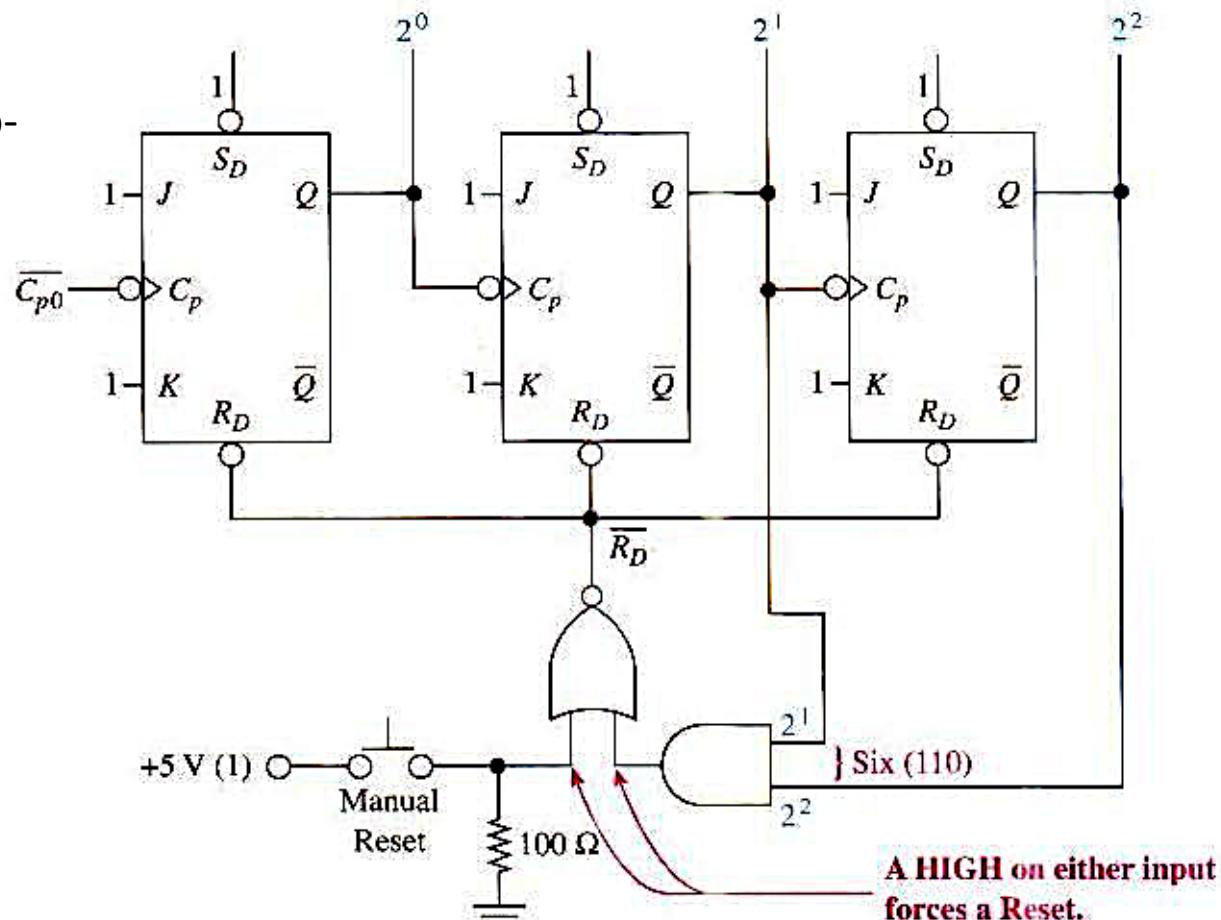


E se circuito
iniciar nos
estados $6_{(10)}$
ou $5_{(10)}$?



Exemplo 7:

Contador assíncrono módulo-6 crescente resetável manualmente via botão externo.

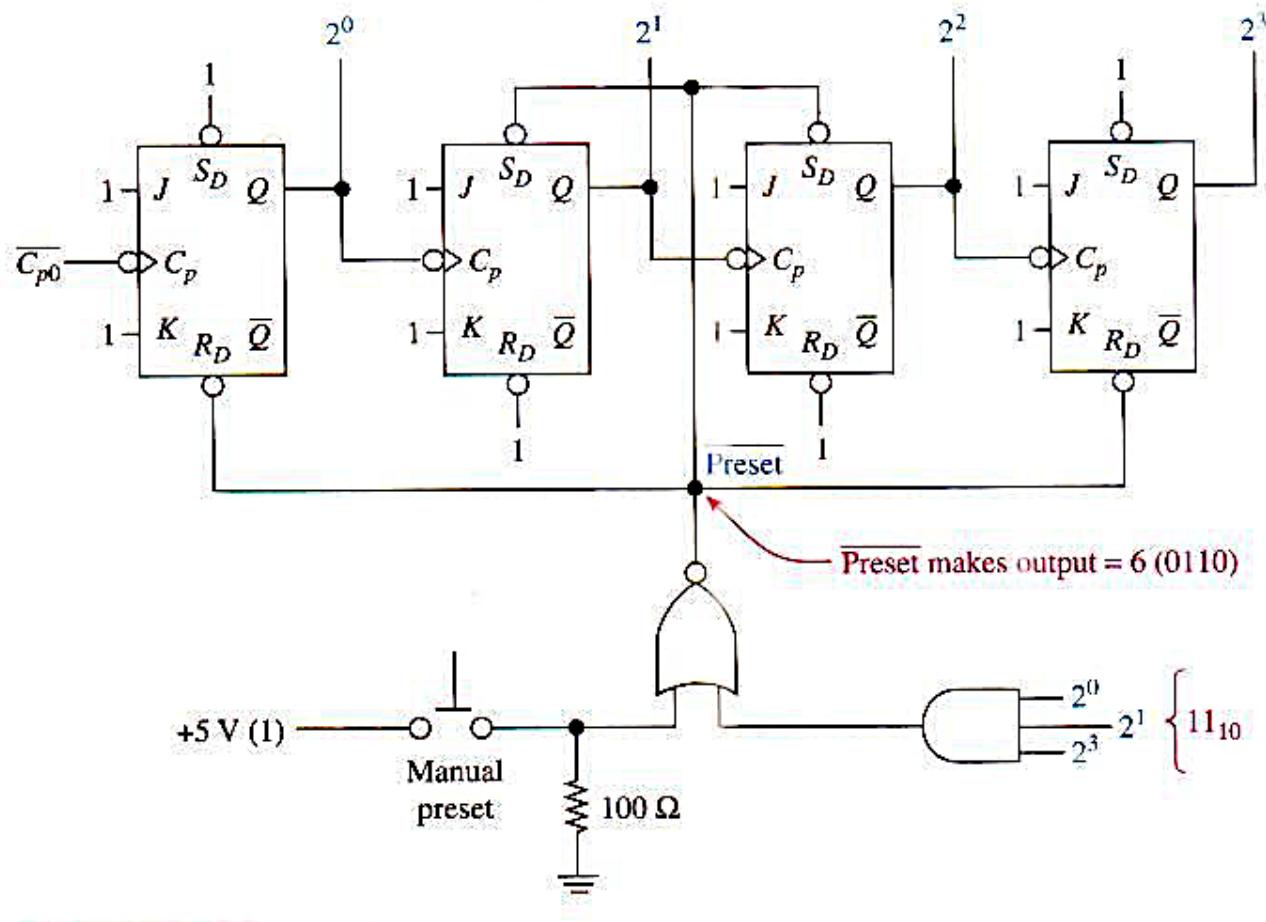
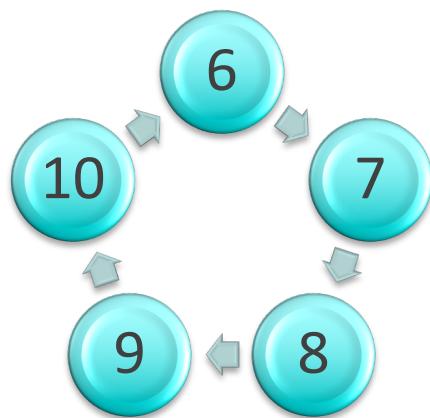


Questões extras:

- Por que o valor do resistor de “pull-down” é baixo?
- O que aconteceria se fosse usado um resistor de $10\text{ K}\Omega$?

Exemplo 8:

Contador crescente de módulo-5 que conta na sequência:



- O que acontece se os FFs iniciarem resetados?

Problema:

Projetar um contador
que conte: 0-1-2-3-4-5 e
que então se detenha e
ative um Led.

Obs.: O processo só
deve ser iniciando
apertando-se um botão
de “Start”.

Problema:

Projetar um contador que conte: 0-1-2-3-4-5 e que então se detenha e ative um Led.

Obs.: O processo só deve ser iniciando apertando-se um botão de “Start”.

