

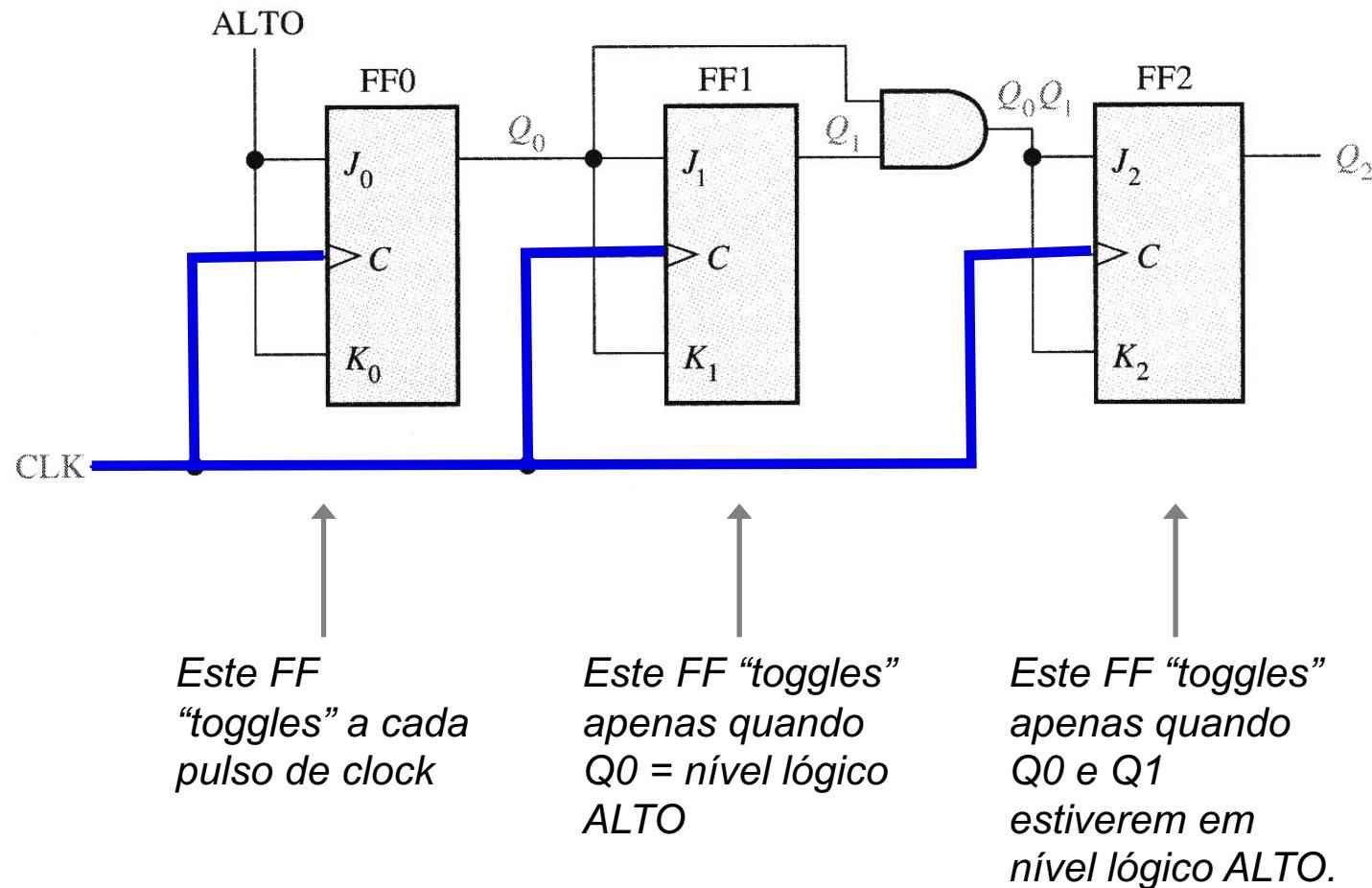


Contadores Síncronos

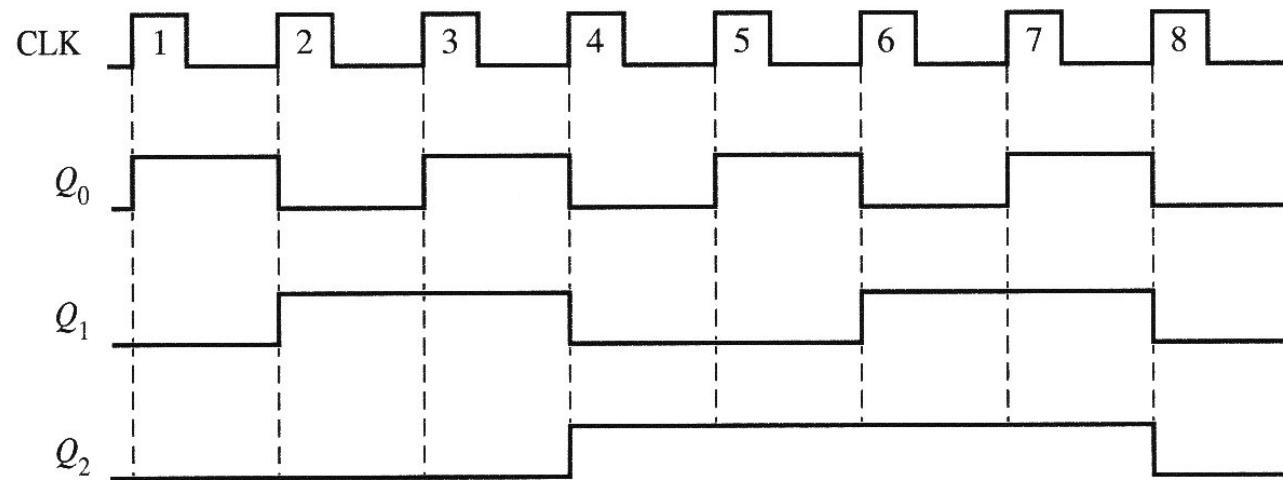
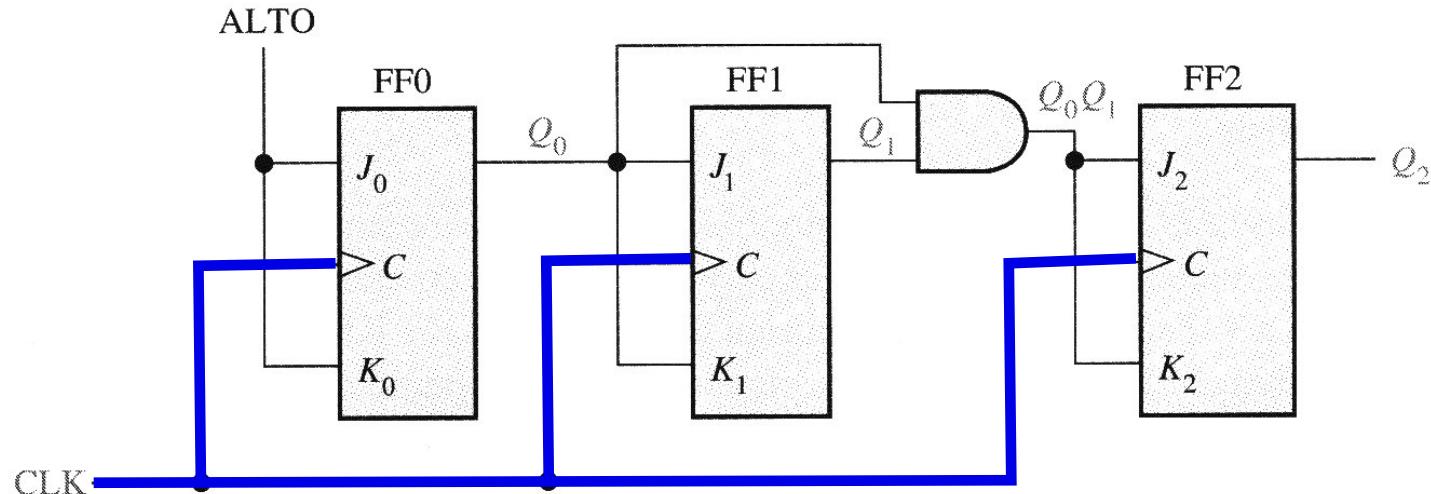
Prof. Fernando Passold

Oct/2008, Abr/2020, 2022.

Contador síncrono binario de 3 bits:

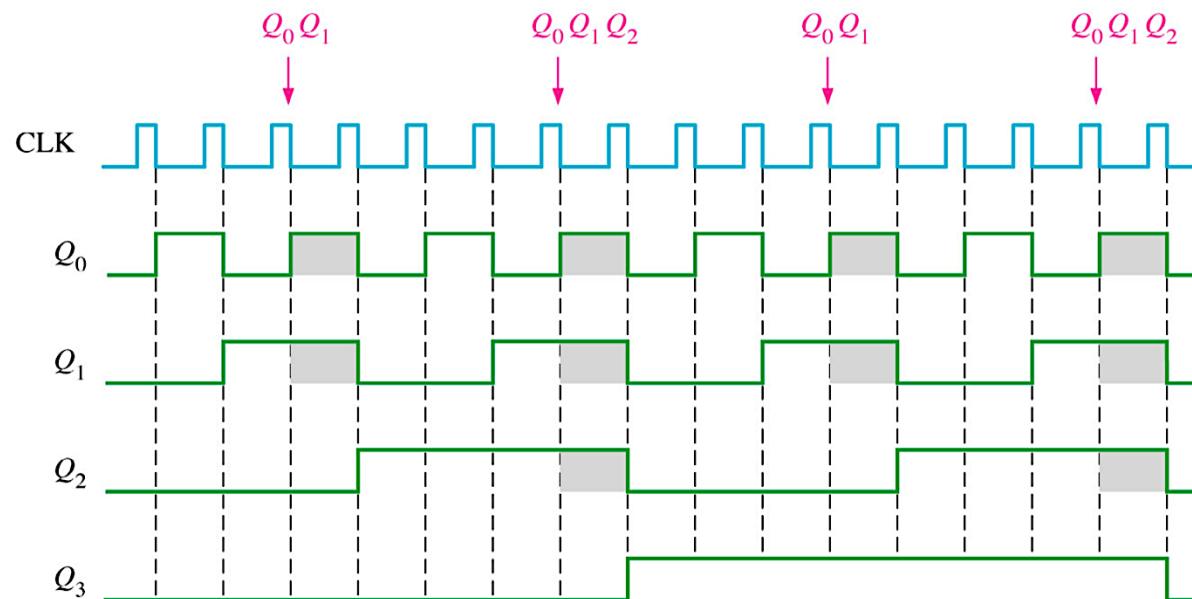
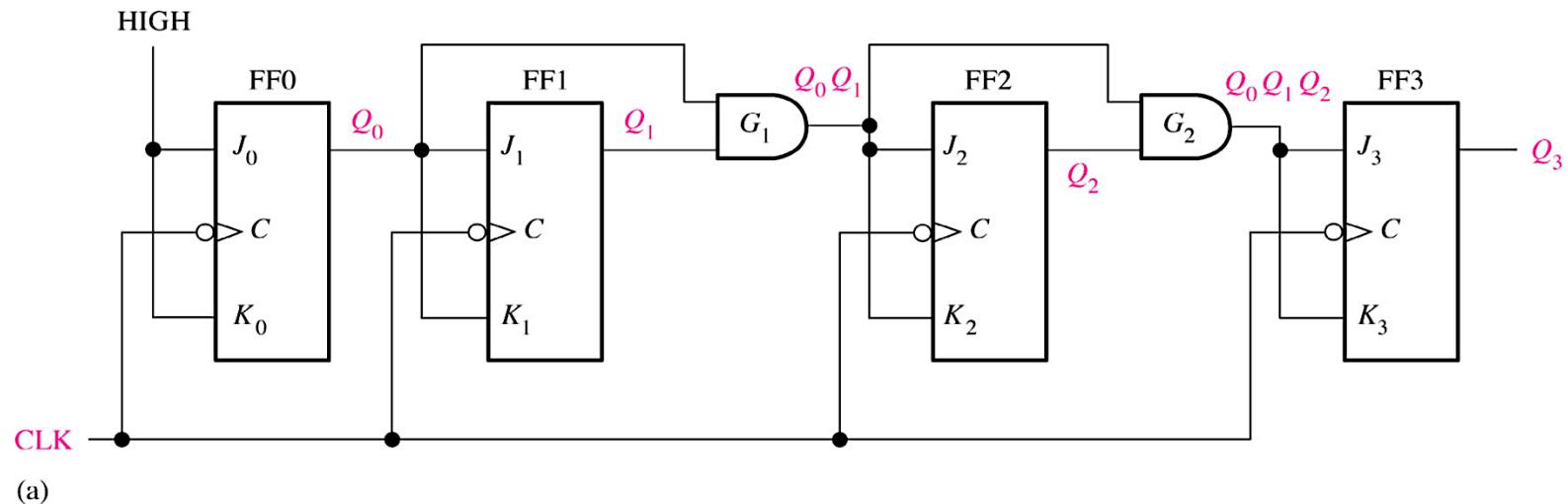


Contador síncrono binário de 3 bits:



Advertência: não
estão retratados
os atrasos de
propagação dos
FFs.

Contador síncrono binário de 4 bits:



Contador síncrono × assíncrono – Detalhes:

Contador síncrono 3 bits (módulo 8):

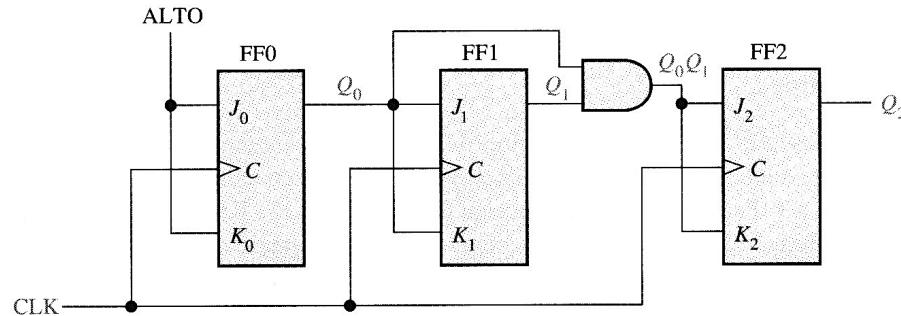
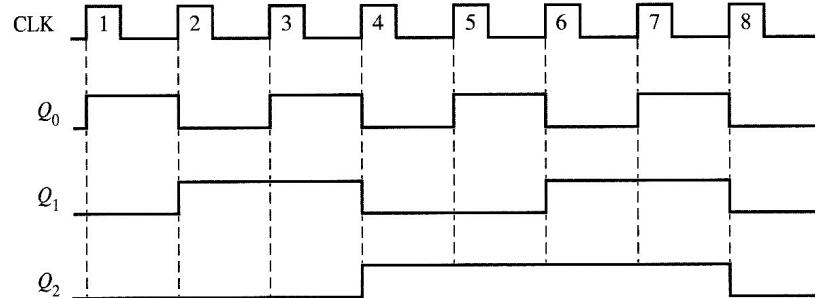


FIGURA 8.14 Contador binario síncrono de 3 bits.



Contador assíncrono 3 bits (módulo 8):

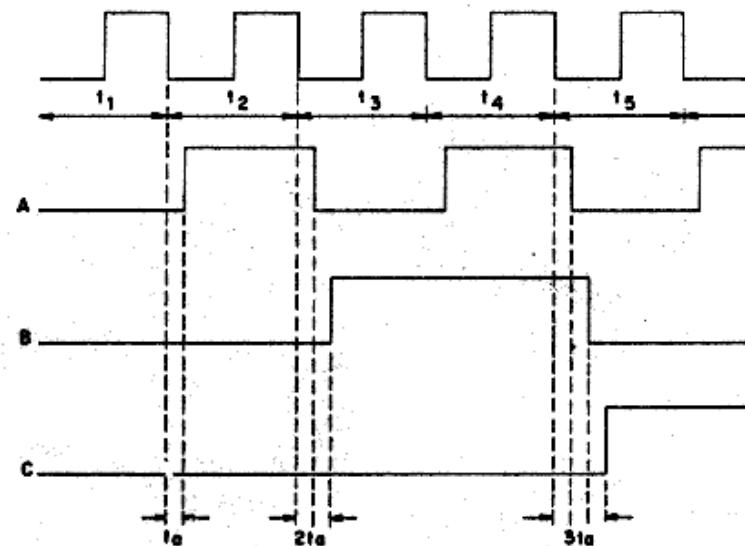
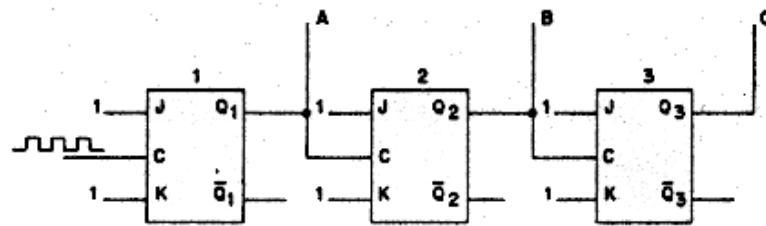
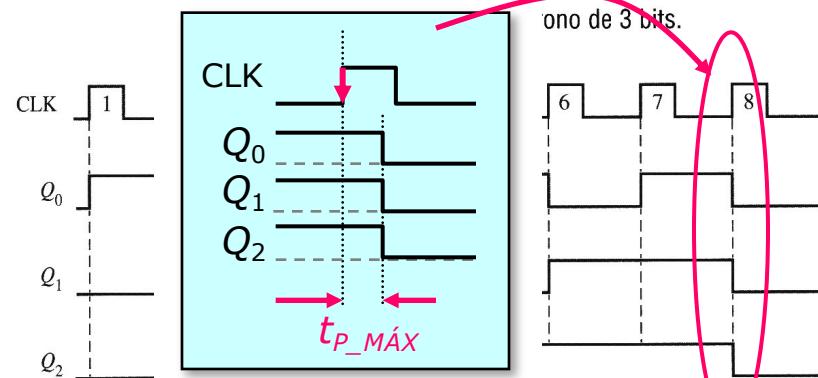
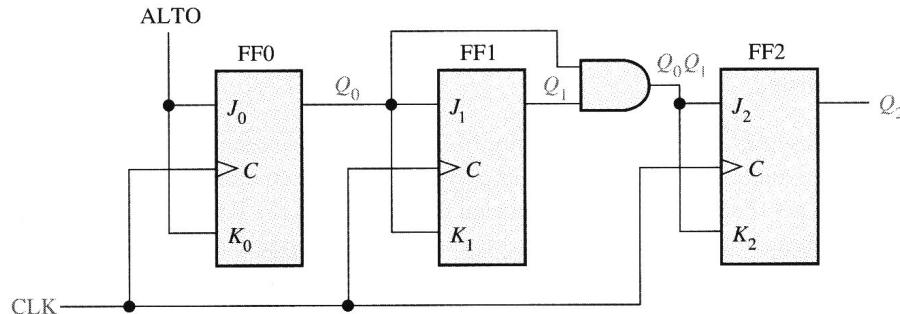


Figura 4.18

Contador síncrono × assíncrono – Detalhes:

Contador síncrono 3 bits (módulo 8):



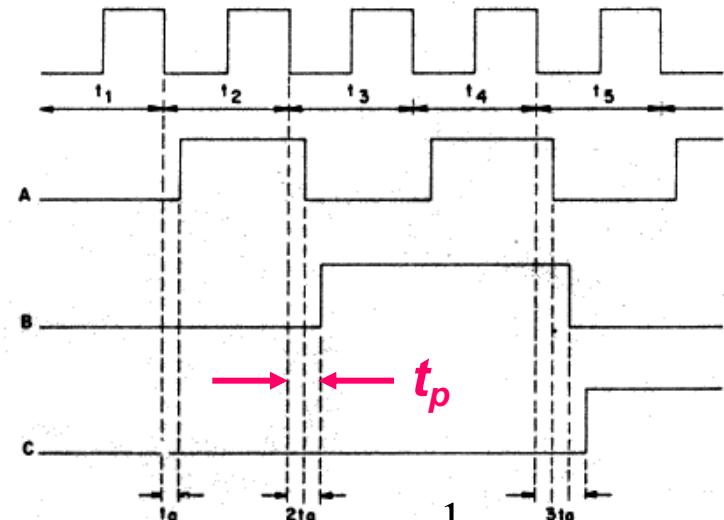
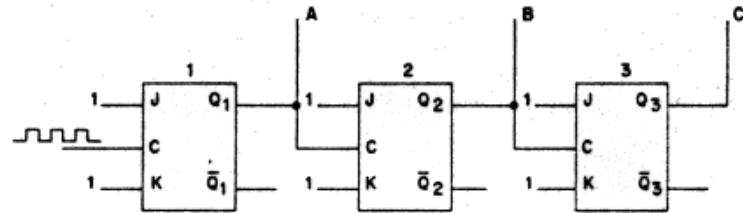
$$f_{MÁX} = \frac{1}{t_{P_{MÁX}}}$$

$$f_{MÁX} = \frac{1}{20 \times 10^{-9}}$$

$$f_{MÁX} = 50 \text{ MHz}$$

| | Typ | Max | Min | Unit |
|-----------|-----------------------------|-----|-----|------|
| t_{PLH} | Clock, Clear, Set to Output | 15 | 20 | ns |
| t_{PHL} | Setup Time | | 20 | ns |
| t_s | | | | |
| t_h | Hold Time | | 0 | ns |
| f_{max} | | 45 | 30 | MHz |

Contador assíncrono 3 bits (módulo 8):



$$f_{MÁX} = \frac{1}{2 \times t_{P_{MÁX}}}$$

$$f_{MÁX} = \frac{1}{40 \times 10^{-9}}$$

$$f_{MÁX} = 25 \text{ MHz}$$

Contador síncrono × assíncrono – Detalhes:

- E sem problemas com *glitches*...

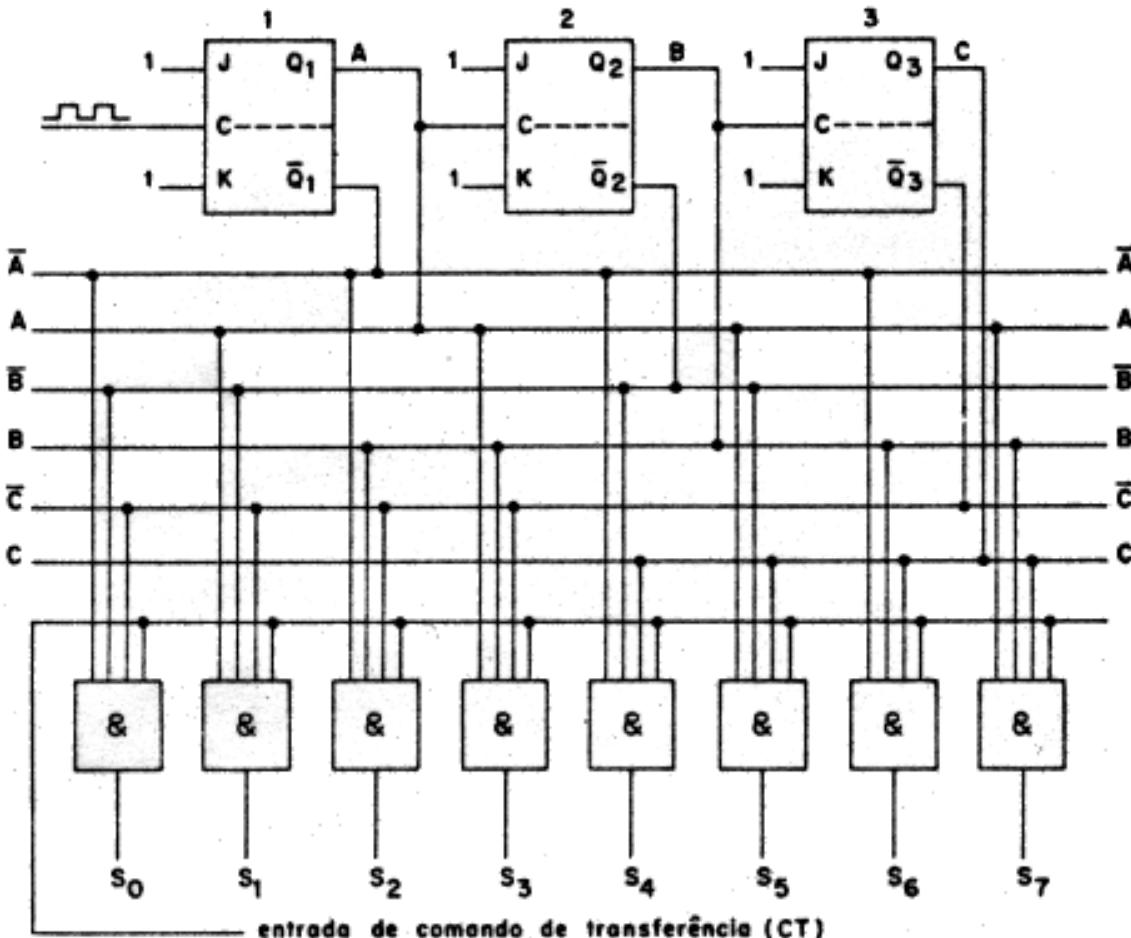


Figura acima: circuito de contador assíncrono con saídas decodificadas.

Contador síncrono × assíncrono – Detalhes:

- E sem problemas com *glitches*...

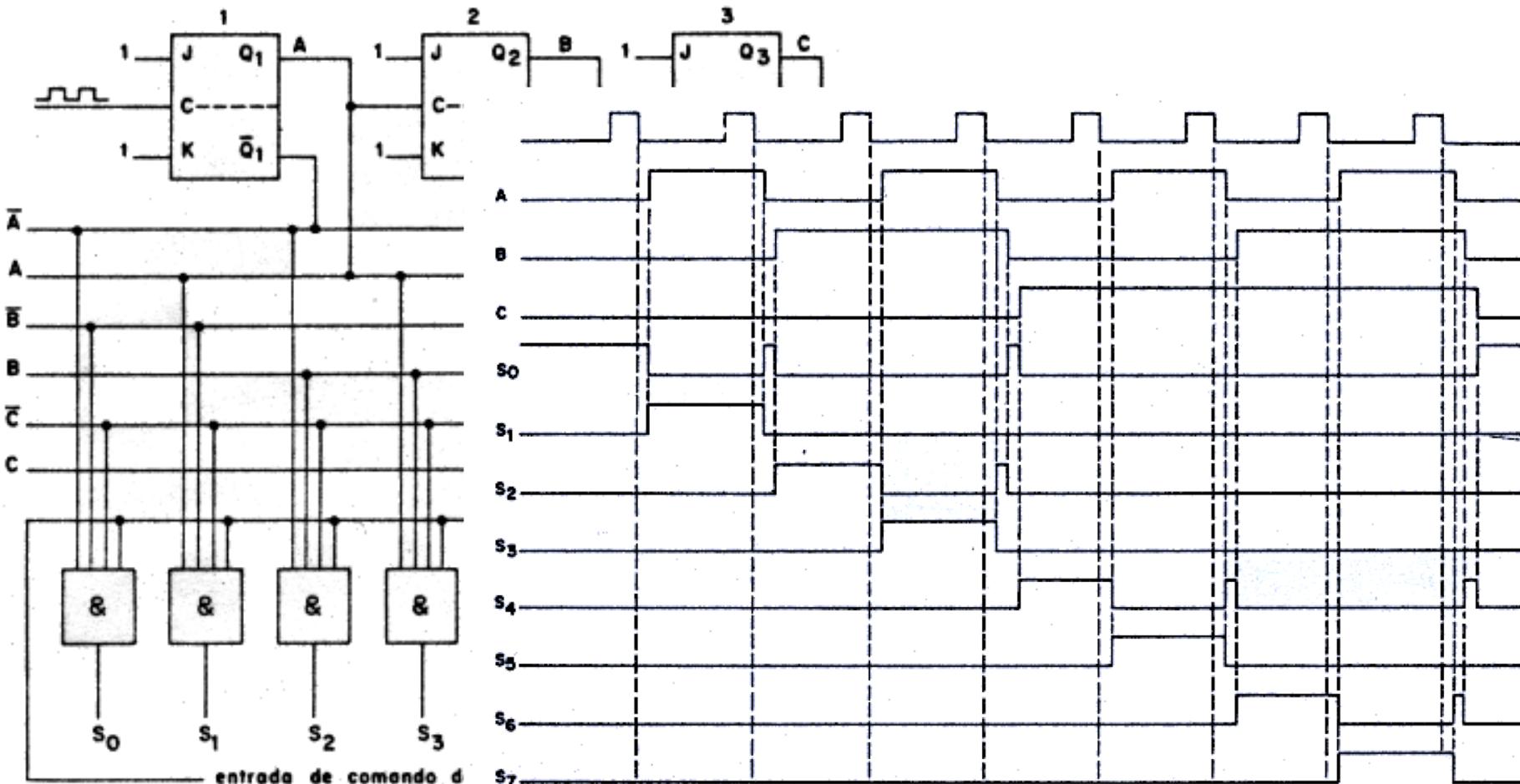


Figura acima: circuito de contador assíncrono con saídas decodificadas.

Contador síncrono × assíncrono – Detalhes:

- E sem problemas com *glitches*...

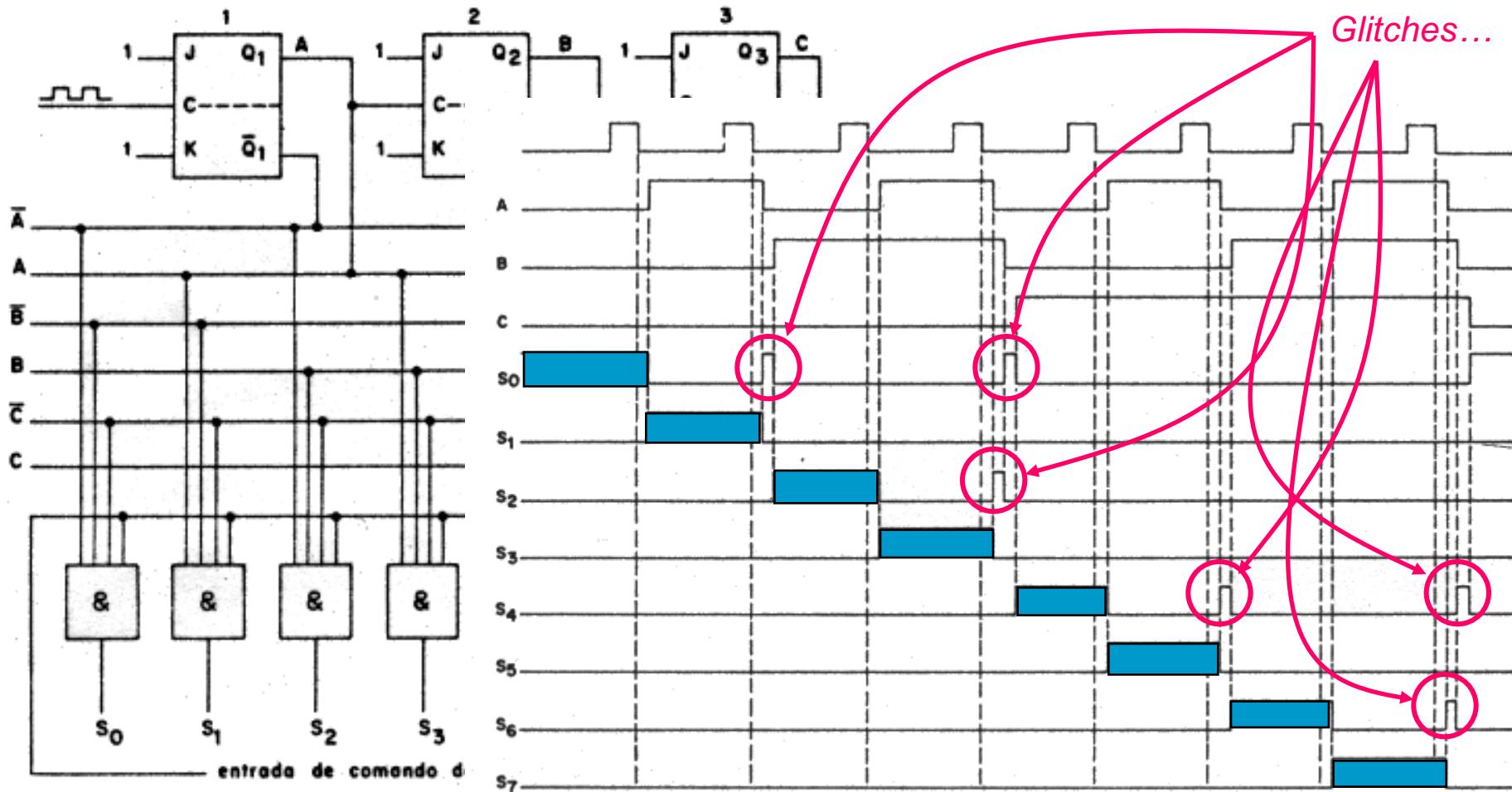
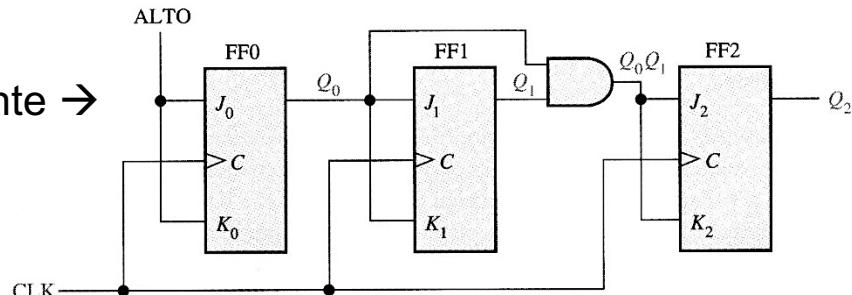


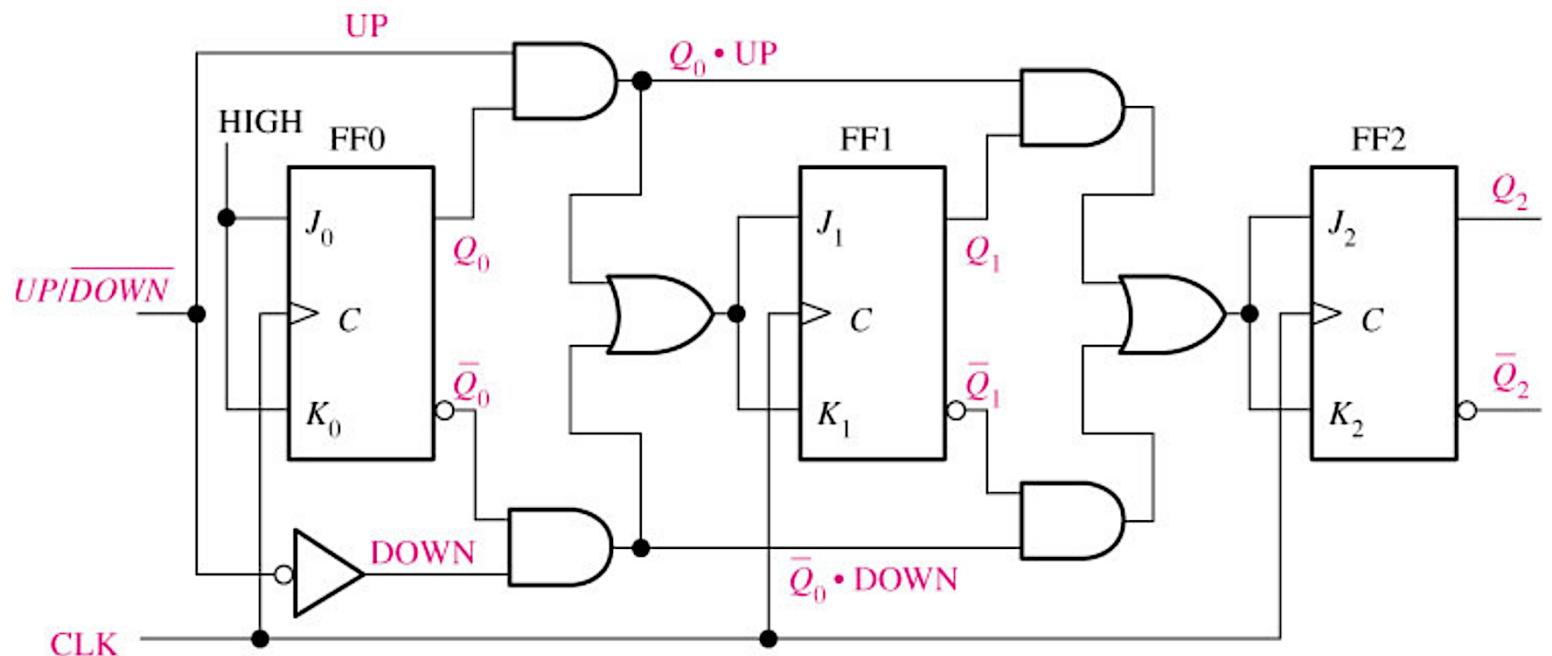
Figura acima: circuito de con-

Contador síncrono ascendente/descendente:

Contador síncrono crescente →

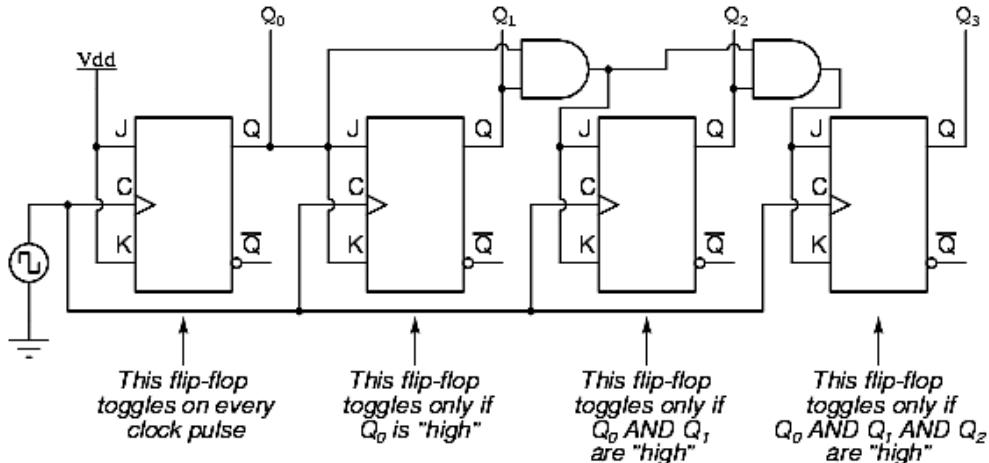


Comando
bidireccional

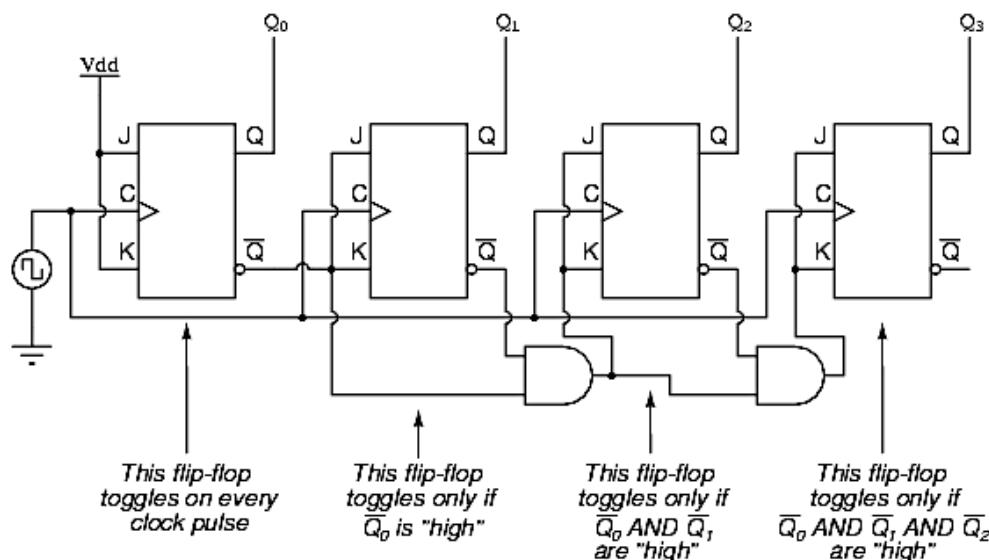


Contador síncrono ascendente/descendente (2):

A four-bit synchronous "up" counter

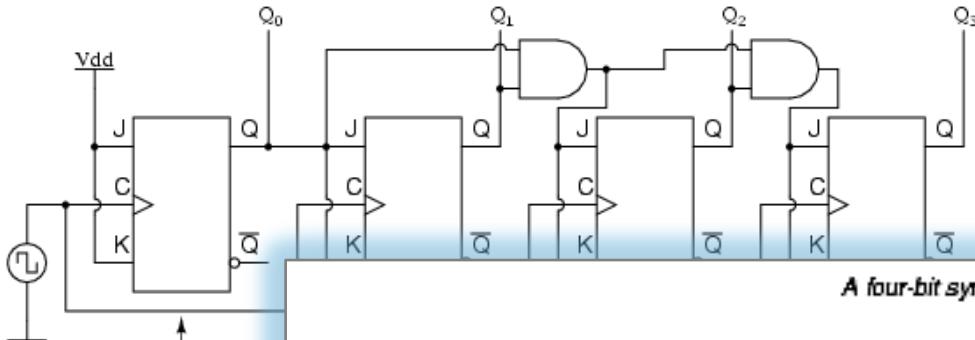


A four-bit synchronous "down" counter



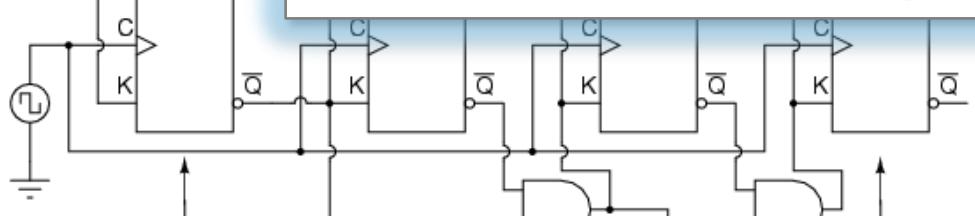
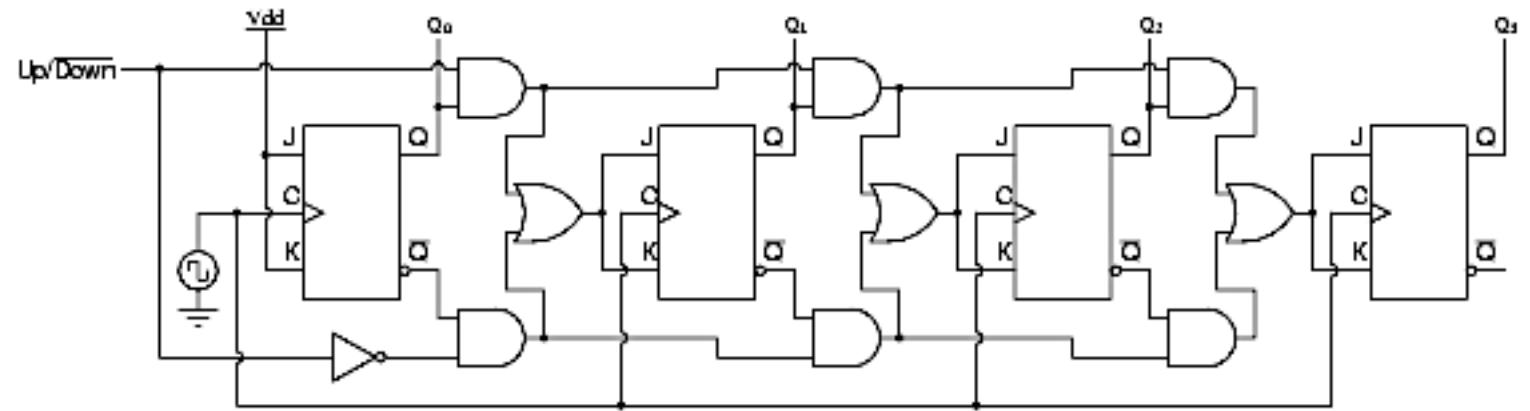
Contador síncrono ascendente/descendente (2):

A four-bit synchronous "up" counter



This flip-flop
toggles on every
clock pulse

A four-bit synchronous "up/down" counter



This flip-flop
toggles on every
clock pulse

This flip-flop
toggles only if
 \bar{Q}_0 is "high"

This flip-flop
toggles only if
 \bar{Q}_0 AND \bar{Q}_1
are "high"

This flip-flop
toggles only if
 \bar{Q}_0 AND \bar{Q}_1 AND \bar{Q}_2
are "high"

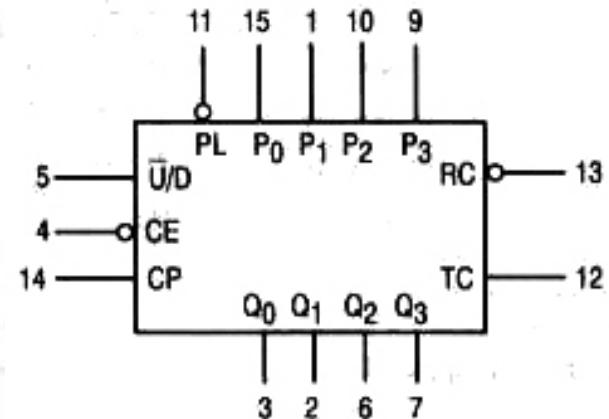
CIs comerciales 74190/74191

- 74190:
- 74191: **PRESETTABLE BCD/DECADE UP/DOWN COUNTERS**
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

The SN54/74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54/74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load (\overline{PL}) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable (CE) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U/D}$) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock (\overline{RC}) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multistage counter applications.

- Low Power . . . 90 mW Typical Dissipation
- High Speed . . . 25 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Individual Preset Inputs
- Count Enable and Up/Down Control Inputs
- Cascadable
- Input Clamp Diodes Limit High Speed Termination Effects



V_{CC} = PIN 16

GND = PIN 8

| | |
|------------------|--|
| CE | Count Enable (Active LOW) Input |
| CP | Clock Pulse (Active HIGH going edge) Input |
| $\overline{U/D}$ | Up/Down Count Control Input |
| PL | Parallel Load Control (Active LOW) Input |
| P_n | Parallel Data Inputs |
| Q_n | Flip-Flop Outputs (Note b) |
| RC | Ripple Clock Output (Note b) |
| TC | Terminal Count Output (Note b) |

CIIs comerciales 74190/74191

FUNCTIONAL DESCRIPTION

The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Data inputs (P_0 – P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state change are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U/D}$ input signal, as indicated in the Mode Select Table. When counting is to be enabled, the \overline{CE} signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH \overline{CE} transition must occur only while the clock is HIGH. Similarly, the $\overline{U/D}$ signal should only be changed when either \overline{CE} or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U/D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

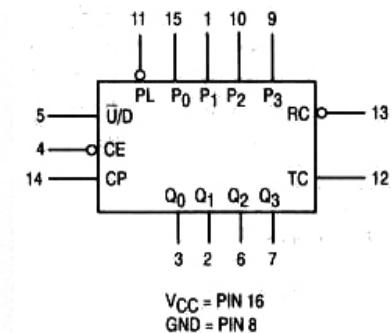
The TC signal is also used internally to enable the Ripple

Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, the \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the \overline{RC} outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The \overline{CE} input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

(permítido) CMOS 40190/40191



MODE SELECT TABLE

| INPUTS | | | | MODE |
|--------|----|------------------|----|------------------|
| PL | CE | $\overline{U/D}$ | CP | |
| H | L | L | ⊟ | Count Up |
| H | L | H | ⊟ | Count Down |
| L | X | X | X | Preset (Asyn.) |
| H | H | X | X | No Change (Hold) |

RC TRUTH TABLE

| INPUTS | | | RC OUTPUT |
|--------|-----|----|-----------|
| CE | TC* | CP | |
| L | H | ⊟ | ⊟ |
| H | X | X | H |
| X | L | X | H |

* TC is generated internally

L = LOW Voltage Level

H = HIGH Voltage Level

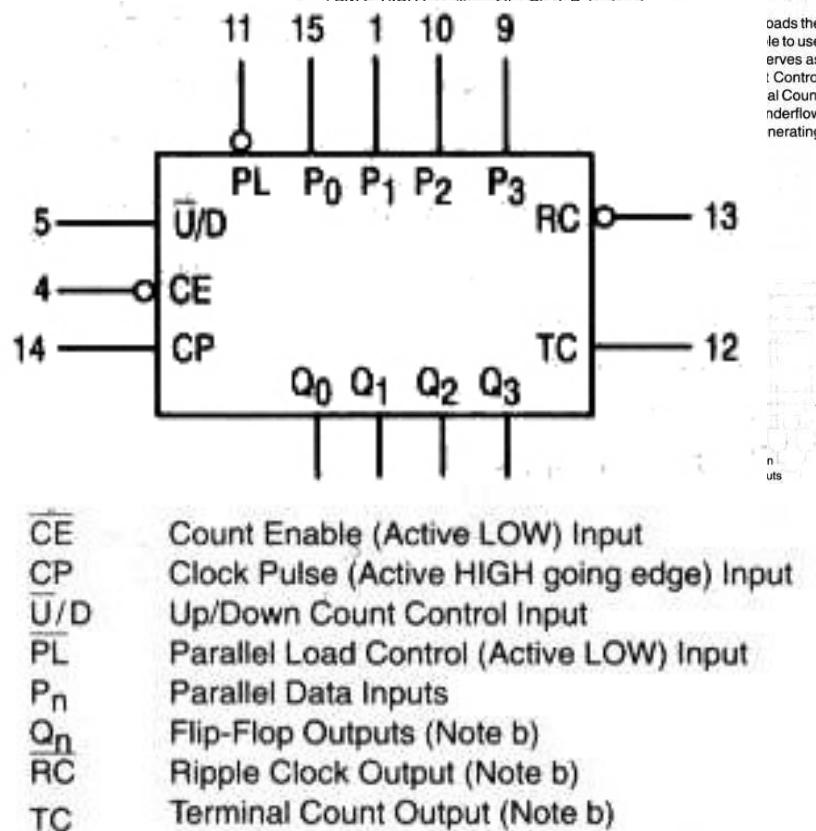
X = Don't Care

⊟ = LOW-to-HIGH Clock Transition

⊟ = LOW Pulse

CI's comerciales 74190/74191

- 74190: PRESETTABLE BCD/DECADE UP/DOWN COUNTERS
- 74191: PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS



RC Truth Table

| Inputs | | | Output |
|-----------------|--------|------|-----------------|
| \overline{CE} | TC^* | CP | \overline{RC} |
| L | H | ↑ | ↑ |
| H | X | X | H |
| X | L | X | H |

Mode Select Table

| Inputs | | | | Mode |
|-----------------|-----------------|------------------|------|------------------|
| \overline{PL} | \overline{CE} | $\overline{U/D}$ | CP | |
| H | L | L | ↑ | Count Up |
| H | L | H | ↑ | Count Down |
| L | X | X | X | Preset (Asyn.) |
| H | H | X | X | No Change (Hold) |

*TC is generated internally

H = HIGH Voltage Level

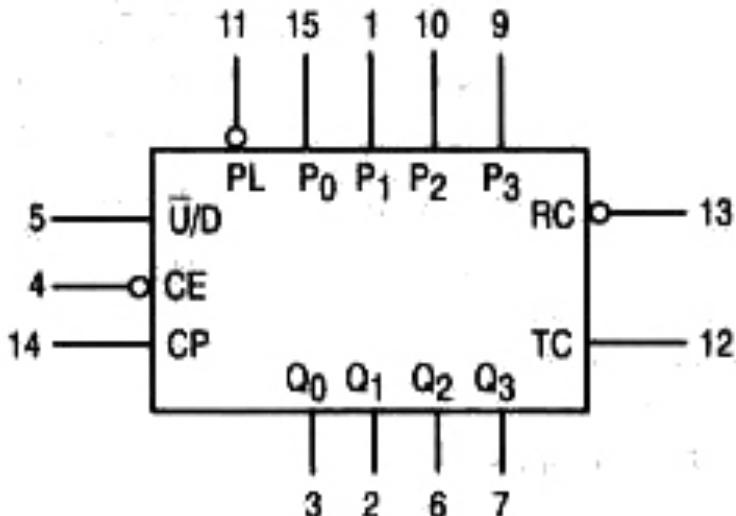
L = LOW Voltage Level

X = Immaterial

↑ = LOW-to-HIGH Clock Transition

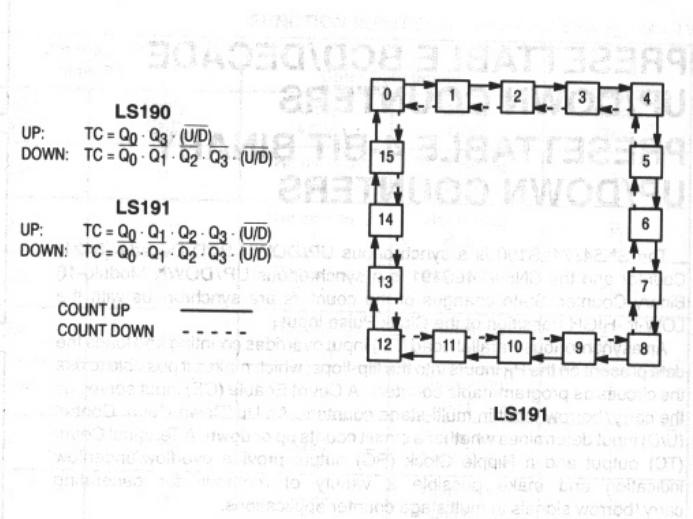
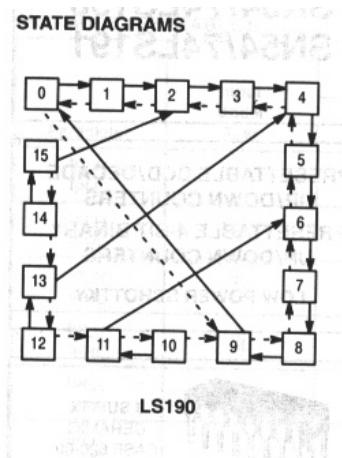
↑ = LOW Pulse

CI's comerciales 74190/74191

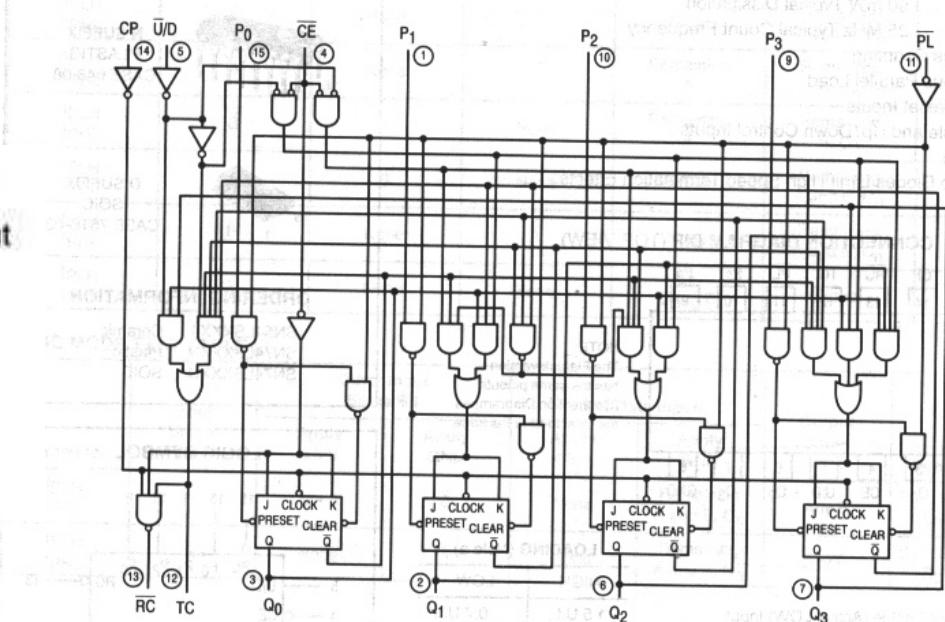


V_{CC} = PIN 16
GND = PIN 8

- CE** Count Enable (Active LOW) Input
- CP** Clock Pulse (Active HIGH going edge) Input
- U/D** Up/Down Count Control Input
- PL** Parallel Load Control (Active LOW) Input
- P_n** Parallel Data Inputs
- Q_n** Flip-Flop Outputs (Note b)
- RC** Ripple Clock Output (Note b)
- TC** Terminal Count Output (Note b)

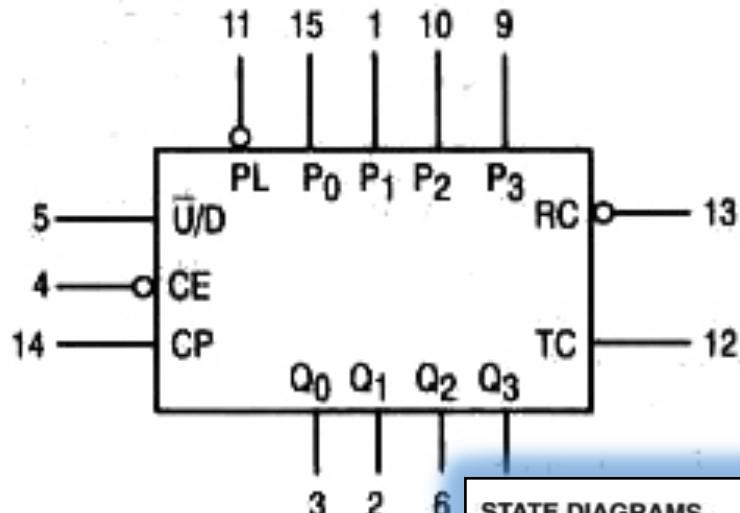


LOGIC DIAGRAMS



DECADE COUNTER
LS190

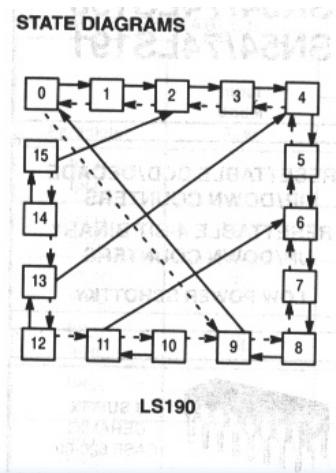
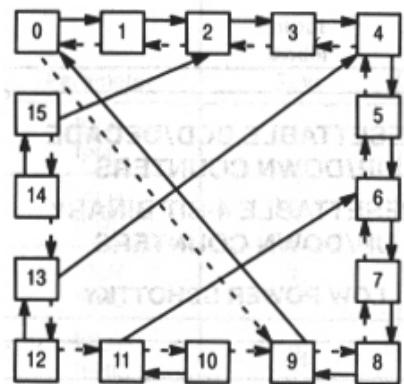
CI's comerciales 74190/74191



CE
CP
U/D
PL
 P_n
 Q_n
RC
TC

Count Enable (Active Low)
Clock Pulse (Active High)
Up/Down Count Control
Parallel Load Control
Parallel Data Inputs
Flip-Flop Outputs (No Latch)
Ripple Clock Output
Terminal Count Output

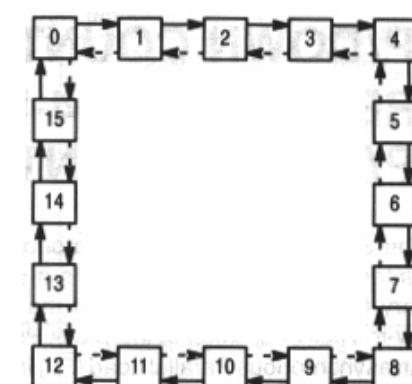
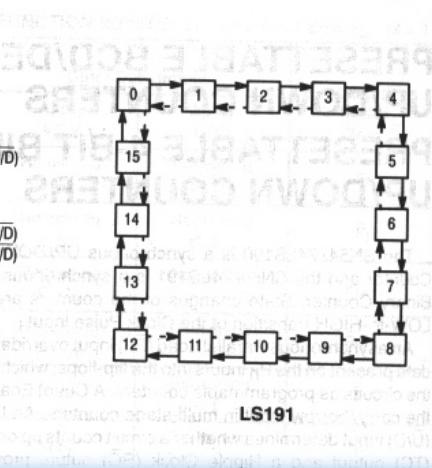
STATE DIAGRAMS



LS190
UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{U/D})$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$

LS191
UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$

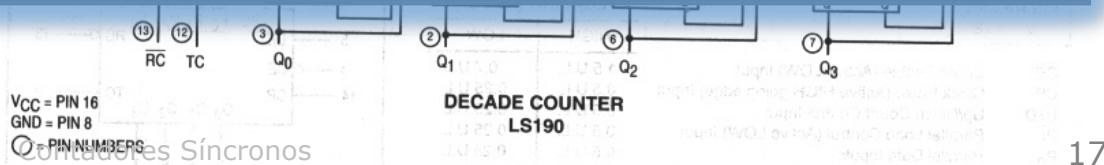
COUNT UP
COUNTER DOWN



LS190
UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{U/D})$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$

LS191
UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$

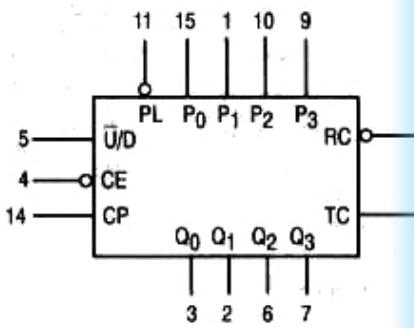
COUNT UP
COUNTER DOWN



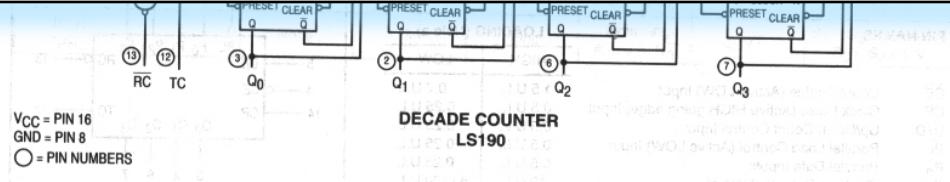
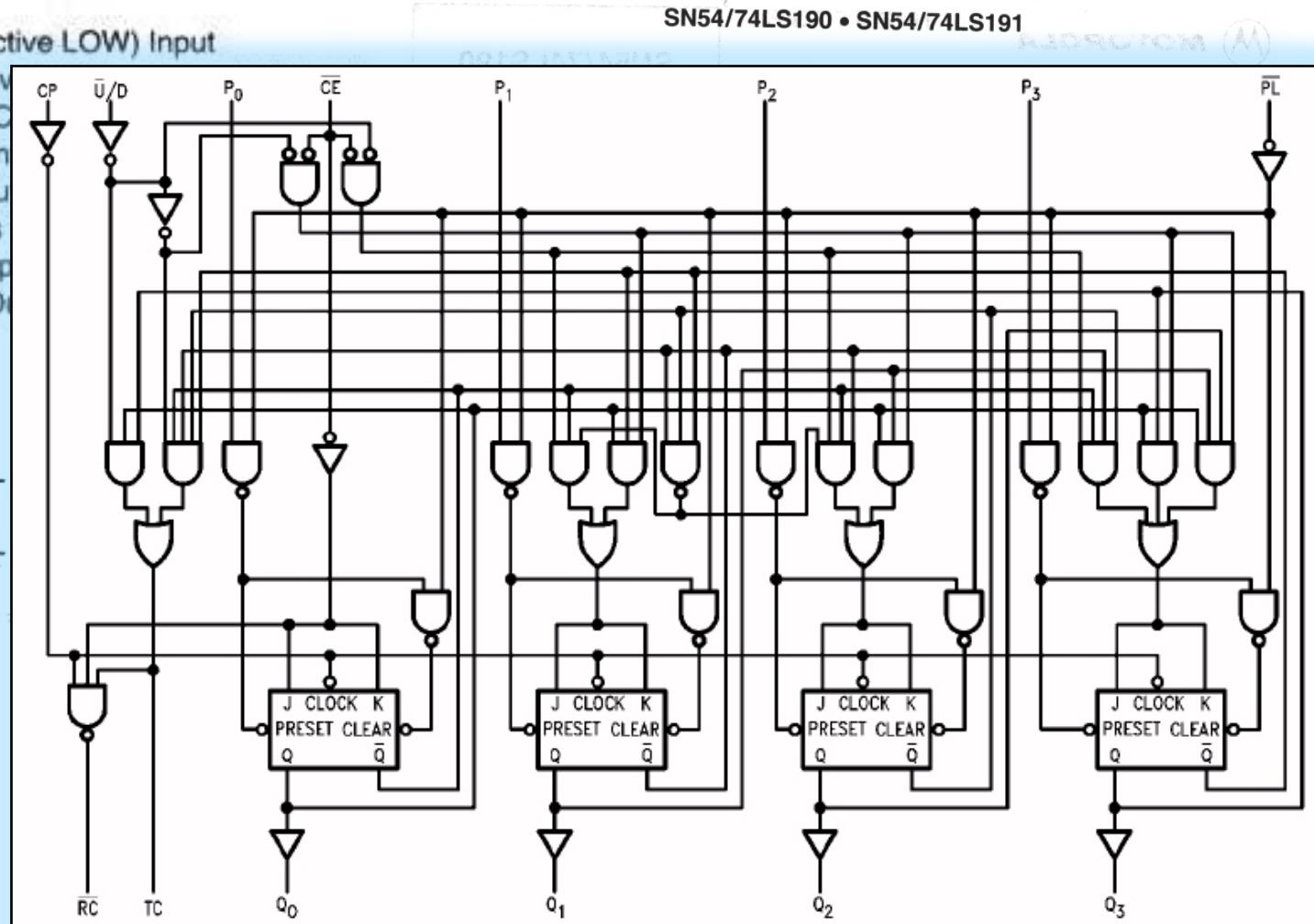
CIIs comerciales 74190/74191

CE
 CP
 U/D
 PL
 P_n
 Q_n
 RC
 TC

Count Enable (Active LOW) Input



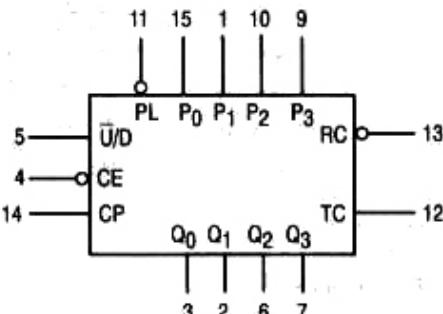
V_{CC} = PIN 16
GND = PIN 8



CIIs comerciales 74190/74191

CE
CP
U/D
PL
P_n
Q_n
RC
TC

Count Enable (Active LOW) Input
Clock Pulse (Active HIGH going edge) Input
Up/Down Count Control Input
Parallel Load Control (Active LOW) Input
Parallel Data Inputs
Flip-Flop Outputs (Note b)
Ripple Clock Output (Note b)
Terminal Count Output (Note b)



AC CHARACTERISTICS ($T_A = 25^\circ C$)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|--------------------------------------|--------------------------------------|--------|----------|----------|------|-----------------|
| | | Min | Typ | Max | | |
| t _{MAX} | Maximum Clock Frequency | 20 | 25 | | MHz | |
| t _{PLH} t _{PHL} | Propagation Delay, PL to Output Q | | 22 33 | 33 50 | ns | |
| t _{PLH} t _{PHL} | Data to Output Q | | 20 27 | 32 40 | ns | |
| t _{PLH} t _{PHL} | Clock to \overline{RC} | | 13 16 | 20 24 | ns | |
| t _{PLH} t _{PHL} | Clock to Output Q | | 16 24 | 24 36 | ns | |
| t _{PLH} t _{PHL} | Clock to TC | | 28 37 | 42 52 | ns | |
| t _{PLH} t _{PHL} | U/D to \overline{RC} | | 30 30 | 45 45 | ns | |
| t _{PLH} t _{PHL} | U/D to TC | | 21 22 | 33 33 | ns | |
| t _{PLH} t _{PHL} | CE to \overline{RC} | | 21 22 | 33 33 | ns | |

AC SETUP REQUIREMENTS ($T_A = 25^\circ C$)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|------------------|-----------------|--------|-----|-----|------|-----------------|
| | | Min | Typ | Max | | |
| t _W | CP Pulse Width | 25 | | | ns | |
| t _W | PL Pulse Width | 35 | | | ns | |
| t _S | Data Setup Time | 20 | | | ns | |
| t _H | Data Hold Time | 5.0 | | | ns | |
| t _{rec} | Recovery Time | 40 | | | ns | |

DEFINITIONS OF TERMS

SETUP TIME (t_S) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

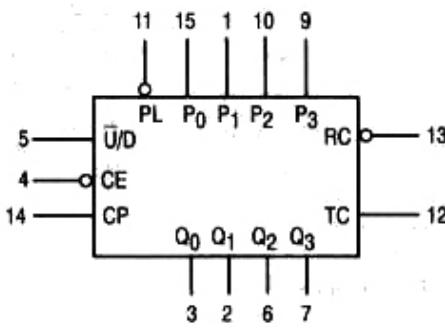
HOLD TIME (t_H) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition.

A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

CIs comerciales 74190/74191

| | |
|-----------------|--|
| \overline{CE} | Count Enable (Active LOW) Input |
| \overline{CP} | Clock Pulse (Active HIGH going edge) Input |
| U/D | Up/Down Count Control Input |
| PL | Parallel Load Control (Active LOW) Input |
| P_n | Parallel Data Inputs |
| Q_n | Flip-Flop Outputs (Note b) |
| RC | Ripple Clock Output (Note b) |
| TC | Terminal Count Output (Note b) |



SN54/74LS190 • SN54/74LS191

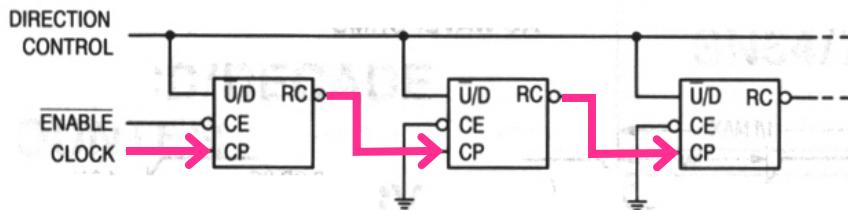


Figure a. n-Stage Counter Using Ripple Clock

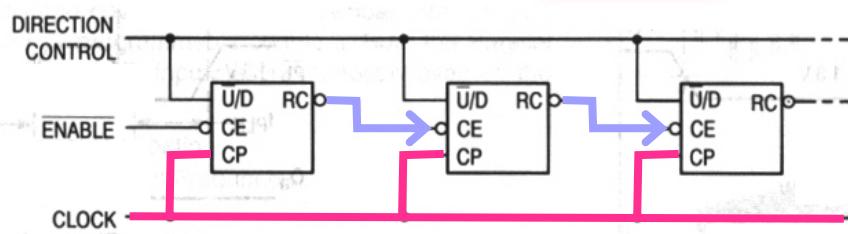


Figure b. Synchronous n-Stage Counter Using Ripple Carry/Borrow

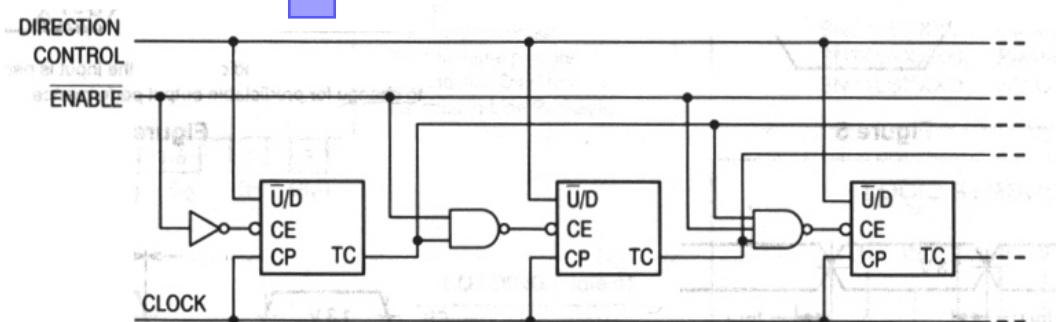
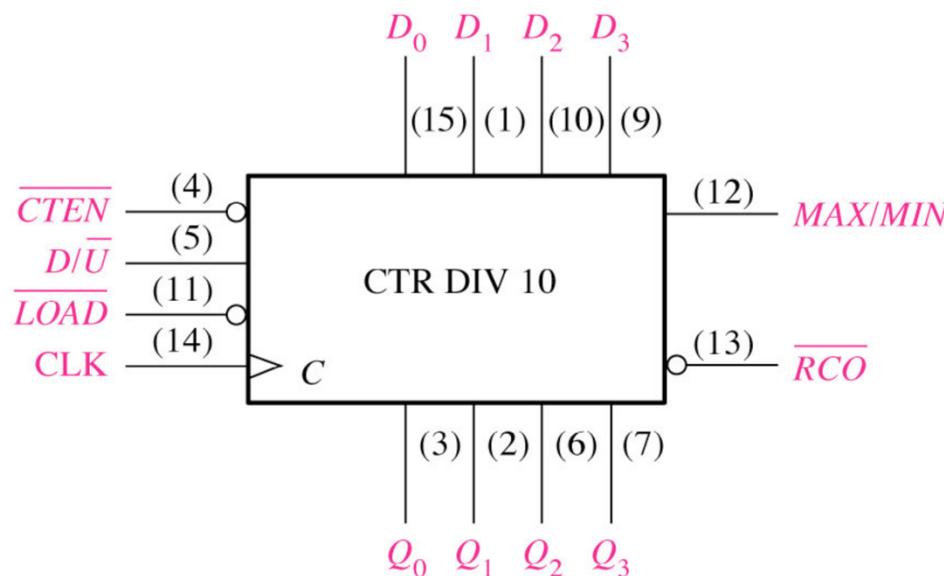


Figure c. Synchronous n-Stage Counter with Parallel Gated Carry/Borrow

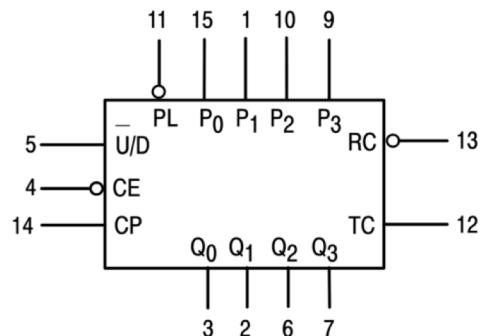
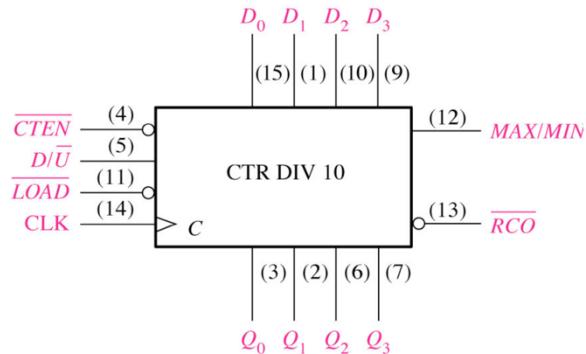
Pastilha comercial 74190:

- Contador síncrono decimal up/down: 74HC190



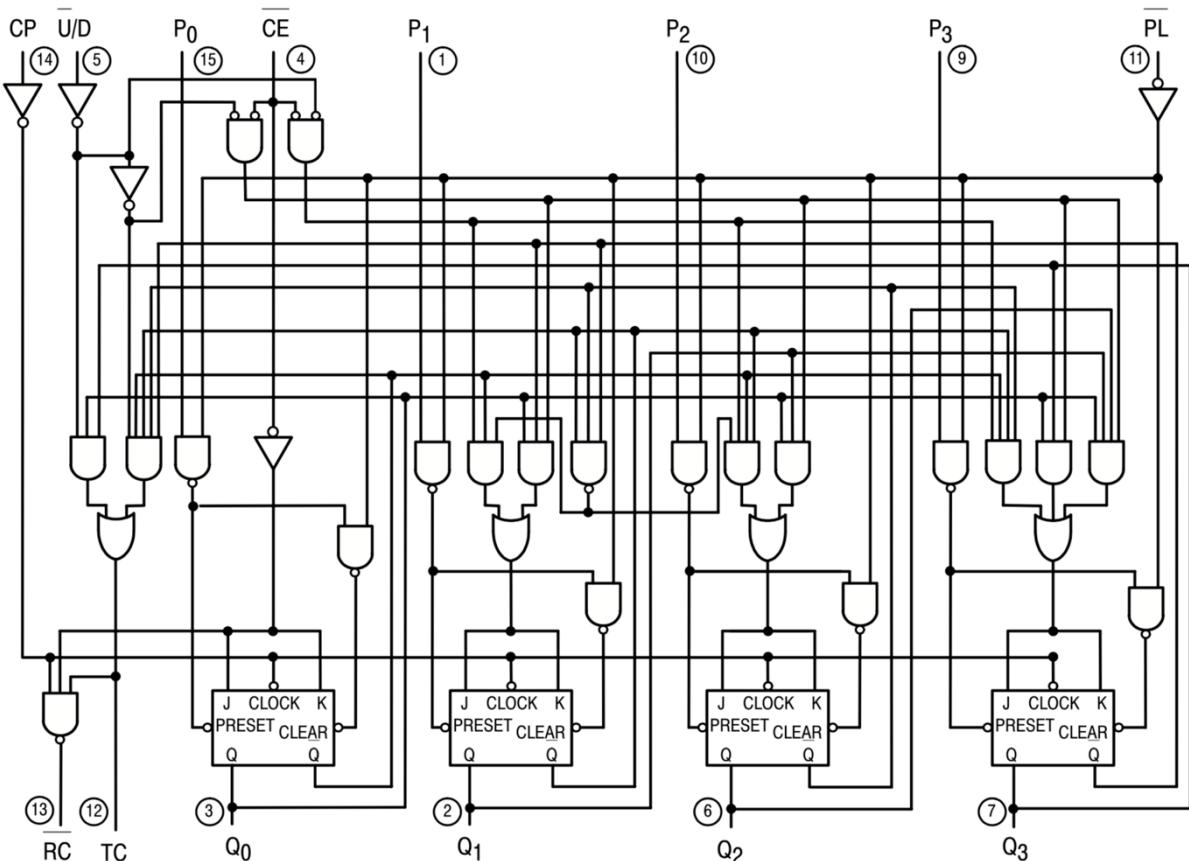
Pastilha comercial 74190:

LOGIC DIAGRAMS



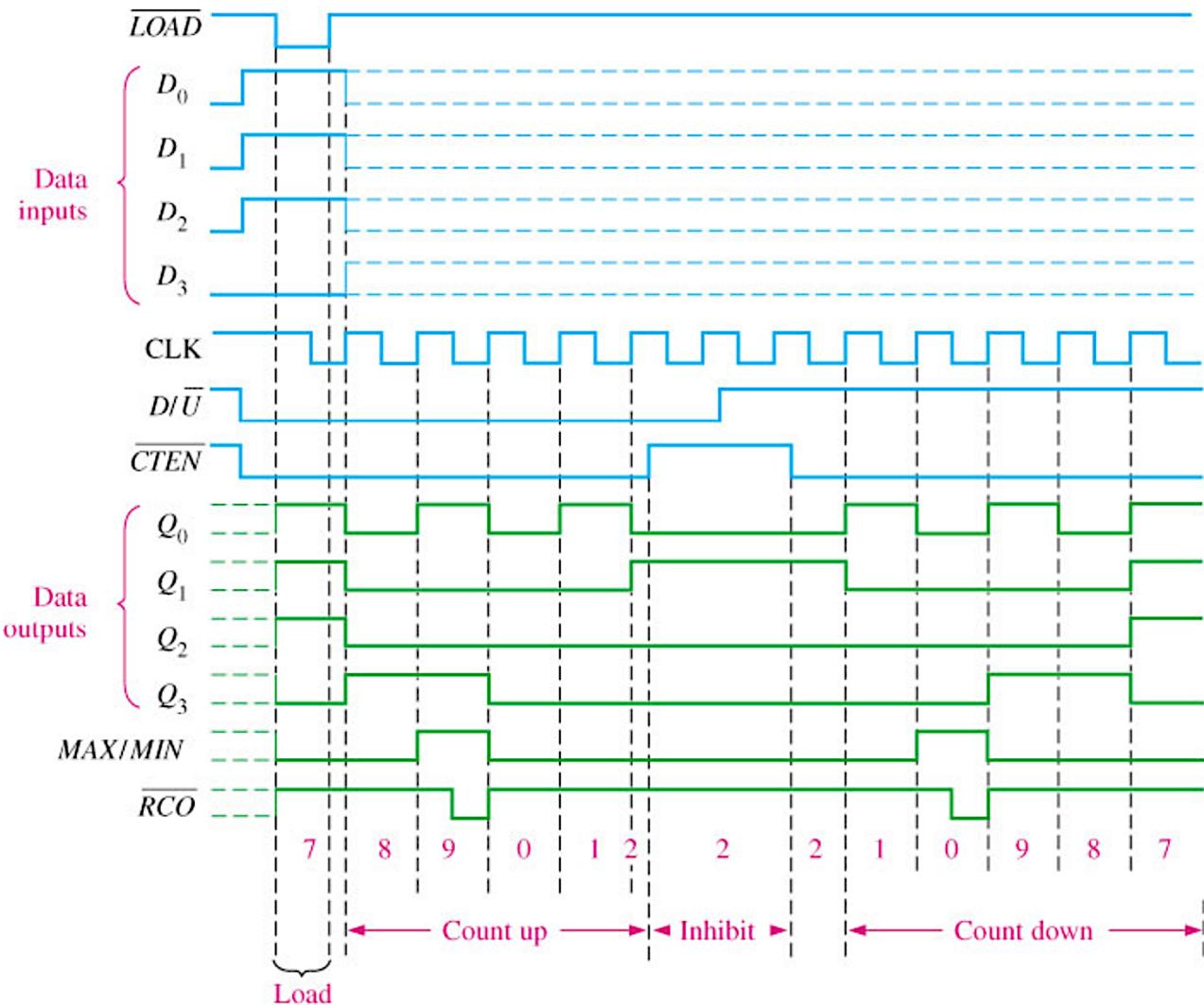
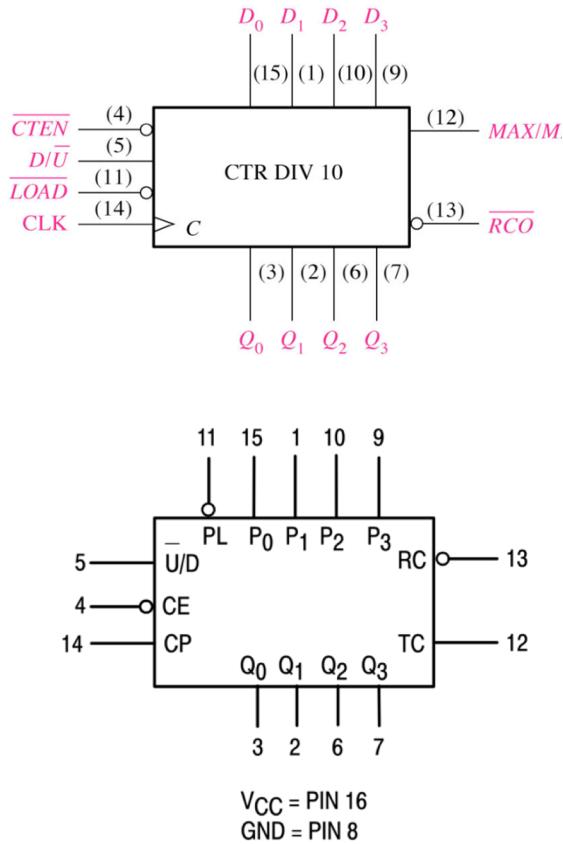
$V_{CC} = \text{PIN } 16$
 $GND = \text{PIN } 8$

$\bigcirc = \text{PIN NUMBERS}$



DECADE COUNTER
LS190

Pastilha comercial 74190:



Pastilha comercial 74190:

Cascadeamentos:

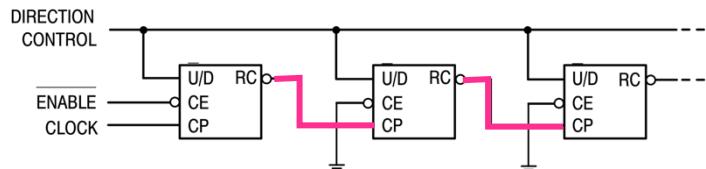


Figure a. n-Stage Counter Using Ripple Clock

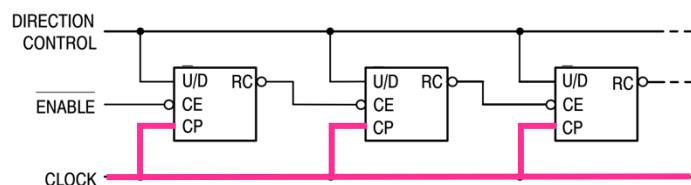


Figure b. Synchronous n-Stage Counter Using Ripple Carry/Borrow

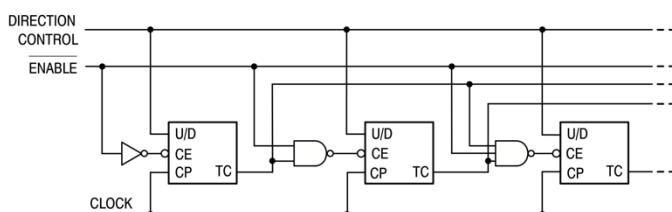
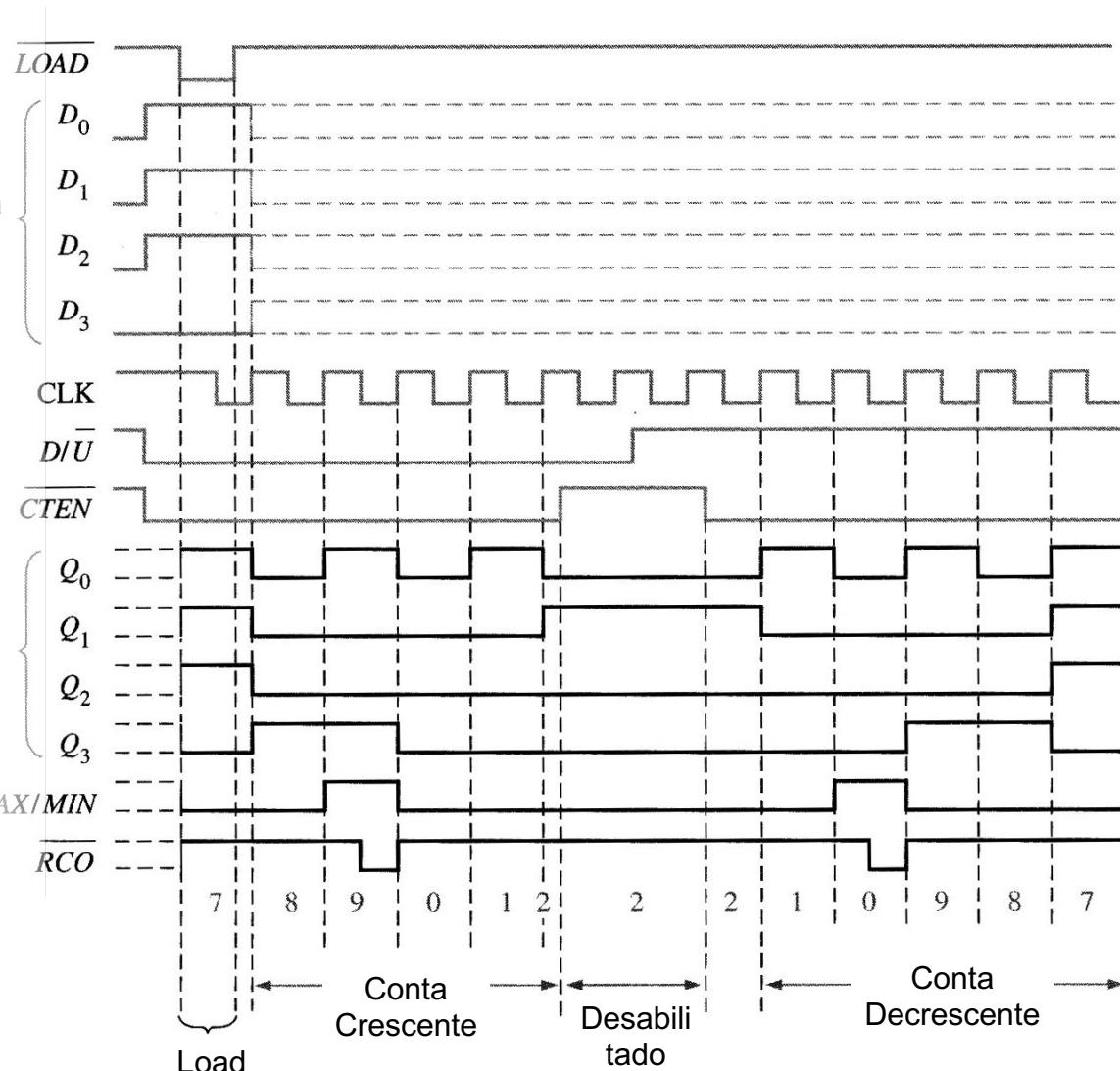


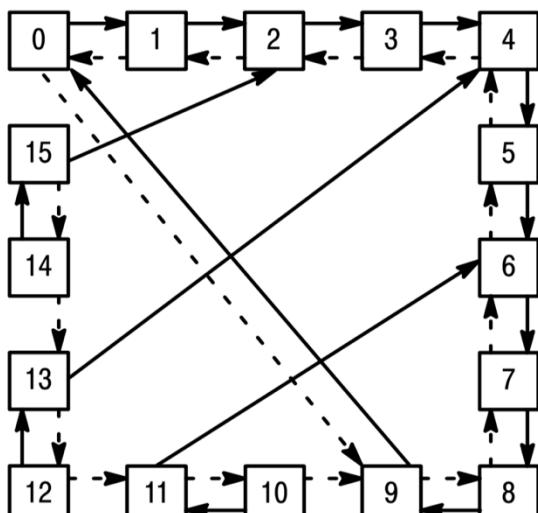
Figure c. Synchronous n-Stage Counter with Parallel Gated Carry/Borrow



Pastilhas comerciais:

- “Família 74LS190/74LS191
 - 74LS190: Presettable BCD/Decade Up/Down Counter;
 - 74LS191: Presettable 4-bit binary Up/Down Counter.

STATE DIAGRAMS



LS190

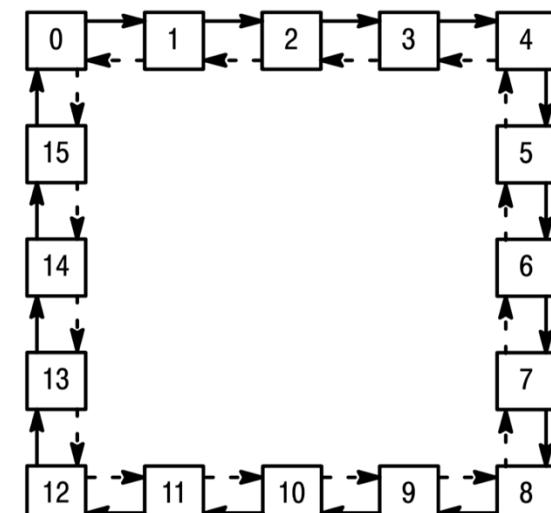
LS190

UP: $TC = Q_0 \cdot Q_3 \cdot \overline{(U/D)}$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

LS191

UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{(U/D)}$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

COUNT UP —————
COUNT DOWN - - - - -



LS191

Pastilhas 74192/74193:



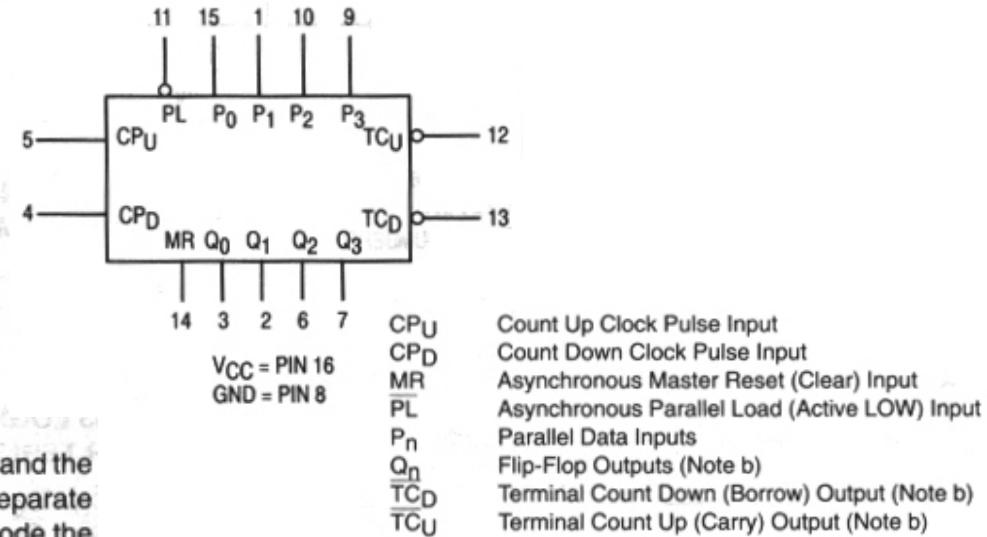
PRESETTABLE BCD/DECADE UP/DOWN COUNTER

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

The SN54/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High Speed Termination Effects



NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive

MODE SELECT TABLE

| MR | PL | CP _U | CP _D | MODE |
|----|----|-----------------|-----------------|----------------|
| H | X | X | X | Reset (Asyn.) |
| L | L | X | X | Preset (Asyn.) |
| L | H | H | H | No Change |
| L | H | ⊓ | H | Count Up |
| L | H | H | ⊓ | Count Down |

L = LOW Voltage Level

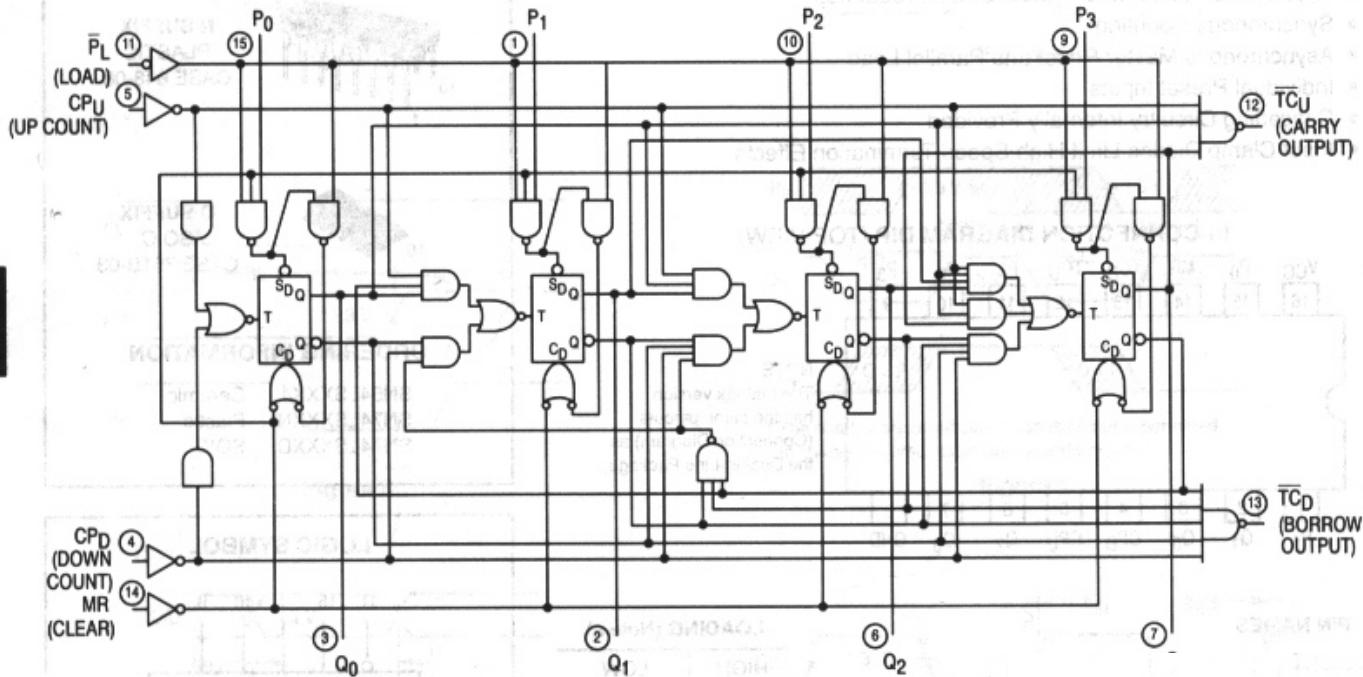
H = HIGH Voltage Level

X = Don't Care

⊓ = LOW-to-HIGH Clock Transition

Pastilhas 74192/74193:

LOGIC DIAGRAMS



VCC = PIN 16

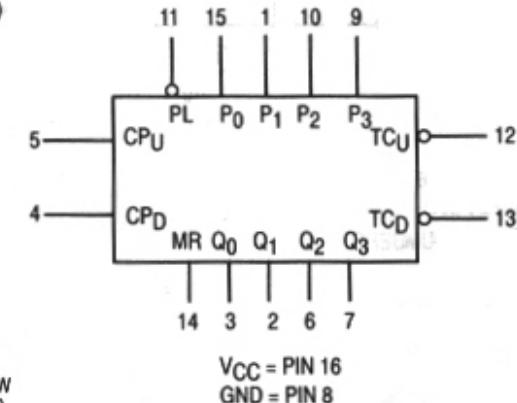
GND = PIN 8

○ = PIN NUMBERS

| | |
|----------------|---|
| CPU | Count Up Clock Pulse Input |
| CPD | Count Down Clock Pulse Input |
| MR | Asynchronous Master Reset (Clear) Input |
| PL | Asynchronous Parallel Load (Active LOW) Input |
| P _n | Parallel Data Inputs |
| Q _n | Flip-Flop Outputs (Note b) |
| TCD | Terminal Count Down (Borrow) Output (Note b) |
| TCU | Terminal Count Up (Carry) Output (Note b) |

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive



MODE SELECT TABLE

| MR | PL | CPU | CPD | MODE |
|----|----|-----|-----|----------------|
| H | X | X | X | Reset (Asyn.) |
| L | L | X | X | Preset (Asyn.) |
| L | H | H | H | No Change |
| L | H | ⊟ | H | Count Up |
| L | H | H | ⊟ | Count Down |

L = LOW Voltage Level

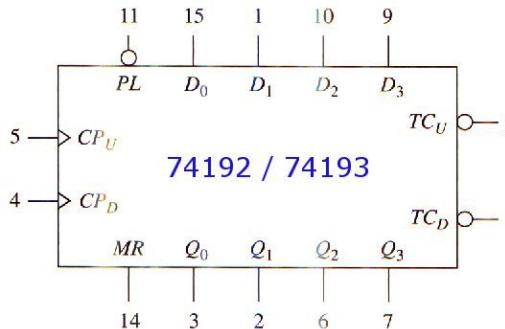
H = HIGH Voltage Level

X = Don't Care

⊟ = LOW-to-HIGH Clock Transition

Pastilhas comerciais:

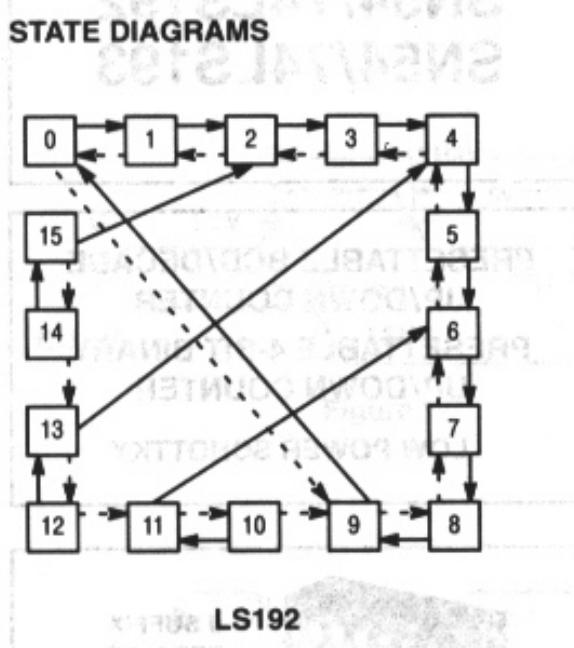
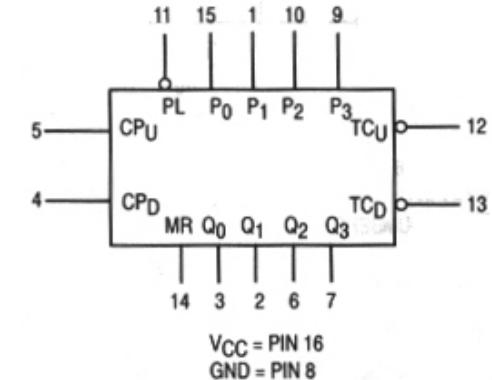
- Contador síncrono up/down: 74HC192/74HC193



| | |
|-----------------|---|
| CP _U | Count Up Clock Pulse Input |
| CP _D | Count Down Clock Pulse Input |
| MR | Asynchronous Master Reset (Clear) Input |
| PL | Asynchronous Parallel Load (Active LOW) Input |
| P _n | Parallel Data Inputs |
| Q _n | Flip-Flop Outputs (Note b) |
| TCD | Terminal Count Down (Borrow) Output (Note b) |
| TCU | Terminal Count Up (Carry) Output (Note b) |

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b. The Output LOW drive



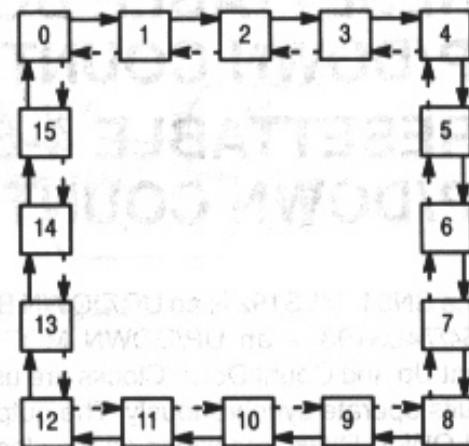
**LS192 LOGIC EQUATIONS
FOR TERMINAL COUNT**

$$\begin{aligned} \overline{\text{TC}}_{\text{U}} &= \overline{Q}_0 \cdot \overline{Q}_3 \cdot \overline{\text{CP}}_{\text{U}} \\ \overline{\text{TC}}_{\text{D}} &= \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{\text{CP}}_{\text{D}} \end{aligned}$$

**LS193 LOGIC EQUATIONS
FOR TERMINAL COUNT**

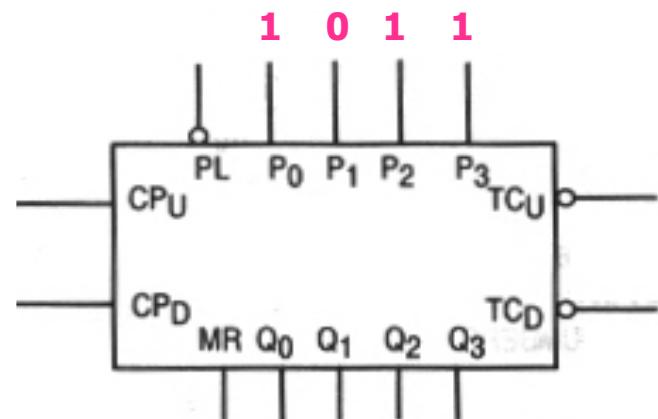
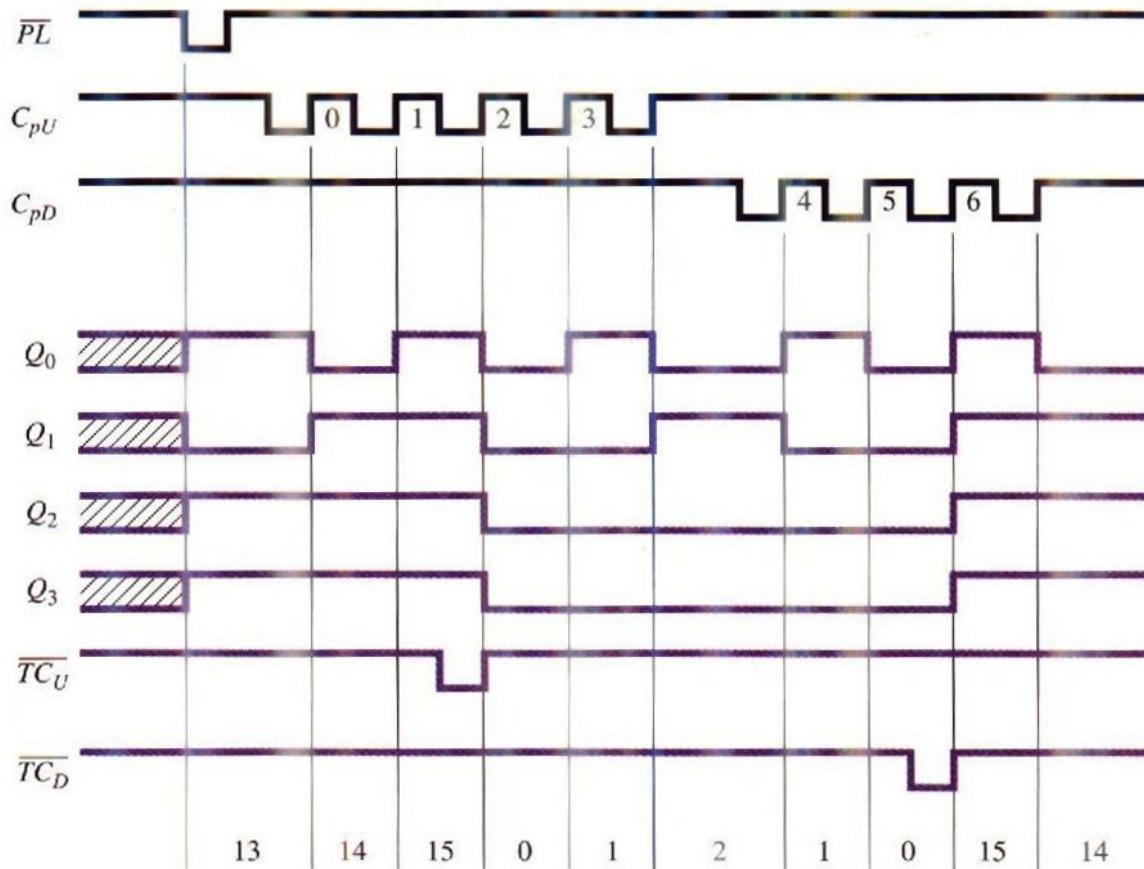
$$\begin{aligned} \overline{\text{TC}}_{\text{U}} &= \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{\text{CP}}_{\text{U}} \\ \overline{\text{TC}}_{\text{D}} &= \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{\text{CP}}_{\text{D}} \end{aligned}$$

COUNT UP
COUNT DOWN



Usando o CI 74193:

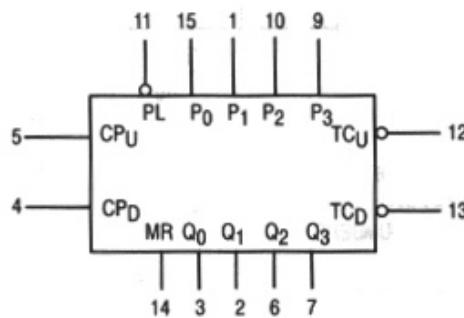
Complete as formas de onda nas saídas das saídas do 74193:



Usando o CI 74192:

Que acontece quando ?

- 1) Resseto todas as suas saídas;
- 2) Realizo carga paralela com $7(10)=0111(2)$;
- 3) Ajusto para contar crescente +5 pulsos de Clock;
- 4) Ajusto para contar decrescente + 5 pulsos de Clock.

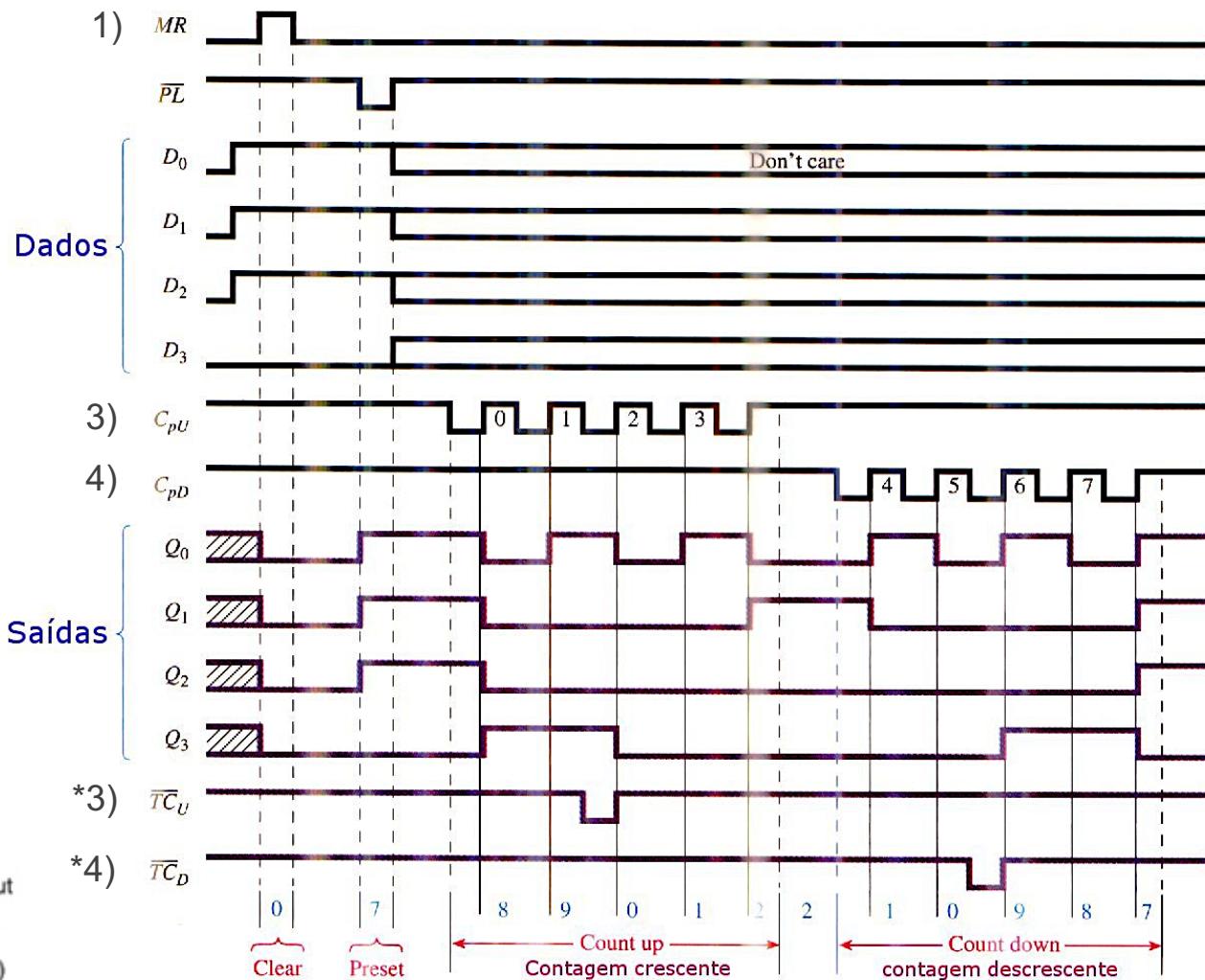


| | |
|----------------|---|
| CPU | Count Up Clock Pulse Input |
| CPD | Count Down Clock Pulse Input |
| MR | Asynchronous Master Reset (Clear) Input |
| PL | Asynchronous Parallel Load (Active LOW) Input |
| P _n | Parallel Data Inputs |
| Q _n | Flip-Flop Outputs (Note b) |
| TCD | Terminal Count Down (Borrow) Output (Note b) |
| TCU | Terminal Count Up (Carry) Output (Note b) |

NOTES:

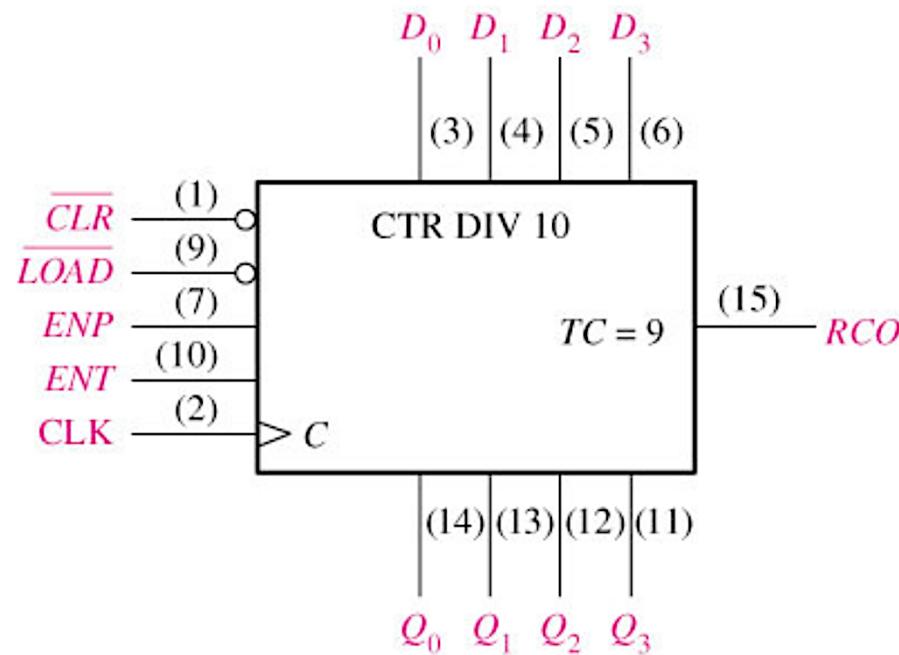
a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b. The Output LOW drive



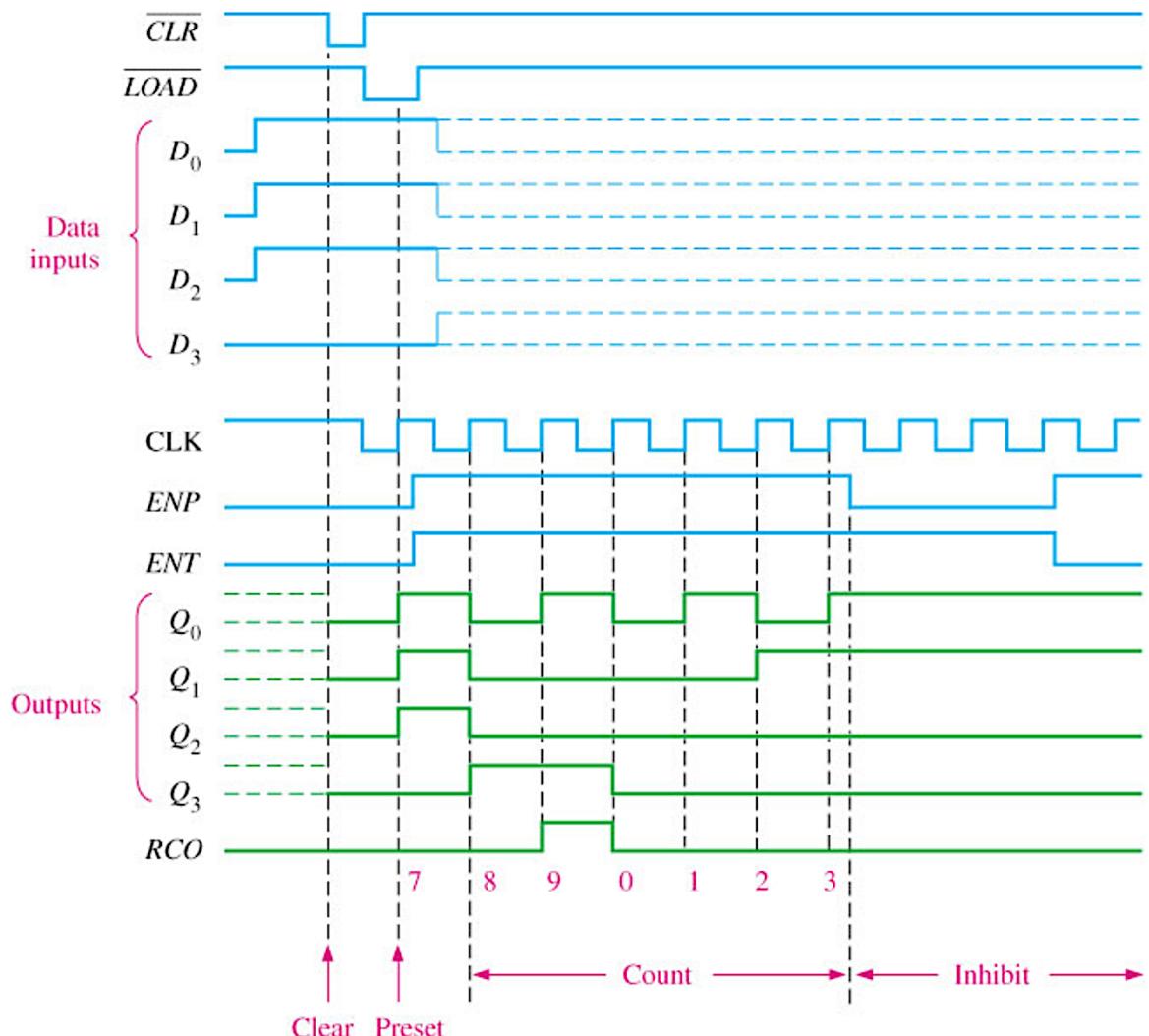
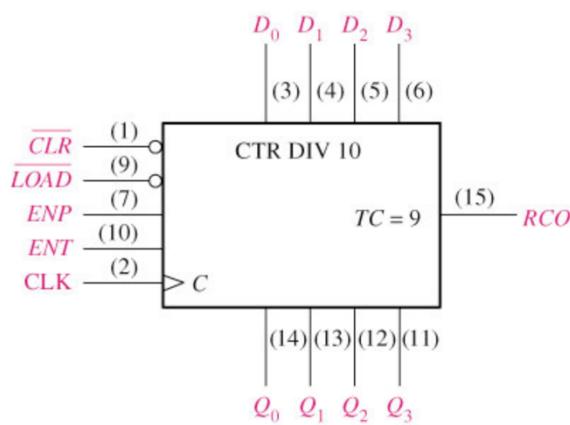
Pastilhas comerciais:

- Contador síncrono decimal up/down: 74HC160



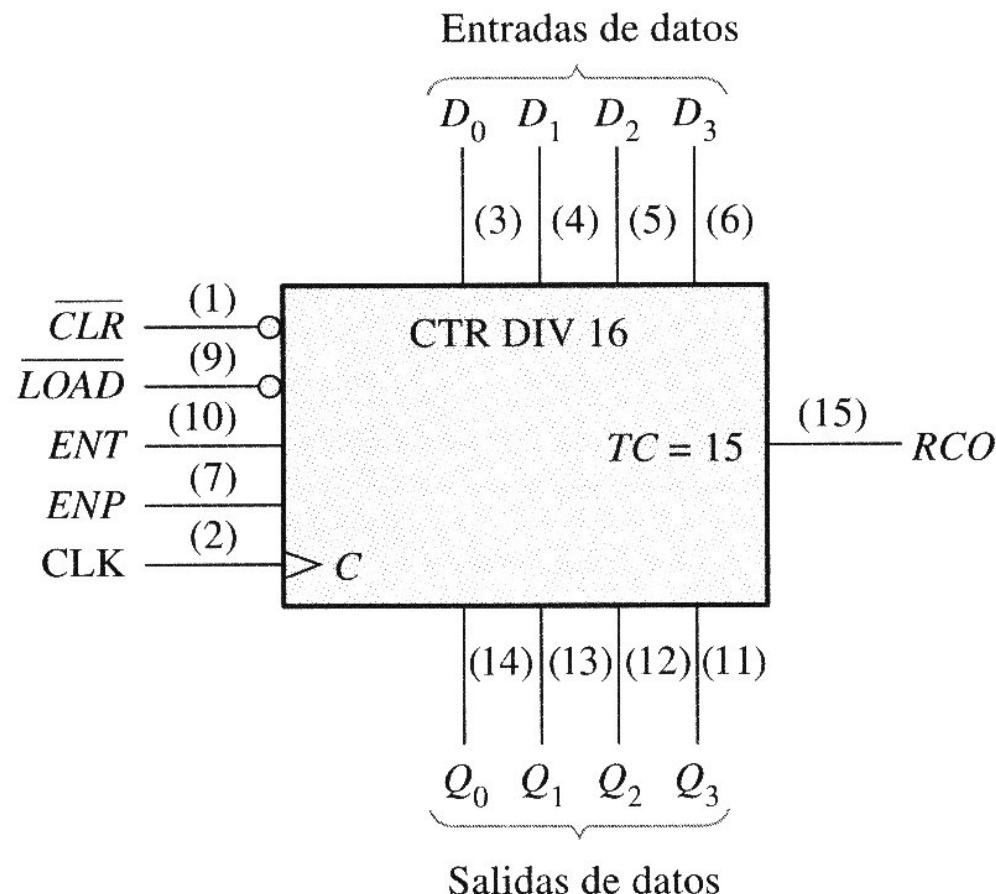
Pastilhas comerciais:

- Contador síncrono decimal up/down: 74HC160



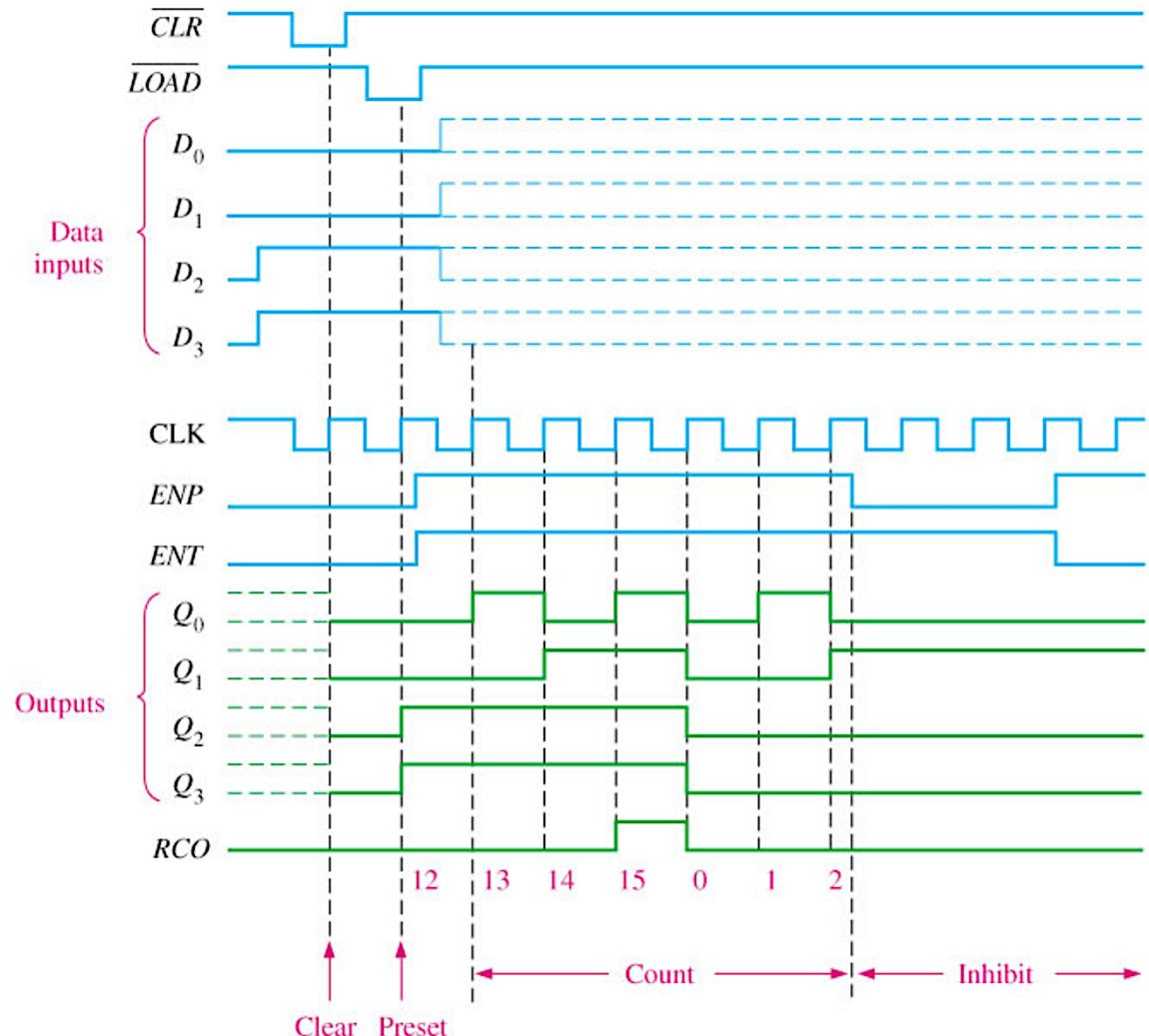
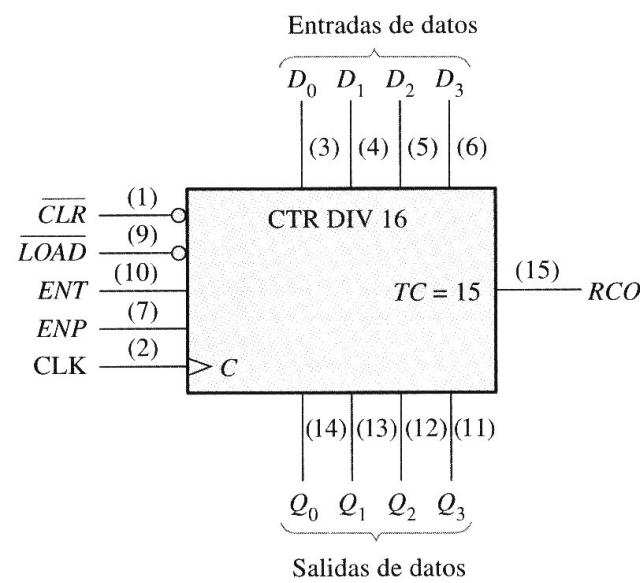
Pastilhas comerciais:

- Contador síncrono binário up/down: 74HC163



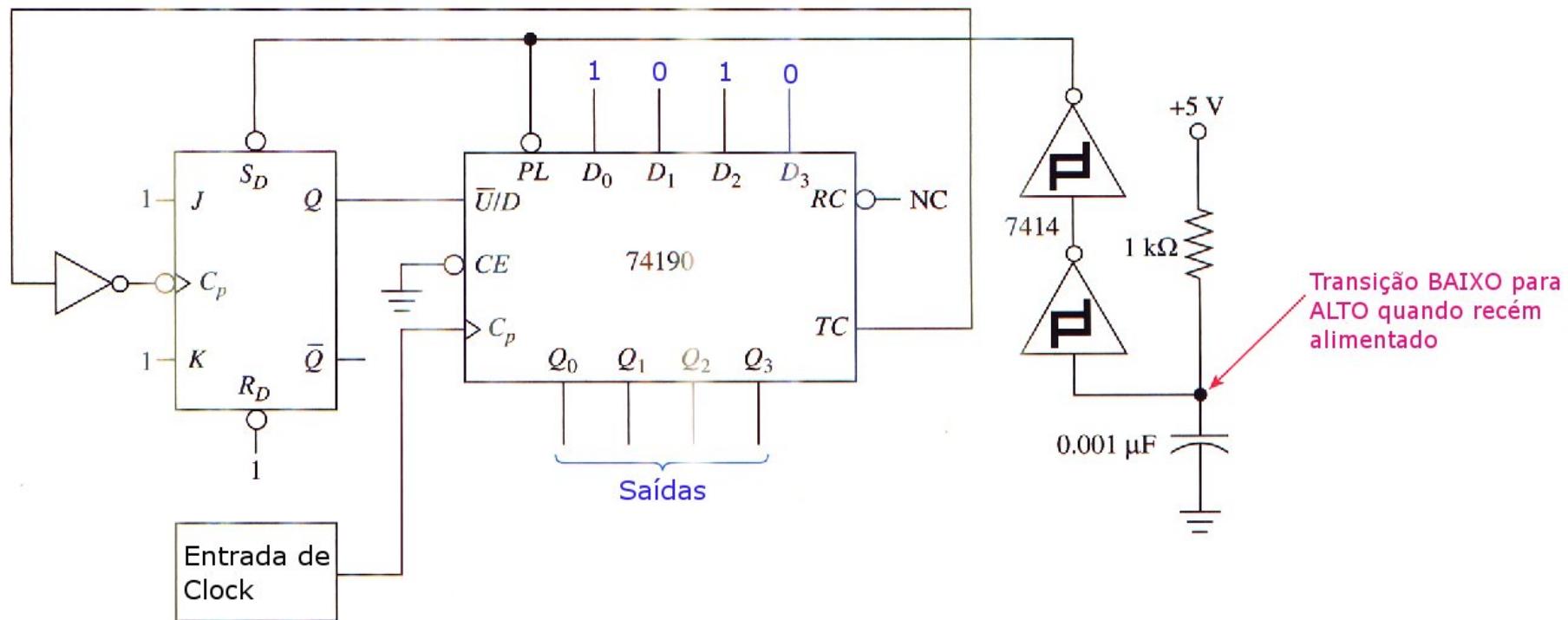
Pastilhas comerciais:

- Contador síncrono binário up/down: 74HC163

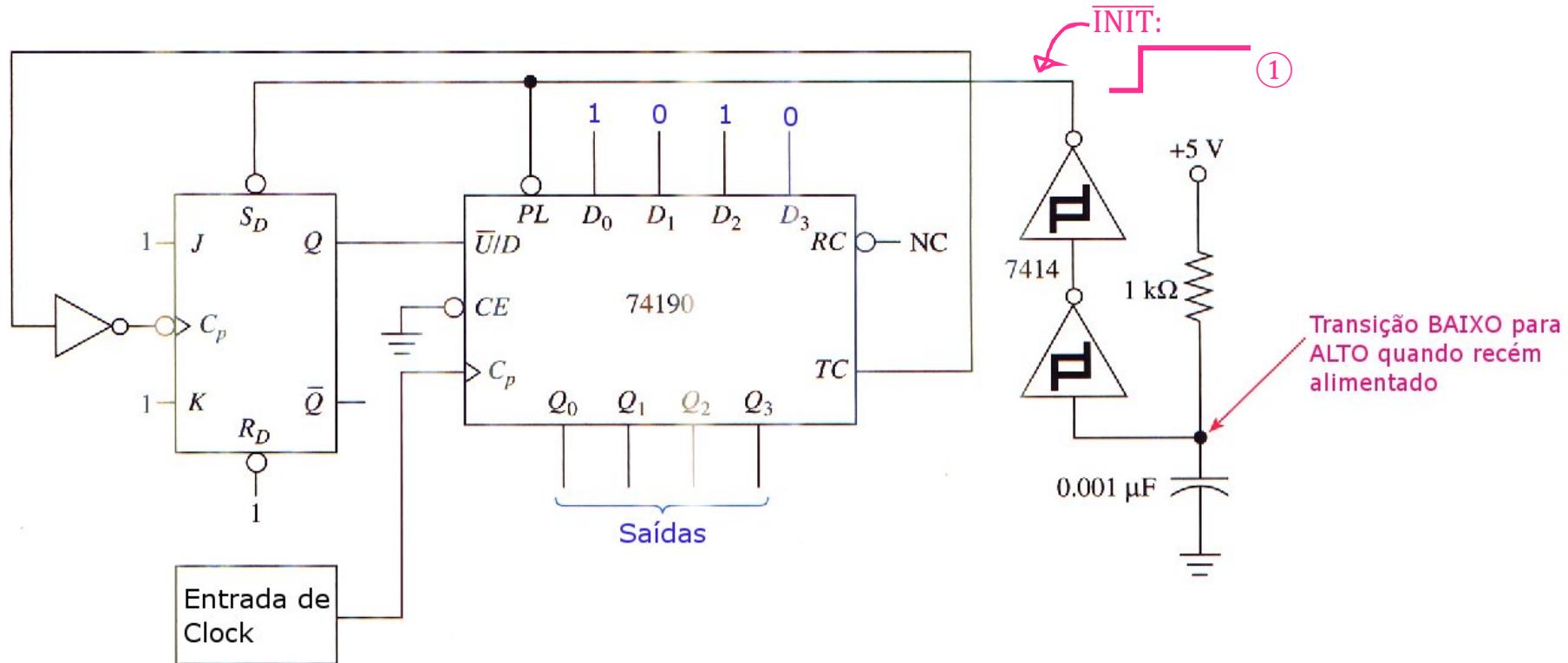


Problema

O que faz o circuito abaixo?



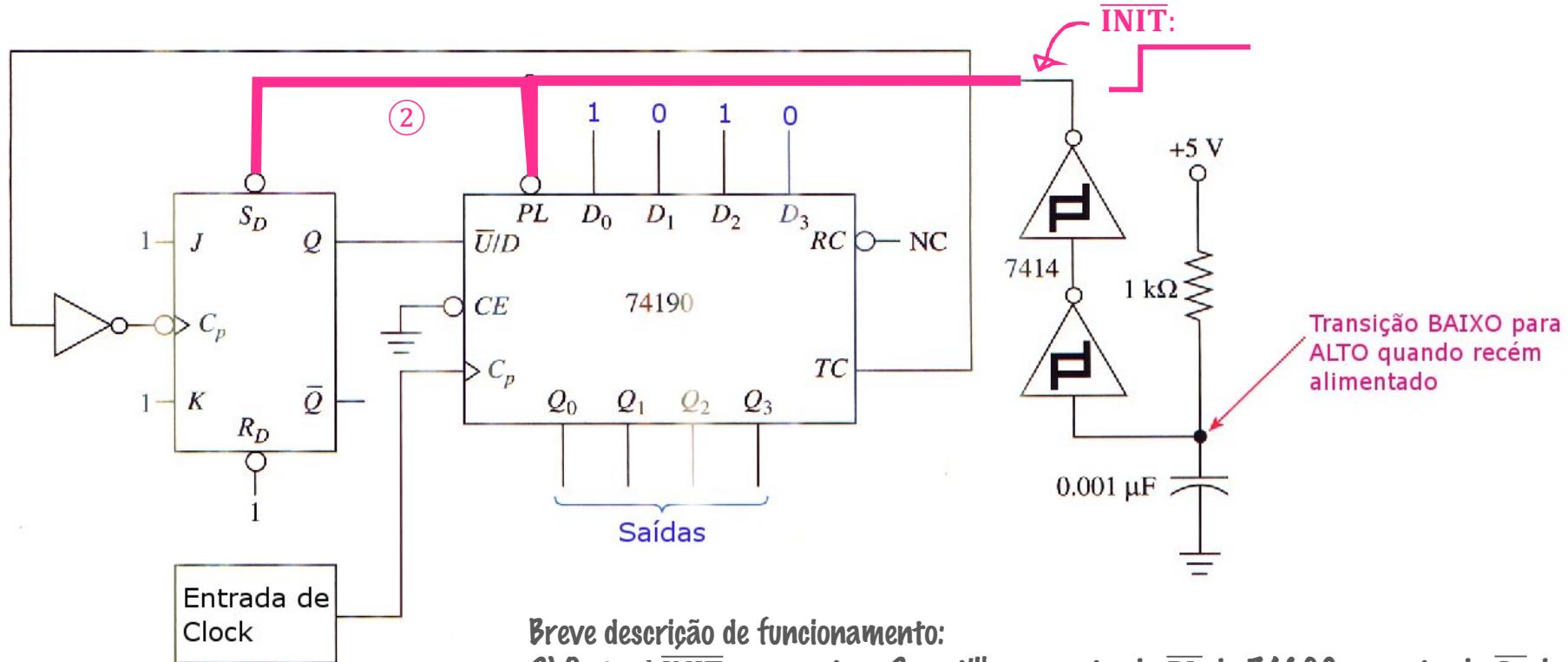
Problema



Breve descrição de funcionamento:

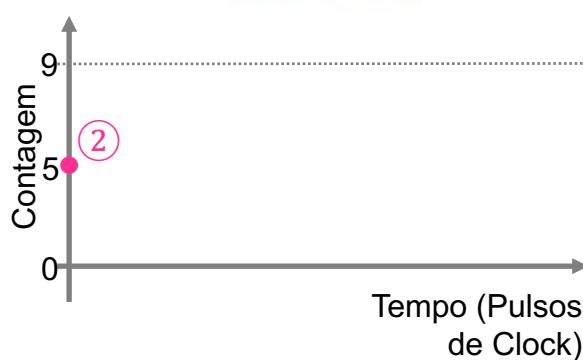
- 1) O circuito formado pelo Resistor e Capacitor gera um pulso que inicia e continua em nível lógico baixo na saída das portas Schmidt trigger enquanto o capacitor carrega. Chamaremos a este pulso de $\overline{\text{INIT}}$. Notar que capacitor carrega rápido, então o sinal $\overline{\text{INIT}}$ é curto. Uma vez carregado, $\overline{\text{INIT}}$ permanece em nível lógico alto.

Problema

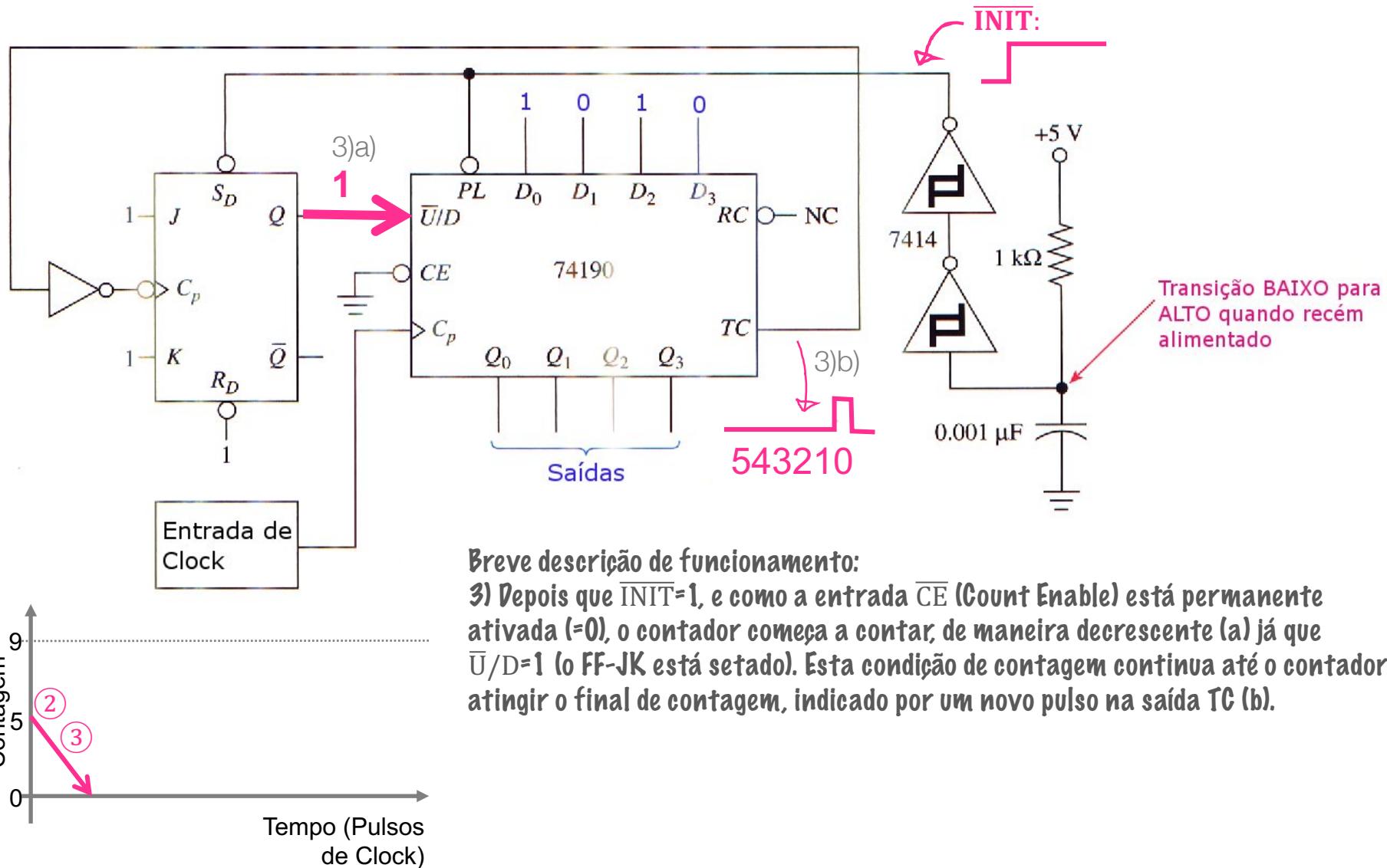


Breve descrição de funcionamento:

2) O sinal $\overline{\text{INIT}}$ se conecta a 2 pastilhas: a entrada $\overline{\text{PL}}$ do 74190 e a entrada $\overline{S_d}$ do FF-JK. Ambas são assíncronas (não dependem do sinal do clock). Isto força respectivamente o “Parallel Load” do contador com o número $D_3D_2D_1D_0 = 0101_{(2)} = 5_{(10)}$ e o “Set” do FF-JK. Desta forma, isto garante que o contador inicie a contagem no número 5. Note que saída do FF-JK controla o sentido de contagem do contador. Como neste caso o FF é setado, $Q=1$, a entrada $\overline{U/D}=1$, forçando o contado num contagem descendente (Down), tão logo o pulso $\overline{\text{INIT}}$ cesse.



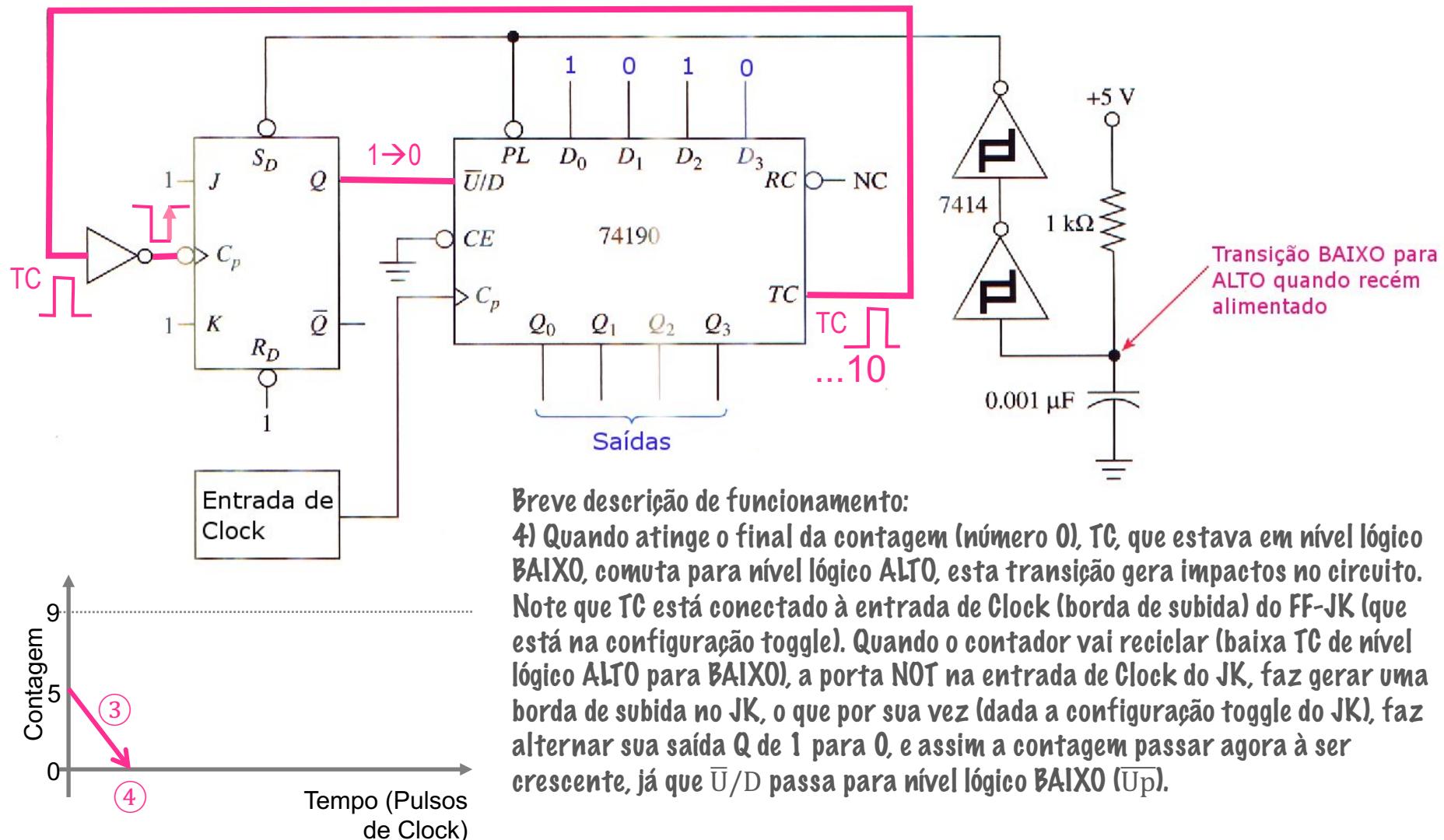
Problema



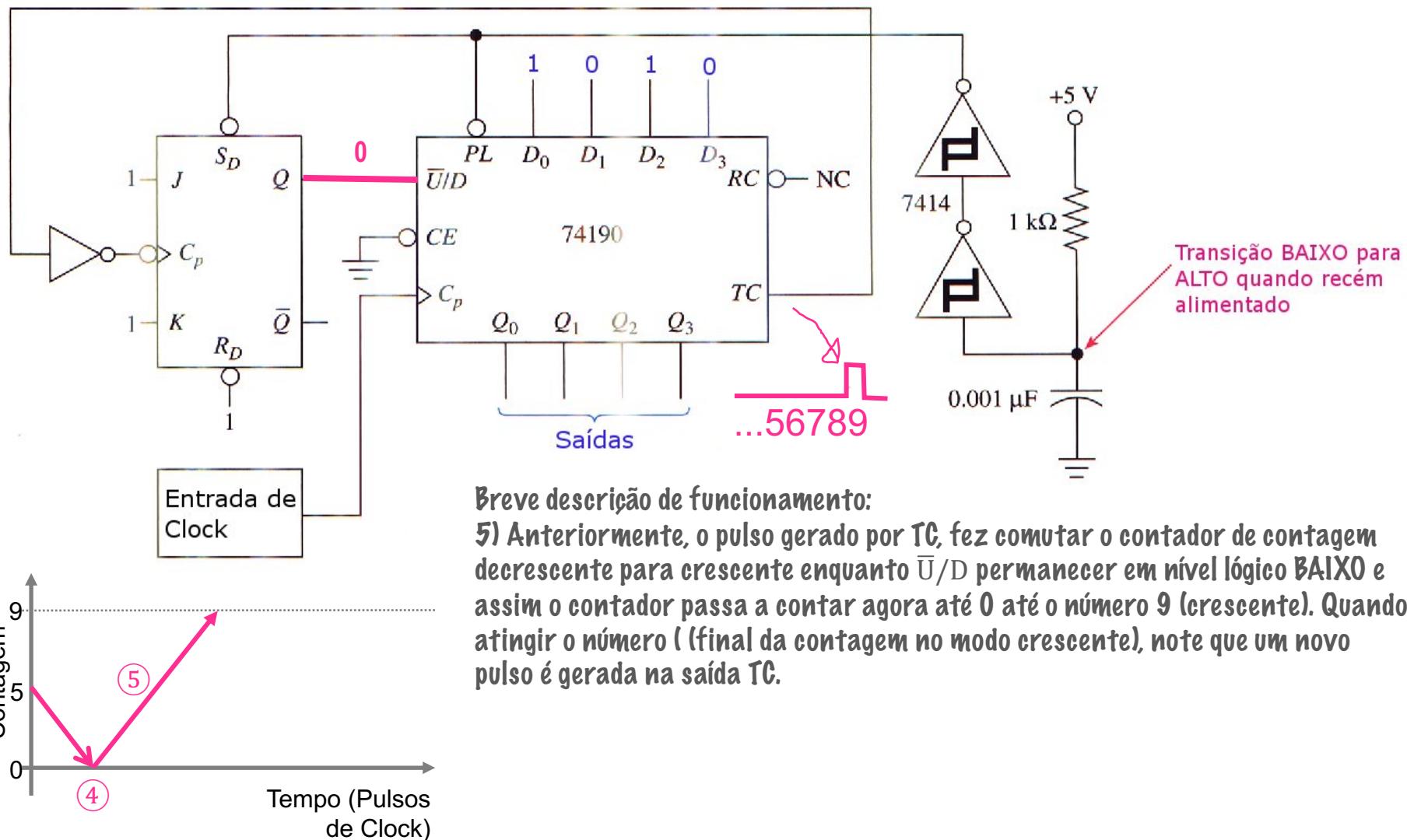
Breve descrição de funcionamento:

3) Depois que $\overline{\text{INIT}}=1$, e como a entrada $\overline{\text{CE}}$ (Count Enable) está permanente ativada ($=0$), o contador começa a contar, de maneira decrescente (a) já que $\overline{\text{U/D}}=1$ (o FF-JK está setado). Esta condição de contagem continua até o contador atingir o final de contagem, indicado por um novo pulso na saída TC (b).

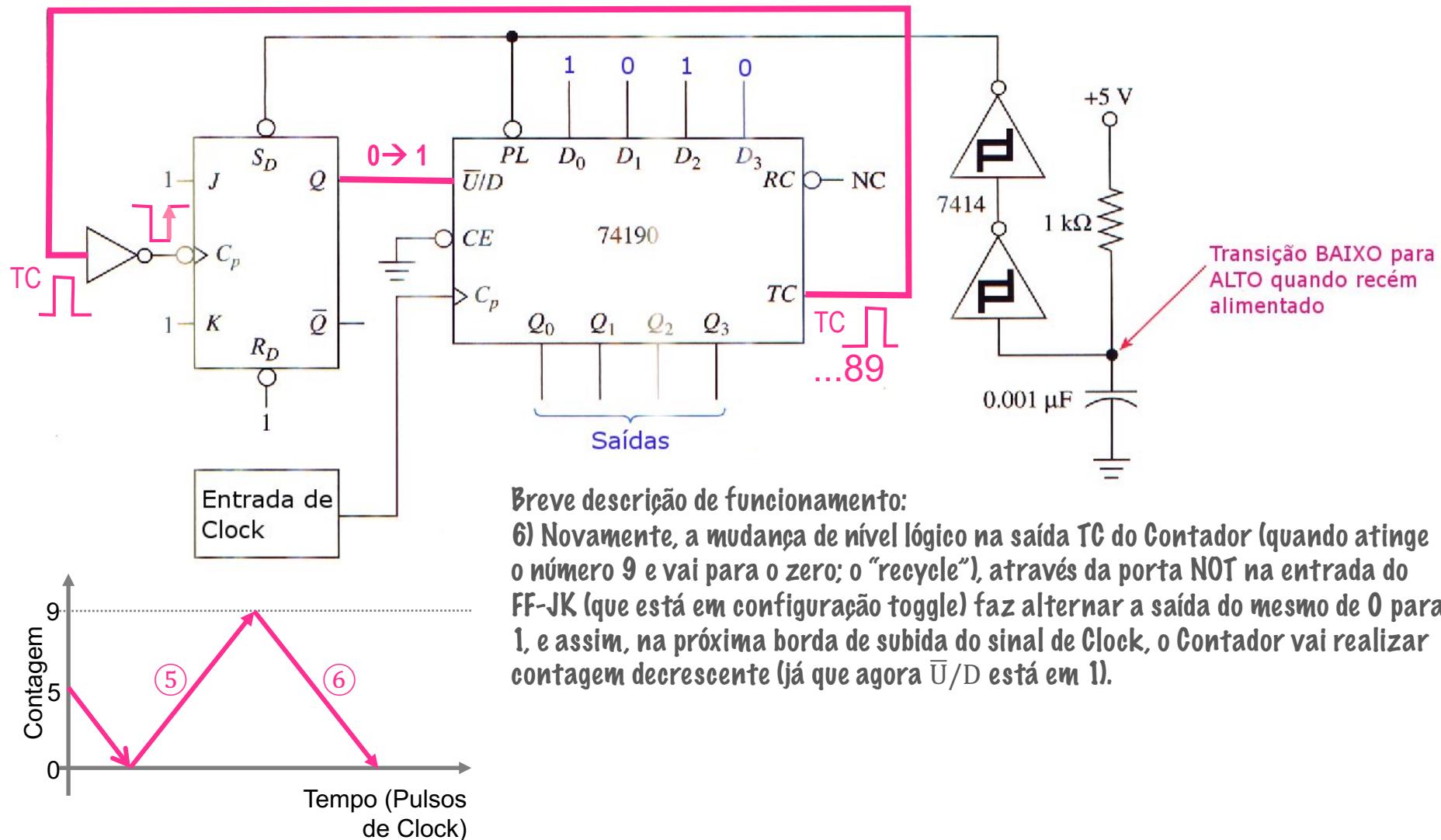
Problema



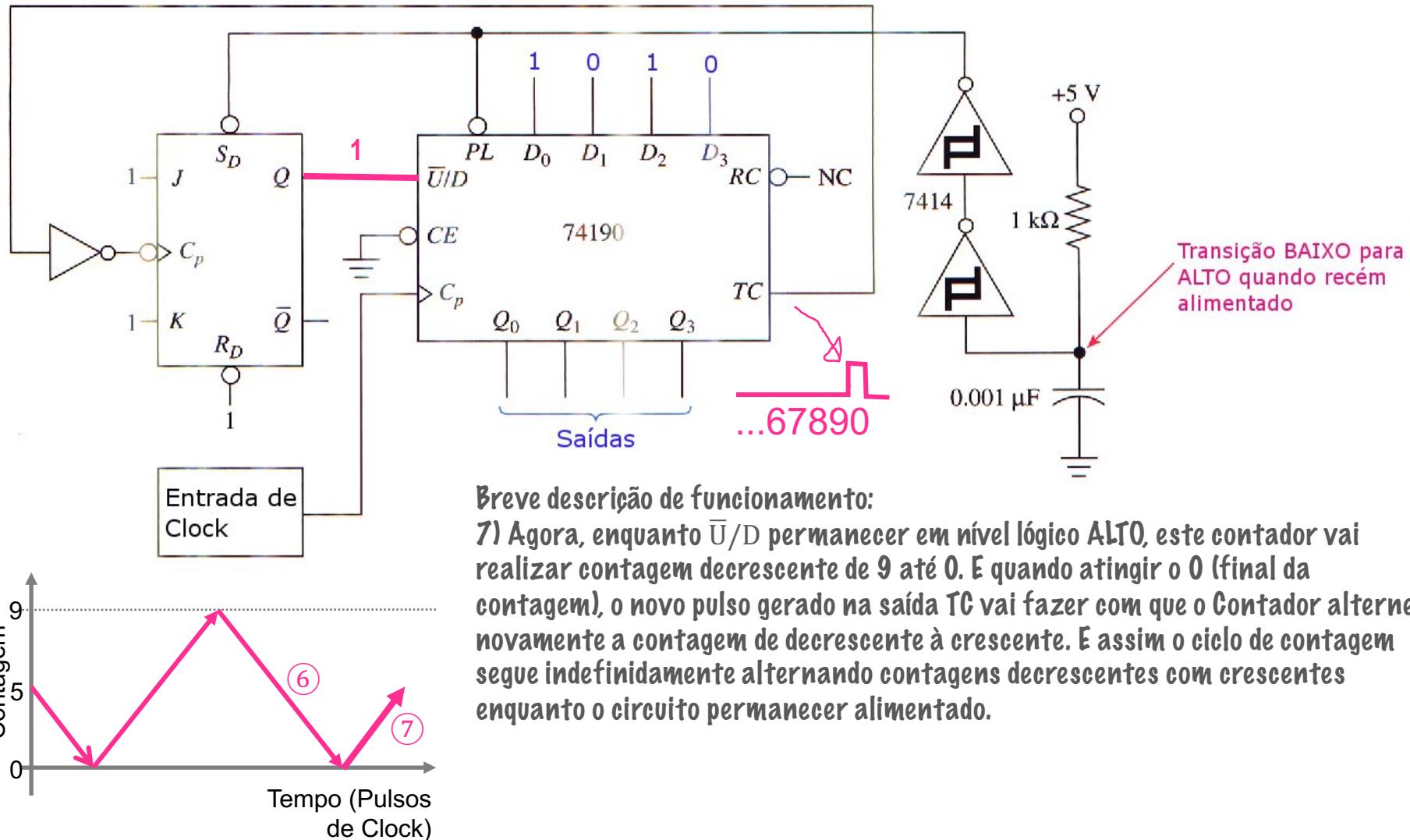
Problema



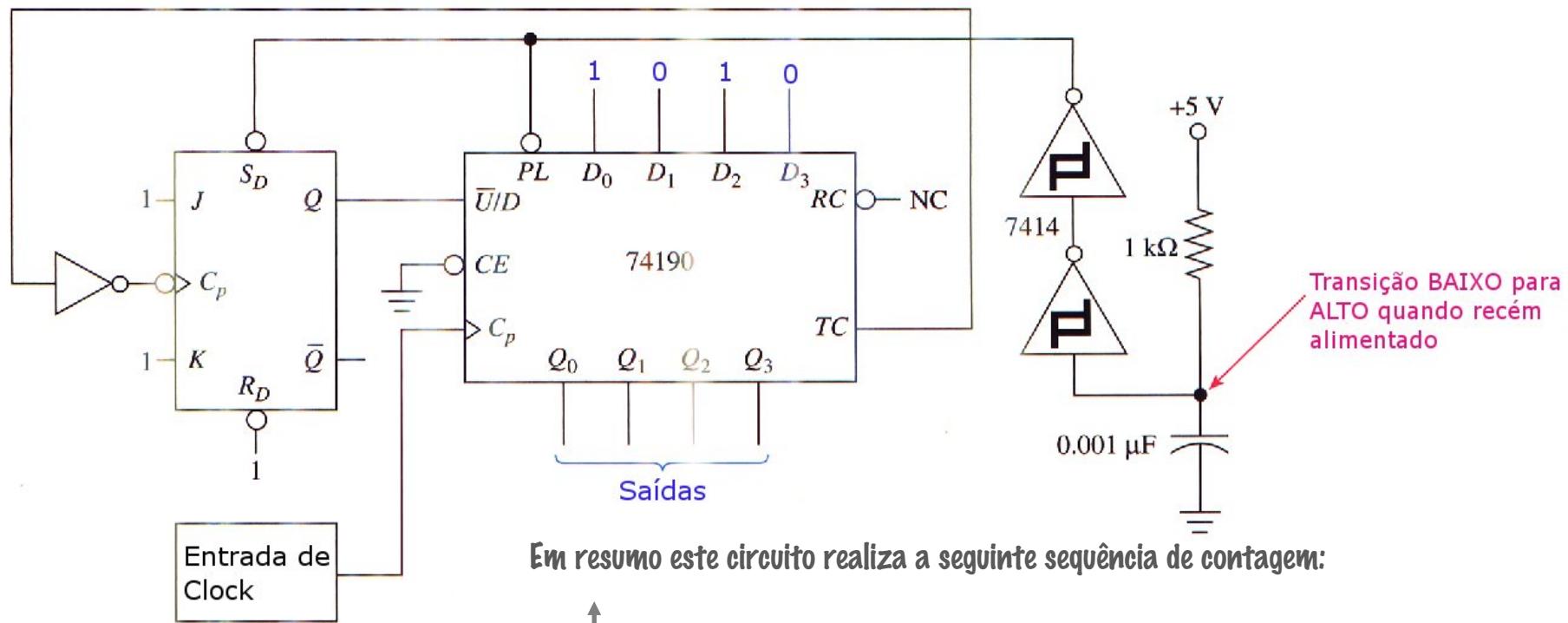
Problema



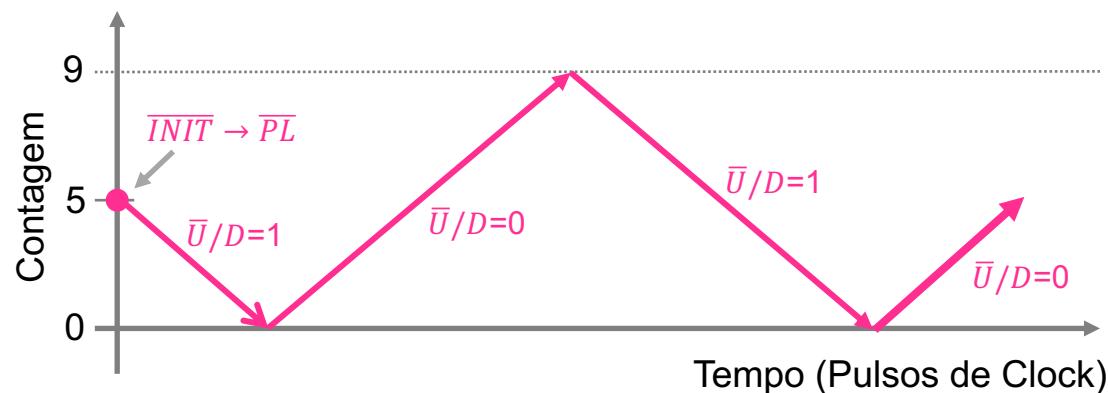
Problema



Problema



Em resumo este circuito realiza a seguinte sequência de contagem:



Projetos:

- Exemplo: contador síncrono decimal:

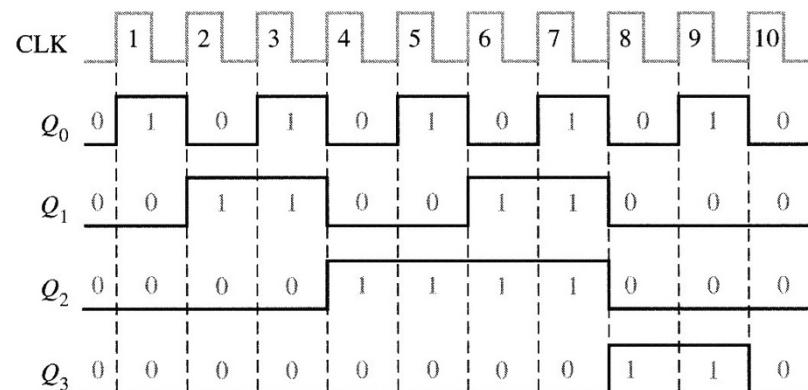
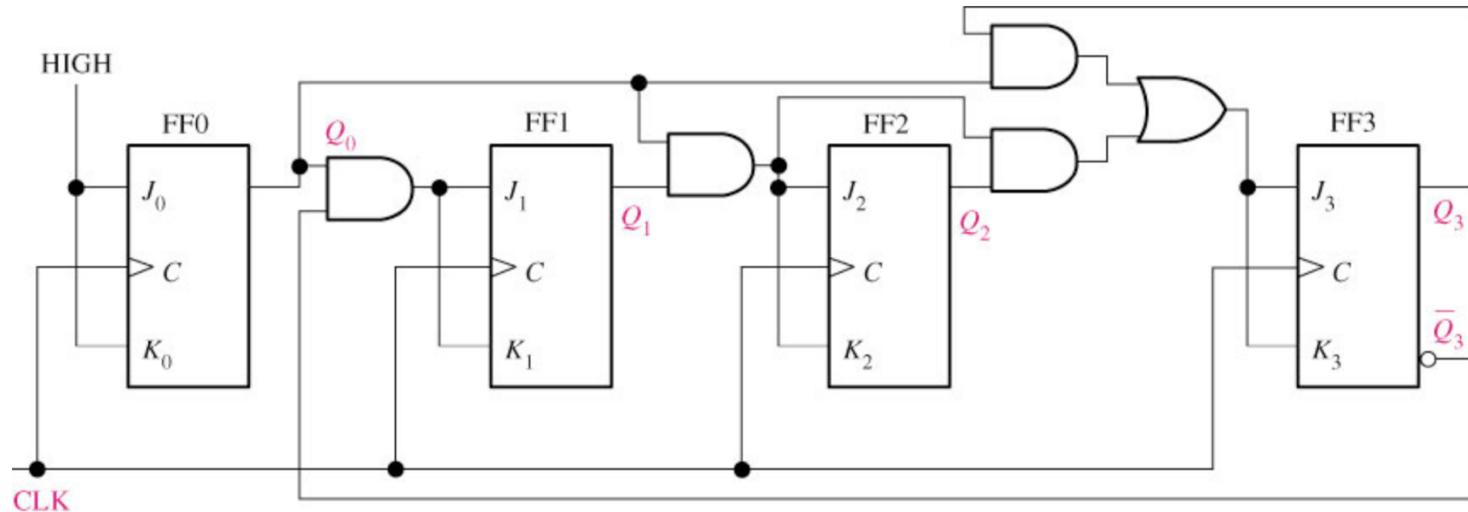


Tabela de transições do FF-JK:

| $Q(t)$ | $Q(t+1)$ | $J(t)$ | $K(t)$ |
|--------|----------|--------|--------|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

Projetos:

- Exemplo: contador síncrono decimal:

2. Mapas de Karnaugh → Circuito final

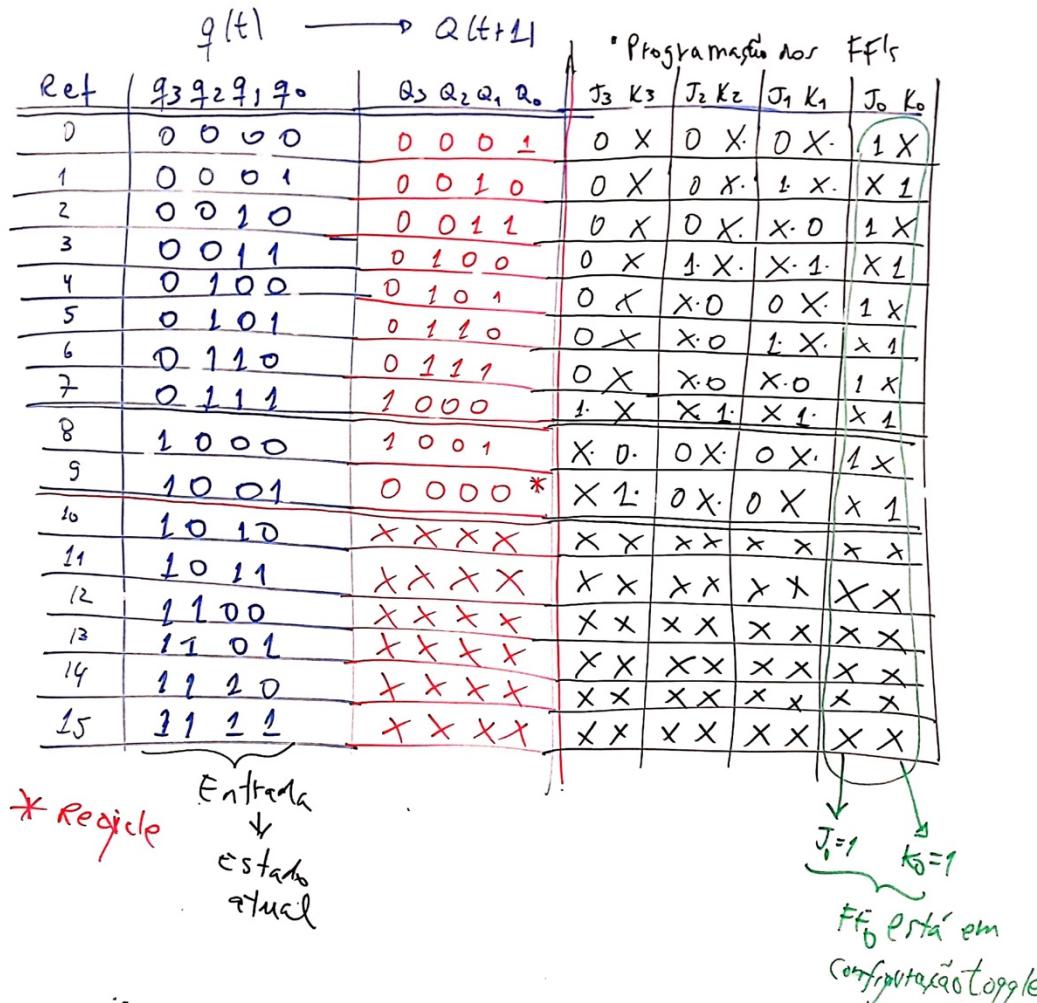


Tabela de transições do FF-JK:

| Q(t) | Q(t+1) | J(t) | K(t) |
|------|--------|------|------|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

Projetos:

- Exemplo: contador síncrono decimal:

- Tabela de transição de contagem (círcuito completo)

$g(t) \rightarrow Q(t+1)$

Ref | $q_3 q_2 q_1 q_0$ | $Q_3 Q_2 Q_1 Q_0$ | $J_3 K_3$ | $J_2 K_2$ | $J_1 K_1$ | $J_0 K_0$

* Programação nos FF's

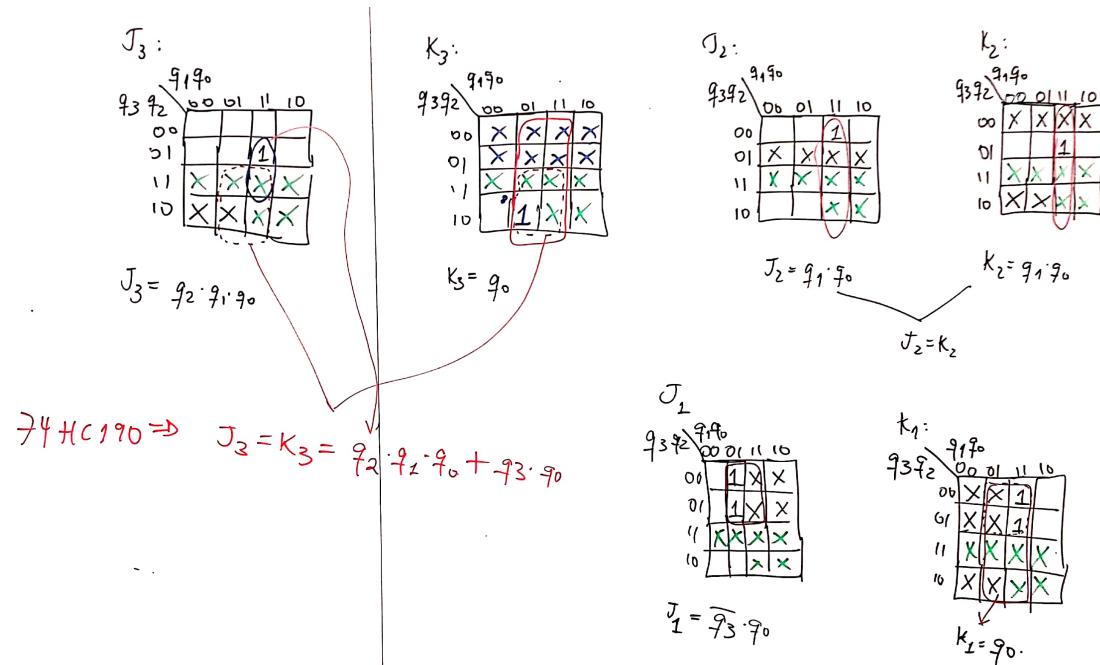
| Ref | $q_3 q_2 q_1 q_0$ | $Q_3 Q_2 Q_1 Q_0$ | $J_3 K_3$ | $J_2 K_2$ | $J_1 K_1$ | $J_0 K_0$ |
|-----|-------------------|-------------------|-----------|-----------|-----------|-----------|
| 0 | 0 0 0 0 | 0 0 0 1 | 0 X | 0 X | 0 X | 1 X |
| 1 | 0 0 0 1 | 0 0 1 0 | 0 X | 0 X | 1 X | X 1 |
| 2 | 0 0 1 0 | 0 0 1 1 | 0 X | 0 X | X 0 | 1 X |
| 3 | 0 0 1 1 | 0 1 0 0 | 0 X | 1 X | X 1 | X 1 |
| 4 | 0 1 0 0 | 0 1 0 1 | 0 X | X 0 | 0 X | X 1 |
| 5 | 0 1 0 1 | 0 1 1 0 | 0 X | X 0 | 1 X | X 1 |
| 6 | 0 1 1 0 | 0 1 1 1 | 0 X | X 0 | X 0 | 1 X |
| 7 | 0 1 1 1 | 1 0 0 0 | 1 X | X 1 | X 1 | X 1 |
| 8 | 1 0 0 0 | 1 0 0 1 | X 0 | 0 X | 0 X | 1 X |
| 9 | 1 0 0 1 | 0 0 0 0 * | X 1 | 0 X | 0 X | X 1 |
| 10 | 1 0 1 0 | X X X X | X X | X X | X X | X X |
| 11 | 1 0 1 1 | X X X X | X X | X X | X X | X X |
| 12 | 1 1 0 0 | X X X X | X X | X X | X X | X X |
| 13 | 1 1 0 1 | X X X X | X X | X X | X X | X X |
| 14 | 1 1 1 0 | X X X X | X X | X X | X X | X X |
| 15 | 1 1 1 1 | X X X X | X X | X X | X X | X X |

* Recicle

Entrada ↓
Estado atual

$J_1 = 1$
 $K_0 = 1$

FF₀ está em configuração toggle.



Projetos:

- Exemplo: contador síncrono decimal:

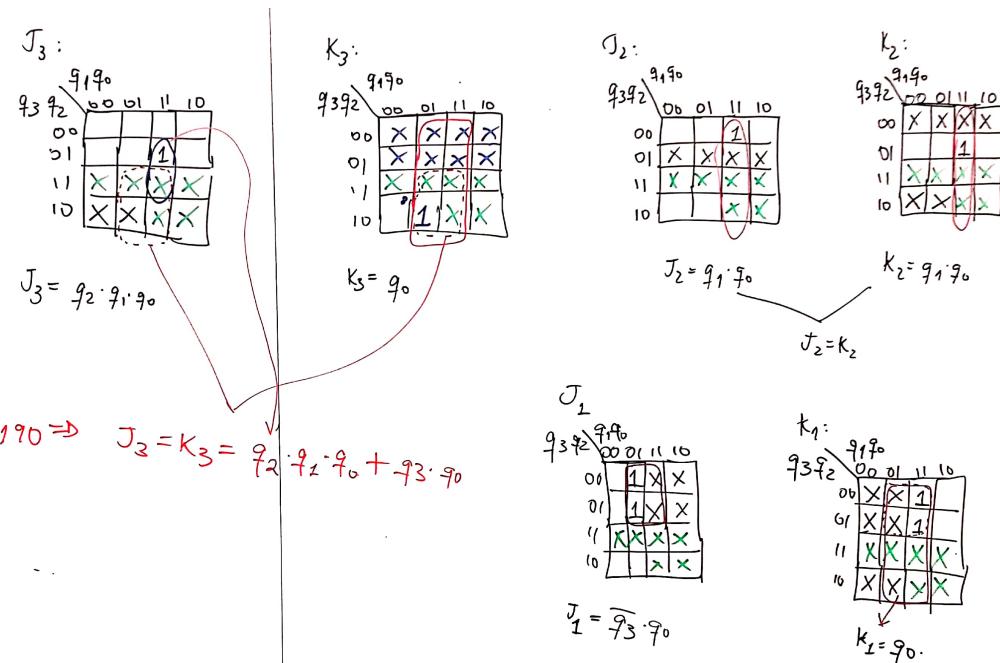
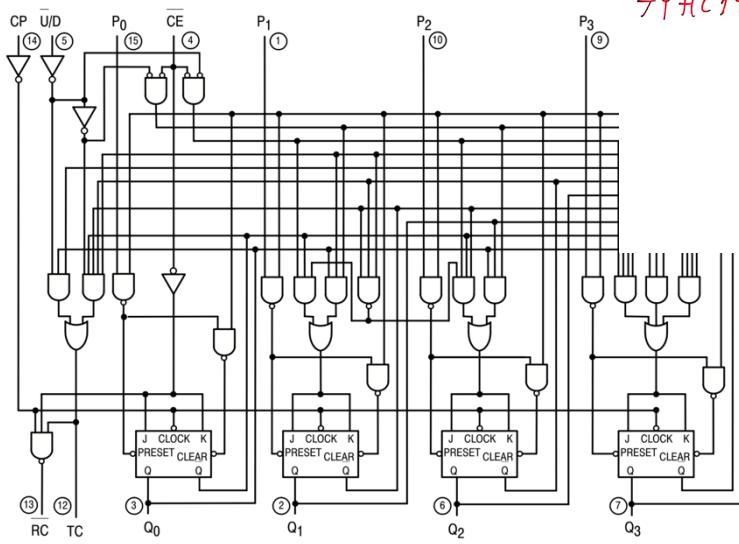
- Tabela de transição de contagem (circuito completo)

$g(t) \rightarrow Q(t+1)$

Ref | $q_3 q_2 q_1 q_0$ | $Q_3 Q_2 Q_1 Q_0$ | $J_3 K_3$ | $J_2 K_2$ | $J_1 K_1$ | $J_0 K_0$ | Programação nos FF's

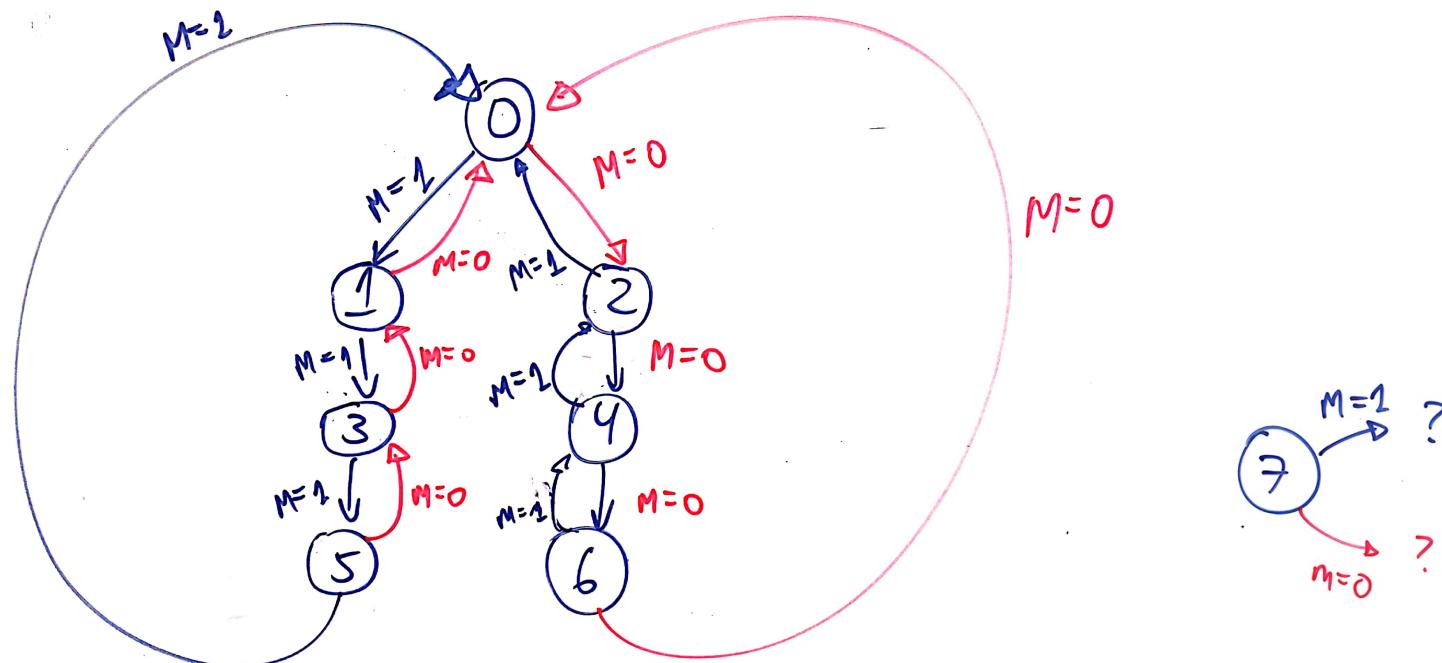
| Ref | $q_3 q_2 q_1 q_0$ | $Q_3 Q_2 Q_1 Q_0$ | $J_3 K_3$ | $J_2 K_2$ | $J_1 K_1$ | $J_0 K_0$ |
|-----|-------------------|-------------------|-----------|-----------|-----------|-----------|
| 0 | 0 0 0 0 | 0 0 0 1 | 0 X | 0 X | 0 X | 1 X |
| 1 | 0 0 0 1 | 0 0 1 0 | 0 X | 0 X | 1 X | X 1 |
| 2 | 0 0 1 0 | 0 0 1 1 | 0 X | 0 X | X 0 | 1 X |
| 3 | 0 0 1 1 | 0 1 0 0 | 0 X | 1 X | X 1 | X 1 |
| 4 | 0 1 0 0 | 0 1 0 1 | 0 X | X 0 | 0 X | 1 X |
| 5 | 0 1 0 1 | 0 1 1 0 | 0 X | X 0 | 1 X | X 1 |
| 6 | 0 1 1 0 | 0 1 1 1 | 0 X | X 0 | X 0 | 1 X |
| 7 | 0 1 1 1 | 1 0 0 0 | 1 X | X 1 | X 1 | X 1 |
| 8 | 1 0 0 0 | 1 0 0 1 | X 0 | 0 X | 0 X | 1 X |
| 9 | 1 0 0 1 | 1 0 1 0 | X 0 | 0 X | 0 X | 1 X |

LOGIC DIAGRAMS



Outros projetos:

- Exemplo₂:



Opções
→ FF's - JK $\Rightarrow 3 \times FF's \Rightarrow 3 \times 2$ entradas (J, K) $\Rightarrow 6$ mapas K
→ FF's - D $\Rightarrow 3 \times FF'r \Rightarrow 3 \times 1$ entrada (D) $\Rightarrow 3$ mapas K ←

Outros projetos:

- Exemplo₂:

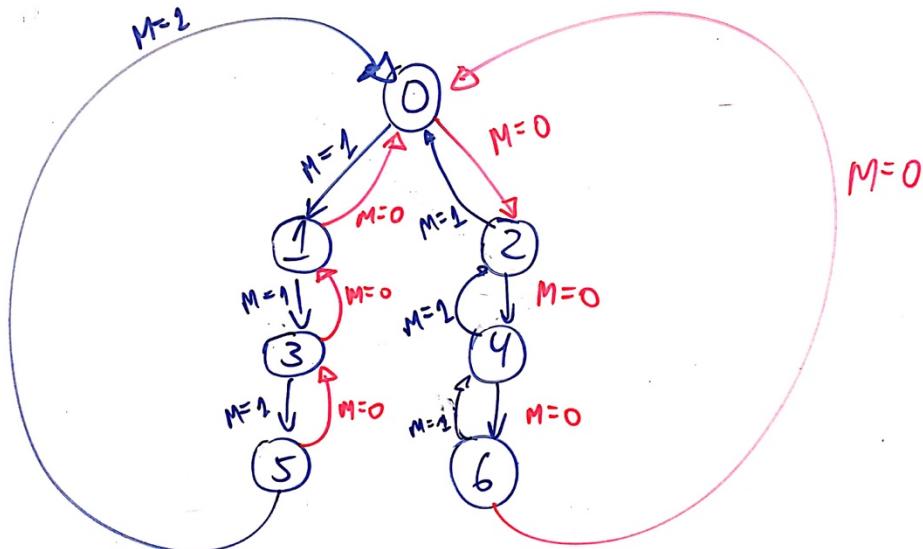


Tabela de transição do circuito completo:

| Ref | M | $q_2^{(t)}$ | $q_1^{(t)}$ | $q_0^{(t)}$ | Q_2 | Q_1 | Q_0 | D_2 | D_1 | D_0 |
|-----|---|-------------|-------------|-------------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | X | X | X | X | X | X |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 12 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 13 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 15 | 1 | 1 | 2 | 1 | X | X | X | X | X | X |

Opções \rightarrow FF's - JK $\Rightarrow 3 \times \text{FF}'s \Rightarrow 3 \times 2$ entradas (J, K) $\Rightarrow 6$ mapas K
 \rightarrow FF's - D $\Rightarrow 3 \times \text{FF}'s \Rightarrow 3 \times 1$ entrada (D) $\Rightarrow 3$ mapas K \leftarrow

Outros projetos:

- Exemplo₂:

Tabela de transição do circuito completo:

| Ref | M | $q_2^{(t)}$ | $q_1^{(t)}$ | $q_0^{(t)}$ | Q_2 | Q_1 | Q_0 | D_2 | D_1 | D_0 |
|-----|---|-------------|-------------|-------------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (1) | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | (1) | 0 | 0 |
| 3 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (1) | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | (1) | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | X | X | X | (X) | (X) | (X) |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (1) |
| 9 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | (1) | (1) |
| 10 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | (1) | 0 | (1) |
| 12 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | (1) | 0 |
| 13 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | (1) | 0 | 0 |
| 15 | 1 | 1 | 2 | 1 | X | X | X | (X) | (X) | (X) |

| $D_2:$ | |
|-----------|-----|
| $q_1 q_0$ | |
| 00 | |
| 01 | (1) |
| 11 | X |
| 10 | |

| $D_1:$ | |
|-----------|-----|
| $q_1 q_0$ | |
| 00 | 1 |
| 01 | (1) |
| 11 | X |
| 10 | 1 |

| $D_0:$ | |
|-----------|---|
| $q_1 q_0$ | |
| 00 | 1 |
| 01 | X |
| 11 | X |
| 10 | 1 |

$$\begin{aligned}
 D_2 &= \overline{M} \cdot q_2 \cdot \overline{q_1} \cdot \overline{q_0} + \overline{M} \cdot \overline{q_2} \cdot q_2 \cdot \overline{q_0} + \\
 &\quad + M \cdot q_2 \cdot q_1 + M \cdot q_1 \cdot q_0 \\
 &= \overline{M} \cdot \overline{q_0} (q_2 \cdot \overline{q_1} + \overline{q_2} \cdot q_1) + M \cdot q_1 (q_2 + q_0) \\
 &= \overline{M} \cdot \overline{q_0} (q_2 \odot q_1) + M \cdot q_1 \cdot (q_2 + q_0)
 \end{aligned}$$

$$\begin{aligned}
 D_1 &= \overline{M} \cdot \overline{q_1} \cdot \overline{q_0} + q_2 \cdot \overline{q_1} \cdot \overline{q_0} + \overline{M} \cdot q_2 \cdot q_0 + \\
 &\quad + M \cdot \overline{q_2} \cdot \overline{q_1} \cdot q_0 \\
 &= \overline{q_1} \cdot \overline{q_0} (\overline{M} + q_2) + q_0 (\overline{M} \cdot q_2 + M \cdot \overline{q_2} \cdot \overline{q_1})
 \end{aligned}$$

$$D_0 = q_1 \cdot q_0 + \overline{M} \cdot q_2 \cdot q_0 + M \cdot \overline{q_2} \cdot \overline{q_1}$$

Outros projetos:

- Exemplo₂:

Tabela de transição do circuito completo:

| Ref | M | $q_2 q_1 q_0$ | $Q_2 Q_1 Q_0$ | $D_2 D_1 D_0$ |
|-----|---|---------------|---------------|---------------|
| 0 | 0 | 0 0 0 | 0 1 0 | 0 (1) 0 |
| 1 | 0 | 0 0 1 | 0 0 0 | 0 0 0 |
| 2 | 0 | 0 1 0 | 1 0 0 | (1) 0 0 |
| 3 | 0 | 0 1 1 | 0 0 1 | 0 0 (1) |
| 4 | 0 | 1 0 0 | 1 1 0 | (1) (1) 0 |
| 5 | 0 | 1 0 1 | 0 1 1 | 0 (1) (1) |
| 6 | 0 | 1 1 0 | 0 0 0 | 0 0 0 |
| 7 | 0 | 1 1 1 | X X X | (X) (X) (X) |
| 8 | 1 | 0 0 0 | 0 0 1 | 0 0 (1) |
| 9 | 1 | 0 0 1 | 0 1 1 | 0 (1) (1) |
| 10 | 1 | 0 1 0 | 0 0 0 | 0 0 0 |
| 11 | 1 | 0 1 1 | 1 0 1 | (1) 0 (1) |
| 12 | 1 | 1 0 0 | 0 1 0 | 0 (1) 0 |
| 13 | 1 | 1 0 1 | 0 0 0 | 0 0 0 |
| 14 | 1 | 1 1 0 | 1 0 0 | (1) 0 0 |
| 15 | 1 | 1 1 1 | X X X | (X) (X) (X) |

D_2 :

| M_{q_2} | | 00 | 01 | 11 | 10 |
|-----------|---|-----|----|----|----|
| 00 | 1 | | | | 1 |
| 01 | 1 | X | | | |
| 11 | | X 1 | | | |
| 10 | | | 1 | | |

D_1 :

| M_{q_2} | | 00 | 01 | 11 | 10 |
|-----------|---|----|----|----|----|
| 00 | 1 | | | | |
| 01 | 1 | 1 | 1 | X | |
| 11 | 1 | | X | | |
| 10 | | 1 | | | |

D_0 :

| M_{q_2} | | 00 | 01 | 11 | 10 |
|-----------|---|----|----|----|----|
| 00 | | | | | |
| 01 | | 1 | X | | |
| 11 | | | X | | |
| 10 | 1 | 1 | X | 1 | 1 |

$$\begin{aligned}
 D_2 &= \overline{M} \cdot q_2 \cdot \overline{q_1} \cdot \overline{q_0} + \overline{M} \cdot \overline{q_2} \cdot q_2 \cdot \overline{q_0} + \\
 &\quad + M \cdot q_2 \cdot q_1 + M \cdot q_1 \cdot q_0 \\
 &= \overline{M} \cdot \overline{q_0} (q_2 \cdot \overline{q_1} + \overline{q_2} \cdot q_1) + M \cdot q_1 (q_2 + q_0) \\
 &= \overline{M} \cdot \overline{q_0} (q_2 \odot q_1) + M \cdot q_1 \cdot (q_2 + q_0)
 \end{aligned}$$

$$\begin{aligned}
 D_1 &= \overline{M} \cdot \overline{q_1} \cdot \overline{q_0} + q_2 \cdot \overline{q_1} \cdot \overline{q_0} + \overline{M} \cdot q_2 \cdot q_0 + \\
 &\quad + M \cdot \overline{q_2} \cdot \overline{q_1} \cdot q_0 \\
 &= \overline{q_1} \cdot \overline{q_0} (\overline{M} + q_2) + q_0 (\overline{M} \cdot q_2 + M \cdot \overline{q_2} \cdot \overline{q_1})
 \end{aligned}$$

$$D_0 = q_1 \cdot q_0 + \overline{M} \cdot q_2 \cdot q_0 + M \cdot \overline{q_2} \cdot \overline{q_1}$$

Outra solução + simples p/circuito?

Outros projetos:

- Exemplo₂:

D_2 :

| | | q ₂ q ₀ | 00 | 01 | 11 | 10 |
|----|----------------|-------------------------------|----|----|----|----|
| | | ∞ | 1 | X | | 1 |
| M | q ₂ | 00 | 1 | X | | 1 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 1 | 0 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 0 |
| 10 | 1 | 1 | 0 | 0 | 0 | 0 |

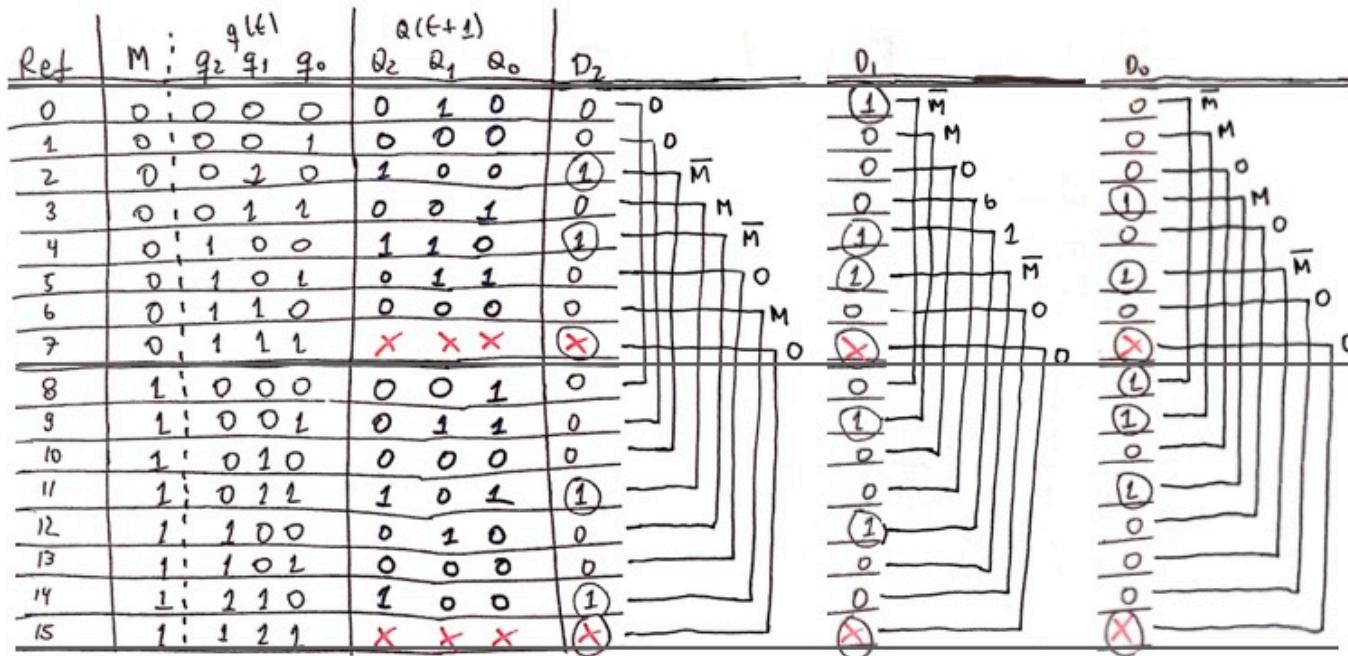
D_1 :

| | | q ₂ q ₀ | 00 | 01 | 11 | 10 |
|----|----------------|-------------------------------|----|----|----|----|
| | | ∞ | 1 | 1 | X | |
| M | q ₂ | 00 | 1 | 1 | X | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 1 | 0 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 0 |
| 10 | 1 | 1 | 0 | 0 | 0 | 0 |

D_0 :

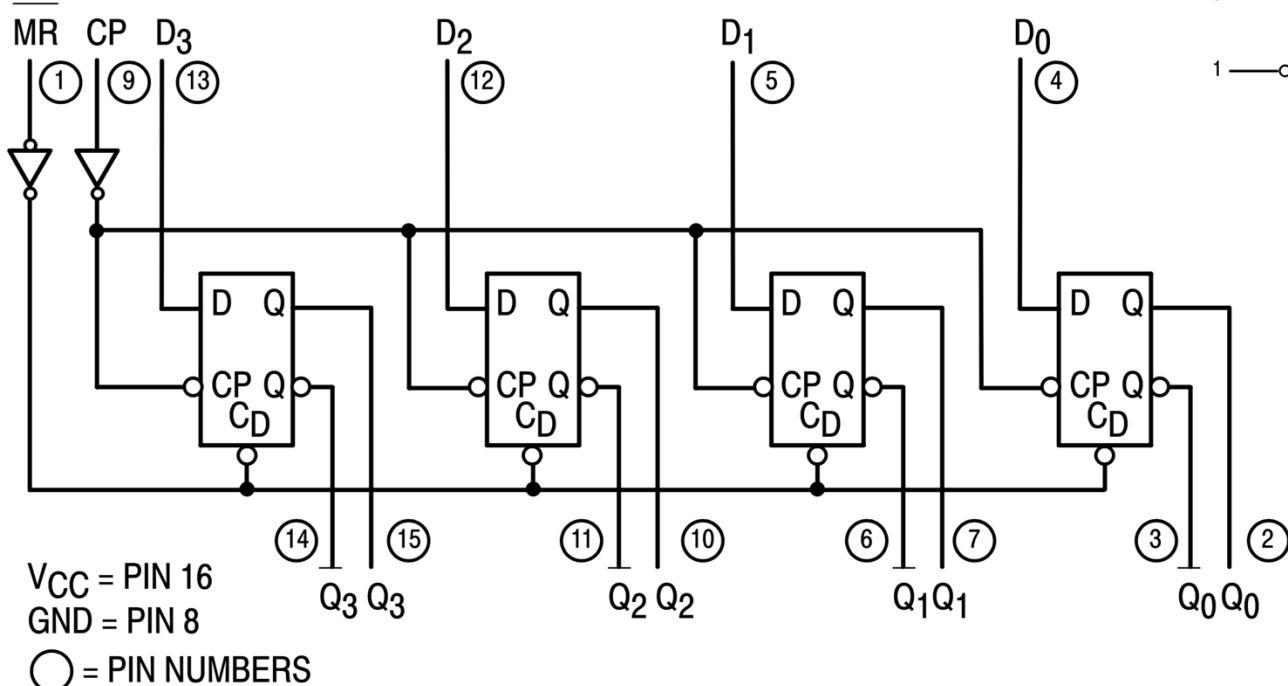
| | | q ₂ q ₀ | 00 | 01 | 11 | 10 |
|----|----------------|-------------------------------|----|----|----|----|
| | | ∞ | 1 | 1 | X | |
| M | q ₂ | 00 | 1 | 1 | X | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 1 | 0 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 0 |
| 10 | 1 | 1 | 0 | 0 | 0 | 0 |

Outra solução + simples
p/circuito? Uso de MUXes

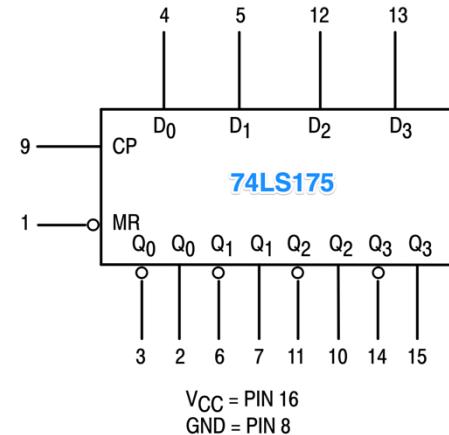


Outros projetos:

- Exemplo₂:



Outra solução + simples
p/circuito? Uso de MUXes e CI
com 4 FF's-D: 74LS175

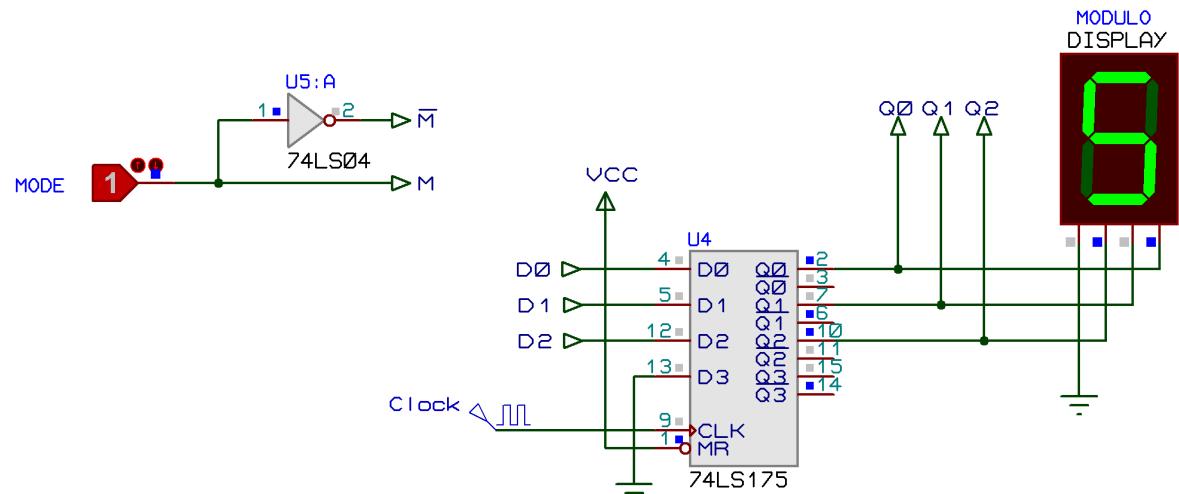
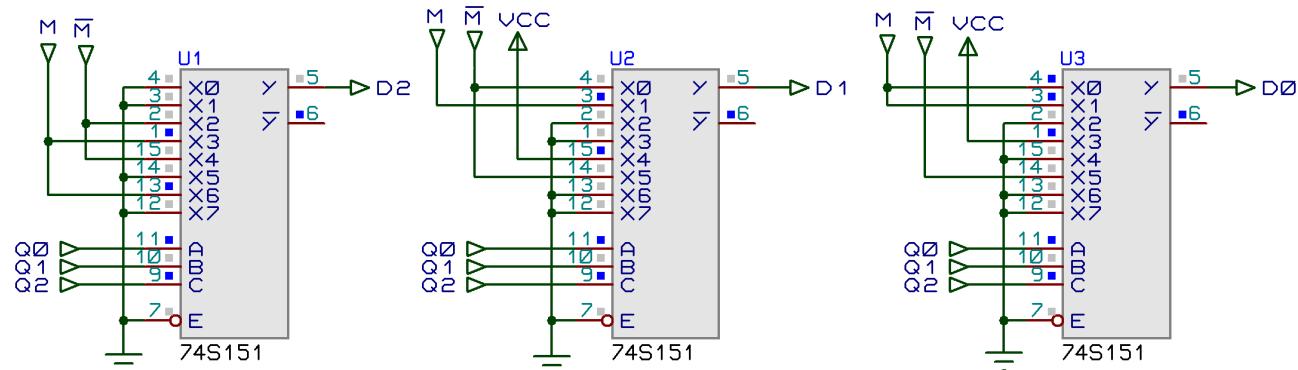
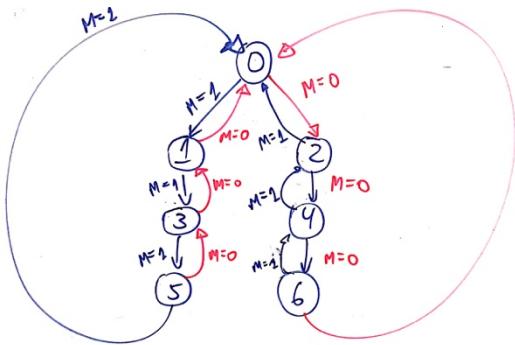


V_{CC} = PIN 16
GND = PIN 8

Outros projetos:

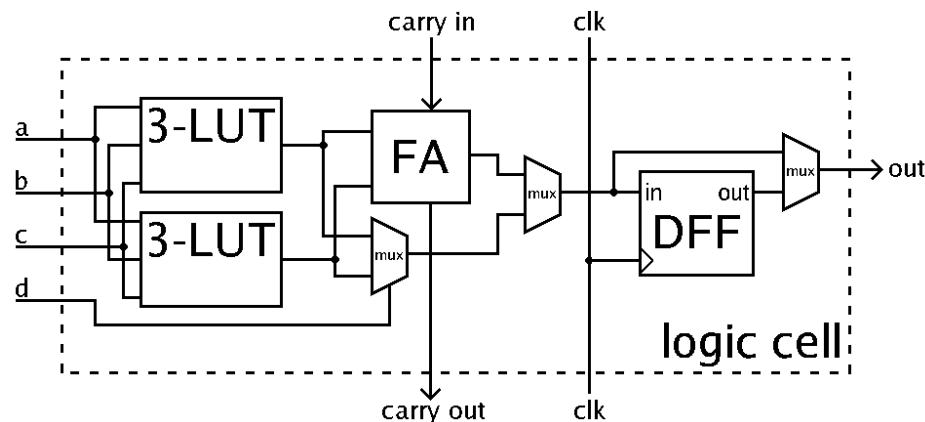
- Exemplo₂:

Solução + simples p/circuito: Uso de MUXes e CI com 4 FF's-D: 74LS175



Detalhe última solução ➔ FPGAs

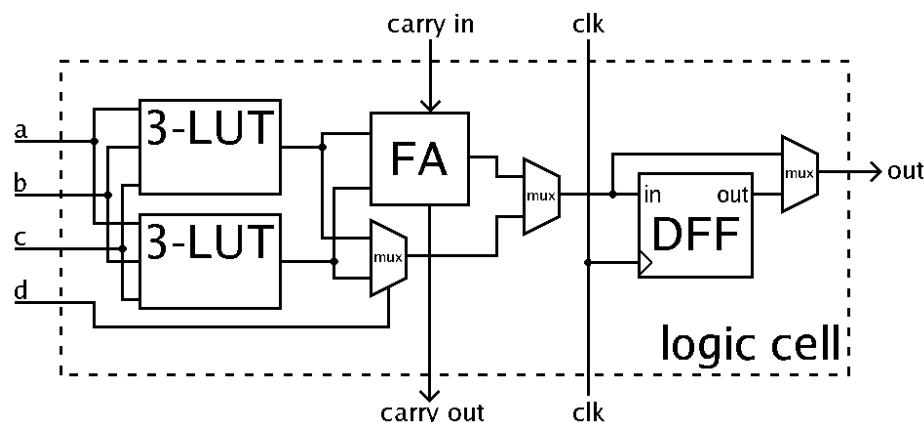
- Estrutura interna (genérica/simplificada) de um FPGA:



- Este tipo de pastilha permite programar o acionamento de Flipf-Flop's através de "lookup tables". A logica combinacional definida para acinar als) entradas(s) de controle do FF fica programada dentro de uma "lookup table", ou "LUT".
- Note a presença de um FF tipo D, um somador completo (FA = Full Adder) e 2 conjuntos de LUT para até 3 variáveis de entrada.
- Note que é comum que o circuito lógico correspondente a cada LUT seja formado usando um Multiplexador, no caso da figura mostrada, seria um MUX para até 8 linhas de entrada, os pontos a, b e c correspondem aos pinos de Select do MUX.

Detalhe última solução ➡ FPGAs

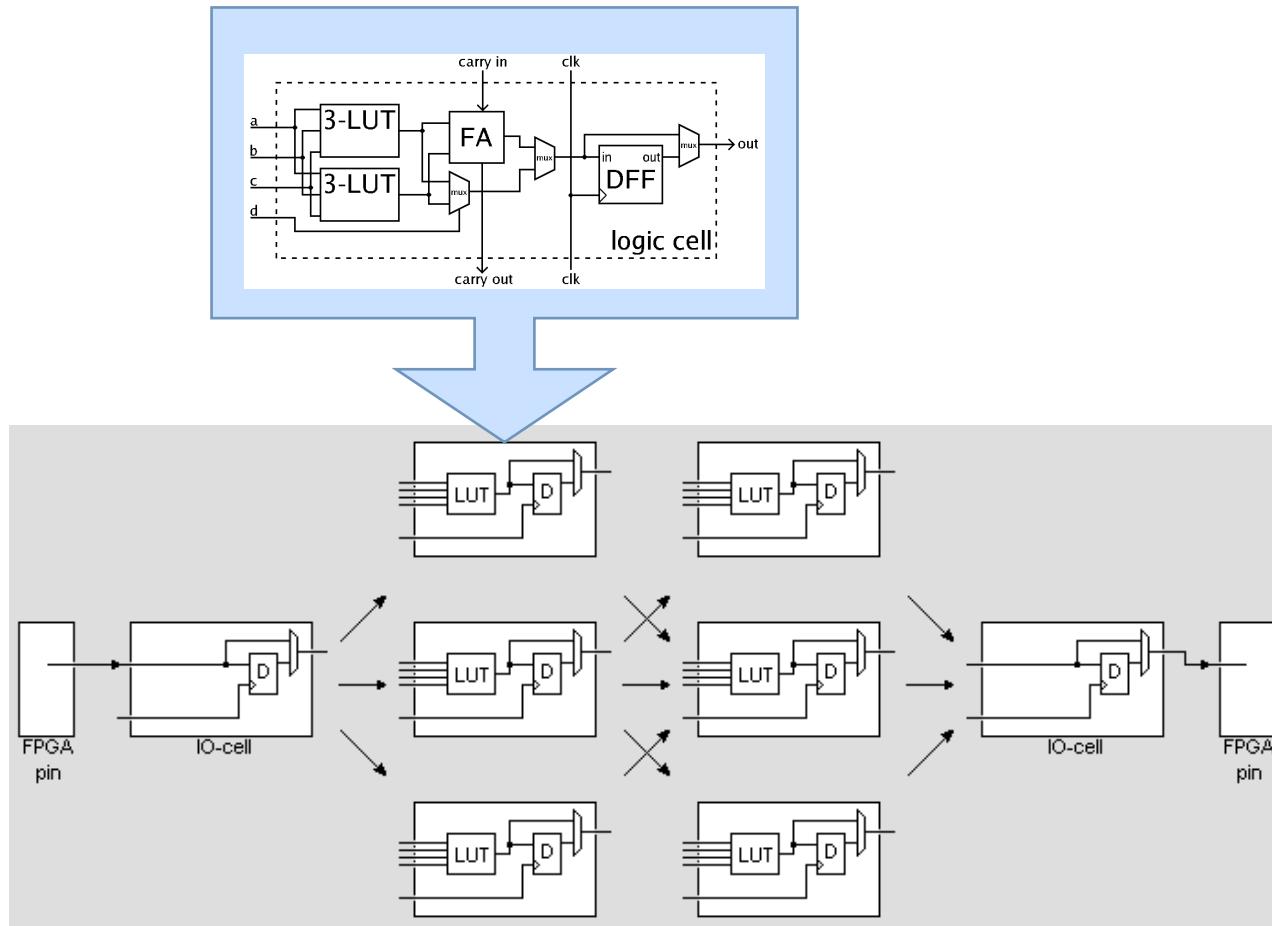
- Estrutura interna (genérica/simplificada) de um FPGA:



- Alguns FPGA's não incluem na sua célula básica um soma-dor completo.
- Neste caso, a saída do MUX é normalmente conectada à entrada de uma porta AND de 2 entradas, onde a segunda entrada da porta AND ficaria conectada ao ponto d (da figura). Note que este ponto d permite que o mesmo atue como um sinal de Enable.
- Uma pastilha FPGA é formada por centenas ou milhares destas células lógicas básicas. Cada célula lógica pode ser conectada a outras células através de recursos de interconexão ("fusíveis") programados por software. Cada célula isoladamente pode fazer pouco, mas com muitas delas conectados juntas, funções lógicas complexas podem ser criadas através de celulas de Entrada/Saída (IO-cells).

Detalhe última solução ➡ FPGAs

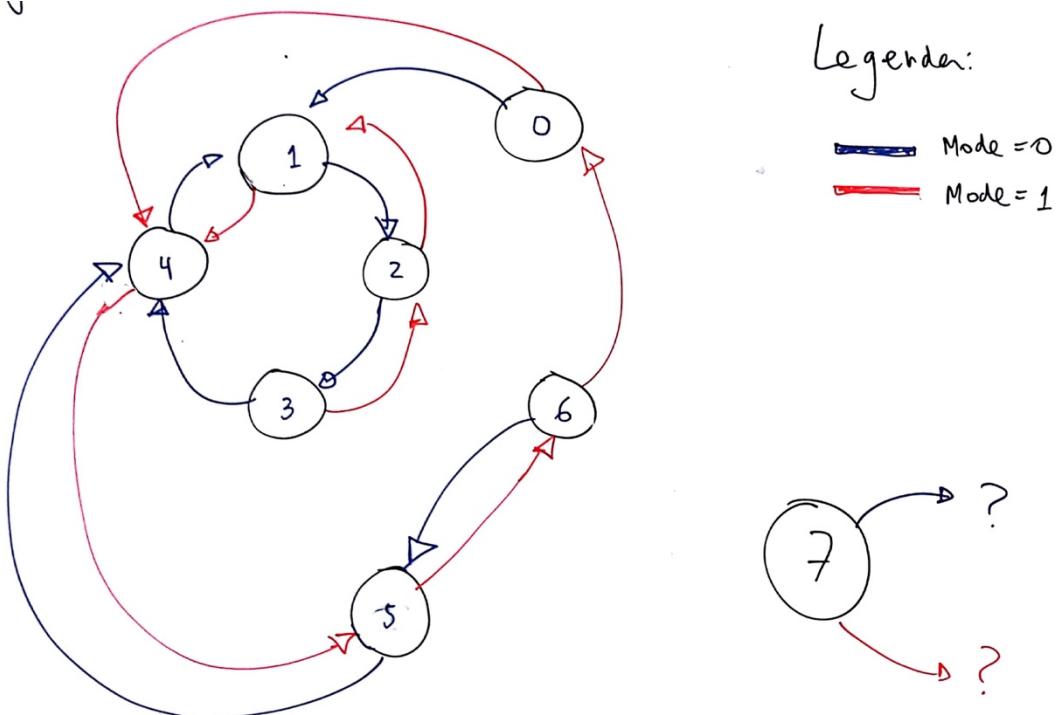
- Estrutura interna (genérica/simplificada) de um FPGA:



Uma pastilha FPGA é formada por centenas ou milhares destas células lógicas básicas. Cada célula lógica pode ser conectada a outras células através de recursos de interconexão ("fusíveis") programados por software. Cada célula isoladamente pode fazer pouco, mas com muitas delas conectadas juntas, funções lógicas complexas podem ser criadas através de células de Entrada/Saída (IO-cells).

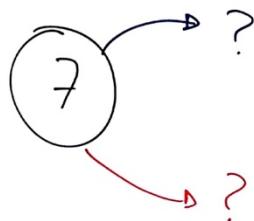
Outros projetos:

- Exemplo₃:



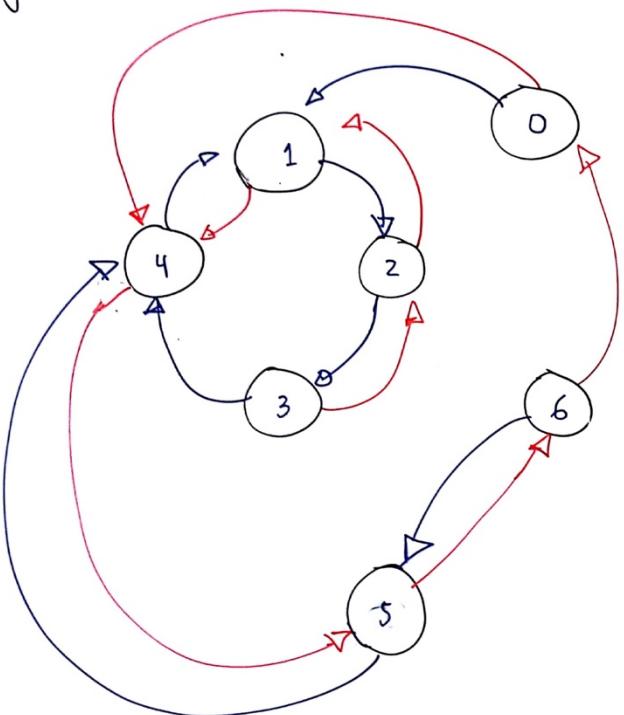
Legend:

- Mode = 0
- Mode = 1



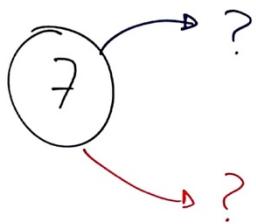
Outros projetos:

- Exemplo 3:



Legenda:

- Mode = 0
- Mode = 1



| Ref | (M) Mode | $g(t)$ $\rightarrow Q(t+1)$ | | | | D_2 D_1 D_0 |
|-----|-------------|-----------------------------|-------|-------|-------------------|-------------------|
| | | q_2 | q_1 | q_0 | Q_2 Q_1 Q_0 | |
| 0 | 0 | 0 | 0 | 0 | 0 0 1 | 0 0 1 |
| 1 | 0 | 0 | 0 | 1 | 0 1 0 | 0 1 0 |
| 2 | 0 | 0 | 1 | 0 | 0 1 1 | 0 1 1 |
| 3 | 0 | 0 | 1 | 1 | 1 0 0 | 1 0 0 |
| 4 | 0 | 1 | 0 | 0 | 0 0 1 | 0 0 1 |
| 5 | 0 | 1 | 0 | 1 | 1 0 0 | 1 0 0 |
| 6 | 0 | 1 | 1 | 0 | 1 0 1 | 1 0 1 |
| 7 | 0 | 1 | 1 | 1 | X X X | X X X |
| 8 | 1 | 0 | 0 | 0 | 1 0 0 | 1 0 0 |
| 9 | 1 | 0 | 0 | 1 | 1 0 0 | 1 0 0 |
| 10 | 2 | 0 | 1 | 0 | 0 0 1 | 0 0 1 |
| 11 | 1 | 0 | 1 | 1 | 0 1 0 | 0 1 0 |
| 12 | 1 | 1 | 0 | 0 | 1 0 1 | 1 0 1 |
| 13 | 1 | 1 | 0 | 1 | 1 1 0 | 1 1 0 |
| 14 | 1 | 1 | 1 | 0 | 0 0 0 | 0 0 0 |
| 15 | 1 | 1 | 1 | 1 | X X X | X X X |

Outros projetos:

- Exemplo 3:

| Ref | (M) Mode | $q(t)$ | $Q(t+1)$ | D_2 | D_1 | D_0 |
|-----|-------------|-----------------|-----------------|-------|-------|-------|
| | | $q_2\ q_1\ q_0$ | $Q_2\ Q_1\ Q_0$ | | | |
| 0 | 0 | 0 0 0 | 0 0 1 | 0 0 1 | 0 0 1 | 0 0 1 |
| 1 | 0 | 0 0 1 | 0 1 0 | 0 1 0 | 0 1 0 | 0 1 0 |
| 2 | 0 | 0 1 0 | 0 1 1 | 0 1 1 | 0 1 1 | 0 1 1 |
| 3 | 0 | 0 1 1 | 1 0 0 | 1 0 0 | 1 0 0 | 1 0 0 |
| 4 | 0 | 1 0 0 | 0 0 1 | 0 0 1 | 0 0 1 | 0 0 1 |
| 5 | 0 | 1 0 1 | 1 0 0 | 1 0 0 | 1 0 0 | 1 0 0 |
| 6 | 0 | 1 1 0 | 1 0 1 | 1 0 1 | 1 0 1 | 1 0 1 |
| 7 | 0 | 1 1 1 | XXX | XXX | XXX | XXX |
| 8 | 1 | 0 0 0 | 1 0 0 | 1 0 0 | 1 0 0 | 1 0 0 |
| 9 | 1 | 0 0 1 | 1 0 0 | 1 0 0 | 1 0 0 | 1 0 0 |
| 10 | 1 | 0 1 0 | 0 0 1 | 0 0 1 | 0 0 1 | 0 0 1 |
| 11 | 1 | 0 1 1 | 0 1 0 | 0 1 0 | 0 1 0 | 0 1 0 |
| 12 | 1 | 1 0 0 | 1 0 1 | 1 0 1 | 1 0 1 | 1 0 1 |
| 13 | 1 | 1 0 1 | 1 1 0 | 1 1 0 | 1 1 0 | 1 1 0 |
| 14 | 1 | 1 1 0 | 0 0 0 | 0 0 0 | 0 0 0 | 0 0 0 |
| 15 | 1 | 1 1 1 | XXX | XXX | XXX | XXX |

D_2 :

| $M\ q_2$ | 00 | 01 | 11 | 10 |
|----------|----|----|----|----|
| 00 | | | 1 | |
| 01 | | 1 | X | 1 |
| 11 | 1 | 1 | X | |
| 10 | 1 | 1 | | |

$$D_2 = M \cdot \bar{q}_1 + \bar{M} \cdot q_2 \cdot q_0 + \bar{M} \cdot q_1 \cdot q_0 + \bar{M} \cdot q_2 \cdot q_1$$

D_1 :

| $M\ q_2$ | 00 | 01 | 11 | 10 |
|----------|----|----|----|----|
| 00 | 1 | | 1 | |
| 01 | 1 | X | | |
| 11 | 1 | X | | |
| 10 | 1 | | | |

$$D_1 = \underbrace{\bar{M} \cdot \bar{q}_2 \cdot \bar{q}_1 \cdot q_0 + \bar{M} \cdot \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + M \cdot \bar{q}_2 \cdot q_0 + M \cdot q_1 \cdot q_0}_{\bar{M} \cdot \bar{q}_2 (q_1 \oplus q_0)}$$

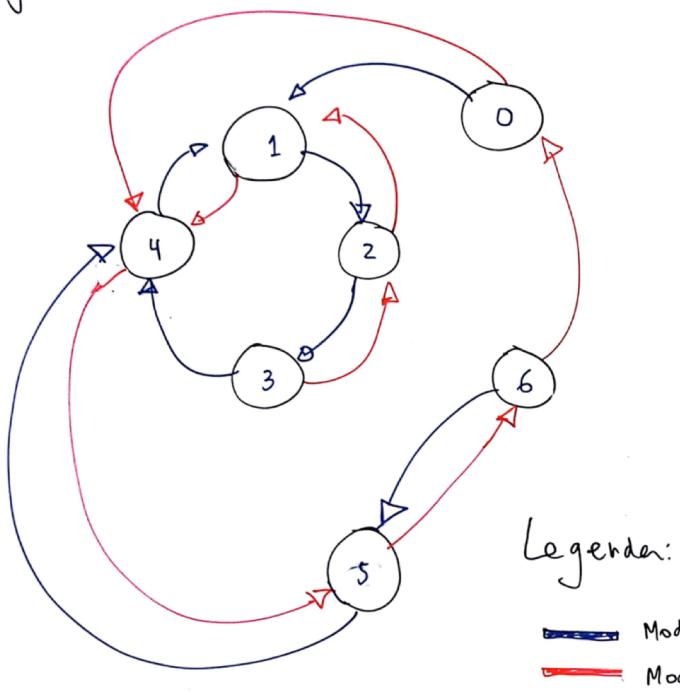
D_0 :

| $M\ q_2$ | 00 | 01 | 11 | 10 |
|----------|----|----|----|----|
| 00 | 1 | | | |
| 01 | 1 | X | 1 | |
| 11 | 1 | | X | |
| 10 | | | 1 | |

$$D_0 = \bar{M} \cdot \bar{q}_0 + \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + q_2 \cdot \bar{q}_1 \cdot \bar{q}_0$$

Outros projetos:

- Exemplo 3:



$$\begin{array}{c}
 M \cdot q_2 \cdot q_1 \cdot q_0 \rightarrow q_2 \cdot q_1 \cdot q_0 \\
 \hline
 0 \cdot 1 \cdot 1 \cdot 1 \rightarrow ?
 \end{array}
 \quad
 \begin{array}{c}
 q_2 \cdot q_1 \cdot q_0 \\
 \hline
 1 \cdot 0 \cdot 0 \\
 0 \cdot 1 \cdot 0
 \end{array}$$

$$D_2 = M \cdot \bar{q}_1 + \bar{M} \cdot q_2 \cdot q_0 + \bar{M} \cdot q_1 \cdot q_0 + \bar{M} \cdot q_2 \cdot q_1$$

$$\text{Mode}=0 \rightarrow D_2 = 0 \cdot \bar{q}_1 + 1 \cdot 1 \cdot 1 + \dots = 1$$

$$\text{Mode}=1 \rightarrow D_2 = 1 \cdot 0 + 0 \cdot q_2 \cdot q_0 + 0 \cdot q_1 \cdot q_0 + 0 \cdot q_2 \cdot q_1 = 0$$

$$D_4 = \bar{M} \cdot \bar{q}_2 \cdot \bar{q}_1 \cdot q_0 + \bar{M} \cdot \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + M \cdot q_2 \cdot q_0 + M \cdot q_1 \cdot q_0$$

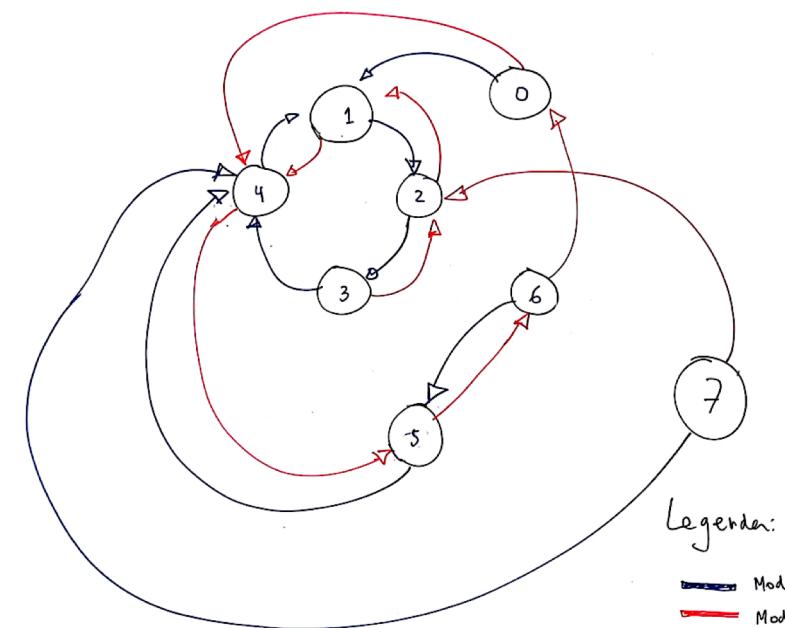
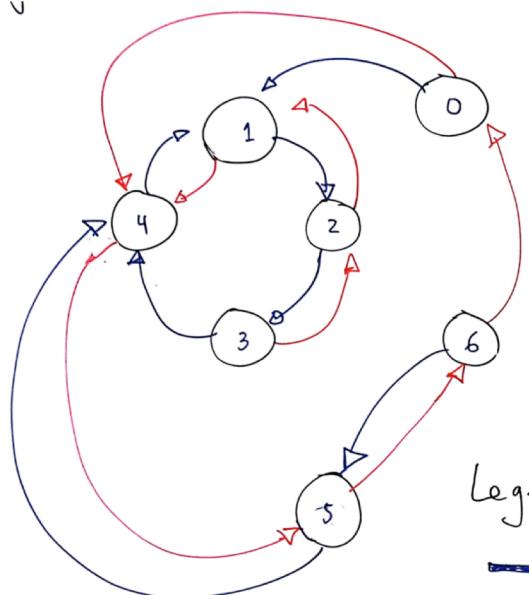
$$\text{Mode}=0 \rightarrow D_4 = \underbrace{1 \cdot \bar{1} \cdot \bar{1} \cdot 1}_0 + \underbrace{1 \cdot \bar{1} \cdot 1 \cdot \bar{1}}_0 + \underbrace{0 \cdot q_2 \cdot q_0}_0 + \underbrace{0 \cdot q_1 \cdot q_0}_0 = 0$$

$$\text{Mode}=1 \rightarrow D_4 = \underbrace{0 \cdot \bar{q}_2 \cdot \bar{q}_1 \cdot q_0}_0 + \underbrace{0 \cdot \bar{q}_2 \cdot q_1 \cdot \bar{q}_0}_0 + \underbrace{1 \cdot 1 \cdot 1}_1 + \dots = 1$$

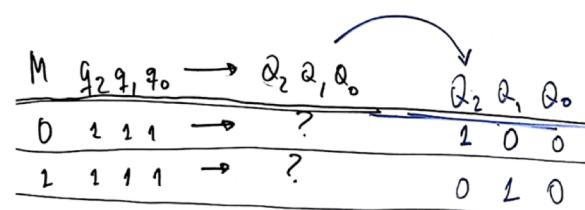
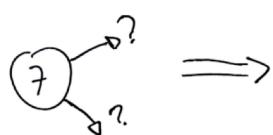
$$D_0 = \bar{M} \cdot \bar{q}_0 + \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + q_2 \cdot q_1 \cdot \bar{q}_0$$

$$M=0 \rightarrow D_0 = 1 \cdot 0 + \underbrace{0 \cdot q_1 \cdot \bar{q}_0}_0 + \underbrace{q_2 \cdot q_1 \cdot 0}_0 = 0$$

$$M=1 \rightarrow D_0 = 0 \cdot \bar{q}_0 + \underbrace{0 \cdot q_1 \cdot \bar{q}_0}_0 + \underbrace{q_2 \cdot q_1 \cdot 0}_0 = 0$$



$7 \rightarrow \text{Mode } 0 \rightarrow 100_{(2)} = 4_{(10)}$
 $7 \rightarrow \text{Mode } 1 \rightarrow 010_{(2)} = 2_{(10)}$



$$D_2 = M \cdot \bar{q}_1 + \bar{M} \cdot q_2 \cdot q_0 + \bar{M} \cdot q_1 \cdot q_0 + \bar{M} \cdot q_2 \cdot q_1$$

$$\text{Mode} = 0 \rightarrow D_2 = 0 \cdot \bar{q}_1 + 1 \cdot 1 \cdot 1 + \dots = 1$$

$$\text{Mode} = 1 \rightarrow D_2 = 1 \cdot 0 + 0 \cdot q_2 \cdot q_0 + 0 \cdot q_1 \cdot q_0 + 0 \cdot q_2 \cdot q_1 = 0$$

$$D_4 = \bar{M} \cdot \bar{q}_2 \cdot \bar{q}_1 \cdot q_0 + \bar{M} \cdot \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + M \cdot q_2 \cdot q_0 + M \cdot q_1 \cdot q_0$$

$$\text{Mode} = 0 \rightarrow D_4 = \underbrace{1 \cdot \bar{1} \cdot \bar{1} \cdot 1}_0 + \underbrace{1 \cdot \bar{1} \cdot 1 \cdot \bar{1}}_0 + \underbrace{0 \cdot q_2 \cdot q_0}_0 + \underbrace{0 \cdot q_1 \cdot q_0}_0 = 0$$

$$\text{Mode} = 1 \rightarrow D_4 = \underbrace{0 \cdot \bar{q}_2 \cdot \bar{q}_1 \cdot q_0}_0 + \underbrace{0 \cdot \bar{q}_2 \cdot q_1 \cdot \bar{q}_0}_0 + \underbrace{1 \cdot 1 \cdot 1}_1 + \dots = 1$$

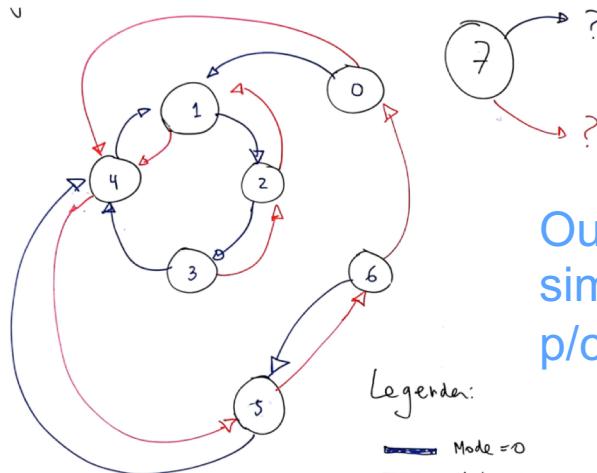
$$D_0 = \bar{M} \cdot \bar{q}_0 + \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + q_2 \cdot q_1 \cdot \bar{q}_0$$

$$M = 0 \rightarrow D_0 = 1 \cdot 0 + \underbrace{0 \cdot q_1 \cdot \bar{q}_0}_0 + \underbrace{q_2 \cdot q_1 \cdot 0}_0 = 0$$

$$M = 1 \rightarrow D_0 = 0 \cdot \bar{q}_0 + \underbrace{0 \cdot q_1 \cdot \bar{q}_0}_0 + \underbrace{q_2 \cdot q_1 \cdot 0}_0 = 0$$

Outros projetos:

- Exemplo 3:



| Ref. | (M) | Mode | $q(t)$ | $\rightarrow Q(t+1)$ | D_2 | D_1 | D_0 |
|------|-----|------|--------|----------------------|-------|-------|-------|
| 0 | 0 | 0 | 0 0 0 | 0 0 1 | 0 0 1 | 0 0 1 | 1 |
| 1 | 0 | 0 | 0 0 1 | 0 1 0 | 0 1 0 | 0 1 0 | 0 |
| 2 | 0 | 0 | 0 1 0 | 0 1 1 | 0 1 1 | 0 1 1 | 0 |
| 3 | 0 | 0 | 0 1 1 | 1 0 0 | 1 0 0 | 1 0 0 | 0 |
| 4 | 0 | 1 | 1 0 0 | 0 0 1 | 0 0 1 | 0 0 1 | 1 |
| 5 | 0 | 1 | 1 0 1 | 1 0 0 | 1 0 0 | 1 0 0 | 0 |
| 6 | 0 | 1 | 1 1 0 | 1 0 1 | 1 0 1 | 1 0 1 | 1 |
| 7 | 0 | 1 | 1 1 1 | X X X | X X X | X X X | X |
| 8 | 1 | 0 | 0 0 0 | 1 0 0 | 1 0 0 | 1 0 0 | |
| 9 | 1 | 0 | 0 0 1 | 1 0 0 | 1 0 0 | 1 0 0 | |
| 10 | 2 | 0 | 0 1 0 | 0 0 1 | 0 0 1 | 0 0 1 | |
| 11 | 1 | 0 | 0 1 1 | 0 1 0 | 0 1 0 | 0 1 0 | |
| 12 | 1 | 0 | 1 0 0 | 1 0 1 | 1 0 1 | 1 0 1 | |
| 13 | 1 | 0 | 1 0 1 | 1 1 0 | 1 1 0 | 1 1 0 | |
| 14 | 1 | 0 | 1 1 0 | 0 0 0 | 0 0 0 | 0 0 0 | |
| 15 | 1 | 1 | 1 1 1 | X X X | X X X | X X X | X |

Outra solução + simples p/circuito?

D_2 :

| $M\bar{q}_2$ | q_1q_0 | 00 | 01 | 11 | 10 |
|--------------|----------|----|----|----|----|
| 00 | 1 | | | | |
| 01 | 1 | X | 1 | | |
| 11 | 1 | 1 | X | | |
| 10 | 1 | 1 | | | |

$$D_2 = M \cdot \bar{q}_1 + \bar{M} \cdot q_2 \cdot \bar{q}_0 + \bar{M} \cdot q_1 \cdot q_0 + \bar{M} \cdot q_2 \cdot q_1 \quad \swarrow$$

D_1 :

| $M\bar{q}_2$ | q_1q_0 | 00 | 01 | 11 | 10 |
|--------------|----------|----|----|----|----|
| 00 | 1 | 1 | | 1 | |
| 01 | 1 | X | | | |
| 11 | 1 | 1 | X | | |
| 10 | 1 | | | 1 | |

D_0 :

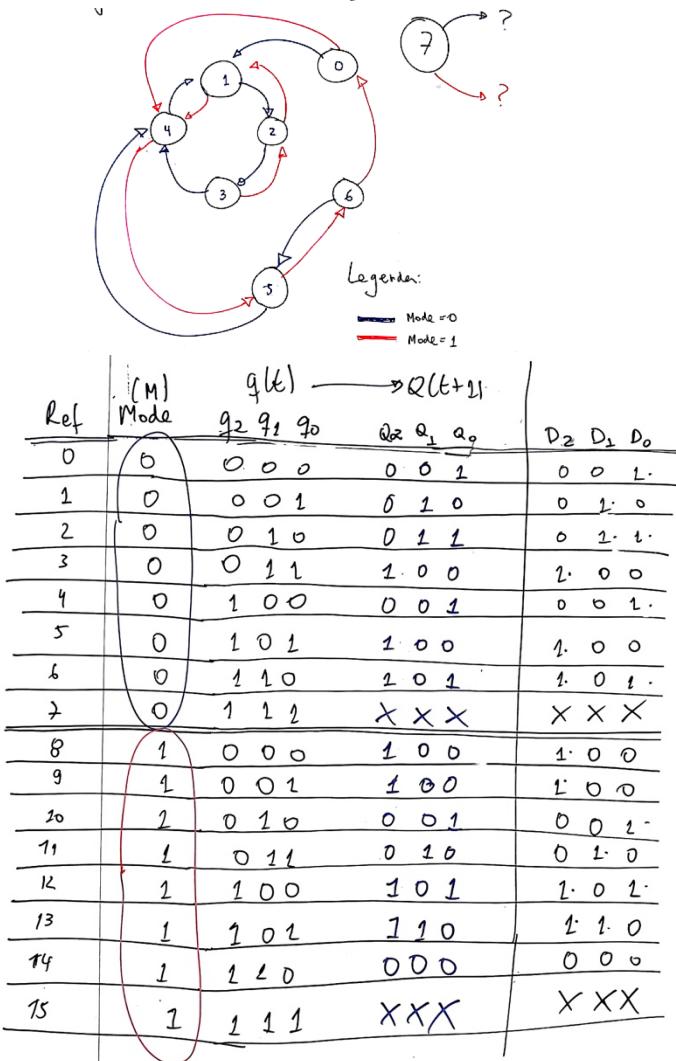
| $M\bar{q}_2$ | q_1q_0 | 00 | 01 | 11 | 10 |
|--------------|----------|----|----|----|----|
| 00 | 1 | 1 | | | |
| 01 | 1 | X | | | |
| 11 | 1 | 1 | X | | |
| 10 | 1 | | | 1 | |

$$D_0 = \bar{M} \cdot \bar{q}_0 + \bar{q}_2 \cdot q_1 \cdot \bar{q}_0 + q_2 \cdot \bar{q}_1 \cdot \bar{q}_0 \quad \searrow$$

$$D_1 = \underbrace{\bar{M} \cdot \bar{q}_2 \cdot \bar{q}_1 \cdot q_0 + \bar{M} \cdot \bar{q}_2 \cdot q_1 \cdot \bar{q}_0}_{\bar{M} \cdot \bar{q}_2 (q_1 \oplus q_0)} + M \cdot q_2 \cdot q_0 + M \cdot q_1 \cdot q_0$$

Outros projetos:

- Exemplo₃:

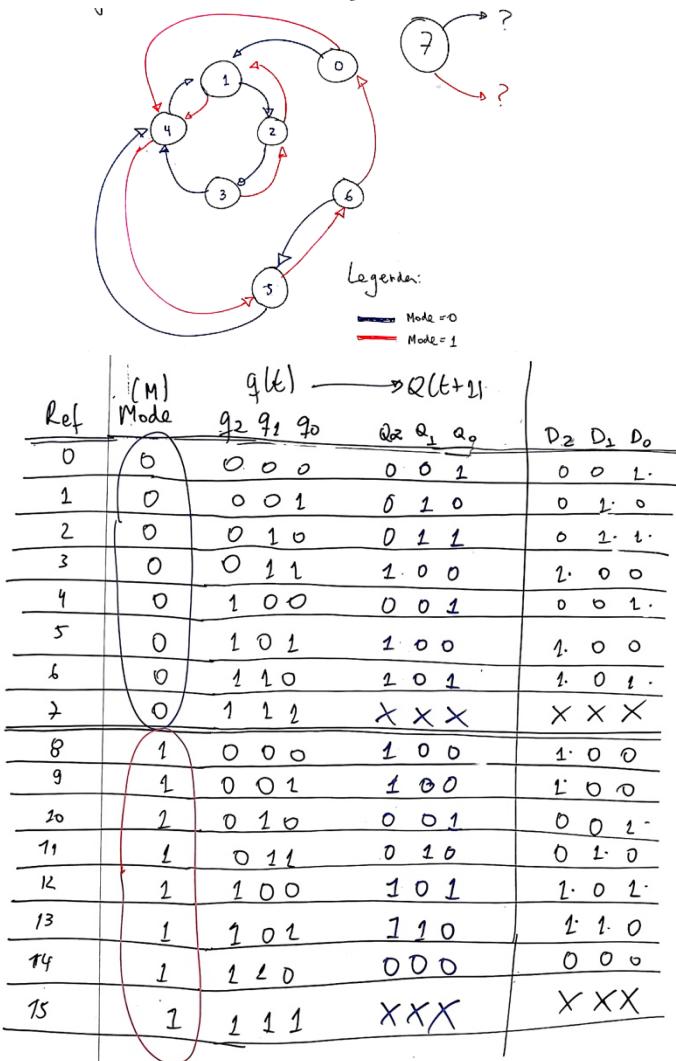


Outra solução + simples: Uso de MUXes:

| <u>Ref'</u> | <u>Ref</u> | <u>M</u> | <u>$g_2\ g_1\ g_0$</u> | <u>D_2</u> |
|-------------|------------|----------|-----------------------------------|-------------------------|
| 0 | 0 | 0 | 0 0 0 | 0 - $x_0 = M$ |
| 1 | 1 | 0 | 0 0 1 | 0 - $x_1 = M$ |
| 2 | 2 | 0 | 0 1 0 | 0 - $x_2 = 0$ |
| 3 | 3 | 0 | 0 1 1 | 1 - $x_3 = \bar{M}$ |
| 4 | 4 | 0 | 1 0 0 | 0 - $x_4 = M$ |
| 5 | 5 | 0 | 1 0 1 | 1 - $x_5 = 1$ |
| 6 | 6 | 0 | 1 1 0 | 1 - $x_6 = \bar{M}$ |
| 7 | 7 | 0 | 1 1 1 | 0 - $x_7 = 0$ |
| 8 | 8 | 1 | 0 0 0 | 1 - |
| 9 | 9 | 1 | 0 0 1 | 1 - |
| 10 | 10 | 1 | 0 1 0 | 0 - |
| 11 | 11 | 1 | 0 1 1 | 0 - |
| 12 | 12 | 1 | 1 0 0 | 1 - |
| 13 | 13 | 1 | 1 0 1 | 1 - |
| 14 | 14 | 1 | 1 1 0 | 0 - |
| 15 | 15 | 1 | 1 1 1 | 0 - |

Outros projetos:

- Exemplo₃:

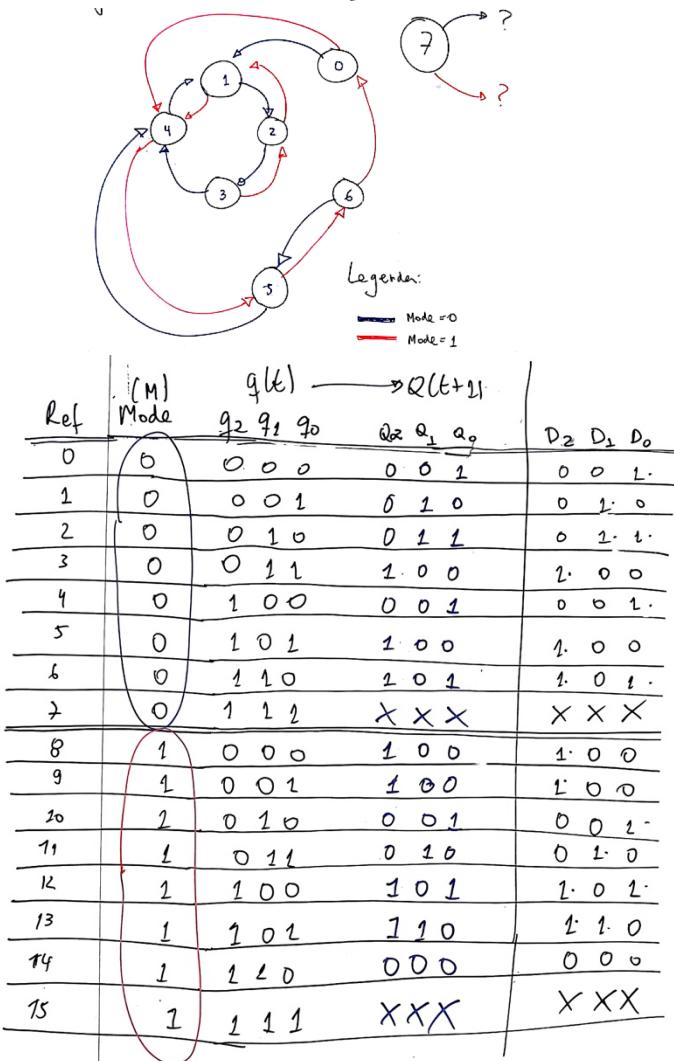


Outra solução + simples: Uso de MUXes:

| R _{f1} | R _{f2} | M | q_2 | q_1 | q_0 | D ₁ |
|-----------------|-----------------|---|-------|-------|-------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | $X_0 = 0$ |
| 1 | 1 | 0 | 0 | 0 | 1 | $X_1 = \bar{M}$ |
| 2 | 2 | 0 | 0 | 1 | 0 | $X_2 = \bar{M}$ |
| 3 | 3 | 0 | 0 | 1 | 1 | $X_3 = M$ |
| 4 | 4 | 0 | 1 | 0 | 0 | $X_4 = 0$ |
| 5 | 5 | 0 | 1 | 0 | 1 | $X_5 = M$ |
| 6 | 6 | 0 | 1 | 1 | 0 | $X_6 = 0$ |
| 7 | 7 | 0 | 1 | 1 | 1 | $X_7 = 0$ |
| 0 | 8 | 1 | 0 | 0 | 0 | |
| 1 | 9 | 1 | 0 | 0 | 1 | |
| 2 | 10 | 1 | 0 | 1 | 0 | |
| 3 | 11 | 1 | 0 | 1 | 1 | |
| 4 | 12 | 1 | 1 | 0 | 0 | |
| 5 | 13 | 1 | 1 | 0 | 1 | |
| 6 | 14 | 1 | 1 | 1 | 0 | |
| 7 | 15 | 1 | 1 | 1 | 1 | |

Outros projetos:

- Exemplo₃:



Outra solução + simples: Uso de MUXes:

| Ref' | Ref | M | q_2 | q_1 | q_0 | D_0 |
|------|-----|---|-------|-------|-------|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | $1 - x_0 = \bar{M}$ |
| 1 | 1 | 0 | 0 | 0 | 1 | $x_1 = 0$ |
| 2 | 2 | 0 | 0 | 1 | 0 | $x_2 = 1$ |
| 3 | 3 | 0 | 0 | 1 | 1 | $x_3 = 0$ |
| 4 | 4 | 0 | 1 | 0 | 0 | $x_4 = 1$ |
| 5 | 5 | 0 | 1 | 0 | 1 | $x_5 = 0$ |
| 6 | 6 | 0 | 1 | 1 | 0 | $x_6 = \bar{M}$ |
| 7 | 7 | 0 | 1 | 1 | 1 | $x_7 = 0$ |
| 8 | 0 | 1 | 0 | 0 | 0 | |
| 9 | 1 | 0 | 0 | 1 | 0 | |
| 10 | 2 | 1 | 0 | 1 | 1 | |
| 11 | 1 | 1 | 0 | 1 | 0 | |
| 12 | 2 | 1 | 1 | 0 | 1 | |
| 13 | 1 | 1 | 1 | 0 | 0 | |
| 14 | 1 | 1 | 1 | 1 | 0 | |
| 15 | 1 | 1 | 1 | 1 | 1 | |