本周汇报

1.13-1.19

◎ 机器学习
Regression

处理数据的方式

AdaGrad优化算法

还需学习下面的视频

花书：线性代数 两个视频

下周继续学习视频第一周内容

Terminal Help hw1.py - Visual Studio Code

hw1.py

D: > research > 李宏毅 > hw1 > hw1.py > ...

```python
# 导入相关库
import sys
import pandas as pd
import numpy as np

# 读入数据
data = pd.read_csv('./train.csv', encoding = 'big5')

# 数据预处理
data = data.iloc[:, 3:]
data[data == 'NR'] = 0
```

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL

```
See the caveats in the documentation: https://pandas.pydata.org/pandas-do
  self._where(-key, value, inplace=True)
['id', 'value']
['id_0', 7.0]
['id_1', 18.0]
['id_2', 24.0]
['id_3', 8.0]
['id_4', 27.0]
['id_5', 22.0]
['id_6', 24.0]
['id_7', 30.0]
['id_8', 17.0]
['id_9', 60.0]
['id_10', 12.0]
['id_11', 9.0]
['id_12', 63.0]
['id_13', 53.0]
['id_14', 22.0]
['id_15', 12.0]
['id_16', 32.0]
['id_17', 67.0]
['id_18', 0.0]
['id_19', 17.0]
['id_20', 42.0]
['id_21', 72.0]
['id_22', 9.0]
```

◎ Vivado

完成了：

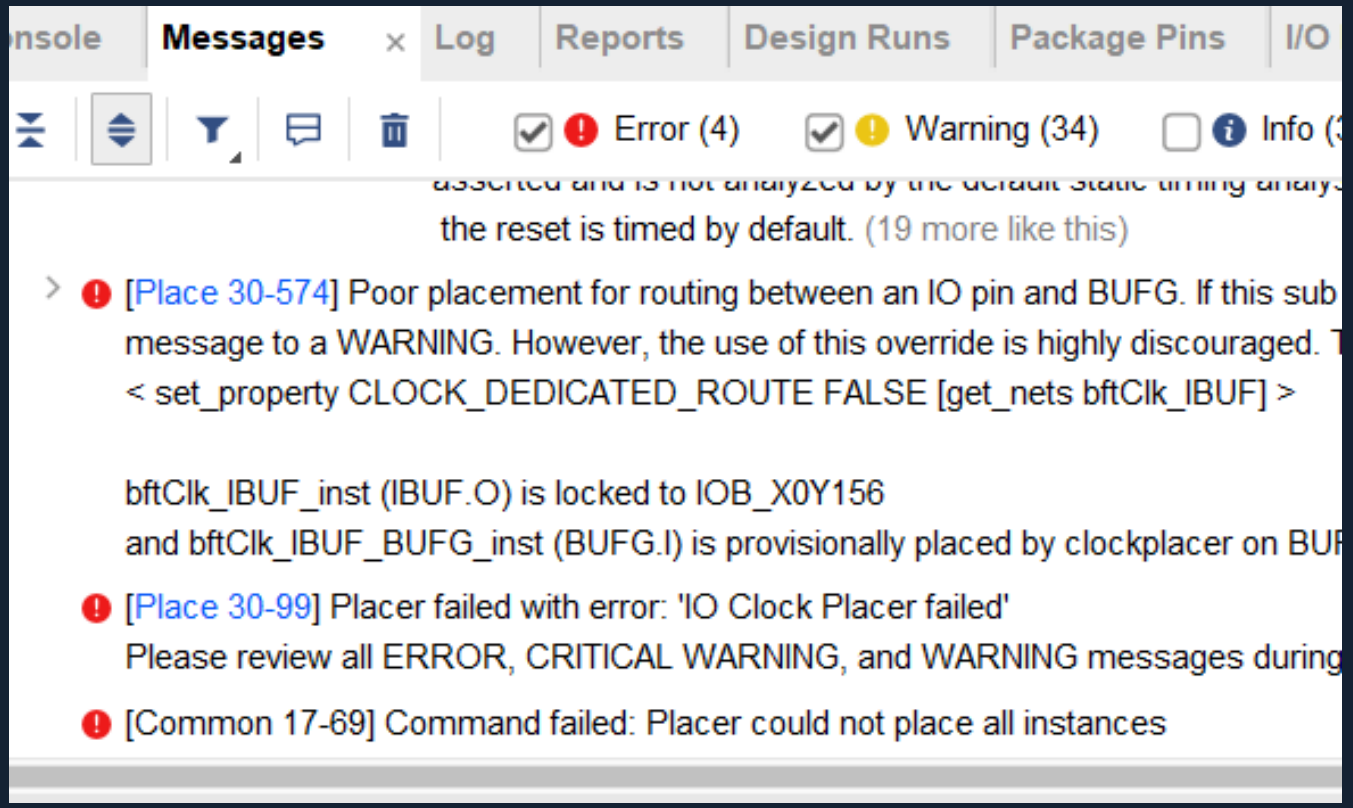
ug888 ug892

I/O Planning:

ug 899 ug471 原理图

Vivado HLS:

ug 998 ug 871 ug902



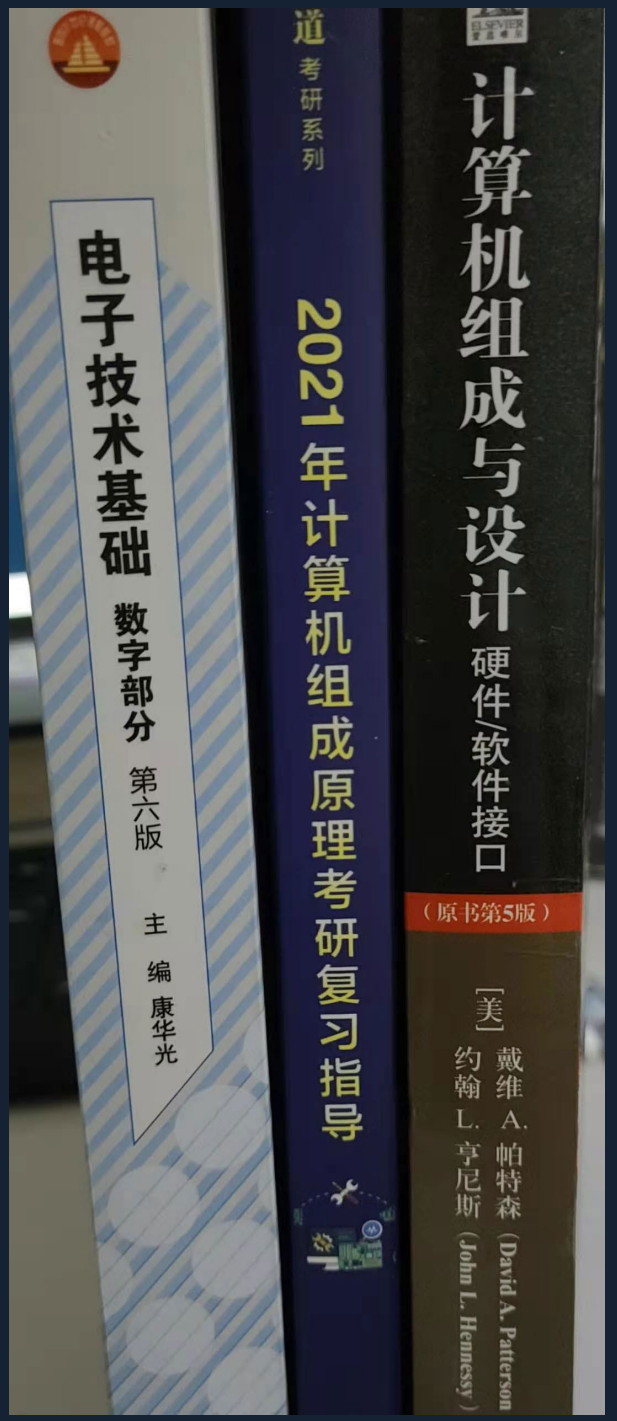
◎ 数电 & 计组

数电完成至3.1

下周至少完成至4.4之前

计组：第一章

下周至少完成第二章



◎ C\Python\Verilog

Verilog:

hdlbits.01xz.net

C:

bilibili.com/video/BV14J4

1U7hj

+ *C Primer Plus*

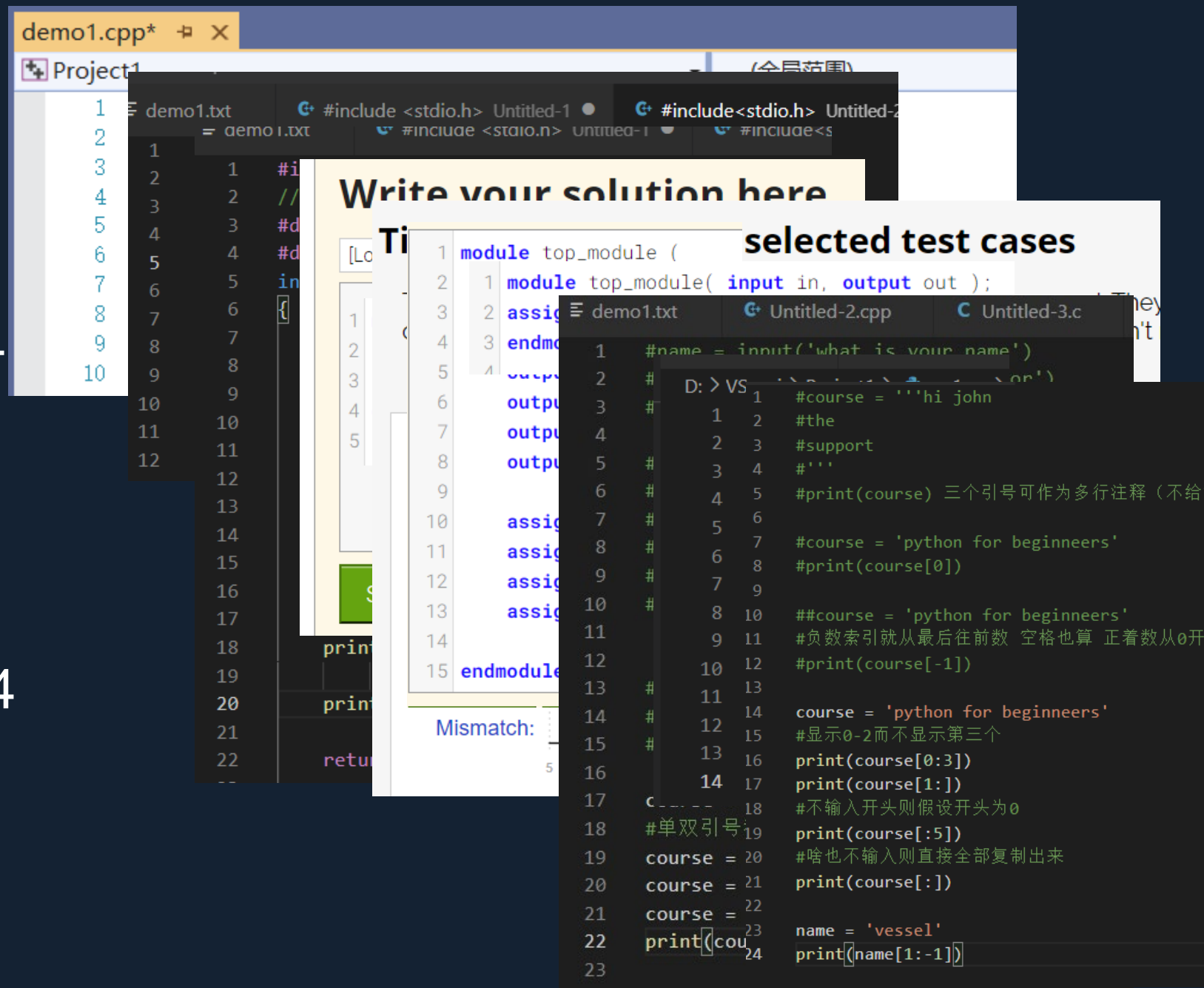
Python:

bilibili.com/video/BV1qE4

11d7Zx?p=10

+ *Python Crash Course*

2nd Edition



◎ 时间分配

课题与求职 5 : 2

- 机器学习

重合部分：

- 数电 & Verilog
- 体系结构
- C & Python
- FPGA

IC：

- SystemVerilog
- UVM
- Tcl
- Linux
- EDA Tools
- …