

WUST

学习总结



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目录 CONTENT

03 01 02 论文 视频 实验

PART

01

题目: An Efficient Hardware Accelerator for Structur ed Sparse Convolutional Neural Networks on FPGAs

[THIS MANUSCIRPT IS FOR IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRA TION (VLSI) SYSTEMS]

01/Paper

CONV layer

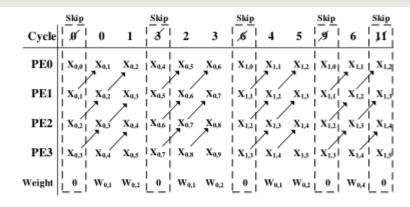


Fig. 3. Sparse wise dataflow for CONV layers. When weights equal to zero, the cycles of processing MACs will be skipped by controlling the upper bound of corresponding loop illustrated in Algorithm [2]

FC layer

Skip				Skip			Skip		Skip		
Cycle	.0′	0	1	3	A	2	,6	3	,8′	,9	<u></u>
PE0	0	$\mathbf{W}_{0,1}$	$\mathbf{W}_{0,2}$	0	0	$\mathbf{W}_{0,5}$	0	$\mathbf{W}_{0,7}$	0	0	
PE1	0	$\mathbf{W}_{1,1}$	$\mathbf{W}_{1,2}$	0	0	$\mathbf{W}_{1,5}$	0	$\mathbf{W}_{1,7}$	0	0	
PE2	0	$\mathbf{W}_{2,1}$	$\mathbf{W}_{2,2}$	0	0	$\mathbf{W}_{2,5}$	0	$\mathbf{W}_{2,7}$	0	0	
PE3	0	$\mathbf{W}_{3,1}$	$\mathbf{W}_{3,2}$	0	٥į	$\mathbf{W}_{3,5}$	0	$\mathbf{W}_{3,7}$	0	0	
Input	X _{0,1}	X _{1,1}	$X_{2,1}$	X3,1	X _{4,1}	$\mathbf{X}_{5,1}$	X _{6,1}	$X_{7,1}$	X _{8,1}	X _{9,1}	

Fig. 4. Execution pattern of FC layers. Similar to CONV layers, the cycles of processing MACs will be skipped when weights equal to zero.

01/ Paper

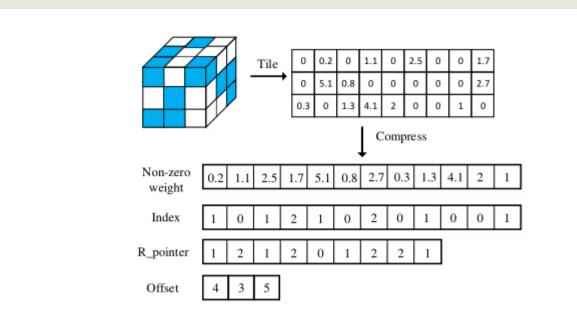


Fig. 7. Index representation of weights in CONV layers. The Index represents the number of pruned weights between two nonzero weights. The r_pointer represents the number of remaining weights in each row. The Offset shows the remaining weights in each channel of one kernel.

01/ Paper

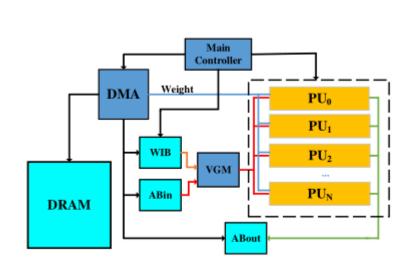


Fig. 6. Accelerator Architecture. The DRAM is implemented with Double Data Rate Random Access Memory in Processing System on Xilinx FPGA.

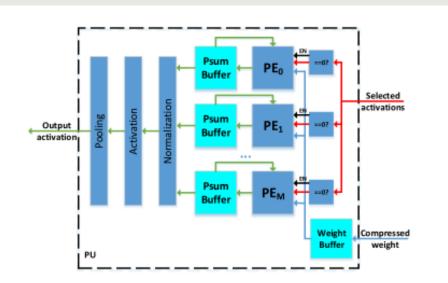


Fig. 10. The architecture of the PU. The PU processes all operations in CNNs. It contains M homogeneous PEs, and the number of PEs can be configured according to the CNN model and FPGA platform.

01/ Paper

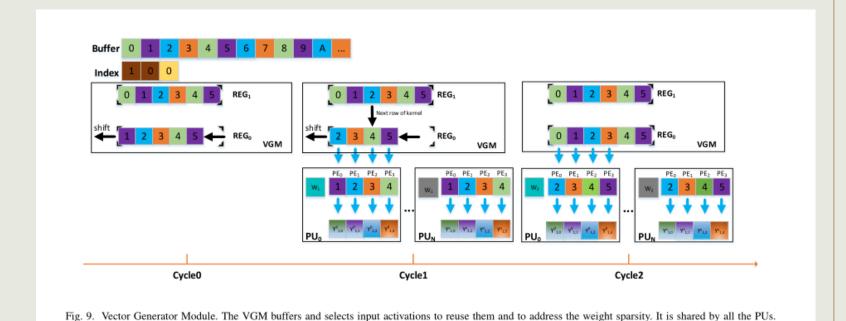


Fig. 10. The architecture of the PU. The PU processes all operations in CNNs. It contains M homogeneous PEs, and the number of PEs can be configured according to the CNN model and FPGA platform.

Output Selected Selected activations Psum Buffer PE1 Selected activations Psum Buffer PE1 Selected activations Psum Buffer PEM Selected activations

Conclusion:

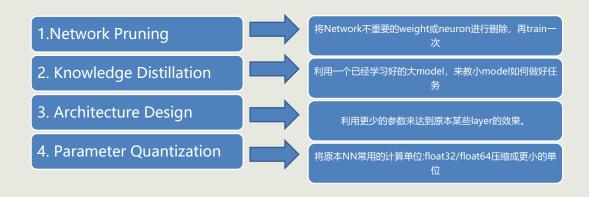
our implementation could achieve 987imag/s and 48imag/s performance for AlexNet and VGG-16 on Xilinx ZCU102, respectively, which provides $1.5 \times$ to $6.7 \times$ speedup and $2.0 \times$ to $6.2 \times$ energy-efficiency over pre-vious CNN FPGA accelerators

PART

02

● 网络压缩

02/ Video



问题: 1.训练的剪枝是否和推理的剪枝方法相同, train时候的剪枝可以剪去 neuron和weight, 推理的时候本文只对weight中的0做了处理。
2. 上篇论文中所做的只是在计算时进行了优化, 并没有对网络进行实质性的改变。