周学习总结
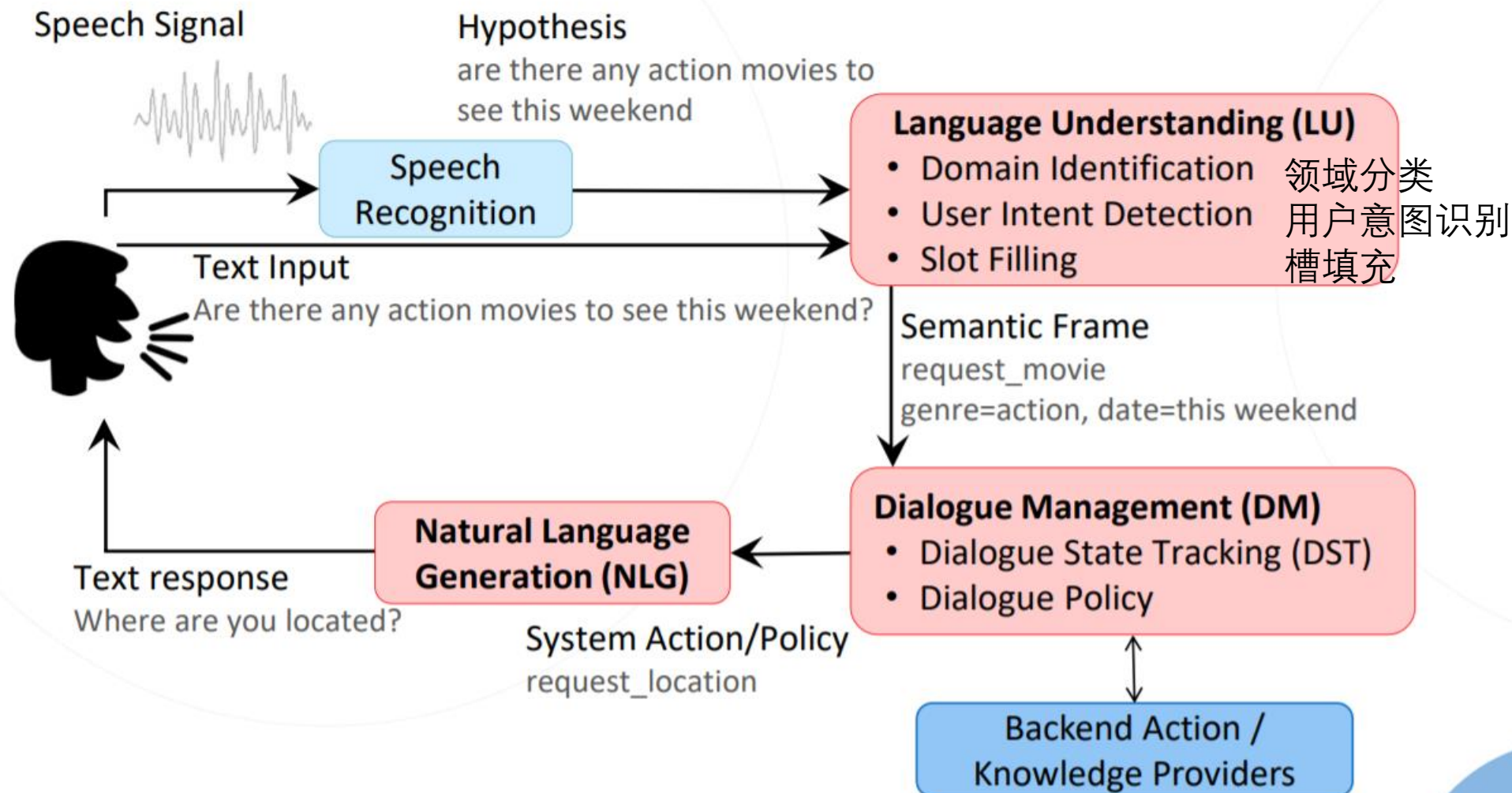
许典

李宏毅视频

- 完成Word Embedding，运行实验RNN(LSTM)，导出模型
  - 实验内容：语句分类，给定一个句子，判断它有没有恶意。

Task-Oriented Dialogue System (Young, 2000)

Speech Signal

Hypothesis
are there any action movies to
see this weekend

Speech Recognition

Text Input
Are there any action movies to see this weekend?

Language Understanding (LU)
- Domain Identification 领域分类
- User Intent Detection 用户意图识别
- Slot Filling 槽填充

Semantic Frame
request_movie
genre=action, date=this weekend

Dialogue Management (DM)
- Dialogue State Tracking (DST)
- Dialogue Policy

Natural Language Generation (NLG)

Text response
Where are you located?

System Action/Policy
request_location

Backend Action / Knowledge Providers

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2. Intent Detection
Requires Predefined Schema

User

find a good eating place for taiwanese food
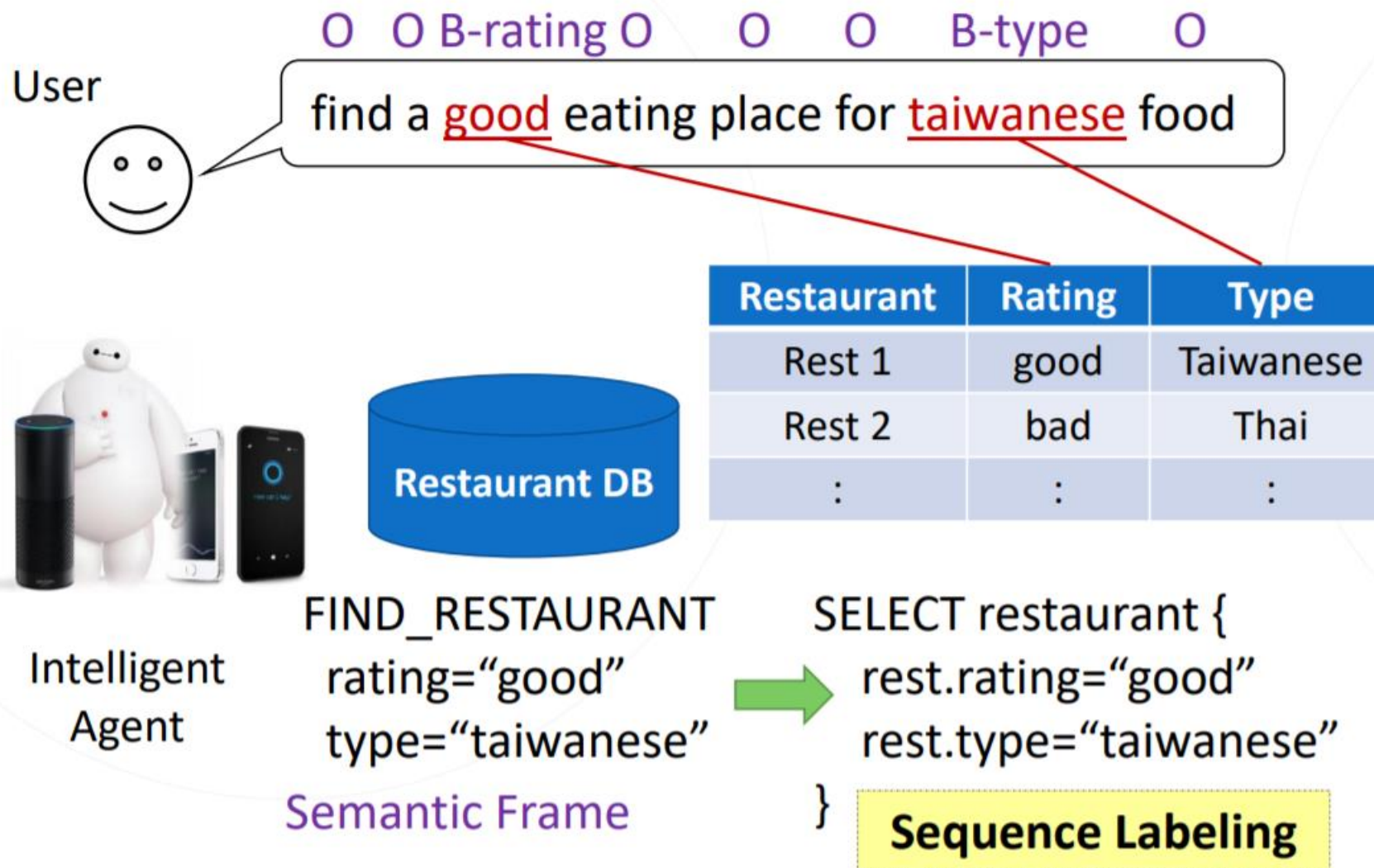
Intelligent
Agent

Restaurant DB

FIND_RESTAURANT
FIND_PRICE
FIND_TYPE
:

Classification!

3. Slot Filling
Requires Predefined Schema

| | O | O | B-rating | O | O | O | B-type | O |

User: find a good eating place for taiwanese food

Restaurant	Rating	Type
Rest 1	good	Taiwanese
Rest 2	bad	Thai
:	:	:

Restaurant DB

Intelligent Agent

FIND_RESTAURANT
rating="good"
type="taiwanese"

Semantic Frame

SELECT restaurant {
   rest.rating="good"
   rest.type="taiwanese"
}

Sequence Labeling

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LU Evaluation

- Metrics
    - Sub-sentence-level: intent accuracy, slot F1
    - Sentence-level: whole frame accuracy

发现缺的一些知识点

- CRF（条件随机场）
- HMM（隐马尔可夫模型）:了解了一些
- Reinforcement Learning（强化学习）

FPGA方面

- 注册了Xilinx Developer，看了一些基础的Vitis、Vitis AI以及自适应计算的基础概念

Hardware Acceleration: General Guidelines

Rules to remember before you move a function for hardware acceleration:

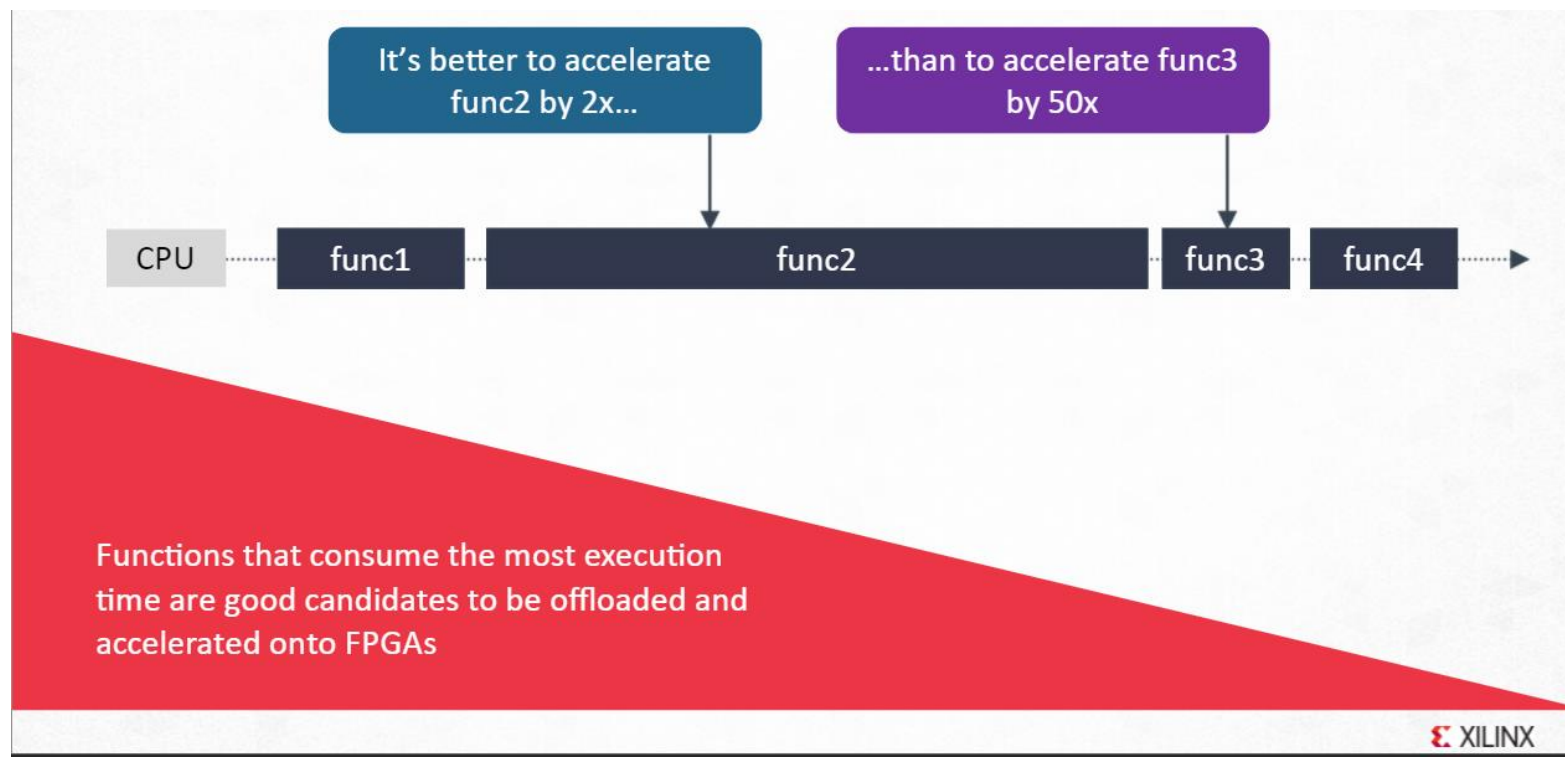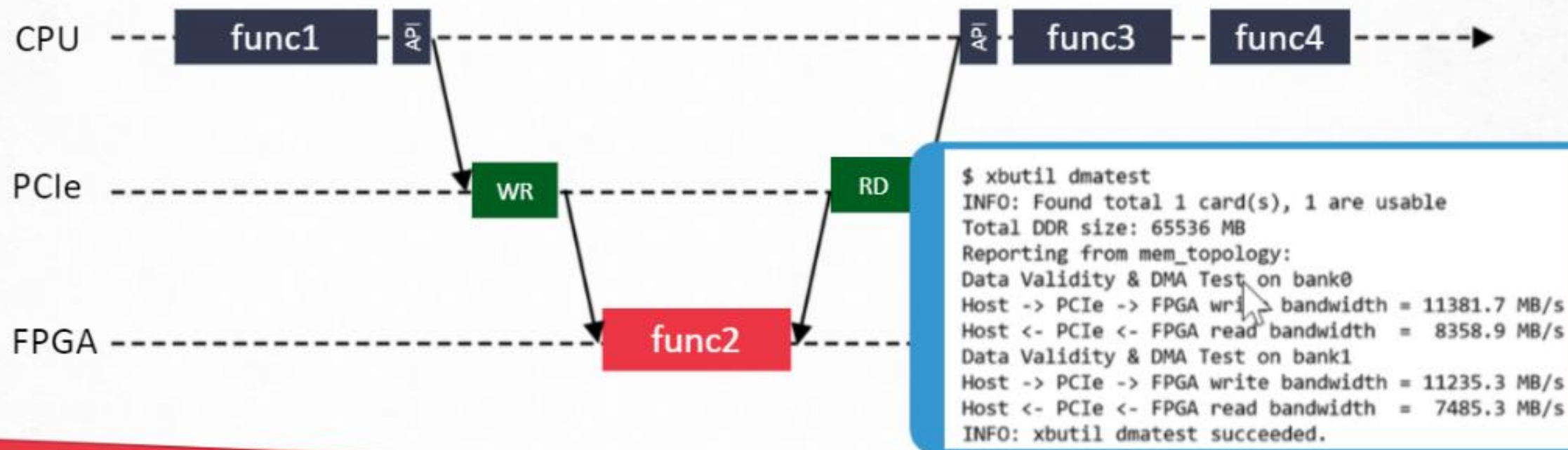| Rule 1	Rule 2	Rule 3	Rule 4
Remember Amdahl's Law 阿姆达尔定律	Target Large, Compute-bound Tasks	Know Your Ceiling	Think Throughput, Not Only Latency

Click each rule to learn more

XILINX

阿姆达尔定律

- 对系统某部分加速时，其对系统整体影响取决于该部分重要性和加速程度。
- 要想显著加速整个系统，必须提升全系统中相当大的部分的速度。

Rule 3: Know Your Ceiling


```
$ xbutil dmatest
INFO: Found total 1 card(s), 1 are usable
Total DDR size: 65536 MB
Reporting from mem_topology:
Data Validity & DMA Test on bank0
Host -> PCIe -> FPGA write bandwidth = 11381.7 MB/s
Host <- PCIe <- FPGA read bandwidth  =  8358.9 MB/s
Data Validity & DMA Test on bank1
Host -> PCIe -> FPGA write bandwidth = 11235.3 MB/s
Host <- PCIe <- FPGA read bandwidth  =  7485.3 MB/s
INFO: xbutil dmatest succeeded.
```

Run DMA tests up front (xbutil dma test) to measure the effective throughput of PCIe interface transfers and thereby determine the upper bound of the acceleration potential

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