SYNOPSYS®

DesignWare® Cores USB 3.0 PHY-Controller Integration Guide

Application Note

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Version 3.10a

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Revision History

Date	Release	Description
August 2019	3.10a	Updated: ■ Figure 1-2 (“USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Device Controller – USB 3.0 PIPE Interface Signals”) ■ Figure 1-6 (“USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Host Controller – USB 3.0 PIPE Interface Signals”) ■ Figure 1-10 (“USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with DRD Controller – USB 3.0 PIPE Interface Signals”) ■ Figure 1-14 (“USB 3.0 PHY in USB 2.0 Mode with Device Controller – USB 3.0 PIPE Interface Signals”) ■ Figure 1-18 (“USB 3.0 PHY in USB 2.0 Mode with Host Controller – USB 3.0 PIPE Interface Signals”) ■ Figure 1-22 (“USB 3.0 PHY in USB 2.0 Mode with DRD Controller – USB 3.0 PIPE Interface Signals”) ■ Figure 1-26 (“USB 3.0 PHY in USB 3.0 Mode (SS only) – USB 3.0 PIPE Interface Signals”) ■ Notes after the following figures: - Figure 1-14 (“USB 3.0 PHY in USB 2.0 Mode with Device Controller – USB 3.0 PIPE Interface Signals”) - Figure 1-18 (“USB 3.0 PHY in USB 2.0 Mode with Host Controller – USB 3.0 PIPE Interface Signals”) - Figure 1-22 (“USB 3.0 PHY in USB 2.0 Mode with DRD Controller – USB 3.0 PIPE Interface Signals”)

(Continued)

Date	Release	Description
January 2019	3.00a	Updated: ■ Changed all references of HS mode to USB 2.0 mode ■ Figures 1-1 to 1-25 inclusive ■ Notes after following figures: - Figure 1-3 on page 8 - Figure 1-11 on page 15 - Figure 1-15 on page 19 - Figure 1-23 on page 26 Removed: ■ OTG DRD sections: - "Integrating USB 3.0 PHY in USB 3.0 Mode (SS and HS only) with OTG DRD Controller" - "Integrating USB 3.0 PHY in USB 3.0 Mode (HS only) with OTG DRD Controller" ■ Subsections on ADP signals:
May 2015	2.00a	Added Non-OTG DRD ■ Section 1.4, "Integrating USB 3.0 PHY in USB 3.0 Mode (SS and HS only) with Non-OTG DRD Controller" ■ Section 1.8, "Integrating USB 3.0 PHY in USB 3.0 Mode (HS only) with Non-OTG DRD Controller" ■ Updated the application note template

Reference Documents

The following reference documents are used in this application note:

- PHY Interface for the PCI Express™, SATA, and USB 3.0 Architectures, Version 4.00, Intel Corp.

  http://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures.pdf

- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Revision 1.05, Intel Corp., March 29, 2001

  http://www.intel.com/technology/usb/download/2_0_Xcvr_macrocell_1_05.pdf

- UTMI+ Specification, Revision 1.0, ULPI Working Group, February 25, 2004

  http://www.ulpi.org/ (may require registration)

- UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, ULPI Working Group, October 20, 2004

  http://www.ulpi.org/ (may require registration)

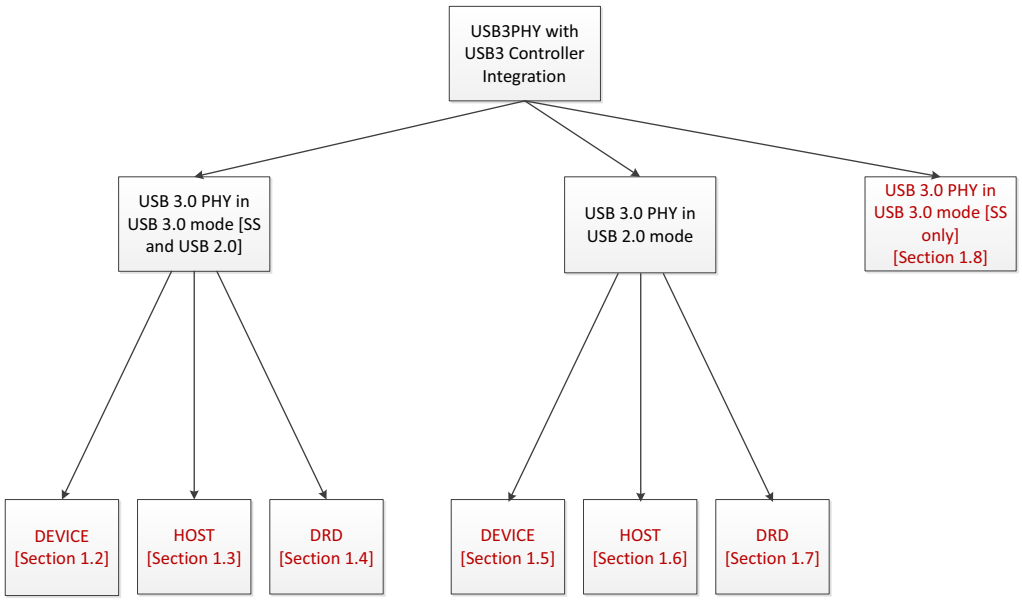
Integrating DWC USB 3.0 PHY with USB 3.0 Controller

Note This application note pertains to 3.30b version of the *DesignWare® Cores USB 3.0 Controller*. There may be variations in signal, parameter, register names, and coreConsultant GUI depending on the DWC_usb3 controller version. See the DWC_usb3 documentation for up-to-date information pertaining to your version of the product.

1.1 Introduction

This application note describes the system-level and IP connectivity between the Synopsys DesignWare USB 3.0 PHY and the Synopsys DesignWare USB 3.0 Controller. The sections in this application note will show how to connect the PHY and the controller for specific configurations as shown in Figure 1-1. The USB 3.0 PHY under discussion is SuperSpeed, and high-speed capable.

Figure 1-1 Integration Modes of USB 3.0 PHY with USB 3.0 Controller



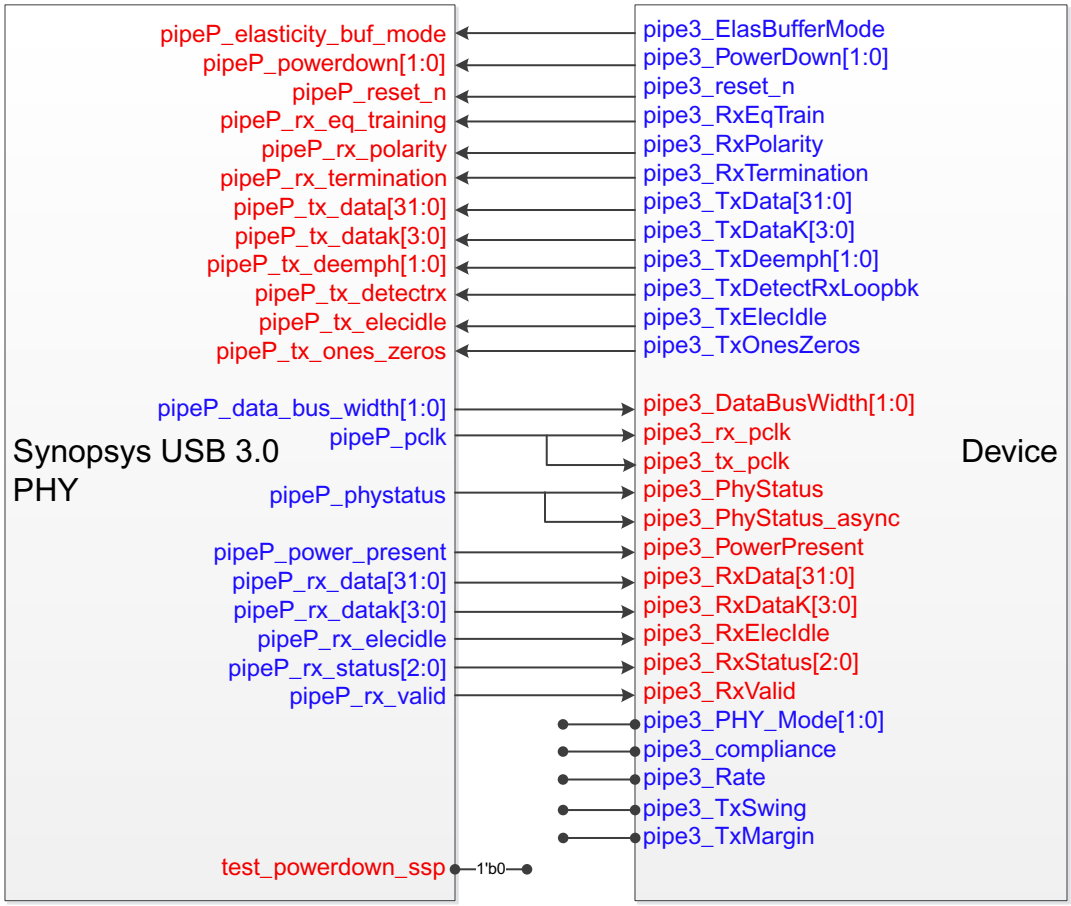
1.2 Integrating USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Device Controller

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals and miscellaneous signals.

1.2.1 USB 3.0 PIPE Signals

Figure 1-2 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 device controller.

Figure 1-2 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Device Controller – USB 3.0 PIPE Interface Signals

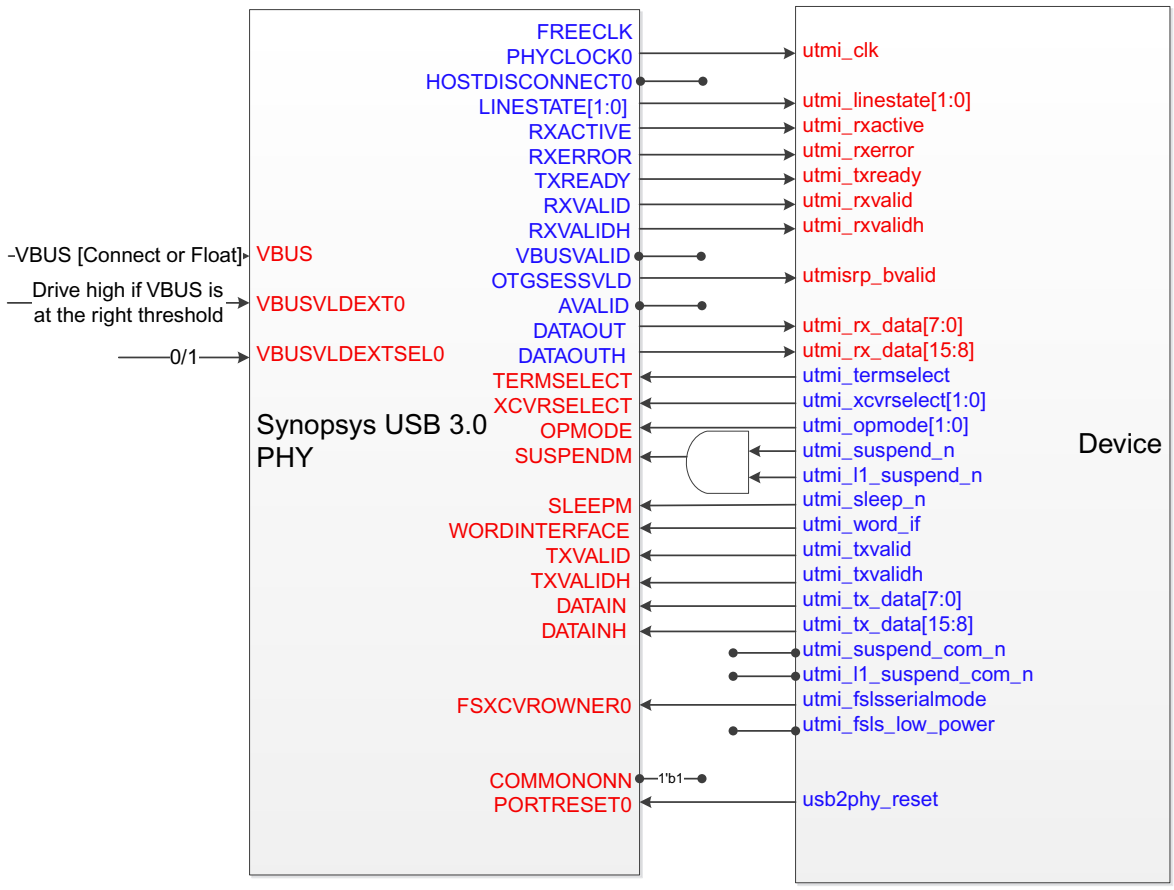


Note The controller outputs pipe3_PHY_Mode[1:0], pipe3_compliance and pipe3_Rate are hard wired to the USB 3.0 values. For more information, refer to *DesignWare Cores USB 3.0 Controller Databook*. The corresponding signals are not implemented in the USB 3.0 PHY.

1.2.2 USB 3.0 PHY UTMI Signals

Figure 1-3 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 device controller.

Figure 1-3 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Device Controller – USB 3.0 UTMI Interface Signals



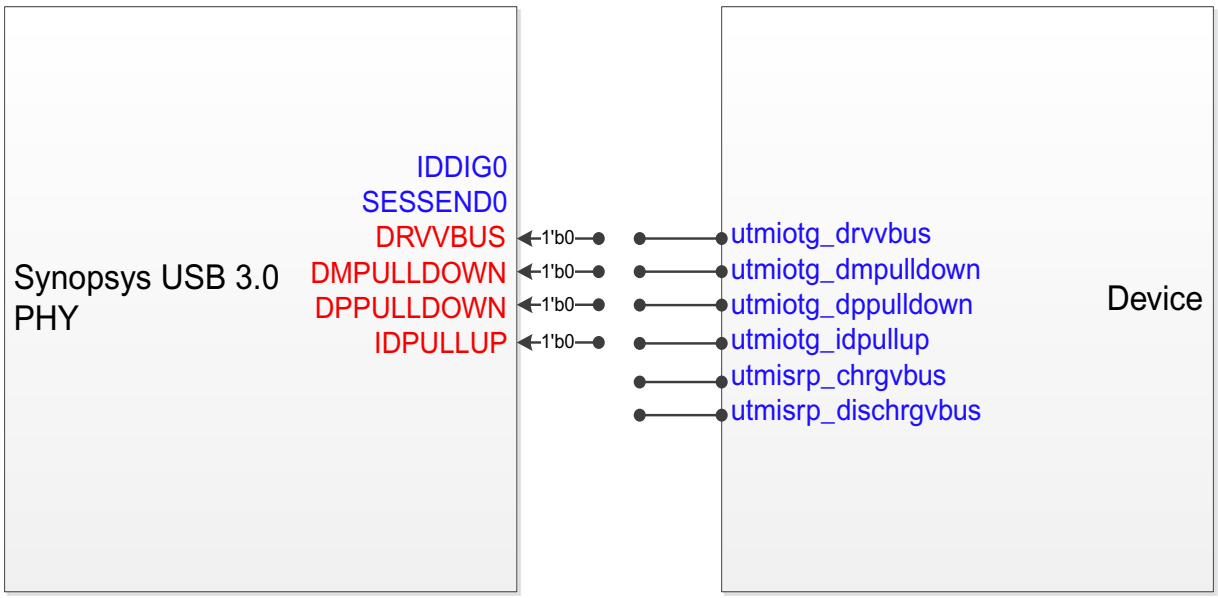
Note

- A USB PHY operating in a Device role must use one of the VBUS detection methods. You can choose to float VBUS in this mode. If you float VBUS, you must do the following:
  - Use the PHY pipeP_power_present output to drive the controller pipe3_PowerPresent input. The PHY AVALID / BVALID / OTGSESSVLD / VBUSVALID outputs will not be operational (they remain at 1'b0) when the external VBUS comparator detection option is used.
  - Use external comparator method (as described in the PHY databook) and drive VBUSVLDEXT0 and VBUSVLDEXTSEL0
- For details on connection of PHYCLOCK/FREECLK to utmi_clk, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.
- When FREECLK is connected to utmi_clk, enable DWC_USB3_FREECLK_USB2_EXIST (refer to *DesignWare Cores USB 3.0 Controller User Guide*).
- For details on usage of utmi_suspend_com and utmi_l1_suspend_com signals, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

1.2.3 USB 3.0 PHY OTG Signals

Figure 1-4 shows the USB 3.0 OTG signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 device controller.

Figure 1-4 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Device Controller – USB 3.0 OTG Signals



1.2.4 USB 3.0 PHY Miscellaneous Signals

Figure 1-5 shows the USB 3.0 miscellaneous signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 device controller.

Figure 1-5 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Device Controller – USB 3.0 Miscellaneous Signals

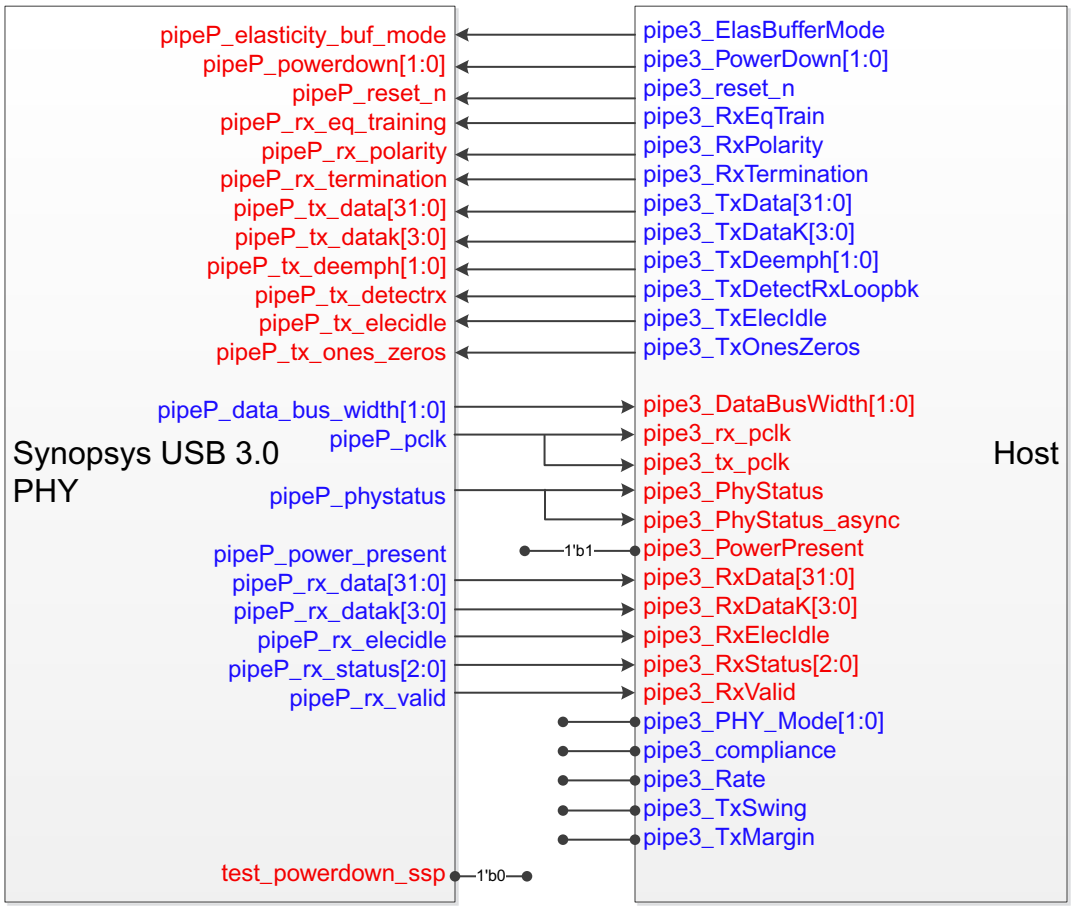
1.3 Integrating USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Host Controller

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals and miscellaneous signals.

1.3.1 USB 3.0 PIPE Signals

Figure 1-6 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 host controller.

Figure 1-6 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Host Controller – USB 3.0 PIPE Interface Signals

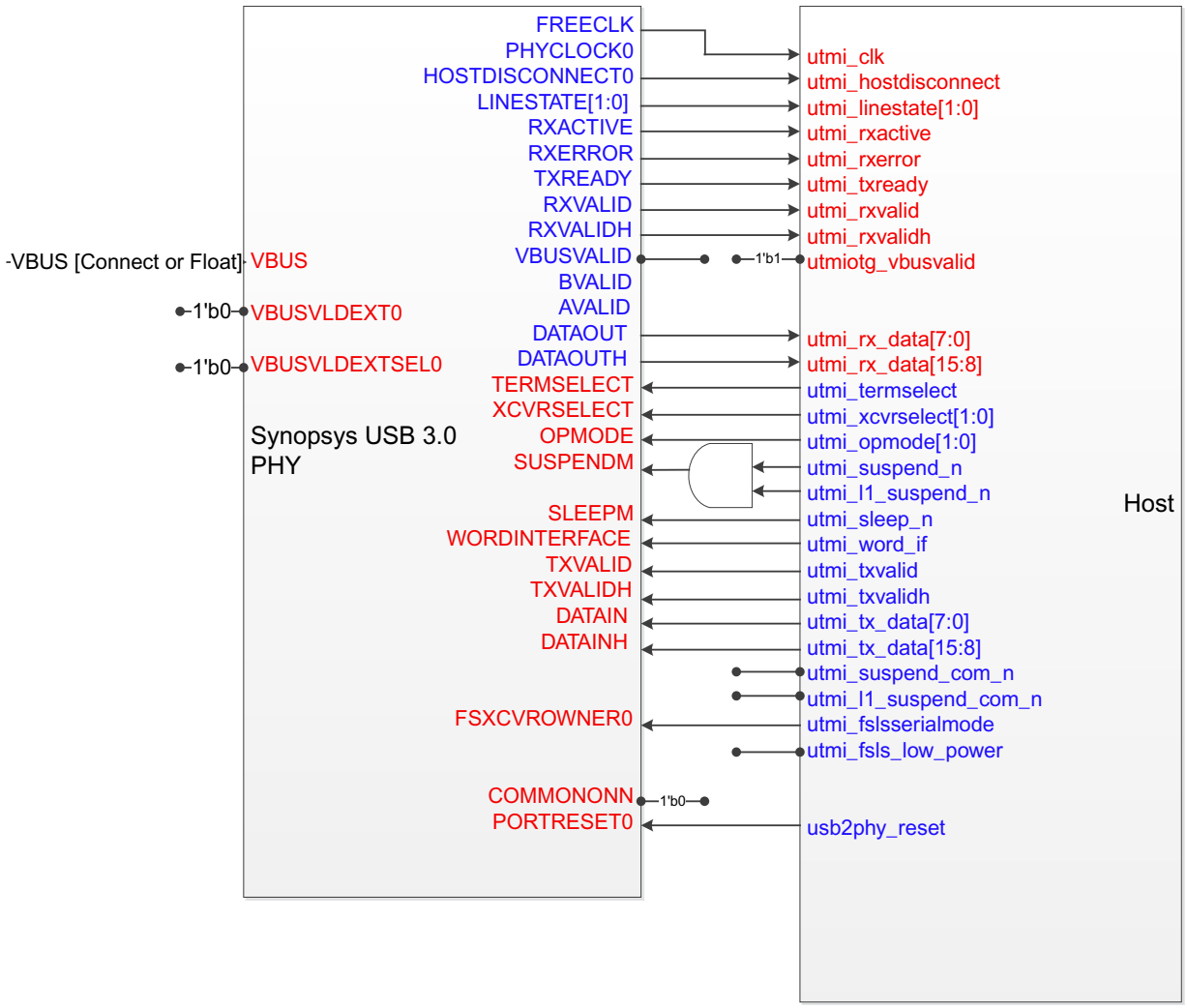


Note The controller outputs pipe3_PHY_Mode[1:0], pipe3_compliance and pipe3_Rate are hard wired to the USB 3.0 values. For more information, refer to the *DesignWare Cores USB 3.0 Controller Databook*. The corresponding signals are not implemented on the USB 3.0 PHY.

1.3.2 USB 3.0 PHY UTMI Signals

Figure 1-7 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 host controller.

Figure 1-7 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Host Controller – USB 3.0 UTMI Interface Signals



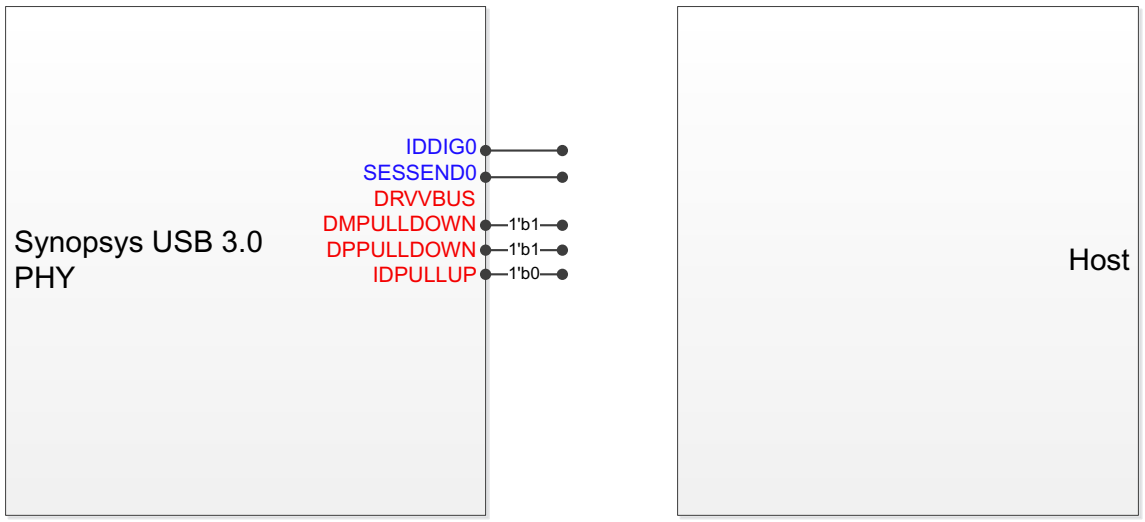
Note

- For details on connection of PHYCLOCK/FREECLK to utmi_clk, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.
- When FREECLK is connected to utmi_clk, enable DWC_USB3_FREECLK_USB2_EXIST (refer to *DesignWare Cores USB 3.0 Controller User Guide*).
- For details on usage of utmi_suspend_com and utmi_l1_suspend_com signals, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

1.3.3 USB 3.0 PHY OTG Signals

Figure 1-8 shows the USB 3.0 OTG signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 host controller.

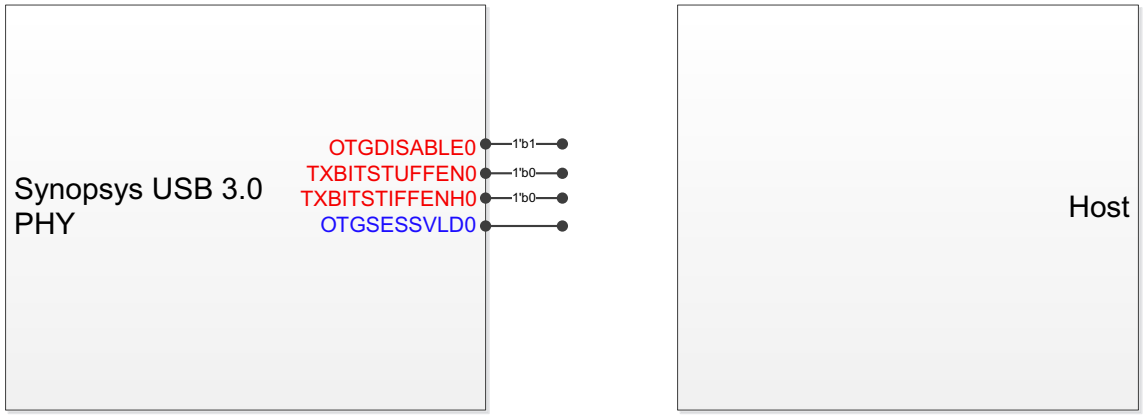
Figure 1-8 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Host Controller – USB 3.0 OTG Signals



1.3.4 USB 3.0 PHY Miscellaneous Signals

Figure 1-9 shows the USB 3.0 miscellaneous signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 host controller.

Figure 1-9 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with Host Controller – USB 3.0 Miscellaneous Signals



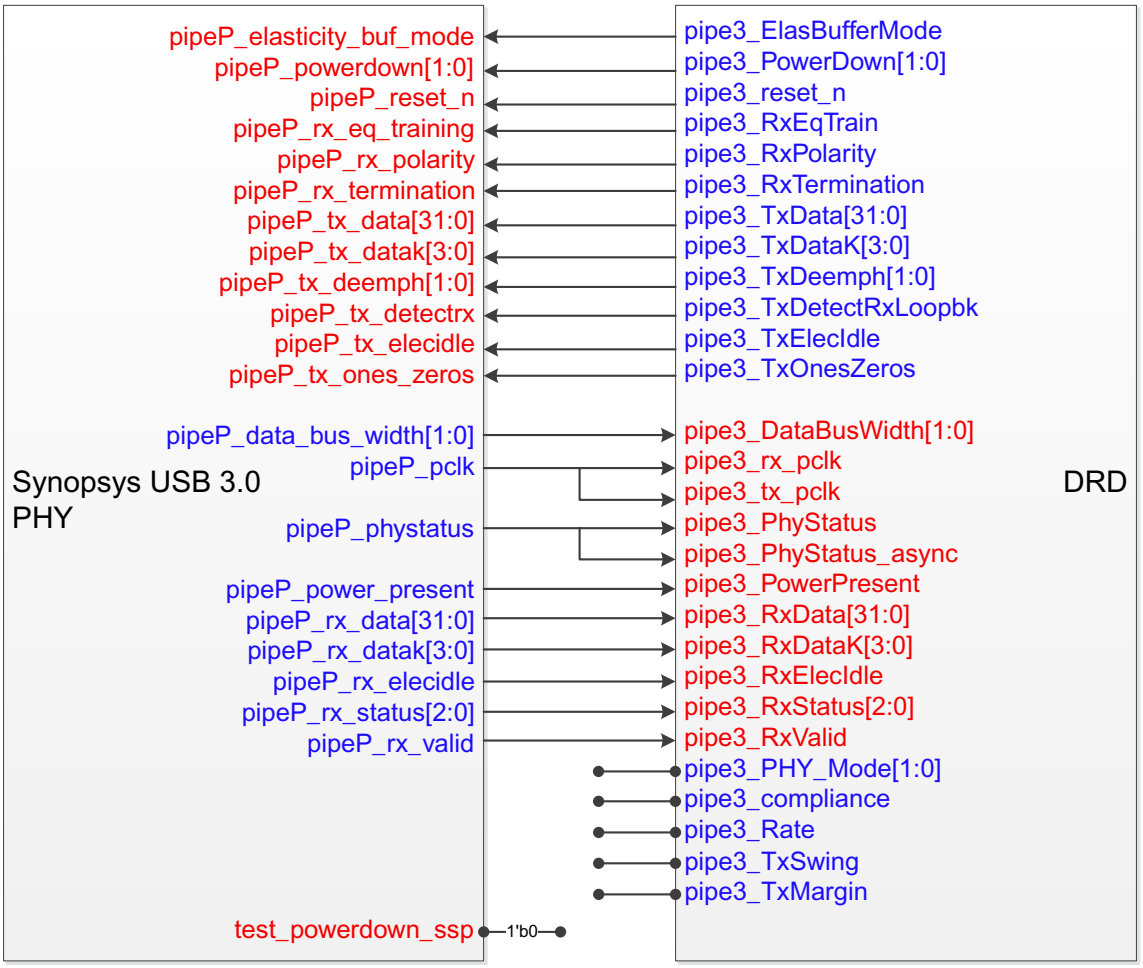
1.4 Integrating USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with DRD Controller

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals, and miscellaneous signals.

1.4.1 USB 3.0 PIPE Signals

Figure 1-10 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 DRD controller.

Figure 1-10 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with DRD Controller – USB 3.0 PIPE Interface Signals

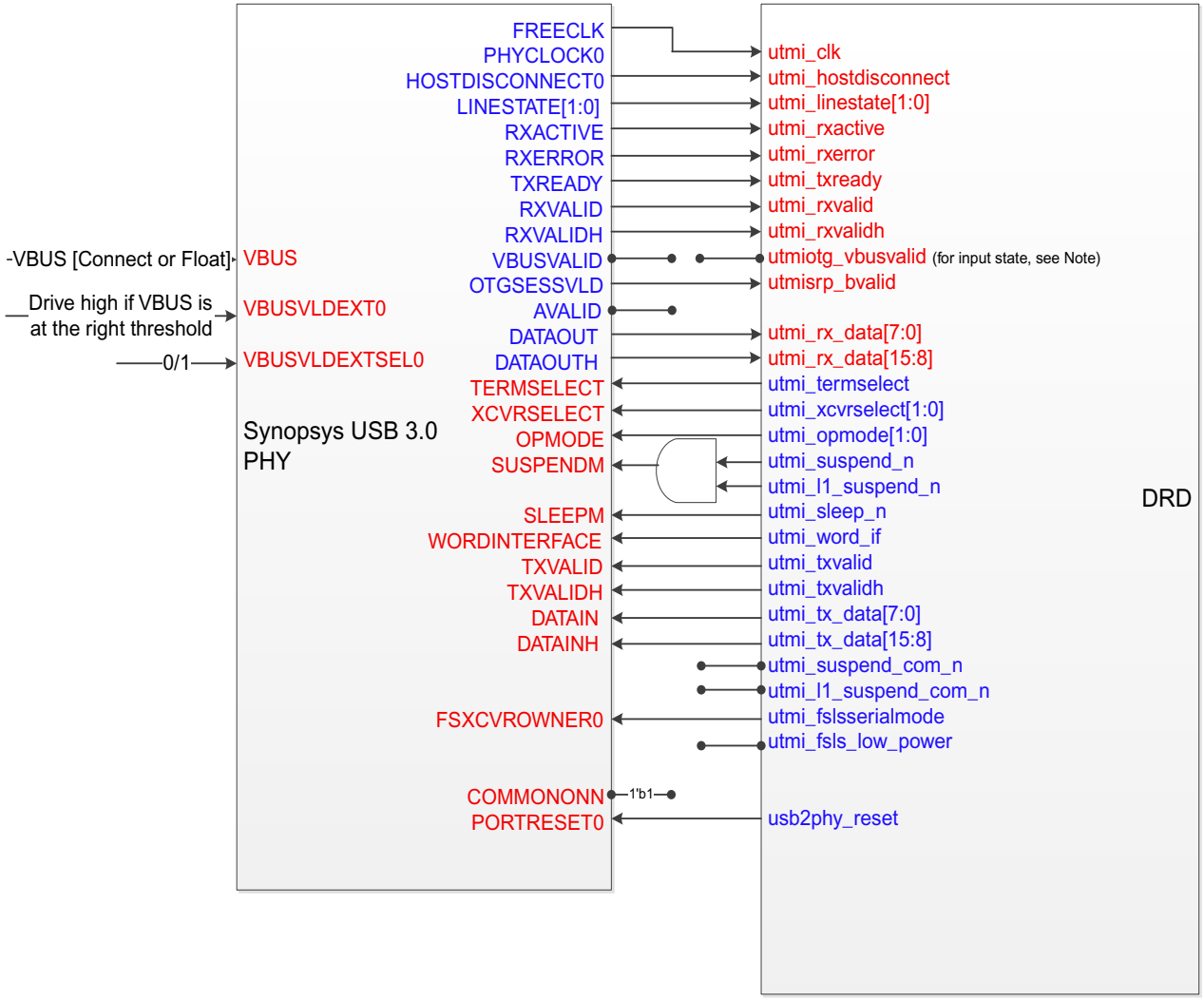


Note The controller outputs pipe3_PHY_Mode[1:0], pipe3_compliance and pipe3_Rate are hard wired to the USB 3.0 values. For more information, refer to the *DesignWare Cores USB 3.0 Controller Databook*. The corresponding signals are not implemented on the USB 3.0 PHY.

1.4.2 USB 3.0 PHY UTMI Signals

Figure 1-11 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 DRD controller.

Figure 1-11 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with DRD Controller – USB 3.0 UTMI Interface Signals



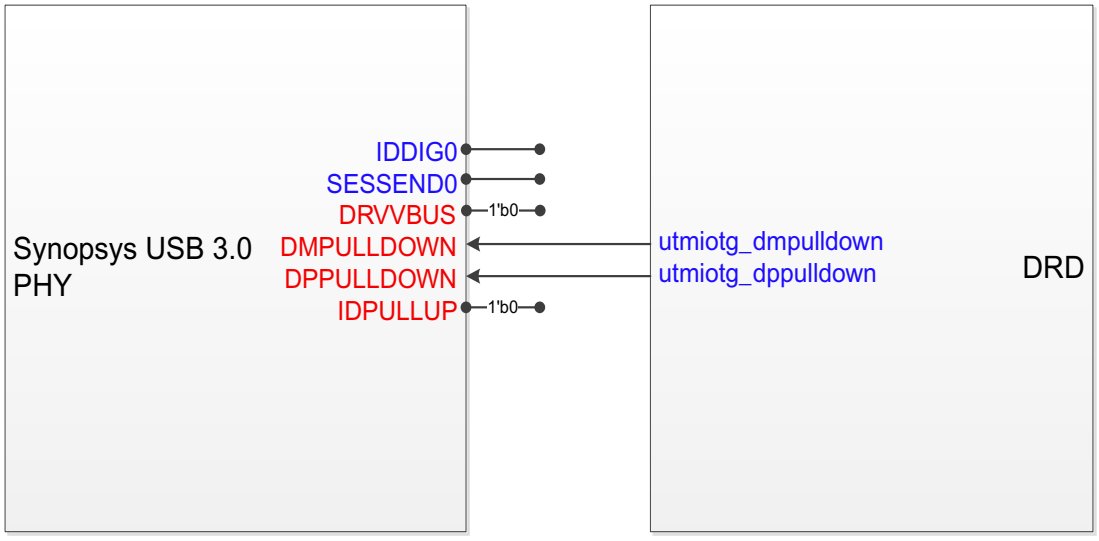
Note

- For Device mode, utmiotg_vbusvalid=1'b0.
- For Host mode, utmiotg_vbusvalid=1'b1.
- A USB PHY operating in a Device role must use one of the VBUS detection methods. You can choose to float VBUS in this mode. If you float VBUS, you must do the following:
  - Use the PHY pipeP_power_present output to drive the controller pipe3_PowerPresent input. The PHY AVALID / BVALID / OTGSESSVLD / VBUSVALID outputs will not be operational (they remain at 1'b0) when the external VBUS comparator detection option is used.
  - Use external comparator method (as described in the PHY databook) and drive VBUSVLDEXT0 and VBUSVLDEXTSEL0
- For details on connection of PHYCLOCK/FREECLK to utmi_clk, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.
- When FREECLK is connected to utmi_clk, enable DWC_USB3_FREECLK_USB2_EXIST (refer to *DesignWare Cores USB 3.0 Controller Databook*).
- For details on usage of utmi_suspend_com and utmi_l1_suspend_com signals, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

1.4.3 USB 3.0 PHY OTG Signals

Figure 1-12 shows the USB 3.0 OTG signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 DRD controller.

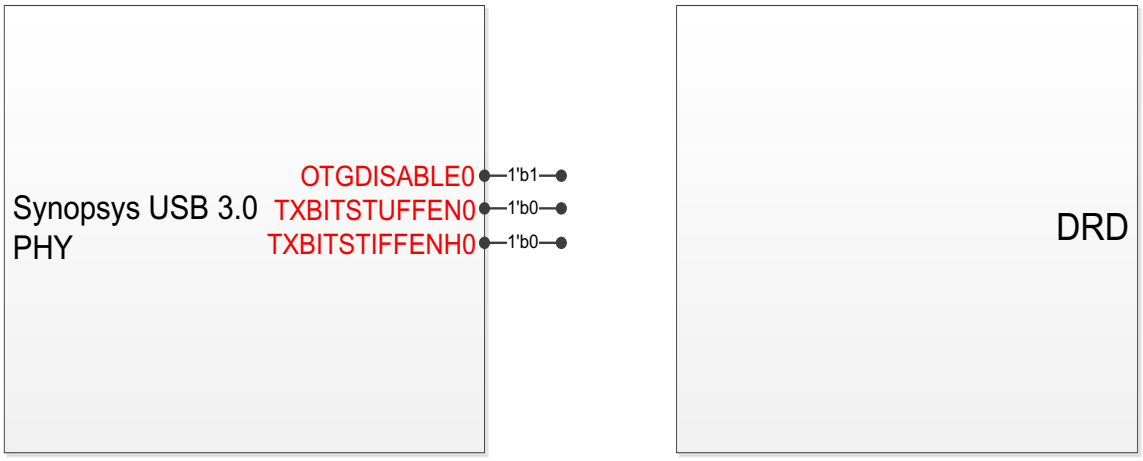
Figure 1-12 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with DRD Controller – USB 3.0 OTG Signals



1.4.4 USB 3.0 PHY Miscellaneous Signals

Figure 1-13 shows the USB 3.0 miscellaneous signals when the USB 3.0 PHY operating in USB 3.0 mode (SS and USB 2.0) is integrated with a USB 3.0 DRD controller.

Figure 1-13 USB 3.0 PHY in USB 3.0 Mode (SS and USB 2.0) with DRD Controller – USB 3.0 Miscellaneous Signals



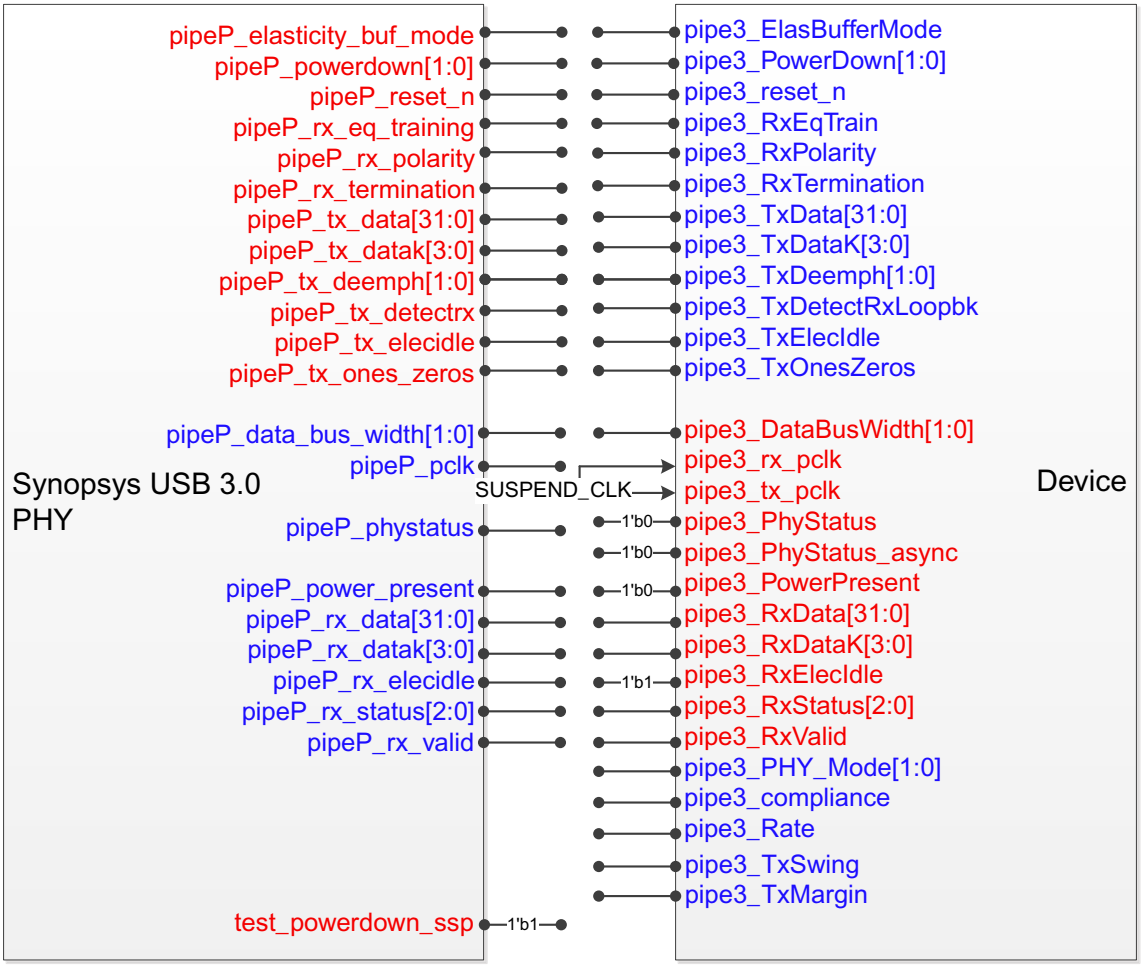
1.5 Integrating USB 3.0 PHY in USB 2.0 Mode with Device Controller

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals and miscellaneous signals.

1.5.1 USB 3.0 PIPE Signals

Figure 1-14 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 device controller.

Figure 1-14 USB 3.0 PHY in USB 2.0 Mode with Device Controller – USB 3.0 PIPE Interface Signals



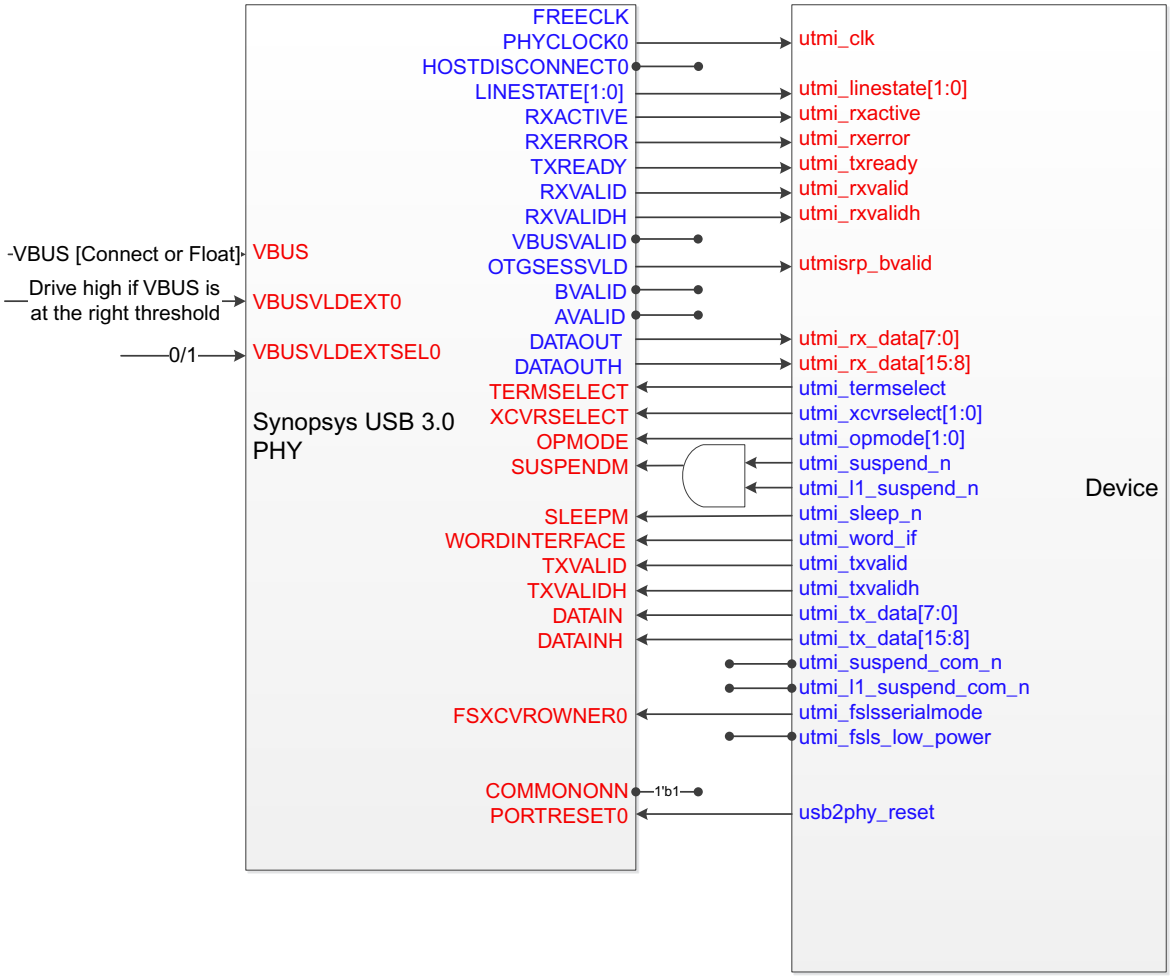
Note

- For details on SUSPEND_CLK, see Chapter 5 of the *DesignWare Cores USB 3.0 Controller Databook*.
- For USB 2.0 mode only, phy_reset is asserted to 1'b1 at least 1 us before asserting test_powerdown_ssp to 1'b1

1.5.2 USB 3.0 PHY UTMI Signals

Figure 1-15 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 device controller.

Figure 1-15 USB 3.0 PHY in USB 2.0 Mode with Device Controller – USB 3.0 UTMI Interface Signals



Note

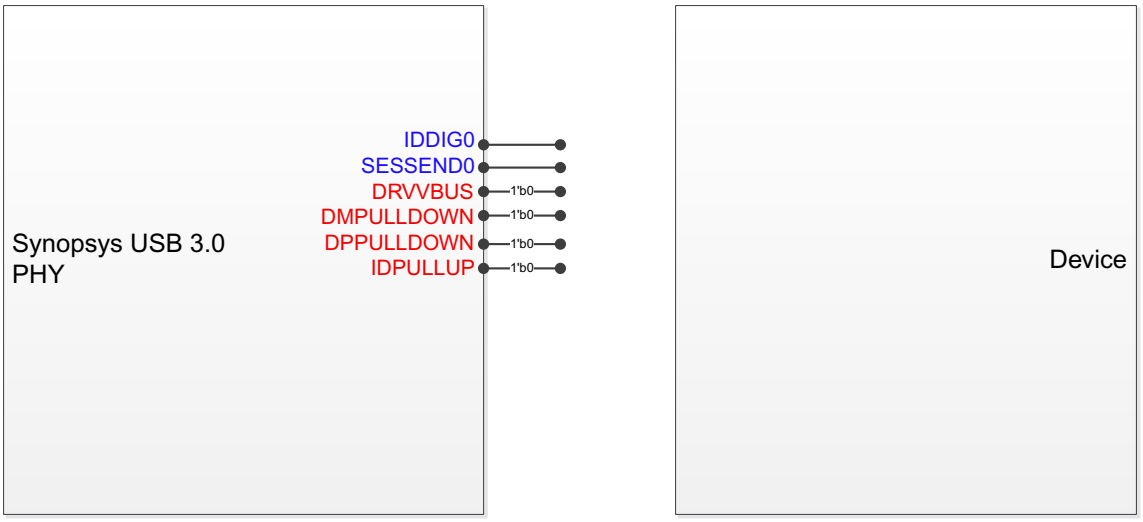
- A USB PHY operating in a Device role must use one of the VBUS detection methods.You can choose to float VBUS in this mode. External comparator can be used if you float VBUS. (Refer to VBUSVLDEXT0 and VBUSVLDEXTSEL0 signals.)

  When VBUS is floating, VBUSVLDEXT0 does not change the OTGSESSVLD0 output. In this scenario, the controller utmisrp_bvalid input must be driven from a signal or register derived from the external VBUS comparator result.
- For details on connection of PHYCLOCK/FREECLK to utmi_clk, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.
  When FREECLK is connected to utmi_clk, enable DWC_USB3_FREECLK_USB2_EXIST (refer to *DesignWare Cores USB 3.0 Controller Databook*).
- For details on usage of utmi_suspend_com and utmi_l1_suspend_com signals, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

1.5.3 USB 3.0 PHY OTG Signals

Figure 1-16 shows the USB 3.0 OTG signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 device controller.

Figure 1-16 USB 3.0 PHY in USB 2.0 Mode with Device Controller – USB 3.0 OTG Signals



1.5.4 USB 3.0 PHY Miscellaneous Signals

Figure 1-17 shows the USB 3.0 miscellaneous signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 device controller.

Figure 1-17 USB 3.0 PHY in USB 2.0 Mode with Device Controller – USB 3.0 Miscellaneous Signals

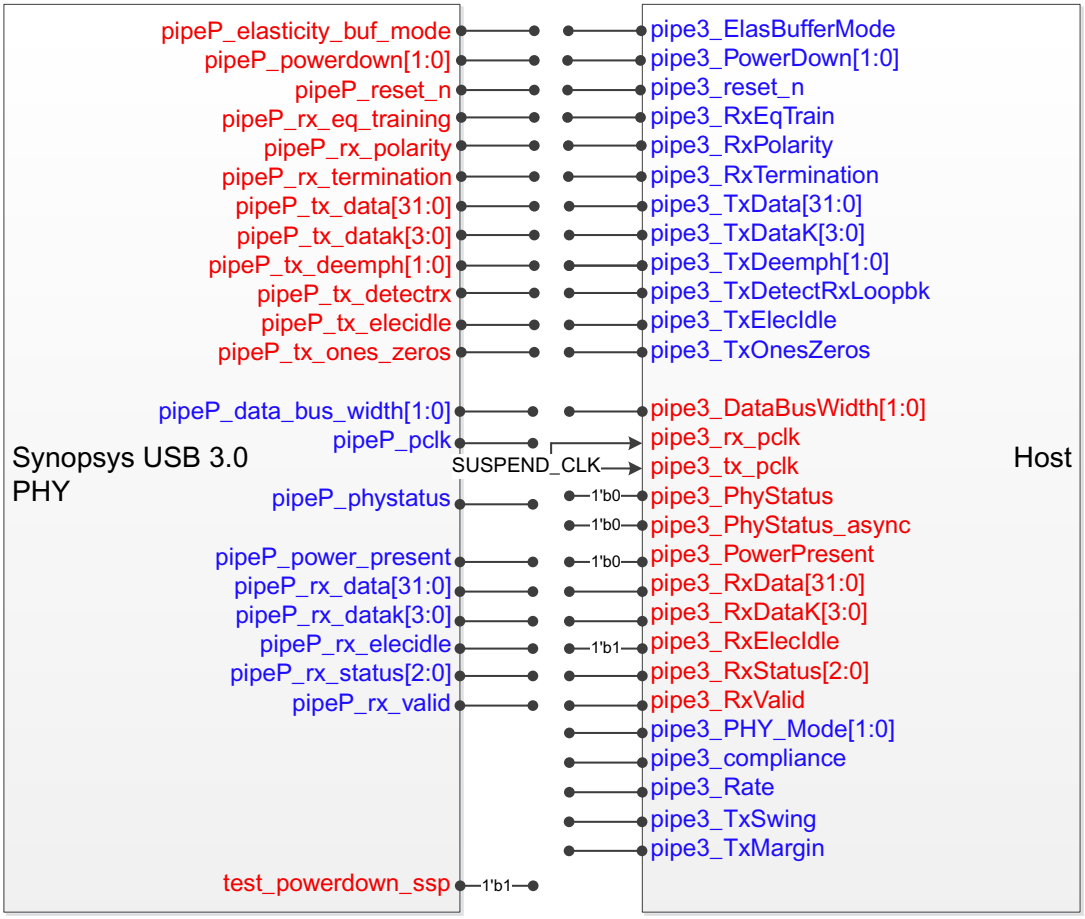
1.6 Integrating USB 3.0 PHY in USB 2.0 Mode with Host Controller

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals and miscellaneous signals.

1.6.1 USB 3.0 PIPE Signals

Figure 1-18 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 host controller.

Figure 1-18 USB 3.0 PHY in USB 2.0 Mode with Host Controller – USB 3.0 PIPE Interface Signals



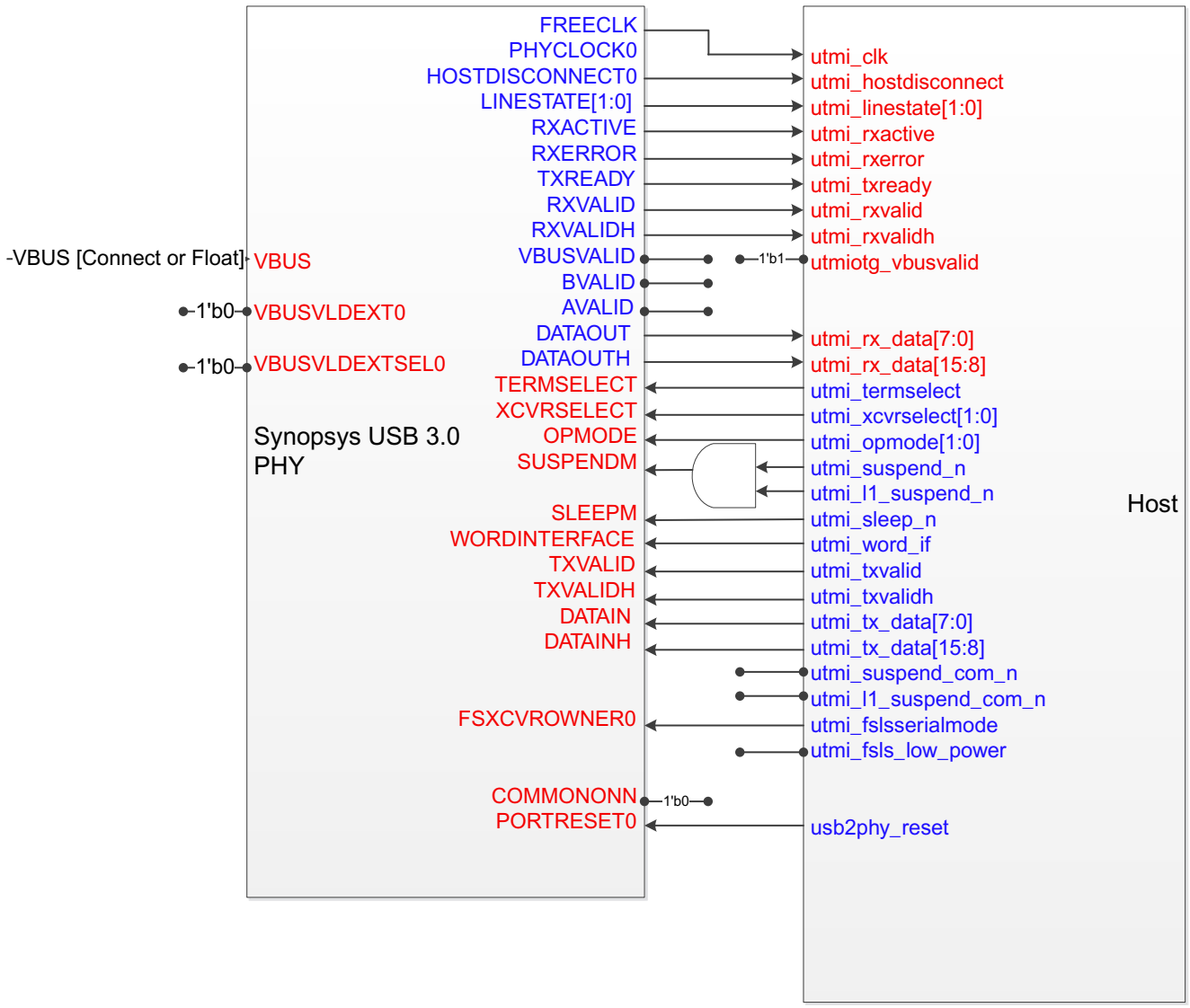
Note

- The controller outputs pipe3_PHY_Mode[1:0], pipe3_compliance and pipe3_Rate are hard wired to the USB 3.0 values. For more information, refer to *DesignWare Cores USB 3.0 Controller Databook*. The corresponding signals are not implemented in the USB 3.0 PHY.
- For details on SUSPEND_CLK, see Chapter 5 of the *DesignWare Cores USB 3.0 Controller Databook*.
- For USB 2.0 mode only, phy_reset is asserted to 1'b1 at least 1 us before asserting test_powerdown_ssp to 1'b1

1.6.2 USB 3.0 PHY UTMI Signals

Figure 1-19 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 host controller.

Figure 1-19 USB 3.0 PHY in USB 2.0 Mode with Host Controller – USB 3.0 UTMI Interface Signals



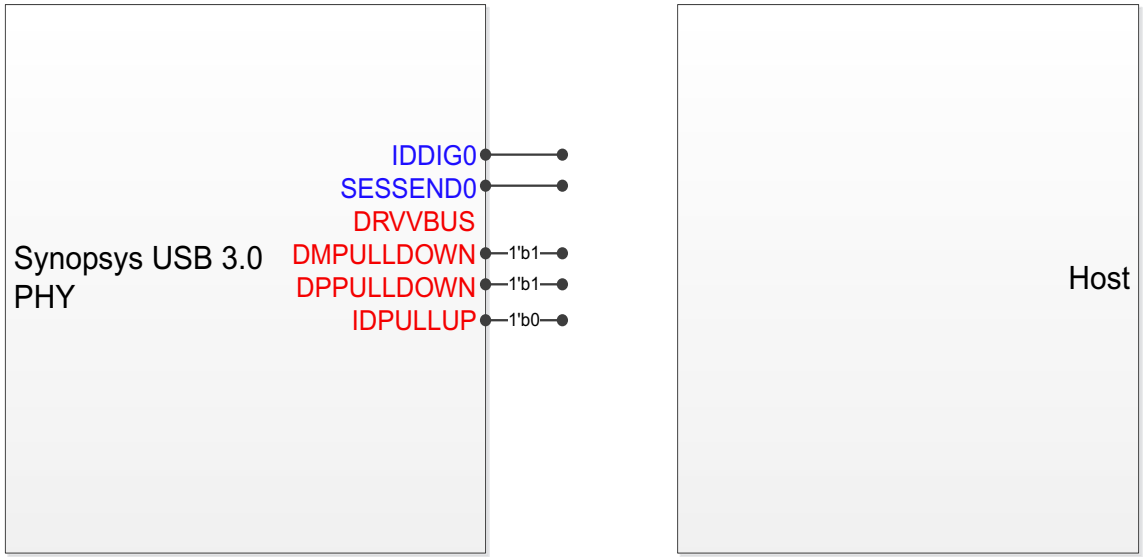
Note

- For details on connection of PHYCLOCK/FREECLK to utmi_clk, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.
  When FREECLK is connected to utmi_clk, enable DWC_USB3_FREECLK_USB2_EXIST (refer to *DesignWare Cores USB 3.0 Controller Databook*).
- For details on usage of utmi_suspend_com and utmi_l1_suspend_com signals, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

1.6.3 USB 3.0 PHY OTG Signals

Figure 1-20 shows the USB 3.0 OTG signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 host controller.

Figure 1-20 USB 3.0 PHY in USB 2.0 Mode with Host Controller – USB 3.0 OTG Signals



1.6.4 USB 3.0 PHY Miscellaneous Signals

Figure 1-21 shows the USB 3.0 miscellaneous signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 host controller.

Figure 1-21 USB 3.0 PHY in USB 2.0 Mode with Host Controller – USB 3.0 Miscellaneous Signals

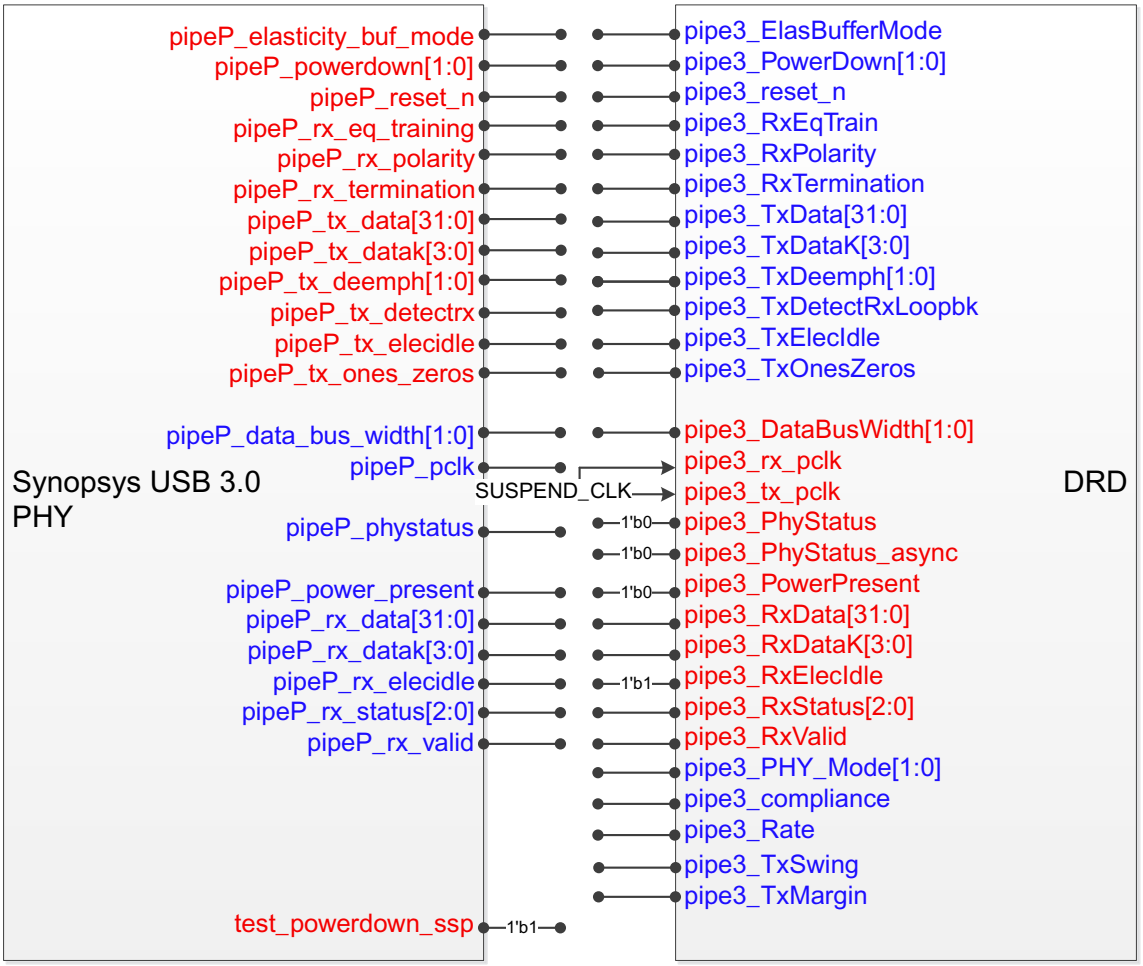
1.7 Integrating USB 3.0 PHY in USB 2.0 Mode with DRD Controller

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals and miscellaneous signals.

1.7.1 USB 3.0 PIPE Signals

Figure 1-22 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 DRD controller.

Figure 1-22 USB 3.0 PHY in USB 2.0 Mode with DRD Controller – USB 3.0 PIPE Interface Signals



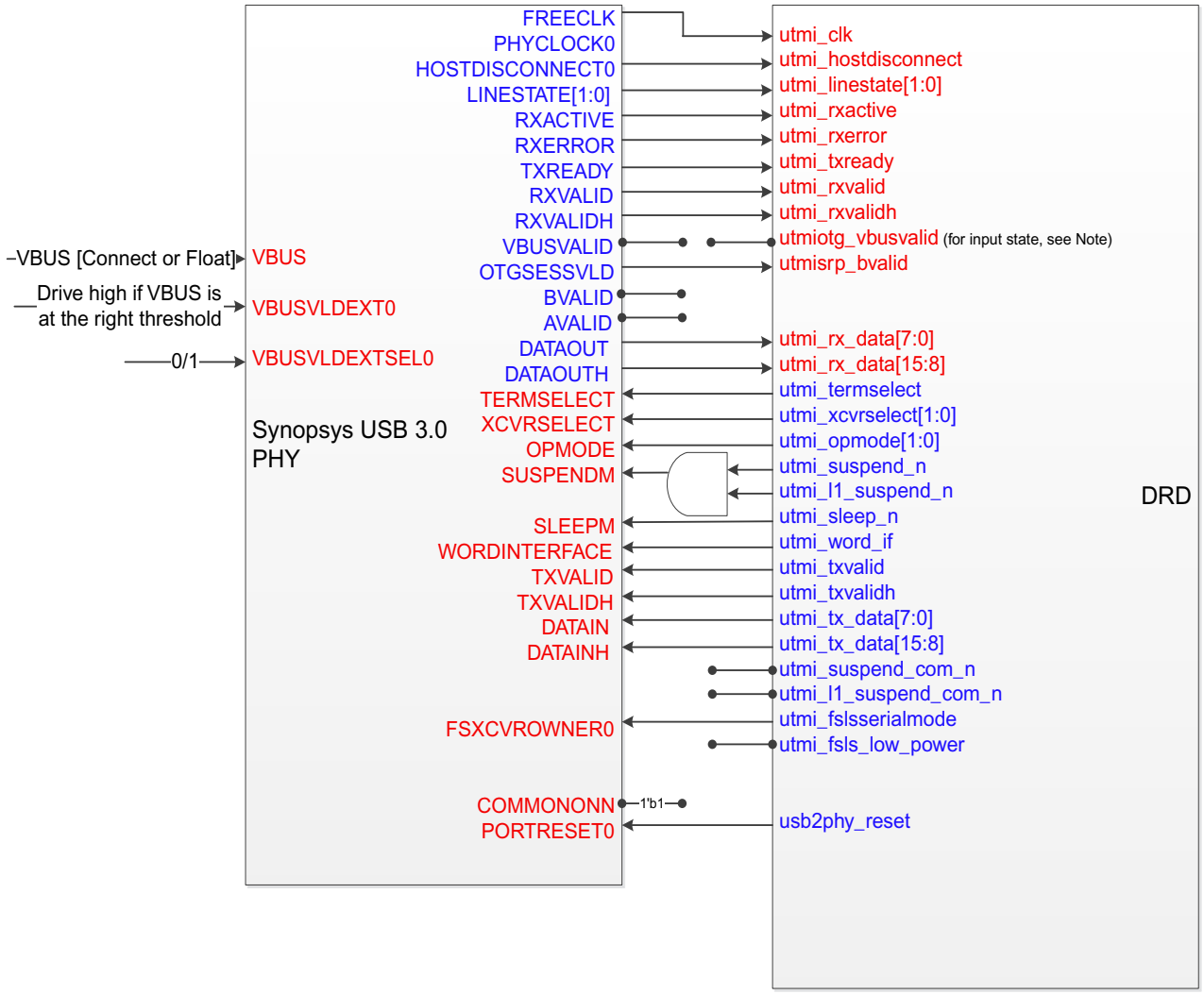
Note

- For details on SUSPEND_CLK, see the *DesignWare Cores USB 3.0 Controller Databook*.
- If the PCS layer is synthesized, pipeP_power_present can be connected from the PHY to pipe3_PowerPresent of the controller.
- For USB 2.0 mode only, phy_reset is asserted to 1'b1 at least 1us before asserting test_powerdown_ssp to 1'b1

1.7.2 USB 3.0 PHY UTMI Signals

Figure 1-23 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 DRD controller.

Figure 1-23 USB 3.0 PHY in USB 2.0 Mode with DRD Controller – USB 3.0 UTMI Interface Signals



Note

- For Device mode, utmiotg_vbusvalid=1'b0.
- For Host mode, utmiotg_vbusvalid=1'b1.
- A USB PHY operating in a Device role must use one of the VBUS detection methods. You can choose to float VBUS in this mode. External comparator can be used if you float VBUS. (Refer to VBUSVLDEXT0 and VBUSVLDEXTSEL0 signals.)

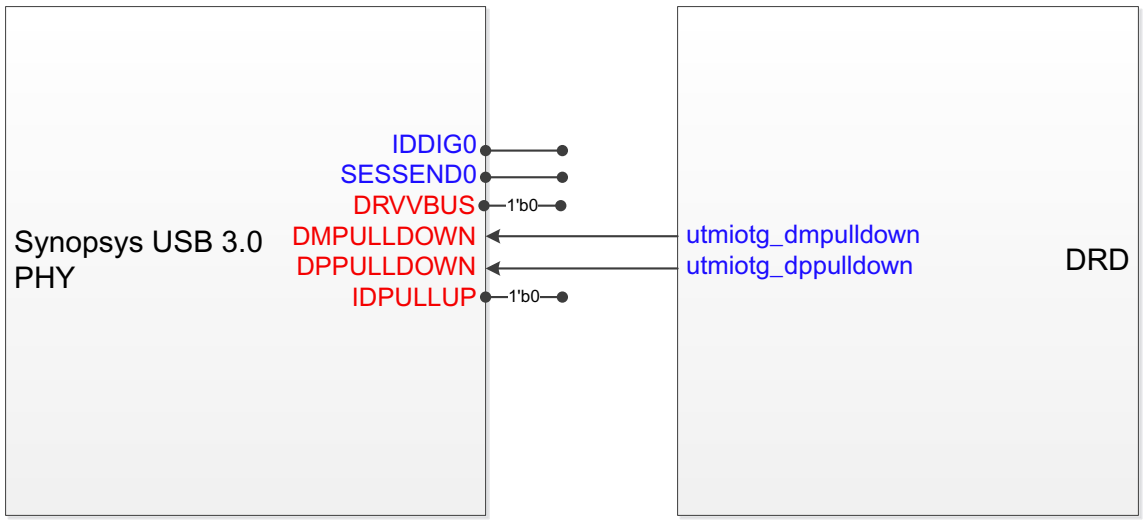
  When VBUS is floating, VBUSVLDEXT0 does not change the OTGSESSVLD0 output. In this scenario, the controller utmisrp_bvalid input must be driven from a signal or register derived from the external VBUS comparator result.
- For details on connection of PHYCLOCK/FREECLK to utmi_clk, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

  When FREECLK is connected to utmi_clk, enable DWC_USB3_FREECLK_USB2_EXIST (refer to *DesignWare Cores USB 3.0 Controller Databook*).
- For details on usage of utmi_suspend_com and utmi_l1_suspend_com signals, see Section 5.3 of the *DesignWare Cores USB 3.0 Controller User Guide*.

1.7.3 USB 3.0 PHY OTG Signals

Figure 1-24 shows the USB 3.0 OTG signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 DRD controller.

Figure 1-24 USB 3.0 PHY in USB 2.0 Mode with DRD Controller – USB 3.0 OTG Signals



1.7.4 USB 3.0 PHY Miscellaneous Signals

Figure 1-25 shows the USB 3.0 miscellaneous signals when the USB 3.0 PHY operating in USB 2.0 mode is integrated with a USB 3.0 DRD controller.

Figure 1-25 USB 3.0 PHY in USB 2.0 Mode with DRD Controller – USB 3.0 Miscellaneous Signals

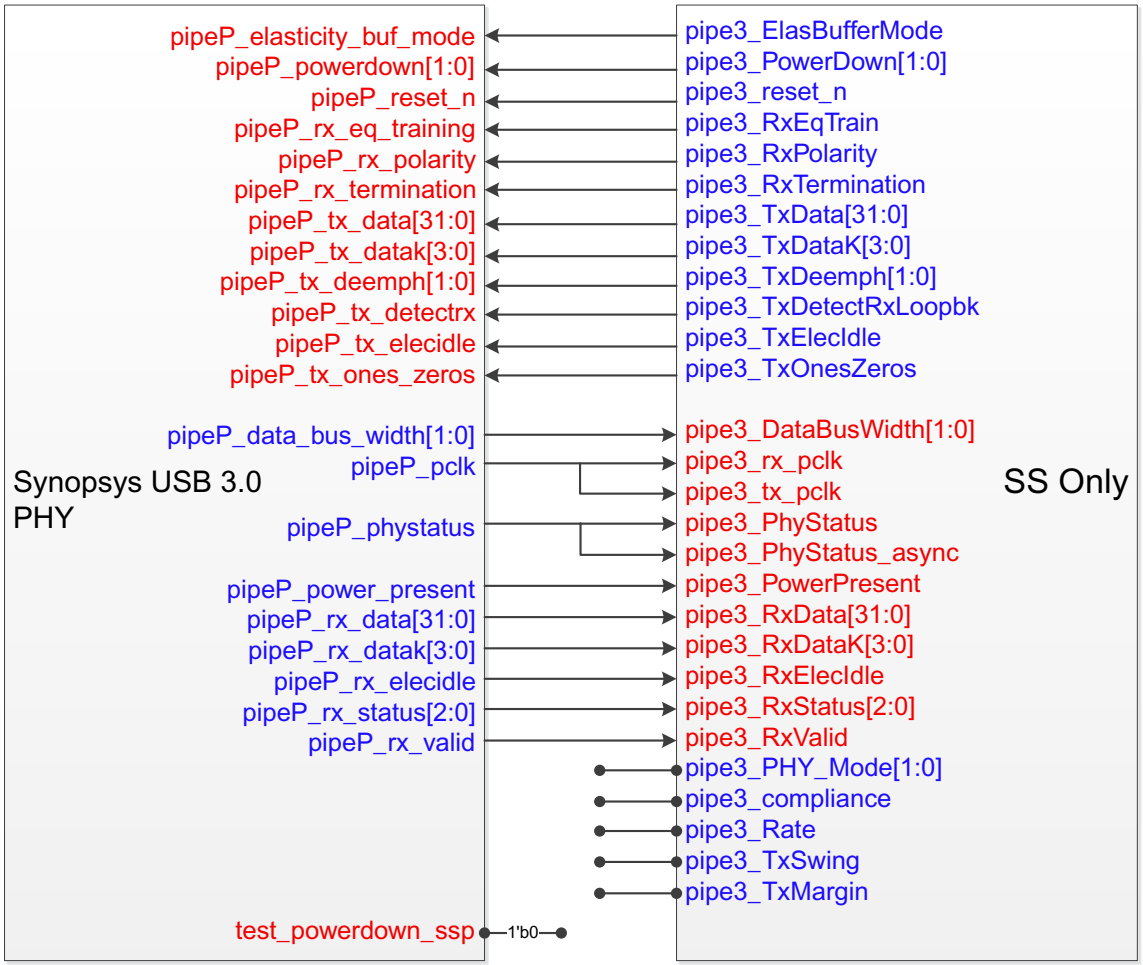
1.8 Integrating USB 3.0 PHY in USB 3.0 Mode (SS only)

The following subsections divide the interface signals into USB 3.0 PIPE signals, UTMI interface signals, OTG signals and miscellaneous signals. The High Speed section of the controller is connected to a USB2PHY. These connections are out of the scope of this application note.

1.8.1 USB 3.0 PIPE Signals

Figure 1-26 shows the USB 3.0 PIPE interface signals when the USB 3.0 PHY operates in USB 3.0 mode (SS only).

Figure 1-26 USB 3.0 PHY in USB 3.0 Mode (SS only) – USB 3.0 PIPE Interface Signals

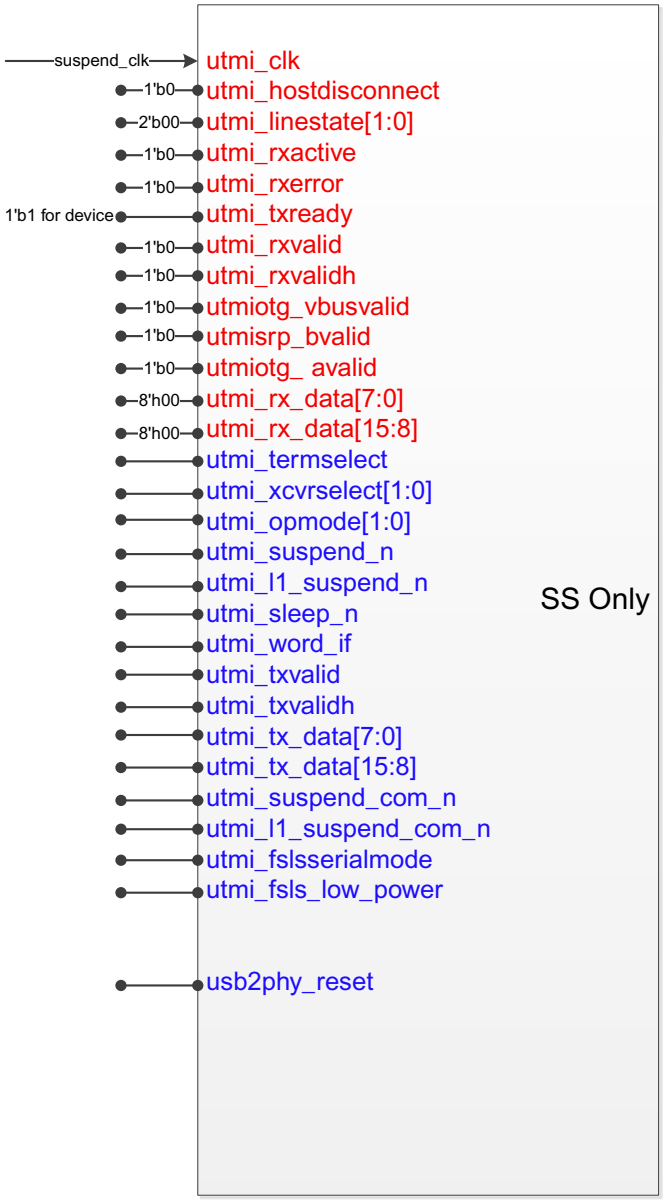


Note The controller outputs pipe3_PHY_Mode[1:0], pipe3_compliance and pipe3_Rate are hard wired to the USB 3.0 values. For more information, refer to *DesignWare Cores USB 3.0 Controller Databook*. The corresponding signals are not implemented on the USB 3.0 PHY.

1.8.2 USB 3.0 PHY UTMI Signals

Figure 1-27 shows the USB 3.0 UTMI interface signals when the USB 3.0 PHY operates in USB 3.0 mode (SS only).

Figure 1-27 USB 3.0 PHY in USB 3.0 Mode (SS only) – USB 3.0 UTMI Interface Signals



Note

- In SS-only configuration, you cannot enable hibernation feature.
- For SS-only host mode, enable GFLADJ.REFCLK_LPM_SEL mode.