Verification Continuum™

ZeBu® Unified Tcl Format Reference Guide

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SYNOPSYS®

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Preface

About This Book

The ***ZeBu® Unified Tcl Format Reference Guide*** describes the UTF commands used with ZeBu.

Intended Audience

This guide is written to help engineers in configuring the ZeBu software.

Contents of This Book

The ***ZeBu® Unified Tcl Format Reference Guide*** has the following chapters:

Chapter	Describes...
Clocks	Lists the commands used with clocks
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Related Documentation

Document Name	Description
ZeBu User Guide	Provides detailed information on using ZeBu.
ZeBu Debug Guide	Provides information on tools you can use for debugging.
ZeBu Debug Methodology Guide	Provides debug methodologies that you can use for debugging.
ZeBu Unified Command-Line User Guide	Provides the usage of Unified Command-Line Interface (UCLI) for debugging your design.
ZeBu UTF Reference Guide	Describes Unified Tcl Format (UTF) commands used with ZeBu.
ZeBu Power Aware Verification User Guide	Describes how to use Power Aware verification in ZeBu environment, from the source files to runtime.
ZeBu Functional Coverage User Guide	Describes collecting functional coverage in emulation.
Simulation Acceleration User Guide	Provides information on how to use Simulation Acceleration to enable cosimulating SystemVerilog testbenches with the DUT
ZeBu Verdi Integration Guide	Provides Verdi features that you can use with ZeBu. This document is available in the Verdi documentation set.
ZeBu Runtime Performance Analysis With zTune User Guide	Provides information about runtime emulation performance analysis with zTune.
ZeBu Custom DPI Based Transactors User Guide	Describes ZEMI-3 that enables writing transactors for functional testing of a design.
ZeBu LCA Features Guide	Provides a list of Limited Customer Availability (LCA) features available with ZeBu.
ZeBu Transactors Compilation Application Note	Provides detailed steps to instantiate and compile a ZeBu transactor.
ZeBu zManualPartitioner Application Note	Describes the zManualPartitioner feature for ZeBu. It is a graphical interface to manually partition a design.
ZeBu Hybrid Emulation Application Note	Provides an overview of the hybrid emulation solution and its components.

Typographical Conventions

This document uses the following typographical conventions:

To indicate	Convention Used
Program code	`OUT <= IN;`
Object names	`OUT`
Variables representing objects names	*<sig-name>*
Message	Active low signal name '<sig-name>' must end with _X.
Message location	`OUT` <= IN;
Reworked example with message removed	OUT_X <= IN;
Important Information	**NOTE:** This rule...

The following table describes the syntax used in this document:

Syntax	Description
[ ] (Square brackets)	An optional entry
{ } (Curly braces)	An entry that can be specified once or multiple times
| (Vertical bar)	A list of choices out of which you can choose one
. . . (Horizontal ellipsis)	Other options that you can specify

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1 Advanced

This section describes the following UTF commands:

- *ztopbuild*

1.1 ztopbuild

Detailed Description

Use this command to specify options for Top-Level build (**zTopBuild**).

```
 ztopbuild [-advanced_command <string>] [-advanced_command_file
<file>] [-advanced_command_netlist <string>] [-edit_netlist_file
<file>]
```

- `-edit_netlist_file #filename`: Specify filename with **zTopBuild** netlist edition commands
- `-advanced_command_file #filename`: Specify advanced command file for **zTopBuild**
- `-advanced_command {<string>}`: Specify any legacy **zTopBuild** command. Valid values: legacy zTopBuild command
- `-advanced_command_netlist {<zTopBuild_netlist_edition_command>}`: Specify any legacy **zTopBuild** netlist edition command

2 Clocks

This section describes the following UTF commands:

- *clocks*
- *clock_config*
- *clock_delay*

2.1 clocks

Detailed Description

Clock handling options

- `-skew_offset NONE | ALL`: Enables global skew offset
- `-skew_offset_synchronous <bool>`: sync/async skew offset
- `-skew_offset_delay_in_ns <int>`: async skew offset delay, but not currently in ns. zCui uses 24ns steps.
- `-localize_clock_tree NONE | FPGA | ZCORE`: Localizes clock tree
- `-glitches NOFILTER | FILTER | DELAY_ENABLES [-detect_clock_delay]`: Filters glitches

  NOTE: `-detect_clock_delay` *is only valid with* `-glitches DELAY_ENABLES`.
- `-direct_routing <bool>`: Direct routing
- `-add_internal_clk #clock_signal`: Specifies internal clock path
- `-add_internal_data #data_signal`: Specifies internal data path
- `-clear_internal_clk_data <bool>`: Clears all paths previously declared using "`-add_internal_clk`" and "`-add_internal_data`" options
- `-advanced_command_file #filename`: Specifies advanced clock handling commands

2.2 clock_config

Description

Defines clock related parameters or add new `zceiClockPort`

Functions

```
clock_config [-accuracy <16|24|32>] [-add_clock_port <string>] [-
clock_name <string>] [-clock_number <2|4|8|16>] [-fk_synchronizer
<bool>] [-frequency <string>] [-number_of_bufgs <int>] [-parameters
<CLK_PERIOD=string,DEF_RESET=string,DEF_RESETN=string,cclockName=stri
ng,clockNum=string>] [-ports
<cclock=string,creset=string,cresetn=string>] [-share_clock_bus
<bool>] [-synthesis <bool>]
```

Option(s)

- `CLK_PERIOD <string>`: Specify the value of parameter '`CLK_PERIOD`' of `zceiClockPort`.
- `DEF_RESET <string>`: Specify the value of parameter '`DEF_RESET`' of `zceiClockPort`.
- `DEF_RESETN <string>`: Specify the value of parameter '`DEF_RESETN`' of `zceiClockPort`.
- `cclock <string>`: Specify the port connection of port '`cclock`' of `zceiClockPort`. exist when '`-add_clock_port zceiClockPort`' is specified
- `cclockName <string>`: Specify the value of parameter '`cclockName`' of `zceiClockPort`.
- `clockNum <string>`: Specify the value of parameter '`clockNum`' of `zceiClockPort`.
- `creset <string>`: Specify the port connection of port '`creset`' of `zceiClockPort`.
- `cresetn <string>`: Specify the port connection of port '`cresetn`' of `zceiClockPort`.

- -accuracy <16|24|32>: Specify the accuracy of clock generation (bits).
- -add_clock_port <string>: Specify the type of the clock port to be added. only zceiClockPort is supported
- -clock_name <string>: Specify the name of the clock port or the XMR to the clock port instance path. |driverfrequency|xclkfrequency|#XMR_to_zClockPort_instance
- -clock_number <2|4|8|16>: Specify the number of resources allocated for the Clock Generator.
- -fk_synchronizer <bool>: Force the use of synchronizer on the RTB to force clocks generated from none zceiClockport to be aligned with zceiClockPort one.
- -frequency <string>: Specify clock frequency. be used with 'MHz'/'kHz' units, in format '100 MHz'
- -number_of_bufgs <int>: Specify the number of bufgs available for DUT clock routing in the FPGAs. non-negative integer number.
- -parameters <CLK_PERIOD=string,DEF_RESET=string,DEF_RESETN=string,cclockName=string,clockNum=string>: Specify the parameter values of the clock port if '-add_clock_port' exists.
- CLK_PERIOD <string>: Specify the value of parameter 'CLK_PERIOD' of zceiClockPort.
- DEF_RESET <string>: Specify the value of parameter 'DEF_RESET' of zceiClockPort.
- DEF_RESETN <string>: Specify the value of parameter 'DEF_RESETN' of zceiClockPort.
- cclockName <string>: Specify the value of parameter 'cclockName' of zceiClockPort.
- clockNum <string>: Specify the value of parameter 'clockNum' of zceiClockPort.
- -ports <cclock=string,creset=string,cresetn=string>: Specify the port connection of the clock port if '-add_clock_port' exists.

- `cclock <string>`: Specify the port connection of port '`cclock`' of `zceiClockPort`. exist when '`-add_clock_port zceiClockPort`' is specified
- `creset <string>`: Specify the port connection of port '`creset`' of `zceiClockPort`.
- `cresetn <string>`: Specify the port connection of port '`cresetn`' of `zceiClockPort`.
- `-share_clock_bus <bool>`: Use remaining clock bus bits for trigger routing. Only supported for ZeBu Server 4 Ultra; Default: true.
- `-synthesis <bool>`: Used if `-clock_name` is Top-down XMR to `zClockPort` instance.

Constraint(s)

At least one of the options should be used

check illegal option combinations

the accepted value for `-add_clock_port` is only `zceiClockPort` now

Note(s)

- `-clock_name` and `-frequency` are the only options supported with ZeBu Companion
- `-accuracy 16` is only supported with ZeBu Server 4 Ultra
- `-share_clock_bus` is only supported with ZeBu Server 4 Ultra

Example(s)

```
clock_config -clock_number 8

clock_config -clock_name masterfrequency -frequency "160MHz"

clock_config -clock_name top.c2 -synthesis true -frequency "450 Mhz"

clock_config -add_clock_port zceiClockPort -clock_name top.dut.clock
-ports {cclock=clk}
```

2.3 clock_delay

Description

Enables Verilog clock delays support

```
clock_delay [-auto_tolerance <bool>] [-clock_wire <string>] [-
clockdelayport_timescale <string>] [-debug <bool>] [-duty_high <int>]
[-duty_low <int>] [-gate_delay <bool>] [-ignore_zero_delay <bool>] [-
insert_clock_delay_port_in_module <string>] [-instance_name <string>]
[-module <list>] [-perf_mode <int>] [-phase <int>] [-reset_duration
<int>] [-reset_value <int>] [-reset_wire <string>] [-sdc_mcp_mode
<int>] [-tolerance <int>]
```

Option(s)

- `-auto_tolerance <bool>`: Computes and sets maximum tolerance for `clock_delay`.
- `-clock_wire <string>`: Sets clock path.
- `-clockdelayport_timescale <string>`: Specify the time scale of all clock delay ports.

  `[|1|10|100] [s|ms|us|ns|fs|ps]`
- `-debug <bool>`: Enables debug mode.
- `-duty_high <int>`: Sets `dutyHigh` for clock delay port defined in UTF command. non-negative integer number.
- `-duty_low <int>`: Sets `dutyLow` for clock delay port defined in UTF command. non-negative integer number.
- `-gate_delay <bool>`: Enables `clock_delay` mode for gate delays.
- `-ignore_zero_delay <bool>`: Ignores processing of #0 delays.
- `-insert_clock_delay_port_in_module <string>`: Defines `clockDelayPort` in module name.
- `-instance_name <string>`: Specify the instance name of clock delay port. delay port instance name.

- `-module <list>`: Lists clock delay modules.
- `-perf_mode <int>`: `clock_delay` performance modes. Only valid for ZS4 onwards. Default Value is 0.
  - 0 - No additional performance optimizations
  - 1 - Module level clock delay replication
  - 2 - FPGA level clock delay replication
  - 3 - No replication, clock delays and $time consumers moved to terminal FPGA
  - 4 - No replication, clock delays moved to terminal FPGA. `$time` consumers stay on any partitioned FPGA. non-negative integer number.
- `-phase <int>`: Sets phase for clock delay port defined in UTF command. non-negative integer number.
- `-reset_duration <int>`: Sets `resetDuration` for clock delay port defined in UTF command. non-negative integer number.
- `-reset_value <int>`: Sets `resetValue` for clock delay port defined in UTF command. non-negative integer number.
- `-reset_wire <string>`: Resets path.
- `-sdc_mcp_mode <int>`: `clock_delay` based support for SDC MCP computation Only valid for ZS4 onwards.
  - 0 - Without any tolerance optimization
  - 1 - Default `clock_delay` tolerance optimization
  - 2 - Tolerance with edges aligned at LCM periods of the clocks
  - 3 - Tolerance with edges aligned with the fastest clock
  - 4 - Tolerance with edges aligned with the posedge of the fastest clock. non-negative integer number.
- `-tolerance <int>`: Sets tolerance for clock_delay. non-negative integer number.

Constraint(s)

`-clockdelayport_timescale` is to set in a valid format.

3 Clustering

This section describes the following UTF commands:

- *clustering*
- *cluster_constraint*
- *set_zcei_partition*
- *defmapping*

3.1 clustering

Description

Specify clustering related parameters

```
clustering [-atomic_module <list>] [-auto_block_selection <bool>] [-
core_adaptive_filling_rates <bool>] [-core_incremental_partitioning
<bool>] [-core_partitioning_goal <density|performance>] [-
core_timing_optimization
<none|post_partitioning|partitioning_driven>] [-input_mapping_file
<file>] [-netlist_file_mode <gzfile|gzstream|stream>] [-
output_mapping_file <file>] [-resource_usage
<Safe|Medium|Aggressive>] [-resource_usage_details
<bram=string,dsp=string,fwc_bit=string,lut=string,lutram=string,qiwc=
string,ramlut=string,reg=string,sdt=string,sdt_bits=string>] [-
routability_aware <bool>] [-routability_aware_params
<effort_level=enum,num_threads=string>] [-system_auto_core_generation
<bool>] [-system_auto_core_generation_advanced_command <string>] [-
system_auto_core_generation_advanced_file <file>] [-
system_core_definition_file <file>] [-system_incremental_partitioning
<bool>] [-system_timing_optimization
<none|post_partitioning|partitioning_driven>]
```

Option(s)

- `-atomic_module <list>`: **zTopBuild** cluster model.
- `-auto_block_selection <bool>`: Enables/disables Automatic Block Selection. This big grain hierarchy based partitioning model block selection improves the partitioner's speed, memory usage and the quality of result for the designs with a well structured hierarchical tree in its upper levels.
- `-core_adaptive_filling_rates <bool>`: Enables adaptive filling rates.
- `-core_incremental_partitioning <bool>`: Enables incremental partitioning.
- `-core_partitioning_goal <density|performance>`: Specify core partitioning goal.
  - `density`: Density oriented **zCore** level partitioner.

  - **Valid values**: density|DENSITY
  - performance: Performance oriented **zCore** level partitioner.
  - **Valid values**: performance|PERFORMANCE
- -core_timing_optimization <none|post_partitioning|partitioning_driven>: Specify core partitioning timing optimization mode.
  - none: No timing optimization.
  - **Valid values**: none|NONE
  - post_partitioning: Post partitioning timing optimization.
  - **Valid values**: post_partitioning|POST_PARTITIONING
  - partitioning_driven: Partitioning driven timing optimization.
  - **Valid values**: partitioning_driven|PARTITIONING_DRIVEN
- -input_mapping_file <file>: Specify filename with complete mapping. Mutually exclusive from all other options.
- -netlist_file_mode <gzfile|gzstream|stream>: Specify modes for driving netlist file from **zTopBuild** to **zTopClustering**.
  - gzfile: gzipped netlist file (default)
  - **Valid values**: gzfile|GZFILE
  - gzstream: gzipped netlist file through a pipe
  - **Valid values**: gzstream|GZSTREAM
  - stream: netlist file through a pipe
  - **Valid values**: stream|STREAM
- -output_mapping_file <file>: Specify output mapping file.
- -resource_usage <Safe|Medium|Aggressive>: Specify resource utilization targets.
  - Safe: Low filling rates.
  - **Valid values**: Safe|safe|SAFE
  - Medium: Standard filing rates.
  - **Valid values**: Medium|medium|MEDIUM

- Aggressive: High filling rates.
- **Valid values**: Aggressive|aggressive|AGGRESSIVE

- -resource_usage_details <bram=string,dsp=string,fwc_bit=string,lut=string,lutram=string,qiwc=string,ramlut=string,reg=string,sdt=string,sdt_bits=string>: Specify manual resource utilization targets.
  - Available resources types are: dsp, bram, lut, reg, ramlut, sdt, sdt_bits and qiwc.
  - bram <string>: bram fillrate in %. fillrate
  - dsp <string>: dsp fillrate in %. fillrate
  - fwc_bit <string>: fwc bit fillrate in %. Valid values: fwc bit fillrate
  - lut <string>: lut fillrate in %. fillrate
  - lutram <string>: ramlut fillrate in %. fillrate
  - qiwc <string>: qiwc fillrate in %. fillrate
  - ramlut <string>: ramlut fillrate in %. fillrate
  - reg <string>: reg fillrate in %. fillrate
  - sdt <string>: sdt fillrate in %. fillrate
  - sdt_bits <string>: sdt bits fillrate in %. bits fillrate
  - bram <string>: bram fillrate in %. fillrate
  - dsp <string>: dsp fillrate in %. fillrate
  - lut <string>: lut fillrate in %. fillrate
  - lutram <string>: ramlut fillrate in %. fillrate
  - qiwc <string>: qiwc fillrate in %. fillrate
  - ramlut <string>: ramlut fillrate in %. fillrate
  - reg <string>: reg fillrate in %. fillrate
  - sdt <string>: sdt fillrate in %. fillrate
  - sdt_bits <string>: sdt bits fillrate in %. bits fillrate
- -routability_aware <bool>: Enable/disable routability aware clustering mode.

- `-routability_aware_params <effort_level=enum,num_threads=string>`: Set advanced routability analysis parameters values. Number of threads can be positive integer value or MAX for maximal available number of threads (default).
- `effort_level <LOW|MEDIUM|HIGH>`: Specify routing effort level.
  - `LOW`: low effort level
  - **Valid values**: `LOW|Low|low`
  - `MEDIUM`: medium effort level
  - **Valid values**: `MEDIUM|Medium|medium`
  - `HIGH`: high effort level
  - **Valid values**: `HIGH|High|high`
- `num_threads <string>`: It is a positive integer value or `MAX` for maximal available number of threads (default).
  - `<int> | MAX`
- `-system_auto_core_generation <bool>`: Enable automatic `zcore` generation.
- `-system_auto_core_generation_advanced_command <string>`: Specify advanced command for **zTopClustering**. command
- `-system_auto_core_generation_advanced_file <file>`: Specify advanced command file for automatic `zcore` generation.
- `-system_core_definition_file <file>`: Specify filename with `zcore` (`defcore`) definitions.
- `-system_incremental_partitioning <bool>`: Enables incremental partitioning.
- `-system_timing_optimization <none|post_partitioning|partitioning_driven>`: Specify system partitioning timing optimization mode.
  - `none`: No timing optimization.
  - **Valid values**: `none|NONE`
  - `post_partitioning`: Post partitioning timing optimization.
  - **Valid values**: `post_partitioning|POST_PARTITIONING`

- partitioning_driven: Partitioning driven timing optimization.
- **Valid values**: partitioning_driven|PARTITIONING_DRIVEN

Constraint(s)

At least one of the options should be used

- -input_mapping_file cannot be used with any of the following options:
  - -system_auto_core_generation
  - -system_auto_core_generation_advanced_file
  - -system_auto_core_generation_advanced_command
  - -system_timing_optimization
  - -system_incremental_partitioning
  - -system_core_definition_file
  - -resource_usage
  - -resource_usage_details
  - -core_partitioning_goal
  - -core_adaptive_filling_rates
  - -core_incremental_partitioning
  - -core_timing_optimization
- -resource_usage cannot be used with -resource_usage_details.

Note(s)

- To enable -system_auto_core_generation_advanced_file \<file\>, use -system_auto_core_generation.
- -system_auto_core_generation_advanced_file \<file\> is valid when -system_auto_core_generation \<bool\> mode is enabled, or when design_size is greater than one module.

Example(s)

```
clustering -resource_usage_details { lut =60, reg= 30, dsp = 50 }
clustering -resource_usage_details lut=60,dsp=50,fvt=75
```

clustering

3.2 cluster_constraint

Description

Specify clustering constraints

```
cluster_constraint [-accept_overflow
<bram=int,dsp=int,lut=int,ramlut=int,reg=int>] [-
allow_ovrd_user_max_fill <bool>] [-command
<merge_blocks|add_group|defcore>] [-exclusive <bool>] [-fnmatch
<bool>] [-group_name <string>] [-instance  <list>] [-level
<core|fpga|both>] [-max_fpga <int>] [-min_fpga <int>] [-overflow
<bram=int,dsp=int,lut=int,ramlut=int,reg=int>] [-rtlname] [-
set_max_fill
<bram=int,dsp=int,fwc_bit=int,fwc_ip=int,lut=int,qiwc=int,ramlut=int,
read_port_
bit=int,read_port_ip=int,reg=int,write_port_bit=int,write_port_ip=int
,zcei_mess_in=int,zcei_mess_out=int>]
```

Option(s)

- `-accept_overflow <bram=int,dsp=int,lut=int,ramlut=int,reg=int>`: Allows filling rates overflow for different types of logic elements according to specified percentage.

  Available logic elements are: `reg, lut, ramlut, bram, dsp`. Default are respectively 5, 10, 10, 0, 0.

  - `bram <int>`: bram overflow in %. non-negative integer number.
  - `dsp <int>`: dsp overflow in %. non-negative integer number.
  - `lut <int>`: lut overflow in %. non-negative integer number.
  - `ramlut <int>`: ramlut overflow in %. non-negative integer number.
  - `reg <int>`: reg overflow in %. non-negative integer number.
- `-rtlname`: Specifies if the input path is interpreted as `RTLNAME`. The default is `false`. The option is used with the `ADD_GROUP` command.

- `-allow_ovrd_user_max_fill <bool>`: Allows to AC algorithm override user settings on `max_fill` constraints.
- `-command <merge_blocks|add_group|defcore>`: Specifies `cluster_constraint` command.
- `merge_blocks`: The auto-clustering retains the specified blocks on the same FPGA. The command can handle multiple statements sharing a common block, in this case all the blocks are merged. This command handle hierarchy overlapping in the following way: if an instance of the hierarchy is touched by several `merge_block` commands, the `merge_block` command that references the closest of its ancestor is selected.
  - **Usage:** `cluster_constraint -command MERGE_BLOCKS -instance <list> [-level CORE|FPGA|BOTH] [-fnmatch <bool>]`

    Valid values: `merge_blocks|MERGE_BLOCKS`
- `add_group`: Defines a logic group of instances that might require the resources of more than one FPGA. One can define multiple groups with several commands. Any instance that does not belong to a group is attached to the default group. It is possible to create a real partitioning of the design by means of group definitions if one declares a group at the top of the design. Therefore, there are no mixing of instances attached to groups and instances attached to the default group.
  - **Usage:** `cluster_constraint -command ADD_GROUP -group_name <string> -instance <list> [-exclusive <bool>] [-fnmatch <bool>] [-max_fpga <int>] [-min_fpga <int>] [-overflow reg=<percentage>,lut=<percentage>,ramlut=<percentage>,bram=<percentage>,dsp=<percentage>]`

    Valid values: `add_group|ADD_GROUP`
- `defcore`: Appends a list of instance paths to be handled as a core and processed altogether. Automatic-clustering uses these definitions to find the best partitioning of the design.
  - **Usage:** `cluster_constraint -command DEFCORE -group_name <string> -instance <list>`

    Valid values: `defcore|DEFCORE`

- `-exclusive <bool>`: No blocks belonging to the default group can be mapped on this core, core is isolated. Default is false. The option is used with `-command ADD_GROUP`.
- `-fnmatch <bool>`: Specifies if the other parameters are interpreted as pattern. The default is false. The option is used with `-command MERGE_BLOCKS` and `-command ADD_GROUP`.
- `-group_name <string>`: Assigns a name to the group of instances. Mandatory option used with `-command ADD_GROUP` and `-command DEFCORE`.
- `-instance <list>`: Specifies a list of instance paths to be grouped together. This group must fit on one FPGA. The option could be used with `MERGE_BLOCKS`, `ADD_GROUP` and `DEFCORE -command` option.
- `-level <core|fpga|both>`: Specifies which tool processes the command core level partitioner (**zTopBuild**,) FPGA level partitioner (**zCoreBuild**) or both. The default is both. The option could be used with `-command MERGE_BLOCKS` and `-command ADD_GROUP`.
  - `core`: Core level.

    Valid values: core|CORE
  - `fpga`: FPGA level.

    Valid values: `fpga|FPGA`
  - `both`: Both core and FPGA level.

    Valid values: `both|BOTH`
- `-max_fpga <int>`: Constraint that specifies the maximum number of FPGAs allowed for this group. The option used with `-command ADD_GROUP`. non-negative integer number.
- `-min_fpga <int>`: Reserves at least this number of FPGA for the group. The option used with `-command ADD_GROUP`. non-negative integer number.
- `-overflow <bram=int,dsp=int,lut=int,ramlut=int,reg=int>`: Specifies overflow percentage which is allowed for different types of logic elements.

  Available logic elements are: `reg, lut, ramlut, bram, dsp`. Defaults are respectively 5, 10, 10, 0, 0. The option used with `-command ADD_GROUP`.

  - `bram <int>`: bram overflow in %. non-negative integer number.
  - `dsp <int>`: dsp overflow in %. non-negative integer number.
  - `lut <int>`: lut overflow in %. non-negative integer number.
  - `ramlut <int>`: ramlut overflow in %. non-negative integer number.
  - `reg <int>`: reg overflow in %. non-negative integer number.
- `-rtlname`: Specifies if the input path is interpreted as `RTLNAME`. The default is false. The option is used with `-command ADD_GROUP`.
- `-set_max_fill <bram=int,dsp=int,fwc_bit=int,fwc_ip=int,lut=int,qiwc=int,ramlut=int,read_port_bit=int,read_port_ip=int,reg=int,write_port_bit=int,write_port_ip=int,zcei_mess_in=int,zcei_mess_out=int>`: Specifies maximum FPGA filling rates for different types of logic elements that consume FPGA hardware resources.

  Available logic elements are: `reg, lut, ramlut, bram, dsp, qiwc, fwc_bit, fwc_ip, read_port_bit, read_port_ip, write_port_bit, write_port_ip, zcei_mess_in, zcei_mess_out`.
  - `bram <int>`: bram fillrate in %. non-negative integer number.
  - `dsp <int>`: dsp fillrate in %. non-negative integer number.
  - `fwc_bit <int>`: fwc bit fillrate in %. non-negative integer number.
  - `fwc_ip <int>`: fwc ip fillrate in %. non-negative integer number.
  - `lut <int>`: lut fillrate in %. non-negative integer number.
  - `qiwc <int>`: qiwc fillrate in %. non-negative integer number.
  - `ramlut <int>`: ramlut fillrate in %. non-negative integer number.
  - `read_port_bit <int>`: read port bit fillrate in %. non-negative integer number.
  - `read_port_ip <int>`: read port ip fillrate in %. non-negative integer number.
  - `reg <int>`: reg fillrate in %. non-negative integer number.

- `write_port_bit <int>`: write port bit fillrate in %. non-negative integer number.
- `write_port_ip <int>`: write port ip fillrate in %. non-negative integer number.
- `zcei_mess_in <int>`: zcei message in fillrate in %. non-negative integer number.
- `zcei_mess_out <int>`: zcei message out fillrate in %. non-negative integer number.

Constraint(s)

At least one of the options should be used

`-command` can only be used with `-instance`

`-instance` can only be used with `-command`

`-command DEFCORE` option without setting `-group_name` option

`-command DEFCORE` with at least one on of: `-fnmatch, exclusive, -min_fpga, -max_fpga` and `-overflow`

`-command MERGE_BLOCKS` with at least one on of: `-group_name, exclusive, -min_fpga, -max_fpga` and `-overflow`

`-command ADD_GROUP` option without setting `-group_name` option

Note(s)

`-set_max_fill, -allow_ovrd_user_max_fill, -accept_overflow` options can be specified without `-command` option.

Example(s)

```
cluster_constraint -set_max_fill {reg = 90, lut = 50 }
cluster_constraint -set_max_fill qiwc=90,bram=70
```

3.3 set_zcei_partition

Description

For **zTopBuild**, specify FPGA for zcei partition

```
set_zcei_partition [-use_fpga <string>]
```

Option(s)

`-use_fpga <string>`: Specify the target FPGA for zcei partition.

Constraint(s)

At least one of the options should be used

3.4 defmapping

Detailed Description

```
defmapping  [-path <mod_inst_name|top_module_name>] [-use_fpga
<fpga_name>] [-object_source [rtl|edif]] [-object_not_found
[fatal|warning]]
```

Parameters

- `args`
- `-path #hierarchy_name`: Specify hierarchical path of a design block, could be an instance or top module.

Note

On ZS3 HW configuration, the hierarchical instance cannot be a transactor.

- `-use_fpga #fpga_name`: Specify FPGA used for given path; `fpga_name` should be in format: `U[0-31].M[0-5].F[0-18]`
- `-object_source [edif|rtl]`: Specifies the source of objects.

  Available policies:

  - `rtl`: Default value. The object is from RTL, a fatal error is displayed in VCS if object not found.
  - `edif`: The object is from Edif, path verification would be performed in ZEBU backend instead of VCS.
  - `-object_not_found [fatal|warning]`: Specifies the mode when invalid path is specified.

    Available policies:

    - `fatal`: Default value. A fatal error is displayed in VCS if the value of option path is not found.
    - `warning`: Only a warning message is displayed in VCS if the value of option path is not found.

Examples

```
defmapping -path Top.inst1 -use_fpga U0.M0.F0 -object_source edif
```

defmapping

4 Compile

This section describes the following UTF commands:

- *compile*
- *disk_space_checker*
- *fpga*
- *global_db*
- *post_compile_command*
- *pre_compile_command*
- *profile*
- *set_hwtop*
- *vcs_exec_command*

4.1 compile

Description

This command specifies compile related options.

```
compile  [-hydra <bool>][-incremental <bool>] [-incremental_params
<netlist_edition=bool,partition=bool,pnr=bool,synthesis=bool,system_r
oute=bool>] [-objective <None|Fast_Turn_Around|Performance|Capacity>]
```

Option(s)

- `-hydra <bool>`: Enable/disable the hydra flow. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-incremental <bool>`: enable/disable incremental compile.
- `-incremental_params <netlist_edition=bool,partition=bool,pnr=bool,synthesis=bool,system_route=bool>`: Specify incremental parameters.

  Available parameter types are: `synthesis, partition, system_route, pnr, netlist_edition`.

  - `netlist_edition <bool>`: enable/disable advanced incremental netlist mode.
  - `partition <bool>`: enable/disable partition incremental compile.
  - `pnr <bool>`: enable/disable P&R incremental compile.
  - `synthesis <bool>`: enable/disable synthesis incremental compile.
  - `system_route <bool>`: enable/disable `system_route` incremental compile.
- `-objective <None|Fast_Turn_Around|Performance|Capacity>`: define compilation objective
  - Valid values: `objective type`

Constraint(s)

At least one of the options should be used

Example(s)

```
compile -incremental true
```

```
compile -incremental true -incremental_params
{synthesis=false,partition=true,system_route=false,pnr=true,netlist_e
dition=true}
```

4.2 disk_space_checker

Description

Disk space checker options

```
disk_space_checker -enable <bool> [-command <string>] [-constants
<core=float,elab=float,pp_fpga=float,synth=float,system=float>] [-
constants_mode <AUTO|MANUAL>] [-email_address <string>] [-
email_address_batch <string>] [-email_notification
<NONE|BATCH|GUI|ALL>] [-log_notification <NONE|BATCH|GUI|ALL>] [-
warning_box_notification <bool>]
```

Option(s)

- `-command <string>`: Shell command is executed if there is no more disk space. command to be executed
- `-constants <core=float,elab=float,pp_fpga=float,synth=float,system=float>`: Relevant only in MANUAL constants mode. Assign a positive floating point value to a compilation step constant.

  Constant value can be: `elab, synth, system, core` or `pp_fpga`.

  - `core <float>`: `core`. non-negative float number.
  - `elab <float>`: `elab`. non-negative float number.
  - `pp_fpga <float>`: `pp_fpga`. non-negative float number.
  - `synth <float>`: `synth`. non-negative float number.
  - `system <float>`: `system`. non-negative float number.
- `-constants_mode <AUTO|MANUAL>`: In `AUTO` mode, `-constants` options shouldn't be provided. **Default**: `AUTO`.
- `-email_address <string>`: Indicates the email address used to inform the user about the missing disk space. Required if `-email_notification==BATCH|ALL`. address used to inform the user
- `-email_address_batch <string>`: Indicates the email address used to inform the user about the missing disk space. Required if `-email_notification==BATCH|ALL`. address used to inform the user about

- `-email_notification <NONE|BATCH|GUI|ALL>`: Enables the notification by email about the missing disk space in batch/GUI or both modes, `NONE` disables it. **Default**: `NONE`.
- `-enable <bool>`: Activates or deactivates disk space checker functionality. This option is mandatory.
- `-log_notification <NONE|BATCH|GUI|ALL>`: Enables the notification in log file about the missing disk space in batch/GUI or both modes, `NONE` disables it. **Default**: `NONE`.
- `-warning_box_notification <bool>`: Activates a warning box to notify the user about the missing disk space. **Default**: `false`.

Constraint(s)

At least one of the options should be used

Note(s)

- `elab, synth`: Common to all backends. Cannot be used inside `create_new_target blocks`.
- `system, core, pp_fpga`: backend settings applied on current target context.

4.3 fpga

Description

Specify fpga PAR options

```
fpga [-advanced_command_file <file>] [-complexity_predictor <bool>]
[-complexity_predictor_bundle_size <int>] [-debug_policy
<Disabled|Enabled|Expert>] [-file_policy <Regular|Compress|Suppress>]
[-first_par_policy <Original|Winner|Both|BothAnyway>] [-inter_die_tdm
<bool>] [-inter_die_tdm_params <strategy=enum>] [-local_disk_path
<string>] [-name <list>] [-param <string>] [-parff <t|f|MULTI_STAGE>]
[-parff_multi_stage <bool>] [-parff_winner_strategy
<Early|Regular|BestTiming>] [-use_local_disk <bool>]
```

Option(s)

- `-advanced_command_file <file>`: Specify advanced command file to specify PARFF settings.
- `-complexity_predictor <bool>`: Enables or disables FPGA complexity predictor. Default value: false.
- `-complexity_predictor_bundle_size <int>`: Number of FPGAs in each complexity predictor bundle. Default value is 8. positive integer number.
- `-debug_policy <Disabled|Enabled|Expert>`: Specify debug policy.
  - `Disabled`: Improve disk space regarding P&R information

    Valid values: `Disabled|DISABLED|disabled`
  - `Enabled`: Enable some Vivado reports

    Valid values: `Enabled|ENABLED|enabled`
  - `Expert`: Launch specific PARFF strategies files for design analysis

    Valid values: `Expert|EXPERT|expert`
- `-file_policy <Regular|Compress|Suppress>`: Specify file policy.

- `-first_par_policy <Original|Winner|Both|BothAnyway>`: Specify first FPGA P&R policy. Only valid with incremental **zPar** "`zpar -incremental`".
- `-inter_die_tdm <bool>`: enable PDM.
- `-inter_die_tdm_params <strategy=enum> {strategy=PDM_DIRECT|PDM_PARFF}`.
  - `strategy <Pdm_Direct|Pdm_Parff>`: Specify PDM strategy.
    - `Pdm_Direct`: PDM is enabled even for Original compilation. User defines which PARFF stages that they also like to introduce PDM based on the PARFF file. **Valid values**: `Pdm_Direct|PDM_DIRECT|pdm_direct`
    - `Pdm_Parff`: User defines which PARFF stages that they like to introduce PDM based on the PARFF file. **Valid values**: `Pdm_Parff|PDM_PARFF|pdm_parff`
- `-local_disk_path <string>`: local disk compilation path
- `-name <list>`: list of FPGA names.
- `-param <string>`: fpga params.
- {par_name1=some_value1, par_name2=some_value2,...}
- `-parff <t|f|MULTI_STAGE>`: Enables or disables parallel automatic recompilation of failing FPGAs. Default value is `false`.
- `-parff_multi_stage <bool>`: Enables or disables parallel automatic recompilation of failing FPGAs - multi stage mode. Default value is `false`.
- `-parff_winner_strategy <Early|Regular|BestTiming>`: Specify parff winner detection strategy.
- `-use_local_disk <bool>`

Constraint(s)

At least one of the options should be used

- `-param` can only be used with `-name` and vice versa.

Note(s)

- `-parff_multi_stage t` also implicitly enables `-parff`. `-parff f -parff_multi_stage t` is not a legal combination.
- If `-use_local_disk` is set to true then directory path must be supplied using `-local_disk_path`.

Example(s)

```
-param par1=val1,par1=val2 or -param {par1=val1, par2=val2}
```

4.4 global_db

Description

```
global_db [-merge_start_fpga_percent <int>] [-number_of_threads
<int>]
```

Option(s)

- `-merge_start_fpga_percent <int>`: In order to shorten compile time (wall clock), this option allows to start the global DB merger already after a set percentage of passing (P&R) FPGAs. non-negative integer number.
- `-number_of_threads <int>`: Specify the number of threads can be used by the `DB_Global`. Valid values: A non-negative integer number.

Constraint(s)

At least one of the options should be used

4.5 post_compile_command

Description

post compilation command for **zCui**

```
post_compile_command [-on_error <ignore|exit>] [<script>]
```

Option(s)

- `-on_error`
  - `ignore`: `ignore` is default.
  - `exit`: Exits compilation on post-compilation errors.
- `script <string>`: Script commands to be executed after compilation.

Constraint(s)

At least one of the options should be used

4.6 pre_compile_command

Description

pre compilation command for **zCui**

```
pre_compile_command [-on_error <ignore|exit>] [<script>]
```

Option(s)

- `-on_error`
  - `ignore`: `ignore` is default.
  - `exit`: Exits compilation on pre-compilation errors.
- `script <string>`: Script commands to be executed before compilation.

Constraint(s)

At least one of the options should be used

4.7 profile

Detailed Description

At least one of the options:

- `-compile <bool>`: Enable profiled compile.
- `-xtors <bool>`: Enable/disable zTune transactional profiler.
- `-xtors_params {param1=val1, param2=val2, ..., paramN=valN>}`: Configure **zTune** transactional profiler. Valid parameters are:

  `TYPE=ZEMI_GLOBAL|ZEMI_DPI|ZEMI_GLOBAL_DPI|LEGACY`

  - `ZEMI_GLOBAL`: profile global (sampling/internal/dpi/b2b) clock stopping for ZEMI transactors
  - `ZEMI_DPI`: profile per DPI clock stopping for ZEMI transactors
  - `ZEMI_GLOBAL_DPI`: profile both global and per DPI clock stopping for ZEMI transactors
  - `LEGACY`: legacy profiling (per transactor zceiClockControl)
- `-dumpvars_report <bool>`: Enable dumping of full `$dumpvars` stats in `dump_num_bits.csv`.
- `-dumpports_report <bool>`: Enable dumping of full `$dumpports` stats in `dump_num_bits.csv`.

4.8 set_hwtop

Description

Specify hardware top module name

```
set_hwtop [-module <string>]
```

Option(s)

- `-module <string>`: Top-level module name

Constraint(s)

At least one of the options should be used

Example(s)

```
set_hwtop -module top_module_name
```

4.9 vcs_exec_command

Description

Specify VCS Command line

```
vcs_exec_command <script>
```

Option(s)

- `script <list>`: `vcs_command_line_or_script` VCS command. Mandatory option

Constraint(s)

At least one of the options should be used

5 converged_flow

Functions

```
converged_flow args
```

Detailed Description

This command is no longer supported. You need to specify a ZeBu Companion architecture file to enable the flow.

6 Cosimulation

This section describes the following UTF commands:

- *environment*
- *set_dualedge*
- *simxl*
- *simxl_allow_concurrent*
- *simxl_enable_zdpi*
- *simxl_move_tf_to_tb*
- *simxl_move_to_tb*
- *simxl_set_hwtop*

6.1 environment

Description

Testbench environment options

```
environment [-generate_wrapper <NONE|C|CPP|SYSTEMC|VHDL|VERILOG>]
```

Option(s)

`-generate_wrapper <NONE|C|CPP|SYSTEMC|VHDL|VERILOG>`: Generate C, C++, SystemC, Verilog, VHDL wrapper or `NONE` restores to default settings.

Constraint(s)

At least one of the options should be used

6.2 set_dualedge

Description

set dual edge

```
set_dualedge [-instance <string>]
```

Option(s)

- `-instance <string>`: Represents instance path

Constraint(s)

At least one of the options should be used

Note(s)

Set value "`yes`" to `defparam` '`dualedge`' of a given `C_COSIM` instance.

6.3 simxl

Description

This command indicates the operation mode in time coupled simulation acceleration with HDL testbench. If it is set to false or if the command is not specified, acceleration behaves as legacy `HDL_COSIM` mode (time decoupled). User can also specify the mode of execution either congruent or fast mode. Congruent mode is by default. However, the 'mode' option has no effect if the 'enable' option is set to false.

```
simxl [-enable <bool>] [-mode <congruent|fast>]
```

Option(s)

- `-enable <bool>`: Specify whether the simxl flow is enabled or not.
- `-mode <congruent|fast>`: Specify whether the execution mode is congruent or fast. Default is congruent.

Constraint(s)

At least one of the following options should be used: `-enable`

Example(s)

```
simxl -enable TRUE -mode FAST
```

6.4 simxl_allow_concurrent

Description

Allow concurrent calls of SW->HW tasks/functions

```
simxl_allow_concurrent -module <string> -tf <list> [-count <int>]
```

Option(s)

- `-count <int>`: Number of concurrent calls of task/function allowed. positive integer number.
- `-module <string>`: Specify the name of the target module. the name of the target module. Mandatory option
- `-tf <list>`: Specify the SW->HW tasks/functions that can be called concurrently. Mandatory option

Example(s)

```
simxl_allow_concurrent -module subdut -tf {TASK1 FUNC1} -count 3
```

6.5 simxl_enable_zdpi

Description

Enable **zDPI** in DUT modules in SimXL flow

```
simxl_enable_zdpi [-all <bool>] [-module <list>]
```

Option(s)

- `-all <bool>`: Specify if **zDPI** needs to be enabled for all modules.
- `-module <list>`: Specify modules for which **zDPI** needs to be enabled.

Constraint(s)

At least one of the options should be used

Example(s)

```
simxl_enable_zdpi -all
simxl_enable_zdpi -module {module1 module2}
```

6.6 simxl_move_tf_to_tb

Description

In SimXL mode, we target to provide the same or similar emulation environment as simulator and we encourage user to use task and function to exchange data between TB and DUV for performance.By moving those tasks and functions to TB, we can resolve performance or HW resource issues or provide solutions for those unsupported cases.

```
simxl_move_tf_to_tb [-module <string>] [-target <list>] [-tf <list>]
```

Option(s)

- `-module <string>`: Specify the name of the target module. the name of the target module.
- `-target <list>`: Specify which tasks/functions need be moved from DUT to TB. All the task/function definition in DUT are moved to TB.
- `-tf <list>`: Specify which tasks/functions need be moved from DUT to TB. All the task/function definition in DUT are moved to TB.

Constraint(s)

At least one of the options should be used

Example(s)

```
simxl_move_tf_to_tb -module subdut -tf {TASK1 FUNC1}
```

6.7 simxl_move_to_tb

Description

There might be some behavior code in some modules which are instantiated in DUT (HW). This command indicates all such module instantiations in DUT are moved to TB. User can also specify some instances being moved to TB if necessary. At least one option should be specified.

```
simxl_move_to_tb [-instance <list>] [-module <list>]
```

Option(s)

- `-instance <list>`: Specify some extra hierarchy instances in DUT need be moved to TB.
- `-module <list>`: Specify which modules need be moved from DUT to TB. All the module instantiations in DUT are moved to TB.

Constraint(s)

At least one of the options should be used

Example(s)

```
simxl_move_to_tb -module {TOP1 TOP2} -instance {TOP3.dut.I1
TOP3.dut.I2}
```

6.8 simxl_set_hwtop

Description

Specify hardware top module or instance names in SimXL flow. Multiple top modules and full hierarchy instances can be set as hardware top.

```
simxl_set_hwtop [-instance <list>] [-module <list>]
```

Option(s)

- `-instance <list>`: Specify full hierarchy instances to be moved to HW.
- `-module <list>`: Specify top-level modules to be moved to HW.

Constraint(s)

At least one of the options should be used

Example(s)

```
simxl_set_hwtop -module {TOP1 TOP2} -instance {TOP3.dut.I1
TOP3.dut.I2}
```

7 Coverage

This section describes the following UTF commands:

- *code_coverage*
- *coverage*

7.1 code_coverage

Description

This command is used to enable code coverage.If enabled, the default state is that force/release statements are honored.If disabled, the default state is that force/release statements are ignored.

```
code_coverage [-line <bool>]
```

Option(s)

- `-line <bool>`: Enable line coverage..

Constraint(s)

At least one of the options should be used

7.2 coverage

Description

This command is used to enable and disable coverage collection feature.

```
coverage [-auto_bin_max <int>] [-enable <bool>]
```

Option(s)

- `-auto_bin_max <int>`: Set global auto bin max value. non-negative integer number.
- `-enable <bool>`: Enables or disables the tracking in the compilation.

Constraint(s)

At least one of the options should be used

8 Debug

This section describes the following UTF commands:

- *csa*
- *debug*
- *probe_config*
- *probe_signals*
- *set_sram_trace*
- *set_trigger*

8.1 csa

Detailed Description

```
csa [-disable]
```

- `-disable`: disable `csa` command

Note (s)

- `csa` command forces optimization to be `noopt` (same as using `optimization -no|-noopt|-no_opt`)
- `csa` command also implicitly enables `debug -set_dyn_probes_on_dut_ios t`

8.2 debug

Description

Debug options

```
debug [-add_clock_counters <bool>] [-advanced_command_file <file>] [-
always_accessible <file>] [-csa <bool>] [-csa_header <bool>] [-
dumpports_maxbits <int>] [-dumpvars_maxbits <int>] [-enable_bram_rw
<bool>] [-enable_hwtop_ports_access
<none|input|output|inout|all|select>] [-memory_backdoor
<all|readmem|none|selected>] [-memory_backdoor_instances <list>] [-
notifier <asn|uip|false>] [-notifier_params
<asn_max_bits=int,asn_max_fanins=int,asn_mode=enum,asn_post_compilati
on_cel=file,asn_zcore_only=bool,uip_cel_file=file,uip_msg_cnl=enum,ui
p_opt=enum,uip_preserve_bits=int,uip_signal_file=file,uip_udp_num=int
,uip_udp_width=enum>] [-offline_debug <bool>] [-offline_debug_params
<incl_xtors=bool>] [-rtlname <list>] [-set_dyn_probes_on_dut_ios
<bool>] [-set_dyn_probes_on_memory_ios <bool>] [-verdi_db
<true|false|old>] [-waveform_reconstruction <bool>] [-
waveform_reconstruction_params
<csa=bool,partitions=int,simzilla=enum,simzilla_distributed_build=boo
l,swave=enum>]
```

Option(s)

- `-add_clock_counters <bool>`: Add clock counters for debugging glitches.
- `-advanced_command_file <file>`: Command file for `zDbPostProc` (Example: importing memories).
- `-always_accessible <file>`: File with dynamic probes that should alway be accessible.
- `-csa <bool>`: if true enables `csa`, if `false` disables `csa` (disregard all previous commands which enable `csa`).
- `-csa_header <bool>`: if `true` enables `csa` with header, if `false` enables `csa` without an header.

- -dumpports_maxbits <int>: Specify max number of bits allowed to be dumped per a single dumpports command. non-negative integer number.
- -dumpvars_maxbits <int>: Specify max number of bits allowed to be dumped per a single dumpvars command. non-negative integer number.
- -enable_bram_rw <bool>: Enable BRAM read/write logging. Only required for offline debugging with RLDRAM instantiations.
- -enable_hwtop_ports_access <none|input|output|inout|all|select>: Enable ports in hw top module and attach debug probes/dve registers. Option select requires -rtlname to be provided.
- -memory_backdoor <all|readmem|none|selected>: Add backdoor access for memories in ZeBu Companion flow.
  - all: add backdoor access to all memory instances in the netlist.

    Valid values: all|ALL
  - readmem: add backdoor access to memory instances related to $readmem in design

    Valid values: readmem|READMEM
  - none: add backdoor access to all memory instances in the netlist.

    Valid values: none|NONE
  - selected: add backdoor access to memory instances specified by the '-memory_backdoor_instances' option.

    Valid values: selected|SELECTED
- -memory_backdoor_instances <list>: Specify memory instances for backdoor access enabling (when the "-memory_backdoor selected" option is used). Wild card name is supported.Cannot accept escape name. If you really want to use escape name, use underscore instead of backslash. For example, use '123mem' instead of 'Smem '.
- -notifier <asn|uip|false>: Enable/Disable the notifier and debug dumping.
  - asn: The Notifier engine integrated.The list of signal are applied to the Notifier engine with the ECO flow.

    Valid values: asn|ASN

- uip: The Notifier engine is integrated with a 1st list of signals. They are provided with a text file or with an FSM described with CEL language.After compilation, the list of signals can be updated thanks to the $dumpvars task call definitions applied at compile timeBelow UIP parameters are available.

  Valid values: uip|UIP

- false: resets all previous setting of notifier and its params

- -notifier_params <asn_max_bits=int,asn_max_fanins=int,asn_mode=enum,asn_post_compilation_cel=file,asn_zcore_only=bool,uip_cel_file=file,uip_msg_cnl=enum,uip_opt=enum,uip_preserve_bits=int,uip_signal_file=file,uip_udp_num=int,uip_udp_width=enum> notifier params {param1=val1, param2=val2, ..., paramN=valN>}.

  - ASN_MAX_BITS <int>: Sets the bus width to specified size. non-negative integer number.
  - ASN_MAX_FANINS <int>: Enables to set the maximal fanin size Notifier Engines. non-negative integer number.
  - ASN_MODE <pipeline|accurate>: Defines the optimization target notifier collector tree.

    - pipeline: Reduce as much as possible frequency penalty. that is, try to avoid congested areas.

    Valid values: pipeline|PIPELINE

    - accurate: Reduce the maximal depth of the tree, that is, optimize the delay of notifier tree.

    Valid values: accurate|ACCURATE

  - ASN_POST_COMPILATION_CEL <file>: Enables user to set a list of signals he wants to track already when launching ZeBu.
  - UIP_CEL_FILE <file>: Specify the CEL file (complex event language) for notifier.
  - UIP_MSG_CNL <1|2|4>: Specify the message pair number for notifier. Default is 1.

- UIP_OPT <capacity|balanced|performance>: Specify the optimization strategy for debug dump.
  - capacity: allocate the largest number of debug resources.

  Valid values: capacity|CAPACITY
  - balanced: allocate the resource to balanced performance and capacity (default)

  Valid values: balanced|BALANCED
  - performance: allocate the resource for best performance.

  Valid values: performance|PERFORMANCE
- UIP_PRESERVE_BITS <int>: Preserve the debug resources for ECO. positive integer number.
- UIP_SIGNAL_FILE <file>: Specify the signals for notifier.

- -offline_debug <bool>: Insert sniffer infrastructure for Post-Run Debug.
- -offline_debug_params <incl_xtors=bool>: offline debug params (comma separated list of name=value pairs).
  - INCL_XTORS <bool>: Enable/disable the new Stimuli Capture and Replay. (when offline_debug is enabled).
- -rtlname <list>: Explicitly specify which top ports to provide debug visibility for.
- -set_dyn_probes_on_dut_ios <bool>: Add dyn probes on DUT IOs. Automatically enabled by csa.
- -set_dyn_probes_on_memory_ios <bool>: Add dyn probes on zMem IOs. Overridden by enable_register_w on newer versions. Automatically enabled by csa.
- -verdi_db <true|false|old>: Control VCS/Verdi flow.
  - true: Enable Post elaboration Verdi flow

  Valid values: true|TRUE|1|True|t|T|y|Y|yes|YES
  - false: Disable Verdi flow

  Valid values: false|FALSE|0|False|f|F|n|N|no|NO
  - old: Enable VCS Verdi flow

Valid values: old|OLD

- -waveform_reconstruction <bool>: Enable/disable all waveform reconstruction parameters.
- -waveform_reconstruction_params <csa=bool,partitions=int,simzilla=enum,simzilla_distributed_build=bool,swave=enum>: Enable/disable a series of debug parameters.
  - CSA <bool>
  - PARTITIONS <int>: number of graph partitions. Valid Values: A positive integer.
  - SIMZILLA <t|f|SEQUENTIAL>
    - t: Enable SIMZILLA

    Valid values: t|enabled|Enabled|ENABLED|true|True|TRUE
    - f: Disable SIMZILLA

    Valid values: f|disabled|Disabled|DISABLED|false|False|FALSE
    - SEQUENTIAL: Enable Sequential SIMZILLA

    Valid values: SEQUENTIAL|sequential|Sequential
    - SIMZILLA_DISTRIBUTED_BUILD <bool>
- SWAVE <enabled|disabled|gls|ENABLE_SEQ>
  - enabled: Enable SWave

  Valid values: enabled|Enabled|ENABLED|true|True|TRUE
  - disabled: Disable SWave

  Valid values: disabled|Disabled|DISABLED|false|False|FALSE
  - gls: Enable SWave in GLS mode

  Valid values: gls|Gls|GLS
  - ENABLE_SEQ: Enable Sequential SWave

  Valid values: ENABLE_SEQ|enable_seq|enable_sequential

Constraint(s)

At least one of the options should be used

- `-csa` cannot be used with any of the following options: `-csa_header`
- `-all` cannot be used with any of the following options: `-offline_debug`, `-verdi_db`
- `-rtlname` option must be specified with `-enable_hwtop_ports_access select`
- `-memory_backdoor_instances` cannot include escaped names

Note(s)

- `-offline_debug` also implicitly enables `csa` and `debug -set_dyn_probes_on_dut_ios t` commands.
- `-csa_header` and `-csa` are mutually exclusive.
- `-csa t` or `-csa_header <bool>` options force optimization to be `noopt` (same as using `optimization -no|-noopt|-no_opt`)
- `-csa t` or `-csa_header <bool>` options also implicitly enable `debug -set_dyn_probes_on_dut_ios t`
- `ASN` and `UIP` are mutual exclusive
- ASN(UIP) parameters can be used only when ASN(UIP) notifier is set.

Example(s)

```
debug -notifier UIP -notifier_params {UIP_SIGNAL_FILE=./signal.txt,
UIP_OPT=CAPACITY, UIP_CEL_FILE=cel.txt, UIP_MSG_CNL=1,
UIP_PRESERVE_BITS=128}

debug -notifier ASN -notifier_params {ASN_MODE=PIPELINE,
ASN_POST_COMPILATION_CEL=cel.txt, ASN_MAX_FANINS=500}
```

8.3 probe_config

Description

Configure static probes

```
probe_config [-action <create|delete>] [-bank <string>] [-clock
<string>] [-clock_path <string>] [-edge <pos|neg|both>] [-type
<sram_trace>]
```

Option(s)

- `-action <create|delete>`: Create
- `-bank <string>`: Specify bank name
- `-clock <string>`: Specify sampling clock name
- `-clock_path <string>`: Specify user defined sampling clock signal path for converged mode only name
- `-edge <pos|neg|both>`: Specify sampling edge.
- `-type <sram_trace>`: Specify probe type.

Constraint(s)

At least one of the options should be used

Note(s)

- `-action, -bank, -edge` options are not supported in converged mode. Converged mode specific options: `-clock composite_clk | driver_clk | user_defined`: Specify clock in converged mode only.
- `-clock_path signal_name`: Specify user defined sampling clock signal path for converged mode only. For `user_defined clock`, the `-clock_path` option should be specified.

- Probe configuration is only required for "`probe_signals -type sram_trace`" support.

8.4 probe_signals

Description

Adds debug visibility to signals

```
probe_signals [-bank <string>] [-clock_name <string>] [-depth <int>]
[-exclude <string>] [-filter_out <string>] [-fnmatch] [-group
<string>] [-hier_sep <string>] [-init_value <string>] [-instance
<string>] [-instance_file <file>] [-label <string>] [-module
<string>] [-module_file <file>] [-object_not_found <string>] [-port
<list>] [-port_file <file>] [-regexp <string>] [-rtlname <list>] [-
rtlname_file <file>] [-select <string>] [-size_gtr_than <int>] [-
size_lwr_than <int>] [-type
<dynamic|static|sram_trace|read_port|write_port>] [-wire <list>] [-
wire_file <file>]
```

Option(s)

- `-bank <string>`: Specify bank number used for static probes with 'sram_trace' type.. bank number used for static probes with 'sram_trace' type.
- `-clock_name <string>`: Specify sampling clock. sampling clock.
- `-depth <int>`: Specify depth of search for given context determined by `module/instance`. integer number.
- `-exclude <string>`: Specify filter objects to be probed based on some `regex/fnmatch` criteria. filter objects to be probed based on some `regex/fnmatch` criteria.
- `-filter_out <string>`: Specify filter criteria for signals to be probed. `_input|is_output|is_inout|is_port|is_instance|is_sync|is_blackbox`
- `-fnmatch`: Specify that fnmatch pattern is used to match names.
- `-group <string>`: Specify group for probes. group for probes.
- `-hier_sep <string>`: Specify hierarchical separator.

- `-init_value <string>`: Specify initial value for `write_port` probes. initial value for `write_port` probes.
- `-instance <string>`: Specify name of instance to be probed. name of instance to be probed
- `-instance_file <file>`: Specify name of file with instance to be probed.
- `-label <string>`: Specify label for `read_port|write_port` probes. label for `read_port|write_port` probes.
- `-module <string>`: Specify name of module to be probed. name of module to be probed
- `-module_file <file>`: Specify name of file with module to be probed.
- `-object_not_found <string>`: Specify level of severity message in case object is not found. |fatal
- `-port <list>`: Specify list of ports to be probed.
- `-port_file <file>`: Specify name of file with ports to be probed.
- `-regexp <string>`: Specify `regex` pattern used to match names. `_pattern`
- `-rtlname <list>`: Specify list with signals to be probed.
- `-rtlname_file <file>`: Specify name of file with signals to be probed.
- `-select <string>`: Specify filter criteria for signals to be probed. `_input|is_output|is_inout|is_port|is_instance|is_sync|is_blackbox`
- `-size_gtr_than <int>`: Selects modules or instances whose size is greater or equal than number given in argument.. integer number.
- `-size_lwr_than <int>`: Selects modules or instances whose size is less or equal than number given in argument.. integer number.
- `-type <dynamic|static|sram_trace|read_port|write_port>`: Specify probe type.
- `-wire <list>`: Specify list of wires to be probed.
- `-wire_file <file>`: Specify name of file with wires to be probed.

Constraint(s)

At least one of the options should be used

8.5 set_sram_trace

Detailed Description

`set_sram_trace options`

- `-clock driverClk|compositeClk|<clock rtlname>`: Specify the clock type.

Note

The command should be used only in ZeBu Companion flow, otherwise ignored.

8.6 set_trigger

Description

Specify a static trigger based on signal full path string

```
set_trigger -hdl_path <string> -name <string>
```

Option(s)

- `-hdl_path <string>`: Specify the hierarchical path for the static trigger signal. path Mandatory option
- `-name <string>`: Specify the static trigger name. name Mandatory option

Example(s)

```
set_trigger -name my_trig -hdl_path {hw_top.trig_sig}
```

9 Design

This section describes the following UTF commands:

- *blackbox*
- *design*
- *force*
- *load_edif*
- *read_sdc*
- *reg_init*
- *set_sw_control_signal*
- *tristate*
- *wire_resolution*
- *zforce*
- *zgate*
- *zinject*

9.1 blackbox

Detailed Description

```
blackbox <ALGO> <MODULE> [-fnmatch] [-new_module <string>]
              [-object_not_found [fatal|warning]] [-out [log|report]]
[-port <list>]
               [-reg_init [0|1]] [-select [is_terminal]]
[-value [0|1|NONE|REG|Z]] [-verbose]
```

Description

Specifies the behavior of blackboxes in the design.

Mandatory Arguments

- `<ALGO>`: Specifies the processing to apply on a black box module. about allowed values
- `define`: Specifies a module as a known blackbox.
- `disconnect`: Disconnects the ports of the blackbox. You might use a per-port command with the '`-port` ' option. In case the '`-value` ' option is specified, outputs or inouts are driven by the given value. Otherwise, the wire is left as dangling.
- `drive`: Specifies a value that drives the outputs/inouts of the blackbox. You might assign different values to different ports with the '`-port` ' option.
- `ignore`: Discards a module from future processing specified by the following commands.
- `remove`: [Will be DEPRECATED] Deletes all instantiations of the blackbox module given in an argument. Please use 'blackbox drive bbox -value none ' instead 'blackbox remove ' command.
- `replace`: Replaces all instantiations of a blackbox module with those of another module specified with the '`-new_module`' option. The original module and its replacement module should have the same interface. On the next release `-algo <ALGO>` might replace `<ALGO>`.

- <MODULE>: Blackbox module name. To search a blackbox module into a specific EDIF library, use the following syntax:

  <edif_library_name>@<blackbox_module_name>

  Both edif_library_name and blackbox_module_name can contain wild cards.

  Type: <MODULE> is a string.

  On the next release -module <MODULE> might replace <MODULE>.

Optional Arguments

- -fnmatch: Indicates that object pathnames can contains wild cards. This option applies to both module name and port names.
- -new_module <string>: Specifies one module to replace blackbox. Wild cards are not allowed for this option. The module name can be specified with the following format 'Library'.

  Example: replace -new_module=<name>
- -object_not_found [fatal|warning]: Specifies the error policy when objects cannot be found.
  - fatal: Default value. A fatal error is displayed.
  - warning: A warning is displayed instead of an error. value: fatal.
- -out [log|report]: Specifies the log output (logfile / file / report). Available values are 'log' or 'report'.
- -port <list>: Specifies a list of ports or port vectors upon which to apply the command. If not specified, the command is applied to all output and inouts ports. The fnmatch option can be also used to match port names.
- -reg_init [0|1]: Specifies the register initial value [0|1]. value is O (only needed when -value REG).

  Example: drive -value REG -reg_init 1

  Values are '0' or '1'.
- -select [is_terminal]: Selects the objects to be processed according to some criteria (valid value is 'is_terminal'). value:
- is_terminal: Selects the module having all its instantiation ports unconnected.

- `-value <VALUE>`: Specifies the driver value `[0|1|NONE|REG|Z]`. This option is meaningful only for drive, disconnect or remove commands.

  Example: `drive -value 1`.

  Values:

  - `0`: A constant 0 is inserted as a driver.
  - `1`: A constant 1 is inserted as a driver.
  - `NONE`: No driver is inserted. This is mostly useful for the 'blackbox drive' command.
  - `REG`: A register writable at runtime is inserted as a driver.
  - `Z`: A disabled tristate signal is inserted as a driver. This signal can be controlled at runtime (enable and value are writable).
- `-verbose`: Verbosity level.

Examples

Example 1:

```
- blackbox disconnect BB18 -port {PV_OUT[0:12]} -value Z
```

Disconnects a subset of an array of ports in blackbox module BB18 and drives them with a disabled high impedance signal.

Example 2:

```
- blackbox disconnect bbox -port io -value Z -reg_init 1
```

Disconnects the 'io' port of all instantiations of the blackbox module and drives the wires with high-impedance signal. This signal can be controlled from `zSelectProbes` in the blackbox hierarchy.

```
<top>.<pathtobackbox>.io.zBB_enable and
<top>.<pathtobackbox>.io.zBB_value
```

Example 3:

```
- blackbox drive bbox -value REG -reg_init 1
```

Drives all the outputs and inouts of the blackbox module with registers initializied to 1. Their names can be found in the `zSelectProbes` hierarchy of the blackbox.

Example 4:

```
- blackbox drive work@BB30 -port {P*\[1[0-9]\]} -value REG -reg_init
1 -fnmatch
```

Drives ports matching wild cards in blackbox module BB30 from the EDIF library 'work' with a register value. Register initial value is 1.

9.2 design

Description

Design options

```
design [-convert_strength <bool>] [-convert_strength_only <bool>] [-
convert_switches <bool>] [-drive_strength_support <bool>] [-netlist
<bool>] [-netlist_mapping <FPGA>] [-report <list>]
```

Option(s)

- `-convert_strength <bool>`: Enable conversion of strength, MOS/RMOS gates and TRANIF gates.
- `-convert_strength_only <bool>`: Enable conversion of strength.
- `-convert_switches <bool>`: Enable conversion of MOS/RMOS gates and TRANIF gates.
- `-drive_strength_support <bool>`: Resolve undriven/multidriver/tristate signals using drive strength semantics. Default: `true`.
- `-netlist <bool>`: Enable netlist specific changes.
- `-netlist_mapping <FPGA>`: Specifies netlist mapping option.
- `-report <list>`: Generate the requested reports. Supported reports: `xmr` and `force`.

Constraint(s)

- `-netlist` can only be used with `-netlist_mapping` and viceversa.

At least one of the options should be used

Note(s)

`-drive_strength_support` is deprecated

9.3 force

Description

Force wires and ports

```
force <mode> [-assign_as_edit <bool>] [-disconnect] [-fnmatch] [-
globalVerbose <bool>] [-hier_sep <string>] [-local_driver_check] [-
module <string>] [-net <string>] [-no_power] [-object_not_found
<fatal|warning>] [-only_if <list>] [-out <string>] [-pin <string>] [-
pin_input <string>] [-pin_output <string>] [-reg_init <string>] [-
rtlname <string>] [-rtlname_input <string>] [-rtlname_output
<string>] [-source_dve <string>] [-source_net <string>] [-source_pin
<string>] [-source_rtlname <string>] [-value <string>] [-verbose]
```

Option(s)

- `mode <assign|config|default|undriven>`: Force command modes. value Mandatory option
- `assign`: 'assign' mode forces the value of a pin or a net to be equal to some other pin, net or constant. In this mode the older driver(s) of the net get disconnected but for tristate buses

  Valid values: `assign|Assign|ASSIGN`
- `config`: '`config`' mode is used to process all commands together or one by one

  Valid values: `config|Config|CONFIG`
- `default`: '`default`' mode is used to allow change of the global verbosity level

  Valid values: `default|Default|DEFAULT`
- `undriven`: '`undriven`' mode is used to set the value of undriven nets

  Valid values: `undriven|Undriven|UNDRIVEN`
- `-assign_as_edit <bool>`: If value is '`yes`', process commands one by one. if the value is '`no`', process all commands together.
- `-disconnect`: Disconnect ALL drivers of the source (net or pin) before force processing. This option is not activated by default. By default, automatic

disconnection is performed except when both source and target objects are tristate or when source object is not driven.

- `-fnmatch`: Matches hierarchical names using `fnmatch` patterns.
- `-globalVerbose <bool>`: Report disconnected/connected DRIVERS for ALL 'force commands'.
- `-hier_sep <string>`: Specifies hierarchy separator used in hierarchical names.
- `-local_driver_check`: Only local connection of target wires are explored to perform necessary disconnection.
- `-module <string>`: Module name for module relative force assign. Supported switches for this mode are:
  - `-rtlname/-rtlname_input/rtlname_output/-pin/-pin_input/-pin_output/-net` for target signals,
  - `-source_rtlname/-source_pin/-source_net` for source signals,
  - `-value [0/1/REG]`, `-reg_init` and `-disconnect`.

  No hierarchical names are allowed for target/source signals, and `-fnmatch` is only allowed in `-value`. `-fnmatch` would result in a fatal error if used with target/source signals. In case of module name conflict between several libraries, the library name can be pre-pended (`library name name`).
- `-net <string>`: Path of net to force.
- `-no_power`: Propagate constant throughout power domains.
- `-object_not_found <fatal|warning>`: Specify error policy in case of objects cannot be forced. value
  - `fatal`: In case object cannot be found, a fatal error is emitted. This is the default

  Valid values: `fatal|Fatal|FATAL`
  - `warning`: In case object cannot be found, a warning is emitted instead of an error

  Valid values: `warning|Warning|WARNING`
- `-only_if <list>`: Specifies driver types to remove when the '`value`' option is set to `REG`.

- `-out <string>`: Choose log output {`logfile` / `file` / `report`}.
- `-pin <string>`: Specifies a path of instance port. The hierarchical net connected to the port is forced.
- `-pin_input <string>`: Specifies a path of instance port. The signal previously connected to the pin is disconnected, then the pin is forced. The signal down the hierarchy of pin is forced.
- `-pin_output <string>`: Specifies a path of instance port. The signal up the hierarchy of the pin is forced.
- `-reg_init <string>`: Initialization of `REG [0|1]`. This option is used only when option value equals REG.
- `-rtlname <string>`: Specifies a RTL path of instance port. The hierarchical net connected to the port is forced.
- `-rtlname_input <string>`: Specifies a RTL path of instance port. The signal previously connected to the pin is disconnected, then the pin is forced. The signal down the hierarchy of pin is forced.
- `-rtlname_output <string>`: Specifies a RTL path of instance port. The signal up the hierarchy of the pin is forced.
- `-source_dve <string>`: DVE signal name used as source in force assign.
- `-source_net <string>`: Path of net used as source in force assign.
- `-source_pin <string>`: Path of instance port used as source in force assign.
- `-source_rtlname <string>`: RTL Path of instance port or net used as source in force assign.
- `-value <string>`: Value of force nets/pins[`0|1|REG`].
- `-verbose`: Report disconnected/connected DRIVERS for ONLY THIS 'force command'.

Constraint(s)

At least one of the options should be used

Example(s)

- Assigning the value of dut.a.b.wirename to `dut.c.d.wirename` (original drivers of dut.c.d.wirename are always disconnected) force assign `-source_net dut.a.b -net dut.c.d -disconnect`
- Assigning binary value 1 to all 16 bits (equivalent to {16'b1111111111111111}) of `dut.instance.in` port vector `force assign -pin {dut.instance.in[15:0]} -value 1`
- Assigning decimal value 8 (equivalent to {16'b0000000000001000}) to `dut.instance.in` port vector `force assign -pin {dut.instance.in[15:0]} -value 8`
- Assigning 16 bits binary value FACE, to `dut.instance.in` port vector, with runtime programmable registers, initialized with corresponding bitfield `force assign -pin {dut.instance.in[15:0]} -value REG -reg_init {16'b1111101011001110}`
- Assigning 32 bits hexadecimal value BABEFACE, to `dut.instance.in` port vector `force assign -pin {dut.instance.in[31:0]} -value {32'hBABEFACE}`
- Assigning binary value 1 to the least significant bit of dut.instance.in port vector and all other bits are forced to 0 `force assign -pin {dut.instance.in[31:16]} -value 'b1` force default `force default -globalVerbose yes`
- Find undriven nets and ports in the design and force them with a runtime programmable register. The number of forced objects (result returned by the command) is written on standard output puts "`undriven count : [force undriven -value REG -reg_init 1]`"
- Module relative force assign:
  - **Multidimenional indexing**: `force assign -module mod -rtlname y -source_rtlname x[0][0] -disconnect`
  - **Wild card matching**: `force assign -module mod* -rtlname sig* -value 1'b1 -fnmatch`
  - **Vector assignment**: `force assign -module mod -rtlname sig_vec -value REG -reg_init 8'b1110_0001`

- **Inside generate block**: `force assign -module mod -net genblk[0].sig -source_pin in`
- `List of target signals with -net/-pin: force assign -module mod -net {x y z} -source_net w`

  NOTE: *-rtlname and the source side cannot accept a list of signals. Both trigger an error.*
- **Part selection**: `force assign -module mod -rtlname x[1:0] -source_net y[1:0]`

  NOTE: *There should be only one part select per signal (example,* `x[1:0][1:0]` *is not allowed), and the part select should be at the end of the signal name (example,* `x[1:0].y` *is not allowed).*

9.4 load_edif

Description

Relates an EDIF file to a module or VHDL unit

```
load_edif [-filename <file>] [-module <string>]
```

Option(s)

- `-filename <file>`: Specify EDIF file.
- `-module <string>`: Specify module or entity name. or entity name

Constraint(s)

At least one of the options should be used

Example(s)

```
load_edif -module my_entity -filename my_mod.edf
```

9.5 read_sdc

Description

SDC reader

```
read_sdc <fileWithoutArgument> [-designFeatures <file>] [-file
<file>] [-instance <string>] [-resilient <bool>]
```

Option(s)

- `fileWithoutArgument <file>`: Specify name of the SDC file.
- `-designFeatures <file>`: `-designFeatures <file>`.
- `-file <file>`: Specify name of the SDC file.
- `-instance <string>`: Specify instance name for which the SDC file is provided. Valid values: Specify instance name for which the SDC file is provided.
- `-resilient <bool>`: Enable SDC handling with resilient flow. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)

Constraint(s)

- At least one of the options should be used
- `fileWithoutArgument` cannot be used with any of the following options: `-file`
- `-designFeatures` cannot be used with any of the following options:
  - `fileWithoutArgument`
  - `-file`
- At least one of the following options should be used:
  - `fileWithoutArgument`
  - `-file`
  - `-designFeatures`

9.6 reg_init

Description

Initializes registers and latches. This command overrides pre-existing initialization values.

```
 reg_init [-default_value <0|1>] [-enable_wls <bool>] [-
exclude_modules <list>] [-filter_context <ALL|DUT>] [-fnmatch] [-
inst_path <string>] [-value <0|1>]
```

Option(s)

- `-default_value <0|1>`: Specifies the initialization value of uninitialized registers and latches. Available values are '0' or '1'. **Default value:** 0.
- `-enable_wls <bool>`: When true, enables synthesis support for '`reg_init -default_value`'. Default is `false`. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-exclude_modules <list>`: Specifies modules to be excluded from consideration. Currently, only for '`-default_value <0|1> -enable_wls true`'.
- `-filter_context <ALL|DUT>`: Specifies whether to consider just the `DUT`, or `ALL`. Currently, only for '`-default_value <0|1> -enable_wls true`'. Default is `DUT`.
- -fnmatch: Indicates that -inst_path and -exclude_modules can contain wildcards. Type: switch.
- -inst_path <string>: Specifies the path of the register or latch you would like to initialize. Will override previous initialization values. Valid values: string
- -value <0|1> Specifies the initialization value of the register or latch given by -inst_path. Available values are '0' or '1'. Default value: 0.

Constraint(s)

- `-inst_path` can only be used with `-value`

At least one of the options should be used

- `-enable_wls true` cannot be used with `-inst_path` or `-value`.
- `-exclude_modules` and `-filter_context` can only be used when `enable_wls true` is used.

Example(s)

```
reg_init -inst_path top.ins1.ins2.reg* -value 1 -fnmatch
```

All registers and latches named `reg1*` of `'ins2'` will be initialized at 1.

```
reg_init -inst_path top.ins1.ins2.reg1 -value 0
```

The register or latch named `'reg1'` of `'ins2'` will be initialized at 0.

9.7 set_sw_control_signal

Description

Specify a signal as software-accessible. Equivalent to creating a DVE register.

```
set_sw_control_signal -hdl_path <string> [-name <string>] [-sync
<bool>]
```

Option(s)

- `-hdl_path <string>`: Specify the hierarchical path for the software control signal. path Mandatory option
- `-name <string>`: Specify the name of software control signal name. name
- `-sync <bool>`: Specify whether the software control signal is synchronized with system clock.

Constraint(s)

At least one of the options should be used

Note(s)

The `-sync` option is supported only in `nodve` mode.

Example(s)

```
set_sw_control_signal -name my_reg -hdl_path hw_top.ctrl_reg -sync
true
```

9.8 transparent_latch

Description

Specify transparent latches

```
transparent_latch [-fnmatch] [-module <string>] [-object_not_found
<fatal|warning>] [-rtlname <string>] [-signal <string>]
```

Option(s)

- `-fnmatch`: Matches hierarchical names using `fnmatch` patterns.
- `-module <string>`: Module name for transparent latch.
- `-object_not_found <fatal|warning>`: Specify error policy in case of objects cannot be forced. value
  - `fatal`: In case object cannot be found, a fatal error is emitted. This is the default

    Valid values: `fatal|Fatal|FATAL`
  - `warning`: In case object cannot be found, a warning is emitted instead of an error

    Valid values: `warning|Warning|WARNING`
- `-rtlname <string>`: Specifies a the hierarchical signal name of transparent latch.
- `-signal <string>`: Path of module port used.

Constraint(s)

At least one of the options should be used

9.9 tristate

Description

Specifies the processing on tristate buses.

```
tristate <buses> [-conflict <wand|wor>] [-dynamic] [-exclude
<string>] [-fnmatch] [-keeper] [-pulldown] [-pullup] [-rtlname]
```

Option(s)

- `buses <list>`: List of hierarchical paths to tristate buses. These paths might contain '*' to match several buses if you use the `-fnmatch` option. Mandatory option
- `-conflict <wand|wor>`: Specifies the behavior of the bus if several tristate drivers are simultaneously enabled. If this option is not specified, the most appropriate conflict resolution for each bus is used.

  Details about allowed values:

  - `wand`: In case of multiple drivers, the option specifies that the resolution function is AND.
  - `wor`: In case of multiple drivers, the option specifies that the resolution function is OR.
- `-dynamic` .
- `-exclude <string>`: Excludes buses whose names match the string defined in argument. This string can contain wild cards when the `fnmatch` option is used value.
- `-fnmatch`: Indicates that bus names can contain wild cards.
- `-keeper`: Specifies if the bus must be implemented as a keeper.
- `warning`: A warning is displayed instead of an error

  Valid values: `warning|WARNING|Warning`
- `fatal`: A fatal error is displayed

  Valid values: `fatal|FATAL|Fatal`

- `-pulldown`: Specifies if the bus must be implemented as a pulldown.
- `-pullup`: Specifies if the bus must be implemented as a pullup.
- `-rtlname`: Specifies whether the given list of hierarchical paths to tristate buses must be considered as signal paths.

Constraint(s)

At least one of the options should be used

Example(s)

Example 1

`tristate -pulldown {top.ins0.busz top.ins*.busz*} -exclude busz1 -fnmatch`: Specifies tristate bus resolution as pulldown for buses whose hierarchical names are matching '`top.ins0.busz top.ins*.busz*`' wild card but whose names are not '`busz1`'.

Example 2

`tristate -pullup {top.ins0.busz top.ins1.busz} -conflict wor`: Specifies tristate bus resolution as pullup for buses `top.ins0.busz andtop.ins1.busz`. If several drivers of this bus are enabled altogether, the resolution function is OR for these signals.

9.10 wire_resolution

Description

- Specifies multidriver resolution (WAND/WOR) for list of signals.
- Defines default multidriver resolution for nets on which no specific resolution has been defined, default tristate bus resolution, default undriven nets behavior.

```
wire_resolution [-conflict <wand|wor>] [-default_conflict <wand|wor>]
[-default_tristate <pullup|pulldown|keeper>] [-default_undriven
<0|1>] [-default_xmr_conflict <wand|wor|xmr>] [-exclude <string>] [-
fnmatch <bool>] [-tristate <pullup|pulldown|keeper>] [-wires <list>]
```

Option(s)

- `-conflict <wand|wor>`: Specifies the default behavior of the bus in case several drivers are simultaneously enabled.
- `-default_conflict <wand|wor>`: It is applied on all wires which do not have specific `-conflict` configuration.
- `-default_tristate <pullup|pulldown|keeper>`: Defines default resolution function when no tristate driver is active on the bus.
- `-default_undriven <0|1>`: Sets the default value for undriven nets.
- `-default_xmr_conflict <wand|wor|xmr>`: Only supported by the UCPC product. It is applied on all XMRs. The XMR value means that the XMR wins.
- `-exclude <string>`: Exclude wires whose names are matching pattern string given in argument value.
- `-fnmatch <bool>`: Indicates that bus names can contain wild cards.
- `-tristate <pullup|pulldown|keeper>`: Specifies the default tristate behavior of the bus in case no drivers are enabled.
- `-wires <list>`: Specifies the wires to be resolved.

Constraint(s)

At least one of the options should be used

- `-default_conflict` cannot be used with any of the following options:
  - `-conflict`
  - `-wires`
  - `-fnmatch`
  - `-exclude`
- `-default_xmr_conflict` cannot be used with any of the following options:
  - `-conflict`
  - `-wires`
  - `-fnmatch`
  - `-exclude`
- `-default_undriven` cannot be used with any of the following options:
  - `-conflict`
  - `-wires`
  - `-fnmatch`
  - `-exclude`
- `-default_tristate` cannot be used with any of the following options:
  - `-conflict`
  - `-wires`
  - `-fnmatch`
  - `-exclude`
- `-conflict` cannot be used with any of the following options:
  - `-default_conflict`
  - `-default_undriven`
  - `-default_tristate`

- `-wires` cannot be used with any of the following options:
  - `-default_conflict`
  - `-default_undriven`
  - `-default_tristate`
- `-fnmatch` cannot be used with any of the following options:
  - `-default_conflict`
  - `-default_undriven`
  - `-default_tristate`
- `-exclude` cannot be used with any of the following options:
  - `-default_conflict`
  - `-default_undriven`
  - `-default_tristate`
- `-conflict` can only be used with `-wires`
- `-fnmatch` can only be used with `-wires`
- `-exclude` can only be used with `-wires`

Usage

- `wire_resolution -conflict <WAND|WOR> -wires <list> [-fnmatch <bool>] [-exclude <pattern>]`
- `wire_resolution [-default_conflict WOR|WAND] [-default_undriven 0|1] [-default_tristate PULLUP|PULLDOWN|KEEPER]`

Note (s)

Mix of two usages are not allowed.

9.11 zforce

Description

Forces and maintains a signal to a given value at runtime until its release. After its release, the original design value is passed.

```
 zforce [-detect_val_change] [-enable_wls <bool>] [-fnmatch] [-mode
<dynamic|static>] [-module <string>] [-object_not_found
<warning|fatal>] [-pin <list>] [-pin_file <file>] [-pin_only] [-
rtlname <list>] [-rtlname_file <file>] [-signal <list>] [-sync
<bool>] [-sync_enable] [-type <global|downstream>] [-uniquify] [-wire
<list>] [-wire_file <file>]
```

Option(s)

- `-detect_val_change`: Detects any value change on the forced net.
- `-enable_wls <bool>`: Enable synthesis support for `zforce`.
- `-fnmatch`: Indicates that object pathnames can contain wild cards.
- `-mode <dynamic|static>`: `zforce` command modes.
  - `dynamic`: 'DYNAMIC' mode is recommended for system resource preservation over performance. Default mode for force.

    Valid values: `dynamic|DYNAMIC|Dynamic`
  - `static`: 'STATIC' mode is recommended for signals that are forced hundreds of times or more during an emulation via dedicated top ports.

    Valid values: `static|STATIC|Static`
- `-module <string>`: Specifies the name of the module under which the signals specified by the `-signal` option are forced.
- `-object_not_found <warning|fatal>`: Specifies the error policy when objects cannot be found.
  - `warning`: A warning is displayed instead of an error.

    Valid values: `warning|WARNING|Warning`

- ❒ `fatal`: A fatal error is displayed.

  Valid values: `fatal|FATAL|Fatal`

- `-pin <list>`: Specifies a list of instance ports. The hierarchical net connected to the port is forced.
- `-pin_file <file>`: Specifies whether the command is applied on pin objects found in a file defined in argument. File path is relative to the **zCui** execution directory..
- `-pin_only`: Forces the net connected to the specified instance port only. Don't force any equivalent nets.
- `-rtlname <list>`: Applies the command to a list instance port paths. The hierarchical net connected to the port is forced..
- `-rtlname_file <file>`: Applies the command to RTL objects found in a file defined in argument. File path is relative to **zCui** execution directory.
- `-signal <list>`: Applies the command to a list signals. Signals are relative to module specified with the `-module` option.
- `-sync <bool>`: Prevents force from potential glitches at the cost of a register. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-sync_enable`: Prevents force from potential glitches at the cost of a register.
- `-type <global|downstream>`: Indicates the way the dynamic force need to be inserted.
  - ❒ `global`: 'GLOBAL' Default value. Indicates that the dynamic force applies to all the readers of the hierarchical wire.

    Valid values: `global|GLOBAL|Global`

  - ❒ `downstream`: 'DOWNSTREAM' Indicates that the dynamic force is applied to the readers downstream.The wire is implicitly oriented and the net might not be multi driven or tristate.

    Valid values: `downstream|DOWNSTREAM|Downstream`

- `-wire <list>`: Applies the command to wire objects.
- `-wire_file <file>`: Applies the command to wire objects found in a file defined in argument. File path is relative to zCui execution directory.

Constraint(s)

At least one of the options should be used

9.12 zgate

Detailed Description

```
     zgate <MODULE> [-clock_freq [25Mhz|50Mhz|100Mhz]] [-clock_name
<string>] [-fnmatch]

           [-hier_sep <string>] [-
insertion_mode[downstream|global|parallel|serial]]

           [-instance_name <string>] [-object_not_found
[fatal|warning]] [-reg_init <string>]

           [-module <name> -signal <list>] [-rtlname <list>] [-
rtlname_file <filename>] [-verbose] [-wire <list>]

           [-wire_file <filename>]
```

Description

Adds a gate in the design. The module interface must be as follows: input port or port-vector named 'D' or 'I' input port named 'C' for sequential module output port named 'Q' or 'O'. With port-vectors: Input and output must be of equal size Have to match the number of instrumented elements Must be within the same context input ports as well as inout ports cannot be instrumented. command does not interrupt a Tcl script in case of an error; the number of error(s) is returned instead.

- Mandatory Arguments
  - `<MODULE>`: Specifies the name of the module to be added. In case of conflict between several libraries, the library name can be prepended (library).
- 4*Option Arguments
  - `-clock_freq [25Mhz|50Mhz|100Mhz]`: In case of a macro with a 'C' input port, this option defines the clock frequency of the system clock that is connected to this port.
  - `-clock_name <string>`: In case of a macro with a 'C' input port, this option defines the wire hierarchical name that is connected to this port. If `rtlname/rtlname_file` option is specified, the hierarchical primary clock path must be an RTL path name too. Following special clocks might be specified as well: `driverClk`, `zFilterClk`, `zDelayClk`, `compositeClk`.

- `-fnmatch`: This options applies only to names specified in '`wire/rtlname`' and '`wire_file/rtlname_file`' options. Only wire or signal names are matched as `fnmatch` expressions. This cannot be used when the input and output ports of the `zgate` module are vectors. Type: switch.
- `-hier_sep <string>`: Specifies the hierarchical separator used to parse wire names if specified. value:
- `-insertion_mode [downstream|global|parallel|serial]`: Specifies the way the module is instantiated.

  Details about allowed values:

  - `downstream`: All downstream readers are driven by the `zgate` instance. `zgate` instantiation context depends on port direction when using the `rtlname` option.
  - `global`: The `zgate` output affects the whole hierarchical net on which it is inserted.
  - `parallel`: Connects the wires to the inputs of the `zgate` instance.
  - `serial`: Direction of the wire is computed and the `zgate` inserted accordingly. In case of multidriver or tristate buses or equipotential loop, insertion might be impossible.

- `-instance_name <string>`: Specifies the instance name to be given to the `zgate`. In case of conflict it is used as a prefix of the `zgate` instance name.
- `-object_not_found [fatal|warning]`: Specifies the error policy when objects cannot be found.

  Available policies:

  - `fatal`: Default value. A fatal error is displayed.
  - `warning`: A warning is displayed instead of an error.

- `-reg_init <string>`: Specifies the initial value of the inserted gate. Value for vectors might be expressed using Verilog number syntax (example: `{32'hBABEFACE}`).
- `-rtlname <list>`: Applies the command to a list of hierarchical paths.
- `-rtlname_file <filename>`: Applies the command to hierarchical paths listed in a file defined in argument. File path is relative to **zCui** execution directory.

- `-module <modulename>`: Specifies the name of the module under which the command is applied to signals specified by -signal option.
- `-signal <list>`: Applies the command to a list signals. Signals are relative to module specified with the `-module` option.
- `-verbose`: Verbosity level.
- `-wire <list>`: Applies the command to a list of hierarchical wire patterns.
- `-wire_file <filename>`: Applies the command to hierarchical wire patterns listed in a file defined in argument. File path is relative to **zCui** execution directory.

Usage Examples

- **Example 1:**

```
- zgate buf -wire "top.CK_2_CK
top.OUT_ins_3mult_gnd_bb_in_io_mod_2_OUT"
-insertion_mode parallel
```

  Adds buffer on several wires in parallel mode.

- **Example 2:**

```
- zgate fd -clock_name compositeClk -verbose -rtlname
{top.instance.in[15:0]} -insertion_mode downstream -reg_init
{16'b1111101011001110} -object_not_found warning
```

  Adds runtime programmable registers synchronized on composite clock, and initialized with corresponding 16-bit bitfield, to top.instance.in 16-bit width port vector.

- **Example 3:**

```
- zgate fd -wire "top.CK_2_CK
top.OUT_ins_3mult_gnd_bb_in_io_mod_2_OUT"
-insertion_mode serial -instance_name zgate_
```

  Adds register on several wires in serial mode.

9.13 zinject

Detailed Description

```
   zinject [-fnmatch] [-init_value [0|1]] [-mode [dynamic|static]] [-
object_not_found [fatal|warning]]
           [-pin <list>] [-pin_file <filename>] [-module <name>] [-
signal <list>] [-rtlname <list>] [-rtlname_file <filename>]
          [-type [comb|disconnect_driver]] [-wire <list>] [-wire_file
<filename>]
```

Description

Assigns signal to a given value at runtime. Automatically released with an event on its driver. Sequential signals are injectable by default.

- Optional Arguments
  - `-fnmatch`: Indicates that object pathnames can contain wild cards.
  - `-init_value [0|1]`: Specifies initialization value `[0|1]` of registers that are used to inject undriven wire or injections performed with driver disconnection. Register's initialization value is set to 0 by default.

    Value: 0.
  - `-mode [dynamic|static]: zinject` command modes.

    Details about allowed values:
    - `dynamic`: 'dynamic' mode is recommended for system resource preservation over performance. Default mode for injection.
    - `static`: 'static' mode is recommended for signals that are forced hundreds of times or more during an emulation via dedicated top ports.

    Value: `dynamic`.
- `-object_not_found [fatal|warning]`: Specifies the error policy when objects cannot be found.

  Available policies:
  - `fatal`: Default value. A fatal error is displayed.

  - warning: A warning is displayed instead of an error.
- -pin <list>: Specifies a list of instance ports. The hierarchical net connected to the port is injected.
- -pin_file <filename>: Specifies whether the command is applied on pin objects found in a file defined in argument. File path is relative to the **zCui** execution directory.
- -rtlname <list>: Applies the command to a list instance port paths. The hierarchical net connected to the port is injected.
- -rtlname_file <filename>: Applies the command to RTL objects found in a file defined in argument. File path is relative to **zCui** execution directory.
- -module <modulename>: Specifies the name of the module under which the signals specified by the -signal option are injected.
- -signal <list>: Applies the command to a list signals. Signals are relative to module specified with the -module option.
- -type [comb|disconnect_driver]: Specifies the injection behavior.

  Details about allowed values:

  - comb: case of injection into a wire with a pre-existing combinational driver, logic is added to the netlist and holds the injected value until the next event on the injected wire. Otherwise, injection is ignored with a warning.
  - disconnect_driver: case of injection into a wire driven by flop or latch, wire might be disconnected and driven by a new register, initialized to 0 (except when init_value option is specified). This option allows you to stick a signal with a runtime-programmable value, and guarantees that the injected signal is no longer be influenced by its original driver.
  - -wire <list>: Applies the command to a list of wires.
  - -wire_file <filename>: Applies the command to wire objects found in a file defined in argument. File path is relative to **zCui** execution directory.

Usage Example

- Example 1:

```
- zinject -mode dynamic -rtlname dut.instance.wirename
```

Injects corresponding wire with a runtime programmable register.

- Example 2:

  ```
  - zinject -mode static -rtlname dut.instance.wirename
  ```

  Injects corresponding wire with a created top port (value), which is used as driver of the injection register.

10 ECO

This section describes the following UTF commands:

- *eco*

10.1 eco

Description

Specify `eco` options

```
eco [-advanced_command <string>] [-advanced_command_file <file>][-
change_not_feasible <DEFAULT|FATAL|WARNING>] [-
force_add_equiv_signals <bool>] [-recompile_on_error
<NEVER|ON_OVERWRITE_ONLY>] [-reserve_force <int>] [-
reserve_force_assign <int>] [-reserve_fwc <int>] [-reserve_monitor
<int>] [-reserve_ports] [-reserve_qiwc <int>] [-reserve_scope <list>]
[-reserve_xtor <int>] [-skip_checking <bool>] [-valueset_fwc
<string>] [-valueset_qiwc <string>]
```

Option(s)

- `-advanced_command <string>: Specify any zECO command. Valid values: zECO command.`
- `-advanced_command_file <file>`: Specify advanced command file for zECO.
- `-change_not_feasible <DEFAULT|FATAL|WARNING>`: Set the behavior when signal change cannot be handled in ECO compilation.
- `-force_add_equiv_signals <bool>`: Enable/disable force adding equivalent signals..
- `-recompile_on_error <NEVER|ON_OVERWRITE_ONLY>`: Set the recompile on error mode.
- `-reserve_force <int>`: Reserve force bit number in each chip. non-negative integer number.
- `-reserve_force_assign <int>`: Reserve force assign number for ECO. non-negative integer number.
- `-reserve_fwc <int>`: Reserve `fwc` IP bit number in each chip. non-negative integer number.
- `-reserve_monitor <int>`: Reserve monitors in each chip. non-negative integer number.

- `-reserve_ports`: Reserve all ports for the design.
- `-reserve_qiwc <int>`: Reserve `qiwc` bit number in each chip. non-negative integer number.
- `-reserve_scope <list>`: Specify the list of modules that reserves resources for ECO compilations.
- `-reserve_xtor <int>`: Reserve transactor size for transactor based force assign. non-negative integer number.
- `-skip_checking <bool>`: Enable/disable skip checking.
- `-valueset_fwc <string>`: Specify the `fwc` valueset name for ECO. is `ZECO_PRESERVE_FWC`.
- `-valueset_qiwc <string>`: Specify the `qiwc` valueset name for ECO. is `ZECO_PRESERVE_QIWC`.

11 Environment

This section describes the following UTF commands:

- *grid_cmd*
- *grid_engine*
- *grid_task_association*
- *nfs_settngs*
- *set_app_var*

11.1 grid_cmd

Description

Specify GRID/LSF commands for compilation

```
grid_cmd [-clear_all] [-delete <string>] [-local] [-njobs <int>] [-
queue <string>] [-submit <string>]
```

Option(s)

- `-clear_all`: Clears out all previous `grid_cmd` settings.
- `-delete <string>`: Job deletion string (if not present, kill -9 is used). _deletion_string
- `-local`: Run jobs in this queue locally (mutually exclusive to `-submit` and `-delete` options).
- `-njobs <int>`: Specify the number of parallel jobs. non-negative integer number.
- `-queue <string>`: Specify queue name (if not present this command is referring to all previously defined queues). `_name`
- `-submit <string>`: Job submission string. `job_submission_string`

Constraint(s)

At least one of the options should be used

- `-clear_all` cannot be used with any other option.
- `-local` cannot be used with any of the following options: `-delete`, `-submit`

11.2 grid_engine

Description

Relaunch jobs in case of grid failure

```
grid_engine [-clear <all>] [-name <string>] [-property <string>] [-
value <string>]
```

Option(s)

- `-clear <all>`: Clears out all previous `grid_engine` declarations.
- `-name <string>`: Specify engine name. `_UPON_FAILURE`
- `-property <string>`: Specify property name. `_string`
- `-value <string>`: Specify property value as string. `_string`

Constraint(s)

At least one of the options should be used

- `-clear` cannot be used with any other option
- `-implementation` cannot be used with any other option

At least one of the following options should be used: `-implementation|-name|-property|-clear`

- `-property` can only be used with -value
- `-value` can only be used with -property

Note(s)

Only one property can be declared per command.

Example(s)

```
grid_engine -name RETRY_UPON_FAILURE -property numberOfRetries -value
5
grid_engine -name RETRY_UPON_FAILURE -property retryExpression -value
{error 131}
grid_engine -name RETRY_UPON_FAILURE -property
invertedRetryExpression -value {^a, b or c}
grid_engine -name RETRY_UPON_FAILURE -property delay -value 10
grid_engine -property gridvendor -value "SGE"
grid_engine -clear
```

11.3 grid_task_association

Description

Specify associations of Zebu tasks and GRID/LSF queues

```
grid_task_association [-clear_all] [-queue <string>] [-task <string>]
```

Option(s)

- `-clear_all`: Clears out all previous `grid_task_association` settings.
- `-queue <string>`: Specify queue name (if not present this command is referring to all previously defined queues). `_name`
- `-task <string>`: Specify task name. `_name`

Constraint(s)

`-clear_all` cannot be used with any other option.

At least one of the options should be used

11.4 nfs_settngs

Description

Specify options for NFS file handling

```
nfs_settings [-access_level <0|1|2|3|4|5>] [-delay <int>] [-
max_retries <int>]
```

Option(s)

- `-access_level <0|1|2|3|4|5>`: Specify access level for retries.
- `-delay <int>`: Specify delay interval (ms) for retries. non-negative integer number.
- `-max_retries <int>`: Specify maximum number of NFS retries. non-negative integer number.

Constraint(s)

At least one of the options should be used

11.5 set_app_var

Description

This command is used to add an option to OptionsDB.

```
set_app_var <name> <value> [-lock <hard|soft>]
```

Option(s)

- name <string>: Name of option to be added to OptionsDB.
- value <string>: Value of option to be added to OptionsDB.
- -lock <hard|soft>: Whether recurrence of the option in same UTF file should cause error/warning.
  - hard: Terminate if same option has been defined previously with this flag
  - soft: Warn and ignore if same option has been defined previously with this flag

Constraint(s)

At least one of the following options should be used: name

At least one of the following options should be used: value

12 Functional Safety

This section describes the following UTF commands:

- *fusa*

12.1 fusa

Description

This command indicates the fault emulation database and the campaign name.

```
fusa [-campaign <string>] [-dut_path <string>] [-fdb_name <string>]
[-fdb_server <string>] [-object_not_found <string>]
```

Option(s)

- `-campaign <string>`: Specify the campaign name. the campaign name.
- `-dut_path <string>`: Specify the DUT path. the DUT path.
- `-fdb_name <string>`: Specify the fault emulation database name. the fault emulation database name.
- `-fdb_server <string>`: Specify the fault emulation database server. the fault emulation database server.
- `-object_not_found <string>`: Specify the message severity for not found objects. Default is fatal.. the message severity for not found objects. Default is fatal.

Constraint(s)

At least one of the options should be used

Example(s)

```
fusa -fdb_server <host name>:80 -fdb_name FDB1 -campaign fc_1
```

13 Memories

This section describes the following UTF commands:

- *memories*
- *memory_preferences*

13.1 memories

Description

Memory inference options

```
memories [-algorithm <DIRECT|TWO_PASS>] [-convert_reset <bool>] [-
drop_write_only <bool>] [-exclude <list>] [-flops] [-inline_readmem]
[-instance <list>] [-make_sync_writes
<false|posedge|negedge|dual|driver|COMPOSITE>] [-
make_sync_writes_specific <FALSE|DRIVER|DUAL|COMPOSITE>] [-
set_default_type
<LUT|BRAM|URAM|ZRM|READ_AFTER_WRITE|READ_BEFORE_WRITE|NO_READ_ON_WRIT
E|OPTIMIZE_CAPACITY|OPTIMIZE_PERFORMANCE|WORD_LENGTH>] [-type
<LUT|BRAM|URAM|ZRM|READ_AFTER_WRITE|READ_BEFORE_WRITE|NO_READ_ON_WRIT
E|OPTIMIZE_CAPACITY|OPTIMIZE_PERFORMANCE|WORD_LENGTH|ZMEM_CLOCK_FREQU
ENCY|ZMEM_TARGET_FREQUENCY|REPLICATE|BRAM_DUAL_PORT_MULTIPLEXED|AUTO>
] [-zmem] [-zmem_port_threshold <int>] [-zmem_scripts <list>] [-
zmem_size_threshold <int>] [-zrm_latency_encoding <ONEHOT|BINARY>]
```

Option(s)

- `-algorithm <DIRECT|TWO_PASS>`: Specify algorithm.
- `-convert_reset <bool>`: Convert reset logic, so there are fewer memory ports, increasing the chance that the array can be implemented as a memory Global option. Default is `false` for UC Phase 1, and true for WLS (Word Level Synthesis).
- `-drop_write_only <bool>`: Drop write-only memories. Global option.
- `-exclude <list>`: list of excluded instances.
- `-flops`: Specify memories to be implemented as flops.
- `-inline_readmem`
- `-instance <list>`: Specifies a list of instances.

- `-make_sync_writes <false|posedge|negedge|dual|driver|COMPOSITE>`: Converts asynchronous writes to synchronous writes.
- `-make_sync_writes_specific <FALSE|DRIVER|DUAL|COMPOSITE>`: make sync writes specific.
- `-set_default_type <LUT|BRAM|URAM|ZRM|READ_AFTER_WRITE|READ_BEFORE_WRITE|NO_READ_ON_WRITE|OPTIMIZE_CAPACITY|OPTIMIZE_PERFORMANCE|WORD_LENGTH>`: Specify default type.
- `-type <LUT|BRAM|URAM|ZRM|READ_AFTER_WRITE|READ_BEFORE_WRITE|NO_READ_ON_WRITE|OPTIMIZE_CAPACITY|OPTIMIZE_PERFORMANCE|WORD_LENGTH|ZMEM_CLOCK_FREQUENCY|ZMEM_TARGET_FREQUENCY|REPLICATE|BRAM_DUAL_PORT_MULTIPLEXED|AUTO>`: Specify type.
- `-zmem`: Specify memories to be implemented as `zMem`s.
- `-zmem_port_threshold <int>`: Specify port threshold for flop vs. `zMem` memories for automatic memory inference. positive integer number.
- `-zmem_scripts <list>`: Specify list of `zMem` scripts.
- `-zmem_size_threshold <int>`: Specify size threshold for flop vs. `zMem` memories for automatic memory inference. positive integer number.
- `-zrm_latency_encoding <ONEHOT|BINARY>`: Latency encoding type.

Constraint(s)

- `-exclude` can only be used with `-inline_readmem`
- `-flops` cannot be used with any of the following options: `-zmem`, `-set_default_type`, `-type`, `-make_sync_writes_specific`
- `-flops`: `-inline_readmem` is not compatible with `-algorithm TWO_PASS`
- `-flops`: using `-algorithm` implies also using `-instance`
- `-inline_readmem` can only be used with `-flops`
- `-algorithm` can only be used with `-flops`

- -zmem: if no -instance use -set_default_type; -make_sync_writes_specific cannot be used without -instance; -inline_readmem is illegal; cannot use -make_sync_writes_specific with -type
- REPLICATE is the only -type that can be used without a -zmem
- -type, when used without -zmem, must be used with -instance
- -set_default_type can only be used with -zmem
- -make_sync_writes_specific can only be used with -zmem
- when -type or -set_default_type value is WORD_LENGTH, or -type is ZMEM_CLOCK_FREQUENCY, ZMEM_TARGET_FREQUENCY, REPLICATE, or BRAM_DUAL_PORT_MULTIPLEXED, -instance value shall be an even-length list of pairs {inst1 num1 ...}
- '-make_sync_writes INDRIVER' is obsolete
- '-make_sync_writes INVDRIVER' is obsolete
- '-make_sync_writes_specific DRIVER_NEGEDGE' is obsolete

At least one of the options should be used

Note(s)

- **Usage of -instances option:**
  - full_hierarchical_path.memory_name
  - module_relative_name.memory_name

    The module_relative_name is based on parent module_name and can include the **relative hierarchical path of the memory**, if the memory array is declared inside a subscope or nested subscopes within the module.

    The **relative hierarchical path of the memory** can be any of the following:
    - a label name of one subscope
    - a combination of nested subscopes label names
- **Usage for the -flops option:**
  - -flops -instance #instances [-inline_readmem [-exclude #instances]]|[-algorithm DIRECT|TWO_PASS] using -

inline_readmem. Also implies implement as flops for the specific modules or instances

- memories -flops -algorithm TWO_PASS -instance {module_name.variable_name}
- memories -flops -algorithm DIRECT is same as memories -flops (that is -algorithm DIRECT is the default)

- **Usage for the -zmem option:**

```
-zmem -instance #instances [-type
LUT|BRAM|ZRM|READ_AFTER_WRITE|READ_BEFORE_WRITE|NO_READ_ON_WRITE|O
PTIMIZE_CAPACITY|OPTIMIZE_PERFORMANCE|WORD_LENGTH
|ZMEM_CLOCK_FREQUENCY|ZMEM_TARGET_FREQUENCY|REPLICATE|BRAM_DUAL_PO
RT_MULTIPLEXED|AUTO] Or [-set_default_type
LUT|BRAM|ZRM|READ_AFTER_WRITE|READ_BEFORE_WRITE|NO_READ_ON_WRITE|O
PTIMIZE_CAPACITY|OPTIMIZE_PERFORMANCE|WORD_LENGTH] Or [-
make_sync_writes_specific FALSE|DRIVER|DUAL|COMPOSITE]
```

- when using -zmem in combination with -type WORD_LENGTH or -type REPLICATE, -instance <list>: <list> should have the following format {instance1 <int> instance2 <int> ...} where <int> is the word length or replication factor per instance.
- when using -zmem in combination with -type ZMEM_CLOCK_FREQUENCY, -instance <list>: <list> should have the following format {instance1 <int> instance2 <int> ...} where <int> is 25, 50, 100, or200.
- when using -zmem in combination with -type ZMEM_TARGET_FREQUENCY, -instance <list>: <list> should have the following format {instance1 <int> instance2 <int> ...} where <int> is target frequency for zMEM in kHz [1-200000]
- when using -zmem in combination with -type BRAM_DUAL_PORT_MULTIPLEXED, -instance <list>: <list> should have the following format {instance1 <int> instance2 <int> ...} where <int> is 0 for false, or 1 for true.
- Using -zmem in combination with -make_sync_writes_specific (zfast: +MakeSyncWrites:<...>) also implies implement as memory for the specific instances

- `-type` must be used with `-zmem`, except for '`-type REPLICATE`', which might be used either with or without `-zmem`, and, like all other `-type` values, might not be used with `-flops`.
- When `-type` is used without `-zmem`, it must be used with `-instance`. Due to `no -zmem`, the arrays specified by `-instance` are not required to be implemented as `zMem`s. `-type` only applies to those arrays which are implemented as `zMem`s (if any), and has no effect on those arrays which are implemented as flops.
- Using `-inline_readmem`. Also implies implement as flops for the specific instances

13.2 memory_preferences

Detailed Description

- [-max_bram_blocks <integer>|DEFAULT]: Specify maximum numbers of BRAM blocks or restore to default the previously set value.
- [-max_uram_blocks <integer>|DEFAULT]: Specify maximum numbers of URAM blocks or restore to default the previously set value.
- [-max_ramlut_blocks|-max_lutram_blocks <integer>|DEFAULT]: Specify maximum numbers of RAMLUT blocks or restore to default the previously set value.
- [-ramlut_to_bram_threshold|-lutram_to_bram_threshold <integer>|DEFAULT]: Specify ratio (percentage) of RAMLUTs to BRAMs or restore to default the previously set value.
- [-bram_to_uram_threshold <integer>|DEFAULT]: Specify ratio (percentage) of BRAMs to URAMs or restore to default the previously set value.
- [-scan_path <list>]
- [-advanced_command_file #filename]: Command file for zMem
- [-advanced_command] <zMem_command>: Specify advanced command for zMem
- [-zmem_clock_frequency 25|50|100|200|AUTO]: The valid values are 25, 50, 100, 200(in MHz) or AUTO. AUTO stands for current default.
- [-manage_dual_port_bram_access <bool>]: Enable/disable simple port ramlut multiplexing.

14 Optimization

This section describes the following UTF commands:

- *optimization*
- *performance*

14.1 optimization

Detailed Description

- `-aggressive|-maxopt|-max_opt [-module <module list>][-instance <instance list>]`: Aggressive optimization if `-module` or `-instance` are present the optimization directive is per the instance/module list (`regex` patterns can be used. for example: all modules which begin with 'a' `-module {a.*}` if `-module` or `-instance` are not present this is a global directive.
- `-normal|-keep_registers [-module <module list>][-instance <instance list>]`: Medium optimization if `-module` or `-instance` are present the optimization directive is per the instance/module list if `-module` or `-instance` are not present this is a global directive (`regex` patterns can be used. for example: all modules which begin with 'a' `-module {a.*}`)
- `-no|-noopt|-no_opt`: No optimization if `-module` or `-instance` are present the optimization directive is per the instance/module list if `-module` or `-instance` are not present this is a global directive (`regex` patterns can be used. for example: all modules which begin with 'a' `-module {a.*}`)
- `-pass_opt_levels <bool>`: Specify whether WLS (Word Level Synthesis) should use the optimization levels specified by `-aggressive`, `-normal`, `-no_opt`, and so on. Default is `true`.
- `-dsp_mult_threshold <int>`: Synthesize DSP for mults when total bits of `args` are greater than `nb`.
- `-dsp_limit <int>`: Limit the maximum number of DSPs in any module. Acceptable values are >= 0. When set to 0, this gives the default, which is no limit. Note that this is not exactly a limit for the modules. Rather, this is the maximum number of DSPs in any module, but after all of the inlining has happened into the modules. If you have used "`optimization -top_down_roots <module_list>`", it is a bit different. Call each module in the `<module_list>` a root module. Each root module is synthesized together with a sub-hierarchy below it. The DSP limit, in this case, is

the limit on the number of DSPs in each root module together with that root module's own sub-hierarchy.

- `-remove_unconnected_blackboxes <bool>`: Specify removal of unconnected blackboxes
- `-latch_clocks <bool>`: Enable clock analysis on `mem` instances and latches.
- `-boundary_opt <bool>`: Deprecated. Boundary optimization: performs ports merging for ports with same/opposite phase and cross-modules constant propagation. WLS flow option. Currently default `false`. Cannot be combined with the newer `-qor_opt_enable` or `-qor_opt_disable` options.
- `-number_of_threads <int>`: Specify number of threads for WLS (Word Level Synthesis). Default is `16`.
- `-qor_opt_enable <list of sub-options>`: The sub-options are `INLINE`, `BOUNDARY`, `THREADED_GLOBAL`, and `ALL`. These enable the specified WLS (Word Level Synthesis) global optimizations. Default is currently for the global optimizations to be `off`.
- `-qor_opt_disable <list of sub-options>`: The sub-options are `INLINE`, `BOUNDARY`, `THREADED_GLOBAL`, and `ALL`. These disable the specified WLS (Word Level Synthesis) global optimizations. Default is currently for the global optimizations to be `off`.
- `-inline <module_list>`: Performs module inlining for a list of modules (this can get also pattern: * matches everything, ? matches any single character, [seq] matches any character in seq, [!seq] matches any character not in seq>]
- `-auto_inline_limit <limit>`: auto inline all modules with `cost <= limit`
- `-auto_inline_port_size_threshold <Threshold>`: auto inline all modules with total port size >= Threshold
- `-auto_inline_cost_refine <bool>`: auto inling optimization in calculating inlining cost.
- `-auto_inline_params <seq_modules>=<bool>`: Enable/disable auto inling parameters. seq_modules enables inlining of sequential blocks. Default value is `false`.

  NOTE: *Avoid counting simple assignments (buffers) towards inlining cost.*

- `-cell_size <int> -instance|-module <list>`: Specifies the maximum cell size that PLAyer creates.
- `-lut_costs <list> [-module <module list>][-instance <instance list>]`: Specifies the relative costs of the different sized LUTs. This is a list of non-negative LUT costs giving the relative costs for LUT2 up through LUT6. if `-module` or `-instance` are present the optimization directive is per the instance/module list if `-module` or `-instance` are not present this is a global directive.

  For example, with the following UTF commands

  - `optimization -lut_costs {10 10 10 50 100}`
  - `optimization -lut_costs {10 12 15 20 30} -module {my_hw_top}`
  - `optimization -lut_costs {10 10 12 15 20} -module {dut}`

    The list `{10 10 10 50 100}` is the global default, while the list `{10 12 15 20 30}` is used for module `my_hw_top`, and the list `{10 10 12 15 20}` is used for module DUT.
- `-enhanced_loop_xform <bool> [-module <module list>][-instance <instance list>]`: Specifies whether or not to use WLS's enhanced loop transformation. Default is `false`. This is currently experimental. If `-module` or `-instance` are present the optimization directive is per the instance/module list if `-module` or `-instance` are not present this is a global directive.
- `-enc_mux_threshold <int> -instance <list> [-regex]`: Controls technology mapping of encoded muxes in terms of the min. number of selector pins in an encoded mux (example: a vector indexing operation or a case statement) required for the mux to be mapped as FPGA fabric mux vs dissolved into LUTs. This is intended to be used by CAEs during bringup rather than the end user.
- `-expand_dsp_mult_threshold <int> -instance <list> [-regex]`: Specifies the max size of multiplier ops that do not use DSP
- `-drop_dead_logic <int> -instance <list> [-regex]`: Eliminate stateful logic that does not contribute to functionality of a module (at the expense of losing visibility on removed logic). True when using full optimization.

`-share_level <0|2> -module <list> [-regex]`

- `-inline_disable <module_list>`: disable inline on list of modules

  NOTE: *(this can get also pattern: * matches everything, ? matches any single character, [seq] matches any character in seq, [!seq] matches any character not in seq>]*

- `-never_inline <module_list>`: Set list of modules to be never inlined

  NOTE: *(this can get also pattern: * matches everything, ? matches any single character, [seq] matches any character in seq, [!seq] matches any character not in seq>]*

- `-never_inline_disable <module_list>`: Disable never inline on list of modules

  NOTE: *(this can get also pattern: * matches everything, ? matches any single character, [seq] matches any character in seq, [!seq] matches any character not in seq>]*

- `-top_down_roots <module_list>`: List of modules as top for limited top-down approach

- `-celldefine <bool>`: treats module in `` `celldefine `` block as UDP for cost computation when auto inlining.

  NOTE: *-celldefine option should only be used with -auto_inline_limit or -auto_inline_port_size_threshold . Default value is t.*

- `-area_effort <DEFAULT|LOW|MEDIUM|HIGH>`

- `-tree <module>`. This specifies as that this module and all below are optimized and mapped together.

  NOTE: *For Synplify Mapping, optimizations work better when the complete module tree is optimized together.*

- `-techmapping <REGULAR|TDS>`: This option is used to specify Timing Driven Synthesis using Synplify Mapping Technology.

  For example:

  ```
  optimization -tree {critical_module} -techmapping {TDS}
  ```

  This runs technology mapping using Synplify Timing Driven Synthesis on `critical_module` and the tree below.

  NOTE: `-techmapping` *should only be used with* `-tree`*. Default value is* `REGULAR`*.*

- `-techmapping_constraints_file <constraints for this module>`

NOTE: `-techmapping_constraints_file` *should only be used with* `-techmapping {TDS}`*. This should contain FDC constraints for this module tree.*

- `-techmapping_advanced_command_file <additional option to be passed to synplify>`

  NOTE: `-techmapping_advanced_command_file` *should only be used with* `-techmapping {TDS}`*. This should contain additional options for Synplify Timing Driven Synthesis.*

14.2 performance

Description

Specify performance options

```
performance [-clock_opt <bool>] [-dynamic_emu_stop_counter <int>] [-
dynamic_emulation <dpi=bool,vlog_force=bool,zforce=bool,zgate=bool>]
[-fetch_mode <bool>] [-safe_mode <bool>] [-safe_mode_params <
clock_latch=bool,memory=bool,set_reset=bool,skew_time=bool>] [-
zemi3_fm_mcp_opt <bool>] [-zemi3_fm_opt <bool>]
```

Option(s)

- `-clock_opt <bool>`: Optimize away the rarely used negedge (or posedge) of fastest design clock to improve throughput of the design. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-dynamic_emu_stop_counter <int>`: Specify number of `driverClk` cycles to stop during runtime to ensure dynamic emulation behavior. Valid values: A non-negative integer number.
- `-dynamic_emulation <dpi=bool,vlog_force=bool,zforce=bool,zgate=bool>`: Enables MCP evaluation to ignore certain rarely used paths and ensure correctness at runtime by holding `driverClk` when those paths are active.
- `-fetch_mode <bool>`: Enables/Disables fetch mode. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-zemi3_fm_opt <bool>`: Optimizes LUT usage and throughput in fetch mode. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)

Constraint (s)

`-zemi3_fm_mcp_opt` can only be used with `-zemi3_fm_opt`.

Note(s)

- `PDM_DIRECT`: PDM is enabled even for Original compilation. User defines which PARFF stages that they also like to introduce PDM based on the PARFF file
- `PDM_PARFF`: User defines which PARFF stages that they like to introduce PDM based on the PARFF file

15 Power

This section describes the following UTF commands:

- *power_profile*
- *set_power_estimation*

15.1 power_profile

Detailed Description

Enable power profile and debug dumping. The debug dumping signals can be specified by `$dumpvars` calls in design, and the power profiled signals are specified by power weighted profile, and all these power profiled signals are also debug signals.

```
profile -weight_profile <file> [-optimize
CAPACITY|BALANCED|PERFORMANCE] [-smash_hierarchy NONE | CRITNET |
MEMORY | BOTH] [-autodrop_extreme_small_memory_weight true|false]
```

Parameters

- `args`
  - `-weight_profile <file>`: Specify the power weight file generated by Spyglass to enable power profile and debug dumping. All the signals used by power profile are also debug dump signals.
  - `-optimize CAPACITY | BALANCED | PERFORMANCE`: Specify the optimization strategy for debug dump. Allocate the largest number of debug resources. Allocate the resource to balanced performance and capacity (default). Allocate the resource for best performance.
  - `-smash_hierarchy NONE | CRITNET | MEMORY | BOTH`: Specify to smash the instrumented memory or critical net instance hierarchy. Do not smash any instrumented power profile instances (default). Smash all the instrumented critical net power profile instances. Smash all the instrumented memory power profile instances. Smash both critical net and memory power profile instances.
  - `-autodrop_extreme_small_memory_weight true|false`: Enables the automatic dropping for extreme small memory weights in IP, which can impact accuracy.

    NOTE: *Since the hardware resource is limited, WAP cannot appropriately represent extreme small weight well, this option discards those extreme small memory weights automatically.*

    NOTE: *This option is disabled by default.*

15.2 set_power_estimation

Detailed Description

```
   set_power_estimation [-fnmatch] [-object_not_found
[fatal|warning]] [-rtlname_file <filename>]
           [-type [dynamic|fwc]] [-wire_file <filename>]
```

Description

Configures the behavior of the Power Estimation feature.

Optional Arguments

- `-fnmatch`: Indicates that object pathnames can contain wild cards.
- `-object_not_found [fatal|warning]`: Specifies the error policy when objects cannot be found.

  Available policies:

  - `fatal`: Default value. A fatal error is displayed.
  - `warning`: A warning is displayed instead of an error.
- `-rtlname_file <filename>`: Specifies the file containing the names of wires used for Power Estimation (one bit per line).
- `-type [dynamic|fwc]`: Specifies the capture mechanism used by Power Estimation. If not specified, fast-waveform-capture is preferred.

  Details about allowed values:

  - `dynamic`: Power Estimation is performed via dynamic-probes.
  - `fwc`: Power Estimation is done through fast waveform captures.
- `-wire_file <filename>`: Specifies the file containing the EDIF names of wires used for Power Estimation (one bit per line).

Command Usage Examples

```
- set_power_estimation -type fwc -rtlname_file ../../src/
power_est.txt
```

Power estimation is performed via the signals found in file `../../src/power_est.txt`.

16 Routing

This section describes the following UTF commands:

- *zpar*

16.1 zpar

Description

System-level place and route (**zPar**) options

```
zpar [-advanced_command <string>] [-advanced_command_file <file>] [-
direct_placement <bool>] [-effort <No|Low|Medium|High>] [-incremental
<bool>] [-max_parallel_jobs <int>] [-placement_number_of_jobs <int>]
```

Option(s)

- `-advanced_command <string>`: Command for **zPar**. `zpar` command
- `-advanced_command_file <file>`: Command file for **zPar**.
- `-direct_placement <bool>`: Use direct placement.
- `-effort <No|Low|Medium|High>`: Specify effort level.
- `-incremental <bool>`: Use zPar incremental mode.
- `-max_parallel_jobs <int>`: Maximum number of **zPar** jobs allowed(Default:0, parallelism is disabled). non-negative integer number.
- `-placement_number_of_jobs <int>`: Number of jobs for placement(Default:0, take default value from **zPar**). non-negative integer number.

Constraint(s)

At least one of the options should be used

Note(s)

- Higher number can potentially increase performance, but consume more computing resources.
- If value for `-placement_number_of_jobs` is not 0, `-max_parallel_jobs` with none zero value must also be defined

17 Runtime

This section describes the following UTF commands:

- *run_manager*

17.1 run_manager

Description

Specify run manager options

```
run_manager [-debug <bool>] [-number_of_instances <int>]
```

Option(s)

- `-debug <bool>`: Specifies whether visibility must be added inside the run manager instances.
- `-number_of_instances <int>`: Specify the number of run manager instances. This should be a positive number. non-negative integer number.

Constraint(s)

At least one of the options should be used

18 set_perf_flow

Description

Define perf flow

```
set_perf_flow<mode>[-patch<string>][-patch_list<list>]
```

Option(s):

- `mode <string>`: perf flow mode
- `-patch <string>`: patch name
- `-patch_list <list>`: list of allowed patch names

19 set_power_profile

Description

`set_power_profile [-bucket_file <file>] [-udp_width <16|32>] [-uip_if_fx_pairs <0|1|2|4>]`

Deprecated command: To be obsoleted. # Use `power_profile` instead.

Option(s)

- `-bucket_file <file>`: Specify the bucket file output by Spyglass
- `-udp_width <16|32>`: Specify the UDP bit width. 16 means each UDP bit width is 16k bits.
- `-uip_if_fx_pairs <0|1|2|4>`: Specify message pair number for conditions, `0|1|2|4`.
  - `0`: enable UIP without conditions.
  - `1`: enable UIP with 1 message pair for conditions and so on.

Constraint(s)

At least one of the options should be used

Example(s)

```
set_power_profile -uip_if_fx_pairs 1 -udp_width 32 -bucket_file {./bucket.txt}
```

20 SMART-ZICE

This section describes the following UTF commands:

- *smart_zice_config*

20.1 smart_zice_config

Description

Smart Z-Ice options

```
smart_zice_config [-connector <HE10>] [-vcc <1v5|1v8|2v5|3v3>]
```

Option(s)

- `-connector <HE10>`: Enable HE10 adapter.
- `-vcc <1v5|1v8|2v5|3v3>`: Value of VCC used for Smart Z-Ice.

Constraint(s)

At least one of the following options should be used: `-vcc|-connector`

Example(s)

```
smart_zice_config -vcc 1v8
smart_zice_config -vcc 3V3 -connector HE10
```

21 Synthesis

This section describes the following UTF commands:

- *assertion_synthesis*
- *dpi_synthesis*
- *synthesis*
- *synplifypro_synthesis*
- *synthesis_preferences*
- *system_tasks*
- *verilog_force_release*

21.1 assertion_synthesis

Detailed Description

```
assertion_synthesis  [-ignore (<sva_type>)] [-path <mod_inst_path>]
[-tree <top_module_name>] [-module <modules list>=""">] [-assert
<assertion_name>]
```

- sva_type can be:
  ALL|CONCURRENT|IMMEDIATE|ASSERT|COVER|PACKAGE|PROC|PROC_LOOP|CONCURRENT_PROC_LOOP|IMMEDIATE_PROC_LOOP
- +assert #instance_name: Synthesize given SVA instance
- -assert #instance_name: Do not synthesize given SVA instance
- +module #module_name: Synthesize all SVAs in all instances of given module
- -module #module_name: Do not synthesize all SVAs in all instances of given module
- +tree #hierarchy_name: Synthesize all SVAs below given hierarchy
- -tree #hierarchy_name: Do not synthesize all SVAs below given hierarchy
- +path #hierarchy_name: Synthesize all SVAs inside given hierarchy instance
- -path #hierarchy_name: Do not synthesize all SVAs inside given hierarchy instance
- -ignore
  ALL|CONCURRENT|IMMEDIATE|ASSERT|COVER|PACKAGE|PROC|PROC_LOOP|CONCURRENT_PROC_LOOP|IMMEDIATE_PROC_LOOP
  #assertion_type: Do not synthesize all SVAs of given type
- -enable ALL|ASSERT|COVER: Synthesize all/ASSERT/COVER SVAs in a design
- -verbose <bool>: Dump removed SVAs into report file 'reportSVA.log'.
- -cover_max_states <int>: Maximum number of states allowed for a Cover property.

- `-enable_ctrl_tasks <bool>`: Handle assertion control tasks in the design.
- `-unique_if_case <bool>`: Enable unique case and unique if transformation to generate violation reports
- `-never_fatal`: Never use SVA as fatal (do not apply SVA trigger)
- `-auto_disable`: Disable assertions after first failure. Improves performance but increases logic
- `-report_only_failure`: Only report SVA failures
- `-fire_all_triggers`, generate (`zsva_trigger == 1'b1`) for static trigger in `vcs.dve`, ignored if `-never_fatal` used

21.2 dpi_synthesis

Detailed Description

```
dpi_synthesis  [-path <mod_inst_path>] [-tree <top_module_name>] [-
module <modules list>] [-dpi <dpi_name>] [-hier <file_name>] [-enable
ALL|ALC] [-ignore FOR_LOOP] [-frequency <int>] [-advanced_dpi <bool>]
[-enable_wls <bool>] [-offline <bool>] [-timestamp <bool>] [-
optimize_width <bool>]
```

Parameters

`args`

- `+dpi #instance_name`: Synthesize given DPI function
- `-dpi #instance_name`: Do not synthesize given DPI function
- `+module #module_name`: Synthesize all DPI calls in all instances of given module
- `-module #module_name`: Do not synthesize all DPI calls in all instances of given module
- `+tree #hierarchy_name`: Synthesize all DPI calls below given hierarchy. This option is deprecated.
- `-tree #hierarchy_name`: Do not synthesize all DPI calls below given hierarchy. This option is deprecated.
- `+path #hierarchy_name`: Synthesize all DPI calls inside given hierarchy instance. This option is deprecated.
- `-path #hierarchy_name`: Do not synthesize all DPI calls inside given hierarchy instance. This option is deprecated.
- `-enable [ALL|ALC]`

NOTE:

- `ALL` *means Synthesize all DPI calls in a design*.

  - ALC *means Synthesize DPI calls in* `always_latch` *or* `always_comb`. ALC *can occur in the same* `dpi_synthesis` *command or by itself in a separate* `dpi_synthesis` *command, with other* `dpi_synthesis` *commands deciding which modules or instances have their DPI functions synthesized*.

- `-ignore for_loop`: Do not synthesize all DPI calls within a for loop
- `-hier #filename`: Specify list of DPI synthesis options in a given file. This option is not supported.
- `-frequency <int>`: Specify the theoretical DPI frequency (in KHz) to reach at run-time
- `-advanced_dpi <bool>`: Synthesize all DPI calls inside initial blocks and all DPI calls with output ports. Must be preceded by `-enable ALL` option.
- `-enable_wls <bool>`: Synthesize all DPI calls inside initial blocks and all DPI calls with output ports under ZS4 UC2 flow.
- 'debug -use_offline_debug true' is incompatible with 'dpi_synthesis -enable_wls true'. Also, do not add 'debug -offline_debug_params {INCL_XTORS=true}' to the UTF.
- `-offline <bool>`: Support Offline mode only when used along with `-enable_wls true`, otherwise this option has no effect
- `-timestamp <bool>`: Support timestamp only when used along with `-enable_wls true`, otherwise this option has no effect
- `-optimize_width <bool>`: Enable optimization of input bits for DPI call.

Duplicated command options are allowed.

21.3 synthesis

Detailed Description

Synthesis options

- `-advanced_command_file <filename>`: Specify legacy **zFast** command file which effects DUT and all transactors.
- `-advanced_command_file_dut_only <filename>`: Specify legacy **zFast** command file effects DUT only.
- `-advanced_command {<zFast_attribute>}`: Specify any legacy **zFast** command
- `-blackbox <blackbox_names>`: Specify units to be forced as blackboxes
- `-full_blackbox <blackbox_names>`: Specify units to be forced as blackboxes already from elaboration stage
- `-dont_make_bbox <blackbox_names>`: Specify units not to be treated as blackboxes
- `-blackbox_path <instance_names>`: Specify instances to be forced as blackboxes
- `-ignore_unique_case <bool>`: Ignore unique keyword in unique case statement
- `-check_utf_vs_advanced_command_file <bool>`: In WLS flow, do some consistency checks between UTF commands and synthesis advanced commands.
- `-wls_option {<wls_option>}`: Specify one wls option.

Note

- `-wls_option` and `-wls_option_file` are applied in the order in which the two of them are found in the UTF file.
- `-wls_option_file <filename>`: Specify additional `wls` option file

  NOTE: `-wls_option_file`*: option file can be set once throughout the UTF file*
- `-simon_option_file <filename>`: Deprecated. Specify additional simon option file.

  NOTE: `-simon_option_file`*: option file can be set once throughout the UTF file.*

Instead, use the newer option `-wls_option_file`.

- `-generate_db_for_fmcheck <bool>`: Generate database in WLS (Word Level Synthesis) flow for `fmcheck`
- `-generate_db_for_fmcheck_modules <module_names>`: Generate database in WLS (Word Level Synthesis) flow for specified units for `fmcheck`.
- `-generate_db_for_fmcheck_module_file <module_file>`: Generate database in WLS (Word Level Synthesis) flow for the units specified in the module file for `fmcheck`.
- `-enable_xmr_check <bool>`: Enable the XMR connectivity check in WLS (Word Level Synthesis) flow, disabled by default
- `-max_loop_iterations <int>`: Specify maximum loop iterations limit.
- `-use_vfs <bool>`: Enable the use of VFS (virtual file system)
- `-wls_enhanced_blackbox_support <bool>`: Enable enhanced blackbox support; default false.
- `-real_number_modeling <bool>`: Enable synthesis of real data type with floating point format; default false.
- `-synthesize_shortreal_with_32bits <bool>`: Enable synthesis of short real in 32-bits floating point format; default `false`.
- `-enhanced_sv_interface_support <bool>`: Enable enhanced System Verilog interface support in WLS (Word Level Synthesis) flow.
- `-enhanced_var_select_xmr <bool>`: avoid module splitting for read XMR with variable select.
- `-disable_bidir_native_xmr <bool>`: process bidirectional XMR at back-end compile.
- `-user_override_fpga_prims <bool>`: allow xilinx primitives definition by user

21.4 synplifypro_synthesis

Detailed Description

Specify synplifypro synthesis groups

- `#name | +tree #name | -tree #name`: Specify hierarchy to be synthesized with `synplifypro`
- `-groupname #group_name`: Synthesis group name
- `-options {name=value ... nameN=valueN}`: Synthesis options
- -real_number_modeling <bool>: Enable synthesis of real data type with floating point format; default false.
- -fp_perf_mode <int>: Enable performance optimization on floating point, different value means different levels; default 0.
- -fp_perf_mode_diag <bool>: Enable diagnostic performance optimization on floating point; default false.
- -synthesize_shortreal_with_32bits <bool>: Enable synthesis of shortreal in 32-bits floating point format; default false.
- -enhanced_sv_interface_support <bool>: Enable enhanced sv interface support in WLS (Word Level Synthesis) flow.
- -enable_xmr_threads <bool>: Enable multi-threaded support in native XMR processing. Enabled by default.
- -hierarchy_info <path>: Hierarchical path for each module in the design dump directory for bottom up compile
- -enhanced_var_select_xmr <bool>: Avoid module splitting for read XMR with variable select.
- -disable_bidir_native_xmr <bool>: Process bidirect XMR at back-end compile.
- -user_override_fpga_prims <bool>: Allow xilinx primitives definition by user
- -consistency_check <bool>: Check the synthesis data structures for consistency.
- Option -task cannot be used without one of the following options:
  - -enable
  - -replace
  - -module

- -enable and -module are mutual exclusive, either enabling on all design or on selective modules.

21.5 synthesis_preferences

Description

Specify synthesis preferences

```
synthesis_preferences [-bundle_mode <string>] [-enable_fmcheck_debug
<bool>] [-enable_wls <bool>] [-log_files <ALWAYS|NEVER|DEFAULT>]
```

Option(s)

- `-bundle_mode <string>`: Specify bundle mode for synthesis. | `SIZE=<int>` | `CARDINAL=<int>`
- `-enable_fmcheck_debug <bool>`: Enabling/Disabling the dumping of encrypted `db`.
- `-enable_wls <bool>`: Enable the WLS (Word Level Synthesis) flow.
- `-log_files <ALWAYS|NEVER|DEFAULT>`: Whether to create log files in `zcui.work/design/synth_Default_RTL_Group/synthesis_log_dir`.
  - `ALWAYS`: Do create the log files.

    Valid values: `ALWAYS|always|Always`
  - `NEVER`: Do not create the log files.

    Valid values: `NEVER|never|Never`
  - `DEFAULT`: The default, currently, is to create the log files.

    Valid values: `DEFAULT|default|Default`

Constraint(s)

At least one of the options should be used

21.6 system_tasks

Detailed Description

Specifies list of hierarchies under which system task/function calls are NOT removed, and are given to synthesis.

NOTE: *All system task/function calls are removed by default except for SVA calls.*

- `-task #task_name"`: Specify system task
- `-replace #replace_value`: Replace system task with given string
- `-exclude #list_of_hierarchies_to_exclude`: Specify list of hierarchies to exclude
- `-remove SVA`: Global option to remove all system tasks from SVAs
- `-enable`: Enable built-in support for system task. Currently only supports `$display`, `$displayh`, `$displayb`.
- `-module #list_of_modules`: Specify list of modules under which system task are not removed and are given to synthesis.
- One of the following options -task, -remove must be used.
  - The `-task` option cannot be used without one of the following options: `-enable`, `-replace`, `-module`.
  - `-enable` and `-module` are mutual exclusive, either enabling on all design or on selective modules.

21.7 verilog_force_release

Description

This command is used to enable or disable support for Verilog force/release statements.If enabled(enable/enable_wls/enable_mixed), the default state is that force/release statements are honored.If disabled, the default state is that force/release statements are ignored.

```
verilog_force_release [-create_task <bool>] [-enable <bool>] [-
enable_mixed <bool>] [-enable_wls <bool>] [-enable_zprop <bool>] [-
exclude <list>] [-include <list>] [-local_driver_check <bool>] [-
treat_as_wire <bool>]
```

Option(s)

- `-create_task <bool>`: create sys-task for synthesis Verilog force/release support. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-enable <bool>`: Sets the default state to enabled/disabled for back-end support for Verilog force/release statements.
- `-enable_mixed <bool>`: Enable synthesis support for Verilog force statements only for logic/reg type nodes on input portconnect and output port, `-enable`, `-include` and `-exclude` are ignored in this mode. and it is exclusive with `-enable_wls`.
- `-enable_wls <bool>`: Enable synthesis support for Verilog force statements, `-enable`, `-include` and `-exclude` are ignored in this mode. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-enable_zprop <bool>`: Enable z value propagation for synthesis Verilog force/release support. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-exclude <list>`: Disables support for force/release statements in these modules, regardless of the default state.
- `-include <list>`: Enables support for force/release statements in these modules, regardless of the default state.

- `-local_driver_check <bool>`: Do not trace driver of the forced signals and only local connection of target wires are forced when set to true.
- `-treat_as_wire <bool>`: Also trace driver of the signals with type `reg` | `logic` | `bit` when set to `true`.

Constraint(s)

At least one of the options should be used

22 System

This section describes the following UTF commands:

- *architecture_file*
- *create_new_target*
- *design_size*
- *pbuild*

22.1 architecture_file

Description

Specify target architecture file for compilation

```
architecture_file -filename <file>
```

Option(s)

- `-filename <file>`: Path to architecture file. Mandatory option

Constraint(s)

At least one of the options should be used

22.2 create_new_target

Detailed Description

- `-open_block <string>`: Open target commands block with specific `<name>`.
- `-close_block <string>`: Close target commands block with specific `<name>`.

  block cannot be opened inside another target block. can open and close block with the same name several times. inside blocks with the same name is assigned to the same target.

  only UTF commands and options which are translated only into backend commands are allowed inside a target block.

Description

Target block actions (multiple target feature) Handles creation and closure of atarget block

```
create_new_target [-close_block <string>] [-open_block <string>]
```

Option(s)

- `-close_block <string>`: Closes a target block. name
- `-open_block <string>`: Opens a new target block or continue existing target block. name

Constraint(s)

At least one of the options should be used

22.3 design_size

Description

Specify number of modules to be used

```
design_size <bram> <dsp> <fwc_bit> <fwc_ip> <lut> <lut6> <qiwc_bit>
<ramlut> <read_ports_bits> <read_ports_ips> <reg> <uram>
<write_ports_bits> <write_ports_ips> <zc_trace_bits> <zcei_mess_in>
<zcei_mess_out> <zrm_ports> <zrm_slots> <zview_bits> [-
max_number_of_modules <float>] [-mode <AUTO|FULL>] [-
number_of_modules <float>] [-resource_margin <float>] [-
resource_margin_details
<bram=float,dsp=float,fwc_bit=float,fwc_ip=float,lut=float,lut6=float
,qiwc_bit=float,ramlut=float,read_ports_bits=float,read_ports_ips=flo
at,reg=float,uram=float,write_ports_bits=float,write_ports_ips=float,
zc_trace_bits=float,zcei_mess_in=float,zcei_mess_out=float,zrm_ports=
float,zrm_slots=float,zview_bits=float>]
```

Option(s)

- `bram <float>`: `bram` fillrate in %. positive float number.
- `dsp <float>`: `dsp` fillrate in %. positive float number.
- `fwc_bit <float>`: `fwc_bit` fillrate in %. positive float number.
- `fwc_ip <float>`: `ramlut` fillrate in %. positive float number.
- `lut <float>`: `lut` fillrate in %. positive float number.
- `lut6 <float>`: `lut6` fillrate in %. positive float number.
- `qiwc_bit <float>`: `qiwc_bit` fillrate in %. positive float number.
- `ramlut <float>`: `ramlut` fillrate in %. positive float number.
- `read_ports_bits <float>`: `read_port_bits` fillrate in %. positive float number.
- `read_ports_ips <float>`: `read_port_ips` fillrate in %. positive float number.

- `reg <float>`: `reg` fillrate in %. positive float number.
- `uram <float>`: `bram` fillrate in %. positive float number.
- `write_ports_bits <float>`: `write_port_bits` fillrate in %. positive float number.
- `write_ports_ips <float>`: `write_port_ips` fillrate in %. positive float number.
- `zc_trace_bits <float>`: `zc_trace_bits` fillrate in %. positive float number.
- `zcei_mess_in <float>`: `zcei_mess_in` fillrate in %. positive float number.
- `zcei_mess_out <float>`: `zcei_mess_out` fillrate in %. positive float number.
- `zrm_ports <float>`: `zrm_ports` fillrate in %. positive float number.
- `zrm_slots <float>`: `zrm_slots` fillrate in %. positive float number.
- `zview_bits <float>`: `zview_bits` fillrate in %. positive float number.
- `-max_number_of_modules <float>`: Represents the maximum number of modules can be used in case of AUTO mode. Should be a positive integer, or 0.5. When compiling for ZS4 HW it is possible to specify 0.5 to map the design on a half-module. positive float number.
- `-mode <AUTO|FULL>`: Specifies `design_size` configuration mode. enables automatic `zcore`, generation, `FULL - full target`
- `-number_of_modules <float>`: Specifies maximum number of modules to be used. Should be a positive integer, or 0.5. When compiling for ZS4 HW it is possible to specify 0.5 to map the design on a half-module. positive float number.
- `-resource_margin <float>`: Specifies margin for design size estimation. positive float number.
- `-resource_margin_details <bram=float,dsp=float,fwc_bit=float,fwc_ip=float,lut=float,lut6=float,qiwc_bit=float,ramlut=float,read_ports_bits=float,read_ports_ips=float,reg=float,uram=float,write_ports_bits=float,write_ports_ips=float,zc_trace_bits=float,zcei_mess_in=float,zcei_mess_out=float,zrm_ports=float,zrm_slots=float,zview_bits=float>`: Specify margin for design size

estimation for the specified resource type Available resources types are: `lut, lut6, bram, reg, dsp, ramlut, fwc_bit, fwc_ip, qiwcread_port_bits, write_port_bits, zcei_mess_out, zc_trace_bits, zview_bits, zrm_slots, zrm_ports`.

- `bram <float>`: `bram` fillrate in %. positive float number.
- `dsp <float>`: `dsp` fillrate in %. positive float number.
- `fwc_bit <float>`: `fwc_bit` fillrate in %. positive float number.
- `fwc_ip <float>`: `ramlut` fillrate in %. positive float number.
- `lut <float>`: `lut` fillrate in %. positive float number.
- `lut6 <float>`: `lut6` fillrate in %. positive float number.
- `qiwc_bit <float>`: `qiwc_bit` fillrate in %. positive float number.
- `ramlut <float>`: `ramlut` fillrate in %. positive float number.
- `read_ports_bits <float>`: `read_port_bits` fillrate in %. positive float number.
- `read_ports_ips <float>`: `read_port_ips` fillrate in %. positive float number.
- `reg <float>`: `reg` fillrate in %. positive float number.
- `uram <float>`: `bram` fillrate in %. positive float number.
- `write_ports_bits <float>`: `write_port_bits` fillrate in %. positive float number.
- `write_ports_ips <float>`: `write_port_ips` fillrate in %. positive float number.
- `zc_trace_bits <float>`: `zc_trace_bits` fillrate in %. positive float number.
- `zcei_mess_in <float>`: `zcei_mess_in` fillrate in %. positive float number.
- `zcei_mess_out <float>`: `zcei_mess_out` fillrate in %. positive float number.
- `zrm_ports <float>`: `zrm_ports` fillrate in %. positive float number.
- `zrm_slots <float>`: `zrm_slots` fillrate in %. positive float number.

- zview_bits <float>: `zview_bits` fillrate in %. positive float number.

Constraint(s)

- `-number_of_modules` cannot be used with any of the following options: `-mode`
- `-number_of_modules` cannot be used with any of the following options: `-max_number_of_modules`

At least one of the options should be used

Note(s)

- The `-mode` option could not be used with the `-number_of_modules` option.
- `-mode AUTO` does not imply the automatic core partitioning. It must be enabled explicitly by '`clustering -system_auto_core_generation true`'

Example(s)

```
design_size -resource_margin_details {lut=20}
design_size -resource_margin 15
```

22.4 pbuild

Detailed Description

- `-user_script #filename`: Specify filename. Mutually exclusive from all other options.
- `-advanced_command_file #filename`: Specify advanced command file for **pBuild**
- `-advanced_command {<pBuild_command>}`: Specify any `pBuild` command

23 Timing

This section describes the following UTF commands:

- *timing_analysis*
- *timing_constraint*
- *set_false_path_from*
- *set_false_path_to*
- *set_global_false_path*

23.1 timing_analysis

Description

Specify timing analysis options

```
timing_analysis [-advanced_async_set_reset_analysis <bool>] [-
advanced_command <string>] [-constraints_input_file <file>] [-
delay_min_zfilter_skew <int>] [-fpga_advanced_command <string>] [-
fpga_advanced_command_file <file>] [-post_fpga
<SKEW|FILTER|NONE|BACK_ANNOTATED>] [-post_fpga_placement <bool>] [-
pre_fpga <LINEAR_DELAY_MODEL|CONSTANTS_BASE_DELAY_MODEL>] [-
report_input_file <file>] [-use_hdl_names <bool>]
```

Option(s)

- `-advanced_async_set_reset_analysis <bool>`: Enables advanced asynchronous set/reset analysis mode (adds asynchronous path into account at multi-cycle path analysis). Default value: False.
- `-advanced_command <string>`: Specify any legacy **zTime** command. _command
- `-constraints_input_file <file>`: Specify filename with **zTime** constraints.
- `-delay_min_zfilter_skew <int>`: Specify the minimum delay (in [ps]) between filter to skew. Default: 40000. non-negative integer number.
- `-fpga_advanced_command <string>`: Command for zFpgaTiming. _command
- `-fpga_advanced_command_file <file>`: Command for zFpgaTiming.
- `-post_fpga <SKEW|FILTER|NONE|BACK_ANNOTATED>`:
  - `SKEW`: Enable the skew time update computation. Valid values: `SKEW|Skew|skew`
  - `FILTER`: Enable the filter time update computation. Valid values: `FILTER|Filter|filter`

  - ❒ NONE: Disable the timing analysis. Valid values: NONE|None|none
  - ❒ BACK_ANNOTATED: Enable SDF timing analysis and disable SKEW and FILTER timing analysis. Valid values: BACK_ANNOTATED|Back_Annotated|back_annotated
- -post_fpga_placement <bool>: Enable/disable the place timing analysis after the ZTIME_ANALYSE_PLACE phase. Default: false.
- -pre_fpga <LINEAR_DELAY_MODEL|CONSTANTS_BASE_DELAY_MODEL>: enables lut/fanout based delay model in **zTime** pre fpga CONSTANTS_BASE_DELAY_MODEL is the default value which disables the pre fpga timing analysis.
- -report_input_file <file>: Specify filename with **zTime** report commands.
- -use_hdl_names <bool>: Enable/disable the usage of HDL names in **zTime** report. Default: false.

Constraint(s)

At least one of the options should be used

23.2 timing_constraint

Description

Specify timing constraints for zTime

```
timing_constraint [-command <SET_FALSE_PATH>] [-from_match <string>]
[-from_match_alias <string>] [-global_match <string>] [-to_match
<string>] [-to_match_alias <string>] [-verbose <bool>]
```

Option(s)

- `-command <SET_FALSE_PATH>`: Specify false path constraints and port/instance/alias name (currently wild card patterns are based, case sensitive) to or from which all paths should be considered as false paths is taken in argument.
- `-from_match <string>`: Matching pattern of ports/instances from which all paths should be considered as false paths.
- `-from_match_alias <string>`: Matching pattern of aliases from which all paths should be considered as false paths.
- `-global_match <string>`: Matching pattern of aliases and wires on which all paths should be considered as false paths.
- `-to_match <string>`: Matching pattern of ports/instances to which all paths should be considered as false paths.
- `-to_match_alias <string>`: Matching pattern of aliases to which all paths should be considered as false paths.
- `-verbose <bool>`: Display the name of false paths found.

Constraint(s)

At least one of the options should be used

23.3 set_false_path_from

Description

This command is used to specify false path constraints

```
set_false_path_from [-case_sens <bool>] [-ins <string>] [-match
<string>] [-match_alias <string>] [-match_ins <string>] [-match_port
<string>] [-match_wire <string>] [-port <string>] [-verbose <bool>]
```

Option(s)

- `-case_sens <bool>`: Matching pattern is case sensitive.
- `-ins <string>`: Specifies the name of the FPGA instance in **zCoreBuild** generated EDIF file of the FPGA instance
- `-match <string>`: Matching pattern using the form `Ins_pattern/Port_pattern`.
- Matching pattern using the form `Ins_pattern/Port_pattern`
- `-match_alias <string>`: Matching alias name. alias name
- `-match_ins <string>`: Matching pattern for FPGA instance name. pattern for FPGA instance name
- `-match_port <string>`: Matching port name pattern. port name pattern
- `-match_wire <string>`: Matching wire name. wire name
- `-port <string>`: Specifies FPGA port name. port name
- `-verbose <bool>`: Displays the name of false paths found.

Constraint(s)

At least one of the options should be used

Note(s)

This command is used to specify false path constraints. All paths starting from this port should be considered as false paths. This port is defined with the '-port=<Port_name>' argument. If it is not a primary port then the '-ins=<Ins_name>' argument must be provided to specify the name of the FPGA instance of the port. Port name and instance name can be specified directly with the '-port=<Port_name>' and '-ins=<Ins_name>' arguments or with wild cards with '-match_port=<Pattern_port>' and '-match_ins=<Pattern_ins>'. **zTime** supports Unix wild cards. Alternatively the '-match' option can be used to specify a match pattern like Ins_pattern/Port_pattern.

23.4 set_false_path_to

Description

This command is used to specify false path constraints.

```
set_false_path_to [-case_sens <bool>] [-ins <string>] [-match
<string>] [-match_alias <string>] [-match_ins <string>] [-match_port
<string>] [-match_wire <string>] [-port <string>] [-verbose <bool>]
```

Option(s)

- `-case_sens <bool>`: Matching pattern is case sensitive.
- `-ins <string>`: Specifies the name of the FPGA instance in **zCoreBuild** generated EDIF file. of the FPGA instance
- `-match <string>`: Matching pattern using the form `Ins_pattern/Port_pattern`.
- `-match_alias <string>`: Matching alias name. alias name
- `-match_ins <string>`: Matching pattern for FPGA instance name. pattern for FPGA instance name
- `-match_port <string>`: Matching port name pattern. port name pattern
- `-match_wire <string>`: Matching wire name. wire name
- `-port <string>`: Specifies FPGA port name. port name
- `-verbose <bool>`: Displays the name of false paths found.

Constraint(s)

At least one of the options should be used

Note(s)

This command is used to specify false path constraints. All paths ending on this port

should be considered as false paths. This port is defined with the '-port=<Port_name>' argument. If it is not a primary port, i.e not in IF FPGA, then the '-ins=<Ins_name>' argument must be provided to specify the name of the FPGA instance of the port. Port name and instance name can be specified directly with the '-port=<Port_name>' and '-ins=<Ins_name>' arguments or with wild cards with '-match_port=<Pattern_port>' and '-match_ins=<Pattern_ins>'. This command supports Unix wild cards. Alternatively the '-match' option can be used to specify a match pattern like Ins_pattern/Port_pattern.

23.5 set_global_false_path

Detailed Description

Specifies global false path constraints to a given node

Usage

```
set_global_false_path [-match=<string>]
```

This command is used to specify global false path constraints on each port and wire names that match a given pattern.

This command supports Unix wild cards. The '`-match`' option is used to specify a match pattern.

- `-match=<string>`: Matching pattern using the form `Ins_pattern/Port_pattern`
- `-case_sens=<bool>`: Matching pattern is case sensitive
- `-verbose=<bool>`: Displays the name of false paths found

24 Transactors

This section describes the following UTF commands:

- *scemi*
- *xtors*
- *zcei*
- *zemi3*
- *zemi4*

24.1 scemi

Detailed Description

SCEMI transactor options

- `-module {list_of_scemi_transactors_modules}`
- `-instance <xmr path to xtor>  (at least one of)[ -debug <bool>|-edge_enable <bool>|-disable <xmr to signal>  ]`
- `-debug <bool>`: Specifies whether visibility must be added inside the transactor or not
- `-edge_enable <bool>`: Specifies whether flops initially synchronized by the input zcei clock are updated with an edge enable block around
- `-disable <xmr to signal>`: Provides a signal that disables the transactor when it is 0
- `-time_stamp [no|uctrl|ctrl]`: Timestamp mode: no timestamp/ uncontrolled timestamp/controlled timestamp
- `-time_stamp_clk <xmr path to clock>`
- `-advanced_synth_command_file <filename>`: Where filename is transactor is specific to global `hcsrc` commands file name

Note

`-advanced_synth_command_file` must be used with `-module`, and should not be used with `-instance`.

24.2 xtors

Description

Marks instance as `Xtor`

```
xtors [-add <string>] [-add_xtor_path <string>] [-mapping_script
<string>] [-type <string>] [-use_zebu_ip_root <bool>]
```

Option(s)

- `-add <string>`: Specify the instance which is marked as `Xtor`. the instance which is be marked as `Xtor`.
- `-add_xtor_path <string>`: Add path to transactor.
- `-mapping_script <string>`: Specify transactor defmapping.
- `-type <string>`: Specify the type of `Xtor` (now support only `zemi3`).
- `-use_zebu_ip_root <bool>`: Use `ZEBU_IP_ROOT` to locate transactors.

Constraint(s)

At least one of the options should be used

24.3 zcei

zcei args

Detailed Description

ZCEI transactor options

- `-module {list_of_zcei_transactors_modules}`
- `-instance <xmr path to xtor>`: (at least one of) `[ -debug <bool>|-edge_enable <bool>|-disable <xmr to signal> ]`
- `-debug <bool>`: Specifies whether visibility must be added inside the transactor or not
- `-edge_enable <bool>`: Specifies whether flops initially synchronized by the input zcei clock are updated with an edge enable block around
- `-disable <xmr to signal>`: Provides a signal that disables the transactor when it is 0
- `-advanced_synth_command_file <filename>`: Where filename is `xtor` specific global `hcsrc` commands file name

Note

`-advanced_synth_command_file` must be used with `-module`, and should not be used with `-instance`.

24.4 zemi3

Description

ZEMI-3 transactor options

```
zemi3 [-advanced_synth_command_file <file>] [-
all_tf_args_are_automatic <bool>] [-allow_mixed_design_clocks <bool>]
[-allow_streaming <bool>] [-async_reset_init <bool>] [-
auto_flush_interval <int>] [-buffered_out_ports_default_width <int>]
[-buffered_out_ports_disable <bool>] [-buffered_out_ports_regardless
<bool>] [-debug <bool>] [-debug_zemi_behav <bool>] [-default_cclk
<string>] [-disable <string>] [-disable_all_xtors <bool>] [-
do_profiling <bool>] [-edge_enable <bool>] [-emit_initial <bool>] [-
exports_excluded_from_back_to_back <list>] [-
external_controlled_clocks <list>] [-hard_max_in_port_width <int>] [-
hard_max_out_port_width <int>] [-instance <list>] [-
max_clocked_loop_iterations <int>] [-max_in_port_width <int>] [-
max_loop_iterations <int>] [-max_out_port_width <int>] [-
merge_multiple_comb_writers <bool>] [-module <list>] [-
optimize_dpi_constant_args <bool>] [-port_optimization_mode
<0|1|2|3>] [-port_width_slop_percent <int>] [-profile_counters_width
<int>] [-protolink <bool>] [-reduce_control_paths <bool>] [-
resolve_events_globally <bool>] [-sample_clock_mode <bool>] [-
start_in_back_to_back <bool>] [-streaming_is_default <bool>] [-
support_dollar_display <bool>] [-task_streaming_is_default <bool>] [-
timestamp <bool>] [-transform_latch <bool>] [-
treat_warnings_as_errors <bool>]
```

Option(s)

- `-advanced_synth_command_file <file>`: filename is transactor specific global `hcsrc` commands file name.
- `-all_tf_args_are_automatic <bool>`: `all_tf_args_are_automatic`.

- `-allow_mixed_design_clocks <bool>`: `allow_mixed_design_clocks`.
- `-allow_streaming <bool>`: allow streaming.
- `-async_reset_init <bool>`: `-async_reset_init` is a global option.
- `-auto_flush_interval <int>`: positive integer number.
- `-buffered_out_ports_default_width <int>`: positive integer number.
- `-buffered_out_ports_disable <bool>`: `buffered_out_ports_disable`.
- `-buffered_out_ports_regardless <bool>`: `buffered_out_ports_regardless`.
- `-debug <bool>`: Specifies whether visibility must be added inside the transactor or not.
- `-debug_zemi_behav <bool>`: `debug_zemi_behav`.
- `-default_cclk <string>`: xmr to signal that is connected to `zceiClockport`. to signal that is connected to `zceiClockport`
- `-disable <string>`: Provides a signal that disables the transactor when it is 0. to signal
- `-disable_all_xtors <bool>`: `-disable_all_xtors` is a global option which provides a disable signal for each transactor instance. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-do_profiling <bool>`: do profiling.
- `-edge_enable <bool>`: Specifies whether flops initially synchronized by the input `zcei` clock are updated with an edge enable block around.
- `-emit_initial <bool>`: `emit_initial`.
- `-exports_excluded_from_back_to_back <list>` `list_of_export_DPI_excluded_from_back_to_back_mode`.
- `-external_controlled_clocks <list>`: `list_of_external_controlled_clocks`.
- `-hard_max_in_port_width <int>`: positive integer number.
- `-hard_max_out_port_width <int>`: positive integer number.

- `-instance <list>`: list of instances.
- `-max_clocked_loop_iterations <int>`: positive integer number.
- `-max_in_port_width <int>`: positive integer number.
- `-max_loop_iterations <int>`: positive integer number.
- `-max_out_port_width <int>`: positive integer number.
- `-merge_multiple_comb_writers <bool>`: `merge_multiple_comb_writers`.
- `-module <list>`: list of transactors modules.
- `-optimize_dpi_constant_args <bool>`: `-optimize_dpi_constant_args` is a global option.
- `-port_optimization_mode <0|1|2|3>`: Specify port optimization mode.
  - |1|2|3 0 for `AREA_OPT`
  - 1 for `THROUGHPUT_OPT`
  - 2 for `LATENCY_OPT`
  - 3 for `DEFAULT_OPT`
- `-port_width_slop_percent <int>`: positive integer number.
- `-profile_counters_width <int>`: positive integer number.
- `-protolink <bool>`: `protolinks`.
- `-reduce_control_paths <bool>`: reduce control paths.
- `-resolve_events_globally <bool>`: `-resolve_events_globally` is a global option.
- `-sample_clock_mode <bool>`: `-sample_clock_mode` is a global option.
- `-start_in_back_to_back <bool>`: start in back to back.
- `-streaming_is_default <bool>`: streaming is default.
- `-support_dollar_display <bool>`: support `$DISPLAY`.
- `-task_streaming_is_default <bool>`: `task_streaming_is_default`.
- `-timestamp <bool>`: `-timestamp` can be used with or without `-module`.

- `-transform_latch <bool>`: `transform_latch`.
- `-treat_warnings_as_errors <bool>`: `-treat_warnings_as_errors` is a global option.

Constraint(s)

- `-emit_initial` can only be used with `-module`
- global options cannot be combined with `-instance`|`-module` options
- `-advanced_synth_command_file` can only be used with `-module`
- check for mandatory combinations of options
- `-advanced_synth_command_file` cannot be used with any of the following options: `-instance`
- `-instance` cannot be used with any of the following options:
  - `-allow_streaming`
  - `-start_in_back_to_back`
  - `-support_dollar_display`
  - `-reduce_control_paths`
  - `-do_profiling`
  - `-streaming_is_default`
  - `-task_streaming_is_default`
  - `-emit_initial`
  - `-hard_max_out_port_width`
  - `-hard_max_in_port_width`
  - `-auto_flush_interval`
  - `-buffered_out_ports_disable`
  - `-buffered_out_ports_default_width`
  - `-buffered_out_ports_regardless`
  - `-port_optimization_mode`

- -profile_counters_width
- -max_out_port_width
- -max_in_port_width
- -port_width_slop_percent
- -all_tf_args_are_automatic
- -external_controlled_clocks
- -allow_mixed_design_clocks
- -exports_excluded_from_back_to_back
- -max_loop_iterations
- -max_clocked_loop_iterations
- -merge_multiple_comb_writers
- -transform_latch
- -debug_zemi_behav
- -default_cclk
- -sample_clock_mode
- -timestamp
- -protolink
- -sample_clock_opt
- -rt_diag
- -rt_config
- -resolve_events_globally
- -async_reset_init
- -optimize_dpi_constant_args
- -treat_warnings_as_errors

- -sample_clock_mode cannot be used with any of the following options: -sample_clock_opt

At least one of the options should be used

- The '-instance' option should be used with at least one of the following options: -debug|-edge_enable|-disable
- The -instance option cannot be used with any of the following options: -advanced_synth_command_file

Note(s)

- -advanced_synth_command_file must be used with -module, and should not be used with -instance
- Usage for the -instance option:

  -instance is only valid with -debug|-edge_enable|-disable, other options cannot be used with -instance
- -default_cclk </tt> can be used either with -module in which case it refers to specific modules, or without -module in which case it refers to all transactors defined until now.

24.5 zemi4

Description

ZEMI4 transactor options

This command is deprecated. You can use the *simxl* command.

```
zemi4 [-advanced_synth_command_file <file>] [-
all_tf_args_are_automatic <bool>] [-allow_mixed_design_clocks <bool>]
[-allow_streaming <bool>] [-async_reset_init <bool>] [-
auto_flush_interval <int>] [-buffered_out_ports_default_width <int>]
[-buffered_out_ports_disable <bool>] [-buffered_out_ports_regardless
<bool>] [-debug <bool>] [-debug_zemi_behav <bool>] [-default_cclk
<string>] [-disable <string>] [-disable_all_xtors <bool>] [-
do_profiling <bool>] [-edge_enable <bool>] [-emit_initial <bool>] [-
exports_excluded_from_back_to_back <list>] [-
external_controlled_clocks <list>] [-hard_max_in_port_width <int>] [-
hard_max_out_port_width <int>] [-instance <list>] [-
max_clocked_loop_iterations <int>] [-max_in_port_width <int>] [-
max_loop_iterations <int>] [-max_out_port_width <int>] [-
merge_multiple_comb_writers <bool>] [-module <list>] [-
optimize_dpi_constant_args <bool>] [-port_optimization_mode
<0|1|2|3>] [-port_width_slop_percent <int>] [-profile_counters_width
<int>] [-protolink <bool>] [-reduce_control_paths <bool>] [-
resolve_events_globally <bool>] [-sample_clock_mode <bool>] [-
start_in_back_to_back <bool>] [-streaming_is_default <bool>] [-
support_dollar_display <bool>] [-task_streaming_is_default <bool>] [-
timestamp <bool>] [-transform_latch <bool>] [-
treat_warnings_as_errors <bool>]
```

Option(s)

- `-advanced_synth_command_file <file>`: `filename` is a transactor specific global `hcsrc` commands file name.
- `-all_tf_args_are_automatic <bool>`: `all_tf_args_are_automatic`.

- `-allow_mixed_design_clocks <bool>`: `allow_mixed_design_clocks`.
- `-allow_streaming <bool>`: allow streaming.
- `-async_reset_init <bool>`: `-async_reset_init` is a global option.
- `-auto_flush_interval <int>`: positive integer number.
- `-buffered_out_ports_default_width <int>`: positive integer number.
- `-buffered_out_ports_disable <bool>`: `buffered_out_ports_disable`.
- `-buffered_out_ports_regardless <bool>`: `buffered_out_ports_regardless`.
- `-debug <bool>`: Specifies whether visibility must be added inside the transactor or not.
- `-debug_zemi_behav <bool>`: `debug_zemi_behav`.
- `-default_cclk <string>`: xmr to signal that is connected to `zceiClockport`. to signal that is connected to `zceiClockport`
- `-disable <string>`: Provides a signal that disables the transactor when it is 0. to signal
- `-disable_all_xtors <bool>`: `-disable_all_xtors` is a global option which provides a disable signal for each transactor instance. Valid values: `0|1|f|false|n|no|t|true|y|yes` (case insensitive)
- `-do_profiling <bool>`: do profiling.
- `-edge_enable <bool>`: Specifies whether flops initially synchronized by the input ZCEI clock are updated with an edge enable block around.
- `-emit_initial <bool>`: `emit_initial`.
- `-exports_excluded_from_back_to_back <list>` `list_of_export_DPI_excluded_from_back_to_back_mode`.
- `-external_controlled_clocks <list>`: `list_of_external_controlled_clocks`.
- `-hard_max_in_port_width <int>`: positive integer number.
- `-hard_max_out_port_width <int>`: positive integer number.

- `-instance <list>`: list of instances.
- `-max_clocked_loop_iterations <int>`: positive integer number.
- `-max_in_port_width <int>`: positive integer number.
- `-max_loop_iterations <int>`: positive integer number.
- `-max_out_port_width <int>`: positive integer number.
- `-merge_multiple_comb_writers <bool>`: `merge_multiple_comb_writers`.
- `-module <list>`: list of transactors modules.
- `-optimize_dpi_constant_args <bool>`: `-optimize_dpi_constant_args` is a global option.
- `-port_optimization_mode <0|1|2|3>`: Specify port optimization mode.
  - `|1|2|3 0 for AREA_OPT`
  - `1 for THROUGHPUT_OPT`
  - `2 for LATENCY_OPT`
  - `3 for DEFAULT_OPT`
- `-port_width_slop_percent <int>`: positive integer number.
- `-profile_counters_width <int>`: positive integer number.
- `-protolink <bool>`: protolinks.
- `-reduce_control_paths <bool>`: reduce control paths.
- `-resolve_events_globally <bool>`: `-resolve_events_globally` is a global option.
- `-sample_clock_mode <bool>`: `-sample_clock_mode` is a global option.
- `-start_in_back_to_back <bool>`: start in back to back.
- `-streaming_is_default <bool>`: streaming is default.
- `-support_dollar_display <bool>`: support `$DISPLAY`.
- `-task_streaming_is_default <bool>`: `task_streaming_is_default`.
- `-timestamp <bool>`: `-timestamp` can be used with or without `-module`.

- `-transform_latch <bool>`: `transform_latch`.
- `-treat_warnings_as_errors <bool>`: `-treat_warnings_as_errors` is a global option.

Constraint(s)

- `-emit_initial` can only be used with -module
- global options cannot be combined with `-instance|-module` options
- `-advanced_synth_command_file` can only be used with `-module`
- check for mandatory combinations of options
- `-advanced_synth_command_file` cannot be used with any of the following options: `-instance`
- -instance cannot be used with any of the following options:
  - `-allow_streaming`
  - `-start_in_back_to_back`
  - `-support_dollar_display`
  - `-reduce_control_paths`
  - `-do_profiling`
  - `-streaming_is_default`
  - `-task_streaming_is_default`
  - `-emit_initial`
  - `-hard_max_out_port_width`
  - `-hard_max_in_port_width`
  - `-auto_flush_interval`
  - `-buffered_out_ports_disable`
  - `-buffered_out_ports_default_width`
  - `-buffered_out_ports_regardless`
  - `-port_optimization_mode`

- -profile_counters_width
- -max_out_port_width
- -max_in_port_width
- -port_width_slop_percent
- -all_tf_args_are_automatic
- -external_controlled_clocks
- -allow_mixed_design_clocks
- -exports_excluded_from_back_to_back
- -max_loop_iterations
- -max_clocked_loop_iterations
- -merge_multiple_comb_writers
- -transform_latch
- -debug_zemi_behav
- -default_cclk
- -sample_clock_mode
- -timestamp
- -protolink
- -sample_clock_opt
- -rt_diag
- -rt_config
- -resolve_events_globally
- -async_reset_init
- -optimize_dpi_constant_args
- -treat_warnings_as_errors

- -sample_clock_mode cannot be used with any of the following options: -sample_clock_opt

At least one of the options should be used

Note(s)

- `-advanced_synth_command_file` must be used with `-module`, and should not be used with `-instance`
- Usage for the `-instance` option:

  `-instance` is only valid with `-debug|-edge_enable|-disable`, other options cannot be used with `-instance`
- `-default_cclk </tt>` can be used either with `-module` in which case it refers to specific modules, or without -module in which case it refers to all transactors defined until now.