SYNOPSYS®

DesignWare® Cores MIPI D-PHY v1.2 Tx 4L for TSMC 12-nm FFC/1.8V

Databook

dwc_mipi_d_t4_tsmc12ffc18ns – Product Code: C426-0

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7.03a	October 2019	Updated: ■ Chapter 3.2.1, “Features” ■ Table 9-1
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–	March 2017	First databook version

Preface

The Synopsys DesignWare® Cores (DWC) IP portfolio includes the DWC MIPI D-PHY v1.2 Tx 4L—Synopsys's Mobile Industry Processor Interface (MIPI) physical layer IP. The DWC MIPI D-PHY v1.2 Tx 4L macro implements the physical layer of the MIPI D-PHY interface. The DWC MIPI D-PHY v1.2 Tx 4L is a reusable IP solution for both DSI host and CSI2 device applications, targeted at the TSMC 12-nm FFC/1.8V fabrication process.

This document describes the DWC MIPI D-PHY v1.2 Tx 4L.

Databook Organization

This databook is organized as follows:

- Chapter 1, "Product Overview", provides an introduction to the DWC MIPI D-PHY v1.2 Tx 4L and its features.
- Chapter 2, "Deliverables", describes the DWC MIPI D-PHY v1.2 Tx 4L deliverables database for a full-package release.
- Chapter 3, "Add-on Macros", describes the analog IO ring and PLL for D-PHY applications using four TX data lanes.
- Chapter 4, "Functional Description", provides a functional overview of the DWC MIPI D-PHY v1.2 Tx 4L and describes its various operating modes.
- Chapter 5, "System-Level Implementation", provides the methodology of IP integration in System-on a chip (SoC).
- Chapter 6, "Characterization and Production Tests", describes the subset of features that can be used during characterization stage and production testing.
- Chapter 7, "Physical-Level Implementation", describes general guidelines regarding the IP physical integration.
- Chapter 8, "Board- and Package-Level Implementation", provides general recommendations for the PCB layout common to most high-speed digital communication environments.
- Chapter 9, "Process-Specific Specifications", provides the specifications that are specific to the fabrication process.
- Appendix A, "Timing Diagrams", shows some important timing diagrams.

Web Resources

- DesignWare IP product information: https://www.synopsys.com/designware-ip.html
- Your custom DesignWare IP page: https://www.synopsys.com/dw/mydesignware.php
- Documentation through SolvNetPlus: https://solvnetplus.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

Reference Documentation

- MIPI Alliance Specification for D-PHY Version 1.2
- MIPI Alliance Test Program, D-PHY Physical Layer Conformance Test Suite Version v1.2 CTS version 1.0
- DesignWare® Cores MIPI D-PHY v1.2 Tx 4L for TSMC 12-nm FFC/1.8V Reference Manual Version 7.07a

STAR on the Web (SotW)

You must review all STARs on the Web (SotWs) associated with your product. SotWs are considered a part of the Synopsys documentation suite, and show critical information related to your product. To review product SotWs, refer to the DesignWare IP product information:

https://www.synopsys.com/designware-ip.html

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- **Product L2:** DWC MIPI D-PHY v1.2 Tx 4L

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  - Include the Product L1 and Product L2 names, process, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
- Or, telephone your local support center:
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  - All other countries:

    http://www.synopsys.com/support/global-support-centers.html

1 Product Overview

This chapter includes the following sections:

1.1 Quick Reference

This section provides the most relevant details of the DesignWare Cores DWC MIPI D-PHY v1.2 Tx 4L (dwc_mipi_d_t4_tsmc12ffc18ns), which are provided along with other details throughout this databook.

Features	
Flexible configuration clock - 17 MHz to 27MHz Lane operation ranging from 80 Mbps to 2.5 Gbps in forward direction Aggregate throughput up to 10 Gbps with four data lanes Attachable PLL clock multiplication unit for High-Speed operation 50% DDR output clock duty-cycle Maximum LP data rate supported of 10Mbps PHY-Protocol Interface (PPI) for clock and data lanes Low-power Escape modes and Ultra Low Power state Programmable HS Amplitude Levels HS Slew Rate Control External Reference Resistor (200 ohm) Internal Pattern Generator Intra- and Inter-PHY testability Analog Test Bus Internal ADC digital voltage sensing	For more a full set of features for this PHY, see "Features" on page 24

PHY Macro Size	PLL Macro Size	Process Technology
450 x 504.96 µm (0.23 mm^2)	190 x 293.136 µm (0.056 mm^2)	TSMC 12-nm FFC/1.8V

Metal Stacks Supported	Junction Temperature	External Resistor
11M_2Xa1Xd_h_3Xe_vhv_2Y2R 9M_2Xa1Xd_h_3Xe_vhv_2Z	-40° C through 125° C	200 ohm (+-1%)

Power Supplies	Minimum ESD/LU Protection Levels
Analog High Voltage (vph) 1.8 V (+10%,-7%) **Analog Low Voltage (vp)** 0.8 V (+10%, -7%) **Analog Low Voltage for PLL (vpl)** 0.8 V (+10%, -7%) **Digital Supply Voltage (vdd)** 0.8 V (+10%,-7%) Specifications for the IP only (not at chip level). The supply range includes supply variation, noise, and IR drops.	**CDM** = 6A (500V or 250V to meet 6A peak current) **HBM** = 2 kV **LU:** +-100mA Level A

Specifications
MIPI Alliance Specification for D-PHY Version 1.2 MIPI Alliance Test Program, D-PHY Physical Layer Conformance Test Suite Version v1.2 CTS version 1.0

1.2 General Product Description

The DesignWare Cores MIPI D-PHY TX 4-Lane macro for TSMC 12-nm FFC/1.8V (referred to as PHY) implements the physical layer of TX universal lanes for the MIPI D-PHY interface. The PHY is stacked in a configuration with four data lanes and one clock lane. Lane 0 is unidirectional for HS support and is bidirectional for Escape modes (LPDT, Trigger, ULPS) and Turnaround and lanes 1 to 3 are unidirectional supporting HS and TX Escape modes (LPDT, Trigger, ULPS). Clocklane is unidirectional supporting HS and ULPS.

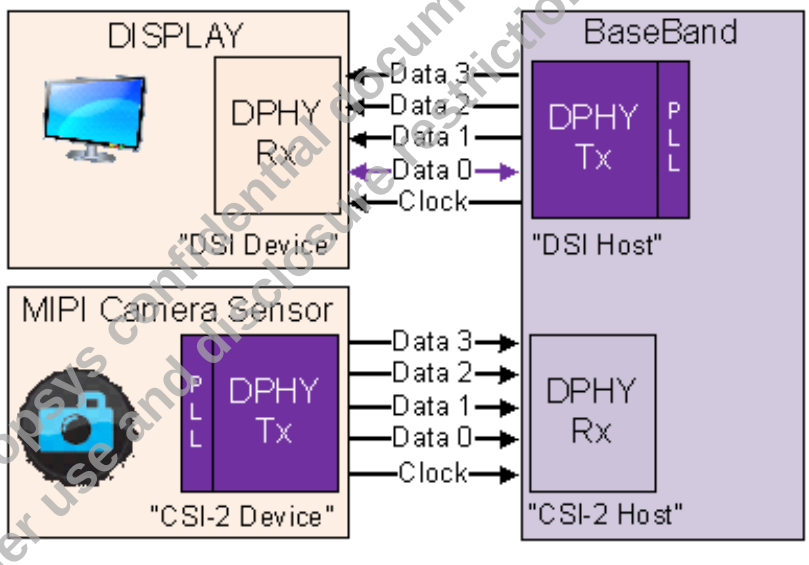
The PHY can be used for both DSI host and CSI-2 device applications.

The PHY also includes a clock multiplier PLL for high-speed (HS) clock generation. The PHY is targeted for high-speed data digital transmission between a host processor and display drivers or camera interfaces supporting a maximum effective bit rate of 2.5 Gbps per lane. The assembled four-data-lane system enables up to 10 Gbps aggregate communication throughput, delivering the bandwidth needed for high-throughput data transfer.

There is an additional reduced-throughput, low-power data transfer mode in each differential pair, which reduces line count and minimizes cable wires and EMI shielding requirements.

Figure 1-1 shows a typical application for the PHY.

Figure 1-1 Typical Application for DWC MIPI D-PHY v1.2 Tx 4L



1.3 Standards Compliance

The PHY is conformant with the MIPI D-PHY interface specification, revision 1.2 and backwards compatible with previous D-PHY specification version 1.1.

1.4 Features

The PHY has the following features:

- Flexible configuration clock - 17 MHz to 27 MHz
- Lane operation ranging from 80 Mbps to 2.5 Gbps in forward direction
- Aggregate throughput up to 10 Gbps with four data lanes
- Attachable PLL clock multiplication unit for High-Speed operation
- 50% DDR output clock duty-cycle
- Maximum LP data rate supported of 10 Mbps
- PHY-Protocol Interface (PPI) for clock and data lanes
- Low-power Escape modes and Ultra Low Power state
- Programmable HS Amplitude Levels
- HS Slew Rate Control
- External Reference Resistor (200 Ω)
- Internal Pattern Generator
- Intra-PHY testability
  - LP/ULPS External Loopback
  - I/O Continuity Test Support
- Inter-PHY testability
  - PHY-2-PHY High Speed Checker
  - PHY-2-PHY High Speed Loopback
  - PHY-2-PHY LP/ULPS External Loopback
- Analog Test Bus
- Internal ADC for digital voltage sensing
- Power Collapsing
- 1.8 V (+10%,-7%) analog high voltage supply operation (vph)
- 0.8 V (+10%,-7%) analog low-voltage analog supply operation (vp)
- 0.8 V (+10%,-7%) digital voltage supply operation (vdd)
- Core Area (including IOs/ESD and add-on PLL): 0.283 mm^2
- Power consumption:
  - HS TX @ 1G5: 28 mW
  - HS TX @ 2G5: 29 mW

1.5 Metal Stacks

The following table lists the library metal stack options provided with the PHY. Contact your sales representative if your metal stack option is not listed.

Table 1-1 Metal Stack Options

Metal Stack	Top Metal in IO Cells
11M_2Xa1Xd_h_3Xe_vhv_2Y2R	11
9M_2Xa1Xd_h_3Xe_vhv_2Z	9

1.6 ESD/ LU Specifications

Table 1-2 shows ESD specifications of the PHY.

Table 1-2 ESD/LU Specifications

Parameter	Condition	Minimum
HBM	In accordance with JS-001-2014	2 kV
CDM[a]	In accordance with JESD22-C101F, Class C2/C1 (500V / 250V)	6A (500V or 250V to meet 6A peak current) peak discharge current
LU	In accordance with JEDEC-JESD78D, Class II (125 degrees Celsius)	+-100mA - Level A

a. Support for both 250V or 500V CDM target level is dependent on max discharge current generated in final SOC/package implementation.

Note Analog IO pads do not support vph (1.8 V rail) power collapsing in case DP/DN are seeing high voltage. Higher leakage current is expected if vph rail is grounded and high voltage is forced on the dp/dn lanes.

1.7 Devices List

The following table lists the primitive devices used by the IP.

Table 1-3 Device List

Device	Description
nch_18_mac	I/O 1.8V VT NMOS
nch_18ud12_mac	Thick Oxide UnderDrive 1.2V NMOS
nch_lvt_mac	CORE Low VT NMOS
nch_ulvt_mac	CORE Ultra Low VT NMOS
ndio_gated18_mac	2T IO 1.8V gated N+/PW DIODE
ndio_hia18_mac	CORE 2T ESD diode N+/PW
ndio_mac	N+/PW Junction DIODE
nmoscap_18	1.8V MOSCAP Varactor
pch_18_mac	I/O 1.8V VT PMOS
pch_lvt_mac	CORE Low VT PMOS
pch_ulvt_mac	CORE Ultra Low VT PMOS
pdio_gated18_mac	2T IO 1.8V gated P+/NW DIODE
pdio_hia18_mac	CORE 2T ESD diode P+/NW
pnp_i2_mac	Cascade PNP (P+/NW/Psub)
rhim_m	P+ Poly Non-Salicided resistor 3T
rm11w	M11 resistor (for 11m only)
rm1w	M1 resistor
rm2w	M2 resistor
rm3w	M3 resistor
rm4w	M4 resistor
rm9w	M9 resistor (for 9m only)

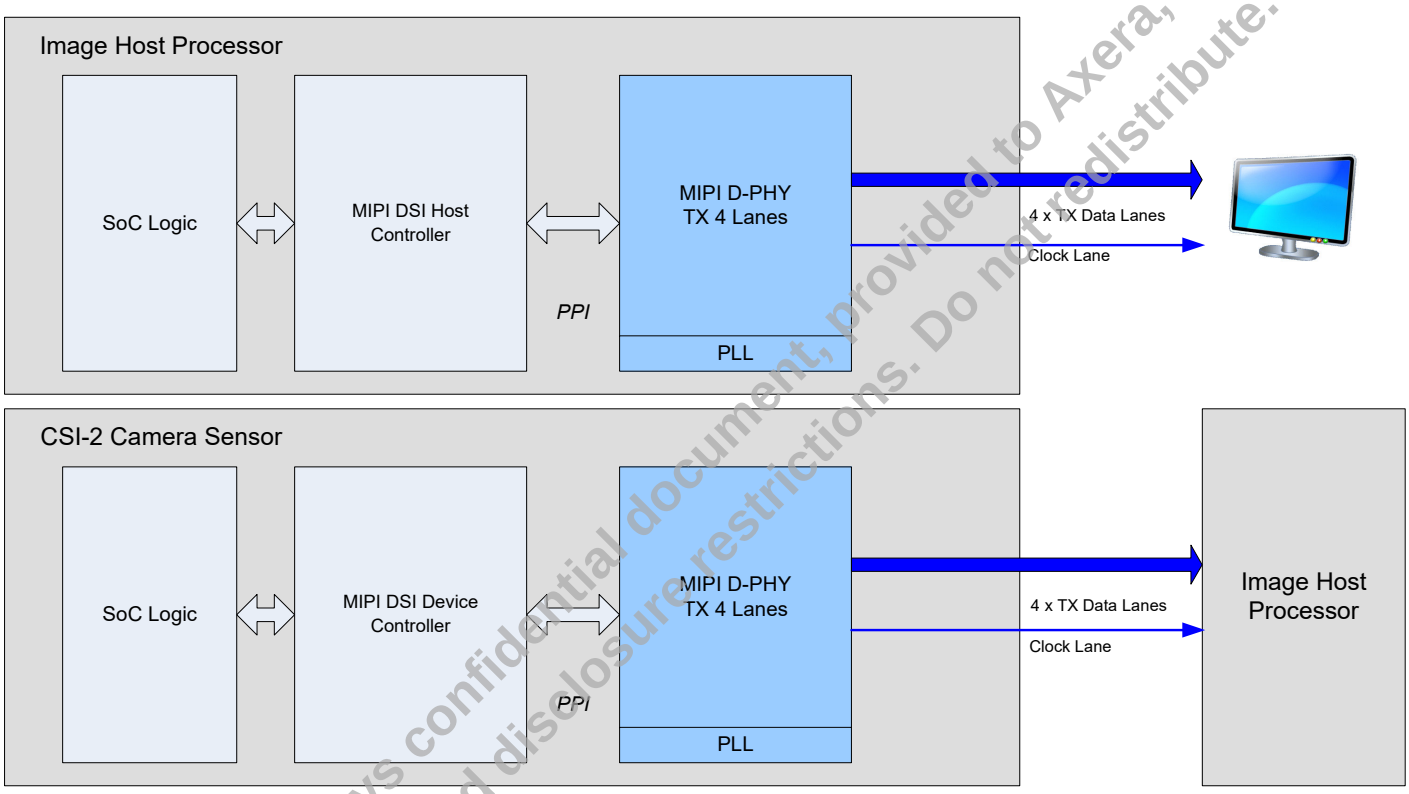
1.8 System-Level Overview

The PHY is the physical layer of a DSI host and a CSI-2 device. This section provides a system-level overview of the PHY. For a functional block diagram and a detailed description of the PHY see "Functional Description" on page 55.

1.8.1 System-Level Block Diagram

Figure 1-2 shows a system-level block diagram of the PHY.

Figure 1-2 DWC MIPI D-PHY v1.2 Tx 4L System-Level Block Diagram



The PHY interfaces with a CSI-2 device or DSI Host controller. A CSI-2 device or DSI Host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 or DSI specifications. This provides an interface between the system and the PHY, allowing the communication with a conformant MIPI Display host processor. The I/O block is responsible for interfacing with the analog physical world. An add-on PLL is used to support High-Speed modes of operation.

For additional information regarding the IO add-on connection block refer to "Add-on Macros" on page 33.

1.8.2 Interfaces

The PHY features both inter-chip and intra-chip interfaces.

- Inter-chip interface – relies on four data lanes and one clock lane.
- Intra-chip interface – defined between the PHY and the higher protocol layers of a communication stack and comprises parallel TX data. This interface complies with the informative Logical PHY-Protocol Interface (PPI) description in Annex A of the D-PHY specification.

1.9 MIPI D-PHY not Used

When the MIPI D-PHY macro is not used on the SoC, clock and data lanes and rext should be grounded or left floating and not bonded out.

- The MIPI D-PHY power supplies should be disconnected and grounded.

2 Deliverables

This chapter describes the standard IP deliverables.

This chapter is divided in the following sections:

2.1 Introduction

The IP is composed by a top-level verilog wrapper shell that instantiates a soft-core portion (represented on the product deliverables by synthesizable RTL and supported with synthesis constraints for its physical implementation) and a hard-macro portion that corresponds to a hard mixed-signal block.

This IP release delivers all views and information necessary to:

- Integrate the IP in the SoC;
- Perform simulations at different levels, from system functional verification to Signal Integrity analysis;
- Enable production tests.

The readme_<*version*>.txt file available in the top-level folder contains additional information about the release.

The deliverables are grouped in the following categories:

- Front-End views which are used for system simulations and floorplanning
- Back-End views which are used for physical design
- Signal Integrity views which are used for analog simulations and performance analysis

For more details about release contents, refer to the "Contents" section of the readme file.

2.2 Front-end Views

Front-end views are provided for the IP, I/Os and PLL add-on. The following Front-End views are provided where applicable for each of the mentioned cells in this full-package release:

- DesignWare Cores MIPI D-PHY v1.2 Tx 4L for TSMC 12-nm FFC/1.8V Databook
- Verilog for top-level instantiation
- Generic technology (GTECH) netlists and models for functional simulations
- Synthesizable soft core RTL
- IP soft macro Synopsys Design Constraints files for Synthesis
- Digital simulation environment
- Liberty timing files in .db and .lib formats
- Library Exchange Format (LEF) file with pin sizes and locations
- QuickStart simulation environment with Testbench examples
- CTL test model

2.3 Back-end Views

Back-End views are provided for the IP, I/Os and PLL add-on and are specific for each metal stack. The following Back-end views are provided where applicable for each of the mentioned cells in this full-package release:

- GDSII layout and layer map files
- Circuit Design Language (CDL) netlist and Layout Versus Schematic (LVS) reports
- Design Rule Check (DRC) reports
- Gate-level Verilog netlist for functional and scan simulations
- Standard Delay Format (SDF) files
- Scan test environment with Automatic Test Pattern Generation (ATPG)

2.4 Signal and Power Integrity Views

The following signal integrity views are related with this full package release:

- IBIS models for signal integrity simulations.
- Current waveforms, along with on-die power grid equivalent capacitance and resistance (Cdie and Rdie, respectively) for power delivery network simulations in the package.

3 Add-on Macros

This chapter describes the Designware PLL and the support IO add-on connection blocks for Flip-Chip integrations for D-PHY applications using four data lanes. It is divided in the following topics:

3.1 Overview

The MIPI D-PHY TX macro is supported by an add-on PLL block to support the High-Speed operation and by IO add-on connection blocks to support Flip-Chip integrations.

These add-on blocks, when used, connect to the MIPI D-PHY macro by physical abutment.

For more details on the IO pads, see "IO Pads and Connection Add-on Blocks" on page 34

For more details on the add-on PLL block, see "DesignWare PLL" on page 35.

3.2 IO Pads and Connection Add-on Blocks

IO pads and ESD protections are embedded within the MIPI D-PHY Tx macro.

The provided support add-on connection blocks correspond to physical connections from the embedded IO pads to the bumps for FlipChip applications. These add-on connection blocks are provided for maximum performance for the overall PHY system. These blocks connect to the MIPI D-PHY macro by physical abutment ensuring maximum performance while keeping integration requirements to a minimum.

3.2.1 Features

The embedded analog IO ring has the following features:

- Complete analog IO ring for the PHY with four lanes (embedded within the IP macro)
- FlipChip (FC) Support through add-on connection block:
  - 153.5 (inline) µm bump pitch
  - 81.6 (UBM) µm bump opening
- Low leakage
- Power Collapsing
- Primary ESD protection
- Latch-up immunity
- Abutment connection to the MIPI D-PHY macro
- 1.8 V (+10%,-7%) analog high voltage supply operation (vph)
- 0.8 V (+10%,-7%) analog low voltage supply operation (vp)

3.3 DesignWare PLL

3.3.1 DesignWare PLL Overview

The MIPI D-PHY is used in applications where the lane bit-rate requirements can change from system to system. To support this, the add-on PLL features a flexible clock-multiplying architecture. This clock-multiplying PLL cell uses a VCO comprised of a pseudo-differential oscillator ring. The VCO output frequency is divided by a programmable counter before being compared to input reference frequency (recommended is a crystal based for cleaner clock reference) input reference frequency by means of a three-state phase-frequency detector (PFD) with no dead-zone. The digital PFD commands a charge-pump, which in turn delivers a charge to the loop filter or, alternatively, extracts a charge from the filter.

The MIPI D-PHY add-on PLL generates quadrature clocks clkout0, clkout90, clkout180 and clkout270 to support the D-PHY macro operation.

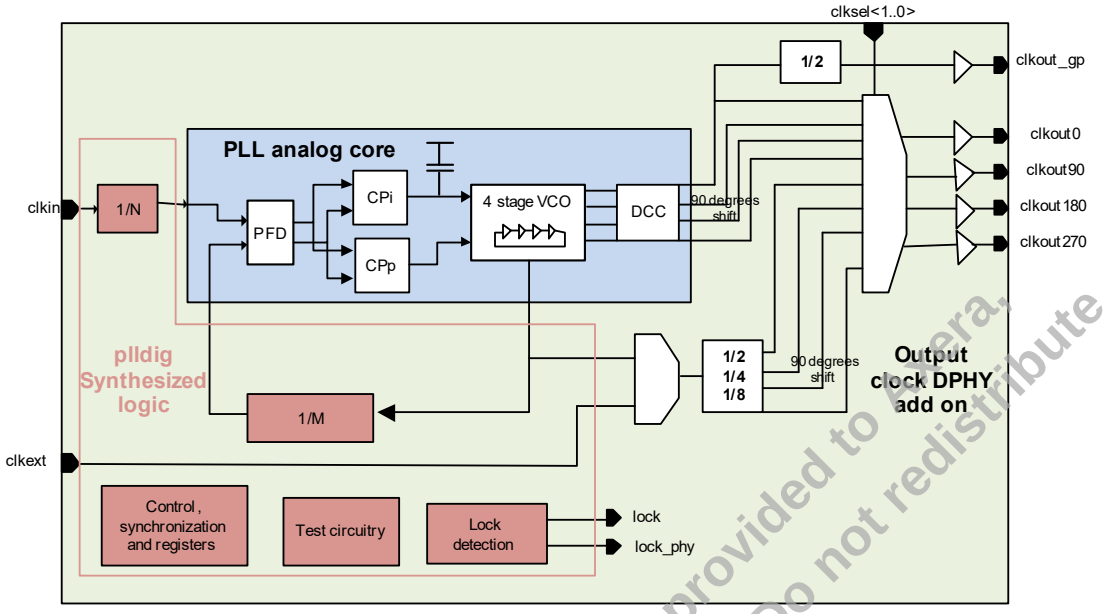
To properly configure the PLL for the desired frequency operation, refer to the relation between PLL output clock phases and the D-PHY data rate. The data rate is given by the double of the PLL output clock phases frequency: Data rate (Gbps) = PLL Fout (GHz) * 2, for example, for 2 Gbps operating frequency, VCO output frequency is 1 GHz. For the correct PLL Fout configuration, refer to PLL requirements and configuration below.

The add-on PLL block can be configured through the PLL owner D-PHY or through its dedicated SoC configuration interface. All PLL configurations for the desired operating frequency need to be done before D-PHY Start-up.

Note Before each D-PHY Start-up, the PLL needs to be properly configured for the desired operation frequency. All PLL related configuration settings should be reviewed and set.

Figure 3-1 shows a functional diagram of the PLL system.

Figure 3-1 PLL Functional Diagram



3.3.2 Features

The DesignWare PLL macro has the following features:

- Flexible clock-multiplying PLL architecture
- Flexible input clock reference - 2 MHz to 64 MHz
- VCO oscillating range - 320 to 1250 MHz
- Output frequency range - 40 to 1250MHz
- Power Collapsing
- Abutment connection to MIPI D-PHY macro
- Capability of sharing high-speed output clock signals with multiple MIPI D-PHY instances
- Analog Test Bus
- Agile Clocking and Direct SoC Control/Observability
- Low-power bypass mode
- 1.8 V +10%,-7% analog high voltage supply operation (vph)
- 0.8 V +10%,-7% analog low voltage supply operation (vpl)
- 0.8 V +10%,-7% digital supply operation (vdd)
- Area: 0.056 mm2

3.3.3 Process-Specific Specifications

Table 3-1 lists parameter specifications for input and output signals.PLL Signals

Table 3-1 Parameter Specifications for PLL Input and Output Signals

Parameter	Condition	MIN	TYP	MAX	Unit
Output Frequency Multiplication Ratio (M)	(feedback multiplication)	40		625[1]	
Input Reference Frequency Division Ratio (N)	(pre division)	1	12	16	
Loop Comparison Frequency	Fref	4		19.2	MHz
Input Reference Clock Frequency	Fclkin	2	19.2	64	MHz
Input Reference Clock Duty Cycle	DCclkin	30		70	%
Input Reference Clock phase noise	> 1MHz offset	-130			dBC/Hz
Bypass Input Clock Frequency	clkext input	320		1250	MHz
Bypass Input Clock Duty Cycle	for vco_cntrl[5:4]=000 Fout=Fin/2	48		52	%
	for vco_cntrl[5:4]=001 Fout=Fin/4	35		65	%
Bypass Input Clock Period Jitter				0.1	UI
updatePLL pulse width		4			Input clock periods
shadow_clear pulse width		5			ns
Tsetup for updatePLL		5			ns
VCO oscillating frequency	fVCO – frequency range	320		1250	MHz
Output Clock Frequency		40		1250	MHz
Orthogonal signal skew		-3.75		3.75	%T
Orthogonal signal skew	Fout = 1250 MHz	-30		30	ps

1)For 2MHz internal comparison frequency

2)The int_cntrl, prop_cntrl, vco_cntrl, p, gmp_cntrl, m and n SOC signals have to be stable "Tsetup for update PLL" before updatePLL signal being asserted

3)Within the frequency limits shown, the VCO frequency is the result of a multiplication of the input reference frequency by M/N

Table 3-1 Parameter Specifications for PLL Input and Output Signals

Parameter	Condition	MIN	TYP	MAX	Unit
Output Clock Duty Cycle		-3.75		3.75	%
Output Clock period Jitter	0.5 GHz<Fout<=1.25 GHz			0.1	UI
Output Clock period Jitter	Fout <= 0.5 GHz			0.2	UI
Lock Time				150	?s
Relock Time	Maximum frequency change: 5%			40	?s
T_clksel2out_off	Time to power down output clocks	1.6		100	ns
T_clksel2out_on	Time to power up output clocks	1.6		100	ns
T_clksel_off, T_off	Minimum time of power down on output clocks	T_clksel2out_off		inf	ns

1)For 2MHz internal comparison frequency

2)The int_cntrl, prop_cntrl, vco_cntrl, p, gmp_cntrl, m and n SOC signals have to be stable "Tsetup for update PLL" before updatePLL signal being asserted

3)Within the frequency limits shown, the VCO frequency is the result of a multiplication of the input reference frequency by M/N

The following tables provide pin descriptions for the DesignWare PLL signals. In addition to describing the function of each signal, the signal descriptions include the following information:

- **Voltage range:** Describes the voltage range expected on this pin.
- **Synchronous:** Indicates that the signal is asserted or de-asserted with respect to a clock edge.
- **Asynchronous:** Indicates that the signal is not asserted or de-asserted with respect to a clock edge.

All digital signals are active high unless stated otherwise.

The PLL related digital signals are separated below in the group of signals that connect to the main D-PHY macro that controls the PLL through the main D-PHY macro soft-core portion and in the group of signals that are available on the PLL interface for direct SoC control and observability. These signals that do not connect to the main D-PHY macro are also listed on section "PLL SoC Control and Observability" on page 53

The PLL related signals are separated below in the following groups of signals. For the PLL Signals Refer the MIPI D-PHY v1.2 Tx 4L for TSMC 12-nm FFC/1.8V *Reference Manual.*

- PLL Power Supply Signals
- PLL-PHY Hard-Macro Interface Signals
- PLL-PHY Soft-Macro Interface Signals
- PLL-SoC Interface Signals

3.3.4 PLL Modes of Operation

The clock-multiplying PLL cell has programmable features that enable you to select the operating mode. The control signals are not stored internally in the PLL. Therefore, any change in their logic value immediately alters the operation of the PLL. Ensure that the control signals remain stable during operation.

Table 3-2 summarizes the operating modes; details of each mode are discussed later in this section.

Table 3-2 PLL Modes of Operation

mpll_pwron	PLL
0	Not operating
1	Operating

By default, the PLL clock multiplier is switched off during shutdown and ULP operation. forcepll can be asserted maintaining the PLL active in all modes except shutdown.

The forcepll signal cannot be used to Start-up the PLL independent of the PHY state.

3.3.4.1 Power Down Mode

In power down mode (mpll_pwron = 0), the control voltage of the VCO is actively pulled high, forcing the VCO oscillation to stop. Also, the Charge Pump current is cut off. The reference clock (clkin) is also internally disabled, thus reducing the power dissipation to a minimal value.

It is recommended that during power down, reference clock is stopped and all control pins are kept a '0'.

This mode also behaves as a reset sequence for the PLL, forcing it to start its lock acquisition from a low output frequency.

3.3.4.2 Initialization

All supplies and input reference clock should be stable before PLL Start-up.

All PLL related configurations need to be reviewed and configured accurately prior D-PHY Start-up. This can be done through the D-PHY test and control interface or through the PLL SoC interface and its shadow registers.

The control over these signals can be done only while PLL is powered down or during agile clocking, being that during agile clocking transitions, only the PLL SoC configuration signals can be used.

Configuring the PLL operation through the D-PHY test and control interface

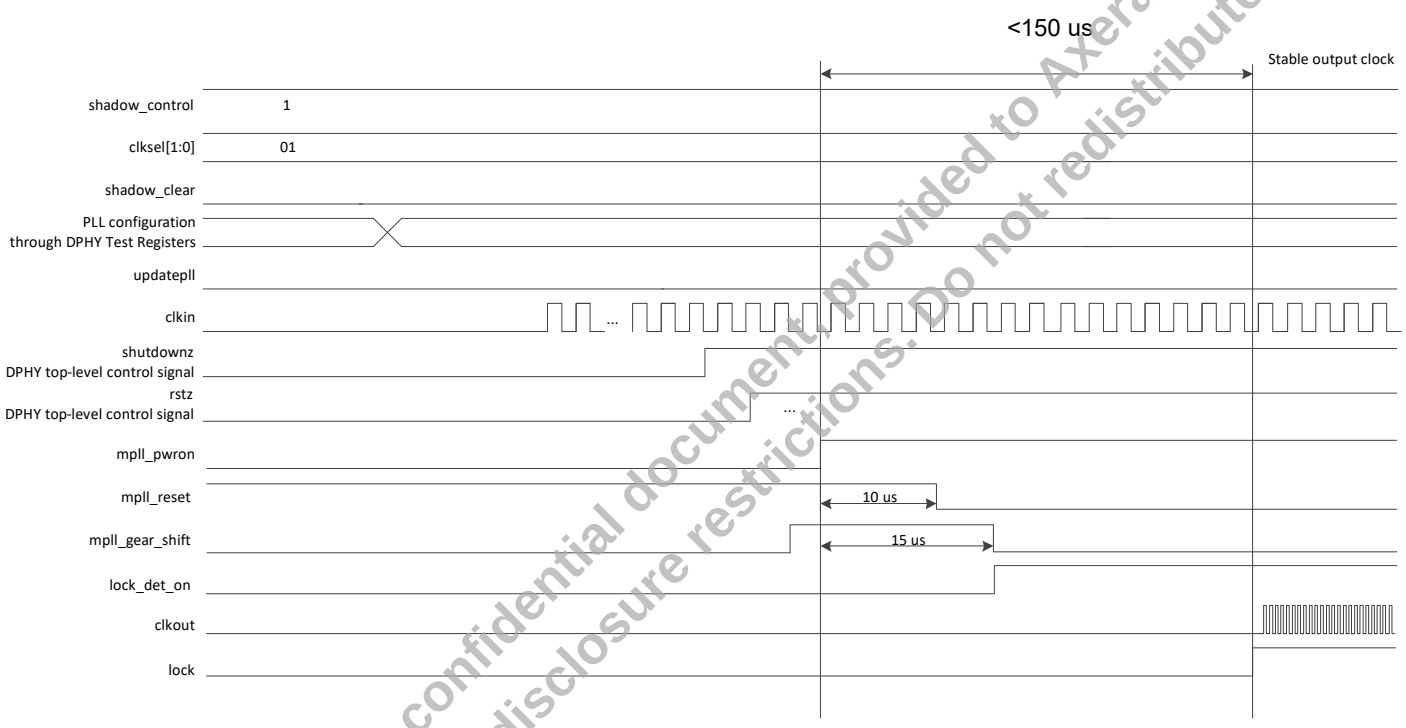
If the PLL operation is configured through the D-PHY test and control interface (pll_shadow_control =1), the following signals and respective test registers need to be reviewed and properly configured:

- m[9:0] - pll_m_ovr[9:0], pll_m_ovr_en – 0x18, 0x19
- n[3:0] - pll_n_ovr[3:0], pll_n_ovr_en – 0x17, 0x19
- vco_cntrl[5:0] - pll_vco_cntrl_ovr[5:0], pll_vco_cntrl_ovr_en – 0x12
- cpbias_cntrl[6:0] - pll_cpbias_cntrl[6:0] – 0x1c

- gmp_cntrl[1:0] - pll_gmp_cntrl[1:0] – 0x13
- int_cntrl[5:0] - pll_int_cntrl[5:0] – 0x0f
- prop_cntrl[5:0] - pll_prop_cntrl[5:0] – 0x0e

Figure 3-2 shows the first PLL configuration done through the PLL PHY Soft macro interface configuration signals and power-up when the PLL is controlled by the D-PHY macro that will enable it and start with the PLL power-up procedure.

Figure 3-2 Initialization Timing Diagram – PLL Configured by PLL PHY Soft Macro Interface



Note

- PLL shadow_control signal must be asserted
- Configuration of the PLL through the D-PHY test and control interface should be done with D-PHY in power-down
- The clk_sel[1:0] signal should be set to 2'b01 for the PLL to output the high-frequency clock needed for the D-PHY operation.

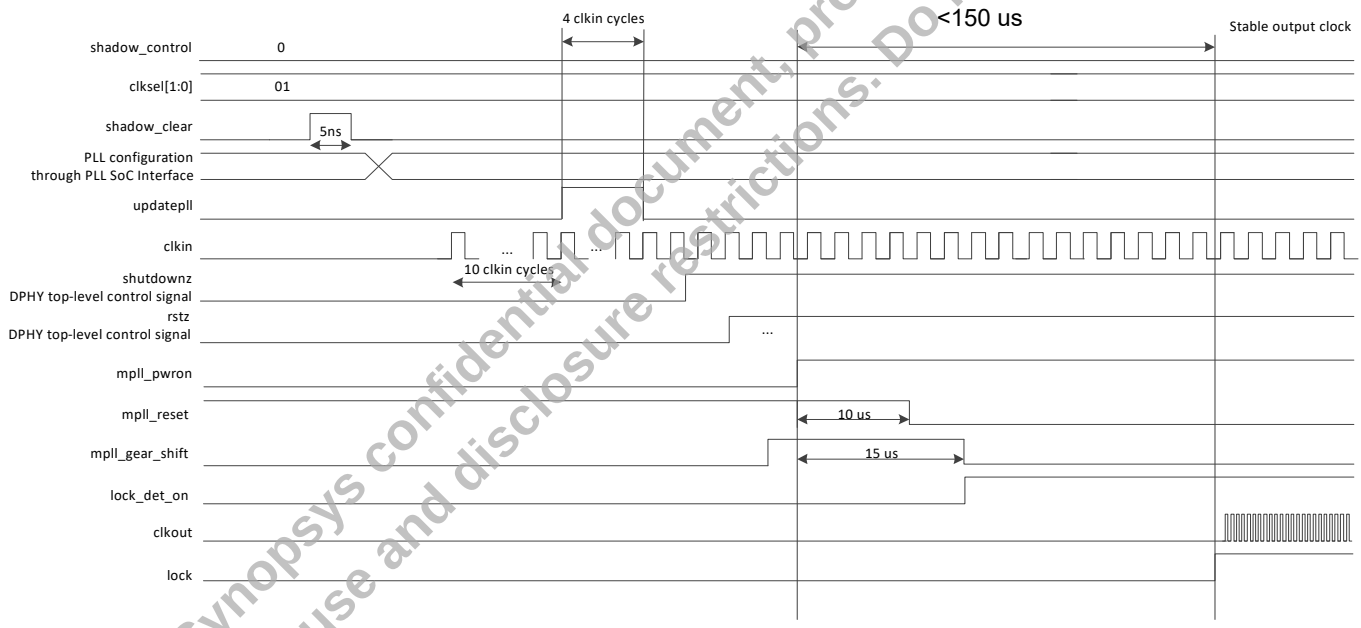
Configuring the PLL operation through the PLL SoC signals

If the PLL operation is configured through the PLL SoC signals through its shadow registers interface (pll_shadow_control =0), the following signals need to be reviewed and properly set:

- m[9:0]
- n[3:0]
- vco_cntrl[5:0]
- cpbias_cntrl[6:0]
- gmp_cntrl[1:0]
- int_cntrl[5:0]
- prop_cntrl[5:0]

Figure 3-3 diagram shows the first PLL configuration done through the PLL SoC signals and its shadow registers interface. The D-PHY macro, as part of its Start-up sequence (after shutdownz and rstz signals are de-asserted), will enable and power-up the PLL by controlling its power-up sequence directly (mpll_pwron, mpll_reset, mpll_gear_shift).

Figure 3-3 Initialization Timing Diagram – PLL Configured by PLL SoC



Note

- PLL shadow_control signal must be de-asserted
- A minimum pulse of 5ns on shadow_clear signal is required to set shadow registers to their reset default value. testclr D-PHY top-level control signal can be kept at 1. It has not relation to the shadow registers as these are on the PLL and are reset with shadow_clear.
- So before any PLL related configuration signal on the PLL SoC side is driven, shadow_clear should be pulsed.
- Input (N), feedback (M) dividers and other required PLL configurations should be set to appropriate values prior to initialization of PLL block.
- After setting all PLL configurations a pulse on updatepll is required to provide this configuration to shadow registers. updatepll signal should be asserted for a minimum of four clkin cycles
- The minimum delay between shadow_clear and updatePLL pulse is required to be 10 refclk cycles, meaning that at least 10 refclk cycles are required before updatePLL assertion.
- The clk_sel[1:0] signal should be set to 2'b01 for the PLL to output the high-frequency clock needed for the D-PHY operation.

PLL Lock Configuration

The following PLL lock related configurations should be set according to table PLL Lock Configurations before D-PHY power-up. This should be done through D-PHY test control registers.

Table 3-3 PLL Lock Configurations

Configuration Signal	Value	Test Register
pll_th1_rw[9:0]	10'h2	0x14
pll_th2_rw[7:0]	8'h60	0x15
pll_th3_rw[7:0]	8'h3	0x16
Default setting of lock_sel	1'b1	0x1D

3.3.4.3 Frequency Change

The architecture allows "on-the-fly" switching between generated frequencies being that the maximum allowed frequency change is 5%. The change occurs due to an update of *M* and *N* division factors, and it is triggered by a pulse on the updatepll signal.

The Agile clocking and relock mode cannot be exercised until PLL is locked on a generated frequency. Before updating PLL output selection to the updated generated frequency, it is required that PLL lock is asserted. On this context, during PLL relock, M and N configuration values cannot be uploaded through updatepll until lock is acquired and PLL is relocking.

A transition on the updatepll signal reads in values and, for a new configuration, another pulse of updatepll is required; refer to Figure 3-5. A minimum T_{setup} for updatepll is necessary in order to ensure that PLL input values are stable in shadow registers.

Figure 3-4 Relock with Output Clock Off

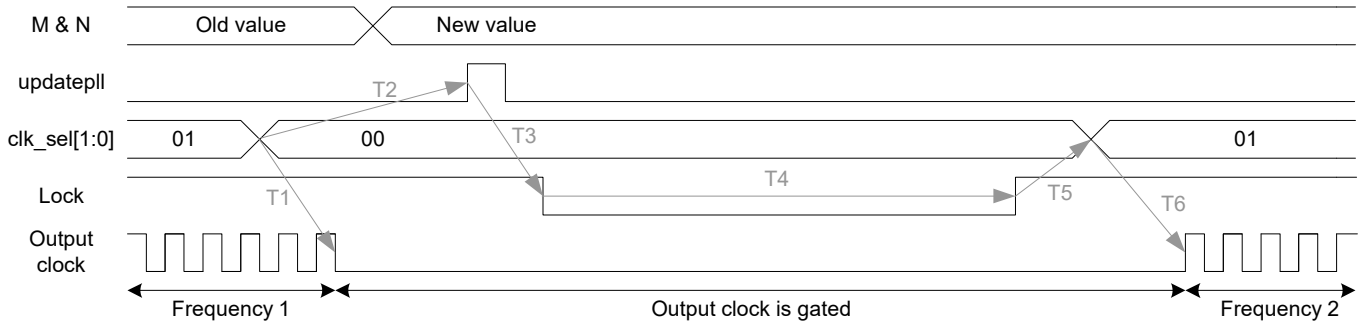
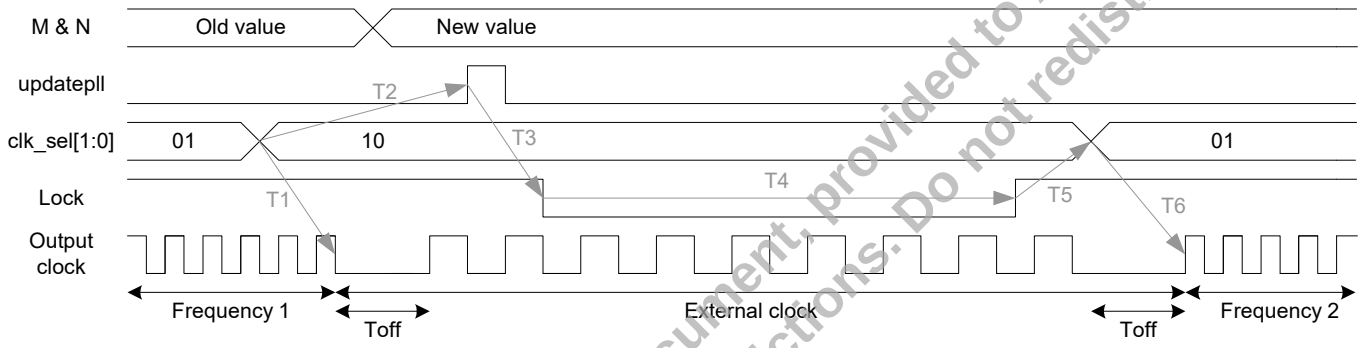


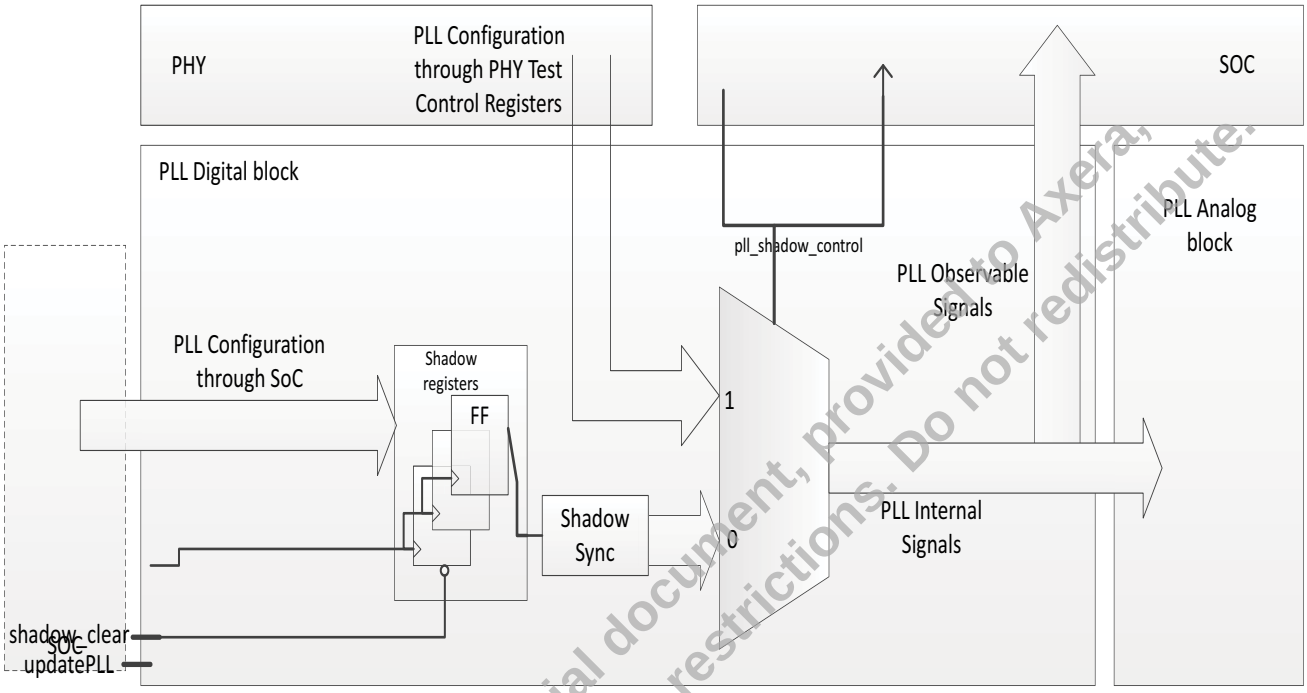
Figure 3-5 Output Clock Driven from External Source during Relock



- T1 — clksel[1:0] change to clock gated or external clock when PLL output clock for F1 is to be off
- T2 — updatepll assertion after clk_sel[1:0] assertion to gated or external clock → dependent on system specification and not on the PHY or PLL
- T3 — updatepll assertion to Lock de-assertion → maximum 3 clkin clock cycles ~125ns [150ns
- T4 — Lock de-assertion to Lock (relock) assertion → currently assuming th_delay = 24, ~32us+1.5us
- T5 — clksel[1:0] change after Lock assertion → dependent on system specification and not on the PHY or PLL
- T6 — clksel[1:0] change to clock stable when PLL starts to output clock for F2

Figure 3-6 on page 44 illustrates the two different approaches in which the PLL main control signals can be used to configure the PLL into the desired operating frequency and the dependency to shadow_control state.

Figure 3-6 PLL SoC Control and Observability



3.3.4.4 Change of Output Clock Source with clksel[1:0]

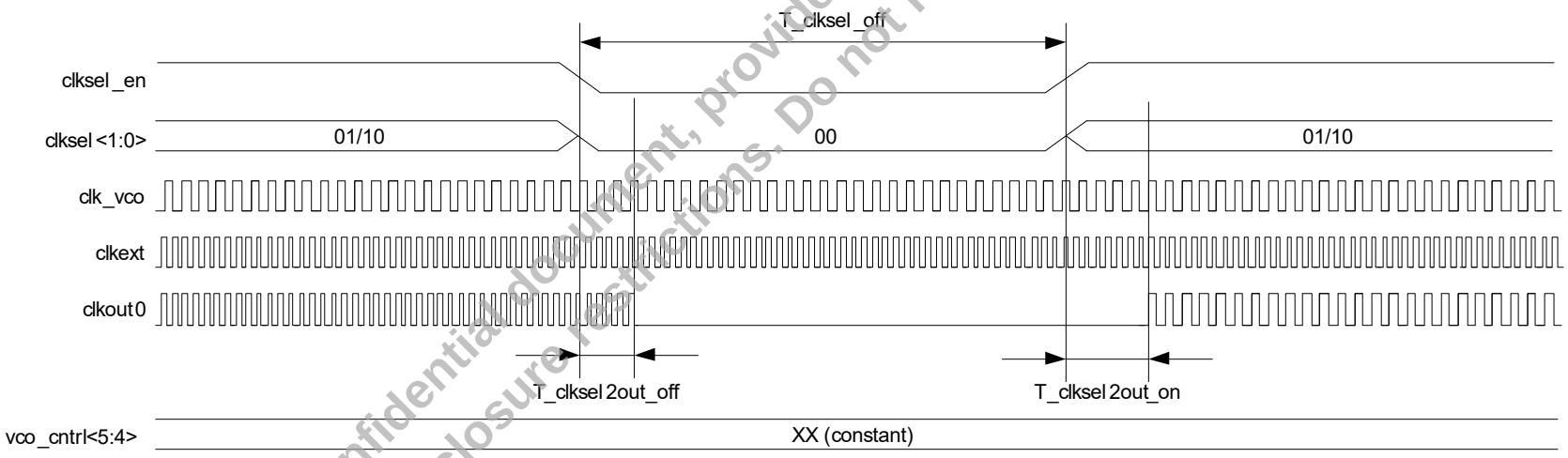
The restriction below is applicable to PLL operating frequencies below 320MHz (640Mbps datarate). In order to change the source of output frequency, as shown in Figure 3-7, you need to:

1. Set clksel[1:0] to “00” or clksel_en to “0”,
2. Wait T_clksel_off,
3. Set clksel[1:0] to “10” or “01”,
4. If clksel_en was set to “0”, then it has to be set to “1”.

clksel_en is internally bonded with clksel[1:0] signals. When clksel_en is set to “0”, clksel[1:0] signals are being forced to “00” internally. When clksel_en is set to “1”, then clksel[1:0] is not changed internally. clksel_en has similar functionality as clksel[1:0] and in some cases it can be treated as redundant signal.

Time T_clksel2out_off depend on vco frequency, external frequency and on output division factor set by vco_cntrl[5:4]. Value of T_clksel2out_off vary from 1.6 ns up to 100ns. Time T_clksel_off has to be longer than T_clksel2out_off, so it has to be at least 100ns long, or longer. The value of T_clksel2out_on varies from 1.6 ns up to 100ns.

Figure 3-7 Transitions and Timings needed to change clksel[1:0]

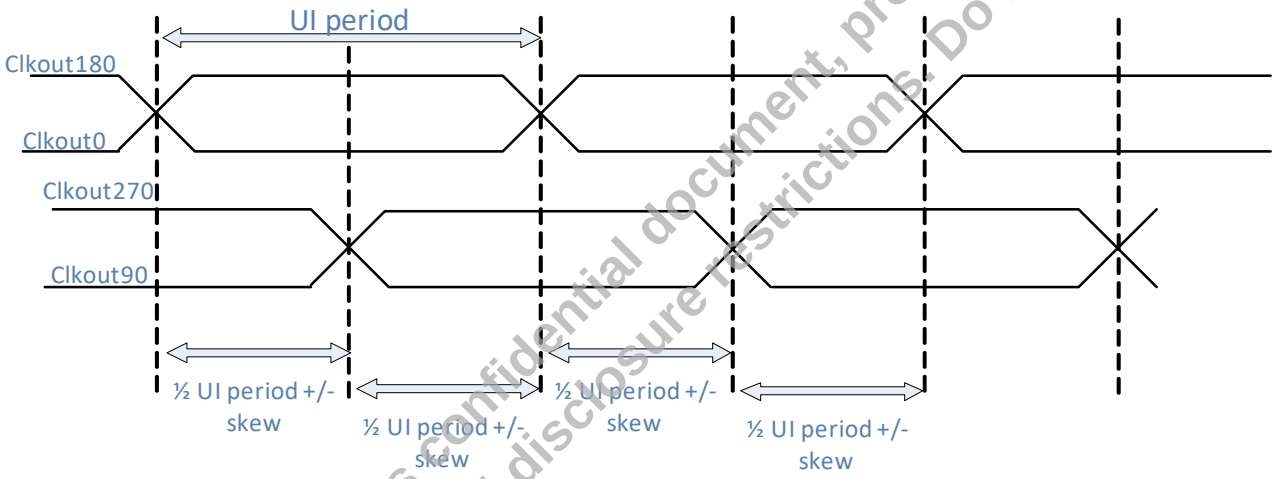


Output clocks starts always in following order: clkout0, clkout90, clkout180, clkout270. Output clocks stops always in following order: clkout0, clkout90, clkout180, clkout270.

3.3.4.5 Skew between Output Clocks

PLL generates quadrature clocks clkout0, clkout90, clkout180 and clkout270. Relation between clocks should pass orthogonal signal skew defined like on picture below

Figure 3-8 Skew between Output Clocks



3.3.4.6 Relock Counter Operation

During a frequency change, the lock changes its state to 0. It flags a lock after several microseconds that are programmed on the th_delay[5:0] counter. The conditions under which the PLL achieves a lock are:

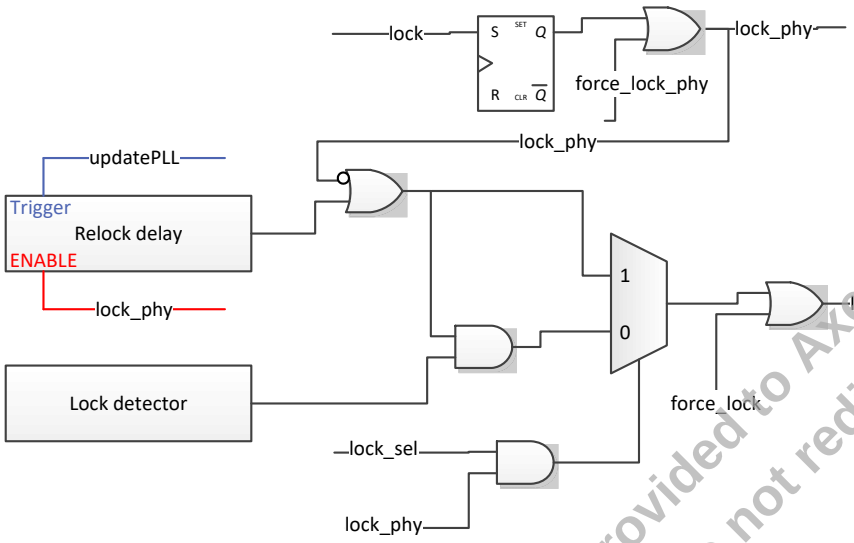
- *total_delay_min* = *clkin_period* * 32 *(*th_delay*[5:0])
- *total_delay_max* = *clkin_period* * 32 *(*th_delay*[5:0]+2)

During a relock phase, the lock signal changes to 1'b1 only when the internal lock detector flags the lock and relock delay counter flags; this is the default. It is possible to select the lock signal based only on the relock delay counter.

The lock_phy signal—the internal lock indicator for a PHY operation—stays at 1'b1 during a relock operation. The relock circuit is gated until the PLL receives the first lock through the lock detector circuit, after which the circuit is re-initialized whenever an updatepll is flagged.

Figure 3-9 illustrates the relock operations.

Figure 3-9 Relock Counter Operation



3.3.4.7 Digital Test Mode

The functionality of digital block can be confirmed is special digital test mode. By setting tstplldig properly it is possible to access certain signals through testlock output. Table 3-4 presents bit correspondence.

Table 3-4 Digital Test Mode Settings

tstplldig[2:0]	Observed on testlock
000	Lock signal—same as lock output
001	clkin—output of input *N* divider
010	fbclk—output of feedback *M* divider
011	int_clkin—clkin gated with onpll to save power
100	Lock signal from lock detector
101	Output from relock delay block
110	buf_vcoclk—VCO clock input of digital
111	updatepll signal

3.3.5 PLL Programmability

3.3.5.1 Output Frequency

The data rate is given by the double of the PLL output clock phases frequency: Data rate (Gbps) = PLL Fout (GHz) * 2

Output frequency is a function of the input reference frequency and of the multiplication/division ratios. It can be determined in the following way:

For:

$$1250\ \text{MHz} \geq f_{\text{out}} \geq 320\ \text{MHz}$$

$$f_{\text{out}} = f_{\text{vco}} = \frac{\text{M}}{\text{N}} \cdot f_{\text{clkin}}$$

Where:

- M – Feedback Multiplication Ratio
- N – Input Frequency Division Ratio

However, the following limits apply:

$$8\ \text{MHz} \geq \frac{f_{\text{clkin}}}{N} \geq 2\ \text{MHz}$$

$$1250\ \text{MHz} \geq f_{\text{vco}} \geq 320\ \text{MHz}$$

Output frequencies below 320MHz are obtained through division

For:

$$320\ \text{MHz} \geq f_{\text{out}} \geq 160\ \text{MHz}$$

$$f_{\text{out}} = \frac{f_{\text{vco}}}{2} = \frac{\text{M}}{2\text{N}} \cdot f_{\text{clkin}}$$

For:

$$160\ \text{MHz} \geq f_{\text{out}} \geq 80\ \text{MHz}$$

$$f_{out} = \frac{f_{vco}}{4} = \frac{1M}{4N} \cdot f_{clkin}$$

For:

$$80\ MHz \geq f_{out} \geq 40\ MHz$$

$$f_{out} = \frac{f_{vco}}{8} = \frac{1M}{8N} \cdot f_{clkin}$$

Table 3-5 shows corresponding selection bits for division ratios.

Table 3-5 Feedback Multiplication Ratio

Parameter	Description	M	m[9:0]
Minimum	Feedback multiplication ratio M=m+2	64	10'h3E
Maximum		625	10'h26F

Table 3-6 Input Divider

Parameter	Description	N	n[3:0]
Minimum	Input divider N=n+1	1	4'h0
Maximum		16	4'hF

3.3.5.2 Charge-pump Programmability

Current of the proportional charge pump

$$Iprop = Icp \times \frac{1 + xpropc}{2} \times \frac{8 - xcp_{progB}}{8 - 2 \times xcp_{progA}}$$

Current of the integral charge pump

$$Iint = Icp \times \frac{1 + xintc}{8} \times \frac{8 - xcp_{progB}}{8 - 2 \times xcp_{progA}}$$

Icp=Ivco/62

xpropc=prop_cntrl[4:0]

xintc=int_cntrl[3:0]

xcp_{progB}= cpbias_cntrl [4:2]

xcp_{progA}= cpbias_cntrl [1:0]

Table 3-7 Charge-pump Programmability

Output frequency [MHz]	vco_cntrl[5:0]	cpbias_cntrl[6:0]	gmp_cntrl[1:0]	int_cntrl[5:0]	prop_cntrl[5:0]
1150 – 1250	000001	0010000	01	000000	001110
1100 – 1152	000001	0010000	01	000000	001101
630 – 1149	000011	0010000	01	000000	001101
420 – 660	000111	0010000	01	000000	001101
320 – 440	001111	0010000	01	000000	001101
210 – 330	010111	0010000	01	000000	001101
160 – 220	011111	0010000	01	000000	001101
105 – 165	100111	0010000	01	000000	001101
80 – 110	101111	0010000	01	000000	001101
52.5 – 82.5	110111	0010000	01	000000	001101
40 – 55	111111	0010000	01	000000	001101

Note The PLL configurations need to always be reviewed and configured for the desired operating frequency before PLL power-up.

3.3.5.3 PLL Bypass

This clock-multiplying PLL can be bypassed according to Table 3-8. Glitch free architecture assures no glitches during switching between external and internal signals.

Table 3-8 PLL Bypass Settings

clksel[1:0]	clkout
00	Clocks stopped
01	Clock generation
10	Buffered clkext
11	Forbidden

D-PHY requires 4 clock phases generated by PLL. In bypass mode the phases are generated using internal divider. PLL output frequency will be 2/4/8 times slower than clkext input frequency. The division factor depends on vco_cntrl[5:4] settings.

Table 3-9 Division Factors based on vco_cntrl[5:4]

vco_cntrl[5:4]	clkout frequency
0x	Fin / 2
10	Fin / 4
11	Fin / 8

Changing vco_cntrl[5:4] dynamically without stopping output clocks or resetting PLL can generate a glitch on the output. This puts a constraint on usage of bypass functionality during relock depicted on figure 5. To generate expected bypass frequency one needs to apply on clkext 2, 4 or 8 times higher frequency (depending on vco_cntrl[5:4] setting).

Consider the following examples:

Example 1: Agile clocking transition from 1.5 Gbps (internal PLL) to 800 Mbps (clkext)

- Vco_cntrl[5:4] = 2'b00
- PLL output clock frequency = clkext/2
- Data rate = PLL output clock frequency * 2
- Data rate (Gbps) = clkext (GHz)
- clkext = 800MHz for 800Mbps data rate

Note Example 1 is valid for PLL configured to output frequency from 160MHz - 1.25GHz (320Mbps - 2.5Gbps)

Example 2: Agile clocking transition from 320 Mbps (internal PLL) to 200 Mbps (clkext)

- Vco_cntrl[5:4] = 2'b10
- PLL output clock frequency = clkext / 4
- Data rate = PLL output clock frequency * 2
- Data rate (Gbps) = clkext / 2 (GHz)
- clkext = 400MHz for 200Mbps data rate

Note

Example 2 is valid for PLL configured to output frequency from 80MHz - 160MHz (160Mbps - 320Mbps)

For PLL output frequency between 40MHz-80MHz (80Mbps - 160Mbps) the following relation is valid:

- PLL output clock frequency = clkext / 8
- Data rate = PLL output clock frequency * 2
- Data rate (Gbps) = clkext / 4 (GHz)

3.3.5.4 Low-power Bypass Mode

Bypass mode is operational during PLL power down. In this case output the frequency is twice as low as the input clkext, for example for 800Mbps data rate operation, you need to input a clkext frequency of 800Mhz for PLL output clocks frequency of 400MHz.

To operate on this mode, before D-PHY Start-up, set the following signals:

- clk_ext_mode_rw to 1'b1, register 0x0b
- pll_force_lock_rw to 1'b1, register 0x1d

3.3.5.5 M and N Synchronization

Since M and N signals can change when the PLL is on lock condition, it is necessary to ensure that the dividers correctly see the change requested. The updatepll signal is used to trigger the internal synchronization mechanisms (edge sensitive). The signals coming from the SOC are stored on a shadow register bank whenever a rise-edge is detected on updatepll. The updatepll signal is also used to trigger the internal synchronization mechanisms that are responsible for moving the signals from the shadow register to the destination clocks.

3.3.5.6 Lock Detector Setting

The PLL includes a lock detection circuit. Its threshold-triggering lock indicators are fully programmable for debugging. Default settings are static and do not change during normal operation.

- Signal th1[9..0] – controls allowed phase error defined by:

  $PHI_{ideal} = (2*th1/m)*360°$

  The feedback clock is sampled with a VCO/2 clock so that the phase relation for the first sampling only occurs approximately one cycle of the VCO/2 clock.

- Signal th2[7..0] – controls number of times that phase error is lower than th1; must be measured consecutively for lock to be asserted

Signal th3[7..0] – controls number of times that phase error is bigger than th1; must be measured consecutively for lock to be de-asserted

3.3.6 PLL SoC Control and Observability

The following signals are directly controlled and observable on the SoC through the PLL interface.

Table 3-10 Observable and Controllable Signals

Observable and controllable signals		
clkext	lock	scanin
clkout_gp	m[9:0]	scanluctrl
clksel[1:0]	m_obs[9:0]	scanmode
cpbias_cntrl[6:0]	n[3:0]	scanout
cpbias_cntrl_obs[6:0]	n_obs[3:0]	scanrstz
force_lock	pll_shadow_control	shadow_clear
gmp_cntrl[1:0]	pll_shadow_control_obs	updatepll
gmp_cntrl_obs[1:0]	prop_cntrl[5:0]	vco_cntrl[5:0]
gp_clk_en	prop_cntrl_obs[5:0]	vco_cntrl_obs[5:0]
int_cntrl[5:0]	scanclk	
int_cntrl_obs[5:0]	scanen	

3.3.7 PLL Scan Mode

3.3.7.1 Overview

The PLL provides a Scan interface for stuck-at fault scan testing.

Not all FF are on the scan chain as some belong to the vco clock domain.

An ATPG model of the digital portion of the PHY is provided that can be used during ATPG pattern generation to stitch the scan chains together and test them during chip-level scan testing. If scan in not being implemented in the PHY, tie all scan input pins to 1'b0 (scanclk, scanen, scanin, scanluctrl, scanmode).

3.3.7.2 Scan Modes

Before entering into scan mode, the PHY scan reset should be set. After some scan clock cycles, PHY should be set in scan mode and after some scan clock cycles, PHY scan reset should be released.

In Scan mode, all analog blocks are powered down, that is, power consumption of the analog blocks corresponds to only their respective leakage current.

To prevent propagation of logic X's in the scan chain, the outputs of all the analog blocks feeding the digital scannable logic are overridden to known states.

The PLL .lib files include all appropriate timing arcs to support Shift and Capture modes.

Note When not in scan mode, the scan clocks must not toggle and scanrstz should be tied low.

3.3.7.3 Scan Functionality Details

This section details scan functionality in the PLL.

3.3.7.3.1 Scan Chains

All scan chains have a maximum of 100 flip-flops and are positive-edge triggered.

All scan chains are terminated with lockup latches.

3.3.7.3.2 Scan Clocks

The PLL has is a separate scanclk inputs that supports a maximum frequency of 100 MHz. The PLL clkin input is internally multiplexed with the scanclk input when in scan mode of operation.

All clock outputs from the PHY, have a scan clock input muxed on them when in scan mode.

3.3.7.3.3 Scan Resets

All resets (primary input resets or internally generated resets) are over-ridden to primary scan reset

3.3.7.3.4 Stuck-At Shift Modes

When in Scan Shift, scan clock input is limited to 100 MHz.

3.3.7.3.5 Stuck-At Capture Modes

With a single scan chain and scan clock group domain, no particular requirements exist for capture mode.

3.3.7.3.6 Scan Integration Notes

If scan stitching with the PHY available scan chains, refer to PHY Scan Integration Notes sub-section for the detailed description on the requirements that must be met.

3.3.7.3.7 ATPG Vectors

When running scan vector simulations, use the full gate-level netlist. The scan netlist provided in the deliverables includes a scan model of the analog portion of the design only and should be used for ATPG generation in Tetramax or equivalent tool. When running scan vector simulations, use the full behavioral analog model within the gate-level netlist and sdf back annotation.

4 Functional Description

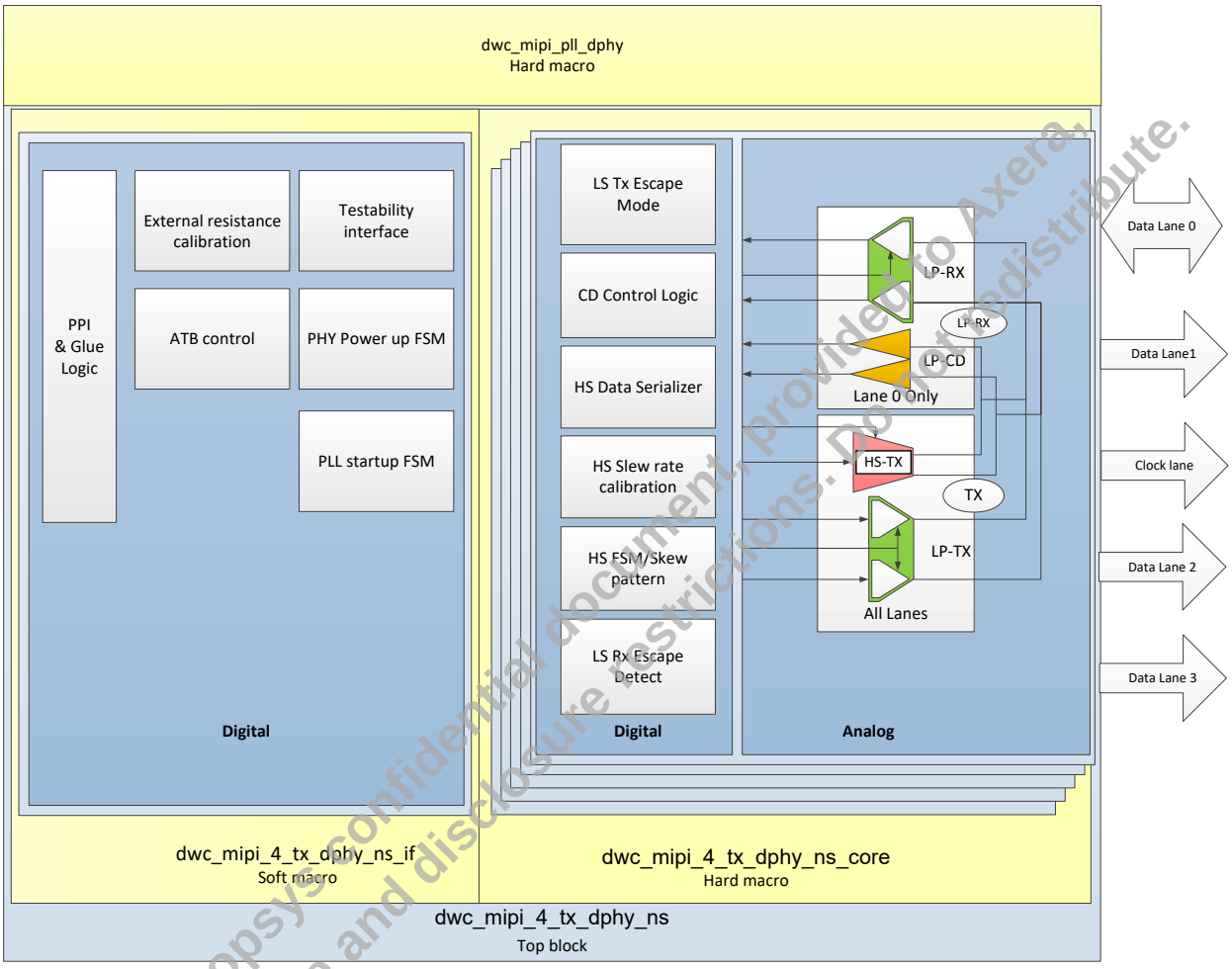
This chapter describes the functional architecture and the various operating modes. It has the following sections:

4.1 Functional Overview

The PHY is composed of two distinct blocks, one mixed-signal hard-macro (dwc_mipi_4_tx_dphy_ns_core) and one digital soft-core (dwc_mipi_4_tx_dphy_ns_if).

Figure 4-1 shows a functional block diagram of the PHY.

Figure 4-1 DWC MIPI D-PHY v1.2 Tx 4L Functional Block Diagram



4.1.1 Mixed-Signal Hard Macro

The mixed-signal hard-macro is composed by an analog and a digital portion:

- Analog portion
  - HS Driver
    - Implements the high-speed TX functionality
    - Replicated for each lane
  - LP Driver
    - Implements the low-power TX functionality

        - Replicated for each lane
    - LP Receiver
        - Available only on data lane 0
    - Contention Detectors
        - Used for contention detector when there is a direction change for data lane 0
    - PLL
        - Generates high-speed clocks required in High Speed operation mode
- Digital portion:
    - The hard macro contains the digital logic related with analog to digital interface, high-speed data path, calibration algorithms, data alignment and PPI logic.

4.1.1.1 45 ohm Termination

MIPI D-PHY supports configuration of HS termination to 45 ohm, through configuration of cb_en_45_ohm_rw signal on 0x20a register.

4.1.1.2 HS TX Slew Rate Calibration

In order to meet D-PHY spec across all frequency range 80-2500 Mbps the PHY has an internal mechanism to calibrate the slew rate. For operating frequency above 1500Mbps it is expected that this control is disabled.

Use the slew rate calibration mechanism referring to "Slew Rate vs DDL Oscillation Target" on page 58. The table documents target configurations that are recommended to set the PHY for typical rise/fall times meeting D-PHY specifications. Perform these configurations as part of the PHY startup sequence and before the PHY is removed from shutdown.

The PHY HS TX rise/fall times and slew-rate control are dependent on system integration, package and board design. Evaluate the PHY configured rise/fall times through the slew-rate control to fine tune the configuration to meet the desired values. Increasing sr_osc_freq_target[11:0] configuration results in a faster slew-rate independent on the state of sr_range. If sr_range=1'b0, the whole configuration range available through sr_osc_freq_target[11:0] results in faster slew-rates than with sr_range=1'b1.

Take in consideration the slew-rate table limits for the PHY configuration, the rise/fall time must be configured to avoid performance issues.

Table 4-1 Supported Rise/Fall Time Limits

Bit rate range	Min UI from the range	Spec for rise / fall
> 1.5 Gbps and ≤ 2.5 Gbps	400 ps	50 ps – 160 ps
> 1 Gbps and ≤ 1.5 Gbps	666 ps	100 ps - 233 ps
> 500 Mbps and ≤ 1 Gbps	1 ns	150 ps - 300 ps
≤ 500 Mbps	2 ns	150 ps - 300 ps

Table 4-2 Slew Rate vs DDL Oscillation Target

sr_range bit 0 of test control register with address 0x272	sr_osc_freq_target[11:8],sr_osc_freq_target[7:0] bit 3:0 of test control register with address 0x271, bit 7:0 of test control register with address 0x270	rise/fall times [ps][1] Typical PVT (Z_{os}= 50 Ohm)
Slew rate control off		
0	12'd920	166
1	12'd657	225

[1] Values for reference only, since those are system integration, package and board design dependent.

4.1.1.3 HS TX Amplitude Control

The D-PHY supports programmable HS Amplitude Levels by changing the HS Transmit Differential output voltage through test control. Set bits [7:5] of test control register with address 0x24 following the description in table "HS TX Amplitude Control"

By default the HS TX Voltage reference is set to 400mV, meaning that the HS differential output |VOD| is 200mV

Table 4-3 HS TX Amplitude Control

cb_sel_v400_prog[2:0]	HS TX Voltage Reference	HS transmit differential voltage - |VOD|
1XX (default)	400mV	200mV
011	450mV	225mV
010	350mV	175mV
001	300mV	150mV
000	200mV	100mV

4.1.2 Digital Soft-Core Macro

The digital soft-core is a purely digital block and contains low speed digital logic with blocks responsible for PHY power up, calibration algorithms and includes tester interface. Figure 4-2 on page 60 illustrates the most relevant state transitions.

The following blocks are included in the soft macro:

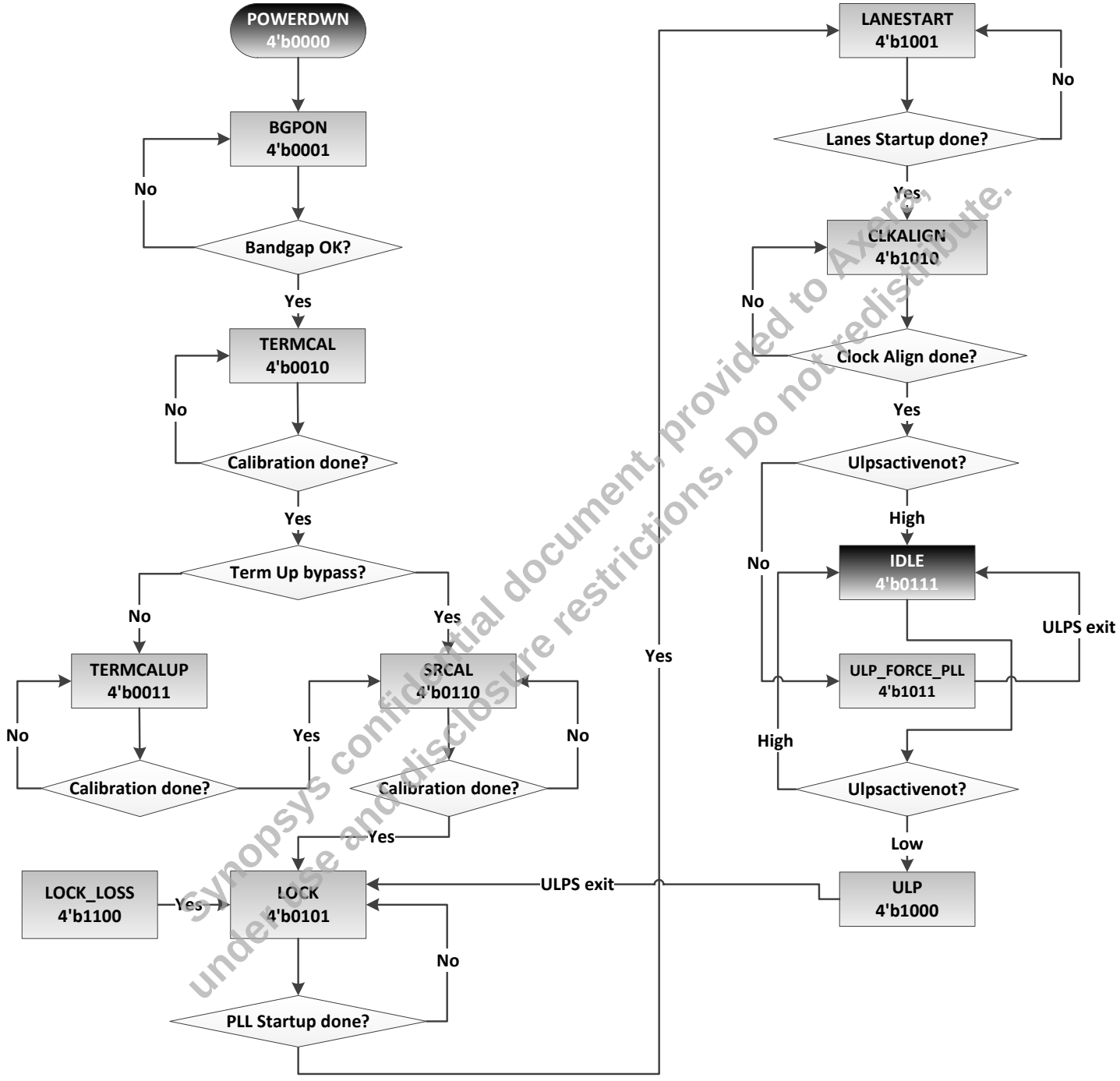
- dwc_mipi_4_tx_dphy_ns_if
  - Top block that instantiates all others.
- dwc_mipi_4_tx_dphy_ns_dphytermcal

  The resistor termination calibration machine is responsible to guarantee that the following PHY parameters meet the specification throughout silicon corners:
  - HS Single ended output impedance Zos
  - HS Single ended output impedance mismatch – Δzos

    The calibration machine relies on external resistor rext (200Ω with 1% spread). This is done by a set of switches (tx_cb_cal_repl<3:0>), that are progressively enabled and disabled resulting in an overall internal replica resistance value higher or lower that rext. The results “higher than” and “lower than” are actually the output of internal comparator than rext.
  - HS termination impedance can be calibrated to 45 Ω through control of cb_en_45_ohm on register 0x21.
- dwc_mipi_4_tx_dphy_ns_ rcal_adc
  - The ADC/DAC block is responsible for generating the control signals that actuate on the analog structures involved in the A/D and D/A conversions.
  - Concerning the D/A conversion, this operation is achieved by providing a direct code in a 10-bit scale that will produce a voltage within the VPH range. Depending on the configuration of the analog switches connected into the ATB bus it is possible to drive the ATB pin with the respective generated voltage. Thermometer encoding is performed within the analog blocks.
  - Concerning the A/D conversion, another type of dynamics is needed since a feedback loop exists to produce the correct code for the analog voltage that is measured. A SAR algorithm is implemented where, for all the code bits, adjustment is being performed depending on error evaluation. This error is generated by a comparator that exists in the CB controlled by the ADC/DAC block.
- dwc_mipi_4_tx_dphy_ns_dphyifpowerctrltx
  - Block responsible for PHY power up
- dwc_mipi_4 _tx_dphy_ns_dphy2txtester
  - To monitor FSM state, refer to test control register 0x03, state_main[3:0] signal. If required, for debugging purposes, the FSM state can be overridden through test control register 0x03 force_state signal.
  - The PHY contains a set of control registers that are primarily used for the PHY configuration of its normal operating modes but that are also used for testing either under the scope of normal silicon characterization or debug activities and production testing in the ATE environment.

- dwc_mipi_4_tx_dphy_ns_mpll_startup
  - PLL power up FSM

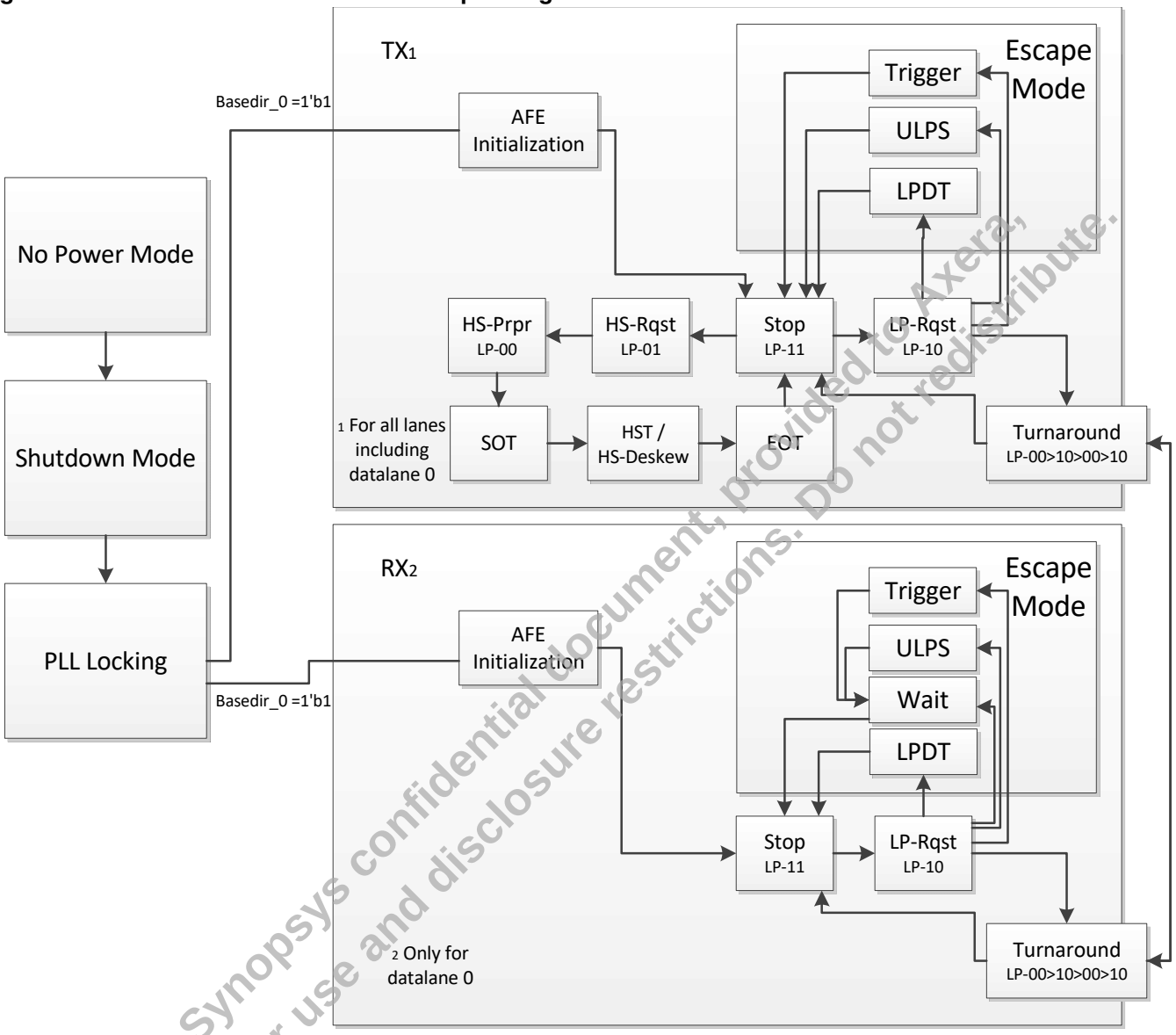
Figure 4-2 Power Up Flow



4.2 Operating Modes

This section describes the various operating modes of the PHY.

Figure 4-3 DWC MIPI D-PHY v1.2 Tx 4L Operating Modes



4.2.1 Initialization

4.2.1.1 No Power Mode

The No Power mode is characterized by the non-existence of any supply voltage applied to the PHY. In order to get to the powered modes, proper voltages should be applied sequentially to the PHY, this task is usually done by the SoC PMU or eventually by global powering up sequence.

The recommended power up sequence is that the core voltage (vdd) powers up first and then the analog voltage powers up (vph, vp, vpl). It is because the circuits supplied from core domain are controlling

circuits supplied from vp and vph domains. Recommended Start-up sequence will result in:

- minimum leakage currents from vp/vph domains during supplies voltage ramp,
- lack of accidental traffic on D-PHY lines as being a result of uncontrolled vp/vph domains.

The vp and core (vdd) supply voltages can be controlled simultaneously.

If leakage or accidental traffic is not a concern for SoC and system, then all power supplies can be ramped-up independently.

The PHY supports power collapsing see "Power Collapsing" on page 62), which ensures valid logical levels across power domains even when one of the supplies is not present at a given time.

4.2.1.2 Shutdown Mode

This mode is the lowest power consumption mode, where all analog blocks are disabled, and digital logic is reset. The current consumption is given by the analog standby current and the digital logic leakage current. It is entered asynchronously when rstz and shutdownz are in low state. It should be ensured that the testclr signal is asserted by default, as it acts as an active high reset to the control block responsible for the configuration values preset. In this mode, the differential lines of datan/datap and clkn/clkp are high impedance (Hi-Z).

All necessary MIPI D-PHY configurations to set the desired operation should be made with the MIPI D-PHY on this mode, before Start-up. This includes the PLL that must be configured to the desired output frequency, which determines the bit rate on the transmission path. For more information, see "DesignWare PLL" on page 35.

If the power domain from the digital logic (vdd) driving the PHY is not available, the PHY should be set in shutdown mode as described above through clamps or other mechanism on the SoC to set the PHY in a known shutdown state through control of the necessary signals.

Power Collapsing

The MIPI D-PHY macro and add-on support power collapsing. If multiple MIPI D-PHY instances are sharing the power rails, the notes presented below are applicable as the state of any power supply rail will apply to all.

The following table documents the supported power collapsing scenarios. Not considering them may lead to undesired behavior such as:

- Unexpected leakage
- Latch-up conditions
- Lane coupling
- Accidental traffic on signal pairs

The PHY should be set in Shutdown Mode during the power collapsing scenarios.

Table 4-4 Power Collapsing Scenarios

vph	vp/vdd	I/Os (rext, clk* and data*)	Support	Comments
Present	**Present**			Not used lanes can be tied to ground/left floating (enable_n set to 1'b0). Is also possible to have VDD supply grounded or floating (digital supply power gating scenario), while VP and VPHY supplies are present.
Present	Present	I/Os bonded out and tied to ground	Supported	
Present	Present	I/Os not bonded out and tied to ground	Supported	
Present	Present	I/Os bonded out and floating	Supported	
Present	Present	I/Os not bonded out and floating	Supported	
Grounded	**Present**			
Grounded	Present	I/Os bonded out and tied to ground	Supported	
Grounded	Present	I/Os not bonded out and tied to ground	Supported	
Grounded	Present	I/Os bonded out and floating	Supported if I/Os not part of LU tests	Not allowed for any external voltage to be driven on the I/Os, what would occur during LU tests. If I/O voltage rises above 0.7V huge current will flow.
Grounded	Present	I/Os not bonded out and floating	Supported	
Floating	**Present**			
Floating	Present	I/Os bonded out and tied to ground	Supported	
Floating	Present	I/Os not bonded out and tied to ground	Supported	
Floating	Present	I/Os bonded out and floating	Not Supported	Not allowed for any external voltage to be driven on the I/Os. If I/O voltage rises above 0.7V vph rail will start charging-up and unexpected leakage may be observed.

Table 4-4 Power Collapsing Scenarios (Continued)

vph	vp/vdd	I/Os (rext, clk* and data*)	Support	Comments
Floating	Present	I/Os not bonded out and floating	Supported	
Present	**Grounded**			If vdd rail is grounded, it is not possible to set PHY in power-down however, with vdd rail grounded, analog portion of the design is set in power-down mode. With only vp/vpl grounded and vdd present, PHY should be set in power-down mode through the control of the necessary PHY input signals.
Present	Grounded	I/Os bonded out and tied to ground	Supported	
Present	Grounded	I/Os not bonded out and tied to ground	Supported	
Present	Grounded	I/Os bonded out and floating	Supported	
Present	Grounded	I/Os not bonded out and floating	Supported	
Grounded	**Grounded**			If vdd rail is grounded, it is not possible to set PHY in power-down however, with vdd rail grounded, analog portion of the design is set in power-down mode. With only vp/vpl grounded and vdd present, PHY should be set in power-down mode through the control of the necessary PHY input signals. Is also possible to have VDD supply floating (digital supply power gating scenario), while VP and VPHY supplies are grounded.
Grounded	Grounded	I/Os bonded out and tied to ground	Supported	Recommendation for when D-PHY is unused on the SoC
Grounded	Grounded	I/Os not bonded out and tied to ground	Supported	Recommendation for when D-PHY is unused on the SoC
Grounded	Grounded	I/Os bonded out and floating	Supported if I/Os not part of LU tests	Not allowed for any external voltage to be driven on the I/Os, what would occur during LU tests. If I/O voltage rises above 0.7V huge current will flow.

Table 4-4 Power Collapsing Scenarios (Continued)

vph	vp/vdd	I/Os (rext, clk* and data*)	Support	Comments
Grounded	Grounded	I/Os not bonded out and floating	Supported	
Floating	**Grounded**			If vdd rail is grounded, it is not possible to set PHY in power-down however, with vdd rail grounded, analog portion of the design is set in power-down mode. With only vp/vpl grounded and vdd present, PHY should be set in power-down mode through the control of the necessary PHY input signals.
Floating	Grounded	I/Os bonded out and tied to ground	Supported	
Floating	Grounded	I/Os not bonded out and tied to ground	Supported	
Floating	Grounded	I/Os bonded out and floating	Supported if I/Os not part of LU tests	Not allowed for any external voltage to be driven on the I/Os. If I/O voltage rises above 0.7V vph rail will start charging-up and unexpected leakage may be observed.
Floating	Grounded	I/Os not bonded out and floating	Supported	
Present	**Floating**			No control over the enable of the analog circuits. This scenario poses risk of leakage from 1.8V domain
Present	Floating	I/Os bonded out and tied to ground	Not Supported	
Present	Floating	I/Os not bonded out and tied to ground	Not Supported	
Present	Floating	I/Os bonded out and floating	Not Supported	
Present	Floating	I/Os not bonded out and floating	Not Supported	
Grounded	**Floating**			
Grounded	Floating	I/Os bonded out and tied to ground	Supported	
Grounded	Floating	I/Os not bonded out and tied to ground	Supported	

Table 4-4 Power Collapsing Scenarios (Continued)

vph	vp/vdd	I/Os (rext, clk* and data*)	Support	Comments
Grounded	Floating	I/Os bonded out and floating	Supported if I/Os not part of LU tests	Not allowed for any external voltage to be driven on the I/Os, what would occur during LU tests. If I/O voltage rises above 0.7V huge current will flow.
Grounded	Floating	I/Os not bonded out and floating	Supported	
Floating	**Floating**			
Floating	Floating	I/Os bonded out and tied to ground	Supported	
Floating	Floating	I/Os not bonded out and tied to ground	Supported	
Floating	Floating	I/Os bonded out and floating	Supported if I/Os not part of LU tests	Not allowed for any external voltage to be driven on the I/Os. If I/O voltage rises above 0.7V vph rail will start charging-up and unexpected leakage may be observed.
Floating	Floating	I/Os not bonded out and floating	Supported	

- The PHY does not use any anti-parallel ESD diodes between vp and vdd and any of the other power supplies. It is therefore expected that floating voltage will be discharged to ground through intrinsic leakage of connected devices. However, there might be cases where the impedance of power switch and leakage of the PHY is similar resulting in a floating condition that can be around half of the supply voltage on the power rail. In such case the PHY can have undefined states and risk of leakage due to cross-coupling effects. It must be ensured that when the power switch is being used that it is OFF impedance is much bigger than the PHY one in OFF state (seen from the power supply pin). If less than 50mV voltage are observed on the floating power supply line, the floating condition can be treated as grounded on the table above.
- D-PHY signal pairs are 1.35V tolerant and must not be connected to 1.8V rail
- When using the PLL add-on, the PLL analog low voltage supply (vpl) should be collapsed together with the IP analog 0.8V supply (vp) power rail.
- It is recommended that you add isolation cells at IP output signals if the IP digital supply is turned off and the block that is interfacing is powered on is a real usage scenario on a given application. This prevents that the outputs of the power gated block ramp slowly, potentially leading to a scenario where they remain around their threshold voltage for some time, causing large current consumption on the interfacing powered digital block.
- If rext or atb is shared with another PHY instance, no PHY instance can be power collapsed. In an integration scenario with multiple D-PHY TX (macro) instances abutted the digital supply (vdd) is shorted. This should be taken into consideration when doing power collapsing.

4.2.2 Active Modes

4.2.2.1 Control Mode

Control mode is the default operating mode. After the initialization is completed (analog calibrations and PLL locking), the PHY remains in this default mode until a request is made either by the protocol layer, or directly through the sequence of low-power signals in the lanes in case of RX (only present in data lane 0). While in control mode, the transmitter side sets the LP-11 state in the lines - this is also called the Stop state.

The receiver side remains in control mode while receiving LP-11 in the lines. Any request must start from and end in Stop state. Following a request, a lane can leave control mode for either high-speed data transfer mode, Escape mode, or Ultra Low Power state.

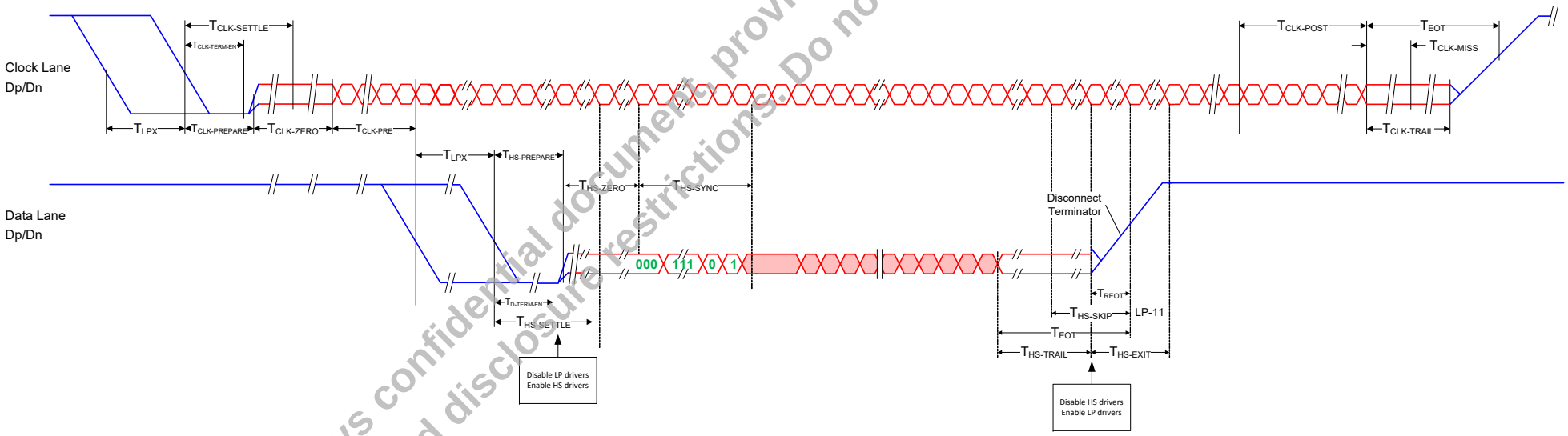
4.2.2.2 High-Speed Data Transmission

Once the initialization sequence is completed, the PHY remains in control mode, which is the default operating mode, until some request appears. High-speed is one of the possible requests at this point. High-speed data transmission occurs in bursts. Only during these bursts the lanes are in high-speed mode. A high-speed burst must start from and return to a Stop state (control mode). A high-speed burst allows for the transmission of payload data by the data lanes. Inherent to such data transmission is the existence of a valid DDR clock in the clock lane. High-speed data bursts are independent for each lane, which means that each data lane can end a high-speed transmission independently of the state of the remaining data lanes. A burst contains the low-power initialization sequence, the high-speed data payload, and also the end of transmission sequence.

From the transmitter side, high-speed mode is entered when the corresponding txrequesths input is set high (assuming that the PHY is in Stop state), PLL is enabled and locked. A TX HS request is not allowed if these conditions are not met. This request is processed in a slightly different way for clock and data lanes. For a clock lane, processing the high-speed starts with the transmission of a low-power sequence (LP01 and LP00). Only after generating this sequence the low-power driver is disabled, and the high-speed driver enabled. After the time necessary to settle TCLK-ZERO, the transmission of the high-speed DDR clock starts. For a data lane, the high-speed entry sequence is the same as for clocklanes (LP01(TLPX) followed by LP00 (THS-prepare) and by THS-ZERO), but in addition, before the payload data there is a leader sequence (THS-SYNC value 8'h1D) that allow for the receiver synchronization. The transmission of such sequence requires the existence of a valid high-speed clock signal in the clock lane. When the high-speed request input is disabled, each lane leaves the high-speed data transmission mode. It is important that a clock lane must be in high-speed mode during the complete high-speed data transmission state of all the lanes. The clock lane must enter the high-speed mode before a high-speed data transmission (Tclk-pre) begins and it must not leave this state before all the lanes finish their respective high-speed (Tclk-post). The operation sequence when leaving the high-speed mode is also slightly different for data and clock lanes. For a clock lane, the high-speed transmission always ends with a HS-0 state (TCLK-trail), followed by the disabling of the high-speed driver, and enabling of low-power driver. As for a data lane, the transmission ends with the

differential state opposite to the last bit transmitted (THS-trail), followed by the disabling of the high-speed driver, and enabling of the low-power driver driving Stop state in the lines (LP11) and returning to Control Mode.

Figure 4-4 High-Speed Data Transmission



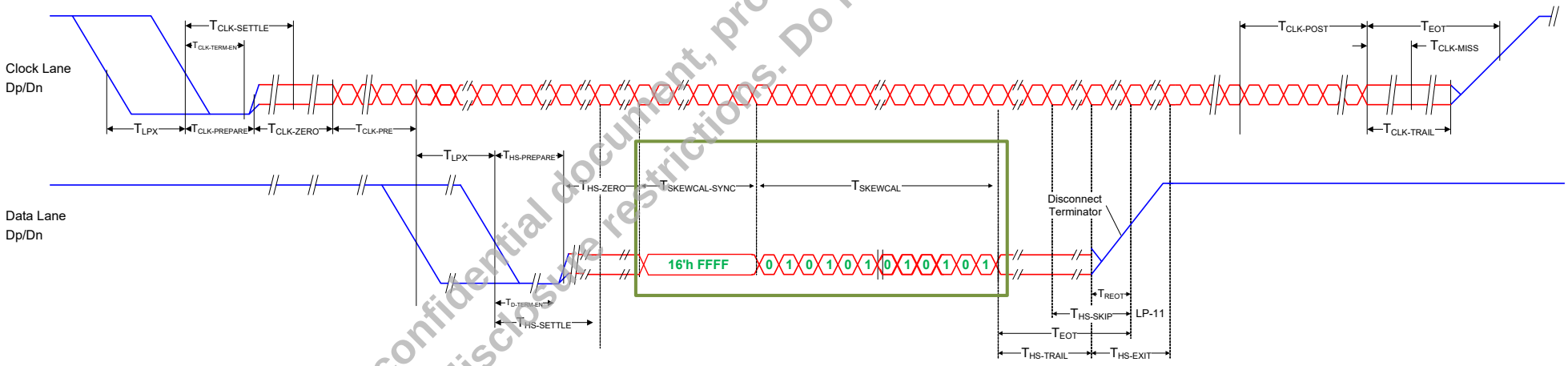
4.2.2.3 DPHY Spec 1.2 High-Speed Deskew Calibration (>1.5 Gbps)

In order to achieve higher data rates in the High-Speed Data Transmission a calibration mode was introduced in D-PHY 1.2 spec. The implemented algorithm will be exercised after the D-PHY RX macro is already powered-up and in STOPSTATE and is triggered by a defined pattern sent by the D-PHY TX.

This mode intends to allow the RX to compensate the skew introduced by TX (TSKEW[TX] static) and by the channel (TSKEW[TLIS] static). High-Speed deskew calibration results in additional margin to correctly sample receiving data for higher data rate. The lines sequence for deskew calibration is very similar to High-speed transfer mode entry. From the transmitter side, high-speed deskew calibration is started when the txskewcalhs input is set high (assuming that the PHY is in Stop state). For clocklane the entry sequence and exit sequence is exactly the same as in normal HS mode. As for the data lanes the entry is the same as for the normal HS except for the leader sequence that is different (value 16'hFFFF for calibration mode) and allows for receiver to distinguish from a normal operation or calibration. After sending the leader sequence a clock pattern is sent in the data lanes while txskewcalhs is asserted to allow deskew calibration on RX side. When this signal is set to low the exit sequence from HS for data lanes and clocklanes takes place exactly as in normal mode.

An initial high-speed deskew calibration should be done by the transmitter when operating above 1.5 Gbps, prior to the first High-Speed Data normal burst. A periodic high-speed deskew calibration is optional and may be used to compensate some VT (voltage, temperature) variations if required.

Figure 4-5 High-Speed Deskew Calibration



4.2.2.3.1 Temperature Change Sensitivity

When RX operates in DPHY 1.2 mode and the junction temperature changes >10 °C, compared to the temperature in the first de-skew sequence, this means that:

- the PHY requires DDL re-calibration.
- TX needs to re-send de-skew pattern.

The reason for this requirement is the fact that DDL block is sensitive to supply and power variations.

In the applications where re-calibration of DDL is not possible, and being exposed only to temperature variations, TX should periodically re-send the de-skew sequence in order to allow RX to adjust its timings.

4.2.2.3.2 Power Supply Change Sensitivity

When RX operates in DPHY 1.1/1.2 mode and average power supply voltage changes more than 3% (ignoring power supply noise), compared to power supply value at the first de-skew sequence, this means that:

- the PHY requires DDL and RX offset cancellation re-calibration.

- TX needs to re-send de-skew pattern.

The reason for this requirement is the fact that DDL block is sensitive to the power variation.

4.2.2.4 Escape Mode

Escape mode is a special mode of operation that uses the data lanes to communicate using the low-power states at low-speed. The PHY supports this mode in both directions for data lane 0 and only in forward direction for lanes 1 to 3. A Data Lane enters the Escape mode through an Escape mode entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00), if an LP-11 is detected before reaching LP-00 state, the entry is aborted and the receiver returns to the Stop state. Once the sequence is correctly completed, the transmitter sends an 8-bit command to indicate a requested action.

Table 4-5 shows the Escape mode supported actions. If the entry command is not valid, it is ignored, erresc error flag goes high, and the receiver waits until the transmitter returns to the Stop state. The PHY applies Spaced-One-Hot encoding (a Mark state is interleaved with a Space state) on commands and data.

Each symbol consists of the following two parts:

- One-Hot phase
- Space state To transmit one bit, a Mark-1 should be sent followed by the Space state. In the case of a zero bit, a Mark-0 should be sent followed by Space state.

Table 4-5 Possible Escape Mode Sequences for Data Lanes

Escape Mode Action	Entry Command Pattern (First Bit to Last Bit to be Transmitted)	Command Type
Low-Power Data Transmission	8'b11100001	mode
Ultra- Lower Power State	8'b00011110	mode
Reset Trigger	8'b01100010	trigger
Unknown - 3	8'b01011101	trigger
Unknown - 4	8'b00100001	trigger
Unknown - 5	8'b10100000	trigger

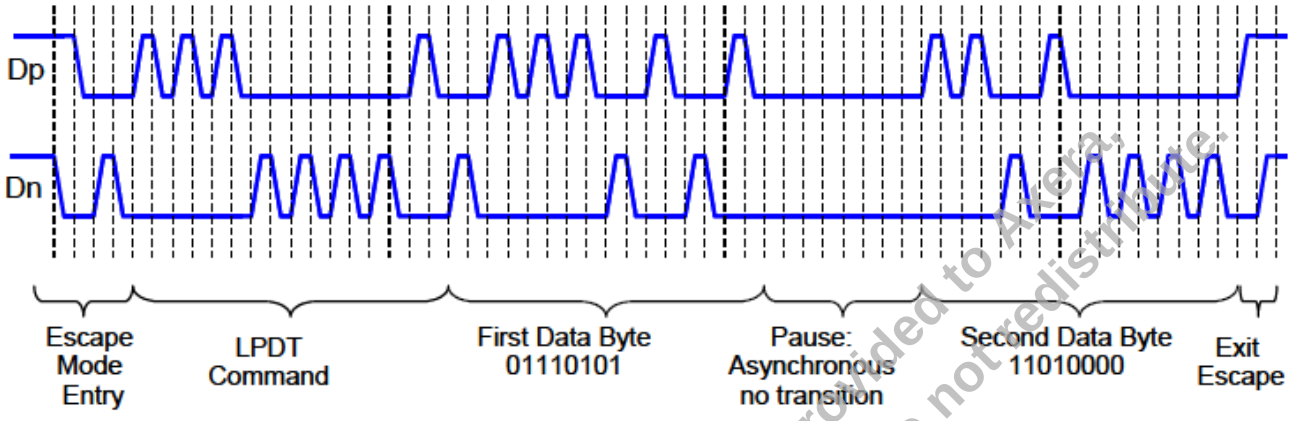
Low-Power Data Transmission (LPDT)

In LPDT mode, the data can be transmitted by the protocol at low speed in Low-Power mode—high-speed drivers or receivers are off and low-power drivers or receivers are on. During LPDT, the protocol can pause

by maintaining a Space state on the lines. The last state before exiting Escape mode is Mark-1—not considered as 1 bit—because it is followed by the Stop state.

Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. This encoding allows data to be self-clocked and does not rely on the Clock Lane.

Figure 4-6 LPDT example



Remote Trigger

This mode allows the protocol to send a flag to the receiving side, on request of the transmitting side. If the Entry Command Pattern matches the Reset-Trigger Command a Trigger is flagged to the protocol at the receive side through the logical PPI. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

Ultra Low Power State (ULPS)

This mode has the lowest power consumption (which can be further reduced when PHY automatically turns off PLL and part of AFE circuitry if all enabled lanes are in forward direction and enter ULPS), excluding the Shutdown mode. For data lanes, this mode is entered by sending an Ultra Lower Power state entry command, after the Escape mode entry command. During this mode, the lines are in the Space state (LP-00). Although the Clock lane does not support regular Escape mode, the Clock lane supports ULPS.

To exit ULPS, the transmitter side drives a Mark-1 followed by a Stop state. The Twakeup time must be ensured by the protocol layer, possibly using TXUlpsExit and TXRequestEsc/TXUlpsClk control signals. By default, the PLL clock multiplier and part of AFE circuitry is switched off if all enabled lanes are in ULPS. If one of the lanes leaves ULPS (using txulpsexit), the PHY will enable the PLL and turn AFE completely on. It is required that the txbyteclkhs clock connection to txbyteclksrc is active and not gated for the ULPS exit procedure to complete. All enabled lanes need to exit ULP state at the same time. The forcepll signal can be

used to maintain the PLL enabled during ULPS or to disable it during ULPS. For this, forcepll needs to be asserted before the PHY enters in ULPS state.

If PLL is disabled during ULPS, and PLL configuration is being done through the PLL SoC signals you must apply updatepll pulse (as described on Figure 3-2 on page 40) before exiting from ULPS.

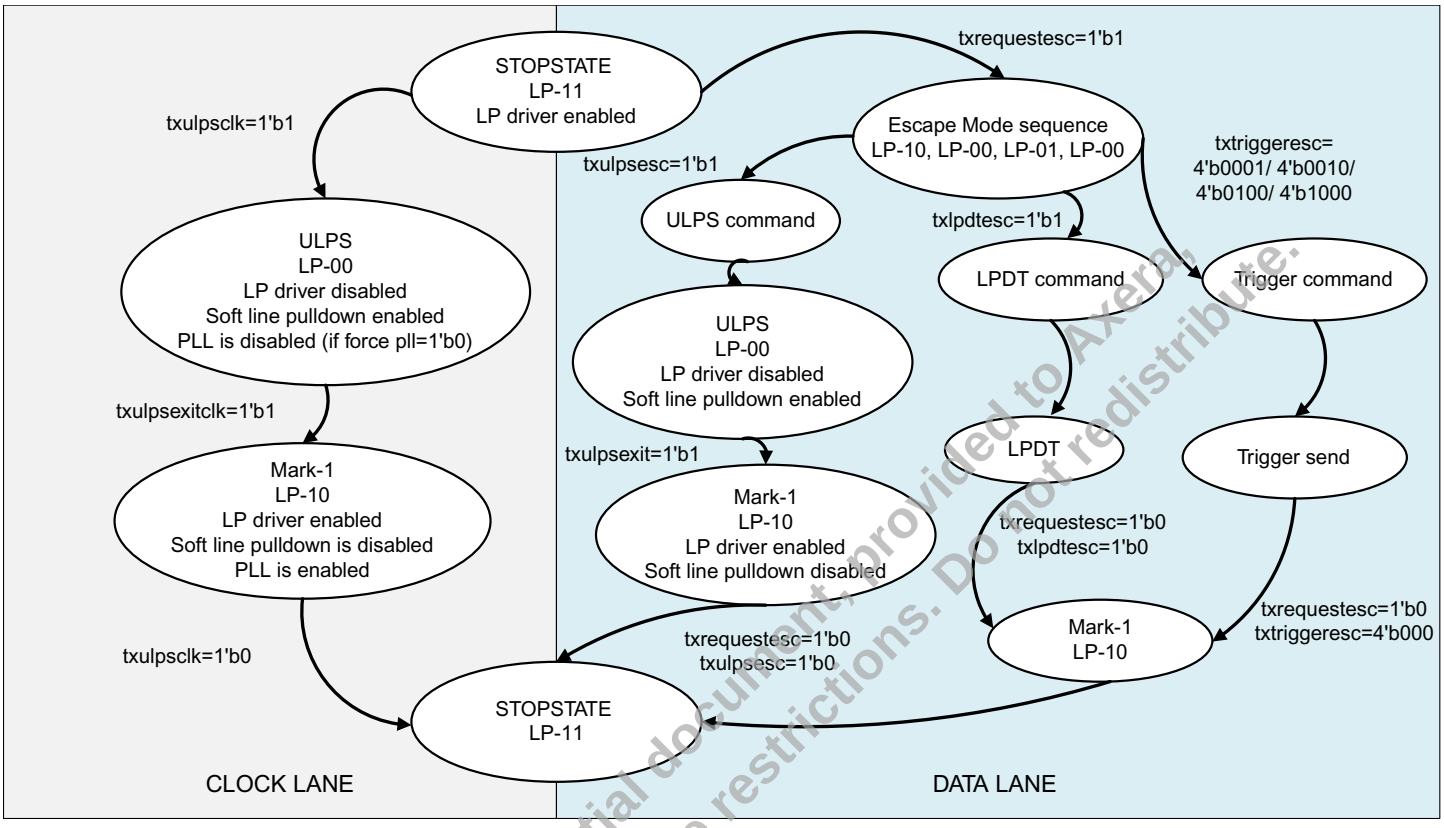
Attention	To disable the PLL in ULPS state, forcepll needs to be de-asserted before the PHY enters the ULPS state. If the clocklane enters ULPS state before datalanes, and txclkesc is generated from txbyteclksrc, the PHY will get stuck due to the lack of txclkesc.

During ULPS state, cfg_clk external clock can be gated for additional power savings as indicated in the following reference procedure:

1. Enter ULP in all enabled lanes (including clock lane) - Global ULP state.
2. Wait until ulpsactivenot_* =1'b0 in all lanes.
3. Wait 20 cfg_clk cycles.
4. Gate cfg_clk.
5. Ungate cfg_clk, at least 20 clock cycles prior to leaving ULP.
6. Leave ULP.
7. Wait until ulpsactivenot_* =1'b1 in all lanes.

Figure 4-7 shows the ULPS state diagram for Clock and Data lanes.

Figure 4-7 Escape Mode Sequences State Diagram



4.2.2.5 Turnaround

The PHY allows the transmission direction of the data lane 0 to be swapped by means of a turnaround request. The sequence of a turnaround operation occurs in this way:

1. Transmitter side
   a. Starts when turnrequest_0 input is set high on transmitter side, assuming the PHY is in Stop state
   b. Transmitter sends specific low-power sequence—LP11, LP10, LP00, L10, L00
2. Receiver side
   a. After receiving complete low-power sequence, receiver enables low-power driver
   b. Transmits LP00, indicating change setting direction_0 output low
   c. Overlapping LP00 transmitted by initial transmitter
   d. Initial receiver side transmits LP10, followed by LP11, returning to Control mode

The turnaround procedure is the same for a Forward-to-Reverse direction or Reverse-to-Forward direction. However, in the Reverse-to-Forward direction, lane 0 only supports Escape Mode.

Figure 4-8 shows the state diagram for a turnaround sequence.

Figure 4-8 Turnaround Sequence State Diagram

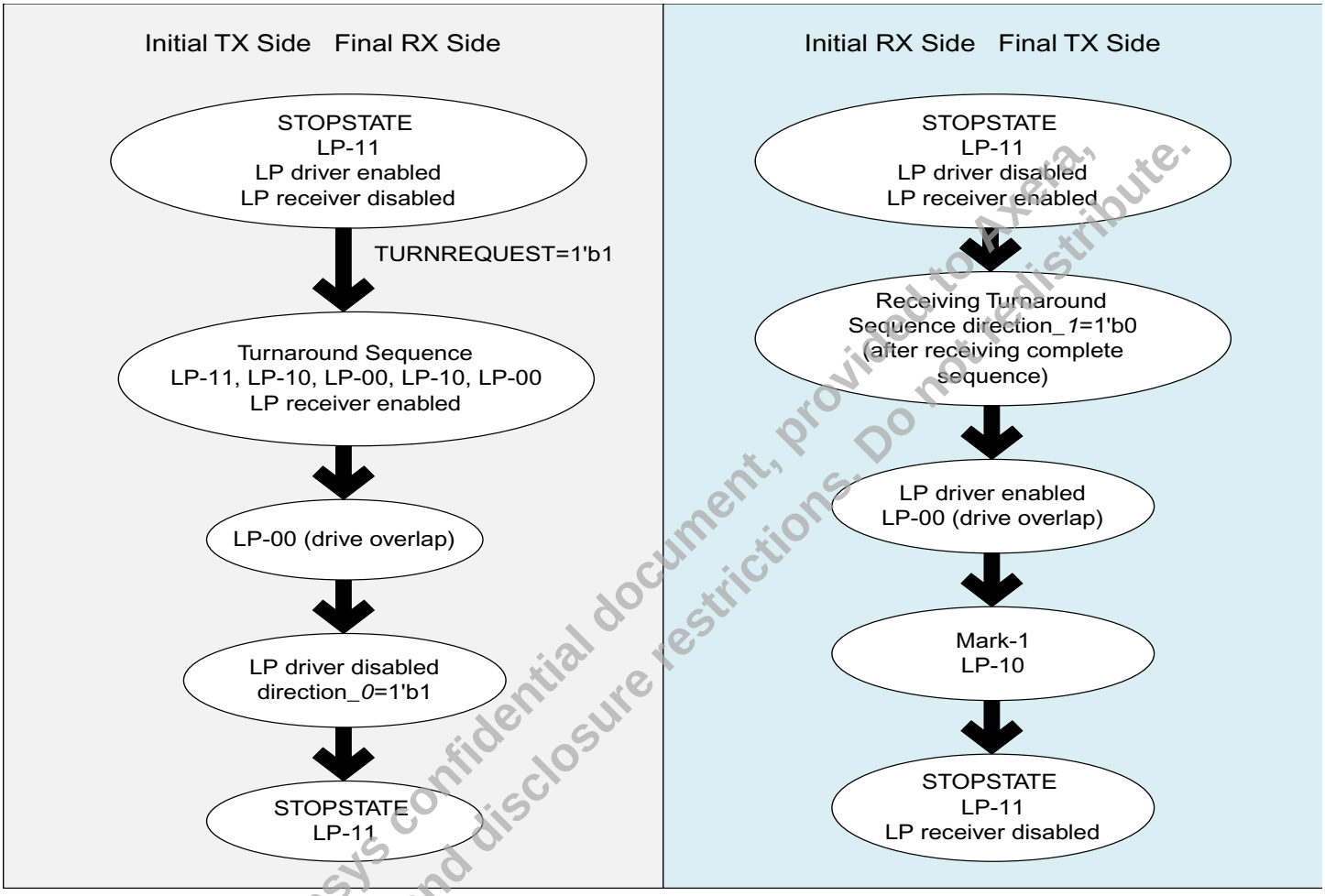
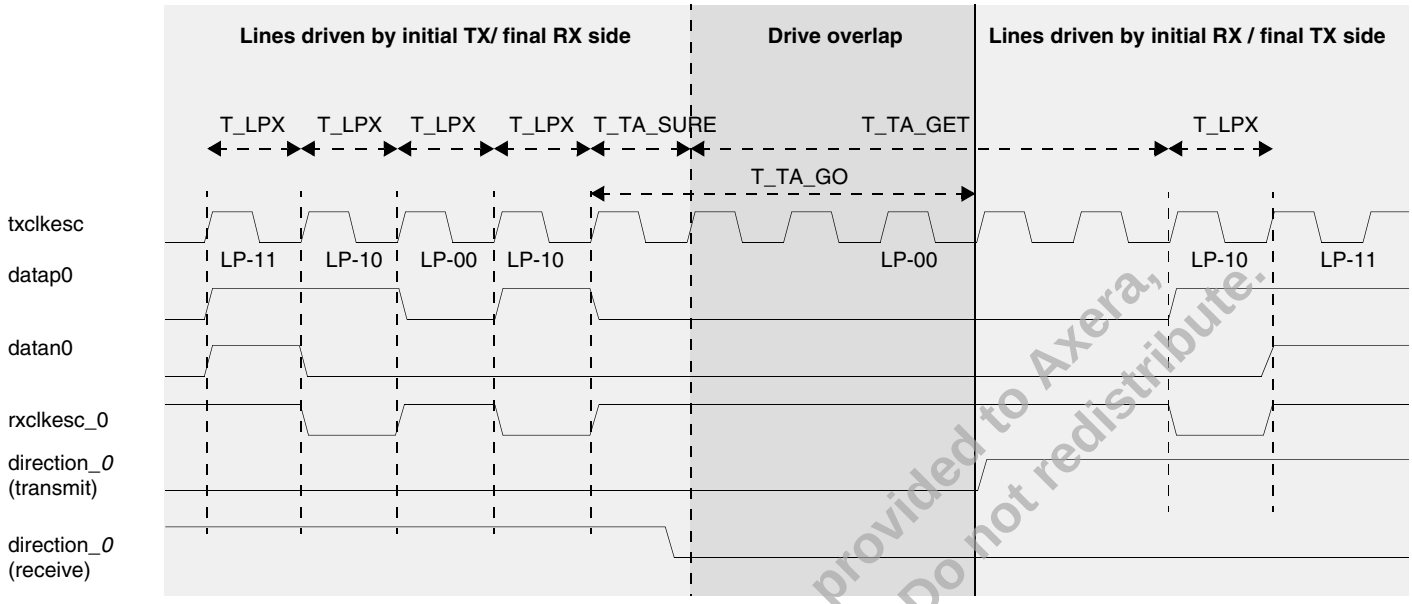


Figure 4-8 shows a timing diagram for a turnaround sequence.

Figure 4-9 Turnaround Timing Diagram



Note The turnaround procedure is the same for a Forward-to-Reverse direction or Reverse-to-Forward direction. However, in the Reverse-to-Forward direction, the PHY only supports Escape Mode. For a Turnaround operation, it is necessary that the txclkesc signal is available on both the transmitter and receiver sides.

4.2.3 Control and Test Modes

4.2.3.1 Overview

The PHY contains a set of control registers that are primarily used for the PHY configuration of its normal operating modes but that are also used for testing either under the scope of normal silicon characterization or debug activities and production testing in the ATE environment. These control registers are accessible through the PHY test and control interface signals (testdin[7:0], testdout[7:0], testen, testclk and testclr).

For correct configuration and testability of the PHY, ensure that this test and control interface is accessible through the link controller and/or by any other means (multiplex/demultiplex layer to chip I/Os, JTAG controller, and so on).

4.2.3.2 Interface Timing

This section contains the timing diagrams for configuring a test code in the PHY. The standard procedure is two-folded; first the necessary test code is programmed and then the related test data words are fed to the tester's inputs.

To configure a test code, have the PHY in shutdown mode (shutdownz=0) and then reset it (rstz=0). This avoids the transient periods in the operation during re-configuration procedures. It is also recommended to apply a tester reset pulse (testclr = 1) before any test code configuration.

The test code programming is done using the following steps:

1. Set the desired test code
   a. Ensure that testclk is set to high.
   b. Place the 8-bit word corresponding to the test code in TESTDIN.
   c. Set testen to high.
   d. Set testclk to low.

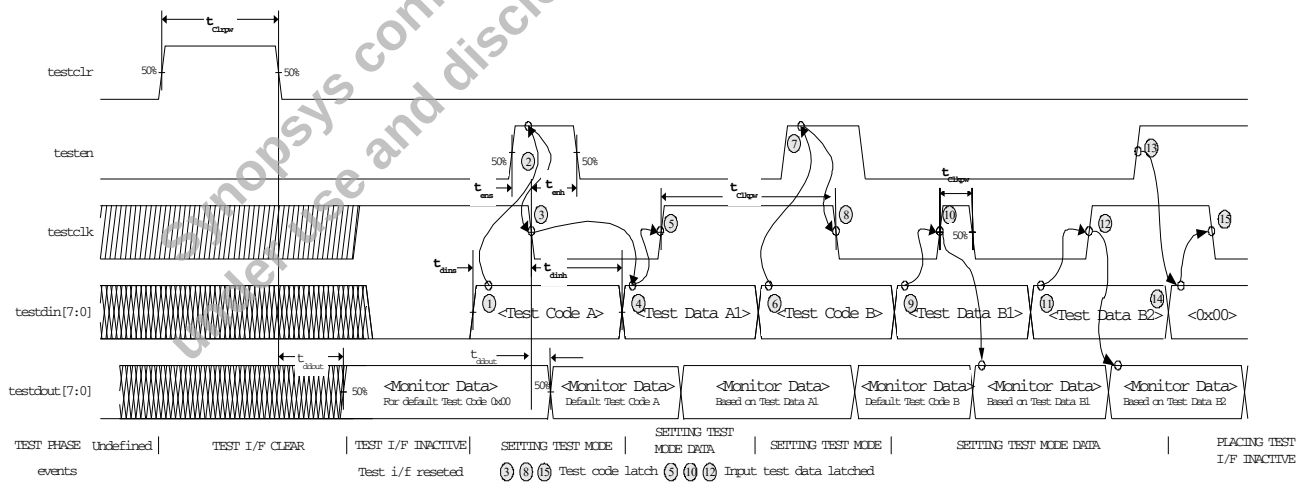
      With the falling edge on testclk, the TESTDIN[7:0] signal content is latched internally as the current test code.
   e. Set testen to low.
2. Enter the necessary test data
   a. Set testclk to low, if not done already.
   b. Place the 8-bit word corresponding to the required test data in TESTDIN.
   c. Set testclk to high.

      Test data is programmed internally.
   d. Repeat the steps to add more test data for the same test code.

Repeat the above procedure to program subsequent test codes. Additionally, a test reset procedure (testclr = 1) is only needed prior to the first programming operation or if you wish to reset the PHY's configuration to its default values and override any changes made meanwhile.

Figure 4-10 shows a generic timing diagram for test operation. After a test code is effectively programmed, TESTDOUT[7:0] asynchronously outputs relevant data for that specific test code, whether it is pure read-back data or other meaningful signals.

Figure 4-10 Testability Interface Timing Diagram



Some important observations on Figure 4-10:

- After the required testclr pulse, TESTDOUT outputs monitor data for the default test code (0x00). This is used to get information out after the PHY is powered up. Such information may be relevant to determine the operation status of the PHY and may not be related to any test code in particular. For the current implementation, TESTDOUT defaults to 0x00.
- Monitor data for a specific test code may change in response to the following events:
  - The test code is programmed and the default output data appears in TESTDOUT.
  - The TESTDOUT is populated with the test code already configured.
  - The TESTDOUT outputs asynchronous internal signals whose timing is unpredictable.
- Some test codes require two write data operations, where the first one sees the testclk going from high to low. It is crucial that the falling edge in the clock does not occur with testen asserted or else the current test data will be latched as an erroneous test code.
- Placing the test interface in inactive mode is best achieved by programming the test code 0x00 as shown in the final sequence in Figure 4-10. Although not mandatory, it is highly recommended to close any reconfiguration with this final sequence.

An additional scenario is that of a case in which two testcodes must be programmed one after the other without any intermediate test data written to the tester. Caution is in order, as the test code is only latched internally with the falling edge of testclk, the inevitable rising edge must occur only when testen is asserted or else the second test code is wrongly interpreted as the test data for the active test code. For details, see Figure 4-11.

Figure 4-11 Two Consecutive Test Codes Handling

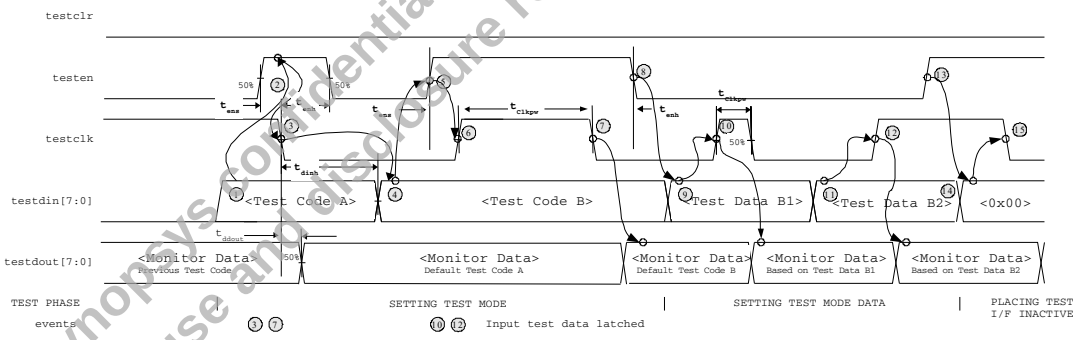


Table 4-6 Timing Constraints for Test Interface

Timing Arc	Description	Minimum	Maximum	Unit
tclrpw	TESTCLR minimum pulse width	5		ns
tclkpw	TESTCLK minimum pulse width	5		ns
tddout	TESTDOUT output delay		10	ns
tens	TESTEN setup time	2		ns

Table 4-6 Timing Constraints for Test Interface (Continued)

Timing Arc	Description	Minimum	Maximum	Unit
tenh	TESTEN hold time	2		ns
tdins	TESTDIN setup time	2		ns
tdinh	TESTDIN hold time	2		ns

The testclk signal acts as a strobe for the test interface and for power reduction purposes we suggest that testclk only has pulses when SoC intends to exercise the test interface and this way not be always toggling.

Note

Monitor data for a specific test code may change in response to the following events:

- The test code is programmed and the default output data appears in testdout.
- The testdout is populated with the test code already configured.
- The testdout outputs asynchronous internal signals whose timing is unpredictable.

4.2.4 Start-Up Sequence

Before D-PHY Start-up, the D-PHY needs to be properly configured for the desired operation. This needs to be done with the PHY in shutdown mode and it is assumed that such configurations are static or at least are stable prior to leaving the Shutdown mode.

Before D-PHY power, set mpll_prg[0]=1 to set PLL regulator in bypass. This control signal can be configured to mpll_prg[0]=0 when in ULPS or power-down for reduced power consumption.

The D-PHY operating frequency and input reference clock frequency need to be configured through hsfreqrange[6:0] and cfgclkfreqrange[5:0].

- IP operating frequency: hsfreqrange[6:0]
- Input reference clock frequency: cfgclkfreqrange[5:0]

Regarding input system clock cfg_clk frequency, cfgclkfreqrange[5:0] needs to be configured according to the following formula:

cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4]

To configure the bit rate operation you should directly configure hsfreqrange for the desired frequency range or set the register hsfreqrange, “Test Code: 0x44”, with the proper code. You can only configure hsfreqrange before the D-PHY Start-up. You can not change hsfreqrange setting during active operation.

Note It is required that the txbyteclkhs clock connection to txbyteclksrc is active and not gated in order to complete start-up.

The PLL needs always to be properly configured for the desired operating frequency before D-PHY Start-up. This configuration can be done through the D-PHY test and control interface or through the PLL SoC shadow registers interface. For additional details see“Initialization” on page 39.

The PHY consists of four data lanes, but applications can use four or lesser number data lanes. In such cases, you are granted access to individual enabling signals (enable_n) that control which lanes should be used and evolve through all the necessary initialization steps. It is not allowed for the enable signals to be changed during operation. They should be set in power-down.

Note When the PHY is operating in HS mode data lane 0 must be enabled.

After the PLL is configured, the D-PHY is responsible for the Start-up and power-down of the PLL within its power sequence logic; this control is transparent to you. After rstz and shutdownz are released, the D-PHY starts its Start-up sequence and, with it enabled, the PLL will lock to the configured operation.

It is assumed that all configurations are static or at least are stable prior to leaving the Shutdown mode. This includes not only configurations through D-PHY SoC interface but all configurations done through the D-PHY test and control interface.

After the reset signals (rstz and shutdownz) are released, the PHY begins an initialization sequence to allow correct operation. The sequence of the release of signals is not critical, but it is recommended that shutdownz precede rstz. It is assumed that the cfg_clk signal is available and stable by that time. If there are no test or configuration operations to be performed, the testclr signal can be kept at logic high level.

Otherwise, the testclr must be de-asserted to bring the control logic out of reset and allow for the necessary configuration steps through the control interface.

The D-PHY specification has many timing intervals which have to be followed to ensure proper operation.

The initialization sequence ends when stopstate LP11 is driven in the lanes and the PHY reaches Control Mode state.

Table 4-7 Frequency Ranges and Defaults

Range (Mbps)	Default Bit Rate (Mbps)	hsfreqrange[6:0]
80 - 97.125	80	0000000
80 - 107.625	90	0010000
83.125 - 118.125	100	0100000
92.625 - 128.625	110	0110000
102.125 - 139.125	120	0000001
111.625 - 149.625	130	0010001
121.125 - 160.125	140	0100001
130.625 - 170.625	150	0110001
140.125 - 181.125	160	0000010
149.625 - 191.625	170	0010010
159.125 - 202.125	180	0100010
168.625 - 212.625	190	0110010
182.875 - 228.375	205	0000011
197.125 - 244.125	220	0010011
211.375 - 259.875	235	0100011
225.625 - 275.625	250	0110011
249.375 - 301.875	275	0000100
273.125 - 328.125	300	0010100
296.875 - 354.375	325	0100101
320.625 - 380.625	350	0110101
368.125 - 433.125	400	0000101
415.625 - 485.625	450	0010110
463.125 - 538.125	500	0100110

Table 4-7 Frequency Ranges and Defaults (Continued)

Range (Mbps)	Default Bit Rate (Mbps)	hsfreqrange[6:0]
510.625 - 590.625	550	0110111
558.125 - 643.125	600	0000111
605.625 - 695.625	650	0011000
653.125 - 748.125	700	0101000
700.625 - 800.625	750	0111001
748.125 - 853.125	800	0001001
795.625 - 905.625	850	0011001
843.125 - 958.125	900	0101001
890.625 - 1010.625	950	0111010
938.125 - 1063.125	1000	0001010
985.625 - 1115.625	1050	0011010
1033.125 - 1168.125	1100	0101010
1080.625 - 1220.625	1150	0111011
1128.125 - 1273.125	1200	0001011
1175.625 - 1325.625	1250	0011011
1223.125 - 1378.125	1300	0101011
1270.625 - 1430.625	1350	0111100
1318.125 - 1483.125	1400	0001100
1365.625 - 1535.625	1450	0011100
1413.125 - 1588.125	1500	0101100
1460.625 - 1640.625	1550	0111101
1508.125 - 1693.125	1600	0001101
1555.625 - 1745.625	1650	0011101
1603.125 - 1798.125	1700	0101110
1650.625 - 1850.625	1750	0111110
1698.125 - 1903.125	1800	0001110
1745.625 - 1955.625	1850	0011110
1793.125 - 2008.125	1900	0101111

Table 4-7 Frequency Ranges and Defaults (Continued)

Range (Mbps)	Default Bit Rate (Mbps)	hsfreqrange[6:0]
1840.625 - 2060.625	1950	0111111
1888.125 - 2113.125	2000	0001111
1935.625 - 2165.625	2050	1000000
1983.125 - 2218.125	2100	1000001
2030.625 - 2270.625	2150	1000010
2078.125 - 2323.125	2200	1000011
2125.625 - 2375.625	2250	1000100
2173.125 - 2428.125	2300	1000101
2220.625 - 2480.625	2350	1000110
2268.125 - 2500	2400	1000111
2315.625 - 2500	2450	1001000
2363.125 - 2500	2500	1001001

4.2.4.1 Configuration Examples

Start-up configuration examples are provided below. If the test and control interface is to be used before DPHY Start-up for any additional configuration or debug purposes, it must be exercised after the testclr pulse and before shutdownz and rstz de-assertion which will start the D-PHY Start-up sequence.

While shutdownz and rstz are de-asserted, the DPHY remains in POWERDWN state. If the PHY properly reached the end of its startup sequence, it will be in IDLE state. For additional details on the startup procedure, refer to sub-section 4.1.2 on page 59 and the FSM states description.

Case 1 (operating rate 1 Gbps; cfg_clk=27 MHz; slew rate calibration enabled):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] = 7'b0001010.
7. Refer to table "Slew Rate vs DDL Oscillation Target" on page 58 and configure test control registers with appropriate values for the specified rise/fall time.
8. Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration.
9. Set mpll_prg[0]=1'b1 hrough test control register 0x1F.

10. Configure register 0x4a to set prg_on_lane0 (bit 6) to 1'b1.
11. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] = 6'b101000.
12. Apply cfg_clk signal with 27Mhz frequency.
13. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface (see "Initialization" on page 39 for additional details).
14. Set basedir_0 = 1'b0.
15. Set all requests inputs to zero.
16. Wait for 15 ns.
17. Set enable_n and enableclk=1'b1.
18. Wait 5ns.
19. Set shutdownz=1'b1.
20. Wait 5ns.
21. Set rstz=1'b1.
22. Wait until stopstatedata_n and stopstateclk outputs are asserted indicating PHY is driving LP11 in enabled datalanes and clocklane.

Case 2 (operating rate 2.5 Gbps; cfg_clk=27 MHz; slew rate calibration disabled):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] = 7'b1001001.
7. Configure register 0x4a to set prg_on_lane0 (bit 6) to 1'b1.
8. Set bit [1] of test control register with address 0xA0 to 1'b1 to bypass slew rate calibration algorithm.
9. Set bits [1:0] of test control register with address 0xA3 to 2'b00 to disable slew rate calibration.
10. Set mpll_prg[0]=1'b1 through test control register 0x1F.
11. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] = 6'b101000.
12. Apply cfg_clk signal with the appropriate frequency with 27 Mhz frequency.
13. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface (see "Initialization" on page 39 for additional details).
14. Set basedir_0 = 1'b0.
15. Set all requests inputs to zero.
16. Wait for 15 ns.

17. Set enable_n and enableclk=1'b1.
18. Wait 5ns.
19. Set shutdownz=1'b1.
20. Wait 5ns.
21. Set rstz=1'b1.
22. Wait until stopstatedata_n and stopstateclk outputs are asserted indicating PHY is driving LP11 in enabled datalanes and clocklane.

Case 3 (operating rate 2.5 Gbps; cfg_clk=27 MHz; slew rate calibration disabled, HS-TX regulator enabled at startup):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] = 7'b1001001.
7. Set bit [1] of test control register with address 0xA0 to 1'b1 to bypass slew rate calibration algorithm.
8. Set bits [1:0] of test control register with address 0xA3 to 2'b00 to disable slew rate calibration.
9. Set mpll_prg[0]=1'b1 through test control register 0x1F.
10. Configure register 0x4a to set prg_on_lane0 (bit 6) to 1'b1.
11. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] = 6'b101000.
12. Apply cfg_clk signal with the appropriate frequency with 27 Mhz frequency.
13. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface (see "Initialization" on page 39 for additional details).
14. Set basedir_0 = 1'b0.
15. Set all requests inputs to zero.
16. Wait for 15 ns.
17. Set enable_n and enableclk=1'b1.
18. Wait 5ns.
19. Set shutdownz=1'b1.
20. Wait 5ns.
21. Set rstz=1'b1.
22. Wait until stopstatedata_n and stopstateclk outputs are asserted indicating PHY is driving LP11 in enabled datalanes and clocklane.

23. Set Bits [3:2] of Test registers with address 0x30, 0x40, 0x50, 0x80 and 0x90 should be set to 2'b11 to turn on HS-TX regulators.
24. Configure registers 0x60 and 0x70 to adjust the HS TX Lane Request State counter for clocklane and datalane to 19 (dec) to reduce LP01 to ~50 ns.
25. Set bit 7 of test control registers with address 0x64 and 0x74 to 1'b1.

4.2.4.2 Configuration for Shorter TLPx Timing

For TLPx = 50 ns the HS TX circuit needs to be powered on at an earlier stage.

You can perform the configuration described below:

1. Enable HS power on for clk and datalanes.
   - On register dphy2txtester_DIG_RDWR_TX_CLKLANE_LANE_3 (address 0x304), set fields (bits [3:2]) to 2'b11.
   - On register dphy2txtester_DIG_RDWR_TX_LANE0_LANE_3 (address 0x504), set fields (bits [3:2]) to 2'b11.
   - On register dphy2txtester_DIG_RDWR_TX_LANE1_LANE_3 (address 0x704), set fields (bits [3:2]) to 2'b11.
2. Change TLPx timer counters.

   Clock lane:
   - On register dphy2txtester_DIG_RDWR_TX_SYSTIMERS_14 (address 0x5c), set field (bit 7) to 1'b1.
   - On register dphy2txtester_DIG_RDWR_TX_SYSTIMERS_15 (address 0x5d), set fields (bits [7:0]) to 19 (example for 2.5 Gbps).

   Data lanes:
   - On register dphy2txtester_DIG_RDWR_TX_SYSTIMERS_20 (address 0x62), set field (bit 7) to 1'b1.
3. On register dphy2txtester_DIG_RDWR_TX_SYSTIMERS_21 (address 0x63), set fields (bits [7:0]) to 19 (example for 2.5 Gbps).

4.2.5 Calibrations Test Control Registers

During Start-up or when Start-up is complete and the PHY has reached stopstate you can use the following test control registers to:

- Check the calibrations status
- Check the calibrations values
- Override the values obtained from the calibrations, for instance for debugging purposes

4.2.5.1 Termination Calibration with rext (FSM State: TERMCAL)

Calibration status:

- 0x22: Termination Calibration Lower Section FSM Control and Override Testdin[7]=1'b0;

- Read bit [5] - rescal_done
- Read bit [6] – rescal_error (multi-toggle flag, not an error)

Calibration value:

Testdin[7]=1'b0;

- Read bits [3:0] - cb_cal_repl[3:0]

Force calibration value:

- Write bit [6] - cb_cal_repl_ovr_en
- Write bits [5:2] - cb_cal_repl_ovr [3:0]

4.2.5.2 Termination Calibration Upper Part with rext (FSM State: TERMCALUP):

Calibration status:

- 0x23: Termination Calibration Upper Section FSM Control and Override Testdin[7]=1'b0;
  - Read bit [5] - rescal_up_done
  - Read bit [6] – rescal_up_error (multi-toggle flag, not an error))

Calibration value:

Testdin[7]=1'b0;

- Read bits [3:0] - cb_cal_repl_up[3:0]

Force calibration value:

- Write bit [6] - cb_cal_repl_up_ovr_en
- Write bits [5:2] - cb_cal_repl_up_ovr[3:0]

4.2.5.3 PLL Startup and Lock Procedure (FSM State: LOCK):

Calibration status:

- 0x0D: PLL Power-Up Control
  - Read bit [6] - pll_startup_done

4.2.5.4 Clock Alignment Procedure (FSM State: CLKALIGN):

Calibration status:

- 0xAE: Clock Align
  - Read bit [2] - ck_align_done

4.2.5.5 Slew Rate Calibration (FSM State: SRCAL):

Calibration status:

- 0xA7: Slew Rate Status Observability
  - Read bit [3] – srcal_done
  - Read bit [2] – sr_finished
  - Read bit [4] – sr_error_flag
  - Read bit [5] – sr_error_above_max
  - Read bit [0] – sr_freq_min_error

Calibration value:

- 0xA9: Slew Rate Observable Signals
  - Read bits [5:1] – sr_control[4:0]

0xA8: Slew Rate Measured DDL Cycles

Testdin[7]=1'b1:

- Read bit [6:0] – sr_freq_meas_out[6:0]

Testdin[7]=1'b1:

- Read bit [3:0] – sr_freq_meas_out[11:7]

Force calibration value:

- 0xA2: Slew Rate Override Control
  - Write bits [4:0] – sr_control_ovr[4:0]
  - Write bit [0] – sr_control_ovr_en

Note The calibration status values are informative. Calibration error flags may be asserted and the PHY still transmits correctly.

5 System-Level Implementation

This chapter provides integration information. This chapter is divided in the following sections:

5.1 Integrating IP in SoC

The IP is composed by a top-level verilog wrapper shell that instantiates a soft-core portion (represented on the product deliverables by synthesizable RTL and supported with synthesis constraints for its physical implementation) and a hard-macro portion that corresponds to a hard mixed-signal block.

The information below lists the steps to be considered to integrate the IP in your SoC:

1. Perform functional verification of your SoC with the IP Verilog behavioral models included.
2. For synthesis use the Synopsys IP constraints, .lib or .db timing models provided in the product deliverables. For further information consult timing model usage, synthesis and static timing analysis sections.
3. Simulate the SoC with the IP back-annotated gate-level netlists.
4. Validate signal-integrity using spice model
5. Follow the physical implementation requirements and guidelines.

5.2 Functional Verification

The product deliverables include the top-level IP wrapper (dwc_mipi_4_tx_dphy_ns.v), Verilog RTL for the soft macro (dwc_mipi_4_tx_dphy_ns_if.v) and a Verilog behavioral model of the hard macro (dwc_mipi_4_tx_dphy_ns_core_gtech.v). The Verilog RTL that represents the soft-macro portion of the IP, can be synthesized into a gate-level netlist by a synthesis tool. The Verilog behavioral model of the hard macro includes a digital part modeled by a netlist of generic (GTECH) gates and an analog non-synthesizable behavioral model.

For simulation purposes, the I/O driver strength (level) must be defined according to the transmission mode (Low-Power or High-Speed).

For proper Low-Power receiver detection, the testbench must assign driver strength using the following command:

bufif1 (pull0,pull1) #(TRISE,TFALL) (OUT, IN, ENABLE);

For proper High-Speed receiver detection, the testbench must assign driver strength using the following command:

bufif1 (supply0,supply1) #(TRISE,TFALL) (OUT, IN, ENABLE);

A definition example can be found on the quickstart testbench that is delivered within the PHY package.

5.2.1 Verilog Model Files and Simulators

The following table indicates the product deliverables directory that stores the files required for functional verification.

Table 5-1 Deliverables Directories

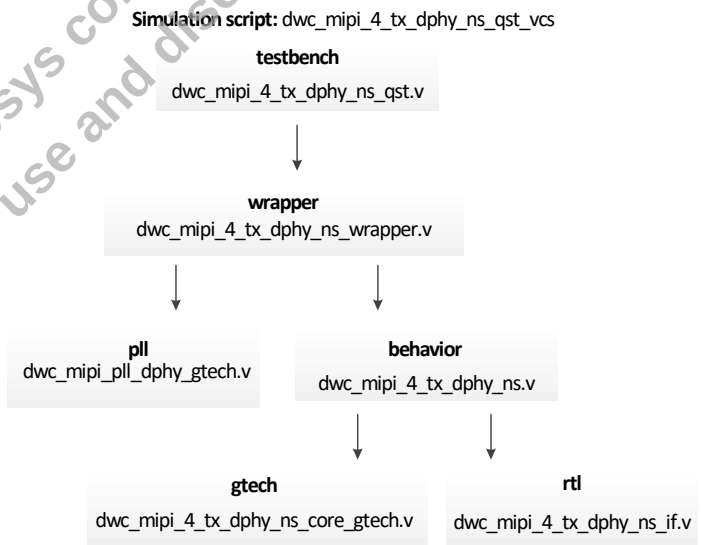
Directory	Description
./dphypll/behavior/	Gtech Verilog model – dphy pll add-on block
./macro/behavior	Top level wrapper (instantiates soft and hard macro)
./macro/behavior	GTECH Verilog model – hard macro
./macro/rtl	Synthesizable IP digital interface – soft macro
./macro/testbench	Quickstart testbench
./macro/testbench	RTL wrapper that instantiates single instance of the MIPI D-PHY and one PLL
./macro/sim	Example scripts to run quickstart and scan testbenches

Reference simulation scripts for the IP are provided for Synopsys VCS in the sim/ directory. The run_dwc_mipi_4_tx_dphy_ns_qst_{sim} scripts include the rtl and behavioral code for the soft and hard macro.

Note VCS X-propagation is not supported.

The following figure exemplifies the test environment components when running testbench script file.

Figure 5-1 Test Environment when running the Testbench Script File



5.3 Timing Model Usage

5.3.1 Clock Structure

The existing clocks in the extracted timing models are as follows:

- txbyteclkhs: [external] - High-speed Transmit byte clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. The maximum frequency for this clock is 312.5 MHz.

Table 5-2 summarizes the clocks and signal direction in the extracted timing models where:

- **External Port** displays the port in .lib where the clock is sourced or sinked.
- **External clock** displays the port in PHY where the clock is sourced or sinked.

Internal clock displays the clocks within the .lib created with clock and generated clock.

Table 5-2 External and Internal Model Clock Signals

	External Port	External Clock	Direction		Internal Clock
FUNCTIONAL	txclkesc_if	txclkesc	Input	→	
	cfgclk_if	cfg_clk	Input	→	
	txbyteclkhs_if	txbyteclkhs	Input	→	
	rxclkesc_lane0	rxclkesc_0	Output	←	lprxdoutlp0 lprxdoutlp1 lprxdoutulp0 lprxdoutulp1 rxclkesc_lp0 rxclkesc_lp1 rxclkesc_ulp0 rxclkesc_ulp1
SCAN	scanclk_if	scanclk	Input	→	

When performing static timing analysis, take care to properly define and observe the existing clocks to ensure that the delay of the clock trees are taken into consideration, providing a correct and accurate timing.

5.3.2 Clock Creation

Besides the existing clocks on the extracted timing models, the clocks documented below must be created for each mode of operation in the complete clock definition for the top-level MIPI D-PHY. The clock creation for each mode is as follows:

5.3.2.1 Functional Mode of Operation

```
create_clock [get_pins <DUTNAME>/mipi_if_inst/cfg_clk] -name cfg_clk -period 37
-waveform {0 18.5}
create_clock [get_pins <DUTNAME>/mipi_if_inst/txclkesc] -name txclkesc -period 50
-waveform {0 25}
```

```
create_clock [get_pins <DUTNAME>/mipi_if_inst/testclk] -name testclk -period 10.0
-waveform {0 5.0}
create_clock [get_pins <DUTNAME>/mipi_if_inst/txbyteclk] -name txbyteclkhs -period 3.2
-waveform [list 0.0 1.6]
create_clock [get_pins <DUTNAME>/I01DPHYCORE/lprxdoutlp0] -name lprxdoutlp0 -period 50
-waveform {0 25}
create_clock [get_pins <DUTNAME>/I01DPHYCORE/lprxdoutlp1] -name lprxdoutlp1 -period 50
-waveform {0 25}
create_clock [get_pins <DUTNAME>/I01DPHYCORE/lprxdoutulp0] -name lprxdoutulp0 -period
50 -waveform {0 25}
create_clock [get_pins <DUTNAME>/I01DPHYCORE/lprxdoutulp1] -name lprxdoutulp1 -period
50 -waveform {0 25}
create_clock [get_pins <DUTNAME>/I01DPHYCORE/txclk_word_clk] -name txclk_word_clk
-period 3.2-waveform [list 0.0 1.6]

create_generated_clock -divide_by 1 -source [get_pins
<DUTNAME>/mipi_core_inst/txclk_word_clk] [get_ports<DUTNAME>/txbyteclksrc] -name
txbyteclksrc

create_clock -name {updatepll} -period $updatepll_period -waveform [list 0.0 4.4]
[get_ports <DUTNAMEPLL>/updatepll]


set_propagated_clock [all_clocks]
```

Note

The edge relation above for these generated clocks is set for a cfg_clk frequency of 27MHz. For different cfg_clk frequencies, the clock creation needs to be revised accordingly, such that the generated clocks frequencies retain the same relation to their source cfg_clk as on the example constraints provided.

The following timing arcs are false and should be disabled when doing static timing analysis:

```
set_disable_timing    [get_cells -hierarchical *pulse_in_ff_reg] -from clear -to preset
set_disable_timing    [get_cells -hierarchical *pulse_in_ff_reg] -from preset -to clear
set_disable_timing    [get_cells <DUTNAME>/mipi_if_inst/I01TXIF/adc_done_reg] -from
clear -to preset
set_disable_timing    [get_cells <DUTNAME>/mipi_if_inst/I01TXIF/adc_done_reg] -from
preset -to clear
```

5.3.2.2 Scan Mode of Operation

```
create_clock [get_ports scanclk] -name "scanclk" -period 10 -waveform {0 5}
set_propagated_clock [all_clocks]
remove_generated_clock { <DUTNAME>/I01DPHYCORE/rxclkesc_0_lp0
<DUTNAME>/I01DPHYCORE/rxclkesc_0_lp1
<DUTNAME>/I01DPHYCORE/rxclkesc_0_ulp0
<DUTNAME>/I01DPHYCORE/rxclkesc_0_ulp1}
```

5.3.2.3 Multi-Mode Operation

Extracted timing models can be created for a single operation mode, the mono-mode model (Functional or Scan), or for multiple operation modes, the multi-mode model.

When multi-mode models are read into PrimeTime, all models are enabled by default. This means that PrimeTime accounts for all timing relations present on the model. It is critical that you select the intended mode to disable all timing constrains for the inactive modes.

This task is performed by using the set_mode command. For example:

```
/*SCANMODE*/
set_mode SCAN <DUTNAME>
/FUNCTIONAL/
set_mode FUNCTIONAL <DUTNAME>
```

After setting the mode, a report_mode command can be performed to ensure that the intended mode is enabled while all other modes are disabled.

5.3.3 Clock Groups

Table 5-3 documents clock groups and relations between them.

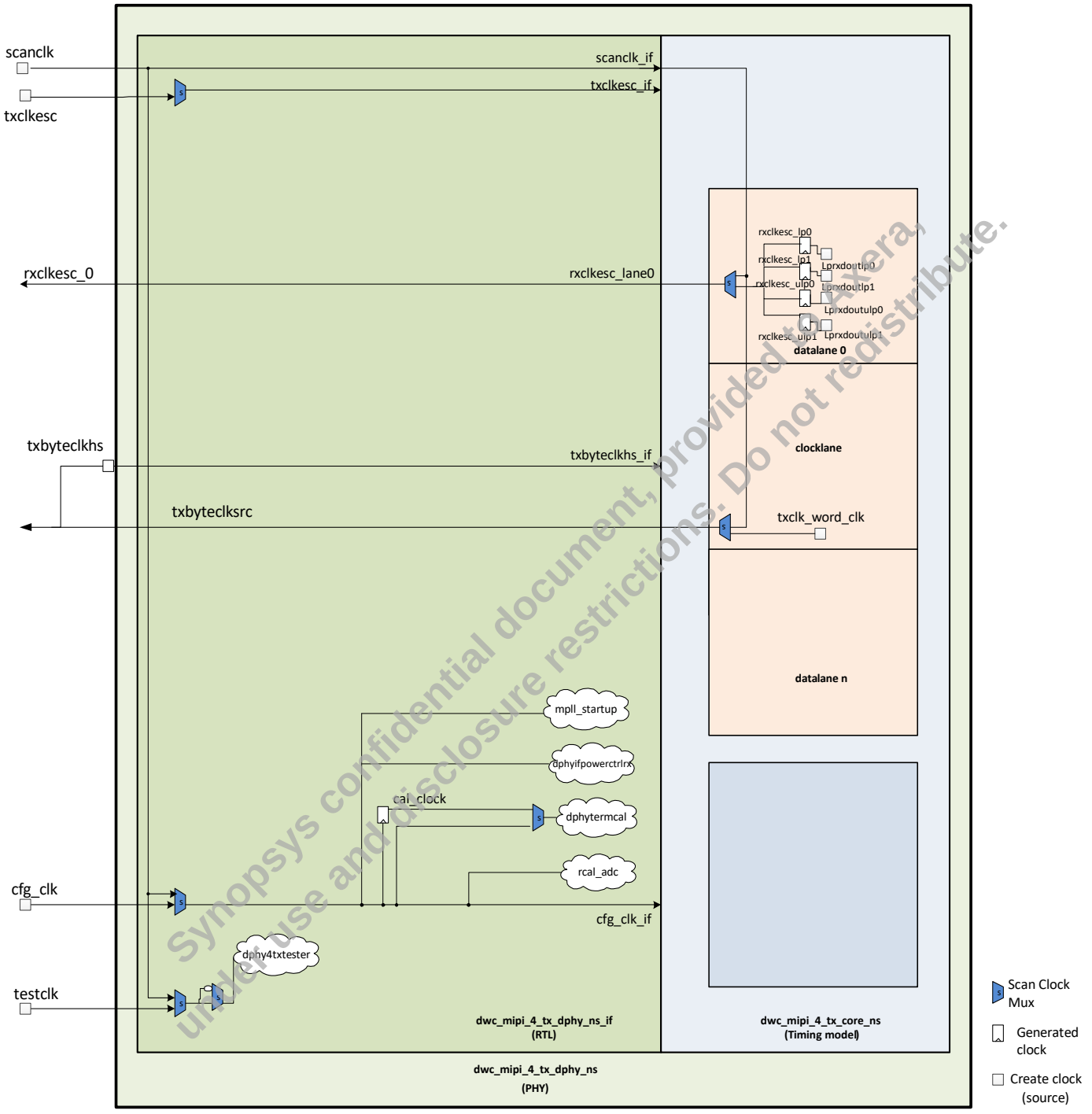
Note All clocks in clock group are synchronous to each other and asynchronous to all clocks of all other clock groups.

Table 5-3 Relation between Clock Groups

Clock Name	Creation point	Description	Clock group
cfg_clk	cfg_clk	config clocks	cfg_clk
cal_clock	mipi_if_inst/clkterm_mux/z	Termination calibration clock	
lprxdoutlp0	mipi_core_inst/lprxdoutlp0	Lane0 low power clock source	lane0_lprx
lprxdoutlp1	mipi_core_inst/lprxdoutlp1		
lprxdoutulp0	mipi_core_inst/lprxdoutulp0		
lprxdoutulp1	mipi_core_inst/lprxdoutulp1		
rxclkesc_lp0	mipi_core_inst/rxclkesc_lp0	Lane0 low power internal clock	
rxclkesc_lp1	mipi_core_inst/rxclkesc_lp1		
rxclkesc_ulp0	mipi_core_inst/rxclkesc_ulp0		
rxclkesc_ulp1	mipi_core_inst/rxclkesc_ulp1		
rxclkesc_0	rxclkesc_lane0	Lane0 low power output	
testclk	testclk	Test interface clock	testclk
txclkesc	txclkesc	LP-TX escape mode clock	txclkesc
scanclk	scanclk	Scan clock	scanclk
txbyteclksrc	mipi_core_inst/txclk_word_clk	txbyteclksrc core output	txbyteclksrc
txbyteclkhs	txbyteclkhs	Top level txbyteclkhs clock	txbyteclkhs

5.4 Clock Timing Model

Figure 5-2 dwc_mipi_4_tx_dphy_ns Clock Structure



5.5 Clock-Domain Crossing Cells

The following generic digital-cells, are primitive modules within the soft macro that are used to instantiate a specific digital cell that must not be logically optimized during synthesis.

These cells are used in CDC points in the soft macro. It is essential that these cells are processed correctly, not just synthesized as additional logic in the soft macro. Failure to do so creates glitch generating and re-convergent logic that causes issues.

Table 5-4 details the name and description of those cells, The BCM synchronizer designs are identified by synchronizer type.

Table 5-4 Synchronizer Cells

Module name	Function	Hand-instantiated cell Required?
DWbb_bcm21_scan	2-stage data signal synchronizer with support for cross-edge sampling	Yes
DWbb_bcm21	2-stage data signal synchronizer	Yes
gen_sync_rst	Asynchronous assert, synchronous de-assert reset synchronizer	Yes
gen_mux	2 input MUX	Yes
DWbb_bcm41_scan	2-stage data signal synchronizer with support for cross-edge sampling. Instantiates DWbb_bcm21_scan	No
DWbb_bcm41	2-stage data signal synchronizer. Instantiates DWbb_bcm21	No
gen_sync	2-stage data signal synchronizer with support for cross-edge sampling. Instantiates DWbb_bcm21_scan	No
static_pulse_catcher	Static signals pulse catcher. Instantiates DWbb_bcm41	No
gen_sync_bus	Bus data signal synchronizer . Instantiates DWbb_bcm41_scan	No

To prevent these modules from being optimized during synthesis, you can either replace the contents of these modules with an instantiation of the appropriate standard cell from a digital library, or synthesize each module stand-alone with a restricted library, so that only the correct cell is selected by the tool. In both cases, a "set_size_only" attribute must be applied to prevent re-optimization of the instance during the complete soft macro synthesis.

Meta-stability behavior is modeled in the synchronizers and can activated by defining the macro REGRESSION during simulations.

For proper verification, the reset synchronizer master cells should be defined with the following instruction:

```
*  set_parameter reset_synchronize_cells "<product_name_prefix>_gen_sync_rst".
```

5.6 Synthesis

The IP digital interface block is delivered as soft macro (RTL), meaning that it may be synthesized alone or with the rest of the RTL of the MIPI controller and SoC.

5.6.1 Constraints

The design constraints format from Synopsys, provided as .tcl files, describes the design intent and surrounding constraints for synthesis, clocking, timing, power, test, and environmental and operating conditions. Typically for synthesis and timing purposes, .tcl files constrain the input and output delays of interface pins, clock definitions, and any timing path exceptions in the design, such as false paths or multi-cycle paths.

In most cases, the soft macro is synthesized with Synopys Controller, or third party controller, RTL so timing constraints are inferred from the adjoining logic and from the IP lib timing model to which the soft macro is connected. When synthesizing the soft macro as an individual block, signals on the SoC interface must be constrained so that sufficient time is budgeted for the adjoining logic to be connected later.

The hard macro should be instantiated as a black box as the .lib/.db timing models provide only timing constraints for synthesizing logic to which the hard macro interfaces with.

5.6.1.1 Constraints Variables

Synthesis Design Constraints constraints provided with the IP, defines conditional variables to handle constraints for standalone or conjunction synthesis. When using Synopsys Controller using CoreConsultant environment these variables are automatically set, however for third party Controller settings should be applied manually.

- Enabling variable “snps_mipi_top_hier” disables additional constraints (false_paths, boundary, input and output delays, …) not needed when performing synthesis in conjunction with other logic, for example Controller.
- Enabling variable “lp_tx_on” enables additional constraints to allow Low Power Transmission. By default Low Power transmission is only required for DSI applications.

Note For complete clock definition refer to “Clock Creation” on page 92

5.6.2 Synthesis Settings

To ensure correct synthesis constraints are applied for synthesizable IP set variable dont_touch_nets_with_size_only_cells and hdlin_keep_signal_name user to true in synthesis scripts.

Note You can safely disable any clock gating check performed in the D-PHY soft macro by the synthesis/STA tool (not counting any integrated clock gating cells that you may have inserted automatically during synthesis). Synopsys’ soft macro RTL does not require a clock gating check to be met.

5.7 Static Timing Analysis

For Static timing analysis of the DUT use the .lib timing models.

5.7.1 Static Timing Analysis Guidelines

5.7.1.1 Guidelines for Running STA of the DUT

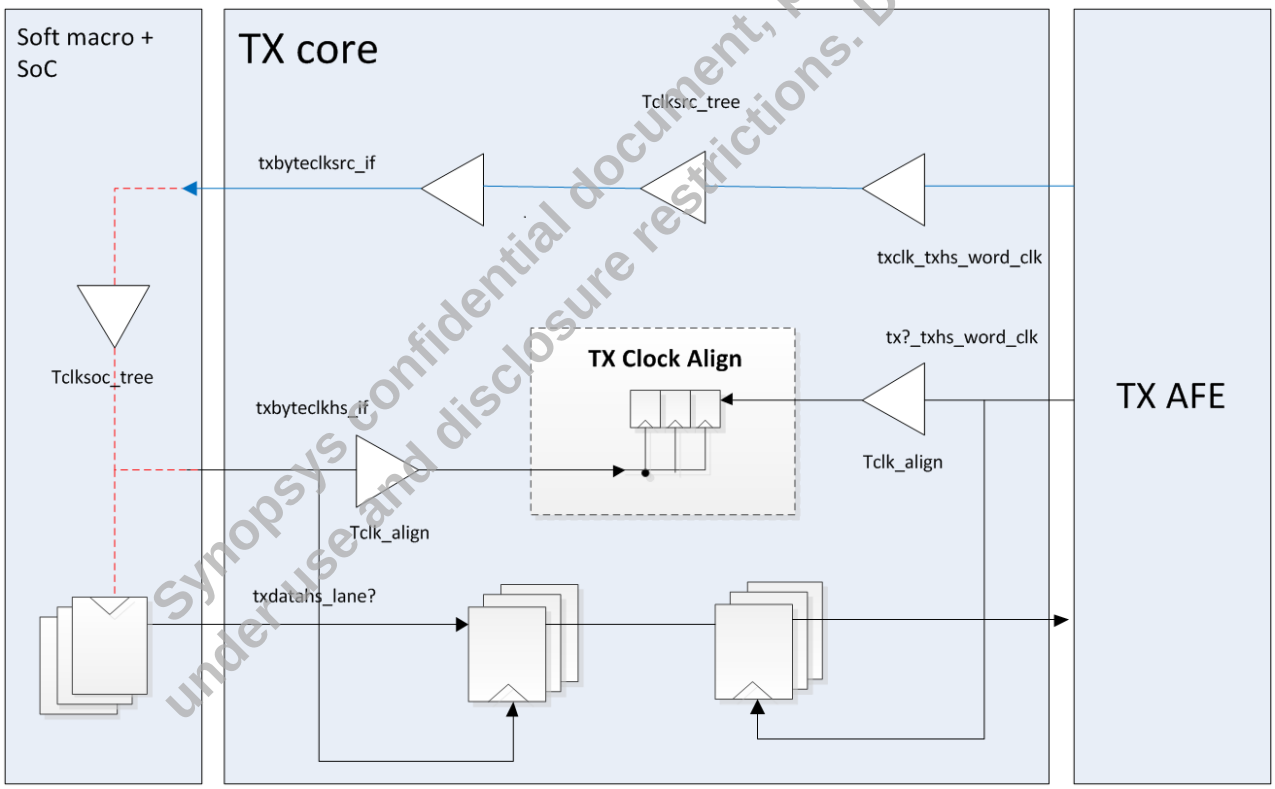
The guidelines for running STA of the DUT are as follows:

1. Define all the input and internal clocks using create_clock. For more information see "Clock Timing Model" on page 96
2. Define generated clocks on all IP core output clocks. You are responsible for any additional timing derate added on this verification for added timing margin on the integration.
3. Set all clocks and generated clocks as propagated clocks: *set_propagate_clocks [all_clocks]*

5.7.2 Clock Alignment Mechanism Requirements

Figure 5-3 illustrates the TX clock alignment mechanism and datapath.

Figure 5-3 TX Clock Alignment Mechanism and Datapath



TX 8-bit parallel data is transferred from the input txbyteclkhs_if to the internal tx?_txhs_word_clk clock domain. These 2 clocks are generated from the same PLL source clock and are the same frequency but asynchronous in phase.

TX clock alignment function is triggered when exiting a ULPS state or at power-up. The ASIC txbyteclkhs_if clock is aligned to the internal tx?_txhs_word_clk to provide a ½ cycle of a setup and hold margin for 8UI clock. The alignment uncertainty is 2UI, leading to a final alignment from 4UI to 6UI.

For a given technology process corner, variation in voltage and/or temperature (VT) can result in variable delay on the txbyteclkhs_if clock path delay in the soft-macro.

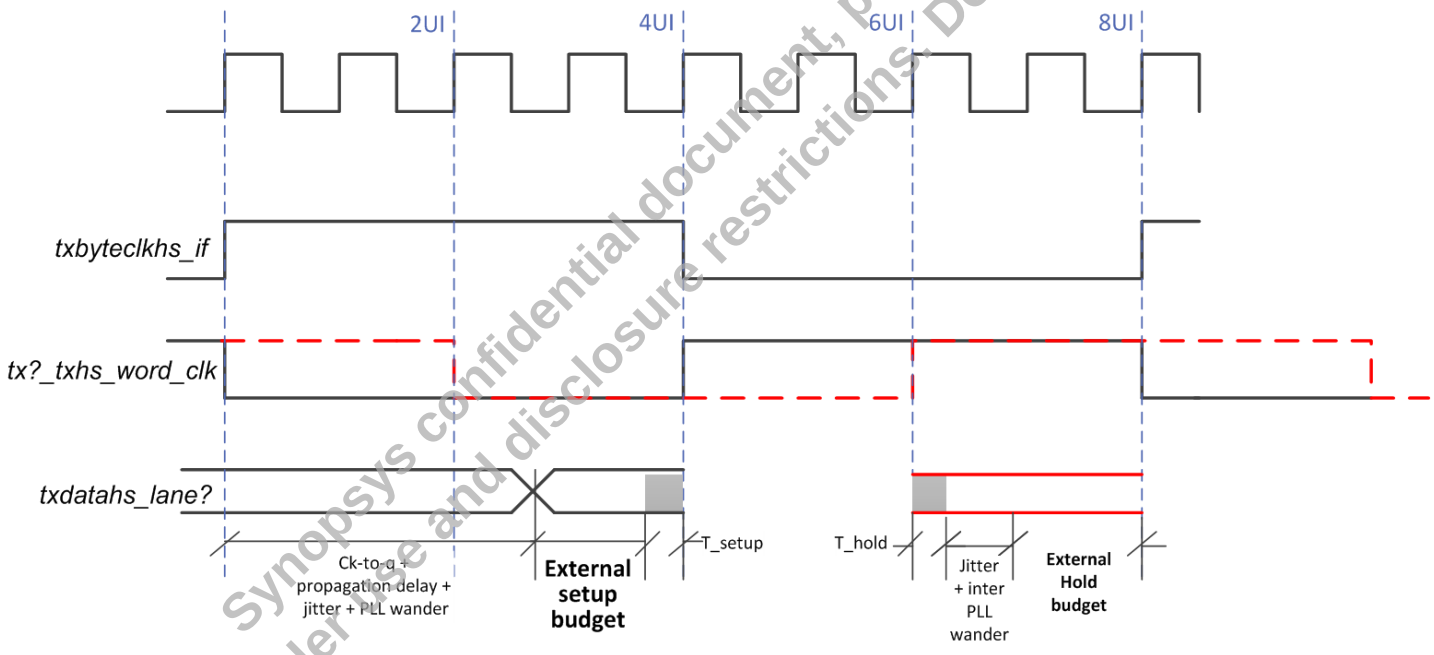
If not constrained, this clock delay variation in voltage and/or temperature (VT) can lead to potential timing path violations on TX data-path transfer between txbyteclkhs_if and tx?_txhs_word_clk within the CORE (hard-macro) and may possibly require periodic clock-align procedure to correct any wrong alignment resulting from a big VT skew after the last clock align procedure.

The txbyteclkhs_if clock path delay variation can be described as the difference between the min and max propagation delays across VT within a corner through the following:

- The clock tree path from the output of the CORE txbyteclkhs_if, through the soft-macro and Controller clock logic and feeds back into the CORE txbyteclkhs_if input along with txdatahs_lane?.
- txclk_txhs_word_clk clock path from the PLL source to the CORE output pin txbyteclksrc_if.

Figure 5-4 illustrates the TX clock delay and margin.

Figure 5-4 TX Clock Delay and Margin



TX clocks are aligned to ½ cycle with a variation of 0 to 2 UI.

The final alignment does not affect clock delay margin calculation.

You are required to have correct clock names (matching clocks in constraints).

SoC integrator shall perform STA analysis to confirm the SoC variation in VT.

- SS corners

- Take all SS corners and report the maximum delay from <DUTNAME>/mipi_core_inst/txbyteclksrc_if to <DUTNAME>/mipi_core_inst/ txbyteclkhs_if for each VT corner
- Take all SS corners and report the minimum delay from <DUTNAME>/mipi_core_inst/txbyteclksrc_if to <DUTNAME>/mipi_core_inst/ txbyteclkhs_if for each VT corner
- Report the difference between the maximum and the minimum path delay

- FF corners
  - Take all FF corners and report the maximum delay from <DUTNAME>/mipi_core_inst/txbyteclksrc_if to <DUTNAME>/mipi_core_inst/ txbyteclkhs_if for each VT corner
  - Take all FF corners and report the minimum delay from <DUTNAME>/mipi_core_inst/txbyteclksrc_if to <DUTNAME>/mipi_core_inst/ txbyteclkhs_if for each VT corner
  - Report the difference between the maximum and the minimum path delay

The maximum variation at SoC, for a given process corner, shall be lower than the margin provided on Table 5-5.

Table 5-5 txbyteclkhs_if Clock Delay Margin Analysis

Operating Speed (Mbps)	Margin (ps)
2500	500

5.8 Quickstart Testbench Description

The quickstart testbench allows testing the IP in all operation modes (see "Operating Modes" on page 61) allowing the configuration of the IP through the test and control interface, initialization, high-speed transfer mode, Escape mode (low power data transmission, remote trigger, ultra low power state) and turnaround. To help in understanding the testbench and to facilitate the verification, a self-checking system is built into the testbench, meaning that any error will automatically be displayed for your awareness. The testbench enables you to perform a quick verification and to ease IP integration into your top-level system, and into more complex testbenches. This quickstart testbench can be the basis for the creation of different verification environments.

The following list details the quickstart testbench minimum set of tests:

- LPDT-TX: All lanes
- ULPS-TX: All lanes
- TRIGGER-TX: All lanes
- HS-TX: All lanes
- Turnaround on Lane 0: TX → RX

- LPDT-RX on Lane 0
- ULPS-RX on Lane 0
- TRIGGER-RX on Lane 0
- Turnaround on Lane 0: RX → TX
- LPDT-RX on Lane 0

This IP model and testbench does not represent an example of exhaustive IP testing. The verification of the release package is only with Synopsys simulator VCS. For issues related to IP model usage with other simulators, contact Synopsys support.

5.9 Gate-level System Verification

To evaluate IP after being synthesized and placed and routed, the IP gate-level netlist and SDFs must be used for proper back-annotation.

The following table describes each portion of models for gate-level simulations and indicates the product deliverables directory where the portion is stored.

Table 5-6 Gate-level Simulation Directories

Directory	Description
./dphypll/behavior/	Unencrypted gate-level model – dphy pll add-on block
./dphypll/timing/sdf	Standard Delay Format (SDF) files for dphy pll add-on block
./macro/behavior	Unencrypted gate-level model – hard macro
./macro/behavior	Verilog model (hard + soft macro)
./macro/rtl	Synthesizable IP digital interface – soft macro
./macro/timing/sdf	Standard Delay Format (SDF) files

To run a simulation, add the *sdf_annotate* command to the testbench as follows:

$sdf_annotate("../timing/sdf/dwc_mipi_4_tx_dphy_ns_core_<corner>_<extraction>_..sdf",dwc_mipi_4_tx_dphy_ns_qst.DUT.i01dphy.mipi_core_inst ,,,"MAXIMUM");

The following issues may occur when running gate-level simulations without SDFs.

- For gate-level simulations, SDF back-annotation of the gate delays is required. Due to non-trivial clocking structures within the IP core, a zero-time or unit-delay simulation of the gate-level model would be non-functional due to race conditions in the Verilog execution caused by simulator event ordering.

- The .sdf files simply represent the hardware's timing. These files are generated at worst-case and best-case process/temperature/voltage corner. However, they are not sufficient for replacing static timing analysis. Synopsys has validated the IP core internal timing, and timing for the IP core interfaces are provided in the .lib timing models. Validate these timings using STA tools, not Verilog simulation.

Note

- Do not use .lib files to generate top SDF for the SoC, because the resultant SDF will contain references to internally generated clocks that are not visible at the top level. To generate SDF for the Soc, generate SDF separately for the SoC portion that excludes the hard macro.
- For gate-level simulations, it is recommended that all reset signals from the involved PHY and PLL add-on blocks are pulsed at simulation start.
- During gate-level simulations, if the PLL SoC interface is not used for configuring the PLL, a pulse should be given on shadow_clear signal to avoid a X simulation artifact that can be visible on this scenario where this interface is not used.

Signal Integrity Simulations – IBIS Model

IBIS model is provided in the standard release package. It should be used for the purpose of channel simulation or transient analysis with fast runtime. IBIS models use lookup tables such as [GND Clamp], [Power Clamp], [Pulldown], [Pullup] to model the input and output I-V characteristics. The lumped capacitance values at TX and RX are modeled in the [C_comp] field.

IBIS model is derived from original SPICE circuit netlist (DUT), with some components expressed as post-layout extractions. After performing AC, DC and transient simulations on the DUT, results are extracted and organized into IBIS model.

Note

IBIS model itself does not include random jitter or deterministic jitter.
Return loss simulation is not the intended use of IBIS model.

5.10 Power Integrity Simulations

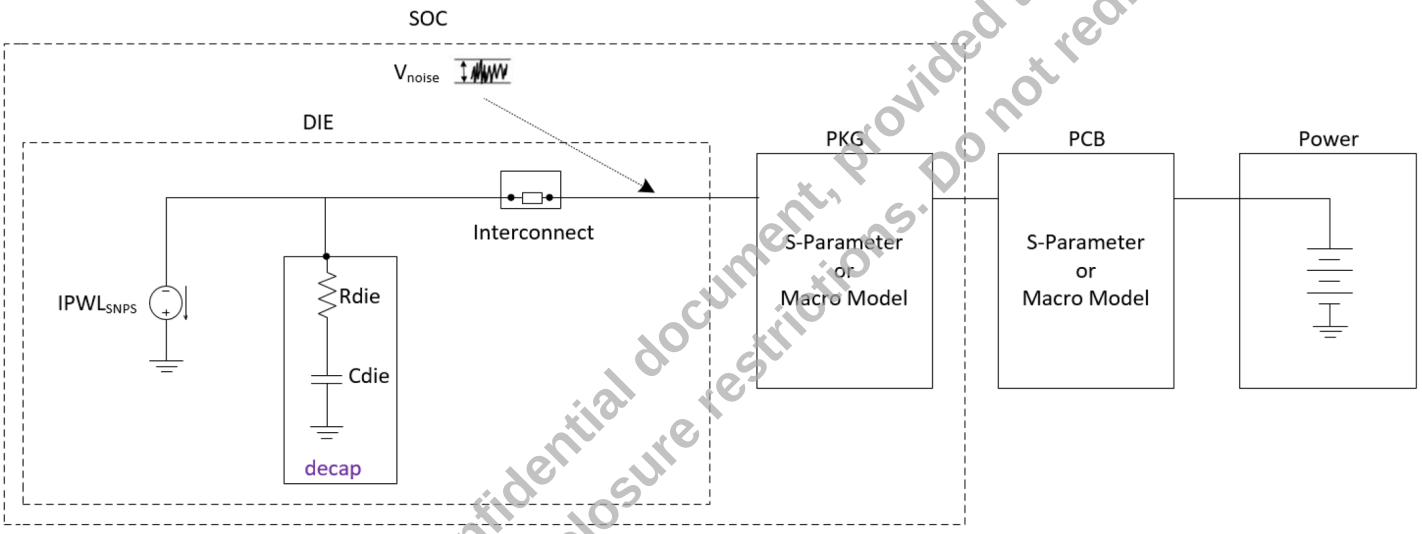
You need to run a power integrity simulation to ensure the package and board PDN design provide low impedance path for supply current, such that ripple at various power rails meets IP specifications.

The IP package waveforms folder includes DPHY hard macro current waveforms, along with on-die power grid equivalent capacitance and resistance (Cdie and Rdie, respectively) for power delivery network (PDN) simulations.

You must build the PDN (integrator target package, integrator target PCB, on-die) and testbench, preparing it for simulations (time and frequency domain). Ripple at package die bumps is measured and compared against specs. Maximum pk-pk tolerated noise is ± 3% of supply, see "Analog Voltage Supply (vph/vp) and Ground (gd)" on page 152.

Figure 5-5 shows the reference schematics for a typical simulation.

Figure 5-5 Power Delivery Network (PDN) Testbench



The next factors affect ripple, and should be optimized to meet performance requirements:

- Package loop inductance – loop inductance from die power and ground bumps to BGA power and group pins. This inductance should be minimized.
- Series inductance from BGA to PCB power ground island where board decoupling capacitors are attached. This inductance is associated with PCB vias, traces that connect BGA pins to power and ground island where decoupling capacitors are mounted. This series inductance add on top of package inductance and are a significant contributor to PDN noise that should be minimized.
- Equivalent series inductance including mounting inductance of PCB decoupling capacitors, especially high speed decoupling capacitor. This inductance has second order effect on PDN noise—pay attention to that when doing PDN optimization.
- Usually high ripple is due to anti resonance between on chip decoupling capacitance and package/PCB series inductance, which results in impedance peaks at certain frequency. AC frequency sweep helps to identify such peak and provides useful insight on optimization.

In the specific case of digital core supply (vdd), PDN analysis must include contribution of R/Cdie and PWL from all vdd blocks shared with DPHY hard macro. This is true for Soc oriented (SOC and DPHY soft macro) and IP oriented (DPHY soft macro), see "SoC/IP vdd/vss Power Domain" on page 155.

Note

Contact Synopsys support in case of:

- interconnect channel is not meeting the DPHY specification
- integrator fails to bound power supply noise to specified limits using PDN and current profiles

6 Characterization and Production Tests

The DWC MIPI D-PHY v1.2 Tx 4L (PHY) has a set of features that can be used during characterization stage and production testing.

This chapter is divided in the following sections:

Note During testing all inputs should be kept low except inputs testclr that default value is high (reset of tester interface) and cfg_clk that needs to be always available. These values should be used unless other values are explicitly mentioned in the test procedure

6.1 Scan Mode

This section describes the supported Scan Mode of operation.

6.1.1 Overview

The PHY provides a Scan interface for stuck-at fault of both hard and soft PHY macro.

All logic supports scan testing (no particular cells are left out of DFT strategy).

An ATPG model of the digital portion of the PHY is provided that can be used during ATPG pattern generation to stitch the scan chains together (refer to integration scenarios on sub-section below) and test them during chip-level scan testing.

If scan in not being implemented in the PHY, tie all scan pins to 1'b0.

If other blocks surrounding the MIPI D-PHY will be in scan mode and the MIPI D-PHY is not, causing random toggling at the MIPI D-PHY inputs, then the MIPI D-PHY should be put in shutdown mode.

If the MIPI D-PHY is in scan mode, all other inputs beside scan_mode are part of the inputs toggling during scan pattern generation.

For details about the Scan related signals functionality descriptions, see Scan Interface Signals in the chapter Signal Descriptions in MIPI D-PHY v1.2 Tx 4L for TSMC 12-nm FFC/1.8V *Reference Manual.*

6.1.2 Scan Modes

Before entering into scan mode, the PHY scan reset should be set. After some scan clock cycles, PHY should be set in scan mode and after some scan clock cycles, PHY scan reset should be released.

In Scan mode, all analog blocks are powered down, that is, power consumption of the analog blocks correspond only to their respective leakage current.

To prevent propagation of logic X's in the scan chain, the outputs of all the analog blocks feeding the digital scannable logic are overridden to known states.

The PHY .lib files include all appropriate timing arcs to support Shift and Stuck-at Capture modes.

Note When not in scan mode, the scan clocks must not toggle and scanrstz should be tied low.

6.1.3 Scan Functionality Details

This section details scan functionality in the PHY.

6.1.3.1 Scan Chains

All scan chains

- have a maximum of 100 flip-flops,
- are positive-edge triggered, and
- are terminated with lockup latches.

6.1.3.2 Scan Clock

The scan clock maximum frequency is 100 MHz.

All clock outputs from the PHY, have a scan clock input muxed on them when in scan mode.

6.1.3.3 Scan Resets

All resets (primary input resets or internally generated resets) are overridden to primary scan reset.

6.1.3.4 ATPG Vectors

When running scan vector simulations, use the full gate-level netlist. The scan netlist provided in the deliverables includes a scan model of the analog portion of the design only and should be used for ATPG generation in Tetramax or equivalent tool. When running scan vector simulations, use the full behavioral analog model within the gate-level netlist and sdf back annotation.

6.2 Silicon Characterization Tests

The PHY's operation and its conformance with the specification from the MIPI Alliance can be checked through a suite of tests defined by the University of New Hampshire's Interoperability Laboratory (UNHIOL) as part of the MIPI Alliance Test Program.

The MIPI Alliance Test Program (D-PHY Physical Layer Conformance Test Suite) and the correspondent Software tool developed by the UNH-IOL may be downloaded from the MIPI Alliance group—

www.mipi.org.

If the tests pass, they provide a reasonable level of confidence that the tested device will properly operate in many MIPI environments, and possibly in all, if the interfacing device is also conformant.

Synopsys uses these tests as part of its internal testchip silicon characterization program for the PHY and recommends using similar approach in addition to interoperability tests with multiple hosts or/and devices. For additional testing details contact your local Synopsys AE.

To perform all tests described in the CTS document (MIPI Alliance Test Program, D-PHY Physical Layer Conformance Test Suite Version v1.2 CTS version 1.0, the system should allow access to all the PPI signals of the PHY.

Due to the extensive list of signals in the PPI, Synopsys strongly recommends multiplexing similar signals from different lanes and providing software access to the static/quasi-static signals to save chip I/Os.

The following list of tests is supported:

- Low Power loopback between data lane 0 and all other data lanes
- PHY-2-PHY Low Power Loopback
- PHY-2-PHY HS loopback

6.2.1 Low Power External Loopback

This test enables a functional verification of the LP driver and receiver present in the data lanes within the same D-PHY using for this purpose this single D-PHY instance.

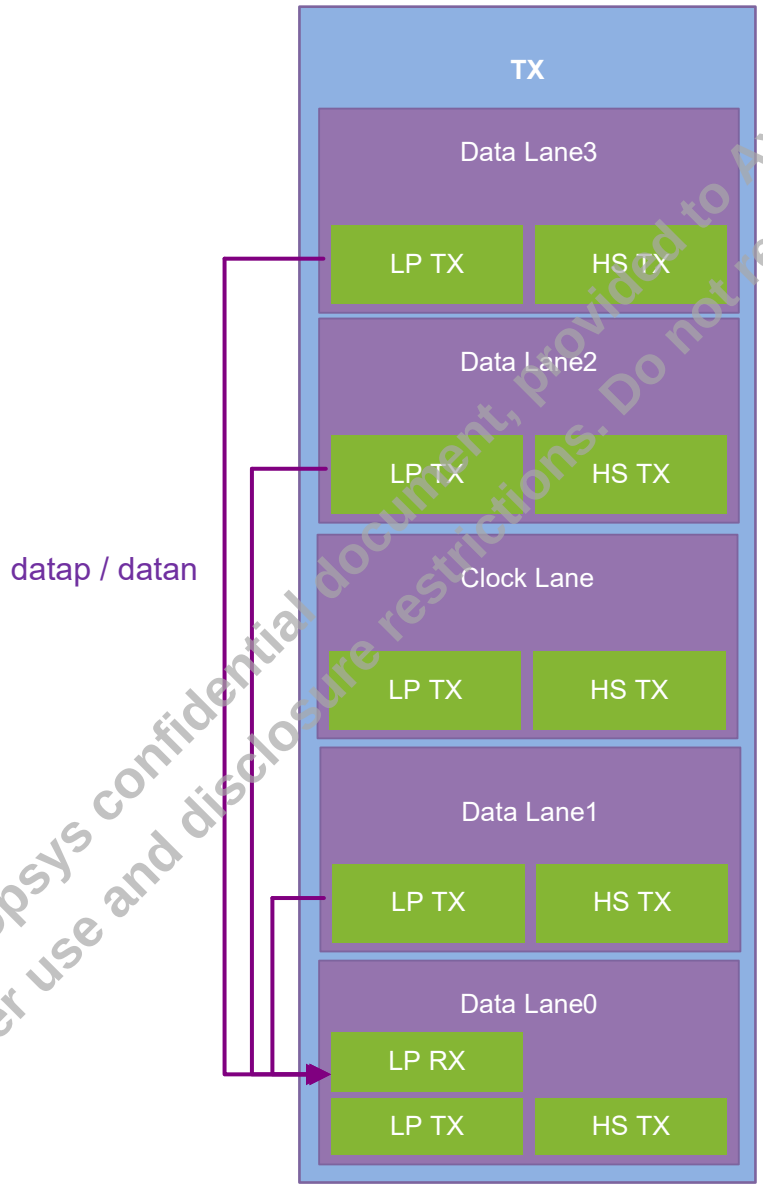
External connections can be established between lane0 and other data lanes to setup this test mode as Lane 0 is the only lane that supports LP RX. In this context it can be used to receive the LP data transmit by the LP TX on the other lanes.

It is not allowed to externally loopback between LP TX and LP RX on lane0.

PLL is not required to be operating for Low Power Loopback test modes.

With a single LP RX on lane 0, this needs to be performed with one lane connecting to lane 0 at a time.

Figure 6-1 Low Power Loopback



For these low power loopbacks there is not auto-checking mechanism.

The low-power received data needs to be consistent with the transmitted data.

Low power loopback test uses clock Escape mode Transmit Clock txclkesc (2 MHz-20MHz range).

LP loopback consists in sending TX patterns using PPI interface of datalane0 to other lanes (0, 1, 2 or 3).

The following example details an LP loopback.

Setup sequence:

1. Set basedir_0 = 1’b1 (boot lane0 into LP-RX mode)
2. Enable lane0 (enable_0 = 1'b1) and the other lane in test
3. Power up the PHY as described in “Start-Up Sequence” on page 78
4. Wait until PHY reaches STOPSTATE (Consider 500us as maximum wait time)
5. Use ULP/LP-TX PPI interface from the lane connecting to lane 0 and verify the results on ULP/LP-RX PPI interface from lane 0
   - Apply txclkesc signal with appropriate frequency.
     - The frequency may range from 2 MHz to 20 MHz corresponding to 1 Mbps or 10 Mbps LP operations respectively.
   - txlpdtesc_n and txvalidesc_n to high.
   - txdataesc_n[7:0] to 8'b11111111.
   - txrequestesc_n to high.
6. [**Measure 1**]
7. [**Measure 2**]

Measure:

1. Check LP-RX outputs in tester interface or on PPI interface of the lane 0 to confirm the received pattern
2. The LP related error signals on the PPI interface can also be checked as pass/fail criteria

The low power loopback test setup can be used to verify a whole different set of cases using for it the same setup:

- LP data transmission/reception for any desired pattern through txdataesc_n[7:0] and rxdataesc_0[7:0]
- Escape mode triggers verification through txtriggeresc_n[3:0] and rxtriggeresc_0[3:0]
- Escape mode ULPS transitions

6.2.2 PHY-2-PHY Low Power Loopback

This test enables a functional verification of the LP transmitter present in the data lanes as exercising an external receiver D-PHY.

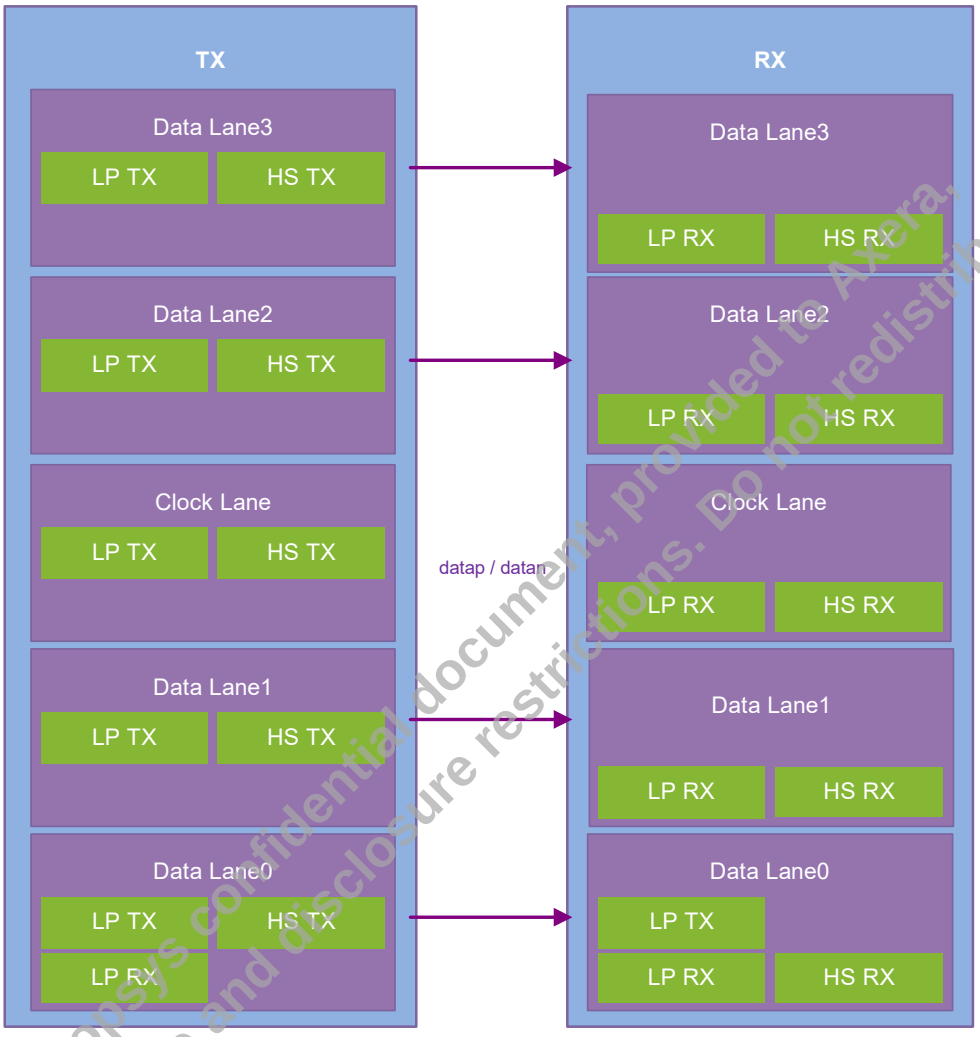
External connections can be established between transmitter and receiver D-PHY as in normal mission mode to setup this test mode.

PLL is not required to be operating for Low power loopback test modes.

Connection between PHYs is done external to MIPI D-PHY.

On this test, data is exercised from LP TX on the transmitter PHY to the LP RX on the receiver PHY.

Figure 6-2 PHY-2-PHY Low Power Loopback



One example test sequence is described below.

Setup sequence:

1. Enable lane0 and all other connected lanes between both TX and RX PHYs
2. Power up both TX and RX PHYs (Power up the TX PHY as described in "Start-Up Sequence" on page 78)
3. Wait until PHYs reach STOPSTATE (Consider 500us as maximum wait time)
4. Use ULP/LP-TX PPI interface from TX PHY and verify the results on ULP/LP-RX PPI interface from RX PHY

- On TX PHY
  - Apply txclkesc signal with appropriate frequency.
    - The frequency may range from 2 MHz to 20 MHz corresponding to 1 Mbps or 10 Mbps LP operations respectively.
  - txlpdtesc_n and txvalidesc_n to high.
  - txdataesc_n[7:0] to 8'b11111111.
  - txrequestesc_n to high.
- On RX PHY
    - [**Measure 1**]
    - [**measure 2**]

Measures:

1. Check LP-RX outputs in tester interface or on PPI interface of the active lanes to confirm the received pattern.
2. The LP related error signals on the PPI interface can also be checked as pass/fail criteria for the scenario exercised.

This PHY-2-PHY low power loopback test can be used to verify different sets of cases using the same setup:

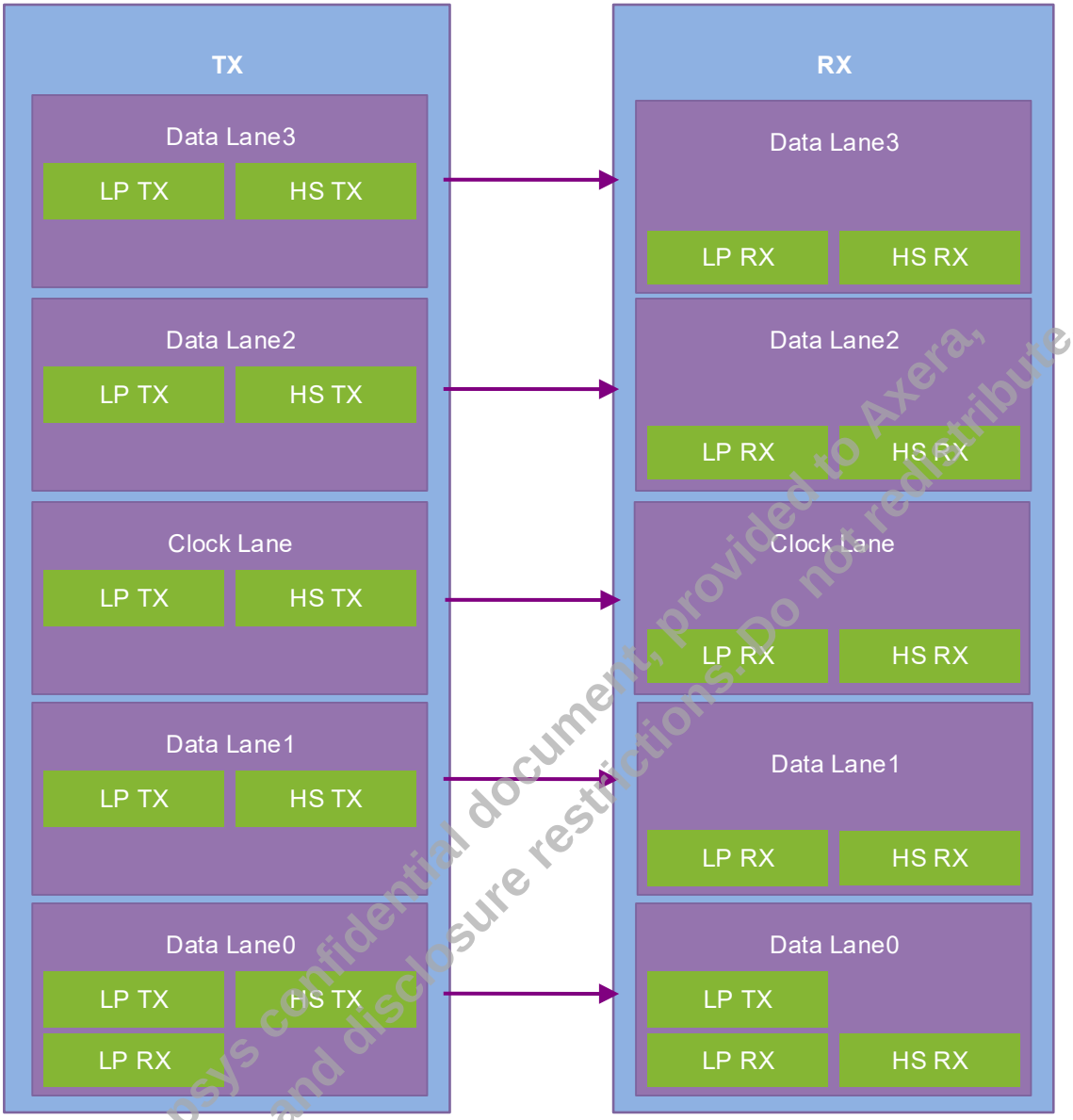
- LP data transmission/reception for any desired pattern through txdataesc_n[7:0] and rxdataesc_n[7:0]
- Escape mode triggers verification through txtriggeresc_n[3:0] and rxtriggeresc_n[3:0]
- Escape mode ULPS transitions

6.2.3 PHY-2-PHY High Speed Loopback

This test can be exercised through the usage of an external D-PHY RX macro and the connections between transmitter and receiver PHY are done externally.

This test enables a functional verification of the HS-TX transmitters and PPI interface (PHY-CTRL). Data is expected to be exercised through the D-PHY TX PPI interface and verified at D-PHY RX PPI interface.

Figure 6-3 PHY-2-PHY High-Speed Loopback



The following setup sequence provides an example for direct HS testing.

Refer to the D-PHY RX databook for instructions on how to setup D-PHY RX in HS direct mode.

Setup sequence

1. Enable TX PHY and RX PHY in direct HS setting hsdirect signal of Test Code 0x0c
2. Power up the TX PHY as described in "Start-Up Sequence" on page 78
3. Power up the RX PHY (as described in the corresponding MIPI D-PHY RX databook section PHY-2-PHY High Speed loopback) in HS direct mode
4. Set txrequesthsclk = 1'b1 and txrequestdatahs_n = 1'b1

5. Wait for txreadyhs assertion.
6. Change txdatahs_n at posedge txbyteclkhs until the completion of the desired burst.
7. On D-PHY RX, check PPI signals corresponding to HS data reception. The received data can also be checked against a checker built outside the PHY.

6.2.4 Testability Signals

The following table describes the testability signals.

Note

- All - CTS / Silicon Characterization or Production Test
- CTS / SC - CTS / Silicon Characterization
- PT - Production Test

Table 6-1 Testability Signals

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
Analog Signals						
rext		N/A - no additional GPIO is required			Input/Output	
atb		ALL	Make it observable		Input/Output	
MIPI Interface Signals						
datapN		N/A - no additional GPIO is required			Input/Output	
datanN		N/A - no additional GPIO is required			Input/Output	
clkp		N/A - no additional GPIO is required			Input/Output	
clkn		N/A - no additional GPIO is required			Input/Output	
System Control Signals						
cfg_clk		ALL	SoC Clock Source	Clock	Input	52 MHz

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
shutdownz	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
rstz	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
hsfreqrange[6:0]	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
cfgclkfreqrange[7:0]	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
refclk		ALL	SoC Clock Source	Clock	Input	64 MHz
forcepll	ALL		Control by SoC register (muALL needed) *		Input	
lock	ALL		Make it observable		Output	
Common PPI Signals						
txskewcalhs	ALL		Control by SoC register (muALL needed) *	txbyteclkhs	Input	
txbyteclkhs		ALL	Connected to tALLbyteclksrc	Clock	Input	312.5 MHz
txbyteclksrc		ALL	Connected to tALLbyteclkhs	Clock	Output	
txclkesc		ALL	SoC Clock Source	Clock	Input	20 MHz
Clock Lane PPI Signals						
txrequesthsclk	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
txulpsclk	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
txulpexitclk	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
stopstateclk	ALL		Make it observable	Asynchronous	Output	
enableclk	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
ulpsactivenotclk	ALL (debug)		Make it observable	Asynchronous	Output	
Data Lane N PPI Signals						
txdatahs_N[7:0]	ALL (additional logic needed to transmit HS BURST)		Control by SoC register (muALL needed) *	txbyteclkhs	Input	
txrequestdatahs_N	ALL		Control by SoC register (muALL needed) *	txbyteclkhs	Input	
txreadyhs_N	ALL		Make it observable	txbyteclkhs	Output	
txrequestesc_N	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
txlpdtesc_N	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
txulpsesc_N	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
txulpsexit_N	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
txtriggeresc_N[3:0]	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
txdataesc_N[7:0]	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
txvalidesc_N	ALL		Control by SoC register (muALL needed) *	txclkesc	Input	
txreadyesc_N	ALL		Make it observable	txclkesc	Output	
rxclkesc_0		ALL	Make it observable	Clock	Output	20 MHz
rxlpdtesc_0	ALL		Make it observable	rxclkesc_0	Output	
rxulpsesc_0	ALL		Make it observable	rxclkesc_0	Output	
rxtriggeresc_0[3:0]	ALL		Make it observable	rxclkesc_0	Output	
rxdataesc_0[7:0]	ALL		Make it observable	rxclkesc_0	Output	
rxvalidesc_0	ALL		Make it observable	rxclkesc_0	Output	
turnrequest_0	ALL (debug)		Control by SoC register (muALL needed) *	txclkesc	Input	
direction_0	ALL (debug)		Make it observable	Asynchronous	Output	
turndisable_0	ALL (debug)		Control by SoC register (muALL needed) *	Asynchronous	Input	
forcerxmode_0	ALL (debug)		Control by SoC register (muALL needed) *	Asynchronous	Input	
forcetxstopmode_N	ALL (debug)		Control by SoC register (muALL needed) *	Asynchronous	Input	
stopstatedata_N	ALL		Make it observable	Asynchronous	Output	

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
enable_N	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
ulpsactivenot_N	ALL		Make it observable	Asynchronous	Output	
erresc_0	ALL		Make it observable	rxclkesc_0	Output	
errsyncesc_0	ALL		Make it observable	rxclkesc_0	Output	
errcontrol_0	ALL		Make it observable	txclkesc	Output	
errcontentionlp0_0	ALL		Make it observable	txclkesc	Output	
errcontentionlp1_0	ALL		Make it observable	txclkesc	Output	
basedir_0	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
Test Interface Signals						
testdin[7:0]	ALL		Control by SoC register (muALL needed) *	testclk	Input	
testdout[7:0]	ALL	ALL	Make it observable	testclk	Output	
testen	ALL		Control by SoC register (muALL needed) *	testclk	Input	
testclk	ALL		Control by SoC register (muALL needed) *	Clock	Input	100 MHz
testclr	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
IO continuity Signals						
cont_en	ALL		Control by SoC register *	Asynchronous	Input	

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
cont_data[10:0]	ALL		Make it observable	Asynchronous	Output	
BIST Signals						
biston	ALL		Control by SoC register (muALL needed) *	Asynchronous	Input	
PLL Signals						
pll_clkout0				Asynchronous	Input	
pll_clkout90				Asynchronous	Input	
pll_clkout180				Asynchronous	Input	
pll_clkout270				Asynchronous	Input	
pll_vreg				Regulated Supply	Input/Output	
pll_clkout_stop				Asynchronous	Input	
pll_vref_mpll_reg				Analog	Output	
pll_atb_sense_sel				Asynchronous	Output	
pll_clksel_en				Asynchronous	Output	
pll_cpbias_cntrl[6:0]				Asynchronous	Output	
pll_force_lock				Asynchronous	Output	
pll_gear_shift				Asynchronous	Output	
pll_gmp_cntrl[1:0]				Asynchronous	Output	
pll_int_cntrl[5:0]				Asynchronous	Output	

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
pll_lock				Asynchronous	Output	
pll_lockdet_mode				Asynchronous	Output	
pll_lock_det_on				Asynchronous	Output	
pll_lock_sel				Asynchronous	Output	
pll_n[3:0]				Asynchronous	Output	
pll_m[9:0]				Asynchronous	Output	
pll_meas_iv[17:0]				Asynchronous	Output	
pll_mpll_prog[16:0]				Asynchronous	Output	
pll_opmode[4:0]				Asynchronous	Output	
pll_prop_cntrl[5:0]				Asynchronous	Output	
pll_pwron				Asynchronous	Output	
pll_refclk				Asynchronous	Output	
pll_reset				Asynchronous	Output	
pll_testlock				Asynchronous	Input	
pll_th1[9:0]				Asynchronous	Output	
pll_th2[7:0]				Asynchronous	Output	
pll_th3[7:0]				Asynchronous	Output	
pll_th_delay[5:0]				Asynchronous	Output	
pll_tstplldig[2:0]				Asynchronous	Output	

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
pll_vco_cntrl[5:0]				Asynchronous	Output	
pll_vpl_det				Asynchronous	Input	
pll_clksel_in[1:0]				Asynchronous	Input	
Dual Interface Signals						
phy_clk_kill_out			If aggregation mode is not used the output signals should be left floating (not connected) and the inputs signals tied to low	Asynchronous	Output	
phy_clk_kill_in				Asynchronous	Input	
phy_clock8sent_out				Asynchronous	Output	
phy_clock8sent_in				Asynchronous	Input	
phy_hstraildone_out				Asynchronous	Output	
phy_hstraildone_in				Asynchronous	Input	
phy_clockungating_out				Asynchronous	Output	
phy_clockungating_in				Asynchronous	Input	
phy_clk_en_out				Asynchronous	Output	
phy_clk_en_in				Asynchronous	Input	
phy_div_en_out				Asynchronous	Output	
phy_div_en_in				Asynchronous	Input	
phy_serial_clk_en_out				Asynchronous	Output	
phy_serial_clk_en_in				Asynchronous	Input	
Scan Interface Signals						

Table 6-1 Testability Signals (Continued)

MIPI DPHY signals	TDR to control or observe	GPIO to control or observe	Requirement	Domain	I/O	Max Frequency (MHz)
scanin[25:0]				scanclk	Input	
scanluctrl[25:0]				scanclk	Input	
scanout[25:0]				scanclk	Output	
scanen			For SCAN	Asynchronous	Input	
scanmode				Asynchronous	Input	
scanclk				clock	Input	100
scanrstz				Asynchronous	Input	

6.3 Production Tests

This section presents an example for a possible set of tests that can be used for test production under ATE environment. The focus is on both parametric and functional tests.

This is a possible approach to test and not a strict guideline. Any other set of tests considered relevant can and should be used to complement these.

The following production tests are supported:

6.3.1 Shutdown or IDDQ

This test verifies that, when placed in Shutdown mode, the PHY is characterized by the lowest power consumption of all powered modes, mostly deriving from internal leakage currents. No activity on the PHY is expected.

Setup sequence:

1. Set shutdownz and rstz signals to logic low, testclr to logic high and scanmode to logic low. This step places the PHY in Shutdown mode
2. Ensure that no clock is driving the PHY (cfgclk, txclksec, testclk, refclk, and the various scan clocks).

Measures:

1. Check that all digital outputs referred to as externally observable are at default values, usually logic-low state; for more information, refer to "PLL SoC Control and Observability" on page 53.
2. No clock should be output by the PHY when placed in this mode.
3. Measure the power consumption from both digital and analog supplies to check that they are at the minimum values in the order of the values defined in "Power Consumption" on page 172.

6.3.2 Initialization

This test verifies the Start-up of the D-PHY macro and it completes after D-PHY macro reaches stopstate, indicating that LP-11 is being driven on the data lanes by the D-PHY transmitter.

Case 1 (operating rate 1 Gbps; cfg_clk=27 MHz; slew rate calibration enabled):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.

4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] = 7'b0001010.
7. Refer to table "Slew Rate vs DDL Oscillation Target" on page 58 and configure test control registers with appropriate values for the specified rise/fall time.
8. Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration.
9. Configure register 0x4a to set prg_on_lane0 (bit 6) to 1'b1.
10. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] = 6'b101000.
11. Apply cfg_clk signal with 27Mhz frequency.
12. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface (see "Initialization" on page 39 for additional details)
13. Set basedir_0 = 1'b0.
14. Set all requests inputs to zero.
15. Wait for 15 ns.
16. Set enable_n and enableclk=1'b1.
17. Wait 5ns.
18. Set shutdownz=1'b1.
19. Wait 5ns.
20. Set rstz=1'b1.
21. Wait until stopstatedata_n and stopstateclk outputs are asserted indicating PHY is driving LP11 in enabled datalanes and clocklane. (Consider 500us as maximum wait time)

Case 2 (operating rate 2.5 Gbps; cfg_clk=27 MHz; slew rate calibration disabled):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] = 7'b1001001.
7. Set bit [1] of test control register with address 0xA0 to 1'b1 to bypass slew rate calibration algorithm
8. Set bits [1:0] of test control register with address 0xA3 to 2'b00 to disable slew rate calibration.
9. Configure register 0x4a to set prg_on_lane0 (bit 6) to 1'b1.
10. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] = 6'b101000.
11. Apply cfg_clk signal with the appropriate frequency with 27Mhz frequency.

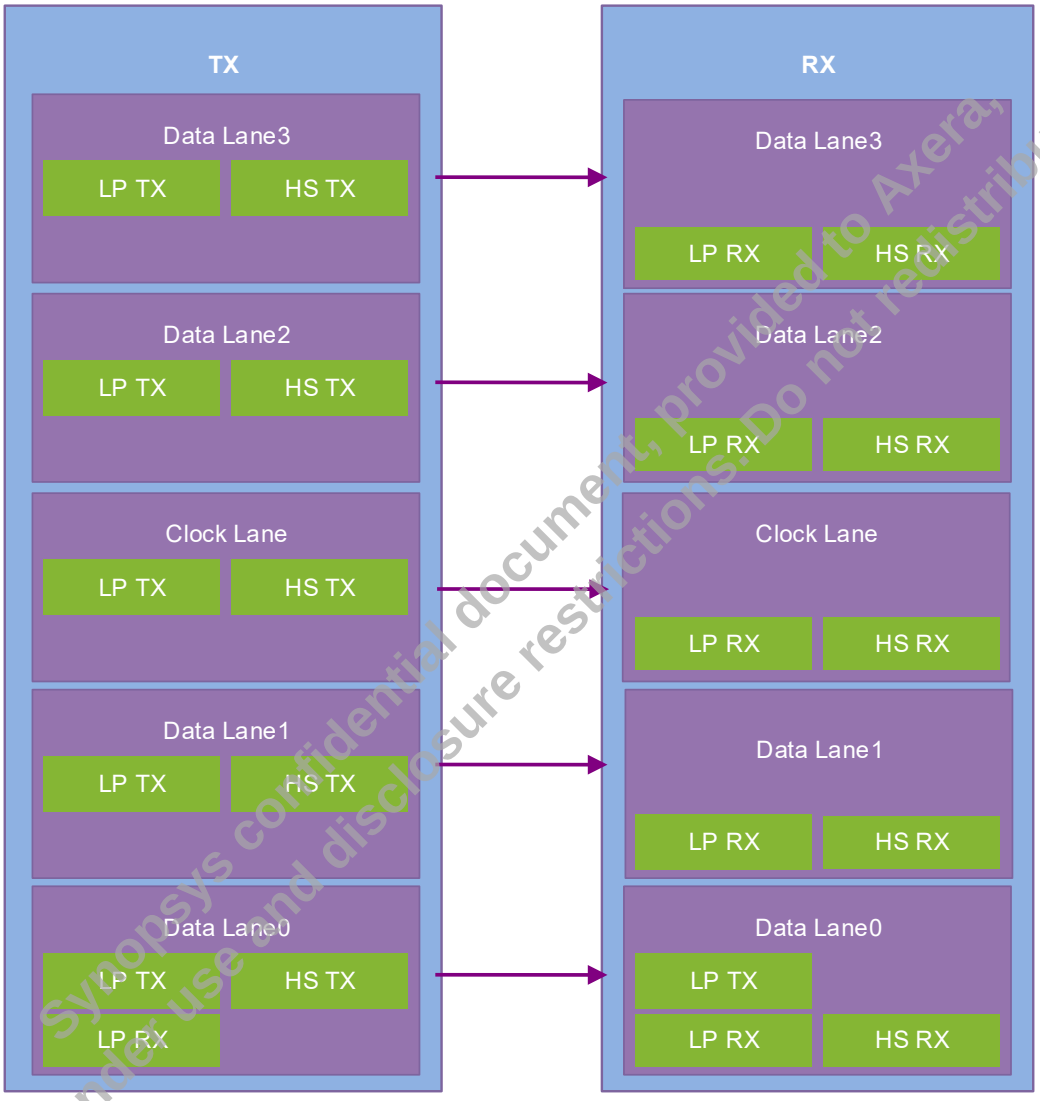
12. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface (see "Initialization" on page 39 for additional details)
13. Set basedir_0 = 1'b0.
14. Set all requests inputs to zero.
15. Wait for 15 ns.
16. Set enable_n and enableclk=1'b1.
17. Wait 5ns.
18. Set shutdownz=1'b1.
19. Wait 5ns.
20. Set rstz=1'b1.
21. Wait until stopstatedata_n and stopstateclk outputs are asserted indicating PHY is driving LP11 in enabled datalanes and clocklane. (Consider 500us as maximum wait time)

6.3.3 PHY-2-PHY High-Speed Checker

This production test can be exercised through the usage of an external D-PHY RX macro and the connections between transmitter and receiver PHY are done externally.

The internal pattern generator will transmit a PRBS9 pattern. X^9 + X^5 + 1.

Figure 6-4 PHY-2-PHY High-Speed Checker



Tests can be configured to send HS data, without low-power to high-speed transitions (direct HS testing), or including low-power to high-speed transitions. During this operation, only the received HS data is verified against the expected pattern.

In the PHY-2-PHY HS Checker mode there is no auto-checking (pass/fail indication) mechanism. There is however the possibility of verifying the error counter on the D-PHY RX side for indication of data corruption. This test must be controlled and verified through the tester interface on both TX and RX D-PHYs. The following test setup sequences exemplify two possible scenarios.

Setup Sequence 1 (includes low-power to high-speed transitions):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] for the desired operating frequency.
7. If bit rate > 1.5 Gbps set bit [1] of test control register with address 0xA0 to 1'b1 to bypass slew rate calibration algorithm.

   Refer to "Slew Rate vs DDL Oscillation Target" on page 58 and configure test control registers with appropriate values for the specified rise/fall time.

   - If bit rate =< 1.5 Gbps: Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration
   - If bit rate > 1.5G bps: Set bits [1:0] of test control register with address 0xA3 to 2'b00 to disable slew rate calibration
8. Set mpll_prg[0]=1'b1 through test control register 0x1F.
9. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] for the appropriate cfg_clk frequency
10. Apply cfg_clk signal with the appropriate frequency.
11. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface as indicated in "Initialization" on page 39.
12. Set basedir_0 = 1'b0.
13. Set all requests inputs to zero.
14. Wait for 15 ns.
15. Set enable_n and enableclk=1'b1.
16. Wait 5ns.
17. For each data lane refer to
    a. Set reverse data on lane 0 by setting hstxbitrev_lane0 on Test Code 0x45
    b. Set reverse data on lane 1 by setting hstxbitrev_lane1 on Test Code 0x55
    c. Set reverse data on lane 2 by setting hstxbitrev_lane2 on Test Code 0x85
    d. Set reverse data on lane 3 by setting hstxbitrev_lane3 on Test Code 0x95
18. Wait 5 ns.
19. Set shutdownz=1'b1.
20. Wait 5 ns.
21. Set rstz=1'b1.

22. Wait until stopstatedata_n and stopstateclk outputs are asserted indicating PHY is driving LP11 in enabled datalanes and clocklane. (Consider 500 us as maximum wait time).
23. Enable DPHY RX PHY (without HS direct feature) and wait until stopstatedata_n, and stopstateclk outputs are asserted (indicating the PHY is receiving LP11).
24. Set BISTON = 1'b1 to enable TX pattern generator (will send LP2HS transitions).
25. Enable pattern matcher (D-PHY RX).
26. Wait 10 us.
27. Latch error counter (D-PHY RX).
28. Check if errors are flagged in enabled datalanes.

Note

- For instructions regarding the D-PHY RX, see the D-PHY RX databook.
- Slew-rate can be configured and enabled before PHY Start-up.
- Error insertion can be enabled through signals pg_reg_err_r_lane* of Test Codes 0x4A, 0x5A, 0x8A and 0x9A, error will be inserted for each pulse on this signal (an error is inserted for each 0->1 transition).
- For D-PHY1.2 (> 1.5 Gbps) operation, the de-skew training sequence should be exercised by the TX macro using TXSKEWCALHS. This must be performed between steps 23. and 24. in the previous sequence.

Setup Sequence 2 (HS direct mode):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr to low.
6. Set hsfreqrange[6:0] for the desired operating frequency.
7. If bit rate > 1.5 Gbps set bit [1] of test control register with address 0xA0 to 1'b1 to bypass slew rate calibration algorithm. Refer to "Slew Rate vs DDL Oscillation Target" on page 58 and configure test control registers with appropriate values for the specified rise/fall time.
   - If bit rate =< 1.5 Gbps: Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration
   - If bit rate > 1.5G bps: Set bits [1:0] of test control register with address 0xA3 to 2'b00 to disable slew rate calibration
8. Set mpll_prg[0]=1'b1 through test control register 0x1F
9. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] for the appropriate cfg_clk frequency
10. Apply cfg_clk signal with the appropriate frequency.

11. Configure PLL operating frequency through D-PHY test control registers or through PLL SoC shadow registers interface as indicated in "Initialization" on page 39.
12. Set basedir_0 = 1'b0.
13. Set all requests inputs to zero.
14. Wait for 15 ns.
15. Set enable_n and enableclk=1'b1.
16. Wait 5 ns.
17. For each data lane refer to
    a. Set reverse data on lane 0 by setting hstxbitrev_lane0 on Test Code 0x45
    b. Set reverse data on lane 1 by setting hstxbitrev_lane1 on Test Code 0x55
    c. Set reverse data on lane 2 by setting hstxbitrev_lane2 on Test Code 0x85
    d. Set reverse data on lane 3 by setting hstxbitrev_lane3 on Test Code 0x95
18. Wait 5ns.
19. Enable DPHY TX in direct HS setting bit [4] of address 0x0C to 1'b1.
20. Set shutdownz=1'b1.
21. Wait 5 ns.
22. Set rstz=1'b1.
23. Read address 0x09C bit[6](enable lanes) and wait until it gets asserted (Consider 500 us as maximum wait time).
24. Enable D-PHY RX in HS direct mode.
25. Read RX PHY address 0x0C9 bit[4], and wait until it gets asserted.
26. Set BISTON = 1'b1 to enable TX pattern generator.
27. Enable pattern matcher (D-PHY RX).
28. Wait 10 us.
29. Latch error counter (D-PHY RX).
30. Check if errors are flagged in enabled datalanes.

Note

- For instructions regarding the D-PHY RX, see the D-PHY RX databook.
- Slew-rate can be configured and enabled before PHY Start-up.
- Error insertion can be enabled through signals pg_reg_err_r_lane* of Test Codes 0x4A, 0x5A, 0x8A and 0x9A, error will be inserted for each pulse on this signal (an error is inserted for each 0->1 transition).
- For D-PHY1.2 (> 1.5 Gbps) operation, the de-skew training sequence should be exercised by the TX macro using TXSKEWCALHS. This must be performed between steps 25. and 26. in the previous sequence.

6.3.4 IO Continuity Test

The supported IO Continuity Test allows applying a given voltage on clock/data lanes and rext pin and observing on a digital signal the respective signal assertion to confirm this external continuity on the respective signal.

Each pin of this output bus is used to verify the continuity from the package external pin all the way to the PHY's analog ports (through package, bonding, die).

This test should be performed with the PHY in shutdown mode and can be enabled through cont_en signal.

Setup sequence:

1. Set shutdownz and rstz signals to logic low, and testclr to logic high. This step places the PHY in Shutdown mode
2. Set cb_on signal through test control register 0x20, bits 1:0=2'b11
3. Set bintpon signal through test control registers 0x30, 0x40, 0x50, 0x80, 0x90, bits 1:0=2'b11
4. Assert cont_en to enable this test mode
5. For each of data/clock lanes and rext, apply 0V voltage
6. Wait 10ns
7. [**Measure 1**]
8. For each of data/clock lanes and rext, apply 1.2V voltage
9. Wait 10ns
10. [**Measure 2**]

Measures:

1. Check that all cont_data signals are de-asserted.
2. Check that all cont_data signals are asserted, confirming the IO continuity between the voltage externally applied and the D-PHY circuitry.

- cont_data[0]: rext
- cont_data[1]: clkn
- cont_data[2]: clkp
- cont_data[3]: datan0
- cont_data[4]: datap0
- cont_data[5]: datan1
- cont_data[6]: datap1
- cont_data[7]: datan2
- cont_data[8]: datap2
- cont_data[9]: datan3

- cont_data[10]: datap3

To validate the procedure on the simulation level:

Force internal nets with 1 or 0 to model the external voltage forced:

- dut.mipi_core_inst. I01AFE.CB. IOcont.a_internal (rext)
- dut.mipi_core_inst. I01AFE. LPTXC.DRVOLOOP.IOcont_1. a_internal (clkp)
- dut.mipi_core_inst. I01AFE. LPTXC.DRVOLOOP.IOcont_0. a_internal (clkn)
- dut.mipi_core_inst. I01AFE. LPTX1.DRVOLOOP.IOcont_1. a_internal (datap0)
- dut.mipi_core_inst. I01AFE. LPTX1.DRVOLOOP.IOcont_0. a_internal (datan0)
- dut.mipi_core_inst. I01AFE. LPTX2.DRVOLOOP.IOcont_1. a_internal (datap1)
- dut.mipi_core_inst. I01AFE. LPTX2.DRVOLOOP.IOcont_0. a_internal (datan1)
- dut.mipi_core_inst. I01AFE. LPTX3.DRVOLOOP.IOcont_1. a_internal (datap2)
- dut.mipi_core_inst. I01AFE. LPTX3.DRVOLOOP.IOcont_0. a_internal (datan2)
- dut.mipi_core_inst. I01AFE. LPTX4.DRVOLOOP.IOcont_1. a_internal (datap3)
- dut.mipi_core_inst. I01AFE. LPTX4.DRVOLOOP.IOcont_0. a_internal (datan3)

6.3.5 DC Parametric Tests

The following procedures perform DC parameter tests of the PHY analog blocks.

- PHY HS-TX DC specification
- PHY LP-TX VOH and VOL DC specifications
- PHY LP-RX DC VIH and VIL specifications

6.3.5.1 HS-TX Test Sequence

The next procedure tests the PHY HS-TX DC specification.

HS TX data bypass control sequence (used for HS mode DC parametric tests on ATE):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr = 1’b0.
6. Set hsfreqrange[6:0] = 7'b00000000 to keep the default bit rate (80 Mbps).
7. Refer to table “Slew Rate vs DDL Oscillation Target” on page 58 and configure test control registers with appropriate values for the specified rise/fall time.
8. Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration.

9. Set mpll_prg[0]=1'b1 through test control register 0x1F.
10. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] for the appropriate cfg_clk frequency
11. Apply cfg_clk signal with the appropriate frequency.
12. Configure PLL operating frequency through D-PHY test control registers, or through PLL SoC shadow registers interface (see "Initialization" on page 61 for additional details).
13. Set basedir_0 input signal to 1'b0.
14. Set all requests inputs to zero.
15. Wait for 15 ns.
16. Set enable_n and enableclk=1'b1.
17. Wait 5 ns.
18. Set hsdirect to 1 by writing test code 0x0C with value 8'b00010001.
19. Set test codes 0x30, 0x41, 0x50 with 0x40 to enable data bypass for one clock and four data lanes.
20. Set test codes 0x36, 0x46, 0x56 with 0xFF or 0x00 (all hstx_data_lane0[7:0] bits set to 1 or 0) depending on the output levels for DC parametric tests.
21. Wait 5 ns.
22. Set shutdownz=1'b1.
23. Wait 5 ns.
24. Set rstz=1'b1.

6.3.5.2 LP-TX Test Sequence

The next procedure tests the PHY LP-TX VOH and VOL DC specifications.

LP TX data bypass control sequence (used for LP mode DC parametric tests on ATE):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr = 1'b0.
6. Set hsfreqrange[6:0] = 7'b00000000 to keep the default bit rate (80 Mbps).
7. Refer to table "Slew Rate vs DDL Oscillation Target" on page 58 and configure test control registers with appropriate values for the specified rise/fall time.
8. Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration.
9. Set mpll_prg[0]=1'b1 through test control register 0x1F.
10. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] for the appropriate cfg_clk frequency
11. Apply cfg_clk signal with the appropriate frequency.

12. Configure PLL operating frequency through D-PHY test control registers, or through PLL SoC shadow registers interface (see "Initialization" on page 61 for additional details).
13. Set basedir_0 input signal to 1'b0.
14. Set all requests inputs to zero.
15. Wait for 15 ns.
16. Set enable_n and enableclk=1'b1.
17. Wait 5 ns.
18. Set test codes 0x33, 0x43, 0x53 with 0x07 or 0x04 to enable data bypass for one clock and four data lanes, and set lptxdin_* with 2'b11 or 2'b00 depending on the output levels for DC parametric tests.
19. Wait 5 ns.
20. Set shutdownz=1'b1.
21. Wait 5 ns.
22. Set rstz=1'b1.

6.3.5.3 LP-RX (Datalane 0) Test Sequence

The next procedure tests the PHY LP-RX DC VIH and VIL specifications.

LP RX data bypass control sequence @ TX IP (used for LP mode DC parametric tests on ATE):

1. Set rstz = 1'b0.
2. Set shutdownz= 1'b0.
3. Set testclr = 1'b1.
4. Wait for 15 ns.
5. Set testclr = 1'b0.
6. Set hsfreqrange[6:0] = 7'b0000000 to keep the default bit rate (80 Mbps).
7. Refer to table "Slew Rate vs DDL Oscillation Target" on page 58 and configure test control registers with appropriate values for the specified rise/fall time.
8. Set bits [1:0] of test control register with address 0xA3 to 2'b01 to enable slew rate calibration.
9. Set mpll_prg[0]=1'b1 through test control register 0x1F.
10. Set cfgclkfreqrange[5:0] = round[(Fcfg_clk(MHz)-17)*4] for the appropriate cfg_clk frequency
11. Apply cfg_clk signal with the appropriate frequency.
12. Configure PLL operating frequency through D-PHY test control registers, or through PLL SoC shadow registers interface (see "Initialization" on page 61 for additional details).
13. Set basedir_0 input signal to 1'b1.
14. Set all requests inputs to zero.
15. Wait for 15 ns.

16. Set enable_n and enableclk=1'b1.
17. Wait 5 ns.
18. Set shutdownz=1'b1.
19. Wait 5 ns.
20. Set rstz=1'b1.
21. Drive DATA0 P/N lanes with LP-11 and wait until stopstatedata_0 outputs are asserted.
22. Drive DATA0 P/N lanes with LP tester threshold voltages.
23. Read value of the following registers, this is a deserialized value of the received bits and must be 2'b11 or 2'b00.

    Lane 0 observability: 0x41[1:0] - lprxdoutlp_lane0[1:0]

6.3.6 ATPG Scan Test

Use ATPG tools to generate manufacturing test patterns to test the digital logic inside the PHY through the scan interface of the different modules.

To confirm ATPG test coverage and ATPG effectiveness, refer to the coverage report available on the database deliverables.

6.4 Analog Test Bus

Some key analog biasing and control voltages can be probed using directly the Analog Test Bus (atb signal) or using the analog-to-digital converter (ADC) of 10bits resolution embedded in the PHY.

Note

- Access to analog test bus is restricted to a single signal. It is not allowed to probe more than one signal. If ATB is shared between two or more PHYs the same constraint applies.
- When selecting between internal nodes to be probed, the sequence must always pass through disabling the analog test bus and probing no signal to then probing the desired signal. This is mandatory to avoid potential conflicts and shorts on the analog test bus.
- Active probe should be used for ATB measurement.

For PLL related signals, pin atb_sense_sel (register 0x11, bit 9) should be set to '1' and appropriate control bit of meas_iv[17:0] bus selected (register 0x1e) for the internal node to be connected to the analog test bus.

Table 6-2 shows the correspondence and expected values for the PHY and PLL related internal nodes. Refer also to the support diagram for additional detail on the internal nodes location within the respective circuit.

Table 6-2 PHY Internal Nodes

Control Signal	Test Register	Description	Expected value
atb_lptx1200_on_clklane	0x39	LP transmitter voltage reference on clklane	1.1V – 1.3V
atb_lptx1200_on_lane*	0x49 (lane0) 0x59 (lane1) 0x89 (lane2) 0x99 (lane3)	LP transmitter voltage reference on data lane	1.1V – 1.3V
cb_atb_vbe_sel	0x2a	Temperature measurement (vbe of bjt device)	~0.7V

Table 6-2 PHY Internal Nodes (Continued)

Control Signal	Test Register	Description	Expected value
atb_sel_clklane[3:0]	0x39	0000 – no signal connected to atb	0V
		0001- vcomm (400mV – voltage below power switch supply of output stage)	0.4V typical, 0.472V when max programmability enabled
		0010 – vp on last serializer MUX in termination	vp supply
		0011 – vp on last serializer MUX in termination	vp supply
		0100 – gd on termination	gd supply
		0101 – cash (boost voltage steering termination switches)	Max 882mV; belongs to vp or vph domain depending on boost on/off
		0110 – vp on inverters in term_boost	vp supply
		0111 – vp on serializer	vp supply
atb_sel_lane*[3:0]	0x49 (lane0) 0x59 (lane1) 0x89 (lane2) 0x99 (lane3)	0000 – no signal connected to atb	0V
		0001 – vcomm (400mV – voltage below power switch supply of output stage)	0.4V typical, 0.472V when max programmability enabled
		0010 – vp on last serializer MUX in termination	vp supply
		0011 – vp on last serializer MUX in termination	vp supply
		0100 – gd on termination	gd supply
		0101 – cash (boost voltage steering termination switches)	Max 882mV; belongs to vp or vph domain depending on boost on/off
		0110 – vp on inverters in term_boost	vp supply
		0111 – vp on serializer	vp supply

Table 6-3 PLL Internal Nodes

Control Signal	Test Register	Description	Expected value @ 2.5Gbps in typical conditions
mpll_meas_iv[0]	0x1e	DCC_p – connects the internal positive DCC control line (vcip/vcqp: depends on mpll_meas_iv[11]) to the analog test bus.	0.41V @ meas_iv[11]=0
mpll_meas_iv[1]		DCC_n – connects the internal negative DCC control line (vcim/vcqm: depends on mpll_meas_iv[11]) to the analog test bus.	0.41V @ meas_iv[11]=0
mpll_meas_iv[2]		ivco – connects internal supply voltage of the VCO (ivco) to the analog test bus.	0.5456V
mpll_meas_iv[3]		vreg_mpll – clock path supply shorted by default to VPL supply line	vp
mpll_meas_iv[4]		vp_cp – connects vp_cp (CP block supply) voltage to the analog test bus.	vp
mpll_meas_iv[5]		vp_cp_ref – connects reference voltage of charge pump regulator to the analog test bus (depends on mpll_prg[7:6], by default vp voltage)	vp
mpll_meas_iv[6]		icopy – connects current source 'icopy'(1/128 of vco current) to the analog test bus.	6.56 uA
mpll_meas_iv[7]		gd – connects gd to the analog test bus.	0V
mpll_meas_iv[8]		vcntrl – connects vcntrl voltage to the analog test bus.	0.3V
mpll_meas_iv[9]		vref – connects vref voltage to the analog test bus.	0.3V
mpll_meas_iv[10]		vpsf – connects vpsf voltage to the analog test bus.	1.43V
mpll_meas_iv[11]		chooses which DCC control lines are measured 1'b - vcip/vcim 0'b - vcqp/vcqm (depend on mpll_meas_iv[0],mpll_meas_iv[1])	N/A
mpll_meas_iv[12]		Not used	N/A
mpll_meas_iv[13]		Not used	N/A
mpll_meas_iv[14]		vmb – connects vmb (vmaster_bias) voltage to the analog test bus.	0.85V
mpll_meas_iv[15]		gd – connects gd to the analog test bus.	0V
mpll_meas_iv[16]		Not used	N/A
mpll_meas_iv[17]		Not used	N/A

As illustrated in Figure 6-6 on page 140 you can choose the internal nodes using the ATB directly or the ADC.

Figure 6-5 ADC Successive Approximation Algorithm

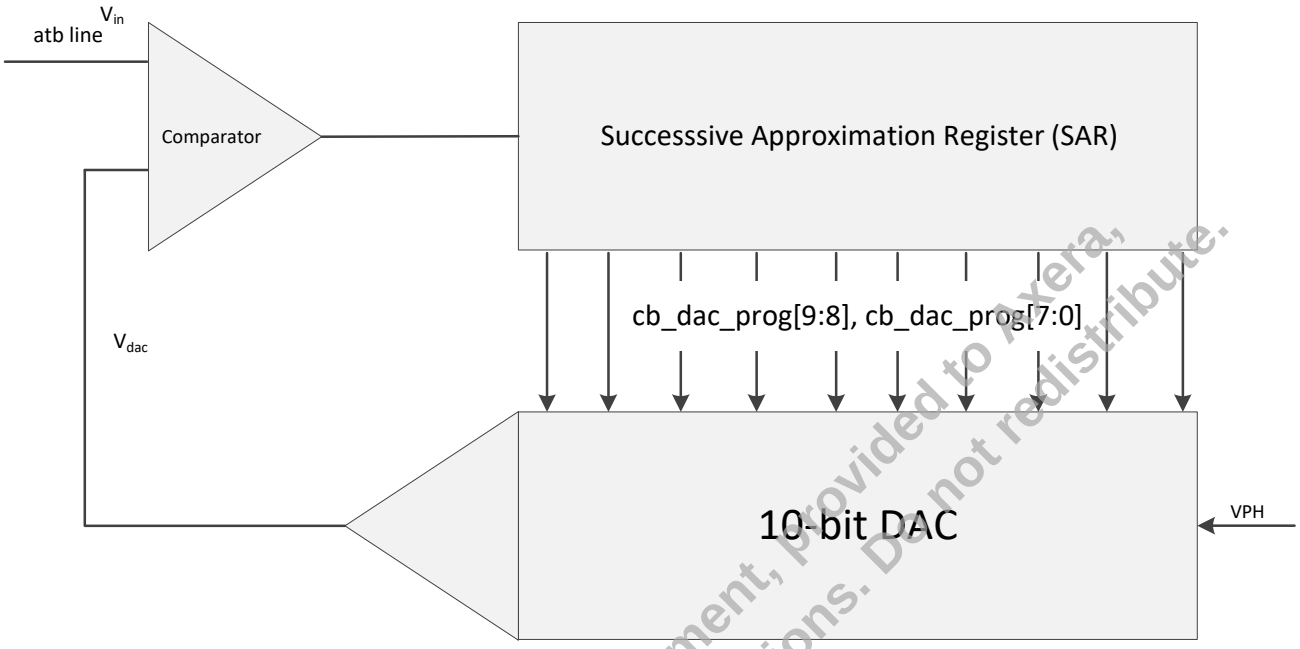
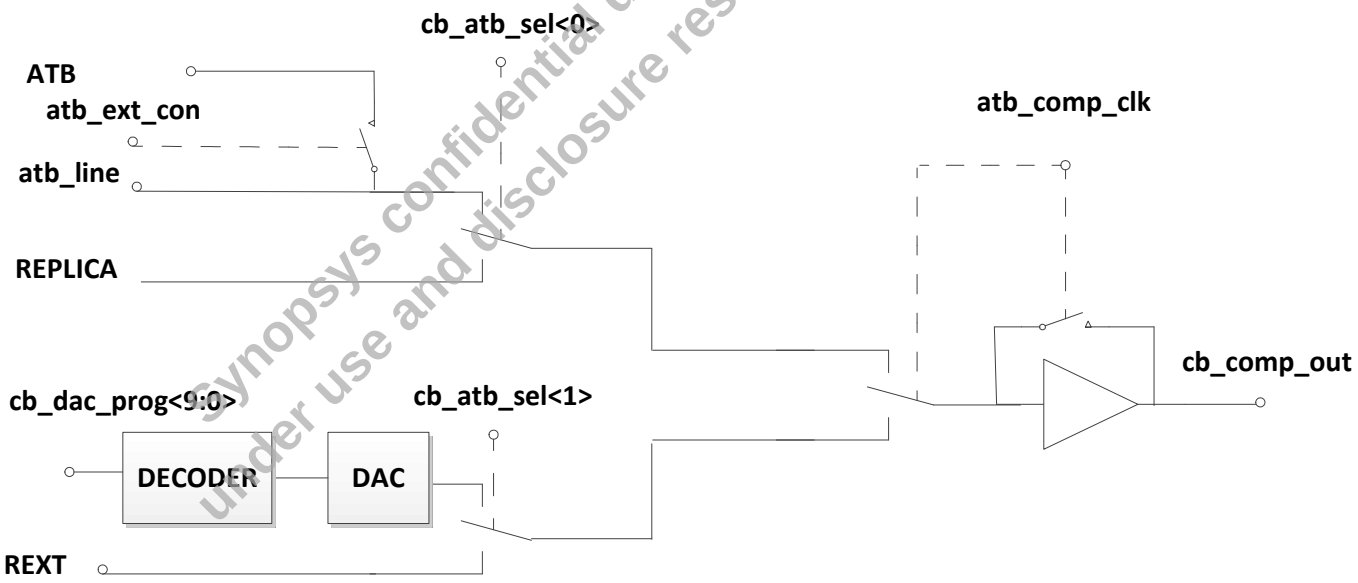


Figure 6-6 Analog Test Bus and Analog to Digital Converter



6.4.1 ATB Probing Procedure

ATB probing procedure (probing atb_lptx1200_on_lane0 node):

Probing sequence:

1. Ensure the PHY is in an active mode.
2. Set bits [2] of test control register with address 0x2A to 1'b1 (atb_ext_con=1b'1).
3. Select atb_lptx1200_on_lane0 and place it on atb_line setting bit[3] of test control register with address 0x49 to 1'b1.
4. Set bit[1:0] of test control register with address 0x2A to 2b'11 (atb_on enable).
5. Check if the observed voltage is within the expected value.

ADC probing procedure (probing atb_lptx1200_on_lane0 node):

1. Ensure the PHY is in an active mode.
2. Set bits [4:3] of test control register with address 0x2A to 2'b00 (cb_atb_sel=2'b00).
3. Select atb_lptx1200_on_lane0 and place it on atb_line setting bit[3] of test control register with address 0x49 to 1'b1.
4. Set testclr to 1'b1 to clear the previous ADC result.
5. Set testclr to 1'b0.
6. Set bit [0] of test control register with address 0x2C to 1'b1 to initiate the conversion procedure. The atb_line is compared with the Vdac value (generated using an ADC that represents the 10-bit input digital word).
7. The digital algorithm (Successive Approximation) iterates the 10 bits until the digital code represents the voltage on atb_line. The comparator output (cb_comp_out) can be observed reading bit[7] of test of TX control register with acddress 0x22.
8. Read test control register with address 0x2C and wait until bit[1] = 1'b1 (adc_done_int). Wait around 60 us. That indicates the conversion process is complete.
9. Read ADC result (cb_dac_prog[9:6],cb_dac_prog[5:0]):
   - Test control register with address 0x2C: cb_dac_prog[5:0] (testdin[7]=1'b1)
   - Test control register with address 0x2C: cb_dac_prog[9:6] (testdin[7]=1'b0)

The analog value can be obtained with:

```
. dec(cb_dac_prog[9:0]) x VPH /(2^10).
```


Note It is not possible to force voltage on probed nodes via DAC, however it is possible to force voltage in a node via ATB if ATB is accessible.

7 Physical-Level Implementation

This chapter describes the physical level implementation recommendations and good practices for the IP SoC integration. On top of these guidelines Signal and Power Integrity analysis should be performed. This chapter is divided in the following sections:

7.1 Pads Assembly

This section provides information about the bump map and pad size.

7.1.1 Bump Pad RDL and UBM Sizing

Bump pitch, bump type and sizing have been designed based on optimized bump placement for the IP. The bump pad redistribution layer (RDL), passivation opening and under-bump metalization (UBM) sizing are based on foundry required dimensions for the bump pitch.

Table 7-1 Bump Pitch Information

Drawn Bump Pitch (um)	Bump Type	Bump Pitch (um)	Drawn UBM (um)	Drawn RDL (um)	Technology Shrink Factor
130 um - 160 um	PAD_FC_LF_BU_150_160(wiAP)	153.5 (inline)	81.6	85.7	2%

Note

Bump pitches listed in Table 7-1 define the bump type, size, and design rule options which were used for IP verification. This does not mean that all bumps in the IP have the exact same maximum bump pitch or average bump pitch spacing; the bumps on the IP meet the following requirements:

- All bumps are spaced at greater than the minimum pitch spacing.
- All bumps are using the same bump dimensions (associated with the pitch listed in Table 7-1).
- All bumps are spaced at greater than the minimum pitch spacing.

For bump pin location information for package design, refer to the RDL pin locations in the LEF delivery file.

For different bump pitch, pad type, or spacing customization options, contact Synopsys.

Note

Ensure that the UBM has the correct size. Foundry and packaging typically require that the UBM shape used from the bump is the same for all bumps within the same die.

The size of the UBM shape is dictated by the minimum bump pitch in the die.

7.2 Physical Integration

For guidance during physical integration, the following table summarizes the compatibility between the supported metal options for the PHY IP and add-on blocks. All blocks connect by physical abutment. For guidance during physical integration, refer to the requirements detailed in the following sub-sections.

7.2.1 Cell Placement

The main concern when placing the IP core macro is to keep it isolated from all possible noise sources in the die.

It is recommended to place the PHY away from any other block that may generate noise, which can lead to the degradation of the cell performance. The best location is at the die periphery, close to the dedicated analog signal and power supply I/O pads.

Around the IP core macro boundary, there should be a keep-out area:

1. No unrelated routing within a 5 µm region
2. No devices within a 5 µm region

The PHY already has N-well "moats" for isolation, but if it is close to a noise source, an extra 10 µm N-well moat tied to vph should be added.

When connecting to the digital interface on the top side of the provided macros, the related routing is allowed to exist within the keep-out area defined above. No additional routing can be done within the PHY area, except for RDL routing and bump connections (if applicable) related to the MIPI D-PHY signal and power connections.

The following table summarizes the compatibility between the supported metal options for the PHY IP and add-on blocks. All blocks connect by physical abutment. Table 7-2 includes the necessary information required to assemble all blocks together.

Table 7-2 Metal Compatibility and Assembly Guidelines

Assembly	IO Type	IO Metal Option	IO Offset (µm × µm)	PLL Metal Option	PLL Offset (µm × µm)	IP Metal Option	IP Offset (µm × µm)
11M_2Xa1Xd_h_3Xe_vhv_2Y2R	FC	11M_2Xa1Xd_h_3Xe_vhv_2Y2R	0, 0	11M_2Xa1Xd_h_3Xe_vhv_2Y2R	260, 504.96	11M_2Xa1Xd_h_3Xe_vhv_2Y2R	0, 0
9M_2Xa1Xd_h_3Xe_vhv_2Z	FC	9M_2Xa1Xd_h_3Xe_vhv_2Z	0, 0	9M_2Xa1Xd_h_3Xe_vhv_2Z	260, 504.96	9M_2Xa1Xd_h_3Xe_vhv_2Z	0, 0

Note	IO structures and ESD protections are embedded on the MIPI D-PHY macro. The IO block to be instantiated together with the MIPI D-PHY macro corresponds to a bump map cell with bumps and respective routing for FC applications.

7.2.2 Cell Rotation and Mirroring

The GDS is delivered such that no rotation is required before placement within the SoC.

If it is rotated or mirrored, the same rotation and/or mirroring must be done on both the PHY hard macro and the add-on blocks, so that the whole integration maintains the connectivity.

For the identification of the correct PHY orientation one can refer to the release package:

- If the product name contains the 'ns' string, the PHY hard macro is north-south orientated, meaning it was implemented for a primary integration on the north or south edge of the SoC.
- If the product name contains the 'ew' string, the PHY hard macro is east-west orientated, meaning it was implemented for a primary integration on the east or west edge of the SoC.
- If the product name does not contain an orientation suffix it can be placed in both north/south or east/west orientations as it has no orientation constraints.

7.2.3 MIPI D-PHY Add-on PLL Integration

The DesignWare PLL should be attached to the IP hard macro. This connection is done by physical abutment and all analog related signals are connected upon this integration, see "PLL Modes of Operation" on page 39.

PLL digital signals that interface the MIPI D-PHY macro are connected to it through its soft-core portion. An additional group of PLL signals, identified on "PLL Modes of Operation" on page 39 and sub-section "PLL SoC Control and Observability" on page 53 are directly accessible to SoC digital logic for control/observability.

7.2.4 Multiple MIPI D-PHY TX Instances Sharing Single PLL

The DesignWare PLL can be integrated together with two IP hard macros by physical abutment; the one that is instantiated below the PLL is the MIPI D-PHY that controls it. The MIPI D-PHY macro instantiated by abutment on the right side of the PLL is able to use the PLL, but not directly configure or control it.

The maximum number of MIPI D-PHY TX 4L instances that can share a single provided PLL corresponds to two being that the DWC MIPI D-PHY TX 4L instantiated below the PLL is the responsible instance for configuring and controlling the PLL add-on block. The other instances are able to use the PLL clock output phases for testability purposes but are not able to directly configure and control the PLL.

The add-on PLL block outputs high-speed clock phases.

The following table summarizes the expected connections to be performed upon integration between the add-on PLL block and the multiple D-PHY instances.

The add-on PLL High Speed clock phases and clkout stop indication signals are propagated through the D-PHY TX.

The PLL lock output should also be connected to the pll_lock input of all D-PHY instances not directly connecting to or controlling the PLL for testability purposes.

Table 7-3 shows the signal connection between the PLL add-on block (center column) the, PHY controlling the PLL, and the PHY not controlling the PLL (if you are using more than one PHY).

See Figure 7-1 on page 150 for a visual representation of the PHYs and PLL add-on block relative position.

If you are using only one PHY, you can ignore column "PHY Signals (PHY on bottom mirrored of PLL, not controlling the PLL)".

Table 7-3 PHY–PLL Signals Connection

PHY Signals (PHY on bottom of PLL, controlling the PLL)	PLL Signals	PHY Signals (PHY on bottom mirrored of PLL, not controlling the PLL)
PLL-PHY Hard-Macro Interface Signals (placed by abutment - physical connected)		
Right Edge Side	Bottom Edge Side	Right Edge Side (before mirror) connection done through adjacent PHY Hard-Macro
pll_clkout0	clkout0	pll_clkout0
pll_clkout90	clkout90	pll_clkout90
pll_clkout180	clkout180	pll_clkout180
pll_clkout270	clkout270	pll_clkout270
pll_clkout_stop	clkout_stop	pll_clkout_stop
pll_vreg	vreg_mpll	pll_vreg
pll_on_hvz	pwrdn_h	pll_on_hvz
tx_atb_line	atb_sense	atb_line – ATB
PLL-PHY Soft-Macro Interface Signals (connected done through additional routing)		
Right Edge Side	Bottom Edge Side	Right Edge Side (before mirror)
pll_atb_sense_sel	atb_sense_sel	pll_atb_sense_sel – Leave floating
pll_clksel_en	clksel_en	pll_clksel_en – Leave floating
pll_clksel_in[1:0] (input)	phy_in_clksel[1:0] (output)	pll_clksel_in[1:0] (input)
pll_cpbias_cntrl[6:0]	phy_cpbias_cntrl[6:0]	pll_cpbias_cntrl[6:0] – Leave floating
pll_force_lock	force_lock_phy	pll_force_lock – Leave floating
pll_gear_shift	mpll_gear_shift	pll_gear_shift – Leave floating
pll_gmp_cntrl[1:0]	phy_gmp_cntrl[1:0]	pll_gmp_cntrl[1:0] – Leave floating
pll_int_cntrl[5:0]	phy_int_cntrl[5:0]	pll_int_cntrl[5:0] – Leave floating
pll_lock	lock_phy	pll_lock

Table 7-3 PHY–PLL Signals Connection (Continued)

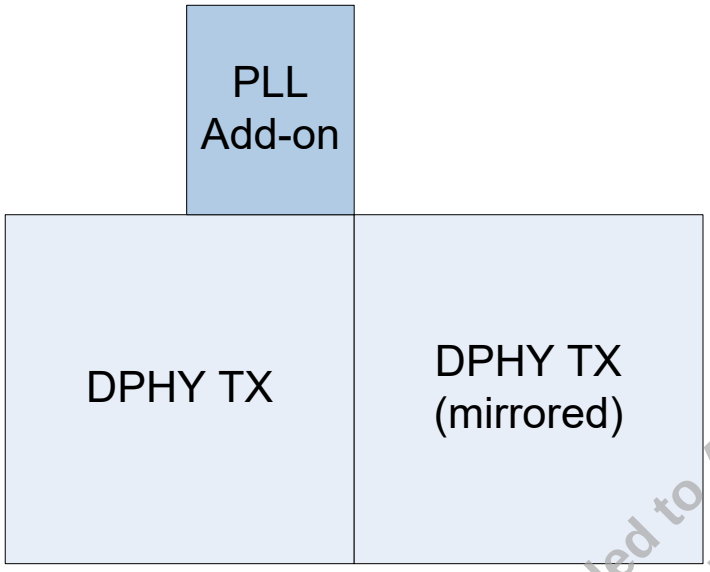
PHY Signals (PHY on bottom of PLL, controlling the PLL)	PLL Signals	PHY Signals (PHY on bottom mirrored of PLL, not controlling the PLL)
pll_lockdet_mode	lockdet_mode	pll_lockdet_mode – Leave floating
pll_n[3:0]	phy_n[3:0]	pll_n[3:0] – Leave floating
pll_m[9:0]	phy_m[9:0]	pll_m[9:0] – Leave floating
pll_meas_iv[17:0]	meas_iv[17:0]	pll_meas_iv[17:0] – Leave floating
pll_mpll_prog[16:0]	mpll_prog[16:0]	pll_mpll_prog[16:0] – Leave floating
pll_opmode[4:0]	mpll_opmode[4:0]	pll_opmode[4:0] – Leave floating
pll_prop_cntrl[5:0]	phy_prop_cntrl[5:0]	pll_prop_cntrl[5:0] – Leave floating
pll_pwron	mpll_pwron	pll_pwron – Leave floating
pll_refclk	clkin	pll_refclk – Leave floating
pll_reset	mpll_reset	pll_reset – Leave floating
pll_testlock	testlock	pll_testlock – Tie low (vss)
pll_th1[9:0]	th1[9:0]	pll_th1[9:0] – Leave floating
pll_th2[7:0]	th2[7:0]	pll_th2[7:0] – Leave floating
pll_th3[7:0]	th3[7:0]	pll_th3[7:0] – Leave floating
pll_th_delay[5:0]	th_delay[5:0]	pll_th_delay[5:0] – Leave floating
pll_vco_cntrl[5:0]	phy_vco_cntrl[5:0]	pll_vco_cntrl[5:0] – Leave floating
pll_lock_det_on	lock_det_on	pll_lock_det_on – Leave floating
pll_lock_sel	lock_sel	pll_lock_sel – Leave floating
pll_tstplldig[2:0]	tstplldig[2:0]	pll_tstplldig[2:0] – Leave floating
PLL-SoC Interface Signals		
Right Edge Side	Bottom Edge Side	Right Edge Side (before mirror)
N/A	clkext	N/A
N/A	m[9:0]	N/A
N/A	m_obs[9:0]	N/A
N/A	n[3:0]	N/A
N/A	n_obs[3:0]	N/A
N/A	clksel[1:0]	N/A
N/A	updatepll	N/A

Table 7-3 PHY–PLL Signals Connection (Continued)

PHY Signals (PHY on bottom of PLL, controlling the PLL)	PLL Signals	PHY Signals (PHY on bottom mirrored of PLL, not controlling the PLL)
N/A	shadow_clear	N/A
N/A	pll_shadow_control	N/A
N/A	pll_shadow_control_obs	N/A
N/A	gmp_cntrl[1:0]	N/A
N/A	gmp_cntrl_obs[1:0]	N/A
N/A	prop_cntrl[5:0]	N/A
N/A	prop_cntrl_obs[5:0]	N/A
N/A	vco_cntrl[5:0]	N/A
N/A	vco_cntrl_obs[5:0]	N/A
N/A	int_cntrl[5:0]	N/A
N/A	int_cntrl_obs[5:0]	N/A
N/A	cpbias_cntrl[6:0]	N/A
N/A	cpbias_cntrl_obs[6:0]	N/A
N/A	force_lock	N/A
N/A	lock	N/A
N/A	gp_clk_en	N/A
N/A	clkout_gp	N/A
N/A	scanclk	N/A
N/A	scanrstz	N/A
N/A	scanluctrl	N/A
N/A	scanmode	N/A
N/A	scanen	N/A
N/A	scanin	N/A
N/A	scanout	N/A

Figure 7-1 illustrates the correct orientation of the multiple MIPI D-PHY TX 4L instances when sharing a single PLL. No other integration and orientation is allowed.

Figure 7-1 Orientation of the Multiple MIPI D-PHY TX



All MIPI D-PHY instances and PLL add-on block should connect by physical abutment.

7.2.5 D-PHY IO Muxing with other Protocols

The MIPI D-PHY macro IOs can be multiplexed with other type of interfaces and protocols.

This feature is useful to re-use existing bumps or pads to minimize the pin count of the SoC.

Special precautions need to be made to make such integration successful:

- All HS differential signal pairs must be loaded symmetrically with +/- 5% tolerance
- Maximum voltage allowed at D-PHY IOs is 1.35V in any operating mode
- When other interface is used the D-PHY macro needs to be configured in power down mode before other traffic takes place
  - vph power collapsing on D-PHY macro is not allowed during the operation of other interfaces
- The added load should not violate S-parameters specification defined in MIPI D-PHY v1.2 specification for driver and receiver characteristics
- Added components should:
  - not cause leakage bigger then 5uA and shall be symmetrical for DP and DN lines
  - only represent capacitive load for D-PHY operation
  - include 2nd ESD protection when connected to D-PHY bumps
- Primary ESD protection located inside the D-PHY macro may not be sufficient to protect added circuit and therefore may require separate assessment

The allowed additional capacitance represented by the added circuit depends on D-PHY maximum data rate and the lower the data rate requirements for D-PHY operation, the more capacitance can be added. If D-PHY IOs are muxed with other interfaces/protocols, maximum allowed D-PHY operating frequency is 2.0 Gbps.

Table 7-4 indicates maximum capacitance that can be added

Note

The maximum capacitance values are approximate values. Due to non-linearity of added components and integration imperfections the final approval of external components shall be evaluated together with a D-PHY macro simulation with spice model of additional circuitry connected to it

The capacitances that represent bump, wirebond pad opening, routing to the bump and routing to pad opening must be subtracted from values presented in the table.

Table 7-4 External Component Maximum Capacitance

DPHY Data rate [Gb/s]	fmax [GHz]	SDD@fmax [dB]	SCC@fmax [dB]	Maximum capacity [pF]
2.5	1.875	<-2.5	<-2.5	1.45
2.0	1.5	<-2.5	<-2.5	2.2
1.5	1.125	<-3	<-6	0.7
1.0	0.75	<-3	<-6	1.95

7.3 Cell Routing and Integration

The D-PHY macro includes embedded IOs and ESD structures. The provided IO add-on blocks include bump map for flipchip integrations and the correspond physical connection from the embedded IO pads to the bumps.

The following sections contain integration guidelines for the IO add-on blocks included in the package, and requirements if they are not used, see "Not Using Synopsys IO Add-on Connection Blocks".

For additional information see "IO Pads and Connection Add-on Blocks" on page 34.

7.3.1 Analog Voltage Supply (vph/vp) and Ground (gd)

MIPI D-PHY is designed with separate power supplies to reduce the noise coupling between clean and noisiest supplies. To avoid impact on performance, the PHY analog supplies must be isolated from the SoC supply rails. These supplies—from single instantiations or multiple instantiations sharing them—must be connected to I/Os and from the I/Os to the package pins.

Attention No power or ground pins can be left unconnected.

Power supply noise cannot exceed the maximum ripple noise amplitude specified for each supply (± 3%), for more information see "Power Integrity Simulations" on page 104. If you cannot meet this specification, contact Synopsys support.

A dedicated vph supply rail is required for the MIPI D-PHY. It can be shared on die between multiple MIPI D-PHY instances, as long as routing resistance from bump/pad to the IPs is less than 0.5 ohm.

On an integration scenario with multiple MIPI D-PHY TX 4L instances, each MIPI D-PHY instance requires a dedicated vp pin on the die.

Analog ground (gd) connections follow identical requirements as analog power supply connections.

7.3.2 Digital Supply (vdd and vss)

Digital supply (vdd and vss) can be shared with SoC digital core supply rails. For additional details on other supported integrations see "SoC/IP Power Domains" on page 155.

Attention All digital power and ground pins must be connected, no digital power or ground pin can be left unconnected.

MIPI D-PHY is designed to work with the digital voltage defined in "Power Consumption" on page 172. These values are valid at the IP level (not package level). Take into account the voltage drop from the voltage source to the IP connections.

Each pin must be connected to all metal layers where it is defined, the connection width must be at least the width of the pin. Calculate the total width of the route for a current higher than the documented PHY current consumption.

The maximum ripple noise amplitude is ± 3% of nominal supply level (peak-peak), see "Power Integrity Simulations" on page 104. If you cannot meet this specification, contact Synopsys support.

vdd and vss can be shared on the die with all MIPI D-PHY instantiations.

For additional requirements regarding vdd, vss power domain and ESD/Latch-UP protection requirements see "ESD/Latch-Up Considerations and Requirements" on page 156.

7.3.3 Analog Auxiliary Signals (atb and rext)

The connection of the rext and atb signals must meet the following requirements:

- rext can be shared between different macros you must ensure that total capacitance on rext pad is inferior to 10 pF. The total capacitance observed on single rext pad, for an individual dphy macro instance, is less or equal to 2 pF. Therefore, max routing capacitance is 10pF -2p*number_of_rext_connections.
- Maximum capacitance added by routing externally to atb must be less than 5.0 pF.
- Resistance of the external routing of rext signal must be less than 1.0 ohm while fulfilling EM rules for 2 mA DC current.
- Resistance of the external routing of atb signal must be less than 5.0 ohm while fulfilling EM rules for 1 mA DC current.
- The atb and rext pins can be shared between different IPs as long as access to these pins is done by one PHY instance at a time.

External routing requirements of atb and rext signals include die, package and pcb.

In case of rext and atb sharing between different macros make sure the total capacitance is inferior to the maximum value considering die, package and pcb.

7.3.4 Not Using Synopsys IO Add-on Connection Blocks

The package includes IO add-on blocks that are optimized for PHY performance, see "IO Pads and Connection Add-on Blocks" on page 34.

You can customize the IOs following the guidelines in this section.

7.3.4.1 Analog Data/Clock Signals (datap*/datan* and clkp/clkn)

The connection of the data and clock signals is critical, and must be done carefully. To obtain the maximum performance, it is highly recommended you follow the next guidelines.

Note These requirements apply to all lanes—both clock and data, independently of the system application—and die.

- Connections must be done with a width at least equal to the pin width.
- Capacitance of these connections must be as low as possible. Maximum capacitance added by routing externally to the PHY should be less than 0.5 pF.
- Resistance of the external routing of clock data signals must be less than 1.25 ohm while fulfilling EM rules for 6 mA DC current (the RDL/Top metal path widths should be able to meet electromigration rules specified for 125°C).
- Complementary *P and *N routing must match, up to and including the bonding wire connections, and PCB traces.
- The capacitance mismatch between pairs of signals from different lanes should be inferior to 10%.

7.3.4.2 Analog Auxiliary Signals (atb/rext)

Same requirements as in "Analog Auxiliary Signals (atb and rext)" on page 153.

7.3.4.3 Analog Power Supplies (vph and vp)

For the analog power supplies (vph and vp) follow the next guidelines.

Note These requirements apply die.

- Connections must be as short as possible, inferior to 0.5 ohm, and at least equal to the pin width.
- Connect the power supplies with the same nominal pad through wide interconnections (at least pin width). Calculate the width of the route for a current higher than the documented PHY current consumption, see "Power Consumption" on page 172.

7.4 SoC/IP vdd/vss Power Domain

For vdd/vss integration, two different integration schemes can be considered: SoC and IP oriented.

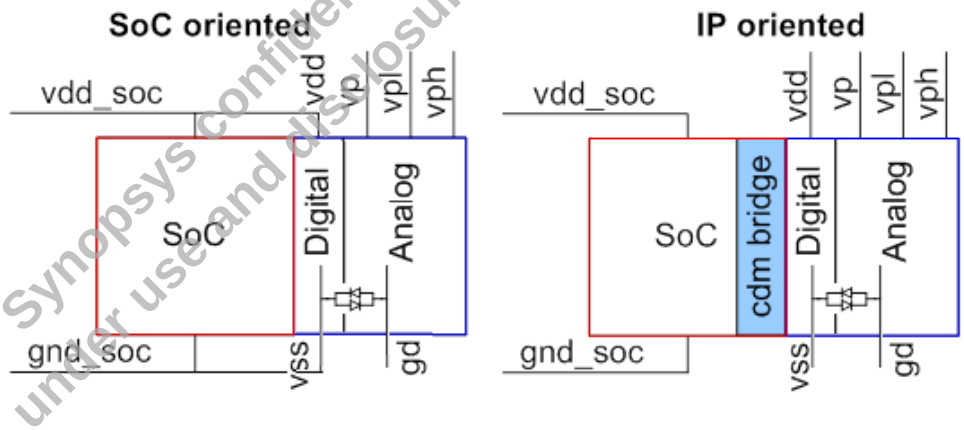
Table 7-5 and Figure 7-2 summarize the differences between the two different integration schemes.

Table 7-5 SoC/IP Power Domains

SoC oriented	IP oriented
vdd/vss shared on die with SoC vdd/vss	vdd dedicated to DPHY (hard macro, and soft macro) and not shared with SoC
vdd/vss routing resistance from macro to bump/power plane less than 0.3 ohm	You should add dedicated bumps to vdd and meet ESD foundry guidelines.
No cdm bridge required	CDM bridge recommended due to cross domain to vdd_soc. If all grounds are shorted on package through common ground plane, CDM bridge may not be necessary, but ESD foundry guidelines should be met.
All grounds should be shorted on package through common ground plane	All grounds should be shorted on package through common ground plane
	If gnd_soc is not shared on die with vss (see IP oriented diagram Figure 7-2): ■ It is recommended you add anti-parallel ESD diodes between PHY vss and gnd_soc, even if these supplies are shorted in the package. ■ It is necessary to add PSUB2 layer ring outside DPHY hard macro.

The back-2-back diodes on Figure 7-2 exist within the PHY implementation.

Figure 7-2 SoC/IP Power Domains



On an SoC oriented integration, the complete vdd cdie used for power integrity analysis must consider the cdie value from the SoC vdd power mesh which is, on this integration, shared with the PHY vdd power mesh.

On a IP oriented integration, the complete vdd cdie used for power integrity analysis must consider the cdie value from the DPHY soft-macro implementation which, on this integration, must be implemented and must share its vdd power mesh with the DPHY hard-macro.

Ensure that in both integrations power integrity analysis is performed, and noise specification of ±3% of nominal supply level (peak-peak) is met. For more information see "Power Integrity Simulations" on page 104.

7.5 ESD/Latch-Up Considerations and Requirements

All input/output elements connecting directly to pads are designed according to the rules for ESD and Latch-Up protection. The PHY is delivered with internal secondary ESD protections that go from simple ESD clamps to cross power domain protections.

During ESD events, the primary ESD protection circuits direct most of the current to the ground buses, keeping the signal pad voltage and voltage across the power buses low.

Back-to-back diodes enable current flow between power domains to prevent large voltage differences from developing between power domains and avoid damage between interfacing circuits due to power bus differences.

The primary ESD protection for signal and power supplies (vph and vp) are embedded inside the PHY. These are implemented through a RC-triggered mechanism that prevents ESD events from damaging the internal circuitry by creating low ohmic connections to appropriate ground domain and further drive the current through anti-parallel diodes to ground domain.

Only core vdd/vss shared digital supply rail protections are required to be added externally.

The vss and gd grounds present in the PHY must be shorted together on package level to enhance CDM protection robustness.

The following requirements should be followed then placing the PHY in SoC:

- Place external to the PHY vdd/vss power clamps at a maximum distance of 200 um spacing from the PHY boundary.
- The maximum vdd/vss routing resistance from SoC power clamps to the PHY boundary border should be < 0.3 ohm. The discharge path for vdd/vss placed inside the PHY is through SoC power mesh as this power domain is shared with the SoC digital core domain, therefore the resistance of this power mesh must be accounted in the 0.3 ohm budget.

If all grounds are shorted at package level, the requirements above can relaxed:

- Place external to the PHY vdd/vss power clamps in such a way that any distance from the center of the PHY to the power clamp is smaller than 1500 um.
- The maximum vdd/vss routing resistance from SoC power clamps to the PHY boundary border should be < 0.3 ohm. The discharge path for vdd/vss placed inside the PHY is through SoC power mesh as this power domain is shared with the SoC digital core domain, therefore the resistance of this power mesh must be accounted in the 0.5 ohm budget.

The Integrator must guarantee that ESD integration at SoC level complies with foundry ESD related checks and verifications.

No additional cross-domain protections are required between digital interface signals on the MIPI D-PHY macro and the SoC digital logic considering both are supplied by the same digital domain.

For additional information regarding ESD/LU specifications see "ESD/ LU Specifications" on page 25.

7.6 External Reference Resistor

The usage of external termination resistor is mandatory. It must be used for calibration of the TX termination to achieve a smaller TX termination value spread after calibration. Without using external termination resistor the spread will be bigger.

When the D-PHY block is using the reference resistor it will force current across the resistor and when it is not using, the current is disabled and rext net is in High-Z.

If used, it is used only on calibration procedures during D-PHY Start-up and can be disconnected afterwards. On this context, a single external termination resistor can be shared across multiple IPs and used by each when required, as long as there is no more than one using it and forcing current across the resistor.

In case of sharing the external reference resistor, there are several ways it can be shared to reduce the number of BGA balls or bump connections.

Apart from the options listed below, it can also be shared on board but requires all PHYs to have dedicated bump connections and BGA balls for each PHY rext pin.

7.6.1 Reference Resistor Sharing Between Multiple PHYs – sharing a BGA Ball

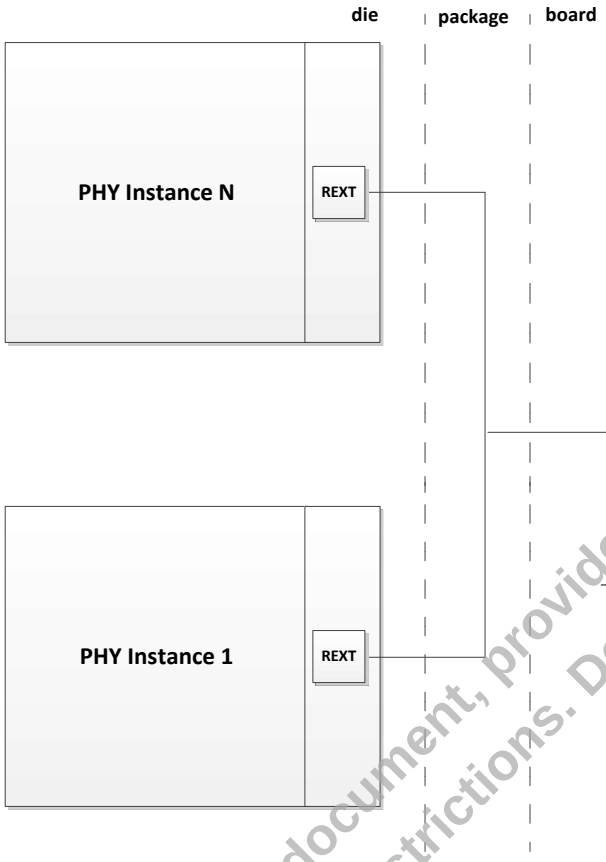
In order to reduce the number of external components and reduce the number of BGA bumps used, it is possible to share a single reference resistor between multiple PMAs.

1. In-package sharing without bump removal

The simplest method to share a reference resistor is to connect the rext connection together in the package substrate. If this is not possible another option is to connect the reference resistor together in the chip. With this approach there is no reduction in the number of rext bumps on the die, but there is a reduction in the number of balls being used.

Make sure you account parasitic resistance and capacitance requirements, see "Analog Auxiliary Signals (atb/rext)" on page 154.

Figure 7-3 Sharing Reference Resistor in Package



7.6.2 Reference Resistor Sharing Between Multiple PHYs – sharing a Single Bump

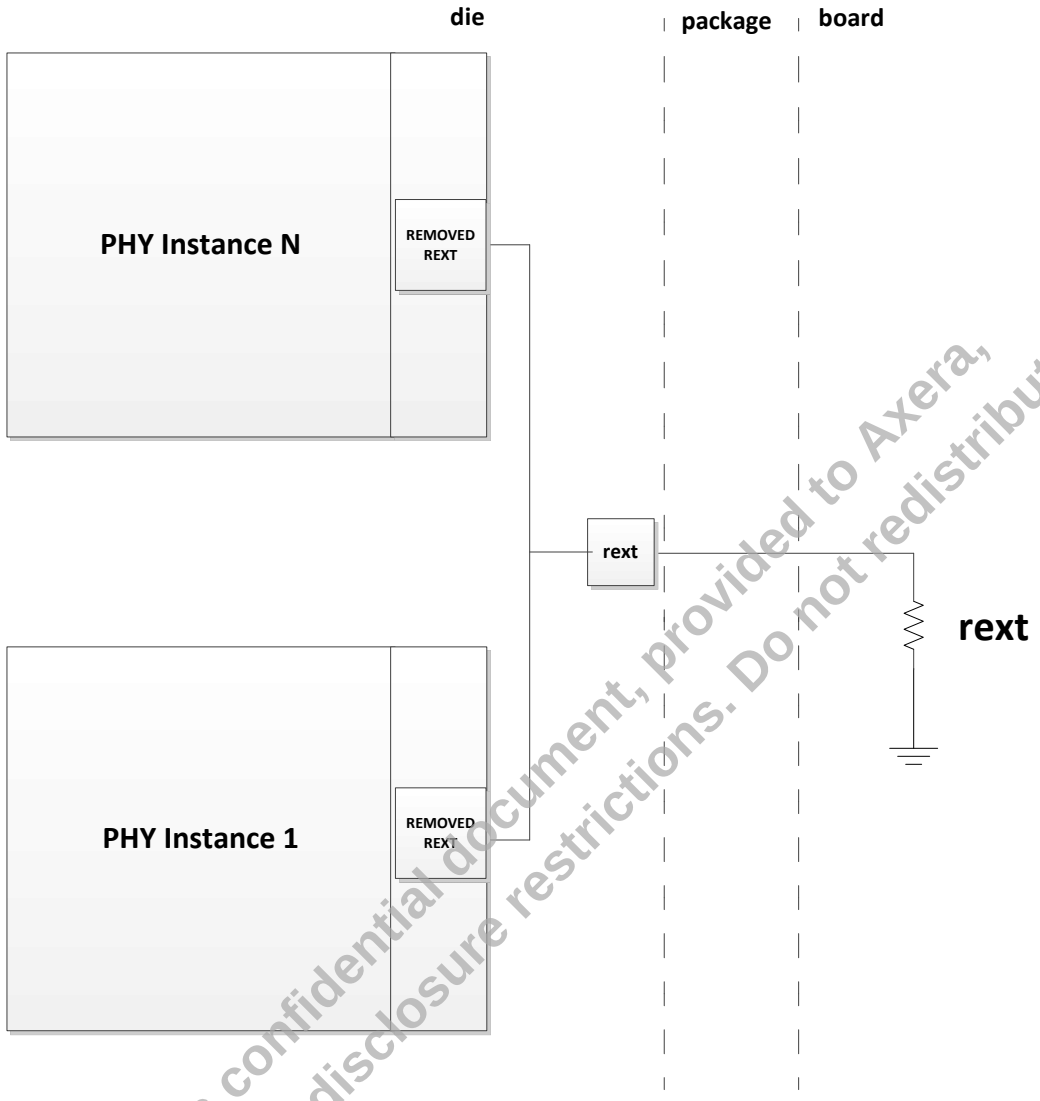
A shared reference resistor may also use a single bump to reduce substrate routing requirements.

There are two ways to implement the single rext bump. It may either be implemented as an additional bump external to the PHYs or it may be implemented as an additional bump internal to one of the PHYs.

The following options require changes at PHY GDS.

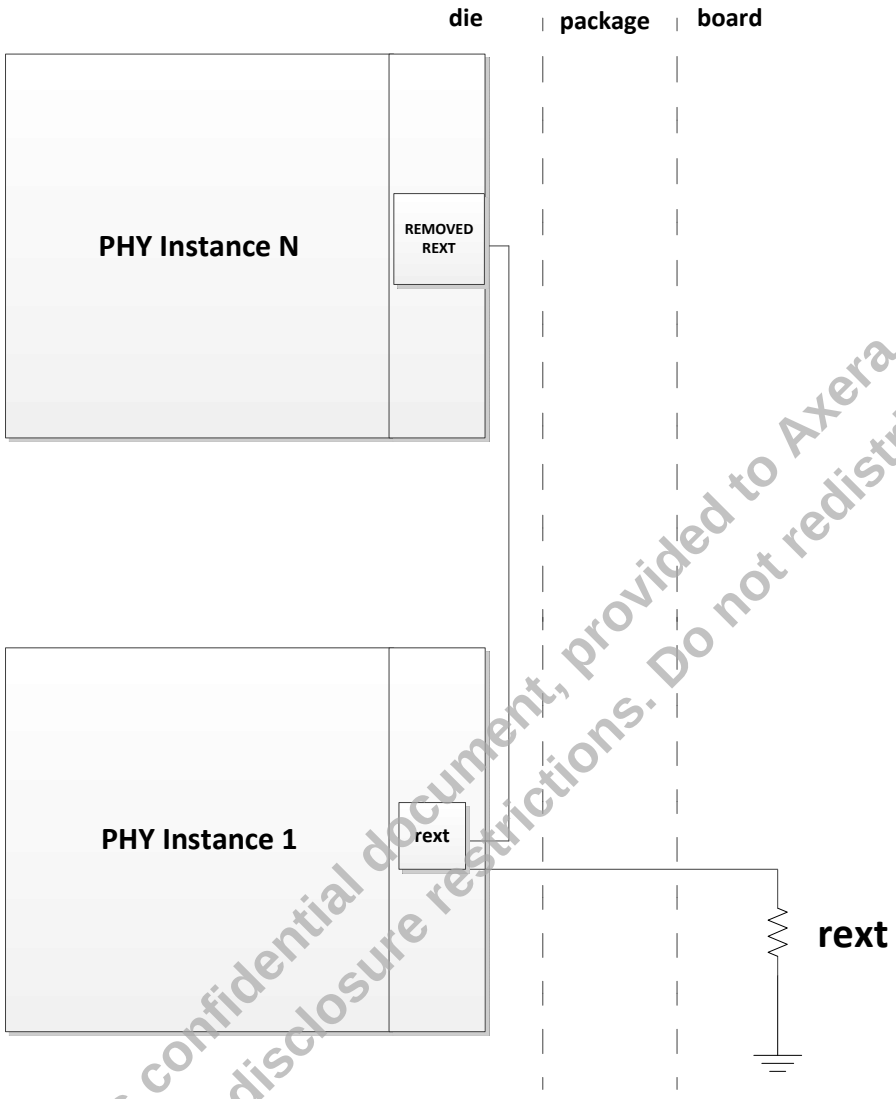
1. On-die sharing of a single external bump among multiple PHY macros to minimize number of bump connections. Single pad located outside PHY block.

Figure 7-4 Sharing Reference Resistor in Package



2. On-die sharing of a single rext macro bump among multiple PHY macros to minimize number of bump connections. Single pad located in one of the PHYs.

Figure 7-5 Sharing Reference Resistor on Die. Pad located on in PHY Block



8 Board- and Package-Level Implementation

This chapter provides package requirements suitable for the MIPI DPHY application and general recommendations for the PCB layout design common to most high-speed digital communication environments.

For DWC MIPI D-PHY 1v2 Tx 4L (PHY) to operate reliably at high data rates, excellent signal integrity is required. The correct package selection and good PCB layout is a key factor to achieve good signal integrity.

This chapter is divided in the following sections:

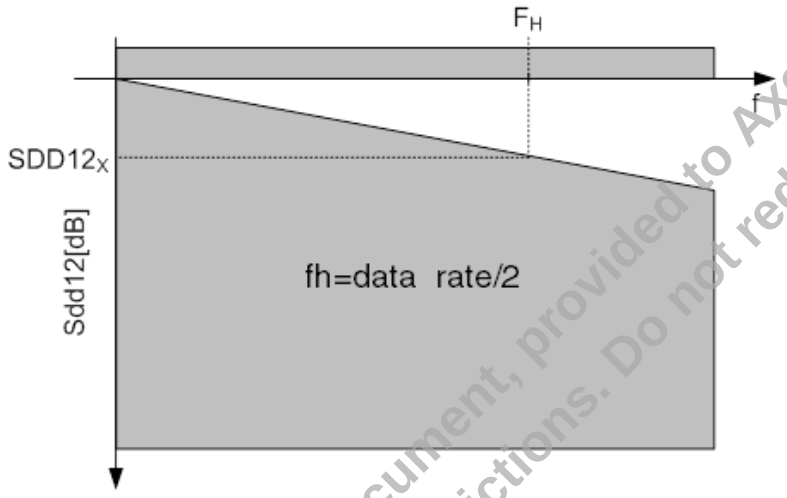
8.1 Package Requirements

Follow these requirements when selecting the package type.

For clock and data signal pairs, the Differential Insertion Loss $SDD12_X$ should be monotonic for frequencies up to 2*data_rate:

- $SDD12_X$ >=-0.3dB at f=data_rate/2.
- SDD11 should be kept < -20dB for frequencies up to ¾*data_rate.

Figure 8-1 Differential Insertion Loss SDD12



For power/ground signals, all must be connected to the package pins. No power/ground pins can be left unconnected.

8.2 PCB Guidelines

This chapter describes the PCB guidelines.

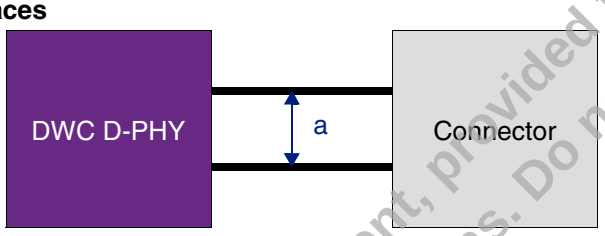
8.2.1 Trace Characteristics

Synopsys recommends that you maintain the TX differential pairs with 100 ohm (±10%) differential impedance. Reflections due to layer transitions need to be considered and properly designed to minimize signal integrity degradation at the higher rates.

Calculate the trace width and spacing for specific PCB characteristics such as copper weight, dielectric thickness, and so on. Symmetry in both shape and length is recommended.

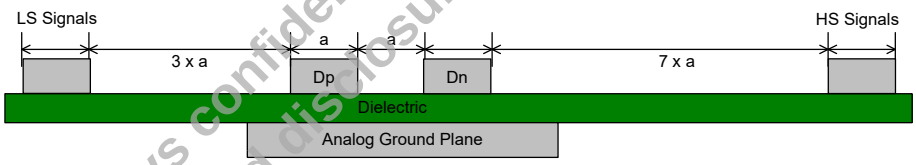
It is recommended to have the signal pairs routed symmetrically between lanes, and propagation delay well matched between data lanes and clock lane. Skew between any data lane and clock lane should be matched within ±10ps, this skew includes any skew due to routing on both package and PCB.

Figure 8-2 PCB Differential Traces



To minimize the crosstalk, take care of signal traces which are routed close to the TX/RX data differential pairs. The minimum recommended spacing is 3x for low-speed non-periodic signals and 7x for high-speed periodic signals. A continuous ground plane below the Dp/Dn lines is required.

Figure 8-3 Crosstalk Protection for Dp/Dn Lines



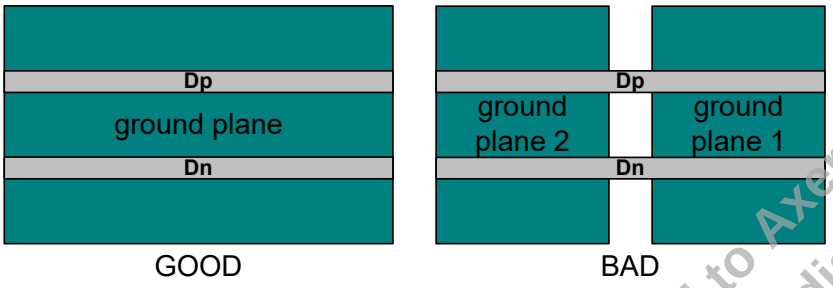
For atb/rext signals, the following requirements should be considered:

- For atb connection (die, package and pcb), capacitance should be < 5pF and resistance < 5 Ω
- For rext connection (die, package and pcb), capacitance should be < 10pF and resistance < 1 Ω
- It is recommended to use similar traces widths and lengths as for data pins.

8.2.2 PCB Layers

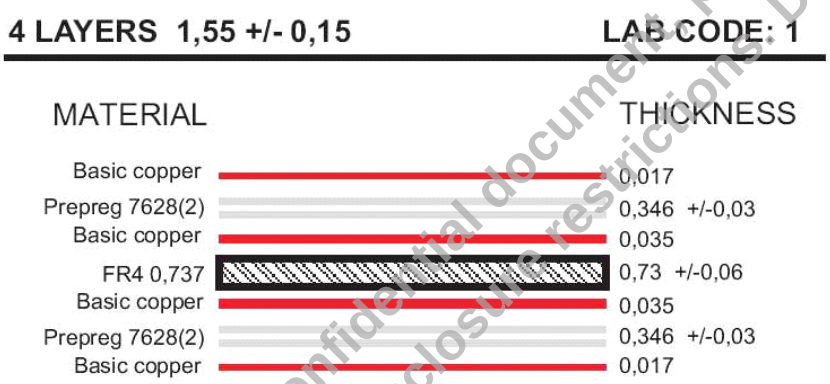
If high-speed signals are routed on the top layer, best results are obtained if layer 2 is a ground plane. Also, there must be only one ground plane under high-speed signals in order to avoid the high-speed signals crossing another ground plane.

Figure 8-4 Ground Planes



Four layers stack example is shown in Figure 8-5.

Figure 8-5 PCB Stack Layers (4 Layers)



8.3 Analog Power Supply Guidelines

This chapter describes the analog power supply guidelines.

8.3.1 Reference Series Resistance and Inductance

To ensure proper operation of PHY, power supply noise much be analyzed and controlled. Power integrity simulation is strongly recommended for IP integration into chip, package and PCB, see "Power Integrity Simulations" on page 104. The following guidelines are for reference, you should validate your package and PCB design through simulations, see "Power Integrity Simulations" on page 104.

- Total series resistance of power and ground connection from die bump to power supply on PCB—including routing resistance on package and PCB, and any parasitic resistance of series component (for example ferrite bead)—should be based on IR drop analysis. At die bump, target DC average is Vp/Vph -7%. The -7% drop covers voltage regulator tolerance, any IR drop from board and package series resistance, and any series DC resistance of component (for example ferrite bead).
- Total series inductance of power and ground connection looking out into PCB, including package loop inductance and series inductance of PCB connection should be minimized. Higher inductance in general results in higher ripple. Target should be inferior to 2 nH for vph and 1 nH for vp. This is not a specification, and not a pass/fail criteria. It provides first order estimate using very simple PDN model and will differ from actual exacted model.

Note	This is not a specification, and not a pass/fail criteria. It provides first order estimate using very simple PDN model and will differ from actual exacted model.

8.3.2 Reference PCB Decoupling Capacitors and Placement

Figure 8-6 shows a high level schematic diagram of the external circuitry required by the PHYs. Table 8-1 provides the power supply requirements.

Note	VDD supply not represented.

Figure 8-6 Schematic Diagram of the External Circuitry

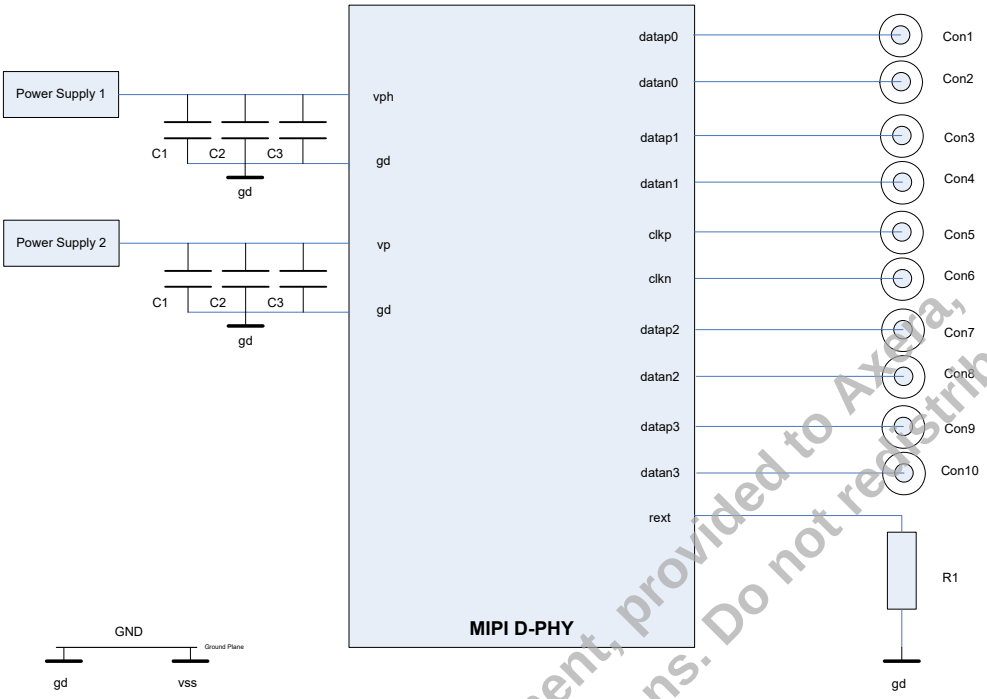


Table 8-1 Power Supply 1 Requirements

Power Supply 1
1.8 V

Table 8-2 Power Supply 2 Requirements

Power Supply 2
0.8 V

8.3.3 Bill of Materials

The bill of materials is shown in Table 8-3.

Table 8-3 Bill of Materials

Connectors	Con1, Con2, Con3, ... Con10 - SMA connectors or other surface mount coaxial connectors with 50 Ω impedance and bandwidth > 3 GHz
Power Supplies	1.8 V DC power supply 0.8 V DC power supply

Table 8-3 Bill of Materials (Continued)

Decoupling[a]	C1 - Capacitor 1 µF (Ceramic X7R)
	C2 - Capacitor 100 nF (Ceramic X7R)
	C3 - Capacitor 10 nF (Ceramic X7R)
Others	R1 - 200 ohm (optional)

a. You might need to adjust the capacitors values depending on the PI simulations.

Capacitor placement can be under the package in BGA pin field using low inductance attachment to minimize equivalent series inductance (ESL). Capacitor with smallest capacitance value should be placed as close as possible to package power and ground pins, and capacitor with larger capacitance can be placed further away.

8.3.4 Ferrite Bead for Analog Power Supply

When analog power supply Vp/Vph is shared with a common supply on PCB that also supplies current to other devices on PCB, a ferrite bead (or inductive choke) is recommended to isolate power-supply noise induced by other devices.

Power integrity and noise analysis are highly recommended to determine the correct specification of the ferrite bead used for noise isolation and to provide low impedance to analog Vp/Vph rail.

Ferrite bead must have high impedance at 100 MHz to isolate noise from other devices, and DC current rating should be at least 500 mA. DC resistance needs to be considered in total series resistance discussed earlier.

Table 8-4 lists the specifications of a sample ferrite bead (for example only).

Table 8-4 Example Ferrite Bead

Component	Impedance @100 MHz	Rated Current	DCR
HZ0805E601R-10	600 ohm	500 mA	300 milliohm

9 Process-Specific Specifications

This chapter includes the following topics:

9.1 Design Implementation Values, Voltage, and Temperature Specifications

Table 9-1 and Table 9-2 provide the design implementation, voltage, and temperature values.

Note Dimension values correspond to drawn dimensions in this databook.

Table 9-1 Design Implementation Values

Design Implementation		Value	Units
PHY	PHY macro size (IOs/ESD protections included as they are embedded on the MIPI D-PHY macro)	Area: 0.23	mm2
		Aspect Ratio: 450 x 504.96	µm
PLL	PLL macro size (add-on block for testability purposes)	Area: 0.056	mm2
		Aspect Ratio: 190 x 293.136	µm
PHY+PLL	Top width of the layout (WTOP)	190	µm
	Bottom width of the layout (WBOTTOM)	450	µm
	Height at left side of the layout (HLEFT)	504.96	µm
	Height at right side of the layout (HRIGHT)	798,096	µm
IO FC	Flipchip bump map For details regarding the Flipchip Area and Aspect Ratio values see the lef abstract view.	Bump pitch: 153.5 (inline)	µm
		Bump opening: 81.6 (UBM)	µm
Calibration	External reference resistor (RREF) 1% (or better) resistor connected to ground	200	Ω

Figure 9-1 Layout Plan

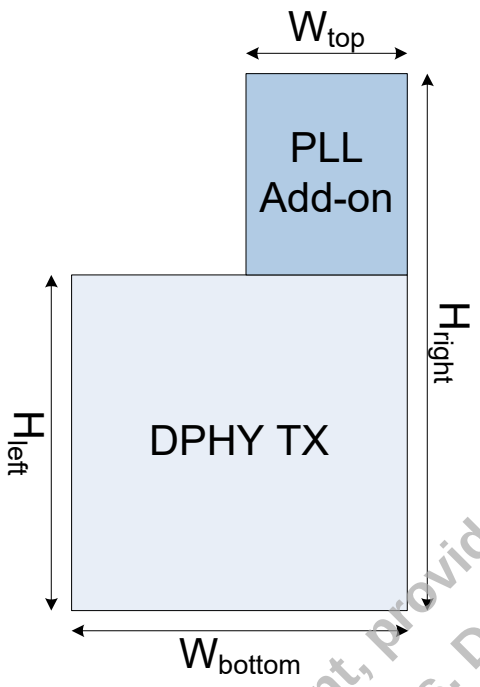


Table 9-2 Overall Voltage and Temperature Specifications

Parameter	Minimum	Typical	Maximum	Unit
Operating Junction Temperature	-40	+25	125	°C
Analog Supply Voltage[a] (vph)	1.674	1.8	1.98	V
Analog Low Supply Voltage[a] (vp)	0.744	0.8	0.88	V
Digital Supply Voltage[a] (vdd)	0.744	0.8	0.88	V

a. Specifications for the IP only (not at chip level). The supply range includes supply variation, noise, and IR drops.

9.2 Power Consumption

The following table provides power consumption values for current consumption for basic configuration with additional data lanes.

Note Power numbers only include single hard-macro power consumption.

Table 9-3 Project Specific Values for Power Consumption

Parameter	Condition			4 Data Lanes Includes PLL TYP	4 Data Lanes Includes PLL MAX	Unit
Supply Current	HS Mode	TX @1 Gbps	vph	5.40	8,8(a)/3,97(b)	mA
			vp	20.50	24.63	mA
			vdd	1.70	9.16	mA
	HS Mode	TX @1.5 Gbps	vph	5.40	8,8(a)/3,97(b)	mA
			vp	20.70	25.00	mA
			vdd	2.00	9.61	mA
	HS Mode	TX @2 Gbps	vph	5.40	8,8(a)/3,91(b)	mA
			vp	21.10	25.75	mA
			vdd	2.60	9.92	mA
	HS Mode	TX @2.5 Gbps	vph	5.40	8,8(a)/3,91(b)	mA
			vp	21.50	26.50	mA
			vdd	3.20	10.89	mA
	LP Mode	TX @10 Mbps (lane 0 only, PLL @2.5 Gbps)	vph	3.80	4.20	mA
			vp	7.00	8.60	mA
			vdd	1.90	8.70	mA

HS mode: Assume PRBS9 Pattern on data lanes and 100% occupation; that is, continuous HS.
a. vph maximum current consumption.
b. vph current consumption when PHY total current consumption (vph+vp+vdd) is maximum.

Table 9-3 Project Specific Values for Power Consumption (Continued)

Parameter	Condition			4 Data Lanes Includes PLL		Unit
				TYP	MAX	
Supply Current (Continued)	LP Mode	TX Control Mode (PLL @2.5Gbps)	vph	4.00	4.60	mA
			vp	7.00	8.60	mA
			vdd	1.80	8.70	mA
	ULPS	TX (PLL disabled)	vph	15	90	µA
			vp	20	750	µA
			vdd	120	7300	µA
	Shutdown		vph	10	20	µA
			vp	20	90	µA
			vdd	100	6800	µA

HS mode: Assume PRBS9 Pattern on data lanes and 100% occupation: that is, continuous HS.
a. vph maximum current consumption.
b. vph current consumption when PHY total current consumption (vph+vp+vdd) is maximum.

9.3 Electrical and Timing Information

This section provides the electrical and timing characteristics of the PHY.

9.3.1 Supply Requirements

Table 9-4 describes the Supply Requirements.

Table 9-4 Electrical and Timing Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{slew}	Supplies slew rate				0.1	V/µs

9.3.2 Input DC Specifications

Table 9-5 describes the Input DC Specifications.

Table 9-5 Input DC Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Apply to CLKP/N and DATAP/N Inputs						
V_I	Input signal voltage range		-50		1350	mV
I_{LEAK}	Input leakage current	$V_{GNDSH(min)} \le V_I \le V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode	-10		10	µA
V_{GNDSH}	Ground shift		-50		50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level		-0.15		1.45	V
$t_{VOH(absmax)}$	Maximum transient time above $V_{OH(absmax)}$				20	ns

9.3.3 HS Line Drivers DC Specifications

Table 9-6 describes the HS Line Drivers DC Specifications.

Table 9-6 HS Line Drivers DC Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω ≤ R_L ≤ 125 Ω **Note:** can be programmed using test control register 0x24(cb_sel_v400_prog[2:0]).	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω ≤ R_L ≤ 125 Ω			14	mV
V_{CMTX}	Steady-state common-mode output voltage	80 Ω ≤ R_L ≤ 125 Ω	150	200	250	mV
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	80 Ω ≤ R_L ≤ 125 Ω			5	mV
V_{OHHS}	HS output high voltage	80 Ω ≤ R_L ≤ 125 Ω			360	mV
Z_{OS}	Single-ended output impedance		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch				10	%

9.3.4 LP Line Drivers DC Specifications

Table 9-7 describes the LP Line Drivers DC Specifications.

Table 9-7 LP Line Drivers DC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OL}	Output low-level SE voltage	-50		50	mV
V_{OH}	Output high-level SE voltage	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	110			Ω
$\Delta Z_{OLP(01,10)}$	Single-ended output impedance mismatch driving opposite level			20	%
$\Delta Z_{OLP(00,11)}$	Single-ended output impedance mismatch driving same level			5	%

9.3.5 LP Line Receiver DC Specifications

Table 9-8 describes the LP Line Receiver DC Specifications.

Table 9-8 LP Line Receiver DC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IL}	Input low voltage, not in ULPS			550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULPS			300	mV
V_{IH}	Input high voltage	740			mV
V_{HYST}	Input hysteresis	25			mV

9.3.6 Contention Line Receiver DC Specifications

Table 9-9 describes the Contention Line Receiver DC Specifications.

Table 9-9 Contention Line Receiver DC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{ILF}	Input low fault threshold			200	mV
V_{IHF}	Input high fault threshold	450			mV

9.4 Switching Characteristics

This section provides the various specifications for the switching characteristics of the PHY.

Note Any expected default values are documented on Typical column in Table 9-10.

9.4.1 Input Clock Specifications

Table 9-10 describes the Input Clock Specifications.

Table 9-10 Switching Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{CFG_CLK}	CFG_CLK frequency	17		52	MHz
DC_{CFG_CLK}	CFG_CLK duty cycle	40	50	60	%
$F_{TXCLKESC}$	txclkesc frequency			20	MHz
$DC_{TXCLKESC}$	txclkesc duty cycle	45	50	55	%
F_{REFCLK}[a]	refclk frequency	2	24	64	MHz
DC_{REFCLK}[a]	refclk duty cycle	30		70	%
$F_{TXBYTECLKHS}$[b]	txbyteclkhs frequency	10		312.5	MHz

a. For further details regarding REFCLK specifications (i.e. phase noise, period jitter see Table 3-1 on page 37);
b. The txbyteclkhs signal should be generated from txbyteclksrc;

9.4.2 Clock Signal and Data-Clock Timing Specifications

Table 9-11 describes the Clock Timing.

Table 9-11 Clock Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
-	Maximum Serial Data rate (forward direction)	80		2500	Mbps	**Condition:** On DATAP/N outputs. 80 Ω ≤ R_L ≤ 125 Ω
F_{DDRCLK}	DDR CLK frequency	40		1250	MHz	**Condition:** On CLKP/N outputs
T_{DDRCLK}	DDR CLK period	0.8		25	ns	**Condition:**80 Ω ≤ R_L ≤ 125 Ω
UI_{INST}	UI instantaneous	0.4		12.5	ns	This value corresponds to a minimum Mbps data rate.
ΔUI	UI variation	-10%		10%	UI	When UI ≥ 1ns, within a single burst.
		-5%		5%	UI	When 0.667ns < UI < 1ns, within a single burst.
t_{CDC}	DDR CLK duty cycle		50		%	**Condition:** t_{CDC} = t_{CPH} / T_{DDRCLK}
t_{CPH}	DDR CLK high time		1		UI	
t_{CPL}	DDR CLK low time		1		UI	
-	DDR CLK / DATA Jitter		75		ps	**Condition:** When UI < 1ns, within a single burst. For PHY operating > 1.5Gbps C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew		0.075		UI	
$t_{SKEW[TX]}$	Data to Clock Skew	-0.15		0.15	UI	For PHY operating at or below 1Gbps
		-0.20		0.20	UI	For PHY operating above 1Gbps and below or at 1G5bps
$t_{SKEW[TLIS]}$		-0.20		0.20	UI	For PHY operating at or below 1Gbps
		-0.10		0.10	UI	For PHY operating above 1Gbps and below or at 1G5bps
$t_{SKEW[TX]}$ static	Static Data to Clock Skew (TX)	-0.20		0.20	UI	For PHY operating above 1G5bps and below or at 2G5bps

Table 9-11 Clock Timing (Continued)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$t_{SKEW[TLIS]\ static}$	Static Data to Clock Skew (Channel	-0.10		0.10	UI	For PHY operating above 1G5bps and below or at 2G5bps
$t_{SKEW[TX]\ dynamic}$	Dynamic Data to Clock Skew (TX)	-0.15		0.15	UI	For PHY operating above 1G5bps and below or at 2G5bps
Channel ISI	ISI			0.2	UI	For PHY operating above 1G5bps and below or at 2G5bps
$T_{SKEWCAL\ initial}$	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	$2^{\wedge 15}$		100	Min (UI) Max (µs)	For PHY operating above 1G5bps and below or at 2G5bps; Should be done prior first High- Speed Data burst. Time controlled by txskewcalhs assertion/de-assertion.
$T_{SKEWCAL\ periodic}$	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	$2^{\wedge 10}$		10	Min (UI) Max (µs)	For PHY operating above 1G5bps and below or at 2G5bps; Time controlled by txskewcalhs assertion/de-assertion.

Table 9-12 HS Line Drivers AC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_r	Differential output signal rise time			0.30	UI	**Condition:** 20% to 80%, RL = 50 W For PHY operating at or below 1Gbps
				0.35	UI	For PHY operating above 1Gbps and below or at 1G5bps
		100			ps	For PHY operating below or at 1G5bps
t_f	Differential output signal fall time			0.30	UI	Condition: 20% to 80%, RL = 50 W For PHY operating at or below 1Gbps
				0.35	UI	For PHY operating above 1Gbps and below or at 1G5bps
		100			ps	For PHY operating below or at 1G5bps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz			15	mV	
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz			25	mV	

9.4.3 LP Line Drivers AC Specifications

Table 9-13 describes the LP Line Drivers AC Specifications.

Table 9-13 LP Line Drivers AC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{rlp} , t_{flp}	Single ended output rise/fall time			25	ns	**Condition:** 15% to 85%, CL < 70 pF C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
t_{reot}				35	ns	**Condition:** 30% to 85%, CL < 70 pF The rise-time of t_{reot} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive. With an additional load capacitance CCM between 0 and 60 pF on the termination center tap at RX side of the Lane
$\partial V/\partial t_{SR}$	Slew rate @ C_{LOAD} = 0pF			500	mV/ ns	**Condition:** 15% to 85%, C_L < 70 pF C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line iwht 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by $V_{PIN(absmax)}$.
	Slew rate @ C_{LOAD} = 5pF			300	mV/ ns	C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line iwht 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by $V_{PIN(absmax)}$.

Table 9-13 LP Line Drivers AC Specifications (Continued)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$\partial V/\partial t_{SR}$	Slew rate @ C_{LOAD} = 20pF			250	mV/ ns	C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line iwht 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by $V_{PIN(absmax)}$.
	Slew rate @ C_{LOAD} = 70pF			150	mV/ ns	C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line iwht 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by $V_{PIN(absmax)}$.
	Slew rate @ C_{LOAD} = 0 to 70pF(Falling Edge Only)	25			mV/ ns	C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line iwht 2ns delay. When the output voltage is between 400 mV and 930 mV. Measured as average across any 50 mV segment of the output signal transition.

Table 9-13 LP Line Drivers AC Specifications (Continued)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$\partial V/\partial t_{SR}$	Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)	25			mV/ns	Measured as average across any 50 mV segment of the output signal transition. When the output voltage is in the range specified by $V_{PIN(absmax)}$ When the output voltage is between 400 mV and 550 mV.
	Slew rate @ C_{LOAD} = 0 to 70pF	25-0.0625 * ($V^{O,INST}$ - 550)			mV/ns	C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF, the distributed line capacitance can be up to 50pF for a transmission line iwht 2ns delay. Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts. When the output voltage is between 550 mV and 790 mV Measured as average across any 50 mV segment of the output signal transition.
C_L	Load capacitance	0		70	pF	C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

9.4.4 HS Line Receiver AC Specifications

Table 9-14 describes the HS Line Receiver AC Specifications.

Table 9-14 HS Line Receiver AC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz			50	mV	$\Delta V_{CMRX(HF)}$*is the peak amplitude of a sine wave superimposed on the receiver inputs.*
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz	-25		25	mV	
C_{CM}	Common mode termination			60	pF	

9.4.5 LP Line Receiver AC Specifications

Table 9-15 describes the LP Line Receiver AC Specifications.

Table 9-15 LP Line Receiver AC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	
T_{MIN}	Minimum pulse response	20			ns	
V_{INT}	Peak interference voltage			200	mV	
f_{INT}	Interference frequency	450			MHz	

A
Timing Diagrams

This appendix shows some important timing diagrams.

This chapter is divided in the following sections:

A.1 Operating Modes Control

Table A-1 Operating Modes Control

Input Signal	Operating Mode						
	Reset	High-Speed Data Transmission	Low-Power Data Transmission	Trigger Request	Ultra Low-Power State	Turnaround	Deskew Calibration
rstz	1'b0	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1
shutdownz	1'b0	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1
testclr	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
txrequesthsclk	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0
txrequestdatahs_n	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0
txrequestesc_n	1'b0	1'b0	1'b1	1'b1	1'b1	1'b0	1'b0
txlpdtesc_*n*	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0
txvalidesc_*n*	1'b0	1'b0	1'b1 (when valid data is in txdataesc_*n*[7:0])	1'b0	1'b0	1'b0	1'b0
txtriggeresc_*n*[3:0]	4'b0000	4'b0000	4'b0000	4'b1000 4'b0100 4'b0010 4'b0001	4'b0000	4'b0000	4'b0000
txulpsesc_*n*	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0
txulpsexit_*n*	1'b0	1'b0	1'b0	1'b0	1'b1 (to start exit procedure from ULPS mode)	1'b0	1'b0
txulpsexitclk	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0
turnrequest_*n*	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0

Table A-1 Operating Modes Control (Continued)

Input Signal	Operating Mode						
	Reset	High-Speed Data Transmission	Low-Power Data Transmission	Trigger Request	Ultra Low-Power State	Turnaround	Deskew Calibration
txskewcalhs	1’b0	1’b0	1’b0	1’b0	1’b0	1’b0	1’b1

A.1.1 High-Speed Data Transmission (Continuous Clock)

Input sequence (txbyteclkhs synchronous):

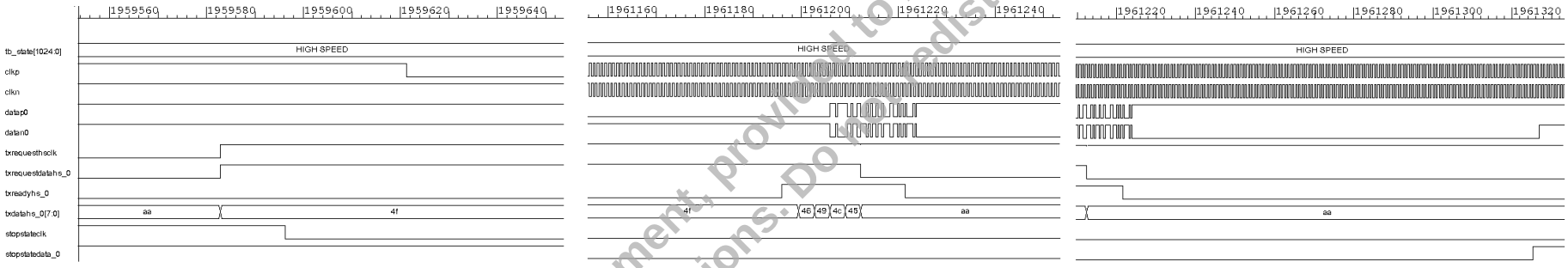
1. Set txrequesthsclk = 1'b1 and txrequestdatahs_n = 1'b1.
2. Wait for txreadyhs assertion.
3. Change txdatahs_n at posedge txbyteclkhs until the completion of the desired burst.
4. Set txrequestdatahs_n = 1'b0.
5. Wait for all stopstatedata_n assertion.
6. Wait for more than 67 txbyteclkhs cycles (in order to guarantee that all data lanes reach control mode).
7. Repeat sequence to send new burst.
8. After completing the HS transmission, set txrequesthsclk = 1'b0.

Note If the application requires multi-lane synchronization, the datalanes must be kept in the Stop state during a minimum 67-byte clock cycles for 2.5Gbps; this occurs after the stopstate_n signals are observed in the PPI. Only then a new request should be issued in the lanes. Using 67 byte-clock cycles for other datarates than 2.5Gbps can increase the dead time between packets. If you want to reduce dead time between packets, see table “High-Speed Transition Times” on page 202 column High-Speed Exit "HS->LP" DATA LANE to reduce the number of cycles according with datarate. Datalane0 stopstate signal is asserted later than the other datatalanes because of an internal synchronization; this wait time can only take into consideration the other enabled datalanes stopstate_n signal to further reduce this latency. Values are not applicable when using clocklane with a single datalane, in this case the new request can be done immediately after txreadyhs_n de-assertion.

A.1.2 High-Speed Data Transmission (Non-continuous Clock)

1. Set txrequesthsclk = 1'b1 and txrequestdatahs_n = 1'b1
2. Wait for txreadyhs assertion.
3. Change txdatahs_n at posedge txbyteclkhs until the completion of the desired burst.
4. Set txrequestdatahs_n = 1'b0.
5. Set txrequestdatahs_n = 1'b0, txrequesthsclk = 1'b0.
6. Wait for stopstateclk assertion.
7. Repeat sequence to send new burst.

Figure A-1 High-Speed Data Transmission (Non-continuous Clock)



Note

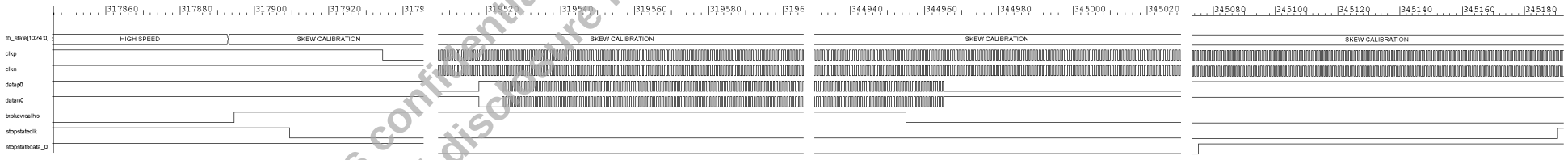
- If a new HS request is made before completion of the ongoing HS transmission process, the PHY starts the new transmission as soon as the current one ends. Because the lanes are independent, each lane starts a new transmission regardless of the state of the remaining lanes. To avoid such behavior, the new HS request should not be made before t > 67byteclk cycles after assertion of all stopstatedata_*n* outputs.
- If the application requires multi-lane synchronization, the datalanes must be kept in the Stop state during a minimum 67-byte clock cycles for 2.5Gbps; this occurs after the stopstate_n signals are observed in the PPI. Only then a new request should be issued in the lanes. Using 67 byte clock cycles for other datarates than 2.5Gbps can increase the dead time between packets. If you want to reduce dead time between packets, see table “High-Speed Transition Times” on page 202 column High-Speed Exit "HS->LP" DATA LANE to reduce the number of cycles according with datarate. Datalane0 stopstate signal is asserted later than the other datatalanes because of an internal synchronization; this wait time can only take into consideration the other enabled datalanes stopstate_n signal to further reduce this latency.
- Values are not applicable when using clocklane with a single datalane; in this case the new request can be done immediately after txreadyhs_n de-assertion.
- txrequestdatahs_*n* and txrequesthsclk can be simultaneously asserted and de-asserted, or if not the case txrequesthsclk needs to be asserted first than txrequestdatahs_n and de-asserted after txrequestdatahs_n in order to guarantee global timing parameters $T_{CLK-PRE}$ and $T_{CLK-POST}$.

A.1.3 High-Speed Deskew Calibration

Input sequence (txbyteclkhs synchronous):

1. Set txskewcalhs = 1'b1.
2. Wait at least minimum defined time for skew calibration of D-PHY spec. For detailed information see Table “Clock Timing” on page 178 and “High-Speed Transition Times” on page 201.
3. Set txskewcalhs = 1'b0.
4. Wait for stopstateclk assertion.
5. Any request can be processed by PHY.

Figure A-2 High-Speed Deskew Calibration



Note

If continuous clock mode needs to be supported keep the txrequesthsclk = 1'b1 while transitioning from to HS clock continuous toggling to deskew calibration and replace step 4 by Wait for the stopstateclk and all stopstatedata_n assertion followed by Wait for more than 67txbyteclkhs cycles (in order to guarantee that all data lanes reach control mode).

If the application requires multi-lane synchronization, the datalanes must be kept in the Stop state during a minimum 67-byte clock cycles for 2.5Gbps; this occurs after the stopstate_n signals are observed in the PPI. Only then a new request should be issued in the lanes. Using 67 byte-clock cycles for other datarates than 2.5Gbps can increase the dead time between packets. If you want to reduce dead time between packets, see table “High-Speed Transition Times” on page 202 column High-Speed Exit "HS->LP" DATA LANE to reduce the number of cycles according with datarate. Datalane0 stopstate signal is asserted later than the other datatalanes because of a internal synchronization; this wait time can only take into consideration the other enabled datalanes stopstate_n signal to further reduce this latency.

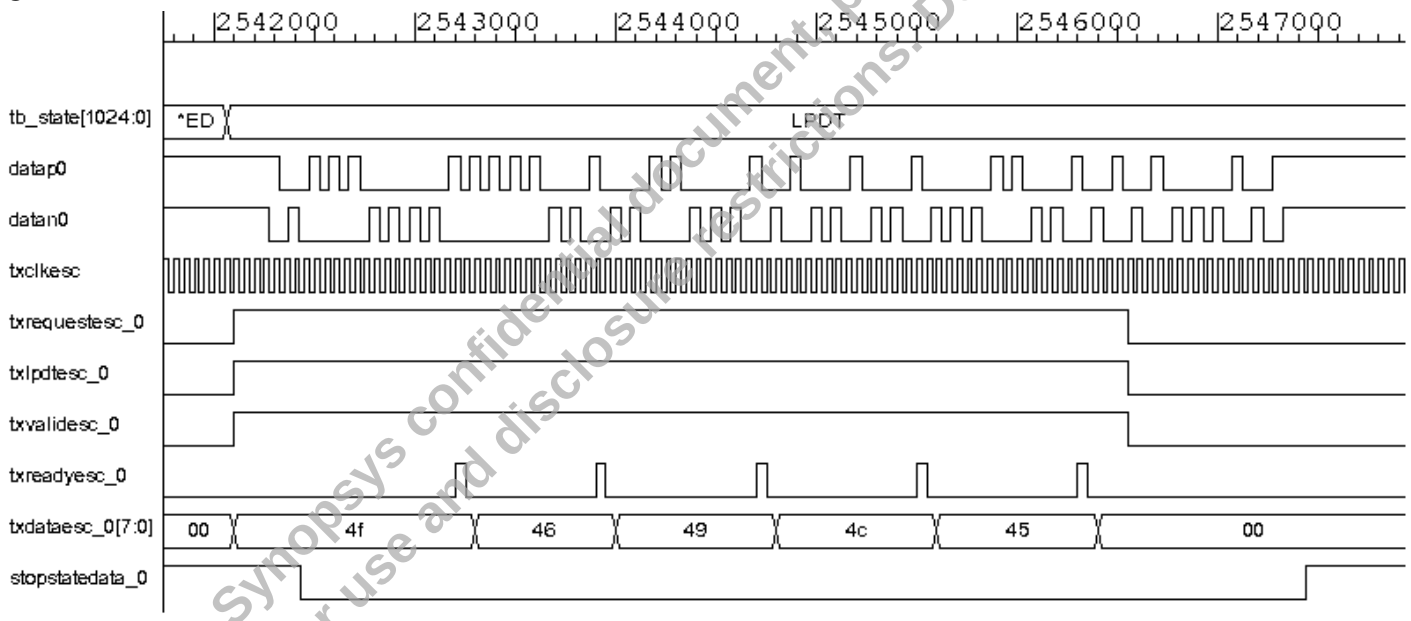
Values are not applicable when using clocklane with a single datalane, in this case the new request can be done immediately after txreadyhs_n de-assertion.

A.1.4 Low-Power Data Transmission (TX)

Input sequence (txclkesc synchronous):

1. Set txrequestesc_n = 1'b1.
2. Set txlpdtesc_N = 1'b1.
3. Set the data to transmit in txdataesc_n.
4. Set txvalidesc_n = 1'b1.
5. Wait for txreadyesc_n assertion.
6. Insert new value in txdataesc_n[7:0].
7. Repeat the txdataesc_n[7:0]/txvalidesc_n/txreadyesc_n sequence for several bytes to be transmitted.
8. Set txrequestesc_n = 1'b0.
9. Set txvalidesc_n = 1'b0.
10. Set txlpdtesc_n = 1'b0.

Figure A-3 Low-Power Data Transmission



Note Data is sampled when txreadyesc_n is asserted simultaneously with txvalidesc_n. If pauses between each byte are to be inserted, txvalidesc_n input should not be set to one during the complete transmission, but rather set to one only when the correct data is set in the txdataesc_n[7:0] input.

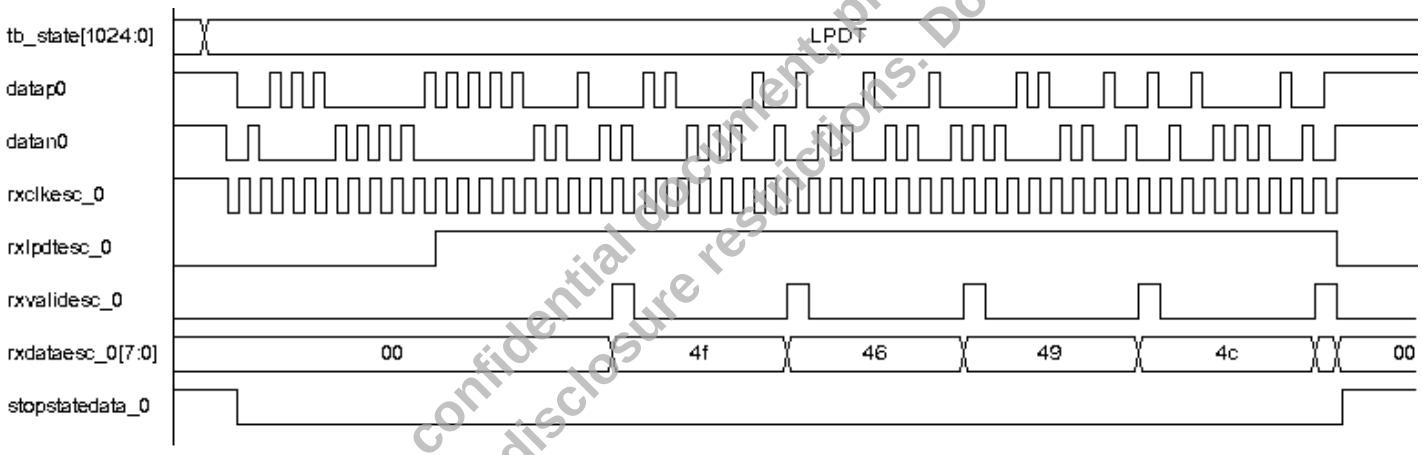
A.1.5 Low-Power Data Reception (RX)

> **Note** This operation is only available on data lane 0

Input sequence:

1. Wait until stopstatedata_0 is de-asserted.
2. Wait for the rxlpdtesc_0 assertion.
3. Wait for the rxvalidesc_0 assertion.
4. rxdataesc_0 changes at posedge rxclkesc_0.
5. Wait for the rxlpdtesc_0 de-assertion.
6. Wait for the stopstatedata_0 assertion.

Figure A-4 Low-Power Data Transmission (RX)



A.1.6 Escape Mode Trigger (TX)

Input sequence (txclkesc synchronous):

1. Set txtriggeresc_n[3:0] = 4'bXXXX (only one X is equal to 1, the remaining must be set to 0).
2. Wait until stopstatedata_n is de-asserted.
3. Set txrequestesc_n = 1'b0.
4. Set txtriggeresc_n[3:0] = 4'b0000.

Figure A-5 TX Trigger

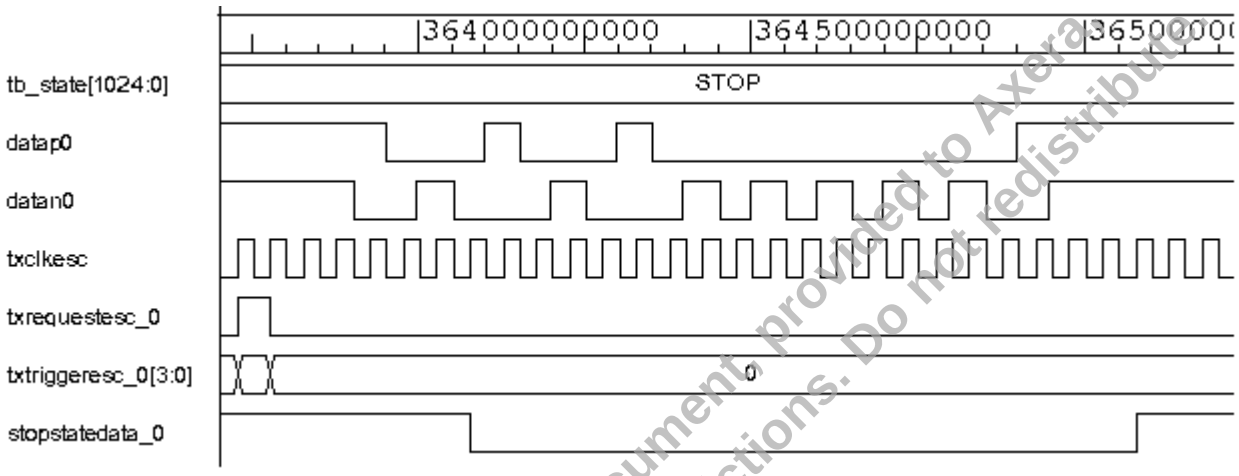


Figure A-6 TX Trigger

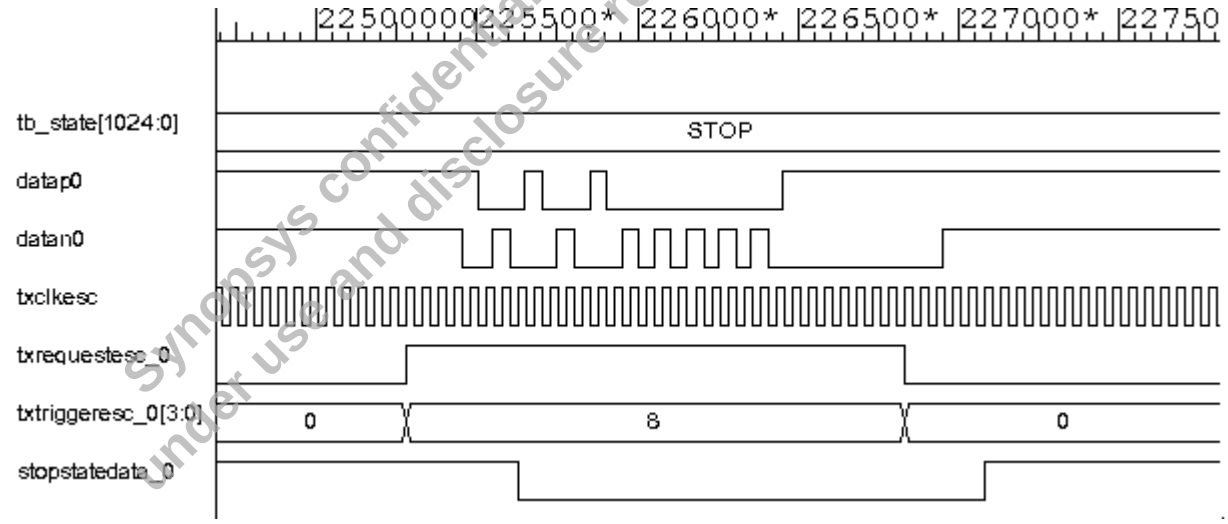


Table A-2 Reset Trigger

txtriggeresc_n[3:0] Value	Escape Mode Trigger
4'b0001	Reset Trigger
4'b0010	Unknown-3
4'b0100	Unknown-4
4'b1000	Unknown-5

Note

- txrequestesc_n and txtriggeresc_n[3:0] should be kept high at least during one txclkesc cycle but can be extended for more txclkec cycles if necessary.
- txrequestesc_n or txtriggeresc_n[3:0] need to be lowered for PHY to move to Stopstate (LP11), if not the case PHY will remain in Mark-1 (LP10) state.
- If a second request is done before the first is finished (and is not kept until after stopstatedata_*n* assertion/de-assertion), it is ignored.
- txtriggeresc_n[3:0] input must be one-hot encoded (the simultaneous assertion of two bits causes erroneous behavior).

A.1.7 Escape Mode Trigger (RX)

Note This operation is only available on data lane 0

Input sequence:

1. Wait until stopstatedata_0 is de-asserted.
2. rxtriggeresc_0 changes at posedge rxclkesc_0.
3. rxtriggeresc_0 = 4'bXXXX (only one X is equal to 1, the remaining must be set to 0).
4. Wait until rxtriggeresc_0[3:0] = 4'b0000.
5. Wait for the stopstatedata_0 assertion.

Figure A-7 RX Trigger

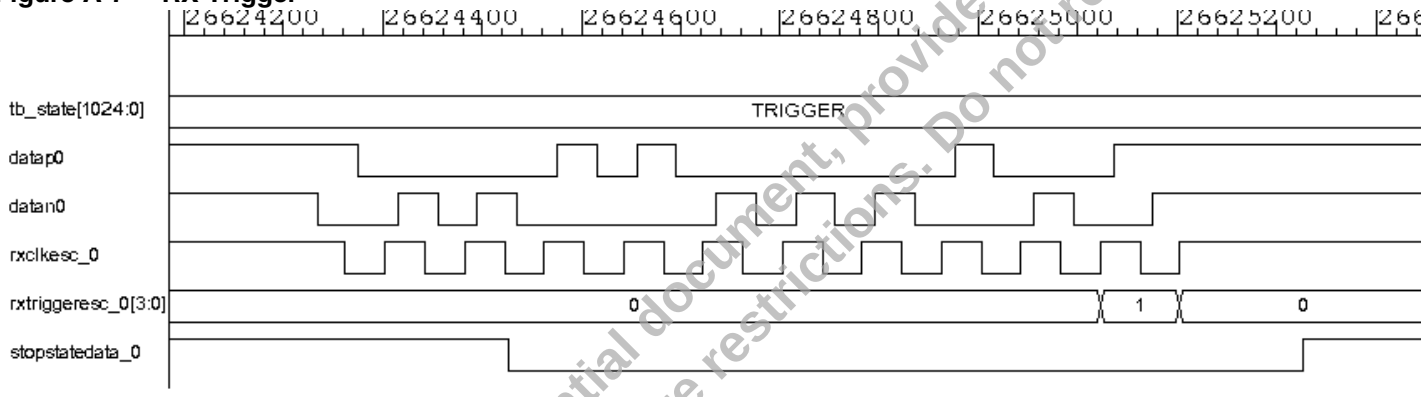


Table A-3 Reset Trigger

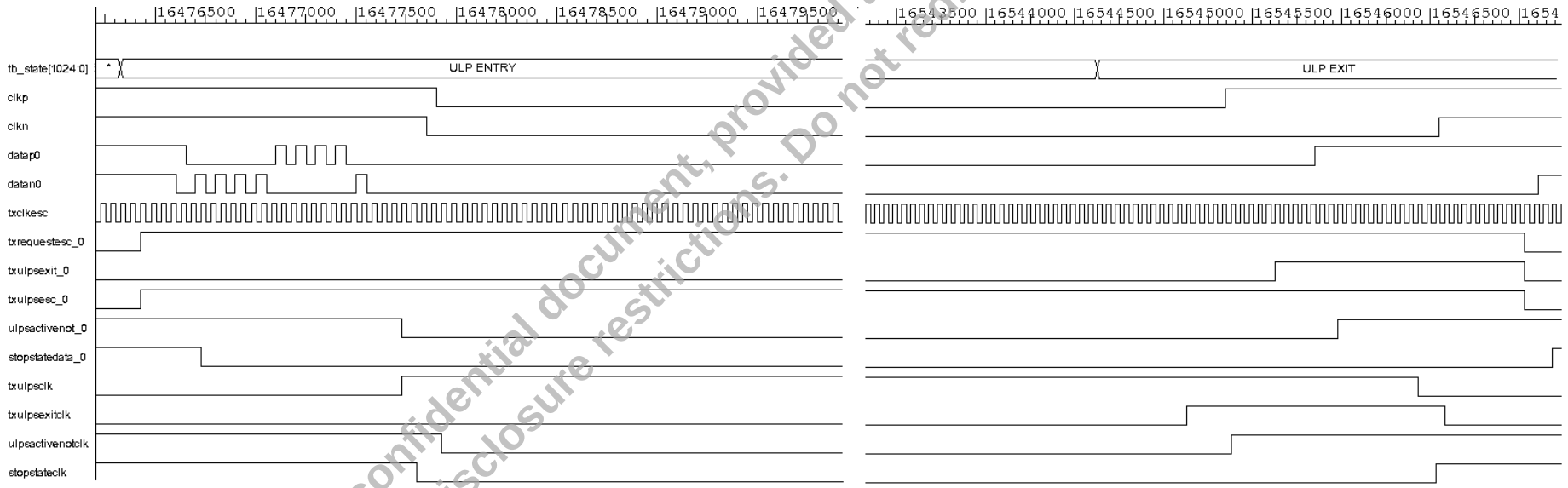
txtriggeresc_n[3:0] Value	Escape Mode Trigger
4'b0001	Reset Trigger
4'b0010	Unknown-3
4'b0100	Unknown-4
4'b1000	Unknown-5

A.1.8 Ultra Low Power State (TX)

Input sequence (txclkesc synchronous):

1. Set txrequestesc_*n* = 1'b1.
2. Set txulpsesc_*n* = 1'b1 (set txulpsclk =1’b1 if clock lane) .
3. Wait for ulpscativenot_n = 1'b0 (wait for ulpscativenotclk=1’b0 if clock lane)
4. Set txulpsexit_*n* = 1'b1 (set txulpexitclk =1’b1 if clock lane) .
5. Wait for t>1 ms (at least after rising edge of ulpsactivenot_n or ulpscativenotclk=1’b0 if clock lane).
6. Set txrequestesc_*n* = 1'b0.
7. Set txulpsesc_*n* = 1'b0. (set txulpsclk =1’b0 if clock lane).
8. Set txulpsexit_*n* = 1'b0. (set txulpexitclk =1’b0 if clock lane).

Figure A-8 Ultra Low Power State (TX)



Note

- txulpsesc_n (txulpsclk) must be set together with txrequestesc_n and lasts for at least one cycle, and can be maintained set until stopstatedata_n (stopstateclk) is de-asserted.
- txulpsexit_*n*/txulpexitclk must be asserted only after the request is completed (when ulpscativenot_*n* or ulpscativenotclk is set to 0).
- Mark-1 state begins sometime after txulpsexit_*n* (txulpexitclk) assertion.
- Exit from ulps state only occurs when txrequestesc_*n* is set low.
- It is required that the txbyteclkhs clock connection to txbyteclksrc is active before leaving ULPS state.
- By default, the PLL clock multiplier is switched off and part of AFE disabled if all enabled lanes are in forward direction and enter ULPS. PHY leaves this state if at least one of the lanes leaves ULPS (using txulpsexit_*n*/txulpexitclk signals).
- If PLL is disabled during ULPS, and PLL configuration is being done through the PLL SoC signals, you must apply updatepll pulse (as described in Figure 3-2 on page 40) before exiting from ULPS.

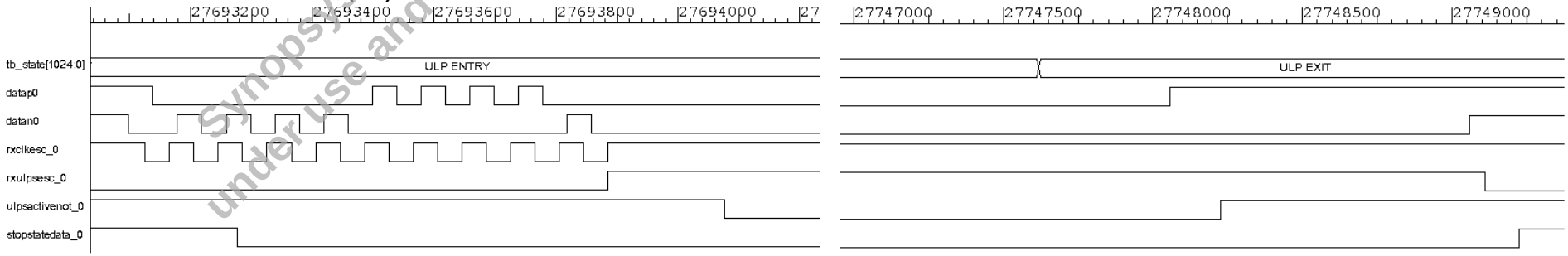
A.1.9 Ultra Low Power State (RX)

> **Note** This operation is only available on data lane 0

Input sequence:

1. Wait until stopstatedata_0 is de-asserted.
2. Wait for the rxulpesc_0 assertion.
3. Wait for the ulpscativenot_0 de-assertion.
4. Wait for the ulpscativenot_0 assertion.
5. Wait for the rxulpesc_0 de-assertion.
6. Wait for the stopstatedata_0 assertion.

Figure A-9 Ultra Low Power State (RX)



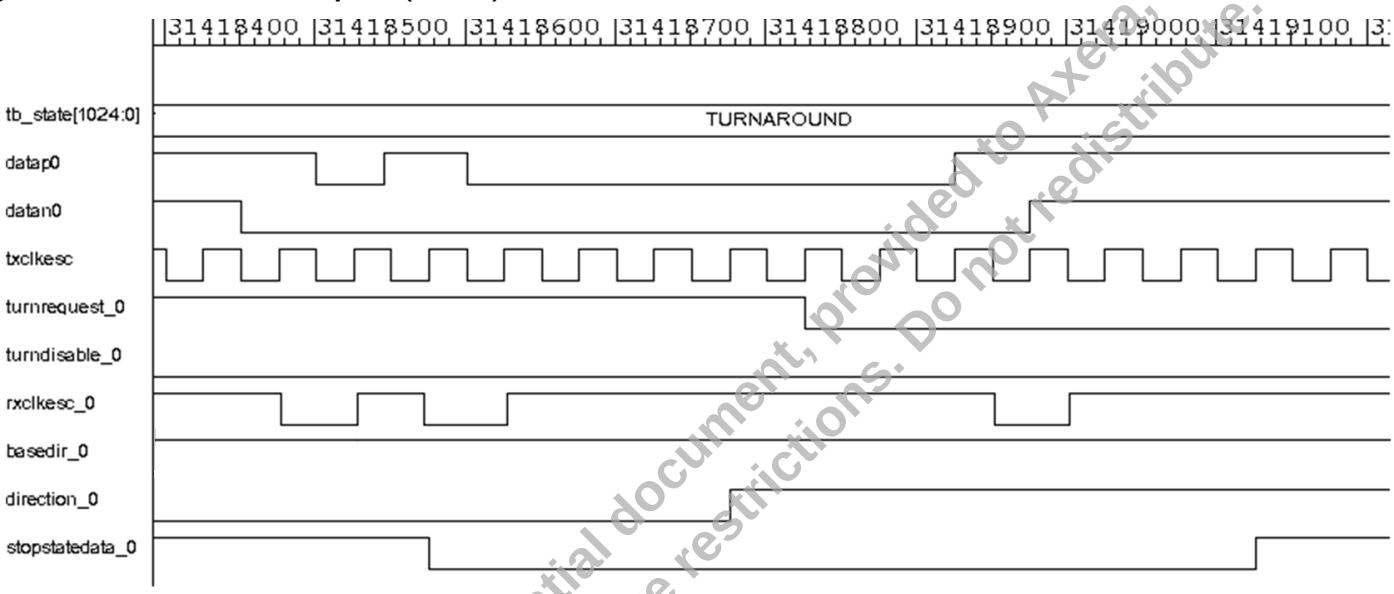
A.1.10 Turnaround Request (TX-RX)

Input sequence (TXCLKESC synchronous):

1. Set turnrequest_0 = 1'b1.
2. Wait until stopstatedata_0 is de-asserted.
3. Wait until direction_0 output is set to 1'b1.
4. Set turnrequest_0 = 1'b0.

Wait until stopstatedata_0 is asserted (turnaround procedure is completed).

Figure A-10 Turnaround Request (TX-RX)



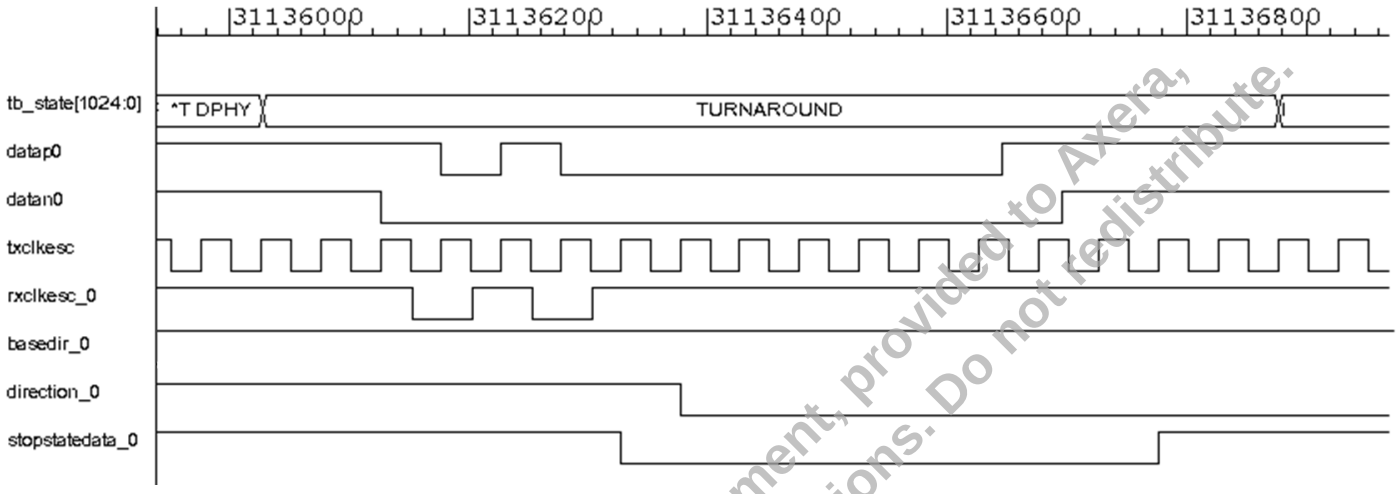
Note The Turnaround Request (TX-RX) is only available on data lane 0.

A.1.11 Turnaround Request (RX-TX)

Input sequence (TXCLKESC synchronous):

1. Wait until stopstatedata_0 is de-asserted.
2. Wait until direction_0 output is set to 1'b0.
3. Wait for the stopstatedata_0 assertion.

Figure A-11 Turnaround Request (RX-TX)



Note The Turnaround Request (RX-TX) is only available on data lane 0.

A.2 High-Speed Transition Times

Table A-4 provides the transition time for High Speed Entry (Low-Speed to High-Speed) and High-Speed Exit (High-Speed to Low-Speed).

Note

The High Speed Entry can be reduced for the minimum spec value of TLP = 50ns, if the high speed driver is always powered.

Bits [3:2] of Test registers with address 0x30, 0x40, 0x50, 0x80 and 0x90 should be set to 2'b11 after startup sequence, see "Start-Up Sequence" on page 78.

hstxthsrqst_datalane and hstxthsrqst_clklane counters must be programmed using the following testcodes:

- 0x70, 0x74 for hstxthsrqst_datalane
- 0x60, 0x64 for hstxthsrqst_clklane

PHY internal counters default values are set that for each hsfreqrange, Global Operation Timing Parameters should be met by default, but some adjustments may need to be done in those counters through the following test control registers because some of parameters depend on analog blocks timings, that vary in PVT.

- 0x64: hstxthsexit_clklane
- 0x61: hstxthsprpr_clklane
- 0x60: hstxthsrqst_clklane
- 0x63: hstxthstrail_clklane
- 0x62: hstxthszero_clklane
- 0x65: hstxthsclkpost_clklane
- 0x74: hstxthsexit_datalanes
- 0x71: hstxthsprpr_datalanes
- 0x70: hstxthsrqst_datalane
- 0x73: hstxthstrail_datalanes
- 0x72: hstxthszero_datalanes
- 0x75: gtp_extension_datalane
- 0x66: gtp_extension_clklane

Table A-4 High-Speed Transition Times

Datarate (Mbps)	hsfreqrange[6:0] (BIN)	High-Speed Entry LP->HS CLK LANE[a]	High-Speed Exit HS->LP CLK LANE[b]	High-Speed Entry LP->HS DATA LANE[c]	High-Speed Entry LP->HS DATA LANE (Considers HS CLK LANE ENTRY)[d]	High-Speed Exit HS->LP DATA LANE[e]	High-Speed Deskew Entry[f]	High-Speed Deskew Exit[g]
Range		Max BYTE						
80	0000000	21	17	15	35	10	35	5
90	0010000	23	17	16	39	10	38	5
100	0100000	22	17	16	37	10	38	5
110	0110000	25	18	17	43	11	41	5
120	0000001	26	20	18	46	11	44	5
130	0010001	27	19	19	46	11	45	5
140	0100001	27	19	19	46	11	46	5
150	0110001	28	20	20	47	12	48	5
160	0000010	30	21	22	53	13	51	5
170	0010010	30	21	23	55	13	53	5
180	0100010	31	21	23	53	13	54	5
190	0110010	32	22	24	58	13	56	5
205	0000011	35	22	25	58	13	59	5
220	0010011	37	26	27	63	15	63	5
235	0100011	38	28	27	65	16	65	5
250	0110011	41	29	30	71	17	70	5
275	0000100	43	29	32	74	18	74	5

Table A-4 High-Speed Transition Times (Continued)

Datarate (Mbps)	hsfreqrange[6:0] (BIN)	High-Speed Entry LP->HS CLK LANE[a]	High-Speed Exit HS->LP CLK LANE[b]	High-Speed Entry LP->HS DATA LANE[c]	High-Speed Entry LP->HS DATA LANE (Considers HS CLK LANE ENTRY)[d]	High-Speed Exit HS->LP DATA LANE[e]	High-Speed Deskew Entry[f]	High-Speed Deskew Exit[g]
300	0010100	45	32	35	80	19	80	5
325	0100101	48	33	36	86	18	85	5
350	0110101	51	35	40	91	20	92	5
400	0000101	59	37	44	102	21	102	5
450	0010110	65	40	49	115	23	114	5
500	0100110	71	41	54	126	24	124	5
550	0110111	77	44	57	135	26	133	5
600	0000111	82	46	64	147	27	146	5
650	0011000	87	48	67	156	28	154	5
700	0101000	94	52	71	166	29	165	5
750	0111001	99	52	75	175	31	174	5
800	0001001	105	55	82	187	32	187	5
850	0011001	110	58	85	196	32	194	5
900	0101001	115	58	88	206	35	204	5
950	0111010	120	62	93	213	36	213	5
1000	0001010	128	63	99	225	38	226	5
1050	0011010	132	65	102	234	38	233	5
1100	0101010	138	67	106	243	39	244	5

Table A-4 High-Speed Transition Times (Continued)

Datarate (Mbps)	hsfreqrange[6:0] (BIN)	High-Speed Entry LP->HS CLK LANE[a]	High-Speed Exit HS->LP CLK LANE[b]	High-Speed Entry LP->HS DATA LANE[c]	High-Speed Entry LP->HS DATA LANE (Considers HS CLK LANE ENTRY)[d]	High-Speed Exit HS->LP DATA LANE[e]	High-Speed Deskew Entry[f]	High-Speed Deskew Exit[g]
1150	0111011	146	69	112	259	42	256	5
1200	0001011	151	71	117	269	43	267	5
1250	0011011	153	74	120	273	45	273	5
1300	0101011	160	73	124	282	46	283	5
1350	0111100	165	76	130	294	47	295	5
1400	0001100	172	78	134	304	49	305	5
1450	0011100	177	80	138	314	49	315	5
1500	0101100	183	81	143	326	52	326	5
1550	0111101	191	84	147	339	52	336	5
1600	0001101	194	85	152	345	52	346	5
1650	0011101	201	86	155	355	53	355	5
1700	0101110	208	88	161	368	53	367	5
1750	0111110	212	89	165	378	53	377	5
1800	0001110	220	90	171	389	54	389	5
1850	0011110	223	92	175	401	54	399	5
1900	0101111	231	91	180	413	55	410	5
1950	0111111	236	95	185	422	56	419	5
2000	0001111	243	97	190	432	56	431	5

Table A-4 High-Speed Transition Times (Continued)

Datarate (Mbps)	hsfreqrange[6:0] (BIN)	High-Speed Entry LP->HS CLK LANE[a]	High-Speed Exit HS->LP CLK LANE[b]	High-Speed Entry LP->HS DATA LANE[c]	High-Speed Entry LP->HS DATA LANE (Considers HS CLK LANE ENTRY)[d]	High-Speed Exit HS->LP DATA LANE[e]	High-Speed Deskew Entry[f]	High-Speed Deskew Exit[g]
2050	1000000	248	99	194	442	58	440	5
2100	1000001	252	100	199	454	59	452	5
2150	1000010	259	102	204	460	61	461	5
2200	1000011	266	105	210	476	62	474	5
2250	1000100	269	109	213	481	63	481	5
2300	1000101	272	109	217	490	65	489	5
2350	1000110	281	112	225	502	66	503	5
2400	1000111	283	115	226	509	66	507	5
2450	1001000	282	115	226	510	67	507	5
2500	1001001	281	118	227	508	67	508	5

a. Cycles from txrequesthsclk is asserted till PHY starts driving High-Speed Clock signal in clocklane (Toggling HS-0/HS-1)
b. Cycles from txrequesthsclk is de-asserted till PHY drives LP11 internally in clocklane
c. Cycles from txrequestdatahs is asserted till payload data starts to be transmitted in the data lanes (if txrequestdatahs is asserted when clock lane is already toggling).
d. Cycles from txrequesthsclk and txrequestdatahs are asserted till PHY starts till payload data starts to be transmitted in the data lanes (considering txrequestdatahs and txrequesthsclk are asserted simultaneously).
e. Cycles from stopstate_n is asserted until PHY is ready to receive new txrequestdatahs request. Datalane0 stopstate signal is asserted later than the other datatalanes because of a internal syncronization, so the 67 byteclk cycles minimum requirement for 2.5 Gbps can be only take into consideration the other enabled datalanes stopstate_n signal. If single datalane and clocklane is used for some application this is not necessary and the new request can be done immediately after txreadyhs_n de-assertion.
f. Cycles from txskewcalhs assertion and sync pattern (16'hFFFF) being driven on the lines.
g. Cycles from txskewcalhs de-assertion and stop skew calibration pattern.