Low Power Techniques

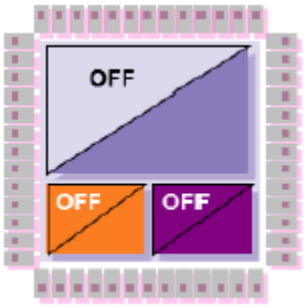
1 Overview

There are several RTL and gate-level design strategies for reducing power. This document describes the power reduction methods in the following sections:

- Power Gating
- Multi-Voltage Design (Multi-VDD)
- Dynamic Voltage and Frequency Scaling
- Adaptive Body-Biasing (ABB)
- Multiple-Vt Library Cells

2 Power Gating

Power gating is a power-saving technique in which portions of the chip are shut down temporarily during periods of inactivity, as illustrated in the following figure:



This technique reduces the leakage power of the chip. Power gating with state retention involves switching off an area of a design when its functionality is not required, then restoring power when it is required.

For example, in a cell phone chip, the block that performs voice processing can be shut down when the phone is in standby mode. When the user places a call or receives an outside call, the voice processing block must “wake up” from its powered-down state.

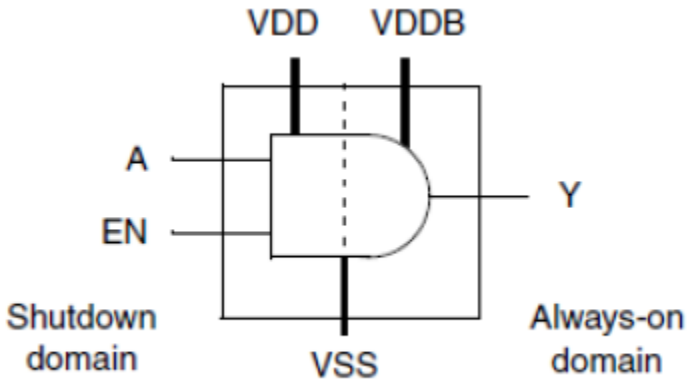
Power gating has the potential to reduce overall power consumption substantially because it lowers leakage power as well as switching power.

2.1 Shutdown

In this technique, the power supply of the entire design is shut off when the circuit is not in use. Such designs do not require data to be retained in registers or latches used in the design. Functional verification of the design is still required to make sure that the position of designs that are awake function properly and to ensure that the system would work when power is restored in the sleeping part of the device.

2.2 Isolation

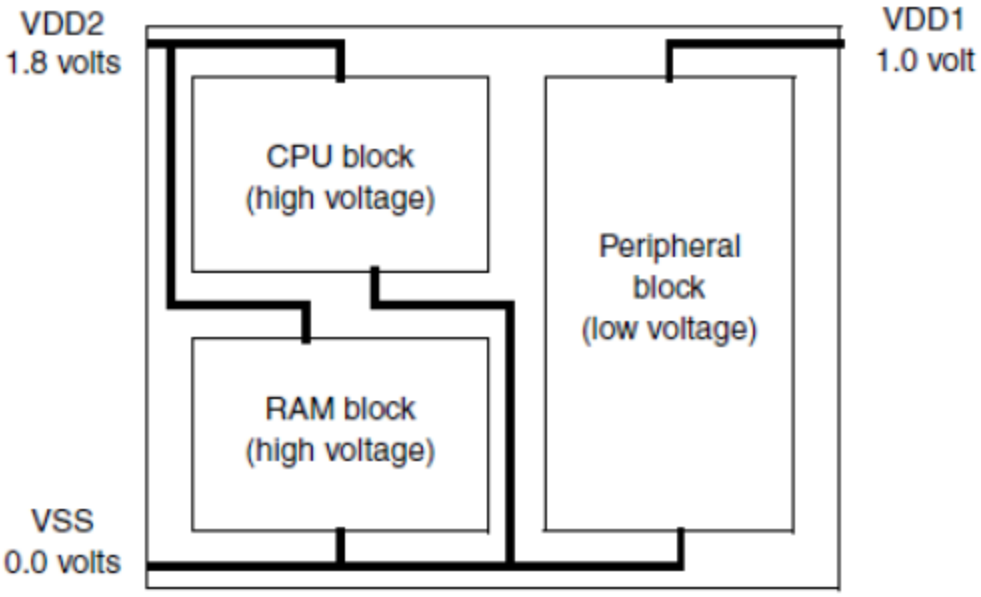
When the power is shut off, each power domain must be isolated from the rest of the design, so that it does not corrupt the downstream logic. Power shutdown results in slow output from the power gated blocks. These outputs spend a significant time at the threshold voltage, causing large crowbar currents in the always on blocks. Isolation cells are used to prevent these crowbar currents. The isolation cells are placed between the outputs of the power gated blocks and inputs of the always on blocks.
In a design with power gating, an isolation cell is required where each logic signal crosses from a power domain that can be powered down to a domain that is not powered down. The cell operates as a buffer when input and output sides of the cell are both powered up, but provides a constant output signal during times that the input side is powered down. An enable input controls the operating mode of the cell. An isolation cell is illustrated in the following figure:



3 Multi-Voltage Design (Multi-VDD)

In this technique, critical paths and blocks in the design are given access to maximum voltage for the process and the specification, but voltage is reduced for those blocks that need less power.

Different parts of a chip might have different speed requirements. For example, the CPU and RAM blocks might need to be faster than a peripheral block. As mentioned earlier, a lower supply voltage reduces power consumption, but also reduces speed. To get maximum speed and lower power at the same time, CPU and RAM can operate with a higher supply voltage while the peripheral block operates with a lower voltage, as shown in the following figure:

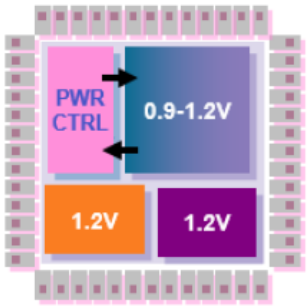


4 Dynamic Voltage and Frequency Scaling

In this technique, supply voltage and clock frequency is reduced based on workload that results in a quarter of the power consumption. Voltage scaling techniques can be of the following types:

- Dynamic - Here, a larger number of voltage levels are dynamically switched to follow changing workloads.
- Adaptive - Here, a closed loop feedback system is used to adjust the voltage.

The following figure illustrates dynamic voltage and frequency scaling:



5 Adaptive Body-Biasing (ABB)

This technique is used to control the leakage current during stand-by and active mode. Reverse body bias is used for stand-by mode and zero body bias is used for active mode. ABB method reduces the leakage current exponentially. When body-to-source junction is reversed biased, the voltage threshold increases, thus reducing the leakage.

6 Multiple-Vt Library Cells

Some CMOS technologies support the fabrication of transistors with different threshold voltages (Vt values). In that case, the cell library can offer two or more different cells to implement each logic function, each using a different transistor threshold voltage. For example, the library can offer two inverter cells: one using low-Vt transistors and another using high-Vt transistors.

In this technique, a low-threshold-voltage library is used for a first pass through synthesis to get maximum performance and meet timing goals. Thereafter, the critical paths in the design, that is, the path or paths in the design that require the highest performance, are determined. Later, areas that do not require low-threshold-voltage cells are located and low-voltage cells are swapped for high-voltage cells to reduce overall power and leakage of the design.

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