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# DFI

## DDR PHY Interface



**DFI 3.0 Specification**  
**18 May 2012**

Release Information			
Rev #	Date	Change	
1.0	30 Jan 2007	Initial Release	
2.0	17 Jul 2007	Modifications/Additions for DDR3 Support	
2.0	21 Nov 2007	Additional modifications/additions for DDR3 support. Added read and write leveling. Changes approved by the Technical Committee for DDR3 support.	
2.0	21 Dec 2007	Removed references to data eye training for PHY Evaluation mode, added a gate training-specific mode signal, corrected references and clarified read <u>training</u> .	
2.0	11 Jan 2008	Modified wording; standardized notations in figures, clarified terminology for read and write leveling.	
2.0	26 Mar 2008	Added timing parameter $t_{rdl\bar{v}l\_en}$ and $t_{wrl\bar{v}l\_en}$ , signal $dfi\_rdl\bar{v}l\_edge$	
2.1	2 Oct 2008	Added initial LPDDR2 support and corrected minor errors from 2.0 release	
2.1	24 Nov 2008	Added frequency change protocol, signal timing definitions, $t_{rdl\bar{v}l\_load}$ and $t_{wrl\bar{v}l\_load}$ timing parameters and adjusted diagrams accordingly	
2.1	30 Jan 2009	Added DFI logo	
2.1	31 Mar 2009	Updated width of $dfi\_rdl\bar{v}l\_edge$ , corrected erroneous figures, updated $t_{rdl\bar{v}l\_en}$ and $t_{wrl\bar{v}l\_en}$ definitions	
2.1	20 May 2009	Added low power control interface, modified leveling request signal description to include frequency change, added $dfi\_data\_byte\_disable$ signal and $t_{phy\_wrdata}$ timing parameters. Added DIMM support to the status interface and updated frequency ratios from an example to a defined method. Updated frequency ratios information for new proposals, modified default values and requirements for some training interface signals, incorporated LPDDR2 training operations changes	
2.1	22 Jun 2009	Expanded frequency ratio information to include vectored read data, expanded use of $dfi\_init\_start$ , added timing diagrams for 1:4 frequency ratio systems	
2.1.1	23 Mar 2010	Added reference to the parity interface to the Overview. Changed $dfi\_parity\_in$ signal to have a phase index. Modified description of $dfi\_freq\_ratio$ signal to make it optional except for MCs/PHYs that support multiple frequency ratios. Expanded figure 32 into two figures to represent odd and even timing parameters.	
2.1.1	01 Apr 2010	Changed minimum value for $t_{lp\_wakeup}$	
2.1.1	20 Apr 2010	Corrected figure 3 timing violation. Corrected erroneous sentence for 2T timing. Corrected figure 35 $t_{phy\_wrlat}$ timing. Correct incorrect references to $t_{phy\_wrlat}$ in frequency ratio read examples.	

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2.1.1	27 May 2010	Added Figure 4 and text to explain differences between Figure 3 and 4.
2.1.1	09 Jun 2010	Modified text in dfi_init_start and surrounding figures 3 and 4 for more clarity.
3.0	21 May 2012	Added DDR4 DRAM support for: CRC, CA parity timing, CRC and CA parity errors, DBI, leveling support, and CA modifications. Added DFI read data rotation clarification, read data pointer resynchronization, independent timing of DFI read data valid per data slice, data path chip select, error interface, and programmable parameters. Renamed PHY evaluation mode. Removed MC evaluation mode and $t_{phy\_wrdelay}$ timing parameter. Added support for refresh during training, multiple CS training, enhancements to the update interface and the idle bus definition.

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## 1.0 Overview

The DDR PHY Interface (DFI) is an interface protocol that defines the signals, timing parameters, and programmable parameters required to transfer control information and data over the DFI, to and from the DRAM devices, and between the MC and the PHY. The programmable parameters are options defined by the MC, PHY, or system and programmed into the MC and/or the PHY. DFI applies to: DDR4, DDR3, DDR2, DDR1, LPDDR2 and LPDDR1 DRAMs.

The DFI protocol does not encompass all of the features of the MC or the PHY, nor does the protocol put any restrictions on how the MC or the PHY interface to other aspects of the system.

This specification is organized by the interface groups listed in Table 1.

**TABLE 1.***Interface Groups*

Interface Group	Description
Control	Required to drive the address, command, and control signals to the DRAM devices.
Write Data	Used to send write and receive valid read data across the DFI.
Read Data	
Update	Provides an ability for the MC or the PHY to interrupt and idle the DFI.
Status	Used for system initialization, feature support, and to control the presence of valid clocks to the DRAM interface.
Training	Used to execute gate training, read data eye training, and write leveling operations.
Low Power Control	Allows the PHY to enter power-saving modes.
Error	Used to communicate error information from the PHY to the MC.

Within each interface group are signals and parameters. Some signals are applicable only to certain DRAM types. All of the DFI signals must use the corresponding parameters.

The DFI signals associated with each interface group, and the device originating the signal, are shown in Figure 1, “Block Diagram of Interface Signals: Control, Write, Read, Update and Status,” on page 17, and Figure 2, “Block Diagram of Interface Signals: Training, Low Power Control and Error,” on page 18. The signal requirements and parameters associated with each signal are listed in Table 2, “DFI Signal Requirements,” on page 19. Other signals may exist between the MC and the PHY for a particular implementation.

Changes in the DFI protocol between versions may result in incompatibilities between MCs and PHYs which were designed to adhere to different versions of the DFI specification. If using devices designed for different versions of the DFI specification, review the changes associated with the corresponding versions and ensure changes will not interfere with interoperability in a specific configuration.

All figures are provided for illustrative purposes only. Timing diagrams may illustrate condensed or otherwise unrealistic signal timing.

A glossary of terminology used in this specification can be found in Table 28, “Glossary of Terms,” on page 131.

## 2.0 Architecture

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The DFI specification requires a DFI clock and DFI-defined signals that must be driven directly by registers referenced to a rising edge of the DFI clock. There are no rules dictating the source of the DFI clock, nor are there restrictions on how the DFI-defined signals are received. For DFI interoperability between the MC and the PHY, ensure compatibility in:

- Signal widths
- Interconnect timing
- Timing parameters
- Frequency ratio
- Function

Interconnect timing compatibility between the MC and the PHY at target frequencies is determined by the specification of the output timing for signals driven and the setup and hold requirements to receive these signals on the DFI per device, as defined by the device.

The DFI specification does not dictate absolute latencies or a fixed range of values that must be supported by each device. Certain DFI timing parameters can be specified as fixed values, maximum values, or as constants based on other values in the system.

DFI timing parameters must be held constant while commands are being executed on the DFI bus; however, if necessary, DFI timing parameters may be changed during a frequency change or while the bus is in the idle state. For more information on timing, refer to Section 5.0, “Signal Timing,” on page 127.

The DFI specification identifies the DFI signals relevant to a specific implementation based upon support for specific DRAM device(s), optional features, and frequency ratio. For more information on which signals are relevant to a specific implementation, refer to Table 2, “DFI Signal Requirements,” on page 19.

The MC and the PHY must operate at a common frequency ratio. For matched frequency systems, the DFI write data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, the DFI write data bus width will be multiplied proportional to the frequency ratio to allow the MC to send all of the DRAM-required write data to the PHY in a single DFI clock cycle. The write data must be delivered with the DFI data words aligned in ascending order.

- In a matched frequency system, the MC and the PHY operate with a 1:1 ratio.
- In a frequency ratio system, the MC and the PHY operate with a common frequency ratio of 1:2 or 1:4; the PHY must be able to accept a command on any and all phases. The frequency ratio depends on the relationship of the reference clocks for the MC and the PHY.

Phase-specific signals with a suffix of “\_pN”, with the phase number N (e.g., **dfi\_wrdata\_pN**), replace the matched frequency signals for the control, write data,

read data, and status interface signals. Phase-specific signals allow the MC to drive multiple commands in a single clock cycle.

Data word-specific signals with a suffix of “\_wN”, with the DFI data word number N (e.g., **dfi\_rddata\_wN**), replace the matched frequency signals for the read interface to distinguish how DRAM words are transferred across the DFI bus.

Variable pulse width-specific signals with a suffix of “\_aN”, with the PHY clock cycle N (e.g., **dfi\_alert\_n\_aN**), replace the matched frequency signals for the status interface to maintain the pulse width during transmission of error signals from the memory system to the PHY.

For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional.

For more information on frequency ratios, refer to Section 4.8, “Frequency Ratios Across the DFI”.

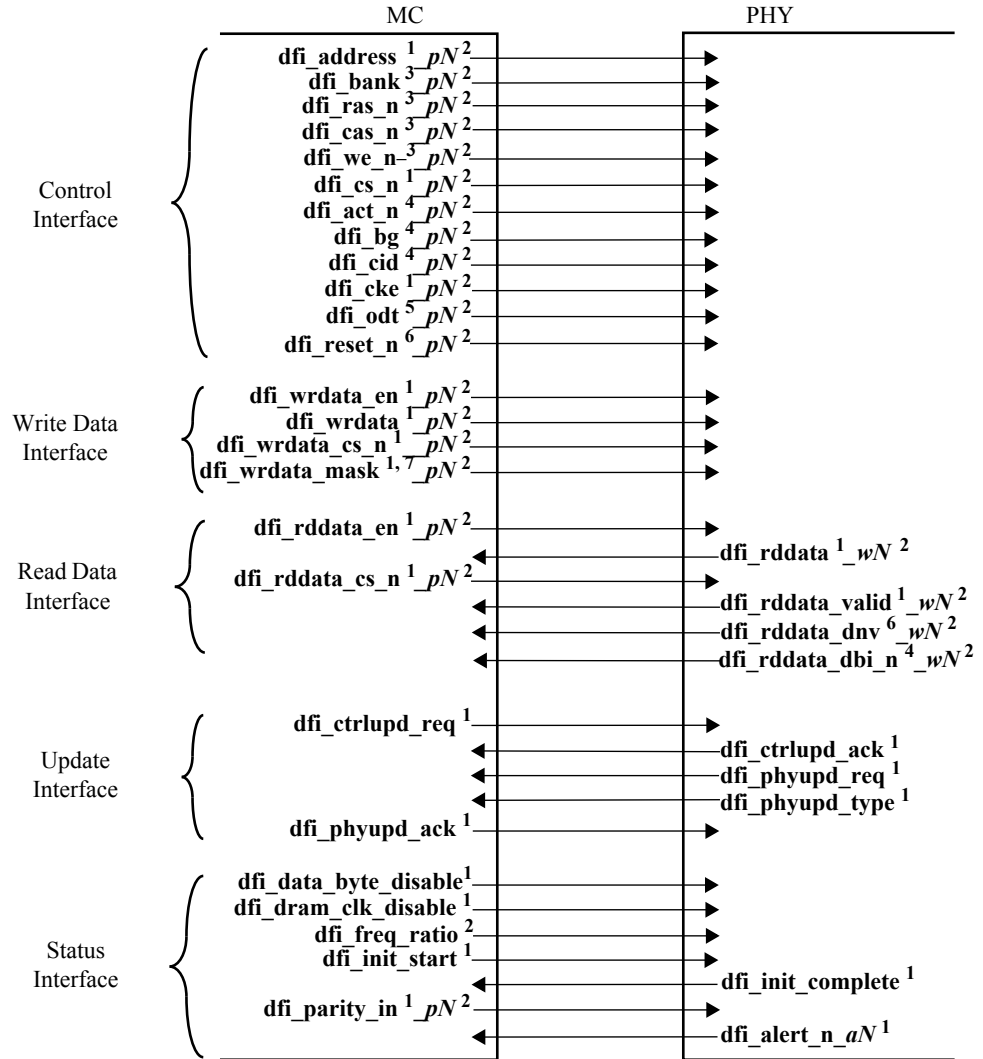
Optional protocols handle data bus inversion (DBI), cyclic redundancy check (CRC), system frequency change, command/address (CA) parity, low power, and the error interface. For more information on optional protocols, refer to Section 4.3, “Data Bus Inversion,” on page 64, Section 4.4.3, “Cyclic Redundancy Check,” on page 73, Section 4.9, “Frequency Change,” on page 109, Section 4.10, “Parity,” on page 111, Section 4.12, “Low Power Control Handshaking,” on page 124, and Section 4.13, “Error Signaling,” on page 126.

The DRAM type and system configuration determine the types of training available to a system; a system may or may not utilize each type of training. If training is supported, the system may utilize DFI training or support a different training method.

The DFI signals associated with control/write data/read data/update/status interface groups, and the device originating the signals, are listed functionally within each interface group in Figure 1, “Block Diagram of Interface Signals: Control, Write, Read, Update and Status,” on page 17. The DFI signals associated with the training/low power/error interface groups, and the device originating the signals, are listed functionally within each interface group in Figure 2, “Block Diagram of Interface Signals: Training, Low Power Control and Error,” on page 18.



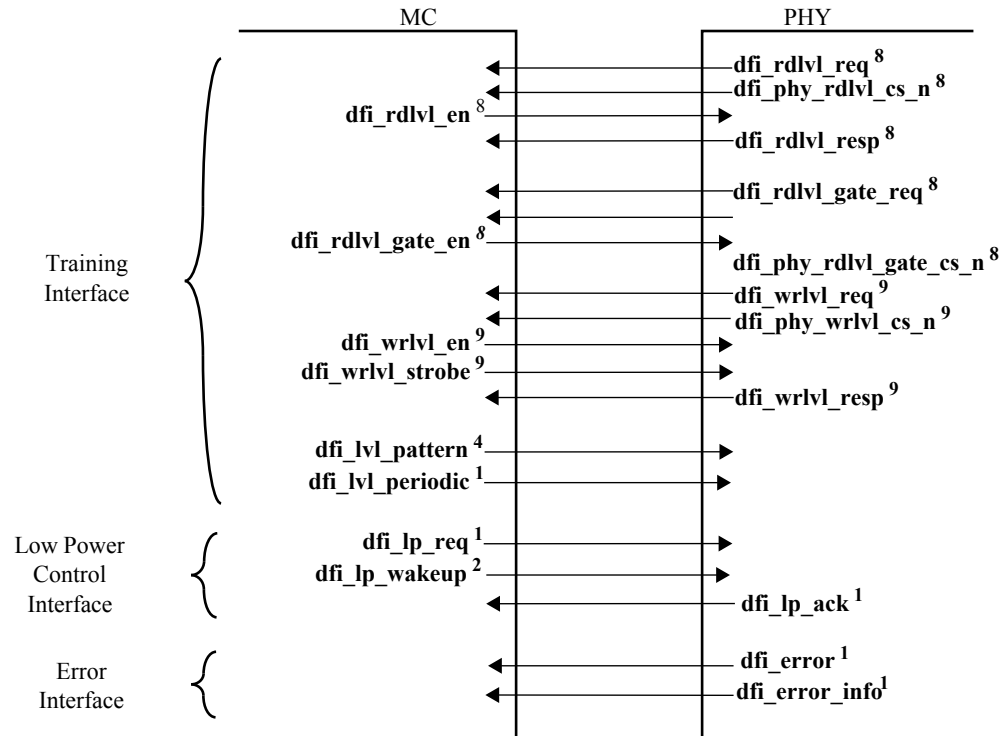
**FIGURE 1.** Block Diagram of Interface Signals: Control, Write, Read, Update and Status



1. Used by all DRAMs.
  2. Optional suffix for frequency ratio systems.
  3. Used with DDR4, DDR3, DDR2, DDR1 and LPDDR1 DRAMs.
  4. Used with DDR4 DRAMs only.
  5. Used with DDR4, DDR3 and DDR2 DRAMs.
  6. Used with LPDDR2 DRAM only.
  7. Dual-function signal. In DDR4 systems with write DBI enabled, the signal transforms from a mask to a write DBI signal.
  8. Used with DDR4, DDR3 and LPDDR2 DRAMs.
  9. Used with DDR4 and DDR3 DRAMs.
- Italicized text indicates that the phase/word/cycle is optional.*

FIGURE 2.

Block Diagram of Interface Signals: Training, Low Power Control and Error



1. Used with all DRAMs.
2. Optional suffix for frequency ratio systems.
3. Used with DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs.
4. Used with DDR4 DRAMs only.
5. Used with DDR4, DDR3 and DDR2 DRAMs.
6. Used with LPDDR2 DRAM only.
7. Dual-function signal. In DDR4 systems with write DBI enabled, the signal transforms from a mask to a write DBI signal.
8. Used with DDR4, DDR3 and LPDDR2 DRAMs.
9. Used with DDR4 and DDR3 DRAMs.

*Italicized text indicates that the phase/word/cycle is optional.*

To determine which signals are required for a specific configuration, review Table 2, “DFI Signal Requirements,” on page 19. This table identifies the signals associated with each interface group, the parameters associated with each signal, and whether the signal is applicable, required, or optional for each device.

Each signal is device-specific and has corresponding parameters which must be used. Multiple parameter types may apply to a signal. Timing parameters are indicated with the prefix **t** (e.g., **t<sub>xxxxx</sub>**). Programmable parameters are indicated with a prefix to indicate the defining device and a suffix (e.g., **phy<sub>xxxx</sub>\_en**). The signals are listed functionally within each interface group.

**TABLE 2.** *DFI Signal Requirements*

Control Interface Group			
Signal	Associated Parameters	MC	PHY
<b>dfi_address_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for all DRAMs. Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs. Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_bank_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_ras_n_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_cas_n_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_we_n_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. <sup>b</sup> Suffix ( <b>_pN</b> ) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>

<b>dfi_cs_n_pN</b>	<b>t<sub>cmd_lat</sub></b> <b>t<sub>ctrl_delay</sub></b>	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_act_n_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4. <sup>b</sup>	Required for DDR4. <sup>b</sup>
<b>dfi_bg_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4. <sup>b</sup>	Required for DDR4. <sup>b</sup>
<b>dfi_cid_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4. <sup>b</sup>	Required for DDR4. <sup>b</sup>
<b>dfi_cke_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for all DRAMs Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_odt_pN</b>	<b>phy<sub>cre_mode</sub></b> <b>t<sub>ctrl_delay</sub></b>	Required for DDR4, DDR3 and DDR2 DRAMs. <sup>b</sup> Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for DDR4, DDR3, and DDR2 DRAMs. <sup>b</sup> Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_reset_n_pN</b>	<b>t<sub>ctrl_delay</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup> Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup> Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>Write Interface Group</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_wrdata_en_pN</b>	<b>phy<sub>cre_mode</sub></b> <b>t<sub>cmd_lat</sub></b> <b>t<sub>phy_crcmax_lat</sub></b> <b>t<sub>phy_crcmin_lat</sub></b> <b>t<sub>phy_wrdata</sub></b> <b>t<sub>wrdata_delay</sub></b> <b>t<sub>phy_wrlat</sub></b> <b>dfi<sub>rw_length</sub></b>	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_wrdata_pN</b>	<b>phy<sub>cre_mode</sub></b> <b>t<sub>phy_wrdata</sub></b> <b>t<sub>phy_wrlat</sub></b>	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>

<b>dfi_wrdata_cs_n_pN</b>	<b>t<sub>phy_wrcsgap</sub></b> <b>t<sub>phy_wrcslat</sub></b>	Required for all DRAMs if any of the training features are supported, otherwise optional.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Optional.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_wrdata_mask_pN</b>	<b>phy<sub>erc</sub>_mode</b> <b>t<sub>phy_wrdata</sub></b> <b>t<sub>phy_wrlat</sub></b>	Required for all DRAMs.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>Read Interface Group</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_rddata_en_pN</b>	<b>t<sub>phy_rdlat</sub></b> <b>t<sub>rddata_en</sub></b> <b>dfi<sub>rw</sub>_length</b>	Required for all DRAMs.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_rddata_wN</b>	<b>t<sub>phy_rdlat</sub></b> <b>t<sub>rddata_en</sub></b>	Required for all DRAMs.  Suffix (_wN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Required for all DRAMs.  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>
<b>dfi_rddata_cs_n_pN</b>	<b>t<sub>phy_rdcsgap</sub></b> <b>t<sub>phy_rdeslat</sub></b>	Required for all DRAMs if read training is supported, otherwise optional.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Optional.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_rddata_valid_wN</b>	<b>t<sub>phy_rdlat</sub></b> <b>t<sub>rddata_en</sub></b>	Required for all DRAMs.  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>	Required for all DRAMs.  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>
<b>dfi_rddata_dnv_wN</b>	<b>t<sub>phy_rdlat</sub></b> <b>t<sub>rddata_en</sub></b>	Required for LPDDR2 DRAM. <sup>b</sup>  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>	Required for LPDDR2 DRAM. <sup>b</sup>  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>
<b>dfi_rddata_dbi_n_wN</b>	<b>phy<sub>dbi</sub>_mode</b> <b>t<sub>phy_rdlat</sub></b> <b>t<sub>rddata_en</sub></b>	Applicable for DDR4 only.  Required when MC DBI support is enabled and <b>phy<sub>dbi</sub>_mode</b> =0.  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>	Applicable for DDR4 only.  Required when MC DBI support is enabled and <b>phy<sub>dbi</sub>_mode</b> =0.  Suffix (_wN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>
<b>Update Interface Group</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>

<b>dfi_ctrlupd_req</b>	$t_{ctrlupd\_interval}$ $t_{ctrlupd\_max}$ $t_{ctrlupd\_min}$ $t_{phyupd\_type0}$ $t_{phyupd\_type1}$ $t_{phyupd\_type2}$ $t_{phyupd\_type3}$ $t_{phyupd\_resp}$	Required for all DRAMs.	Optional.
<b>dfi_ctrlupd_ack</b>	$t_{ctrlupd\_min}$ $t_{ctrlupd\_max}$	Required for all DRAMs.	Optional.
<b>dfi_phyupd_req</b>	$t_{phyupd\_type0}$ $t_{phyupd\_type1}$ $t_{phyupd\_type2}$ $t_{phyupd\_type3}$ $t_{phyupd\_resp}$	Required for all DRAMs.	Optional.
<b>dfi_phyupd_type</b>	$t_{phyupd\_type0}$ $t_{phyupd\_type1}$ $t_{phyupd\_type2}$ $t_{phyupd\_type3}$	Required for all DRAMs.	Optional.
<b>dfi_phyupd_ack</b>	$t_{phyupd\_type0}$ $t_{phyupd\_type1}$ $t_{phyupd\_type2}$ $t_{phyupd\_type3}$ $t_{phyupd\_resp}$	Required for all DRAMs.	Optional.
<b>Status Interface Group</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_data_byte_disable</b>		Optional.	Optional.
<b>dfi_dram_clk_disable</b>	$t_{dram\_clk\_disable}$ $t_{dram\_clk\_enable}$	Required for all DRAMs.	Required for all DRAMs.
<b>dfi_freq_ratio</b>		Required if the system supports multiple frequency ratios. <sup>b</sup> Not applicable if the system supports a single ratio.	Required if the system supports multiple frequency ratios. Not applicable if the system supports a single ratio.

<b>dfi_init_start</b>	<b>t<sub>init_start</sub></b> <b>t<sub>init_complete</sub></b>	Applicable if device supports data byte disabling, multiple frequency ratios, or the frequency change protocol.  Required for systems supporting frequency change.	Applicable if device supports data byte disabling, multiple frequency ratios, or the frequency change protocol.  Required for systems supporting frequency change.
<b>dfi_init_complete</b>	<b>t<sub>init_start</sub></b> <b>t<sub>init_complete</sub></b>	Required for all DRAMs.	Required for all DRAMs.
<b>dfi_parity_in_pN</b>	<b>t<sub>parin_lat</sub></b>	Optional. Only relevant for PHYs that support command parity and require the MC to generate the parity information.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>	Optional. Only relevant for PHYs that support command parity and require the MC to generate the parity information.  Suffix (_pN) required for frequency ratio systems to replicate information across the phases. <sup>a</sup>
<b>dfi_alert_n_aN</b>	<b>phy_crc_mode</b> <b>t<sub>parin_lat</sub></b> <b>t<sub>phy_crcmax_lat</sub></b> <b>t<sub>phy_crcmin_lat</sub></b>	Optional. Only relevant for PHYs that support command parity and require the MC to generate the parity information.  Suffix (_aN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>	Optional. Only relevant for PHYs that support command parity and require the MC to generate the parity information.  Suffix (_aN) required for frequency ratio systems to replicate information across the word. <sup>a</sup>
<b>Training Interface Group - Read Training</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_rdlvl_req</b>	<b>t<sub>rdlvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Optional.  Only applicable when read training is supported.
<b>dfi_phy_rdlvl_cs_n</b>	<b>t<sub>rdlvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Optional.  Only applicable when read training is supported.
<b>dfi_rdlvl_en</b>	<b>t<sub>rdlvl_en</sub></b> <b>t<sub>rdlvl_max</sub></b> <b>t<sub>rdlvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Required for DDR4, DDR3 and LPDDR2 DRAMs when read training is supported. <sup>b</sup>
<b>dfi_rdlvl_resp</b>	<b>t<sub>rdlvl_max</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Required for DDR4, DDR3 and LPDDR2 DRAMs when read training is supported. <sup>b</sup>
<b>dfi_rdlvl_gate_req</b>	<b>t<sub>rdlvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Optional.  Only applicable when read training is supported.
<b>dfi_phy_rdlvl_gate_cs_n</b>	<b>t<sub>rdlvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Optional.  Only applicable when read training is supported.

<b>dfi_rdlvl_gate_en</b>	<b>t<sub>rdlrvl_en</sub></b> <b>t<sub>rdlrvl_max</sub></b> <b>t<sub>rdlrvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Required for DDR4, DDR3 and LPDDR2 DRAMs when read training is supported. <sup>b</sup>
<i>(not associated with a signal)</i>	<b>phy<sub>rdlrvl_en</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Required for DDR4, DDR3 and LPDDR2 DRAMs when read training is supported. <sup>b</sup>
<i>(not associated with a signal)</i>	<b>phy<sub>rdlrvl_gate_en</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs. <sup>b</sup>	Required for DDR4, DDR3 and LPDDR2 DRAMs when read training is supported. <sup>b</sup>
<b>Training Interface Group - Write Leveling</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_wrlvl_req</b>	<b>t<sub>wrlvl_resp</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup>	Optional when write leveling is supported.
<b>dfi_phy_wrlvl_cs_n</b>	<b>t<sub>wrlvl_resp</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup>	Optional when write leveling is supported.
<b>dfi_wrlvl_en</b>	<b>t<sub>wrlvl_en</sub></b> <b>t<sub>wrlvl_max</sub></b> <b>t<sub>wrlvl_resp</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup>	Required for DDR4 and DDR3 DRAMs when write leveling is supported. <sup>b</sup>
<b>dfi_wrlvl_strobe</b>	<b>t<sub>wrlvl_en</sub></b> <b>t<sub>wrlvl_ww</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup>	Required for DDR4 and DDR3 DRAMs when write leveling is supported. <sup>b</sup>
<b>dfi_wrlvl_resp</b>	<b>t<sub>wrlvl_max</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup>	Required for DDR4 and DDR3 DRAMs when write leveling is supported. <sup>b</sup>
<i>(not associated with a signal)</i>	<b>phy<sub>wwlrvl_en</sub></b>	Required for DDR4 and DDR3 DRAMs. <sup>b</sup>	Required for DDR4 and DDR3 DRAMs when write leveling is supported. <sup>b</sup>
<b>Training Interface Group - Leveling</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_lvl_pattern</b>	<b>t<sub>rdlrvl_en</sub></b> <b>t<sub>rdlrvl_max</sub></b> <b>t<sub>rdlrvl_resp</sub></b>	Required for DDR4. <sup>b</sup>	Required for DDR4. <sup>b</sup>
<b>dfi_lvl_periodic</b>	<b>t<sub>rdlrvl_en</sub></b> <b>t<sub>rdlrvl_max</sub></b> <b>t<sub>rdlrvl_resp</sub></b> <b>t<sub>wrlvl_en</sub></b> <b>t<sub>wrlvl_max</sub></b> <b>t<sub>wrlvl_resp</sub></b>	Required for DDR4, DDR3 and LPDDR2 DRAMs.	Optional.



<b>Low Power Control Interface Group (optional)</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_lp_req</b>	$t_{lp\_resp}$	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
<b>dfi_lp_wakeup</b>	$t_{lp\_wakeup}$	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
<b>dfi_lp_ack</b>	$t_{lp\_resp}$ $t_{lp\_wakeup}$	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
<b>Error Interface Group (optional)</b>			
<b>Signal</b>	<b>Associated Parameters</b>	<b>MC</b>	<b>PHY</b>
<b>dfi_error</b>	$t_{error\_resp}$	Supported for all DRAM types. Required when error interface is supported.	Supported for all DRAM types. Required when error interface is supported.
<b>dfi_error_info</b>	$t_{error\_resp}$	Optional.	Optional.

- a. For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase  $N$  ( $pN$ )/data word  $N$  ( $wN$ )/clock cycle  $N$  ( $aN$ ), as applicable. The phase 0 suffixes are not required.
- b. Other DRAMs must hold this signal in the idle state.

## 3.0 Interface Signal Groups

### 3.1 Control Interface

The control interface handles the transmission of signals required to drive the address, command, and control signals to the DRAM devices; the interface includes signals and timing parameters. The signals are intended to be passed to the DRAM devices in a manner that maintains the timing relationship among the signals on the DFI; the  $t_{ctrl\_delay}$  timing parameter defines the delay introduced between the DFI interface and the DRAM interface.

Some of the control interface signals are DRAM technology-specific and are only required if the associated technology is used. Examples of DRAM technology-specific control interface signals are:




- **dfi\_reset\_n** is specific to DDR4 and DDR3 DRAMs
- **dfi\_odt** is specific to DDR4, DDR3, and DDR2 DRAMs

For LPDDR2 DRAMs, the CA bus is mapped onto to the **dfi\_address** bus. The following signals must be held at constant values when present in an LPDDR2 implementation: **dfi\_cid**, **dfi\_bank**, **dfi\_bg**, **dfi\_act\_n**, **dfi\_ras\_n**, **dfi\_cas\_n** and **dfi\_we\_n**. The **dfi\_address** bus must have a minimum of 20 bits to hold the LPDDR2 rising and falling DDR CA bus for the entire clock period. The PHY is responsible for transmitting the 20-bit **dfi\_address** bus as a double data rate 10-bit output, transmitting to the LPDDR2 DRAM on the rising and falling CA phases. The LPDDR2 interface mapping is detailed in Table 3, “Bit Definitions of the dfi\_address bus for LPDDR2”.

For frequency ratio systems, the buses/signals of the control interface are replicated into phase-specific signals with a suffix of “\_pN” that defines the signal value for each phase N of the DFI PHY clock. Phase 0 may exclude the suffix if desired. The MC may issue commands on any phase to communicate with the PHY. For example, the MC may issue commands only on a single phase, such as phase 0, or may issue commands on any combination of phases; the PHY must be able to accept a command on any and all phases.

TABLE 3.

*Bit Definitions of the dfi\_address bus for LPDDR2*

dfi_address		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CA Bus		LPDDR2 1										9	8	7	6	5	4	3	2	1	0
		LPDDR2 2																			
		9	8	7	6	5	4	3	2	1	0										

For more information on the control interface, refer to Section 4.2, “Control Signals,” on page 62. The signals and parameters in the control interface are listed in Table 4 and Table 5.

For more information on the control interface, refer to Section 4.2, “Control Signals,” on page 62. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the control interface are listed in Table 4, “Control Signals”.

**TABLE 4.** *Control Signals*

Signal	From	Width	Default	Description
<b>dfi_act_n</b> or <b>dfi_act_n_pN</b> <sup>a</sup>	MC	1-bit	_b	<u>Activation command</u> . This signal is asserted as a bank activate command.
<b>dfi_address</b> or <b>dfi_address_pN</b> <sup>a</sup>	MC	DFI Address Width	_b, c	<u>DFI address bus</u> . These signals define the address information.  The PHY must preserve the bit ordering of the <b>dfi_address</b> signals when reflecting this data to the DRAM devices.  For DDR4 DRAMs, the <b>dfi_address</b> bus defines the column address and a portion of the row address. DDR4 devices do not use the <b>dfi_address</b> bits [16:14] since DDR4 devices transmit the row address bits [16:14] on <b>dfi_ras_n</b> , <b>dfi_cas_n</b> , and <b>dfi_we_n</b> .  For larger density devices, <b>dfi_address</b> bits A17 and above are utilized. Consequently, when a larger density device interfaces with a DDR4 system, there can be gaps in the address bus.  For systems that support multiple DRAM classes, all or a subset of the <b>dfi_address</b> bits [16:14] can be used to address a non-DDR4 DRAM.  For LPDDR2 DRAMs, the <b>dfi_address</b> bus maps to the CA bus as described in Section 3.1, “Control Interface,” on page 26.
<b>dfi_bank</b> or <b>dfi_bank_pN</b> <sup>a</sup>	MC	DFI Bank Width	_b	<u>DFI bank bus</u> . These signals define the bank information.  The PHY must preserve the bit ordering of the <b>dfi_bank</b> signals when reflecting DFI bank data to the DRAM devices.
<b>dfi_bg</b> or <b>dfi_bg_pN</b> <sup>a</sup>	MC	DFI Bank Group Width	_b	<u>DFI bank group</u> . This signal defines the bank group of a command.
<b>dfi_cas_n</b> or <b>dfi_cas_n_pN</b> <sup>a</sup>	MC	DFI Control Width	0x1 <sup>d</sup>	<u>DFI column address strobe</u> . This signal defines the column address strobe information.
<b>dfi_cid</b> or <b>dfi_cid_pN</b> <sup>a</sup>	MC	DFI Data Width/8	_b	<u>DFI Chip ID</u> . This signal defines the chip ID.  The <b>dfi_cid</b> signal is required for 3D stacked solutions.
<b>dfi_cke</b> or <b>dfi_cke_pN</b> <sup>a</sup>	MC	DFI Chip Select Width	0x0 <sup>e</sup> 0x1 <sup>e</sup>	<u>DFI clock enable</u> . This signal defines the clock enable.  The MC must drive CKE signals in all phases. The PHY must be able to accept a command on any and all phases for DFI frequency ratio compliance.

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_cs_n</b> or <b>dfi_cs_n_pN</b> <sup>a</sup>	MC	DFI Chip Select Width	0x1	<u>DFI chip select</u> . This signal defines the chip select.
<b>dfi_odt</b> or <b>dfi_odt_pN</b> <sup>a</sup>	MC	DFI Chip Select Width	0x0	<u>DFI on-die termination control bus</u> . These signals define the ODT. The MC must drive ODT signals in all phases. The PHY must be able to accept a command on any and all phases for DFI frequency ratio compliance.
<b>dfi_ras_n</b> or <b>dfi_ras_n_pN</b> <sup>a</sup>	MC	DFI Control Width	0x1 <sup>d</sup>	<u>DFI row address strobe bus</u> . These signals define the row address strobe.
<b>dfi_reset_n</b> or <b>dfi_reset_n_pN</b> <sup>a</sup>	MC	DFI Chip Select Width	0x0 0x1 <sup>f</sup>	<u>DFI reset bus</u> . These signals define the RESET. Reset signals are only required for DFI DDR4 and DDR3 support.
<b>dfi_we_n</b> or <b>dfi_we_n_pN</b> <sup>a</sup>	MC	DFI Control Width	0x1 <sup>d</sup>	<u>DFI write enable signal</u> . This signal defines the write enable.

- For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N(aN), as applicable. The phase 0 suffixes are not required.
- This signal is not meaningful during initialization; no default value is required.
- For LPDDR2 memory systems, the **dfi\_address** bus must be driven with an NOP until **dfi\_init\_complete** is asserted.
- This signal has multiple purposes with DDR4 devices. For all commands that have **dfi\_act\_n** de-asserted, this signal communicates command encoding similar to the functionality defined for other DRAM devices. When **dfi\_act\_n** is asserted, the signal transmits upper row address bits with the following address mapping: **dfi\_cas\_n** → A15, **dfi\_ras\_n** → A16, **dfi\_we\_n** → A14.
- Most DRAMs define CKE as low at reset; some devices, such as Mobile DDR, define CKE as high at reset. The default value should reflect the DRAM definition.
- In general, the **dfi\_reset\_n** signal is defined as low at reset; however, in some cases it may be necessary to hold **dfi\_reset\_n** high during initialization.

The timing parameters associated with the control interface are listed in Table 5, “Control Timing Parameters”.

**TABLE 5.** *Control Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
<b>t<sub>cmd_lat</sub></b>	MC	0	_a	DFI PHY clock cycles <sup>b</sup>	Specifies the number of DFI clocks after the <b>dfi_cs_n</b> signal is asserted until the associated CA bus is driven.

Parameter	Defined By	Min	Max	Unit	Description
$t_{ctrl\_delay}$	PHY	0	a	DFI clock cycles	Specifies the number of DFI clock cycles that occur between any control signal change and when the change reaches the DRAM interface. If the DFI clock and the DRAM clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.

- The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.
- For matched frequency systems, a DFI PHY clock is identical to the DFI clock. For frequency ratio systems, this timing parameter is defined in terms of DFI PHY clock cycles.

## 3.2 Write Data Interface

The write data interface handles the transmission of write data across the DFI; the interface includes signals, timing parameters, and programmable parameters.

Table 6, “Write Data Signals,” on page 31 describes the signals **dfi\_wrddata** (write data bus), **dfi\_wrddata\_cs\_n** (write data chip select), **dfi\_wrddata\_en** (write data and data mask enable), and **dfi\_wrddata\_mask** (write data byte mask).

The **dfi\_wrddata** bus transfers write data from the MC to the PHY. The **dfi\_wrddata\_en** signal indicates to the PHY that valid **dfi\_wrddata** will be transmitted in  $t_{phy\_wrddata}$  cycles.

### 3.2.1 Write Data Mask/Write DBI

The **dfi\_wrddata\_mask** signal has two mutually exclusive functions. If the DBI feature (described in Section 4.3, “Data Bus Inversion,” on page 64) is not enabled, then **dfi\_wrddata\_mask** defines the bytes within the **dfi\_wrddata** signals that will be written to DRAM. Alternately, if the DBI feature is enabled and **phydbi\_mode**=0, the **dfi\_wrddata\_mask** signal is no longer a mask, instead it becomes a write DBI signal and indicates whether the write data is inverted

### 3.2.2 Write Data Chip Select

If data chip select is enabled, the **dfi\_wrddata\_cs\_n** signal indicates which chip select is accessed for the associated write data to independently compensate for timing differences on the data interface accessing different chip selects.

### 3.2.3 Write Data CRC

If the MC generates the CRC, the MC sends the appropriate CRC data word across the DFI bus using the existing **dfi\_wrddata** signals, and adjusts control signal timing to handle the additional data word.

Table 7, “Write Data Timing Parameters,” on page 32 describes the write timing parameters  $t_{\text{phy\_wrcsgap}}$ ,  $t_{\text{phy\_wrcslat}}$ ,  $t_{\text{phy\_wrdata}}$ ,  $t_{\text{phy\_wrlat}}$ ,  $t_{\text{wrdata\_delay}}$ ,  $t_{\text{phy\_crcmax\_lat}}$  and  $t_{\text{phy\_crcmin\_lat}}$ .

The  $t_{\text{phy\_wrcsgap}}$  timing parameter specifies the minimum number of additional DFI PHY clocks required between commands when changing the target chip select driven on the **dfi\_wrdata\_cs\_n** signal, and defines a minimum additional delay between commands when changing the target chip select as required by the PHY. The  $t_{\text{phy\_wrcslat}}$  parameter specifies the number of DFI PHY clocks between when a write command is sent on the DFI control interface and when the associated **dfi\_wrdata\_cs\_n** signal is asserted, and has a delay defined relative to the command to maximize timing flexibility.

The  $t_{\text{phy\_wrdata}}$  parameter specifies the number of DFI PHY clock cycles between when the **dfi\_wrdata\_en** signal is asserted to when the associated write data is driven on the **dfi\_wrdata** bus. The  $t_{\text{phy\_wrlat}}$  parameter specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the **dfi\_wrdata\_en** signal is asserted. The  $t_{\text{wrdata\_delay}}$  parameter specifies the number of DFI clocks between when the **dfi\_wrdata\_en** signal is asserted and when the corresponding write data transfer is completed on the DRAM bus.

The PHY-defined  $t_{\text{phy\_crcmax\_lat}}$  and  $t_{\text{phy\_crcmin\_lat}}$  timing parameters create a window in which erroneous data is transmitted across the DFI. The MC can use these timing parameters to pinpoint the command or set of commands associated with the error condition to efficiently reissue commands after the CRC error is addressed. The CRC error timing parameters define the relationship between **dfi\_wrdata\_en** and **dfi\_alert\_n\_aN**.

Table 8, “Write Data Programmable Parameters,” on page 33 describes the programmable parameters applicable when CRC and DBI features are enabled. When the optional CRC feature is enabled in DFI, the programmable parameter, **phy\_crc\_mode**, is utilized to send CRC data as part of the write data burst. When the optional DBI feature is enabled in DFI, the PHY-defined **phy\_dbi\_mode** parameter determines whether DBI generation and data inversion is performed by the MC or the PHY.

### **3.2.4 Frequency Ratio**

For frequency ratio systems, the signals are replicated into phase-specific signals with a suffix of “\_pN” that defines the signal value for each phase N of the PHY clock. Phase 0 may exclude the suffix if desired.

The signals and parameters in the write data interface are listed in Table 6, “Write Data Signals,” on page 31, Table 7, “Write Data Timing Parameters,” on page 32, and Table 8, “Write Data Programmable Parameters,” on page 33.

For more information on the write data interface, refer to Section 4.4, “Write Transactions,” on page 65. For more information on which signals are required and

which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the write data interface are listed in Table 6, “Write Data Signals”.

**TABLE 6.** Write Data Signals

Signal	From	Width	Default	Description
<b>dfi_wrdata</b> or <b>dfi_wrdata_pN</b> <sup>a</sup>	MC	DFI Data Width	_ b	<u>Write data.</u> These signals transfer write data from the MC to the PHY <b>t<sub>phy_wrdata</sub></b> cycles after the <b>dfi_wrdata_en</b> signal is asserted and continues transferring data for the number of cycles that the <b>dfi_wrdata_en</b> signal is asserted.
<b>dfi_wrdata_cs_n</b> or <b>dfi_wrdata_cs_n_pN</b> <sup>a</sup>	MC	DFI Chip Select Width x DFI Data Enable Width <sup>c</sup>	_ b	<u>DFI Write Data Chip Select.</u> This signal has two functions and is defined similar to the <b>dfi_cs_n</b> signal.  During write leveling, <b>dfi_wrdata_cs_n</b> indicates which chip select is currently active.  During non-leveling operation, <b>dfi_wrdata_cs_n</b> is an optional signal for the MC to indicate which chip select is accessed or targeted for associated write data.
<b>dfi_wrdata_en</b> or <b>dfi_wrdata_en_pN</b> <sup>a</sup>	MC	DFI Data Enable Width <sup>d</sup>	0x0	<u>Write data and data mask enable.</u> This signal indicates to the PHY that valid <b>dfi_wrdata</b> will be transmitted in <b>t<sub>phy_wrdata</sub></b> cycles. Both <b>t<sub>phy_wrlat</sub></b> and <b>t<sub>phy_wrdata</sub></b> may be defined as zero.  Ideally, there is a one-to-one correspondence between <b>dfi_wrdata_en</b> bits and PHY data slices. The <b>dfi_wrdata_en</b> [0] signal corresponds to the lowest segment of <b>dfi_wrdata</b> signals.
<b>dfi_wrdata_mask</b> or <b>dfi_wrdata_mask_pN</b> <sup>a</sup>	MC	DFI Data Width / 8	b	<u>Write data byte mask.</u> This bus is used to transfer either the write data mask or the write DBI information, depending on system/ DRAM settings. Uses the same timing as the <b>dfi_wrdata</b> signal.  <ul style="list-style-type: none"> <li>• <b>dfi_wrdata_mask</b> [0] = Masking or DBI for the <b>dfi_wrdata</b> [7:0] signals</li> <li>• <b>dfi_wrdata_mask</b> [1] = Masking or DBI for the <b>dfi_wrdata</b> [15:8] signals, etc.</li> </ul> If the <b>dfi_wrdata</b> bus is not a multiple of 8, then the uppermost bit of the <b>dfi_wrdata_mask</b> signal corresponds to the most significant partial byte of data.

- For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N (aN), as applicable. The phase 0 suffixes are not required.
- This signal is not meaningful during initialization; no default value is required.
- The width is defined to be replicated and multiply driven to each of the PHY data slices for interconnect simplicity.
- Since all bits of the **dfi\_wrdata\_en** signal are identical, the width of the signal on the MC side and the PHY side may be different; the PHY is not required to use all of the bits.

The timing parameters associated with the write data interface are listed in Table 7, “Write Data Timing Parameters”.

TABLE 7. Write Data Timing Parameters

Parameter	Defined By	Min	Max	Unit	Description
$t_{\text{phy\_crcmax\_lat}}$	System	1	- <sup>a</sup>	DFI PHY clock cycles <sup>b</sup>	Specifies the maximum number of DFI clocks between <b>dfi_wrdata_en</b> and the associated CRC error; transmitted on <b>dfi_alert_n_aN</b> . Can be used with $t_{\text{phy\_crcmin\_lat}}$ to determine a window of time in which the erroneous data was transmitted across the DFI bus.
$t_{\text{phy\_crcmin\_lat}}$	System	0	- <sup>a</sup>	DFI PHY clock cycles <sup>b</sup>	Specifies the minimum number of DFI clocks between <b>dfi_wrdata_en</b> and the associated CRC error; transmitted on <b>dfi_alert_n_aN</b> . Can be used with $t_{\text{phy\_crcmax\_lat}}$ to determine a window of time in which the erroneous data was transmitted across the DFI bus.
$t_{\text{phy\_wrcsgap}}$	PHY	0	- <sup>a</sup>	DFI PHY clock cycles <sup>b</sup>	Specifies the minimum number of additional DFI PHY clocks required between commands when changing the target chip select driven on the <b>dfi_wrdata_cs_n</b> signal. This parameter needs to be supported in the MC transaction-to-transaction timing. The minimum assertion duration of <b>dfi_wrdata_cs_n</b> is determined by $t_{\text{phy\_wrcsgap}} + \text{dfi\_rw\_length}^c$ .
$t_{\text{phy\_wrcslat}}$	PHY	0	- <sup>a</sup>	DFI PHY clock cycles <sup>b</sup>	Specifies the number of DFI PHY clocks between when a write command is sent on the DFI control interface and when the associated <b>dfi_wrdata_cs_n</b> signal is asserted.
$t_{\text{phy\_wrdata}}$	PHY	0 <sup>d</sup>	- <sup>d</sup>	DFI PHY clock cycles <sup>b</sup>	Specifies the number of DFI PHY clock cycles between when the <b>dfi_wrdata_en</b> signal is asserted to when the associated write data is driven on the <b>dfi_wrdata</b> signal. This has no impact on performance, only adjusts the relative time between enable and data transfer. DFI 1.0 and DFI 2.0 MCs only support a $t_{\text{phy\_wrdata}}$ value of 1. The MC should support a range of $t_{\text{phy\_wrdata}}$ values. A PHY is generally designed to operate at a single $t_{\text{phy\_wrdata}}$ value.
$t_{\text{phy\_wrlat}}$	PHY	0 <sup>d</sup>	- <sup>d</sup>	DFI PHY clock cycles <sup>b</sup>	Specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the <b>dfi_wrdata_en</b> signal is asserted. NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.
$t_{\text{wrdata\_delay}}$	System	0	-	DFI clock cycles	Specifies the number of DFI clocks between when the <b>dfi_wrdata_en</b> signal is asserted and when the corresponding write data transfer is completed on the DRAM bus.

- a. The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.
- b. This timing parameter is defined in terms of DFI PHY clock cycles for frequency ratio systems. For matched frequency systems, a DFI PHY clock is identical to the DFI clock.
- c. The **dfi\_rw\_length** value is the total number of DFI clocks required to transfer one DFI read or write command worth of data. For a matched frequency system: **dfi\_rw\_length** would typically be equal to (burst length/2). For a frequency ratio system: **dfi\_rw\_length** would typically be equal to ((burst length/2)/frequency ratio).



- d. The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

The programmable parameters associated with the write data interface are listed in Table 8, “Write Data Programmable Parameters”.

**TABLE 8.** *Write Data Programmable Parameters*

Parameter	Defined By	Description
<b>phy<sub>crc</sub>_mode</b>	PHY	Sends CRC data as part of the data burst. <ul style="list-style-type: none"> <li>• ‘b0 = CRC code generation and validation performed in the MC.</li> <li>• ‘b1 = CRC code generation and validation performed in the PHY.</li> </ul>
<b>phy<sub>dbi</sub>_mode</b>	PHY	Determines which device generates DBI and inverts the data. <ul style="list-style-type: none"> <li>• ‘b0 = DBI generation and data inversion performed in the MC.</li> <li>• ‘b1 = DBI generation and data inversion performed in the PHY.</li> </ul>

### 3.3 Read Data Interface

The read data transaction handles the capture and return of data across the DFI; the interface includes signals, timing parameters, and a programmable parameter.

The width is defined to be replicated and multiply driven to each of the PHY data slices for interconnect simplicity.

Table 9, “Read Data Signals,” on page 35 describes the signals **dfi\_rddata** (read data bus), **dfi\_rddata\_cs\_n** (data path chip select), **dfi\_rddata\_en** (read data enable), **dfi\_rddata\_valid** (read data valid indicator), and the DRAM-specific LPDDR2 signal **dfi\_rddata\_dnv** (dfi data not valid) and the DDR4 signal **dfi\_rddata\_dbi\_n**. When the **dfi\_rddata\_dbi\_n** signal is used, it is sent with the **dfi\_rddata** signal.

#### 3.3.1 Read DBI

If the DBI feature is enabled and **phy<sub>dbi</sub>\_mode**=0, the MC captures read DBI data transmitted from the PHY and selectively inverts the read data for DBI as required.

#### 3.3.2 Read Data Chip Select

In some memory systems with multiple chip selects, it may be desirable to independently compensate for timing differences on the data interface accessing different chip selects. In this case, the PHY may require knowledge of the target chip select for each read transaction. The optional **dfi\_rddata\_cs\_n** signal provides the target data path chip select value to each of the PHY data slices.

The data path chip select signal **dfi\_rddata\_cs\_n** is defined similar to the **dfi\_cs\_n** signal, and has a separate timing parameter, **t<sub>phy\_rdcslat</sub>**, with a delay defined relative to the command to maximize timing flexibility. Additionally, the **t<sub>phy\_rdcsgap</sub>** timing parameter defines a minimum additional delay between commands when changing the target chip select as required by the PHY.

### **3.3.3 Read Data Valid**

The **dfi\_rddata\_valid** signal allows each PHY data slice to return **dfi\_rddata** independently. The **dfi\_rddata\_valid** signal width is equivalent to the number of PHY data slices.

When valid data is being transferred, the **dfi\_rddata\_valid** signal must be asserted. The signal is applicable to each clock cycle of **dfi\_rddata\_en** and the corresponding assertion of **dfi\_rddata\_valid** for the transaction, observing the one-to-one correspondence between the **dfi\_rddata\_en** and **dfi\_rddata\_valid** signals.

DFI dictates a timing relationship using the **t<sub>phy\_rdlat</sub>** parameter from enable to **dfi\_rddata\_valid**; DFI does not dictate an exact number of cycles. The **dfi\_rddata\_valid** signal can assert earlier than the maximum delay, and does not need to be held for consecutive cycles provided the **t<sub>phy\_rdlat</sub>** value is met for every transfer.

Table 10, “Read Data Timing Parameters,” on page 36 describes the timing parameters **t<sub>phy\_rdcsgap</sub>**, **t<sub>phy\_rdcslat</sub>**, **t<sub>rddata\_en</sub>**, and **t<sub>phy\_rdlat</sub>**.

The **t<sub>phy\_rdlat</sub>** parameter defines the maximum number of cycles allowed from the assertion of the **dfi\_rddata\_en** signal to the assertion of the **dfi\_rddata\_valid** signal for all data slices. This parameter is specified by the system, but the exact value of this parameter is not determined by the DFI specification.

The **t<sub>rddata\_en</sub>** and **t<sub>phy\_rdlat</sub>** timing parameters must be held constant while commands are being executed on the DFI bus; however, if necessary, the timing parameters may be changed when the bus is in the idle state. These parameters work together to define a maximum number of cycles from the assertion of a read command on the DFI control interface to the assertion of the **dfi\_rddata\_valid** signal, indicating the first valid data of the contiguous read data. Read data may be returned earlier by asserting the **dfi\_rddata\_valid** signal before **t<sub>phy\_rdlat</sub>** cycles have expired. When the signal **dfi\_rddata\_valid** is asserted, the entire DFI read data word from the associated data slice must be valid. For the LPDDR2 DFI, the signal **dfi\_rddata\_dnv** must also be sent with the read data signal **dfi\_rddata** when the **dfi\_rddata\_valid** signal is asserted.

### **3.3.4 Frequency Ratio**

For frequency ratio systems, the read data enable signal is replicated into phase-specific signals with a suffix of “\_pN” that defines the signal value for each phase N of the DFI PHY clock relative to the DFI clock. The read data, read data valid and read data not valid signals are replaced with DFI data word-specific signals with a suffix of “\_wN”

with the DFI data word N. For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional.

Table 11, “Read Data Programmable Parameter,” on page 37 describes the programmable parameter **phydbi\_mode** which applies to both write and read signals.

For more information on the read data interface, refer to Section 4.5, “Read Transactions,” on page 79. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the read data interface are listed in Table 9, “Read Data Signals”.

**TABLE 9.** *Read Data Signals*

Signal	From	Width	Default	Description
<b>dfi_rddata</b> or <b>dfi_rddata_wN<sup>a</sup></b>	PHY	DFI Data Width	_ <sup>b</sup>	<u>Read data bus.</u> This bus transfers read data from the PHY to the MC. Read data is expected to be received at the MC within <b>t<sub>phy_rdat</sub></b> cycles after the <b>dfi_rddata_en</b> signal is asserted.
<b>dfi_rddata_cs_n</b> or <b>dfi_rddata_cs_n_pN<sup>a</sup></b>	MC	DFI Chip Select Width		<u>DFI Read Data Chip Select.</u> This signal has two functions.  During read <u>training</u> , <b>dfi_rddata_cs_n</b> indicates which chip select is currently active.  During non-leveling operation, <b>dfi_rddata_cs_n</b> is an optional signal for the MC to indicate which chip select is accessed or targeted for associated read data.
<b>dfi_rddata_dbi_n</b> or <b>dfi_rddata_dbi_n_wN<sup>a</sup></b>	PHY	DFI DBI Width		<u>Read Data DBI.</u> This signal is sent with <b>dfi_rddata</b> bus indicating DBI functionality. This signal is used only when <b>phydbi_mode=0</b> .
<b>dfi_rddata_en</b> or <b>dfi_rddata_en_pN<sup>a</sup></b>	MC	DFI Data Enable Width <sup>c</sup>	0x0	<u>Read data enable.</u> This signal indicates to the PHY that a read operation to memory is underway and identifies the number of data words to be read. The <b>dfi_rddata_en</b> signal must be asserted <b>t<sub>rddata_en</sub></b> cycles after the assertion of a read command on the DFI control interface and remains valid for the duration of contiguous read data expected on the <b>dfi_rddata</b> bus.  Ideally, there is a single <b>dfi_rddata_en</b> bit for each PHY data slice. The <b>dfi_rddata_en</b> [0] signal corresponds to the lowest segment of <b>dfi_rddata</b> signals.
<b>dfi_rddata_valid</b> or <b>dfi_rddata_valid_wN<sup>a</sup></b>	PHY	DFI Read Data Valid Width	0x0	<u>Read data valid indicator.</u> Each bit of the <b>dfi_rddata_valid</b> signal is asserted with the corresponding <b>dfi_rddata</b> for the number of cycles that data is being sent. The timing is the same as for the <b>dfi_rddata</b> bus.  The width of the <b>dfi_rddata_valid</b> signal is equivalent to the number of PHY data slices. Ideally, there is a one-to-one correspondence between a <b>dfi_rddata_valid</b> signal bit and each PHY data slice. The <b>dfi_rddata_valid</b> [0] signal corresponds to the lowest segment of the <b>dfi_rddata</b> signals.

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_rddata_dnv</b> or <b>dfi_rddata_dnv_wN</b> <sup>a</sup>	PHY	DFI Data Width / 8	0x0	<u>DFI data not valid</u> . The timing is the same as for the <b>dfi_rddata_valid</b> signal.  The <b>dfi_rddata_dnv</b> [0] signal correlates to the <b>dfi_rddata</b> [7:0] signals, the <b>dfi_rddata_dnv</b> [1] signal correlates to the <b>dfi_rddata</b> [15:8] signals, etc. If the <b>dfi_rddata</b> bus is not a multiple of 8, then the uppermost bit of the <b>dfi_rddata_dnv</b> signal corresponds to the most significant partial byte of data.

- For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N(aN), as applicable. The phase 0 suffixes are not required.
- This signal is not meaningful during initialization; no default value is required.
- Since all bits of the **dfi\_rddata\_en** signal are identical, the width of the signal on the MC side and the PHY side may be different; the PHY is not required to use all of the bits.

The timing parameters associated with the read data interface are listed in Table 10, “Read Data Timing Parameters”.

**TABLE 10.** *Read Data Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
<b>t<sub>phy_rdcsgap</sub></b>	PHY	0	_a	DFI PHY clock cycles <sup>b</sup>	Specifies the minimum number of additional DFI PHY clocks required between commands when changing the target chip select driven on the <b>dfi_rddata_cs_n</b> signal. This parameter needs to be supported in the MC transaction-to-transaction timing. The minimum assertion duration of <b>dfi_rddata_cs_n</b> is determined by <b>t<sub>phy_rdcsgap</sub></b> + <b>dfi<sub>rw</sub>_length</b> <sup>c</sup> .
<b>t<sub>phy_rdcslat</sub></b>	PHY	0	_a	DFI PHY clock cycles <sup>b</sup>	Specifies the number of DFI PHY clocks between when a read command is sent on the DFI control interface and when the associated <b>dfi_rddata_cs_n</b> signal is asserted.
<b>t<sub>phy_rdlat</sub></b>	PHY	0	_a	DFI PHY clock cycles <sup>b</sup>	Specifies the maximum number of DFI PHY clock cycles allowed from the assertion of the <b>dfi_rddata_en</b> signal to the assertion of each of the corresponding bits of the <b>dfi_rddata_valid</b> signal.
<b>t<sub>rddata_en</sub></b>	System	0	_a	DFI PHY clock cycles <sup>b</sup>	Specifies the number of DFI PHY clock cycles from the assertion of a read command on the DFI to the assertion of the <b>dfi_rddata_en</b> signal.  NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.

- The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.
- For matched frequency systems, a DFI PHY clock is identical to the DFI clock. For frequency ratio systems, this timing parameter is defined in terms of DFI PHY clock cycles.

- c. The **dfi<sub>rw</sub>\_length** value is the total number of DFI clocks required to transfer one DFI read or write command worth of data. For a matched frequency system: **dfi<sub>rw</sub>\_length** would typically be equal to (burst length/2). For a frequency ratio system: **dfi<sub>rw</sub>\_length** would typically be equal to ((burst length/2)/frequency ratio).

The programmable parameter associated with the read data interface is listed in Table 11, “Read Data Programmable Parameter”.

**TABLE 11.** *Read Data Programmable Parameter*

Parameter	Defined By	Min	Max	Description
<b>phydbi_mode</b>	PHY	0	1	Determines which device generates DBI and inverts the data. <ul style="list-style-type: none"> <li>• ‘b0 = DBI generation and data inversion performed in the MC.</li> <li>• ‘b1 = DBI generation and data inversion performed in the PHY.</li> </ul>

### 3.4 Update Interface

The update interface handles the transmission of updates to internal settings to compensate for environmental conditions; the interface includes signals and timing parameters. To ensure that updates do not interfere with signals on the DRAM interface, the DFI supports update modes where the DFI bus is placed in an idle state.

When the DFI bus is in an idle state, the control interface is not sending any commands and all read and write data has transferred on the DFI bus, reached its destination (DRAM or MC), and the write data transfer has completed on the DRAM bus; the DRAM bus is unchanged. The DFI specification supports both MC-initiated and PHY-initiated updates. For more information on the update interface, refer to Section 4.6, “PHY Update,” on page 87.

If a MC initiates an update request by asserting the **dfi\_ctrlupd\_req** signal, following initialization, and training if required, the PHY can acknowledge or ignore the request. If the PHY acknowledges the request, by asserting the **dfi\_ctrlupd\_ack** signal, the protocol described in Section 4.6.1, “MC-Initiated Update,” on page 87 must be followed.

The **t<sub>ctrlupd\_interval</sub>** parameter defines the maximum interval at which the MC can assert **dfi\_ctrlupd\_req** signals. Following a self-refresh exit, the **dfi\_ctrlupd\_req** signal must be asserted prior to allowing read/write traffic to begin.

If a PHY initiates an update request by asserting the **dfi\_phyupd\_req** signal, the MC must acknowledge the request by asserting the **dfi\_phyupd\_ack** signal. The DFI specifies up to 4 different update PHY-initiated request modes. Each mode differs only in the number of cycles that the DFI interface must be suspended while the update occurs. During this time, the MC is responsible for placing the system in a state where the DFI bus is suspended from all activity other than activity specifically related to the

update process being executed. For more details, refer to Section 4.6.2, “PHY-Initiated Update,” on page 88.

The DFI specification does not require the PHY to issue update requests nor does the specification specify an interval in which requests must be offered. If the PHY offers update requests, it must follow the specified protocol.

It is possible that both update request signals (**dfi\_ctrlupd\_req** and **dfi\_phyupd\_req**) could be asserted at the same time. When both request signals are driven, the MC and the PHY could violate the protocol by simultaneously acknowledging the other’s request. To prevent this situation, the MC is not permitted to assert both **dfi\_ctrlupd\_req** and **dfi\_phyupd\_ack** at the same time. If **dfi\_ctrlupd\_req** is asserted at the same time as **dfi\_phyupd\_req**, the PHY is permitted to de-assert **dfi\_phyupd\_req**, though it is not required to be de-asserted. This is the only situation in which the PHY is permitted to de-assert the **dfi\_phyupd\_req** signal without an acknowledge from the MC. Since it is the PHY (not the MC) that uses the Update interface to request the DFI bus to be IDLE, the PHY should not de-assert **dfi\_phyupd\_req** unless the signal is no longer required due to the assertion of **dfi\_ctrlupd\_req**. The acknowledged request must follow the appropriate protocol.

The signals and timing parameters in the update interface are listed in Table 12 and Table 13.

For more information on the update interface, refer to Section 4.6, “PHY Update,” on page 87. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the update interface are listed in Table 12, “Update Interface Signals”.

**TABLE 12.** *Update Interface Signals*

Signal	From	Width	Default	Description
<b>dfi_ctrlupd_ack</b>	PHY	1 bit	0x0	<p><u>MC-initiated update acknowledge.</u> The <b>dfi_ctrlupd_ack</b> signal is asserted to acknowledge a MC-initiated update request. The PHY is not required to acknowledge this request.</p> <p>While this signal is asserted, the DFI bus must remain in the idle state except for transactions specifically associated with the update process.</p> <p>If the PHY acknowledges the request, the <b>dfi_ctrlupd_ack</b> signal must be asserted before the <b>dfi_ctrlupd_req</b> signal de-asserts. If the PHY ignores the request, the <b>dfi_ctrlupd_ack</b> signal must remain de-asserted until the <b>dfi_ctrlupd_req</b> signal is de-asserted.</p> <p>The <b>dfi_ctrlupd_req</b> signal is guaranteed to be asserted for at least <b>t<sub>ctrlupd_min</sub></b> cycles.</p>

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_ctrlupd_req</b>	MC	1 bit	0x0	<p><u>MC-initiated update request.</u> The <b>dfi_ctrlupd_req</b> signal is used with a MC-initiated update to indicate that the DFI will be in the idle state for some time, in which case the PHY may perform an update.</p> <p>The <b>dfi_ctrlupd_req</b> signal must be asserted for a minimum of <math>t_{ctrlupd\_min}</math> cycles and a maximum of <math>t_{ctrlupd\_max}</math> cycles.</p> <p>A <b>dfi_ctrlupd_req</b> signal assertion is an invitation for the PHY to update and does not require a response.</p> <p>The behavior of the <b>dfi_ctrlupd_req</b> signal is dependent on the <b>dfi_ctrlupd_ack</b> signal:</p> <ul style="list-style-type: none"> <li>• If the update is acknowledged by the PHY, then the <b>dfi_ctrlupd_req</b> signal remains asserted as long as the <b>dfi_ctrlupd_ack</b> signal is asserted, but <b>dfi_ctrlupd_req</b> de-asserts before <math>t_{ctrlupd\_max}</math> expires. While <b>dfi_ctrlupd_req</b> is asserted, the DFI bus remains in the idle state except for transactions specifically associated with the update process.</li> <li>• If the update is not acknowledged, the <b>dfi_ctrlupd_req</b> signal may de-assert at any time after <math>t_{ctrlupd\_min}</math>, and before <math>t_{ctrlupd\_max}</math>.</li> </ul>
<b>dfi_phyupd_ack</b>	MC	1 bit	0x0	<p><u>PHY-initiated update acknowledge.</u> The <b>dfi_phyupd_ack</b> signal is used for a PHY-initiated update to indicate that the DFI is idle and remains in the idle state until the <b>dfi_phyupd_req</b> signal de-asserts.</p> <p>The MC must assert the <b>dfi_phyupd_ack</b> signal within <math>t_{phyupd\_resp}</math> cycles of the <b>dfi_phyupd_req</b> signal, and must remain asserted as long as the <b>dfi_phyupd_req</b> signal remains asserted. The <b>dfi_phyupd_ack</b> signal must de-assert on the cycle following the detection of <b>dfi_phyupd_req</b> signal de-assertion. The <b>dfi_phyupd_req</b> cannot be asserted prior to the de-assertion of <b>dfi_phyupd_ack</b> for the previous transaction.</p> <p>NOTE: If a <b>dfi_ctrlupd_req</b> occurs at the same time as a <b>dfi_phyupd_req</b>, then the <math>t_{phyupd\_resp}</math> requirement is allowed to not be met since <b>dfi_phyupd_ack</b> and <b>dfi_ctrlupd_req</b> cannot be asserted simultaneously.</p> <p>While <b>dfi_phyupd_ack</b> is asserted, the DFI bus must remain in the idle state except for transactions specifically associated with the update process.</p> <p>The time period from when the <b>dfi_phyupd_ack</b> signal is asserted to when the <b>dfi_phyupd_req</b> signal is de-asserted is a maximum of <math>t_{phyupd\_typeX}</math> cycles, based on the <b>dfi_phyupd_type</b> signal.</p>

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_phyupd_req</b>	PHY	1 bit	0x0	<p><u>PHY-initiated update request.</u> The <b>dfi_phyupd_req</b> signal is used for a PHY-initiated update to indicate that the PHY requires the DFI bus to be placed in an idle state and not send control, read or write commands or data for a specified period of time. The maximum time required is specified by the <b>t<sub>phyupd_typeX</sub></b> parameter associated with the <b>dfi_phyupd_type</b> signal.</p> <p>Once asserted, the <b>dfi_phyupd_req</b> signal must remain asserted until the request is acknowledged by the assertion of the <b>dfi_phyupd_ack</b> signal and the update has been completed. The MC must acknowledge this request.</p> <p>While this signal is asserted, the DFI bus must remain in the idle state other than any transactions specifically associated with the update process.</p> <p>The de-assertion of the <b>dfi_phyupd_req</b> signal triggers the de-assertion of the <b>dfi_phyupd_ack</b> signal.</p>
<b>dfi_phyupd_type</b>	PHY	2 bits	_ a	<p><u>PHY-initiated update select.</u> The <b>dfi_phyupd_type</b> signal indicates which one of the 4 types of PHY update times is being requested by the <b>dfi_phyupd_req</b> signal. The value of the <b>dfi_phyupd_type</b> signal determines which of the timing parameters (<b>t<sub>phyupd_type0</sub></b>, <b>t<sub>phyupd_type1</sub></b>, <b>t<sub>phyupd_type2</sub></b>, <b>t<sub>phyupd_type3</sub></b>) is relevant. The <b>dfi_phyupd_type</b> signal must remain constant during the entire time the <b>dfi_phyupd_req</b> signal is asserted.</p>

a. This signal is not meaningful during initialization; no default value is required.

The timing parameters associated with the update interface are listed in Table 13, “Update Timing Parameters”.

**TABLE 13.** *Update Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
<b>t<sub>ctrlupd_interval</sub></b>	MC	_ a	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the MC may wait between assertions of the <b>dfi_ctrlupd_req</b> signal.
<b>t<sub>ctrlupd_min</sub></b>	MC	1	_ a	DFI clock cycles	Specifies the minimum number of DFI clock cycles that the <b>dfi_ctrlupd_req</b> signal must be asserted.
<b>t<sub>ctrlupd_max</sub></b>	MC	_ a	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the <b>dfi_ctrlupd_req</b> signal can assert.



Parameter	Defined By	Min	Max	Unit	Description
<b>t<sub>phyupd_type0</sub></b>	PHY	1	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the <b>dfi_phyupd_req</b> signal may remain asserted after the assertion of the <b>dfi_phyupd_ack</b> signal for <b>dfi_phyupd_type</b> = 0x0. The <b>dfi_phyupd_req</b> signal may de-assert at any cycle after the assertion of the <b>dfi_phyupd_ack</b> signal.
<b>t<sub>phyupd_type1</sub></b>	PHY	1	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the <b>dfi_phyupd_req</b> signal may remain asserted after the assertion of the <b>dfi_phyupd_ack</b> signal for <b>dfi_phyupd_type</b> = 0x1. The <b>dfi_phyupd_req</b> signal may de-assert at any cycle after the assertion of the <b>dfi_phyupd_ack</b> signal.
<b>t<sub>phyupd_type2</sub></b>	PHY	1	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the <b>dfi_phyupd_req</b> signal may remain asserted after the assertion of the <b>dfi_phyupd_ack</b> signal for <b>dfi_phyupd_type</b> = 0x2. The <b>dfi_phyupd_req</b> signal may de-assert at any cycle after the assertion of the <b>dfi_phyupd_ack</b> signal.
<b>t<sub>phyupd_type3</sub></b>	PHY	1	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the <b>dfi_phyupd_req</b> signal may remain asserted after the assertion of the <b>dfi_phyupd_ack</b> signal for <b>dfi_phyupd_type</b> = 0x3. The <b>dfi_phyupd_req</b> signal may de-assert at any cycle after the assertion of the <b>dfi_phyupd_ack</b> signal.
<b>t<sub>phyupd_resp</sub></b>	PHY	1	_ a	DFI clock cycles	Specifies the maximum number of DFI clock cycles after the assertion of the <b>dfi_phyupd_req</b> signal to the assertion of the <b>dfi_phyupd_ack</b> signal.

- a. The minimum supportable value is 1; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

## 3.5 Status Interface

The status interface signal conveys status information between the MC and the PHY for initialization and clock control to the DRAM devices.

### 3.5.1 Initialization

At initialization, the **dfi\_init\_start** signal indicates to the PHY that the frequency ratio and/or data byte lane use has been defined. The PHY may use this signal to know when these settings are valid from the MC.

During normal operation, once both the **dfi\_init\_complete** and **dfi\_init\_start** signals have been asserted, the **dfi\_init\_start** signal is used to trigger frequency change. At initialization, the **dfi\_init\_complete** signal indicates that the PHY is ready to accept DFI transactions. During frequency change, the **dfi\_init\_complete** signal indicates an acceptance of the frequency change request. The optional **dfi\_data\_byte\_disable** signal is used to inform the PHY which data slices will be unused. The value of the **dfi\_data\_byte\_disable** signal must be defined at initialization and is not expected to change.

The byte lanes correspond to the byte order defined for the **dfi\_wrdata** and **dfi\_rddata** signals. The MC and the PHY must both support the same partial use of data signals in order to use byte disabling. For example, if the MC disables the upper bits (most significant bits) of the data bus, the PHY must be able to operate accurately with the remaining byte lanes. The DFI specification does not define supported active/inactive patterns, and therefore care must be taken to insure the interoperability of the MC and the PHY.

For more information on initialization, refer to Section 4.1, “Initialization,” on page 60.

### **3.5.2 Clock Disabling**

The **dfi\_dram\_clk\_disable** signal is used by the MC to inform the PHY when to enable/disable the clock to the DRAMs. The timing parameters **t<sub>dram\_clk\_disable</sub>** and **t<sub>dram\_clk\_enable</sub>** define the timing of the DRAM clock enable/disable relative to the **dfi\_dram\_clk\_disable** signal.

For more information on the DFI clock interface, refer to Section 4.7, “DFI Clock Disabling,” on page 90.

### **3.5.3 Frequency Ratio**

The optional **dfi\_freq\_ratio** signal is used to convey frequency ratio information to the PHY. This static signal indicates the ratio expected by the MC, and dictates how control, read and write information is passed across the DFI.

For more information on the frequency ratio protocol, refer to Section 4.8, “Frequency Ratios Across the DFI,” on page 91.

### **3.5.4 Frequency Change**

The DFI specification defines a frequency change protocol between the MC and the PHY to allow the devices to change the clock frequency of the MC and the PHY without completely resetting the system.

The signals used in the frequency change protocol are **dfi\_init\_start** asserted in normal operation, and **dfi\_init\_complete**; the behavior of the **dfi\_init\_start** signal is dependent on the **dfi\_init\_complete** signal. The associated timing parameters are **t<sub>init\_start</sub>** and **t<sub>init\_complete</sub>**.

For more information on the frequency change protocol, refer to Section 4.9, “Frequency Change,” on page 109.

### **3.5.5 CRC and CA Parity**

The optional CRC and CA parity support signals are provided specifically for DDR4 and DDR3 DRAMs. The DDR4 and DDR3 systems include additional I/O pins with information that should be communicated between the DRAMs and the MC. The MC

communicates its command parity setting on the **dfi\_parity\_in** signal and the PHY reports command parity errors on the **dfi\_alert\_n\_aN** signal.

For more information on CRC and CA parity support signals, refer to Section 3.6, “DFI Training Interface,” on page 47 and Section 3.6, “DFI Training Interface,” on page 47.

The **dfi\_init\_start** signal and the **dfi\_init\_complete** signal are used at initialization and as part of the frequency change protocol.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the status interface are listed in Table 14, “Status Interface Signals”.

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**TABLE 14.** *Status Interface Signals*

Signal	From	Width	Default	Description
<b>dfi_alert_n_aN</b> <sup>a</sup>	PHY	DFI Alert Width	1	<u>CRC or parity error indicator.</u> This optional signal is driven when a CRC or parity error is detected in the memory system. The PHY is not required to distinguish between a CRC and CA parity error. The PHY holds the current state until the PHY error input transitions to a new value; the pulse width of the <b>dfi_alert_n_aN</b> signal matches the pulse width of the DRAM subsystem error signal, plus or minus synchronization cycles.  The <b>dfi_alert_n_aN</b> signal is received at the MC within $t_{phy\_paritylat}$ cycles after the command associated with a <b>dfi_parity_in</b> signal is driven.
<b>dfi_data_byte_disable</b>	MC	DFI Data Width / 8	_b	<u>Data byte disable.</u> When set, this signal indicates that the associated data byte is not being used. In this state, the PHY is permitted to place the associated bytes in a low power state. When the bit is clear, the byte operates normally. The byte lanes correspond to the byte order defined for the <b>dfi_wrdata</b> and <b>dfi_rddata</b> signals.  This signal may only be defined during initialization, and then is expected to remain constant. Once defined, the MC drives the <b>dfi_init_start</b> signal to the PHY.
<b>dfi_dram_clk_disable</b>	MC	DFI Chip Select Width	0x0 <sup>c</sup>	<u>DRAM clock disable.</u> When active, this indicates to the PHY that the clocks to the DRAM devices must be disabled such that the clock signals hold a constant value. When the <b>dfi_dram_clk_disable</b> signal is inactive, the DRAMs should be clocked normally.

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## Interface Signal Groups

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Signal	From	Width	Default	Description
<b>dfi_freq_ratio</b>	MC	2 bits	_ b	<p><u>DFI frequency ratio indicator.</u> This signal defines the frequency ratio for this system.</p> <p>This signal is required for MCs and PHYs that support multiple frequency ratios and the DFI frequency ratio protocol.</p> <p>This signal is optional for MCs and PHYs that support only a single frequency ratio or do not support the DFI frequency ratio protocol.</p> <p>This signal may only be defined during initialization, and is expected to remain constant. Once defined, the MC drives the <b>dfi_init_start</b> signal to the PHY.</p> <ul style="list-style-type: none"><li>• ‘b00 = 1:1 MC:PHY frequency ratio (matched frequency)</li><li>• ‘b01 = 1:2 MC:PHY frequency ratio</li><li>• ‘b10 = 1:4 MC:PHY frequency ratio</li><li>• ‘b11 = Reserved</li></ul>
<b>dfi_init_complete</b>	PHY	1 bit	0x0	<p><u>PHY initialization complete.</u> The <b>dfi_init_complete</b> signal indicates that the PHY is able to respond to any proper stimulus on the DFI. All DFI signals that communicate commands or status must be held at their default values until the <b>dfi_init_complete</b> signal asserts. During a PHY re-initialization request (such as a frequency change), this signal is de-asserted.</p> <p>For a frequency change request, the de-assertion of the <b>dfi_init_complete</b> signal acknowledges the frequency change protocol. Once de-asserted, the signal should only be re-asserted within <b>t<sub>init_complete</sub></b> cycles after the <b>dfi_init_start</b> signal has de-asserted, and once the PHY has completed re-initialization.</p>

Signal	From	Width	Default	Description
<b>dfi_init_start</b>	MC	1 bit	0x0 <sup>d</sup> 0x1	<p><u>DFI setup stabilization or frequency change initiation.</u> This optional signal can perform two functions.</p> <p>When <b>dfi_init_start</b> is asserted during initialization, the MC is indicating that it is ready to drive the DFI signals and that the <b>dfi_data_byte_disable</b> and/or <b>dfi_freq_ratio</b> signals (if present) have been defined.</p> <p>When <b>dfi_init_start</b> is asserted during normal operation, the MC is requesting a frequency change.</p> <p>Once asserted, the <b>dfi_init_start</b> signal may be held or released.</p> <p>The behavior of the <b>dfi_init_start</b> signal is dependent on the <b>dfi_init_complete</b> signal:</p> <ul style="list-style-type: none"> <li>• If the PHY accepts the frequency change request, it must de-assert the <b>dfi_init_complete</b> signal within <b>t<sub>init_start</sub></b> cycles of the <b>dfi_init_start</b> assertion. The MC continues to hold the <b>dfi_init_start</b> signal asserted until the clock frequency change has been completed. The de-assertion should be used by the PHY to re-initialize on the new clock frequency.</li> <li>• If the frequency change is not acknowledged (the <b>dfi_init_complete</b> signal remains asserted), the <b>dfi_init_start</b> signal must de-assert after <b>t<sub>init_start</sub></b> cycles.</li> </ul> <p>Initialization is complete when both the <b>dfi_init_start</b> and the <b>dfi_init_complete</b> signals are asserted simultaneously for at least 1 DFI clock.</p>
<b>dfi_parity_in</b> or <b>dfi_parity_in_pN<sup>a</sup></b>	MC	1 bit	0x0 <sup>e</sup> 0x1 <sup>e</sup>	<p><u>Parity value.</u> This optional signal has a one-to-one correspondence with each DFI command and is valid for 1 cycle. This value applies to the <b>dfi_address</b>, <b>dfi_bank</b>, <b>dfi_bg</b>, <b>dfi_act_n</b>, <b>dfi_cas_n</b>, <b>dfi_ras_n</b> and <b>dfi_we_n</b> signals. This signal is only relevant for PHYs that support command parity and require the MC to generate the parity information.</p> <ul style="list-style-type: none"> <li>• ‘b0 = An even number of the parity value signals are electrically high.</li> <li>• ‘b1 = An odd number of the parity value signals are electrically high.</li> </ul>

- For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N (aN), as applicable. The phase 0 suffixes are not required.
- At initialization, this signal must be driven with the valid settings for the system to convey information to the PHY. Refer to Section 14, “Status Interface Signals,” on page 43.
- This signal may be programmed while **dfi\_init\_complete** is not asserted; it should be programmed according to which clocks are being used.
- The PHY may optionally wait for the **dfi\_init\_start** signal assertion before asserting the **dfi\_init\_complete** signal.
- The value of this signal must reflect the correct parity for the selected control interface signals.

The timing parameters associated with the status interface are listed in Table 15, “Status Timing Parameters”.

**TABLE 15.** *Status Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$t_{\text{dram\_clk\_disable}}^a$	PHY	0	_ <sup>b</sup>	DFI clock cycles <sup>c</sup>	Specifies the number of DFI clock cycles from the assertion of the <b>dfi_dram_clk_disable</b> signal on the DFI until the clock to the DRAMs at the PHY-DRAM boundary maintains a low value. NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.
$t_{\text{dram\_clk\_enable}}^a$	PHY	0	_ <sup>b</sup>	DFI clock cycles <sup>c</sup>	Specifies the number of DFI clock cycles from the de-assertion of the <b>dfi_dram_clk_disable</b> signal on the DFI until the first valid rising edge of the clock to the DRAMs at the PHY-DRAM boundary. NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.
$t_{\text{init\_complete}}$	PHY	0	_ <sup>b</sup>	DFI clock cycles <sup>c</sup>	Specifies the maximum number of DFI clock cycles after the de-assertion of the <b>dfi_init_start</b> signal to the re-assertion of the <b>dfi_init_complete</b> signal.
$t_{\text{init\_start}}$	MC	0	_ <sup>b</sup>	DFI clock cycles <sup>c</sup>	Specifies the number of DFI clock cycles from the assertion of the <b>dfi_init_start</b> signal on the DFI until the PHY must respond by de-asserting the <b>dfi_init_complete</b> signal. If the <b>dfi_init_complete</b> signal is not de-asserted within this time period, the PHY is indicating that it can not support the frequency change at this time. In this case, the MC must abort the request and release the <b>dfi_init_start</b> signal. Once $t_{\text{init\_start}}$ expires, the PHY must not de-assert the <b>dfi_init_complete</b> signal. The MC may re-assert <b>dfi_init_start</b> at a later point.
$t_{\text{parin\_lat}}$	MC	0	_ <sup>b</sup>	DFI PHY clock cycles <sup>c</sup>	Specifies the number of DFI clocks between when the <b>dfi</b> command is asserted and when the associated <b>dfi_parity_in</b> signal is driven.
$t_{\text{phy\_paritylat}}$	PHY	4	_ <sup>b</sup>	DFI clock cycles <sup>c</sup>	Specifies the maximum number of DFI clock cycles between when the <b>dfi_parity_in</b> signal is driven and when the associated <b>dfi_alert_n_aN</b> signal is returned.

- a. If the DFI clock and the DRAM clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.
- b. The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.
- c. For matched frequency systems, a DFI PHY clock is identical to the DFI clock. For frequency ratio systems, this timing parameter is defined in terms of DFI PHY clock cycles.

### 3.6 DFI Training Interface

The DFI training interface enables increased accuracy at higher speeds in the alignment of critical timing signals on DDR4, DDR3 and LPDDR2 DRAMs; the interface includes signals, timing parameters, and programmable parameters.

The DRAM type and system configuration determine the types of training available to a system; a system may or may not utilize each type of training. If training is supported, the system may utilize DFI training or support a different training method. There are three training operations; the first two operations (gate training, and read data eye training) are collectively referred to as “read training”.

1. Gate training, used by DDR4, DDR3 and LPDDR2 DRAMs.
2. Read data eye training, used by DDR4, DDR3 and LPDDR2 DRAMs.
3. Write leveling, used by DDR4 and DDR3 DRAMs.

To be DFI-compliant, the MC is required to support all applicable training operations whereas the PHY optionally supports each training operation.

Support for each training operation is enabled or disabled through the corresponding programmable parameter and the enable may be implemented as programmable registers within the device.

The read training and write leveling signals that communicate from the MC to the PHY are multiply driven inside the MC to allow a direct connection from the MC to each PHY data slice and the signals must be driven with the same value.

The read training, write leveling, training signals that communicate from the PHY to the MC may be individually driven by each PHY data slice or collectively driven as a single signal.

More information on the training interface is provided in Section 4.10.1, “CA Parity Timing,” on page 112. The signals, timing parameters, and programmable parameters for the training interface are listed in Table 16, “Training Interface Signals,” on page 49, Table 17, “Training Interface Timing Parameters,” on page 53, and Table 18, “DFI Training Programmable Parameters,” on page 54.

The MC and the PHY can be synchronized with the defined training sequences, and the sequence required for each training operation, with **dfi\_lvl\_pattern** encoding. For information on **dfi\_lvl\_pattern** encoding, refer to Section 3.6.3, “dfi\_lvl\_pattern Encoding,” on page 54.

Long or short training sequences can be defined with the **dfi\_lvl\_periodic** signal. For information on the **dfi\_lvl\_periodic** signal, refer to Section 3.6.4, “Periodic Training Flag,” on page 55.

### **3.6.1 Read Training Operation**

In DFI read training mode, the MC sets up the DRAM for gate training or read data eye training and periodically issues read commands. The PHY evaluates the data returned from the commands and adjusts the gate training and read data eye training capture timing accordingly.

Multiple training sequences can be defined, with either the MC or the PHY supplying the sequence information. In DFI training mode, the PHY is responsible for adjusting the delays and evaluating the responses from the DRAM. Therefore, it is the PHY, not the MC, which determines the sequences necessary to accomplish training. The MC must provide flexibility to run sequences required by the PHY and should not dictate a set of sequences.

A read training sequence can be initiated from the MC or the PHY. In both cases, the MC asserts the **dfi\_rdlvl\_en** signal to initiate or accept the training sequence, and the MC holds the enable signal asserted until the current training operation completes. During read training, **dfi\_rddata\_cs\_n** indicates the chip select that is currently being trained.

In DDR4 systems, the MC drives the **dfi\_lvl\_pattern** signal to define the required training sequence. The **dfi\_lvl\_pattern** signal must be valid when either **dfi\_rdlvl\_gate\_en** (for read gate training) or **dfi\_rdlvl\_en** (for read data eye training) is asserted. Similar to **dfi\_rdlvl\_en**, the **dfi\_lvl\_pattern** signal may transition after training completes.

For more information on **dfi\_rddata\_cs\_n**, refer to Section 3.3, “Read Data Interface,” on page 33 and Table 9, “Read Data Signals,” on page 35.

For more information on read training, refer to Section 4.11, “DFI Training Operations,” on page 114.

### **3.6.2 Write Leveling Operation**

The goal of write leveling is to locate the delay at which the write DQS rising edge aligns with the rising edge of the DRAM clock. By identifying this delay, the system can accurately align the write DQS within the DRAM clock.

A write leveling sequence can be initiated from the MC or the PHY. In both cases, the MC asserts the **dfi\_wrlvl\_en** signal to initiate or accept the leveling sequence, and the MC holds the enable signal asserted until the current training operation completes. During write leveling, **dfi\_wrdata\_cs\_n** indicates the chip select that is currently being trained.

The signals used in write leveling are: **dfi\_wrlvl\_en**, **dfi\_wrlvl\_req**, and **dfi\_wrlvl\_strobe**. The programmable parameter is **phy\_wrlvl\_en**. The write leveling chip select signal is **dfi\_phy\_wrlvl\_cs\_n**.



For more information on **dfi\_phy\_wrlvl\_cs\_n**, refer to Section 3.2, “Write Data Interface,” on page 29 and Table 6, “Write Data Signals,” on page 31.

For more information on write leveling signals, refer to Section 58, “Read Training in DFI Training Mode for LPDDR2 Memory Systems,” on page 119.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the training interface are listed in Table 16, “Training Interface Signals”.

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**TABLE 16.** *Training Interface Signals*

Signal	From	Width	Default	Description
<b>dfi_calvl_capture</b>	MC	DFI CA Training MC I/F Width		<u>CA training capture</u> . This signal is asserted for one DFI clock pulse; initiates the capture of the CA bus value from the DQ bus within the PHY. The capture pulse is asserted <b>t<sub>calvl_capture</sub></b> cycles after the calibration command is driven on <b>dfi_cs_n</b> .
<b>dfi_phy_calvl_cs_n</b>	PHY	DFI Chip Select Width		<u>CA training chip select</u> . Indicates the target chip select associated with the current <b>dfi_calvl_req</b> . This signal is only valid when <b>dfi_calvl_req</b> is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.
<b>dfi_calvl_en</b>	MC	DFI CA Training MC I/F Width		<u>PHY CA training logic enable</u> . This signal is asserted during CA training and can be used by the PHY to enable the associated logic to execute training. If the PHY initiated the CA training request ( <b>dfi_calvl_req</b> ), then this serves as acknowledgement of the request. <ul style="list-style-type: none"> <li>• 'b0 = Normal operation</li> <li>• 'b1 = CA training enabled. The assertion of this signal immediately initiates the CA training process.</li> </ul>
<b>dfi_calvl_req</b>	PHY	DFI CA Training PHY I/F Width		<u>PHY-initiated CA training request</u> . This is an optional signal for the PHY; other sources may be used to initiate CA training or the MC may initiate CA training independently.  If the PHY asserts the <b>dfi_calvl_req</b> signal, the MC must acknowledge this request by asserting the <b>dfi_calvl_en</b> signal within <b>t<sub>calvl_resp</sub></b> cycles, after which the PHY should de-assert the <b>dfi_calvl_req</b> signal.  The PHY is not required to assert this signal during initialization or a frequency change operation. However, if the PHY does assert the request during a frequency change, the <b>dfi_calvl_req</b> signal must be asserted before or coincident with the assertion of the <b>dfi_init_complete</b> signal.

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_calvl_resp</b>	PHY	DFI CA Training Response Width		<p><u>CA training response</u>. This signal indicates that the PHY has completed the current CA training routine. The training sequence may consist of one or more training routines to each of the two CA segments. The response is defined as follows:</p> <ul style="list-style-type: none"> <li>• 'b00 = Not done</li> <li>• 'b01 = Done with pattern, do not change CA segment</li> <li>• 'b10 = Done with pattern, change CA segment</li> <li>• 'b11 = Complete</li> </ul> <p>The <b>dfi_calvl_resp</b> signal is asserted during both phase 1 CA training (enabled with MR41) and phase 2 CA training (enabled with MR48).</p> <p>The width of the <b>dfi_calvl_resp</b> signal is generally defined as two bits.</p>
<b>dfi_lvl_pattern</b>	MC	4-bits x DFI Read Training PHY I/F Width	0	<p><u>Training pattern</u>. Used to determine which training pattern should be run with the current read training operation. This is used with both gate training and read data eye training.</p>
<b>dfi_lvl_periodic</b>	MC	DFI Leveling PHY I/F Width	0	<p><u>Training length indicator (full or periodic)</u>. Global signal used for all training interfaces, which dictates the type of training required.</p> <ul style="list-style-type: none"> <li>• 'b0 = Full training required; long sequence used during initialization and for larger variations.</li> <li>• 'b1 = Periodic training required; shorter sequence used for small variations.</li> </ul>
<b>dfi_phylvl_ack_cs_n</b>	MC	DFI Chip Select Width		<p><u>DFI PHY training chip select acknowledge</u>. MC acknowledgement of PHY request to train a chip select; granted only when the DRAM bus is idle and available for the PHY to use for training.</p>
<b>dfi_phylvl_req_cs_n</b>	PHY	DFI Rank Width		<p><u>DFI PHY training chip select request</u>. This signal enables the PHY to request to train each chip select individually.</p>
<b>dfi_phy_rdlvl_cs_n</b>	PHY	DFI Chip Select Width x DFI Read Training PHY I/F Width	0x1	<p><u>Read training chip select for read data eye training</u>. Indicates the target chip select associated with the current <b>dfi_rdlvl_req</b>. This signal is only valid when <b>dfi_rdlvl_req</b> is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.</p>
<b>dfi_phy_rdlvl_gate_cs_n</b>	PHY	DFI Chip Select Width x DFI Read Training PHY I/F Width	0x1	<p><u>Read training chip select for gate training</u>. Indicates the target chip select associated with the current <b>dfi_rdlvl_gate_req</b>. This signal is only valid when <b>dfi_rdlvl_gate_req</b> is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.</p>

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_phy_wrlvl_cs_n</b>	PHY	DFI Chip Select Width x DFI Write Leveling PHY I/F Width	0x1	<u>Write leveling chip select.</u> Indicates the target chip select associated with the current <b>dfi_wrlvl_req</b> . This signal is only valid when <b>dfi_wrlvl_req</b> is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.
<b>dfi_rdlvl_en</b>	MC	DFI Read Leveling MC I/F Width	0x0	<p><u>PHY read data eye training logic enable.</u> This signal is asserted during read data eye training. If the PHY initiated the read data eye training request (<b>dfi_rdlvl_req</b>), then this serves as an acknowledge of that request.</p> <ul style="list-style-type: none"> <li>• ‘b0 = Normal operation</li> <li>• ‘b1 = Read Data eye training logic enabled. The assertion of this signal immediately initiates read data eye training.</li> </ul> <p>This signal may enable specific training logic within the PHY. If the <b>dfi_rdlvl_en</b> signal is asserted, the MC and the PHY must reset their DFI read data word pointers to 0 on de-assertion of this signal. For more information, refer to Section 4.8.4, “Read Data Interface in Frequency Ratio Systems”.</p>
<b>dfi_rdlvl_gate_en</b>	MC	DFI Read Leveling MC I/F Width	0x0	<p><u>PHY gate training logic enable.</u> This signal is asserted during gate training. If the PHY initiated the gate training request (<b>dfi_rdlvl_gate_req</b>), then this serves as an acknowledge of that request.</p> <ul style="list-style-type: none"> <li>• ‘b0 = Normal operation</li> <li>• ‘b1 = Gate training logic enabled. The assertion of this signal immediately triggers gate training.</li> </ul> <p>If the <b>dfi_rdlvl_gate_en</b> signal is asserted, the MC and the PHY must reset their DFI read data word pointers to 0 on de-assertion of this signal. For more information, refer to Section 4.8.4, “Read Data Interface in Frequency Ratio Systems”.</p>
<b>dfi_rdlvl_gate_req<sup>a</sup></b>	PHY	DFI Read Leveling PHY I/F Width	0x0	<p><u>PHY-initiated gate training request.</u> The PHY initiates gate training, other sources may be used to initiate gate training, or the MC may initiate gate training independently.</p> <p>The PHY may drive independent gate training requests from each data slice; however the MC must gate train all data slices based on a single assertion of the <b>dfi_rdlvl_gate_req</b> signal.</p> <p>If the PHY asserts the <b>dfi_rdlvl_gate_req</b> signal, the MC must acknowledge the request by asserting the <b>dfi_rdlvl_gate_en</b> signal within <b>t<sub>rdlrvl_resp</sub></b> cycles, after which the PHY should de-assert the <b>dfi_rdlvl_gate_req</b> signal.</p> <p>The PHY should not assert <b>dfi_rdlvl_gate_req</b> during initialization and frequency change operations because the MC is responsible for gate training during these operations.</p>

## Interface Signal Groups

Signal	From	Width	Default	Description
<b>dfi_rdlvl_req<sup>a</sup></b>	PHY	DFI Read Leveling PHY I/F Width	0x0	<p><u>PHY-initiated read data eye training request.</u> The PHY initiates read data eye training, other sources may be used to initiate read data eye training, or the MC may initiate read data eye training independently.</p> <p>The PHY may drive independent read data eye training requests from each data slice; however the MC must read level all data slices based on a single assertion of the <b>dfi_rdlvl_req</b> signal.</p> <p>If the PHY asserts the <b>dfi_rdlvl_req</b> signal, the MC must acknowledge the request by asserting the <b>dfi_rdlvl_en</b> signal within <b>t<sub>rdlvl_resp</sub></b> cycles, after which the PHY should de-assert the <b>dfi_rdlvl_req</b> signal.</p>
<b>dfi_rdlvl_resp</b>	PHY	DFI Read Leveling Response Width		<p><u>Read training response.</u></p> <p>Indicates that the PHY has completed read data eye training or gate training.</p> <p>The width of the <b>dfi_rdlvl_resp</b> signal is generally defined as a bit-per-PHY data slice.</p>
<b>dfi_wrlvl_en</b>	MC	DFI Write Leveling MC I/F Width	0x0	<p><u>PHY write leveling logic enable.</u> This signal is asserted during write leveling. If the PHY initiated the write leveling request (<b>dfi_wrlvl_req</b>), then this serves as an acknowledge of that request.</p> <ul style="list-style-type: none"> <li>• ‘b0 = Normal operation</li> <li>• ‘b1 = Write leveling enabled. The assertion of this signal initiates write leveling.</li> </ul>
<b>dfi_wrlvl_req<sup>a</sup></b>	PHY	DFI Write Leveling PHY I/F Width	0x0	<p><u>PHY write leveling request.</u> This is an optional signal for the PHY; other sources may be used to initiate write leveling, or the MC may initiate write leveling independently.</p> <p>The PHY may drive independent write leveling requests from each data slice; however the MC must write level all data slices based on a single assertion of the <b>dfi_wrlvl_req</b> signal.</p> <p>If the PHY asserts the <b>dfi_wrlvl_req</b> signal, the MC must acknowledge the request by asserting the <b>dfi_wrlvl_en</b> signal within <b>t<sub>wrlvl_resp</sub></b> cycles, after which the PHY should de-assert the <b>dfi_wrlvl_req</b> signal.</p>
<b>dfi_wrlvl_resp</b>	PHY	DFI Write Leveling Response Width		<p><u>Write leveling response.</u> Indicates that the PHY has completed write leveling.</p> <p>The width is generally defined as a bit-per-PHY data slice.</p>
<b>dfi_wrlvl_strobe</b>	MC	DFI Write Leveling MC I/F Width	0x0	<p><u>Write leveling strobe.</u> Asserts for one DFI clock pulse; initiates the capture of the write level response from the DQ bus within the PHY.</p>

## Interface Signal Groups

- a. The PHY should not assert this signal during initialization, and it is not required to assert the signal during a frequency change operation. The MC is responsible for read data eye training during initialization and frequency change operations. If the PHY does assert this signal, the PHY must assert it prior to asserting **dfi\_init\_complete**.

Timing parameters relevant for certain read training and write leveling operations are identified in Table 17, “Training Interface Timing Parameters,” on page 53. All timing parameters are defined only once for the interface and must apply to all PHY data slices.

**TABLE 17.** *Training Interface Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$t_{\text{calvl\_capture}}$	PHY	1	-a	DFI clock cycles	<u>CA training capture delay from command</u> . Specifies the number of DFI clock cycles after the controller transmits the calibration command on <b>dfi_cs_n</b> before the <b>dfi_ca_capture</b> pulse is driven.
$t_{\text{calvl\_en}}$	PHY	1	_a	DFI clock cycles	<u>CA training enable time</u> . Specifies the minimum number of DFI clock cycles from the assertion of the <b>dfi_calvl_en</b> signal to the de-assertion of the <b>dfi_cke</b> signal.
$t_{\text{calvl\_max}}$	MC	1	_a	DFI clock cycles	<u>CA training maximum time</u> . Specifies the maximum number of DFI clock cycles that the MC will wait for a response ( <b>dfi_calvl_resp</b> ) to a CA training enable signal ( <b>dfi_calvl_en</b> ).
$t_{\text{calvl\_resp}}$	MC	1	_a	DFI clock cycles	<u>CA training response</u> . Specifies the maximum number of DFI clock cycles after a CA training request is asserted ( <b>dfi_calvl_req</b> ) to when the MC will respond with a CA training enable signal ( <b>dfi_calvl_en</b> ).
$t_{\text{calvl\_cc}}$	PHY	1	_a	DFI clock cycles	<u>CA training chip select to chip select delay</u> . Specifies the minimum number of DFI clock cycles from one calibration command to the next calibration command.
$t_{\text{rdlvl\_en}}$	PHY	1	_a	DFI clock cycles	<u>Read training enable time</u> . Specifies the minimum number of DFI clock cycles from the assertion of the <b>dfi_rdlvl_en</b> or <b>dfi_rdlvl_gate_en</b> signal to the first read (DDR4 or DDR3) or mode register read (LPDDR2) command.
$t_{\text{rdlvl\_max}}$	MC	1	_a	DFI clock cycles	<u>Read training maximum time</u> . Specifies the maximum number of DFI clock cycles that the MC waits for a response ( <b>dfi_rdlvl_resp</b> ) to a read training enable signal ( <b>dfi_rdlvl_en</b> or <b>dfi_rdlvl_gate_en</b> ).
$t_{\text{rdlvl\_resp}}$	MC	1	_a	DFI clock cycles	<u>Read training response</u> . Specifies the maximum number of DFI clock cycles after a read training request is asserted ( <b>dfi_rdlvl_req</b> or <b>dfi_rdlvl_gate_req</b> ) to when the MC responds with a read training enable signal ( <b>dfi_rdlvl_en</b> or <b>dfi_rdlvl_gate_en</b> ).
$t_{\text{rdlvl\_rr}}$	PHY	1	_a	DFI clock cycles	<u>Read training command-to-command delay</u> . Specifies the minimum number of DFI clock cycles after the assertion of a read command to the next read command.  For DDR4 and DDR3 DRAMs, references a read data command.  For LPDDR2 DRAMs, references a mode register read command.

## Interface Signal Groups

Parameter	Defined By	Min	Max	Unit	Description
$t_{wrlvl\_en}$	PHY	1	_ a	DFI clock cycles	<u>Write leveling enable time.</u> Specifies the minimum number of DFI clock cycles from the assertion of the <b>dfi_wrlvl_en</b> signal to the first assertion of the <b>dfi_wrlvl_strobe</b> signal.
$t_{wrlvl\_max}$	MC	1	_ a	DFI clock cycles	<u>Write leveling maximum time.</u> Specifies the maximum number of DFI clock cycles that the MC waits for a response ( <b>dfi_wrlvl_resp</b> ) to a write leveling enable signal ( <b>dfi_wrlvl_en</b> ).
$t_{wrlvl\_resp}$	MC	1	_ a	DFI clock cycles	<u>Write leveling response.</u> Specifies the maximum number of DFI clock cycles after a write leveling request is asserted ( <b>dfi_wrlvl_req</b> ) to when the MC responds with a write leveling enable signal ( <b>dfi_wrlvl_en</b> ).
$t_{wrlvl\_ww}$	PHY	1	_ a	DFI clock cycles	<u>Write leveling write-to-write delay.</u> Specifies the minimum number of DFI clock cycles after the assertion of the <b>dfi_wrlvl_strobe</b> signal to the next assertion of the <b>dfi_wrlvl_strobe</b> signal.

- a. The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

The programmable parameters for read training and write leveling are limited to the parameters defined in Table 18, “DFI Training Programmable Parameters”. The DFI programmable parameters may be implemented as programmable registers within the devices and must be defined by each device.

**TABLE 18.** *DFI Training Programmable Parameters*

Parameter	Defined by	Description
<b>phy_rdlvl_en</b>	PHY	Specifies whether the PHY is supporting read data eye training on the DFI bus <ul style="list-style-type: none"> <li>• ‘b0 = Disabled</li> <li>• ‘b1 = Enabled</li> </ul>
<b>phy_rdlvl_gate_en</b>	PHY	Specifies whether the PHY is supporting gate training on the DFI bus. <ul style="list-style-type: none"> <li>• ‘b0 = Disabled</li> <li>• ‘b1 = Enabled</li> </ul>
<b>phy_wrlvl_en</b>	PHY	Specifies whether the PHY is supporting write leveling on the DFI bus. <ul style="list-style-type: none"> <li>• ‘b0 = Disabled</li> <li>• ‘b1 = Enabled</li> </ul>

### 3.6.3 *dfi\_lvl\_pattern Encoding*

To synchronize the MC and the PHY with the defined training sequences, and the specific sequence required for each training operation, the MC transmits the **dfi\_lvl\_pattern** signal across the DFI bus to the PHY.

The **dfi\_lvl\_pattern** signal must be valid when the enable signal is asserted for gate training or read data eye training. Similar to the enable signal, the **dfi\_lvl\_pattern** signal may transition when training completes.

For more information on **dfi\_lvl\_pattern** signal encoding, refer to Table 25, “DDR4 Encoding of dfi\_lvl\_pattern,” on page 122.

### **3.6.4 Periodic Training Flag**

The **dfi\_lvl\_periodic** control signal is a general purpose training signal that is relevant when the PHY can execute a long or short training sequence as needed.

The **dfi\_lvl\_periodic** signal defines the type of training required and determines if a full training sequence is required. The MC sets a single bit on the **dfi\_lvl\_periodic** signal to indicate to the PHY whether the system may require a longer training sequence (when initializing or re-starting from the self refresh state), or whether the system only needs a short training (when in an operating state and simply tuning the delays).

The **dfi\_lvl\_periodic** signal is utilized with all training interfaces and all DRAM types that utilize training. The encoding of the **dfi\_lvl\_periodic** signal is defined in Table 16, “Training Interface Signals,” on page 49.

The timing parameters associated with the training interface are listed in Table 17, “Training Interface Timing Parameters,” on page 53.

For more information on which signals are required and which signals are optional, refer to Section 2, “DFI Signal Requirements,” on page 19.

## **3.7 Low Power Control Interface**

The Low Power Control interface handles transmission of signals to enter and exit an idle state; the interface includes signals and timing parameters. Low Power Control is an optional feature for both the MC and the PHY unless the system requires a low power interface. It may be advantageous to place the PHY in a low power state when the MC has knowledge that the memory subsystem will remain in the idle state for a period of time. Depending on the state of the system, the MC communicates state information to the PHY allowing the PHY to enter the appropriate power saving state.

The Low Power Control interface consists of signals that inform the PHY of a low power mode opportunity, as well as how quickly the MC will require the PHY to resume normal operation, and timing parameters. Section 19, “Low Power Control Interface Signals,” on page 56 describes the signals used in the low power control interface: **dfi\_lp\_req** (low power opportunity request), **dfi\_lp\_ack** (low power acknowledge) and **dfi\_lp\_wakeup** (low power wakeup time).

Table 20, “Low Power Control Timing Parameters,” on page 58 describes the timing parameters: **t<sub>lp\_resp</sub>** and **t<sub>lp\_wakeup</sub>**.

More information on the low power control interface is provided in Section 4.12, “Low Power Control Handshaking,” on page 124. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the low power interface are listed in Table 19, “Low Power Control Interface Signals”.

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**TABLE 19.** *Low Power Control Interface Signals*

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Signal	From	Width	Default	Description
<b>dfi_lp_ack</b>	PHY	1 bit	0x0	<p><u>Low power acknowledge.</u> The <b>dfi_lp_ack</b> signal is asserted to acknowledge the MC low power opportunity request. The PHY is not required to acknowledge this request.</p> <p>If the PHY acknowledges the request, the <b>dfi_lp_ack</b> signal must be asserted within <b>t<sub>lp_resp</sub></b> cycles after the <b>dfi_lp_req</b> signal assertion. Once asserted, this signal should remain asserted until the <b>dfi_lp_req</b> signal de-asserts. The signal must de-assert within <b>t<sub>lp_wakeup</sub></b> cycles after the <b>dfi_lp_req</b> signal de-asserts, indicating that the PHY is able to resume normal operation.</p> <p>If the PHY ignores the request, the <b>dfi_lp_ack</b> signal must remain de-asserted for the remainder of the low power mode opportunity. The <b>dfi_lp_req</b> signal is asserted for at least <b>t<sub>lp_resp</sub></b> cycles.</p>
<b>dfi_lp_req</b>	MC	1 bit	0x0	<p><u>Low power opportunity request.</u> The <b>dfi_lp_req</b> signal is used by the MC to inform the PHY of an opportunity to switch to a low power mode.</p> <p>The MC must assert a constant value on the <b>dfi_lp_wakeup</b> signal while this signal is asserted before the request is acknowledged by the PHY through the assertion of the <b>dfi_lp_ack</b> signal or until <b>t<sub>lp_resp</sub></b> cycles have elapsed.</p> <p>The MC may increase the value of the <b>dfi_lp_wakeup</b> signal if both the <b>dfi_lp_req</b> and <b>dfi_lp_ack</b> signals are asserted.</p> <p>Following the de-assertion of the <b>dfi_lp_req</b> signal, the PHY has <b>t<sub>lp_wakeup</sub></b> cycles to resume normal operation and de-assert the <b>dfi_lp_ack</b> signal.</p>



TABLE 19. Low Power Control Interface Signals

Signal	From	Width	Default	Description
<b>dfi_lp_wakeup</b>	MC	4 bits	_ a	<p><u>Low power wakeup time.</u> The <b>dfi_lp_wakeup</b> signal indicates which one of the 16 wakeup times the MC is requesting for the PHY.</p> <p>The signal is only valid when the <b>dfi_lp_req</b> signal is asserted. The <b>dfi_lp_wakeup</b> signal must remain constant until the <b>dfi_lp_ack</b> signal is asserted. Once the request has been acknowledged, the MC may increase the <b>dfi_lp_wakeup</b> signal, permitting the PHY to enter a lower power state. The PHY is not required to change power states in response to the wakeup time change.</p> <p>The MC may not decrease this value once the request has been acknowledged. The value of the <b>dfi_lp_wakeup</b> signal at the time that the <b>dfi_lp_req</b> signal is de-asserted sets the <b>t<sub>lp_wakeup</sub></b> time.</p> <ul style="list-style-type: none"> <li>• ‘b0000 = <b>t<sub>lp_wakeup</sub></b> is 16 cycles</li> <li>• ‘b0001 = <b>t<sub>lp_wakeup</sub></b> is 32 cycles</li> <li>• ‘b0010 = <b>t<sub>lp_wakeup</sub></b> is 64 cycles</li> <li>• ‘b0011 = <b>t<sub>lp_wakeup</sub></b> is 128 cycles</li> <li>• ‘b0100 = <b>t<sub>lp_wakeup</sub></b> is 256 cycles</li> <li>• ‘b0101 = <b>t<sub>lp_wakeup</sub></b> is 512 cycles</li> <li>• ‘b0110 = <b>t<sub>lp_wakeup</sub></b> is 1024 cycles</li> <li>• ‘b0111 = <b>t<sub>lp_wakeup</sub></b> is 2048 cycles</li> <li>• ‘b1000 = <b>t<sub>lp_wakeup</sub></b> is 4096 cycles</li> <li>• ‘b1001 = <b>t<sub>lp_wakeup</sub></b> is 8192 cycles</li> <li>• ‘b1010 = <b>t<sub>lp_wakeup</sub></b> is 16384 cycles</li> <li>• ‘b1011 = <b>t<sub>lp_wakeup</sub></b> is 32768 cycles</li> <li>• ‘b1100 = <b>t<sub>lp_wakeup</sub></b> is 65536 cycles</li> <li>• ‘b1101 = <b>t<sub>lp_wakeup</sub></b> is 131072 cycles</li> <li>• ‘b1110 = <b>t<sub>lp_wakeup</sub></b> is 262144 cycles</li> <li>• ‘b1111 = <b>t<sub>lp_wakeup</sub></b> is unlimited</li> </ul>

a. This signal is not meaningful during initialization; no default value is required.

The timing parameters associated with the low power interface are listed in Table 20, “Low Power Control Timing Parameters”.

**TABLE 20.** *Low Power Control Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
<b>t<sub>lp_resp</sub></b>	MC	1 <sup>a</sup>	7	DFI clock cycles	Specifies the maximum number of DFI clock cycles after the assertion of the <b>dfi_lp_req</b> signal to the assertion of the <b>dfi_lp_ack</b> signal.
<b>t<sub>lp_wakeup</sub></b>	MC	16	_ <sup>b</sup>	DFI clock cycles	Specifies the target maximum number of DFI clock cycles that the <b>dfi_lp_ack</b> signal may remain asserted after the de-assertion of the <b>dfi_lp_req</b> signal. The <b>dfi_lp_ack</b> signal may de-assert at any cycle after the de-assertion of the <b>dfi_lp_req</b> signal.

- a. It is recommended to fix this timing parameter at 7 cycles.
- b. The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

### 3.8 Error Interface

The error interface handles the transmission of error information; the interface includes signals and timing parameters. The error interface is an optional feature for both the MC and the PHY.

In a DDR memory sub-system, the PHY may detect various error conditions including DRAM errors (e.g., ECC errors) or PHY-specific errors (e.g., loss of DLL lock or a read DQS error). In error-condition scenarios, it may be desirable to communicate the error information from the PHY to the MC for error reporting and other possible error responses. The MC is not required to take any action other than reporting errors.

The error interface defines two signals and a timing parameter. The PHY may support the **dfi\_error** signal with or without **dfi\_error\_info**. The PHY may use a subset of the **dfi\_error\_info** signal; un-driven signals must be tied LOW at the MC.

The error signals are not phased for Frequency Ratio. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

The signals associated with the error interface are listed in Table 21, “Error Signals”.

**TABLE 21.** *Error Signals*

Signal	From	Width	Default	Description
<b>dfi_error</b>	PHY	DFI Error Width	0	<u>DFI Error</u> . Indicates that the PHY has detected an error condition.
<b>dfi_error_info</b>	PHY	DFI Error Width * x 4	0	<u>DFI Error Info</u> . Provides additional information about the source of the error detected. Only considered valid when <b>dfi_error</b> is asserted.

Typically, the width of the **dfi\_error** signal would be equal to 1-bit per data slice plus 1 bit for control. The PHY may implement **dfi\_error** as a single bit or any other width not exceeding the sum of the data slices + 1 bit for control. The MC should accept 1 bit per instance as defined by the sum of data slices plus 1 bit for control.

The **dfi\_error\_info** signal is 4-bits per instance. The number of instances should be the same for the **dfi\_error** and **dfi\_error\_info** signals. The **dfi\_error\_info** signal is defined for some error types in this specification and may be further defined as design-specific errors by the PHY.

The error interface defines a maximum timing parameter,  $t_{\text{error\_resp}}$ . The timing parameter defines the maximum delay between receiving a command or data, and detection of an error associated with that command or data.

The timing parameter associated with the error interface is listed in Table 22, “Error Timing Parameter”.

**TABLE 22.** *Error Timing Parameter*

Parameter	Defined By	Min	Max	Unit	Description
$t_{\text{error\_resp}}$	PHY	1	a	DFI clock cycles	Specifies the maximum number of DFI clock cycles that may occur from the DFI bus transaction(s) which are known to be affected by the error condition and the assertion of the <b>dfi_error</b> signal.

- a. The minimum supportable value is 1; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

## 4.0 Functional Use

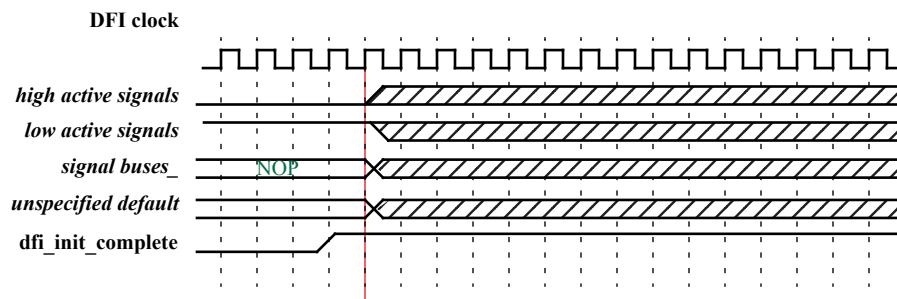
While some of the diagrams illustrate DFI PHY signals, these signals are only an interpretive example of internal PHY signals, they are not signals on the DFI.

### 4.1 Initialization

The DFI signals that communicate commands or status, shown in Figure 3, “Dependency on **dfi\_init\_complete**”, must maintain their default value until the **dfi\_init\_complete** signal is asserted.

FIGURE 3.

Dependency on **dfi\_init\_complete**



The default value for each signal is listed in the corresponding interface table. For example, the default for control signals are listed in the default column of Table 4, “Control Signals,” on page 27.

1. High active signals have a default value of 0 (e.g., **dfi\_odt**, **dfi\_wrdata\_en**).
2. Low active signals have a default value of 1 (e.g., **dfi\_cs\_n**, **dfi\_we\_n**).
3. Signal buses have an unspecified default value (e.g., **dfi\_address**<sup>1</sup>, **dfi\_cid**).
4. State-specific signals have state-specific values (e.g., **dfi\_dram\_clk\_disable**, **dfi\_parity\_in**).

1. The **dfi\_address** signal does not have a default value in most cases. However, for LPDDR2 DRAMs, the **dfi\_address** bus must drive a NOP command until the **dfi\_init\_complete** signal is asserted.

The **dfi\_init\_start** signal is used to indicate that the MC is ready to drive the DFI signals and that two optional signals of the status interface (**dfi\_data\_byte\_disable** and **dfi\_freq\_ratio**) are valid. The **dfi\_data\_byte\_disable** signal informs the PHY if the MC is disabling certain byte lanes from use during data transfers, and the **dfi\_freq\_ratio** signal identifies the MC:PHY frequency ratio. The PHY may use the **dfi\_init\_start** signal assertion to know that these status signals are valid.

Figure 4, “System Setting Signals - **dfi\_init\_start** Asserts Before **dfi\_init\_complete**” shows that during initialization, if data byte disabling or the frequency ratio protocol are implemented, the **dfi\_init\_start** signal should only be asserted after the **dfi\_data\_byte\_disable** and/or the **dfi\_freq\_ratio** signals have been defined. If the PHY requires this information for proper initialization, the PHY should wait for the

**dfi\_init\_start** assertion before asserting the **dfi\_init\_complete** signal. Once asserted, the MC may release or hold the **dfi\_init\_start** signal.

FIGURE 4.

System Setting Signals - **dfi\_init\_start** Asserts Before **dfi\_init\_complete**

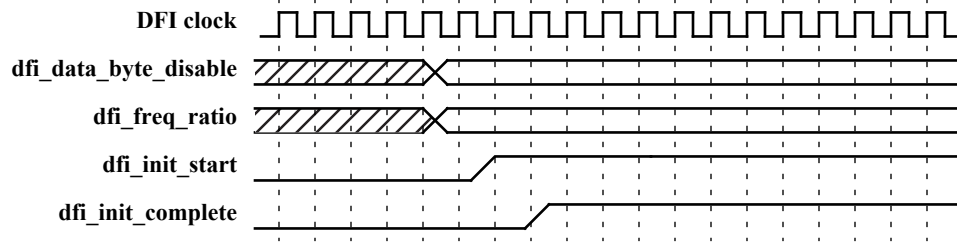
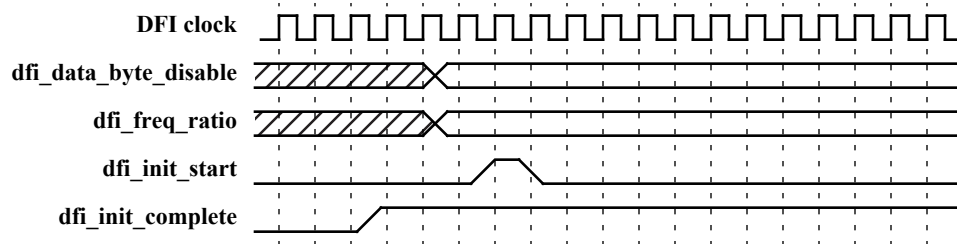


Figure 5, “System Setting Signals - **dfi\_init\_start** Asserts After **dfi\_init\_complete**” shows that the **dfi\_init\_complete** signal may be asserted before the assertion of the **dfi\_init\_start** signal. If neither the data byte disabling nor the frequency ratio protocol are implemented, or the PHY does not require this information for proper initialization, the PHY may assert the **dfi\_init\_complete** signal without regard to the assertion of the **dfi\_init\_start** signal.

NOTE: The **dfi\_init\_start** signal must be asserted during initialization, even if the PHY is not requiring this information. The MC may immediately de-assert the **dfi\_init\_start** signal, or may continue to hold it asserted.

FIGURE 5.

System Setting Signals - **dfi\_init\_start** Asserts After **dfi\_init\_complete**



The DFI specification does not impose or dictate a reset sequence or any type of signal training for either the PHY or the MC prior to DFI signal assertion. However, the assertion of the **dfi\_init\_complete** signal signifies that the PHY is ready to respond to any assertions on the DFI by the MC and ensures appropriate responses on the DFI. The PHY must guarantee the integrity of the address and control interface to the DRAMs prior to asserting the **dfi\_init\_complete** signal.

For LPDDR2 DRAMs, the **dfi\_address** bus must drive a NOP command until the **dfi\_init\_complete** signal is asserted and the signals **dfi\_act\_n**, **dfi\_bank**, **dfi\_bg**, **dfi\_cid**, **dfi\_cas\_n**, **dfi\_ras\_n** and **dfi\_we\_n** are unused and must remain at a constant value when the DFI bus is being used.

Some of the training interface signals must remain at default until after the assertion of the **dfi\_init\_complete** signal. No default value must be maintained for the following signals: **dfi\_act\_n**, **dfi\_bank**, **dfi\_bg**, **dfi\_wrdata**, **dfi\_wrdata\_mask**, **dfi\_rddata**, **dfi\_phyupd\_type**, **dfi\_rdlvl\_resp**, **dfi\_wrlvl\_resp** and **dfi\_lp\_wakeup**. The **dfi\_address** signal also has no default value except for LPDDR2 DRAMs.

## 4.2 Control Signals

The DFI control signals consist of the Command Address (CA) signals **dfi\_act\_n**, **dfi\_address**, **dfi\_bank**, **dfi\_bg**, **dfi\_cas\_n**, **dfi\_ras\_n** and **dfi\_we\_n**, and **dfi\_cid**, **dfi\_cke**, **dfi\_cs\_n**, **dfi\_odt**, and **dfi\_reset\_n**. The DFI control signals correlate to the DRAM control signals, and are driven according to the timing parameters **t<sub>ctrl\_delay</sub>** and **t<sub>cmd\_lat</sub>**.

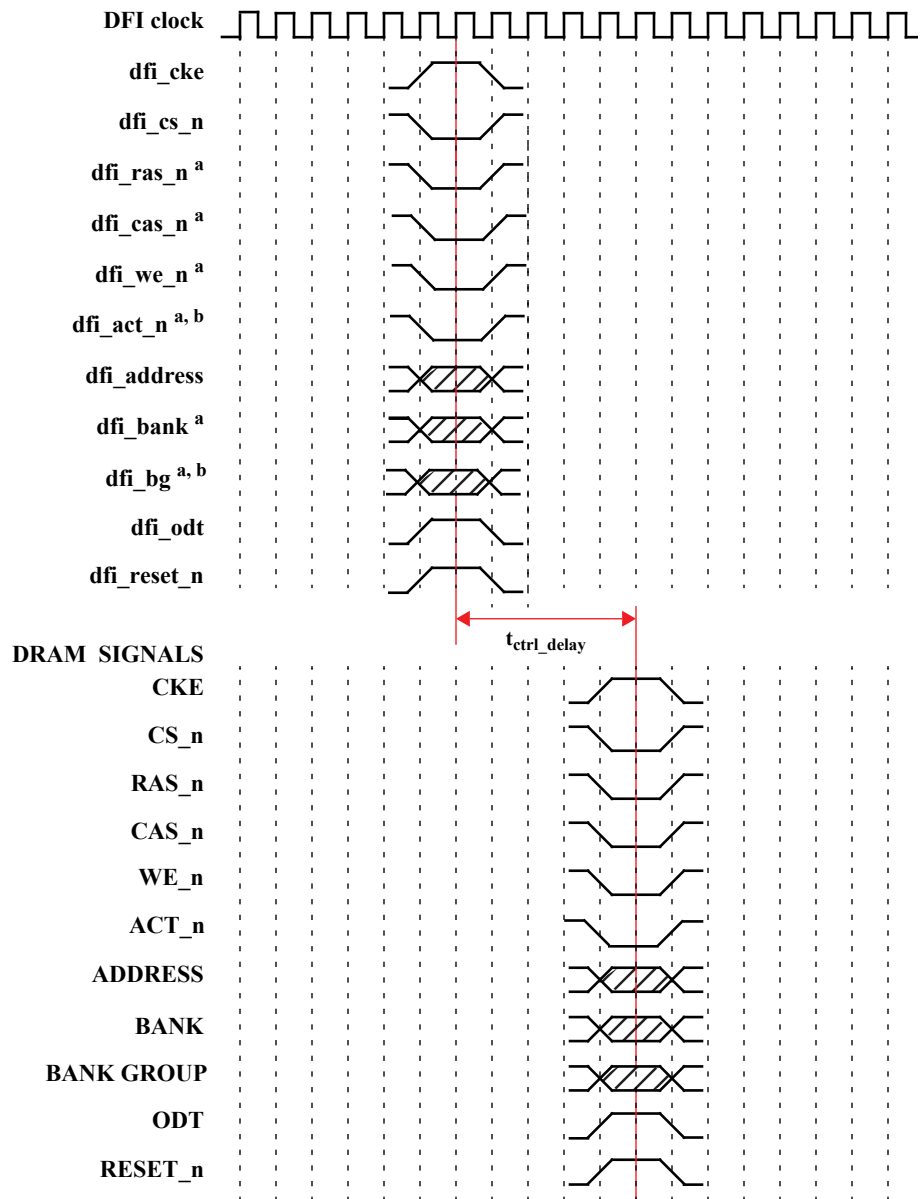
For more information on control signals and parameters, refer to Section 3.1, “Control Interface”.

Figure 6, “DFI Control Interface Signal Relationships” shows that the control signals are driven to the DRAMs and the DFI relationship of the control signals is expected to

be maintained at the PHY-DRAM boundary so any delays should be consistent across all signals and defined through the timing parameter  $t_{ctrl\_delay}$ .

FIGURE 6.

DFI Control Interface Signal Relationships



- a) For LPDDR2, these signals are not used and should be held in an idle state.
- b) Only valid for DDR4; held constant for non-DDR4 systems.

The system may not utilize all of the pins on the DRAM interface such as additional banks and chip selects, however, these signals must still be driven through the DFI and may not be left floating.

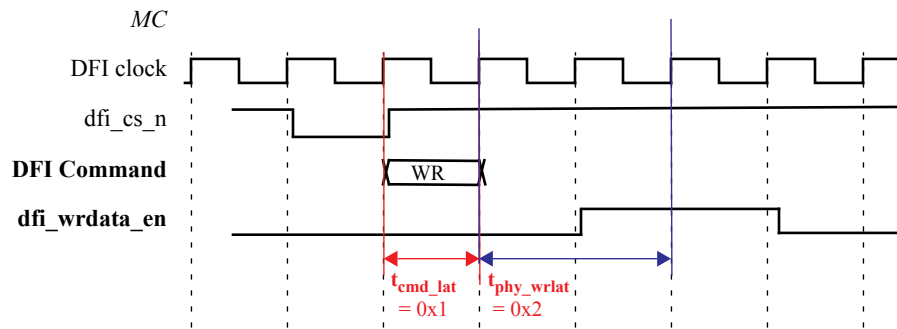
Based on current DRAM settings, the MC defines  $t_{cmd\_lat}$  with the parameter value defining when the CA bus is driven for each command. The timing of the CA bus assertion is relative to the assertion of **dfi\_cs\_n**.

Figure 7, “Example of  $t_{cmd\_lat}$  ( $t_{cmd\_lat}=1$ ,  $t_{phy\_wrlat}=2$ )” illustrates how the  $t_{cmd\_lat}$  parameter relates the DFI command to the DFI chip select. Furthermore, Figure 7 shows how DFI timing parameters, such as  $t_{phy\_wrlat}$ , relate to the DFI command when  $t_{cmd\_lat}$  is defined as a non-zero value.

For more information on  $t_{cmd\_lat}$ , refer to Table 5, “Control Timing Parameters,” on page 28.

FIGURE 7.

Example of  $t_{cmd\_lat}$  ( $t_{cmd\_lat}=1$ ,  $t_{phy\_wrlat}=2$ )



### 4.3 Data Bus Inversion

DBI is an optional DFI feature used with write and read data transmissions to generate write DBI data and invert both write and read data for DBI as required. When DBI is enabled, the **phy\_dbi\_mode** parameter is applicable.

If **phy\_dbi\_mode** = 0, the MC controls the DBI functionality and the **dfi\_rddata\_dbi\_n** signal is required. If **phy\_dbi\_mode** = 1, the PHY performs DBI generation and data inversion. If DBI is required in a system, either the MC or the PHY can generate the DBI output to DRAM and the output must be used to selectively invert data for write commands.

The PHY defines the **phy\_dbi\_mode** parameter value to determine how DBI is handled, as defined in Table 8, “Write Data Programmable Parameters”.

If the MC supports DBI on DFI, the MC must support both settings of the **phy\_dbi\_mode** parameter; the MC must be able to generate DBI and invert the write data and read data



as needed for DBI, and interface with a PHY that generates and handles the data inversion for DBI. The PHY can optionally support either setting of the **phydbi\_mode** parameter; the PHY can optionally generate DBI and invert the write data and read data as required. If the PHY does not generate DBI and invert the corresponding write/read data, the PHY must be able to interface to a MC that has DBI support. When both CRC and DBI are enabled in a system, special care needs to be taken regarding where CRC and DBI are performed in order to operate correctly.

When **phydbi\_mode** = 0, the PHY transfers the read DBI data on **dfi\_rddata\_dbi** coincident with **dfi\_rddata**. The MC transfers the write DBI data on **dfi\_wrdata\_mask** coincident with **dfi\_wrdata**.

## **4.4 Write Transactions**

The write data transaction handles the transmission of write data across the DFI bus.

The DFI write transaction includes the signals for write data (**dfi\_wrdata**), write data mask (**dfi\_wrdata\_mask**), write data enable (**dfi\_wrdata\_en**), and the optional write data chip select (**dfi\_wrdata\_cs\_n**), and the associated timing parameters **t<sub>phy\_wrlat</sub>** and **t<sub>phy\_wrdata</sub>**, and programmable parameters **phy\_crc\_mode** and **phydbi\_mode**.

The **dfi\_wrdata\_en** signal must correlate with the number of data transfers executed on the DRAM bus; one continuous assertion of the **dfi\_wrdata\_en** signal may encompass data for multiple write commands.

If write data chip select is enable, the **dfi\_wrdata\_cs\_n** signal provides the target data path chip select value to each of the PHY data slices. For more information on these signals, refer to Section 3.2, “Write Data Interface,” on page 29.

### **4.4.1 Write Transaction Sequence**

The sequence for DFI write transactions is listed below; the effect of using the optional write data chip select, CRC, or DBI is shown within brackets.

1. The write command is issued.
2. **t<sub>phy\_wrlat</sub>** cycles elapse (**t<sub>phy\_wrlat</sub>** can be zero).

[If write data chip select is enabled, **t<sub>phy\_wrcslat</sub>** cycles elapse.]

The **t<sub>phy\_wrlat</sub>** parameter defines the number of cycles between when the write command is driven on the DFI to assertion of the **dfi\_wrdata\_en** signal. The **t<sub>phy\_wrlat</sub>** parameter is PHY-defined but may be specified in terms of other fixed system values.

The write timing parameters (**t<sub>phy\_wrdata</sub>** and **t<sub>phy\_wrlat</sub>**) must be held constant while commands are being executed on the DFI bus; however, if necessary, the write timing parameter values may be changed when the bus is in the idle state. The **t<sub>phy\_wrdata</sub>**

and  $t_{\text{phy\_wrlat}}$  timing parameters work together to define the number of cycles from the assertion of a write command on the DFI control interface to when write data is driven on the DFI bus and must be consistent with the write latency timing that correlates to the DRAM timing.

[If chip select is enabled, the PHY defines the  $t_{\text{phy\_wrclat}}$  timing parameter to specify the desired alignment of the command to the **dfi\_wrdata\_cs\_n** signal; the PHY defines the  $t_{\text{phy\_wrcsgap}}$  timing parameter to specify the additional delay it requires between two consecutive commands that are targeting different chip selects. The  $t_{\text{phy\_wrclat}}$  timing parameter must be held constant while commands are being executed on the DFI bus; however, if necessary, the  $t_{\text{phy\_wrclat}}$  parameter value may be changed when the bus is in the idle state. The PHY may require the MC to add delay beyond other system timing requirements to account for PHY-specific adjustments transitioning between data path chip selects.]

[The gap timing requirement may only be applicable to certain chip-select-to-chip-select transitions and not be applicable to other data path chip select transitions where the PHY is not required to make an internal adjustment on the transition; this gap timing requirement is system-specific. For example, a system may not require additional delay on transitions between chip select 0 and chip select 1, but may require additional delay when transitioning from chip select 0 to chip select 2. Accordingly, the interface does not require the gap timing to be applied to every chip select transition.]

3. [If chip select is enabled and the MC supports chip select, the MC drives **dfi\_wrdata\_cs\_n** a minimum of the DFI data transfer width ( $\text{dfi\_rw\_length}$ ) plus the gap timing ( $t_{\text{phy\_wrcsgap}}$ ). The minimum time the chip select is guaranteed to remain driven to the PHY relative to the write command is defined by  $t_{\text{phy\_wrclat}} + \text{dfi\_rw\_length} + t_{\text{phy\_wrcsgap}}$ .

The maximum delay that can be achieved between the assertion of a new chip select value on **dfi\_wrdata\_cs\_n** and the corresponding **dfi\_wrdata\_en** is limited to the maximum time the PHY has from changing the target chip select to receiving the write data transfer ( $t_{\text{phy\_wrlat}} - t_{\text{phy\_wrclat}}$ ).

The PHY must define the  $t_{\text{phy\_wrclat}}$  and  $t_{\text{phy\_wrcsgap}}$  timing parameters to allocate the time between transactions to different chip selects necessary for PHY-specific adjustments.

If the MC does not support chip select but the PHY does support it, the PHY inputs should be tied-off disabled.]

4. For non-contiguous write commands, the **dfi\_wrdata\_en** signal is asserted on the DFI after  $t_{\text{phy\_wrlat}}$  is met and remains asserted for the number of cycles required to complete the write data transfer sent on the DFI control interface;  $t_{\text{phy\_wrlat}}$  can be zero.

[If CRC is enabled, the MC extends the **dfi\_wrdata\_en** signal to accommodate the extended DRAM burst length and the signal is asserted for an odd number of cycles per burst.]

5. For contiguous write commands, the **dfi\_wrdata\_en** signal is asserted after **t<sub>phy\_wrlat</sub>** is met and remains asserted for the entire length of the data stream; **t<sub>phy\_wrlat</sub>** can be zero. [If CRC is enabled, the MC extends the **dfi\_wrdata\_en** signal to accommodate the extended DRAM burst length and the signal may be asserted for an odd number of cycles per burst.]
6. **t<sub>phy\_wrdata</sub>** cycles elapse.
7. The associated write data (**dfi\_wrdata**) and masking (**dfi\_wrdata\_mask**) signals are sent.

[If CRC is enabled, the MC utilizes the **dfi\_wrdata** bus to send CRC data to the PHY; the MC utilizes the **dfi\_wrdata\_pN** outputs for frequency ratio systems.]

[If DBI is enabled, **dfi\_wrdata\_mask** transfers the write data inversion information instead of the write data mask.]

The MC must always drive **dfi\_wrdata** and associated signals with the correct timing relative to the write command as defined by the timing parameters **t<sub>phy\_wrdata</sub>** and **t<sub>phy\_wrlat</sub>**.

The **t<sub>phy\_wrdata</sub>** parameter defines the timing requirements between the assertion of the **dfi\_wrdata\_en** signal assumed and when the write data is driven on the **dfi\_wrdata** signal. The exact value of the **t<sub>phy\_wrdata</sub>** parameter for a particular application is determined by how many cycles the PHY must receive the **dfi\_wrdata\_en** signal prior to receiving the **dfi\_wrdata** signal.

If the PHY requires notification of pending write data sooner than 1 cycle, the **t<sub>phy\_wrdata</sub>** parameter may be increased. However, setting **t<sub>phy\_wrdata</sub>** to a value greater than 1 may restrict the minimum write latency supported by the interface. The DFI specification does not dictate a value for the **t<sub>phy\_wrdata</sub>** parameter.

8. The **dfi\_wrdata\_en** signal de-asserts **t<sub>phy\_wrdata</sub>** cycles before the last valid data is transferred on the **dfi\_wrdata** bus.
9. **t<sub>phy\_wrdata\_delay</sub>** cycles elapse. The DFI bus enters the idle state.

The idle state timing parameter defines the number of DFI clocks from **dfi\_wrdata\_en** to the completion of the write data transfer on the DRAM bus. The MC drives the next value (any valid chip select or inactive).

Seven situations showing system behavior with two write transactions are presented in Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13 and Figure 14. System behavior with three write transactions using **dfi\_wrdata\_cs\_n** is shown in Figure 15,

“Write Commands Utilizing dfi\_wrdata\_cs\_n,” on page 73.

Figure 8, shows back-to-back writes for a system with a  $t_{\text{phy\_wrlat}}$  of zero and a  $t_{\text{phy\_wrdata}}$  of one. The **dfi\_wrdata\_en** signal is asserted with the write command for this situation, and is asserted for two cycles per command to inform the DFI that two cycles of DFI data are sent for each write command. The timing parameters and the timing of the write commands allow the **dfi\_wrdata\_en** signal and the **dfi\_wrdata** stream to be sent contiguously.

FIGURE 8.

Back-to-Back Writes (DRAM Burst of 4:  $t_{\text{phy\_wrlat}}=0$ ,  $t_{\text{phy\_wrdata}}=1$ )

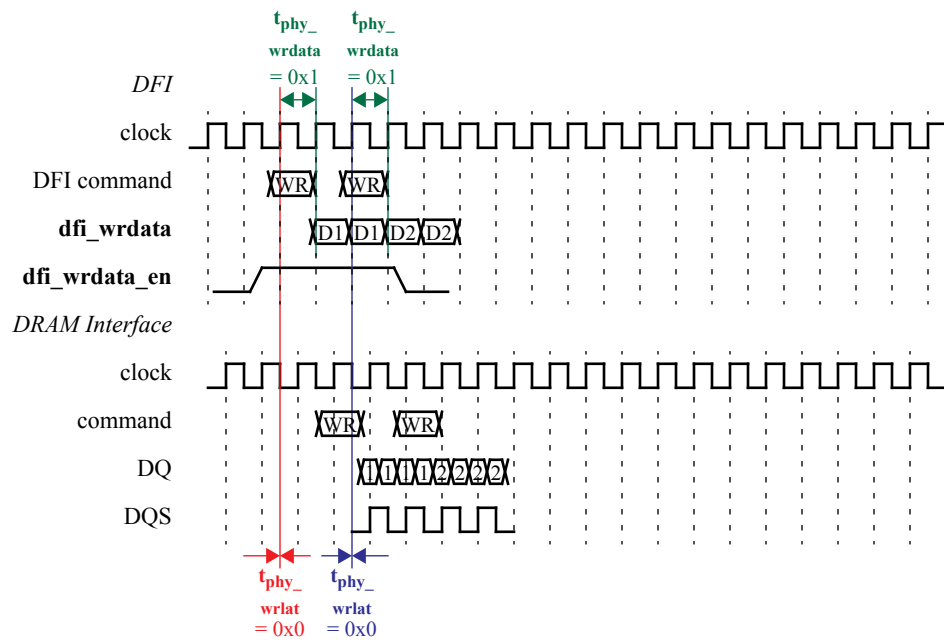


Figure 9 shows an interrupted write command. The **dfi\_wrdata\_en** signal should be asserted for 4 cycles for each of these write transactions. However, since the first write is interrupted, the **dfi\_wrdata\_en** signal is asserted for a portion of the first transaction and the complete second transaction. The **dfi\_wrdata\_en** signal will not de-assert

between write commands, and the **dfi\_wrddata** stream will be sent contiguously for a portion of the first command and the complete second command.

**FIGURE 9.**

*Back-to-Back Interrupted Contiguous Writes (DRAM Burst of 8:  $t_{\text{phy\_wrlat}}=3$ ,  $t_{\text{phy\_wrdata}}=2$ )*

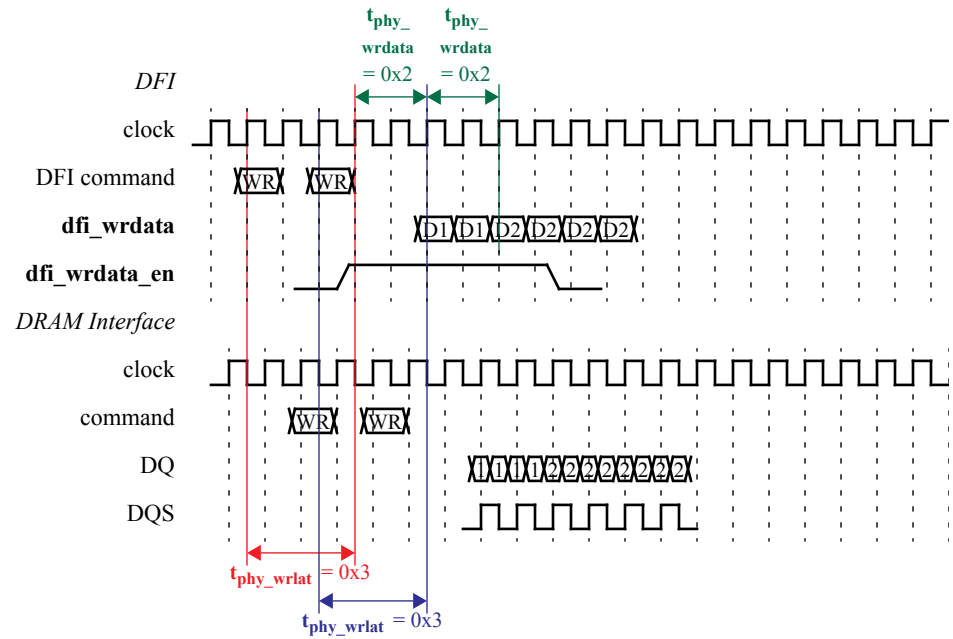


Figure 10 shows back-to-back burst-of-8 writes. The **dfi\_wrdata\_en** signal must be asserted for 4 cycles for each of these write transactions.

**FIGURE 10.**

*Back-to-Back Writes (DRAM Burst of 8:  $t_{\text{phy\_wrlat}}=4$ ,  $t_{\text{phy\_wrdata}}=4$ )*

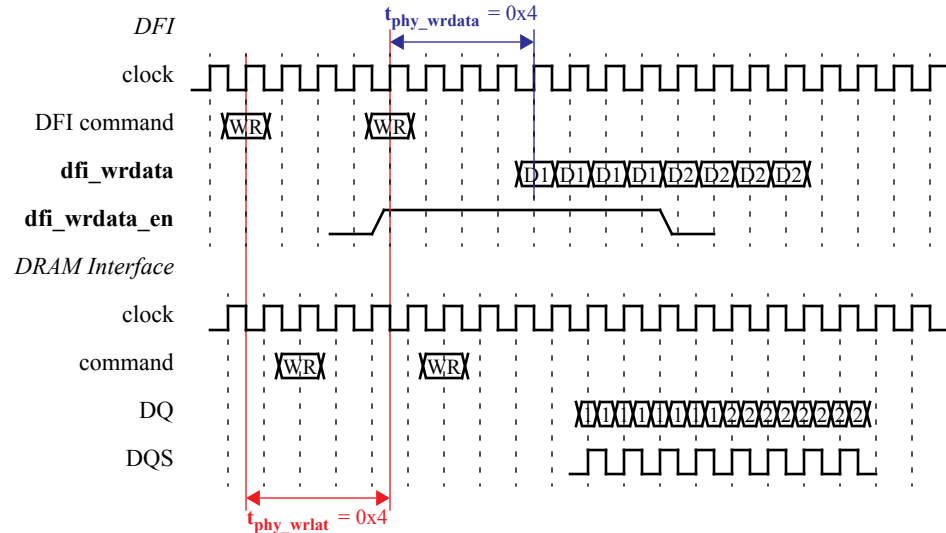


Figure 11, Figure 12, Figure 13 and Figure 14 also show two complete write commands, with different  $t_{\text{phy\_wrlat}}$  and  $t_{\text{phy\_wrdata}}$  timing parameters and for different DRAM types. The **dfi\_wrdata\_en** signal is asserted for two cycles for each write transaction. The  $t_{\text{phy\_wrlat}}$  timing and the timing between the write commands causes

the **dfi\_wrdata\_en** signal to be de-asserted between commands. As a result, the **dfi\_wrdata** stream is non-contiguous.

FIGURE 11.

Two Independent Writes (DRAM Burst of 4:  $t_{\text{phy\_wrlat}}=0$ ,  $t_{\text{phy\_wrdata}}=1$ )

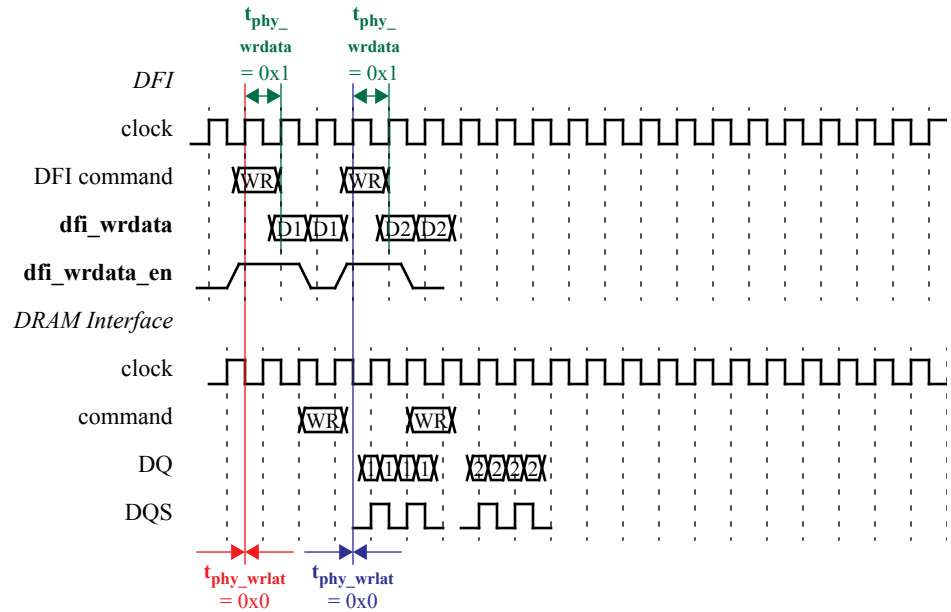


FIGURE 12.

Two Independent Writes (DRAM Burst of 4:  $t_{\text{phy\_wrlat}}=3$ ,  $t_{\text{phy\_wrdata}}=1$ )

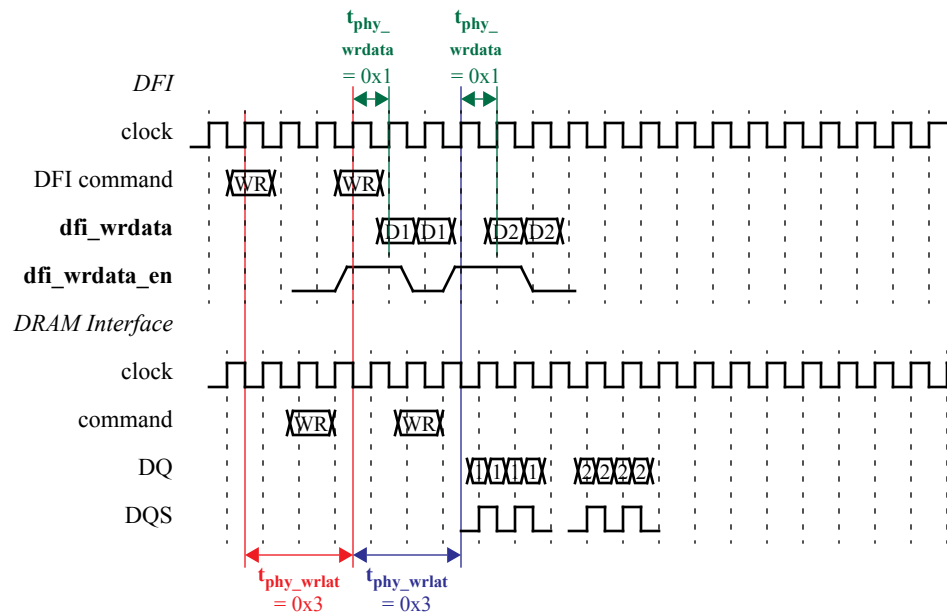


FIGURE 13.

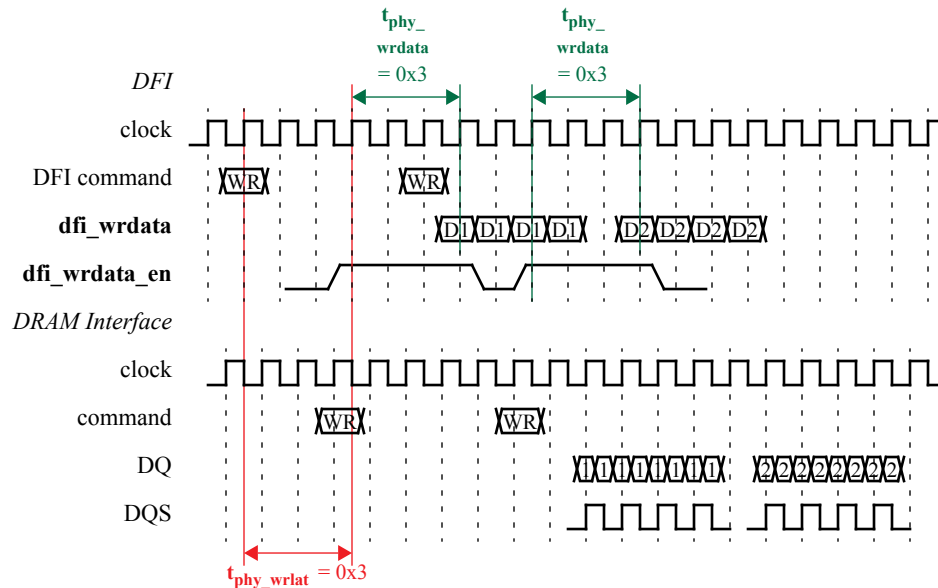
Two Independent Writes (DRAM Burst of 8:  $t_{\text{phy\_wrlat}}=3$ ,  $t_{\text{phy\_wrdata}}=3$ )

FIGURE 14.

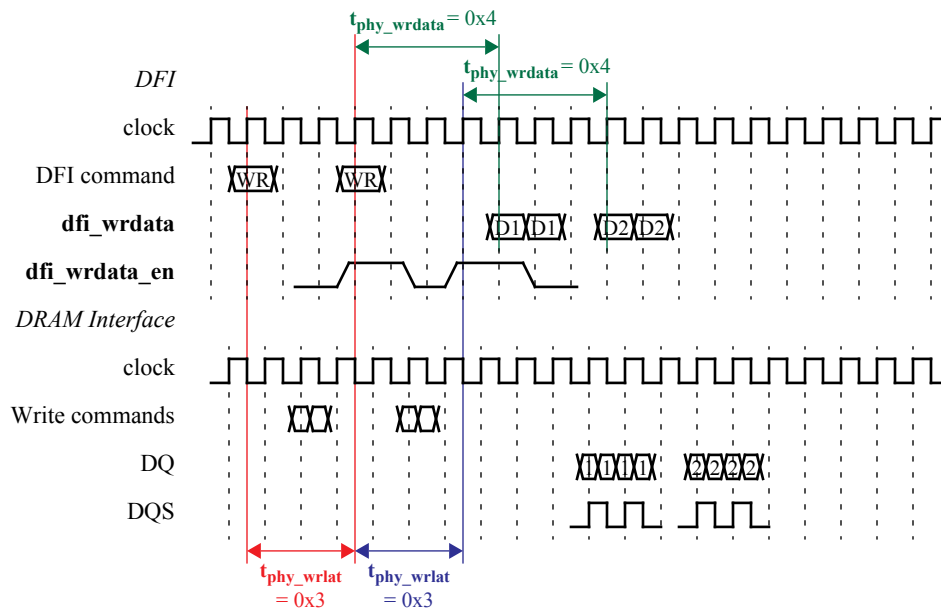
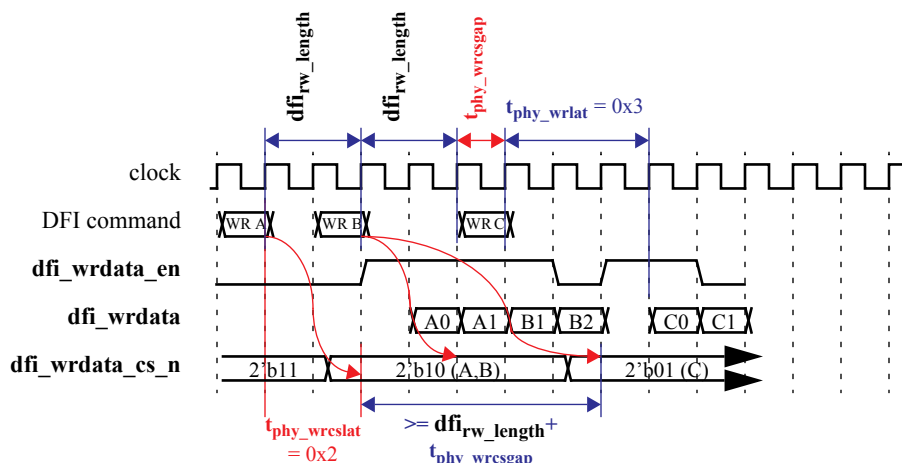
Two Independent Writes (DRAM Burst of 4:  $t_{\text{phy\_wrlat}}=3$ ,  $t_{\text{phy\_wrdata}}=4$ )



Figure 15, “Write Commands Utilizing dfi\_wrdata\_cs\_n” shows three write commands, with a gap between the second and third commands.

FIGURE 15.

Write Commands Utilizing **dfi\_wrdata\_cs\_n**



#### 4.4.2 DBI - Write

DBI is an optional DFI feature used with write data transmissions. The **phy\_dbi\_mode** parameter is only needed when DBI is supported in DFI.

For more information on the **phy\_dbi\_mode** parameter, refer to Table 7, “Write Data Timing Parameters,” on page 32.

When the MC generates the write DBI data, the MC also inverts write data for DBI as required. The MC transmits the write DBI data across the DFI bus on **dfi\_wrdata\_mask\_pN**. In DBI mode, the PHY is only required to transfer the write DBI data through the PHY. While write data is transmitting, the DBI data transmits simultaneously on the **dfi\_wrdata\_mask** signal. The **dfi\_wrdata\_mask** signal is sent coincident with the corresponding **dfi\_wrdata** bus.

For frequency ratio systems, the **dfi\_wrdata\_mask** signal is extended, with a signal defined per phase.

When both DBI and CRC are enabled in a system, special care needs to be taken regarding where DBI and CRC are performed in order to operate correctly.

#### 4.4.3 Cyclic Redundancy Check

CRC is an optional DFI feature used with write data transmissions to send CRC data as part of the write data burst. CRC elongates a burst of 8 unit intervals (UI) from 8UI to

10UI. When CRC is used, either the MC or the PHY can generate the CRC data; the MC must generate the CRC data if the PHY does not generate it.

While either the MC or the PHY can generate the CRC data, the PHY defines the value of the **phy\_crc\_mode** programmable parameter. The **phy\_crc\_mode** parameter is only needed when CRC is supported in DFI and uses the following definition to determine how CRC is handled:

- **phy\_crc\_mode** == 0 → CRC generation is handled in the MC
- **phy\_crc\_mode** == 1 → CRC generation is handled in the PHY

When CRC is supported in DFI, the system must be capable of the conditions listed in Table 23, “Systems Requiring CRC Support”.

TABLE 23.

*Systems Requiring CRC Support*

Description	MC	PHY
Generates CRC Data	Yes	Optional
Interfaces with CRC Data	Yes	Yes <sup>a</sup>

a. Required if the PHY does not generate the CRC data.

Regardless of which device generates the CRC, the MC asserts ODT such that it applies to all data sent + CRC data words.

#### 4.4.3.1 MC CRC Support (**phy\_crc\_mode** == 0)

When the MC generates the CRC data, the **phy\_crc\_mode** == 0 and the MC has the following requirements.

- The MC must assert the **dfi\_wrdata\_en** signal for the data transmitted across the DFI bus, including CRC data.
- The MC spaces commands to handle an extended burst with CRC.
- The MC generates **dfi\_odt** (**dfi\_odt\_pN** in frequency ratio systems) based on the DRAM burst length including CRC data. With CRC enabled, the MC may need to extend ODT.
- The MC needs to receive and capture error information from the PHY. These CRC write data errors are transmitted on the **dfi\_alert\_n\_aN** signal. The MC must support a **dfi\_alert\_n\_aN** input. If the PHY does not generate the **dfi\_alert\_n\_aN** PHY output, the **dfi\_alert\_n\_aN** input to the MC should be tied to a de-asserted state.

With CRC, the **dfi\_wrdata\_en** signal could be asserted for an odd number of cycles per burst. Without exception, the PHY must support the odd CRC burst timing.

DFI dictates that when CRC is used, the CRC data word must be incorporated in the burst of write data, but DFI does not dictate placement within the burst. The specific

ODT timing requirements are dependent on the chip selects accessed and system architecture. The **dfi\_odt** assertion and de-assertion are identical in the MC CRC and PHY CRC support modes. The ODT signal timing shown is only an example of one potential solution.

To further compare MC CRC support mode and PHY CRC support mode, DFI ODT signals are included in Figure 16, “DFI Write Data Bus for MC CRC Support Mode (Two Bursts starting in Phase 0),” on page 75, Figure 18, “DFI Write Data Bus for PHY CRC Support Mode,” on page 78 and Figure 19, “DFI Write Data Bus for PHY CRC Support Mode with Burst Chop,” on page 79.

Figure 16 and Figure 17 illustrate the DFI write data bus for a 2:1 frequency ratio system with CRC extending a burst of 8 by 1 additional clock DRAM cycle.

The **dfi\_wrdata\_en** signal is only asserted for the data transmitted across the DFI, and consequently is not extended to include CRC data words.

FIGURE 16.

DFI Write Data Bus for MC CRC Support Mode (Two Bursts starting in Phase 0)

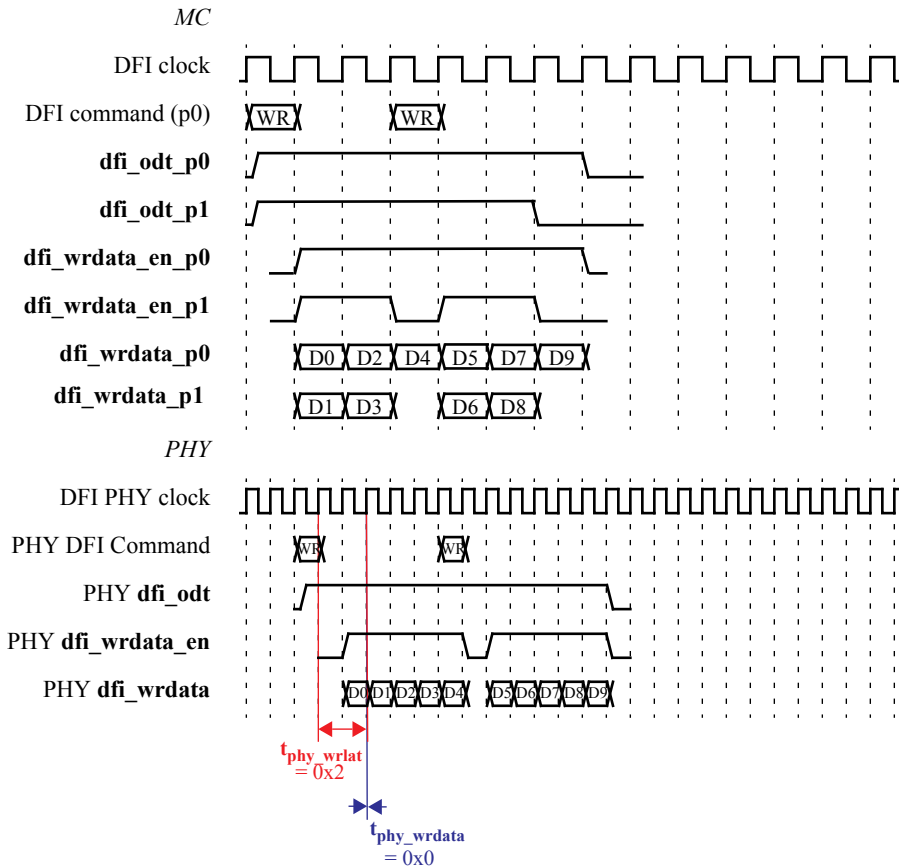
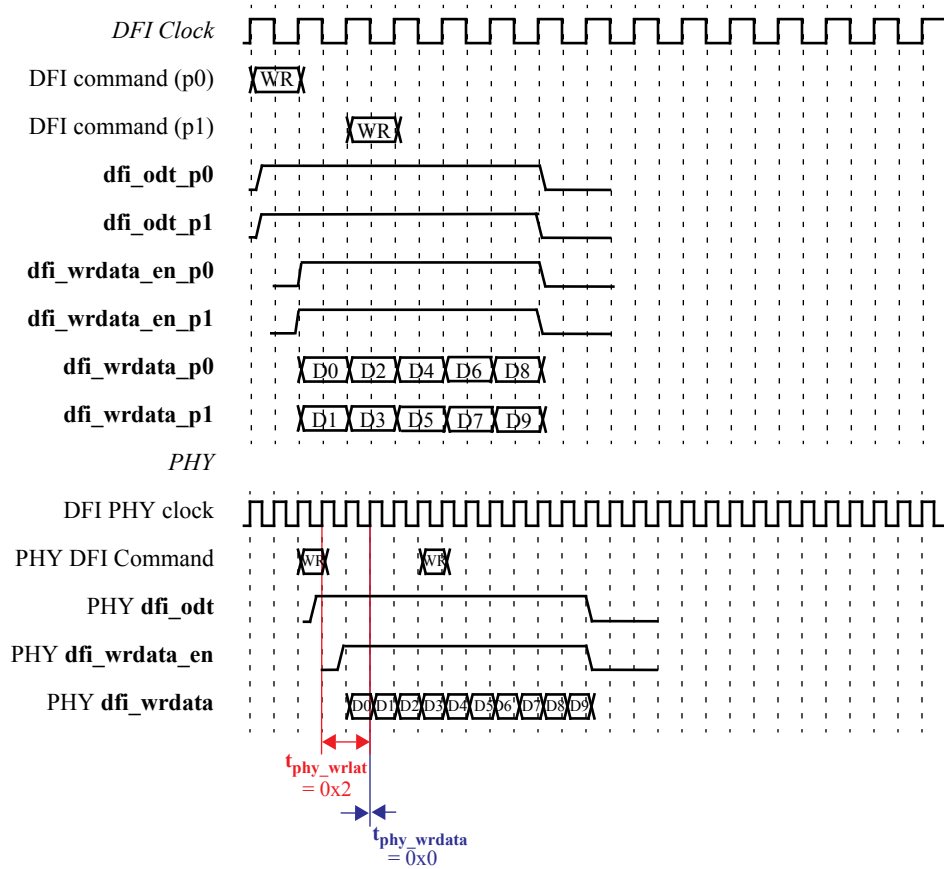


FIGURE 17.

DFI Write Data Bus for MC CRC Support Mode (Two Back-to-Back Bursts)



#### 4.4.3.2 PHY CRC Support ( $\text{phy\_crc\_mode} == 1$ )

If a PHY is capable of generating CRC data, the  $\text{phy\_crc\_mode} == 1$  and the MC has the following requirements.

- The MC must disable its CRC generation logic so that CRC data is not transmitted across the DFI bus for write commands.
- The MC must assert the **dfi\_wrdata\_en** signal only for the data transmitted across the DFI bus, NOT for CRC.
- The MC spaces commands to handle an extended burst with CRC.
- The MC generates **dfi\_odt** (**dfi\_odt\_pN** in frequency ratio systems) based on the DRAM burst length including CRC data. With CRC enabled, the MC may need to extend ODT.
- The MC needs to receive and capture error information from the PHY. These CRC write data errors are transmitted on the **dfi\_alert\_n\_aN** signal. The MC must support a **dfi\_alert\_n\_aN** input. If the PHY does not generate the **dfi\_alert\_n\_aN** PHY output, the **dfi\_alert\_n\_aN** input to the MC should be tied to a de-asserted state.

#### **4.4.3.3 Burst Chop 4 with PHY CRC Support (`phy_crc_mode == 1`)**

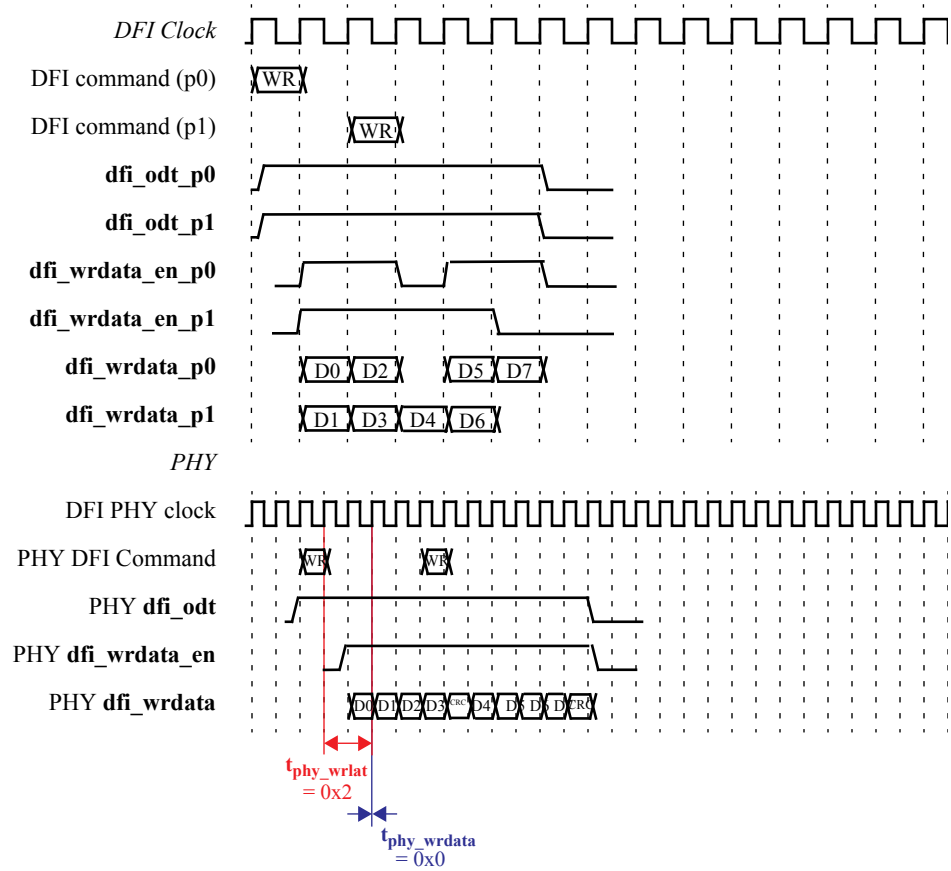
In Burst Chop4 (BC4) mode, the memory burst is extended for CRC, similar to a burst of 8 requiring a 10 UI transfer. When the PHY generates the CRC data, the controller does not adjust **dfi\_wrdata\_en\_pN** to account for the transfer of CRC data words. In a system supporting dynamic burst lengths and BC4, the PHY can use the width of the **dfi\_wrdata\_en\_pN** signal to determine whether a transfer is a burst of 8 or whether the transfer is a BC4 data transmission. The PHY can utilize this information to determine how to generate CRC and when to send the CRC data.

Figure 18 and Figure 19 show PHY outputs that include a single extra CRC data word, shown at the end of the burst (the location of the CRC data word is DRAM-dependent). The figures also show that **dfi\_odt** assertion and de-assertion for PHY CRC support are identical to the MC CRC Support mode in which the **dfi\_odt** signals are extended to cover both CRC and write data. The specific ODT timing requirements are dependent on the chip selects accessed and the system topology. The ODT signal timing shown is only an example of one potential solution.

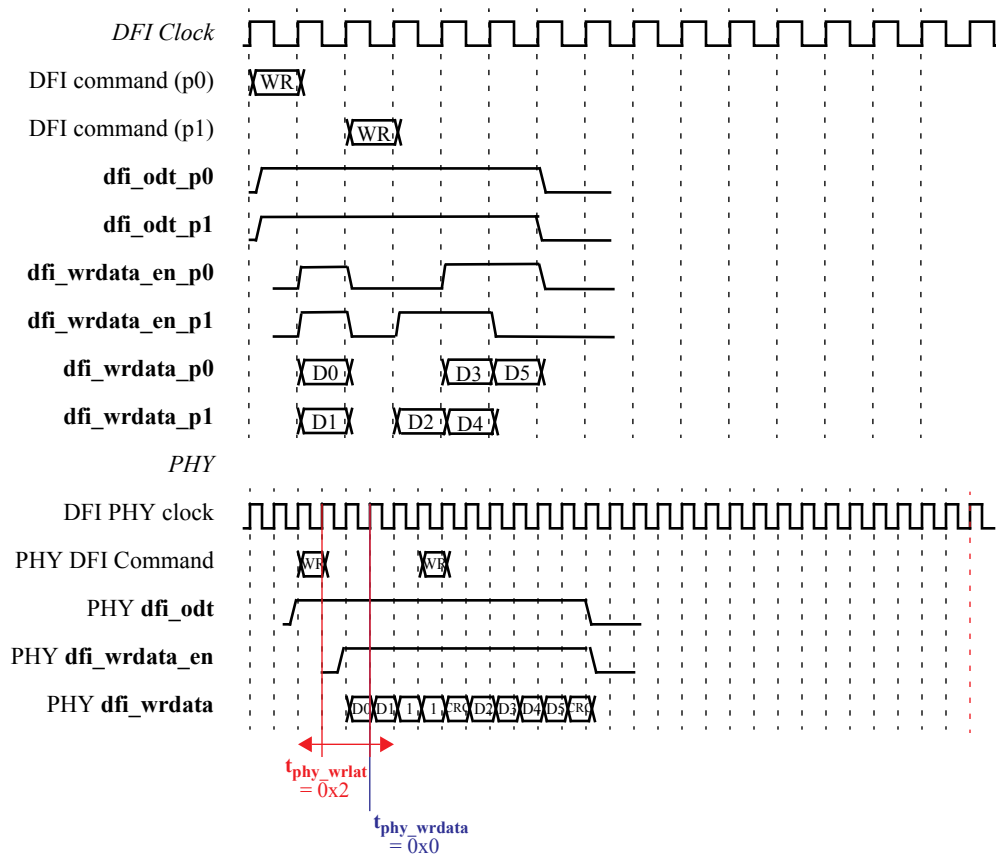
Figure 19, “DFI Write Data Bus for PHY CRC Support Mode with Burst Chop” illustrates a write BC4 case. This example shows a BC4 write followed by a burst of 8 write. With BC4, the MC only transmits 2 data words across the DFI bus. For both BC4 and burst of 8 commands, the CRC data is transmitted at the end of the burst, in UI9 and UI10.

FIGURE 18.

DFI Write Data Bus for PHY CRC Support Mode



**FIGURE 19.** *DFI Write Data Bus for PHY CRC Support Mode with Burst Chop*



## 4.5 Read Transactions

The read data transaction handles the capture and return of data across the DFI bus.

The DFI read transaction includes the signals for read data enable (**dfi\_rddata\_en**), read data (**dfi\_rddata**), read data valid (**dfi\_rddata\_valid**), target data chip select (**dfi\_rddata\_cs\_n**), and the DRAM-specific read data not valid (**dfi\_rddata\_dnv**) for LPDDR2 DRAMs, and **dfi\_rddata\_dbi** for DDR4 systems. The timing parameters are  $t_{rddata\_en}$  and  $t_{phy\_rdlat}$ .

The **dfi\_rddata\_en** signal must correlate with the number of data transfers executed on the DRAM bus.

If used, the **dfi\_rddata\_cs\_n** signal provides the target data path chip select value to each of the PHY data slices. For more information on these signals, refer to Section 3.3, “Read Data Interface,” on page 33.

For the DFI, the read data must be returned from the PHY within a maximum delay defined by the sum of the  $t_{\text{rddata\_en}}$  and  $t_{\text{phy\_rdlat}}$  timing parameters. The  $t_{\text{rddata\_en}}$  is a fixed delay, but the  $t_{\text{phy\_rdlat}}$  is defined as a maximum value. The delay can be adjusted as long as both the MC and the PHY coordinate the change such that the DFI specification is maintained. Both parameters may be expressed as equations based on other fixed system parameters.

#### 4.5.1 Read Transaction Sequence

The sequence for DFI read transactions is listed below; the effect of using the optional read data chip select or DBI is shown within brackets.

1. The read command is issued.
2.  $t_{\text{rddata\_en}}$  cycles elapse.

[If using read data chip select,  $t_{\text{phy\_rdcslat}}$  cycles elapse.]

[The PHY defines the  $t_{\text{phy\_rdcslat}}$  timing parameter to specify the desired alignment of the command to the **dfi\_rddata\_cs\_n** signal; the PHY defines the  $t_{\text{phy\_rdcsgap}}$  timing parameter to specify the additional delay it requires between two consecutive commands that are targeting different chip selects. The PHY may require the MC to add additional delay beyond other system timing requirements to account for PHY-specific adjustments transitioning between chip selects].

[The gap timing requirement is system-specific and may only be applicable to certain chip-select-to-chip-select transitions and not be applicable to other chip select transitions where the PHY is not required to make an internal adjustment on the transition. For example, a system may not require additional delay on transitions between chip select 0 and chip select 1, but may require additional delay when transitioning from chip select 0 to chip select 2. Accordingly, the interface does not require the gap timing to be applied on every chip select transition].

3. The  $t_{\text{rddata\_en}}$  parameter defines the timing requirements between the read command on the DFI interface and the assertion of the **dfi\_rddata\_en** signal to maintain synchronicity between the MC and the PHY for the start of contiguous read data expected on the DFI interface. The exact value of this parameter for a particular application is determined by memory system components. For non-contiguous read commands,  $t_{\text{rddata\_en}}$  cycles elapse, and the **dfi\_rddata\_en** signal is asserted on the DFI and remains asserted for the number of contiguous cycles that read data is expected.
4. For contiguous read commands,  $t_{\text{rddata\_en}}$  cycles after the first read command of the stream, the **dfi\_rddata\_en** signal is asserted and remains asserted for the entire length of the data stream.
5. One continuous assertion of the **dfi\_rddata\_en** signal may encompass data for multiple read commands. The **dfi\_rddata\_en** signal de-asserts to signify there is no more contiguous data expected from the DFI read command(s). Note that the **dfi\_rddata\_en** signal is not required to be asserted for any fixed number of cycles. The MC continues to drive **dfi\_rddata\_cs\_n** a minimum of the data transfer width



(**dfi\_rw\_length**) plus the gap timing (**t<sub>phy\_rdcsgap</sub>**); the MC may then drive the next chip select or a valid value (any valid chip select or inactive).

The minimum time the chip select is guaranteed to remain driven to the PHY relative to the read command is defined by **t<sub>phy\_rdcslat</sub> + dfi\_wr\_length + t<sub>phy\_rdcsgap</sub>**.

The maximum delay that can be achieved from the assertion of a new chip on **dfi\_rddata\_cs\_n** and the corresponding **dfi\_rddata\_en** is limited to the maximum time the PHY has to make internal adjustments associated with changing the target chip select relative to the read data transfer (**t<sub>rddata\_en</sub> - t<sub>phy\_rdcslat</sub>**).

The PHY must define the **t<sub>phy\_rdcslat</sub>** and **t<sub>phy\_rdcsgap</sub>** timing parameters to allocate the time between transactions to different chip selects necessary for internal adjustments.

6. The data is returned with the **dfi\_rddata\_valid** signal asserted.

[For LPDDR2 memory systems, the **dfi\_rddata\_dnv** signal has the same timing as the **dfi\_rddata** signal.]

7. The associated read data signal (**dfi\_rddata**) is sent.

[If DBI is enabled, the read data dbi signal (**dfi\_rddata\_dbi**) is sent coincident with the read data signal.]

Ten situations are presented in Figure 20, Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, Figure 26 and Figure 27, Figure 28 and Figure 29.

Figure 20 shows a single read transaction. In this case, the **dfi\_rddata\_en** signal is asserted for two cycles to inform the DFI that two cycles of DFI data are expected and data is returned **t<sub>phy\_rdlat</sub>** cycles after the **dfi\_rddata\_en** signal assertion.

FIGURE 20.

Single Read Transaction of 2 Data Words

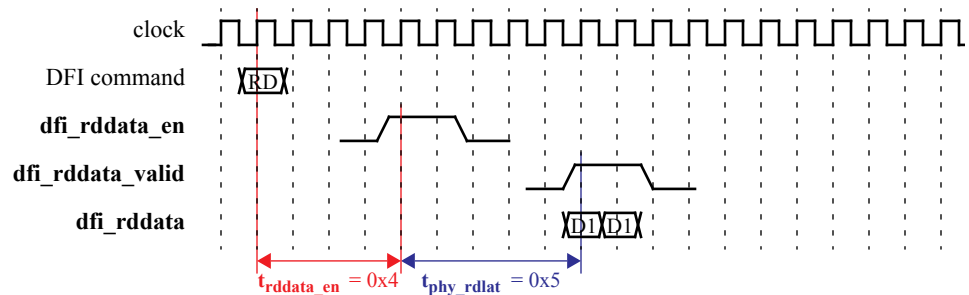


Figure 21 shows a single read transaction where the data is returned in less than the maximum delay. The data returns one cycle less than the maximum PHY read latency.

FIGURE 21.

Single Read Transaction of 4 Data Words

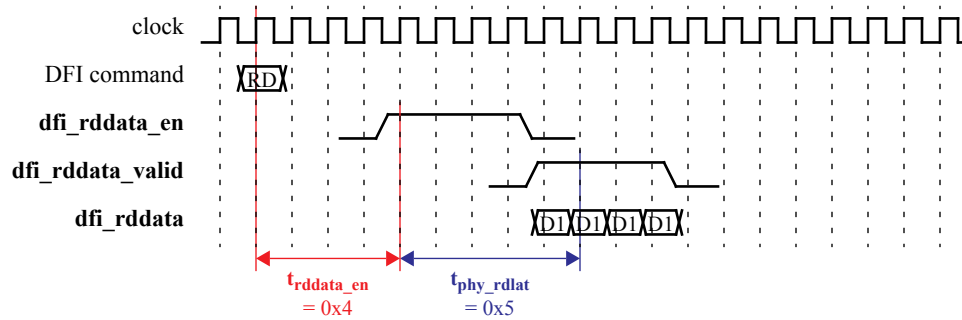


Figure 22 shows an interrupted read command. The **dfi\_rddata\_en** signal must be asserted for 4 cycles for each of these read transactions. However, since the first read is interrupted, the **dfi\_rddata\_en** signal is asserted for a portion of the first transaction and the complete second transaction. In this case, the **dfi\_rddata\_en** signal will not deassert between read commands.

FIGURE 22.

Back-to-Back Read Transactions with First Read Burst Interrupted (DDR1 Example BL=8)

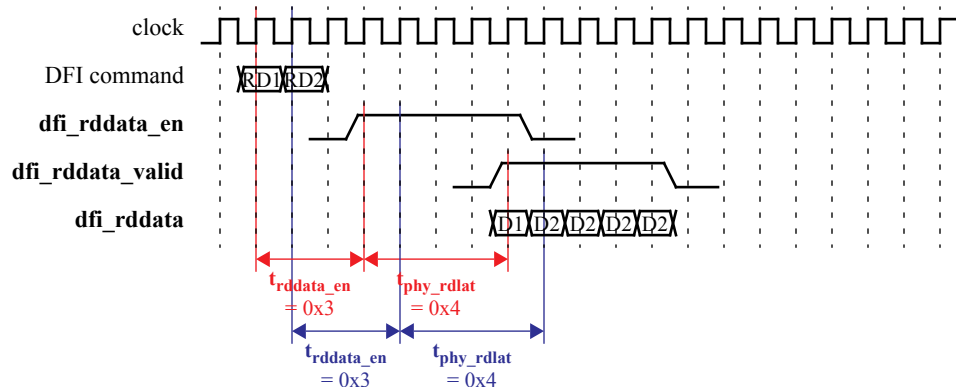
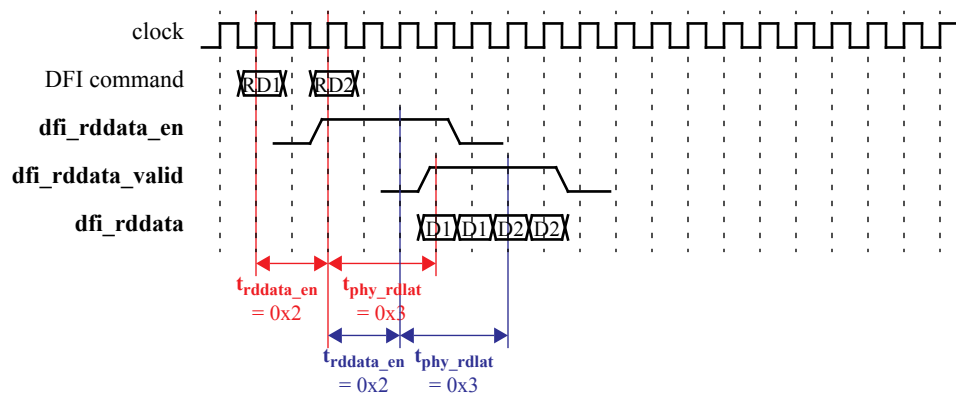


Figure 23 and Figure 24 also show two complete read transactions. The **dfi\_rddata\_en** signal is asserted for two cycles for each read transaction. In Figure 23, the values for the timing parameters are such that the read data is returned in a contiguous data stream for both transactions. Therefore, the **dfi\_rddata\_en** signal and the **dfi\_rddata\_valid** signal are each asserted for the complete read data stream.

FIGURE 23.

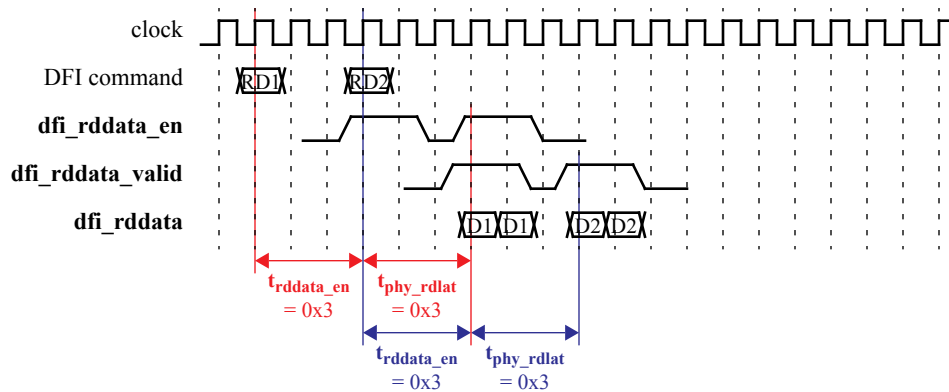
Two Independent Read Transactions (DDR1 Example)



In Figure 24, the  $t_{rddata\_en}$  timing and the timing between the read commands causes the **dfi\_rddata\_en** signal to be de-asserted between commands. As a result, the **dfi\_rddata\_valid** signal is de-asserted between commands and the **dfi\_rddata** stream is non-contiguous.

FIGURE 24.

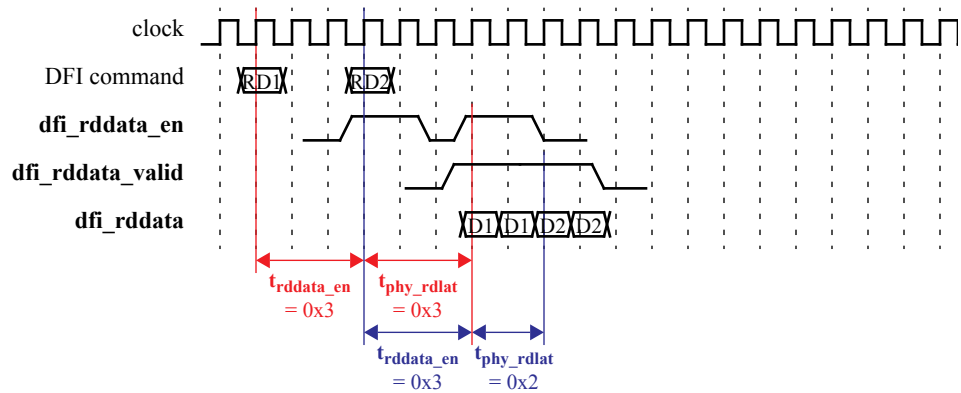
Two Independent Read Transactions (DDR2 Example)



In Figure 25, the effective  $t_{\text{phy\_rdlat}}$  for the two transactions is different. This results in a situation in which the **dfi\_rddata\_valid** signal remains asserted across commands and the **dfi\_rddata** stream is contiguous.

FIGURE 25.

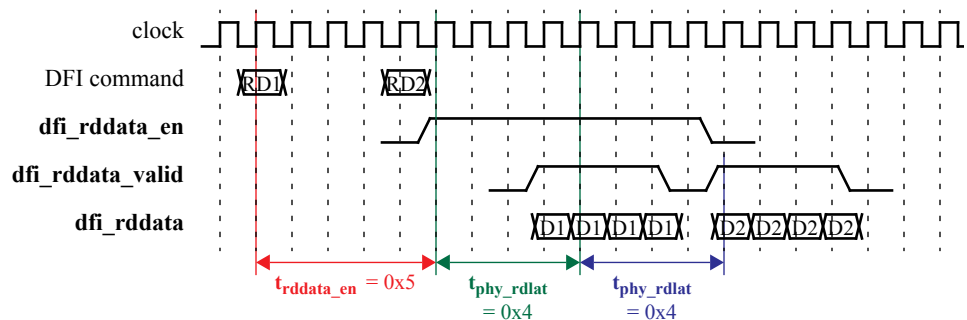
Two Independent Read Transactions (DDR2 Example)



The data may return to the DFI in fewer cycles than maximum delay. In Figure 26, the first read data transfer is returned in three cycles, even though the  $t_{\text{phy\_rdlat}}$  timing parameter is set to four cycles. The second read data transfer is returned in the maximum of four cycles.

FIGURE 26.

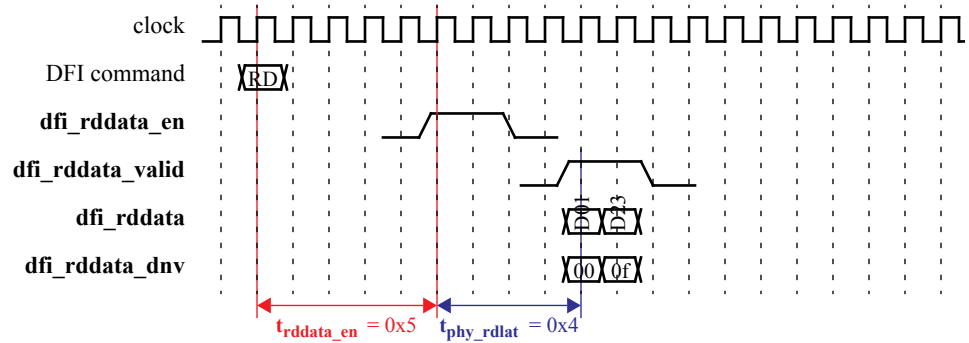
Two Independent Read Transactions (DDR3 Example)



LPDDR2 DRAMs define a new transaction type of mode register read (MRR). From the DFI perspective, a mode register read is handled like any other read command and utilizes the same signals. Figure 27 shows an MRR transaction for a LPDDR2 memory device.

FIGURE 27.

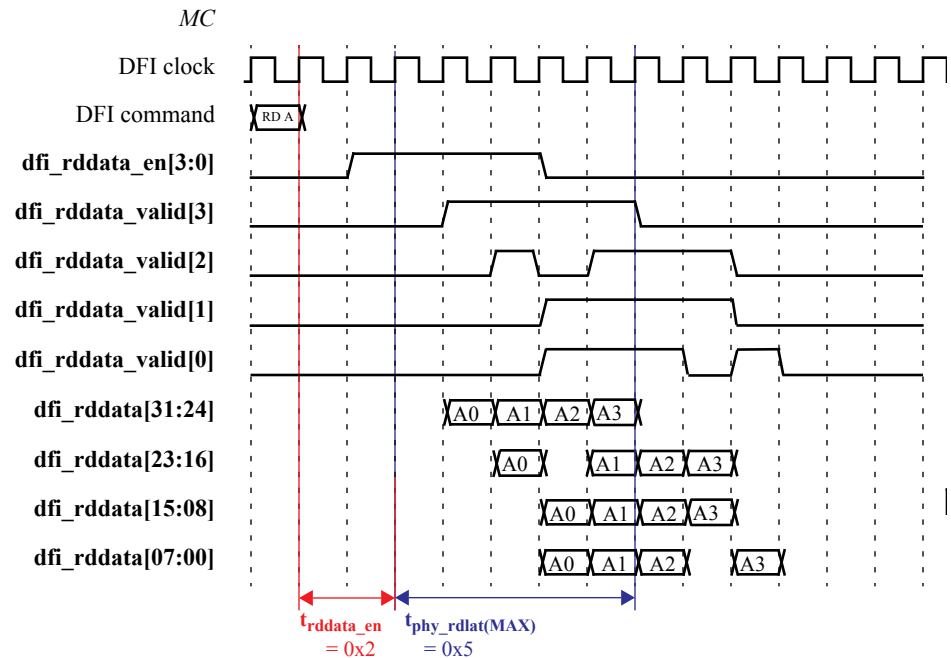
Example MRR Transactions with LPDDR2



In Figure 28, the **dfi\_rddata\_valid** signals are transferred independently. This figure shows a one-to-one correspondence between the data words for **dfi\_rddata\_en** and **dfi\_rddata\_valid**; the **dfi\_rddata\_valid** words do not need to be contiguous.

FIGURE 28.

DFI Read Data Transfer Illustrating **dfi\_rddata\_valid** Definition



**FIGURE 29.** *Read Commands Utilizing `dfi_rddata_cs_n`*



#### 4.5.2 DBI - Read

DBI is an optional DFI feature used with read data transmissions. The **phydbi\_mode** parameter is only needed when DBI is supported in DFI. If DBI is required in a system, DRAM DBI input must be received and used to selectively invert data for read commands.

For more information on the **phydbi\_mode** parameter, refer to Table 8, “Write Data Programmable Parameters,” on page 33.

#### 4.5.2.1 MC DBI Support (phy\_dbi\_mode==0)

The PHY captures the DRAM read DBI data and transmits the data over the DFI to the MC using the **dfi\_wrdata\_mask** and **dfi\_rddata\_dbi** signals. For more information on the DBI signals, refer to Table 6, “Write Data Signals,” on page 31 and Table 9, “Read Data Signals,” on page 35. The timing of the **dfi\_rddata\_dbi** signal is identical to the timing of the **dfi\_rddata** signal, and the DBI data is sent coincident with the corresponding **dfi\_rddata** bus.

For frequency ratio systems, the **dfi\_rddata\_dbi** signal is extended, similar to **dfi\_rddata**, with a signal defined per phase. For example, with a 4:1 frequency system, the DBI information is transmitted across the **dfi\_rddata\_dbi\_w0**, **dfi\_rddata\_dbi\_w1**, **dfi\_rddata\_dbi\_w2**, and **dfi\_rddata\_dbi\_w3** signals.

The timing of the phase outputs for DBI is identical to the **dfi\_rddata\_wN** outputs, with the data returned in a rolling order.

#### **4.5.2.2 PHY DBI Support ( $\text{phy\_dbi\_mode}==1$ )**

When the PHY generates the write DBI data, the **dfi\_rddata\_dbi** signal is not needed.

## **4.6 PHY Update**

The DFI contains signals to support MC-initiated and PHY-initiated update processes. The signals used in the update interface are: **dfi\_ctrlupd\_req**, **dfi\_ctrlupd\_ack**, **dfi\_phyupd\_req**, **dfi\_phyupd\_type** and **dfi\_phyupd\_ack**. The idle state timing parameters used in the update interface are:  $t_{\text{ctrl\_delay}}$  and  $t_{\text{wrdata\_delay}}$ .

For more information on the signals, refer to Section 3.4, “Update Interface,” on page 37. For more information on the idle state timing parameters, refer to Table 5, “Control Timing Parameters,” on page 28 and Table 7, “Write Data Timing Parameters,” on page 32.

### **4.6.1 MC-Initiated Update**

During normal operation, the MC may encounter idle time during which no commands are issued to the DRAMs and all outstanding read and write data have been transferred on the DFI bus and the write data transfer has completed on the memory bus. Assertion of the **dfi\_ctrlupd\_req** signal indicates the control, read and write interfaces on the DFI are idle. While the **dfi\_ctrlupd\_ack** signal is asserted, the DFI bus may only be used for commands related to the update process.

The MC guarantees that **dfi\_ctrlupd\_req** signal is asserted for at least  $t_{\text{ctrlupd\_min}}$  cycles, allowing the PHY time to respond. The PHY may respond to or ignore the update request. To acknowledge the request, the **dfi\_ctrlupd\_ack** signal must be asserted while the **dfi\_ctrlupd\_req** signal is asserted. The **dfi\_ctrlupd\_ack** signal must de-assert at least one cycle before  $t_{\text{ctrlupd\_max}}$  expires.

The MC must hold the **dfi\_ctrlupd\_req** signal as long as the **dfi\_ctrlupd\_ack** signal is asserted, and must de-assert the **dfi\_ctrlupd\_req** signal before  $t_{\text{ctrlupd\_max}}$  expires.

Figure 30, “MC-Initiated Update Timing Diagram” shows that the DFI does not specify the number of cycles after the **dfi\_ctrlupd\_ack** signal de-asserts before the **dfi\_ctrlupd\_req** signal de-asserts.

FIGURE 30.

MC-Initiated Update Timing Diagram

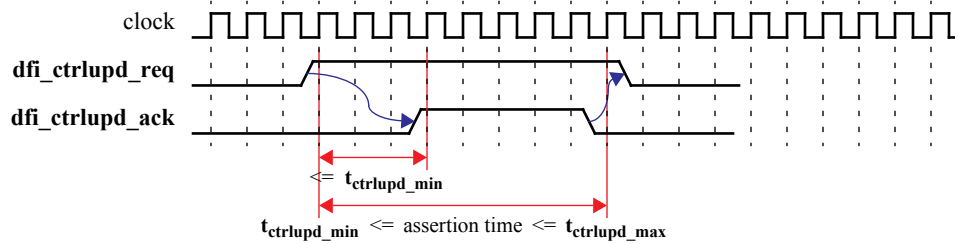
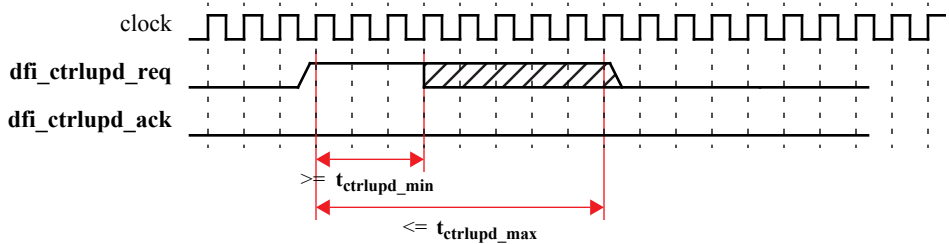


Figure 31, “MC-Initiated Update with No Response” shows the important point that the **dfi\_ctrlupd\_ack** signal is not required to assert when the **dfi\_ctrlupd\_req** signal is asserted. The MC must assert the **dfi\_ctrlupd\_req** signal for at least  $t_{ctrlupd\_min}$  within every  $t_{ctrlupd\_interval}$  cycle, but the total number of cycles that the **dfi\_ctrlupd\_req** signal is asserted must not exceed  $t_{ctrlupd\_max}$ .

FIGURE 31.

MC-Initiated Update with No Response



#### 4.6.2 PHY-Initiated Update

The PHY may also trigger the DFI to enter an idle state. This update process utilizes three signals: **dfi\_phyupd\_req**, **dfi\_phyupd\_type** and **dfi\_phyupd\_ack**. The **dfi\_phyupd\_req** signal indicates the need for idle time on the DFI, the **dfi\_phyupd\_type** signal defines the type of update required, and the **dfi\_phyupd\_ack** signal is the MC’s response signal. Four update types are specified by the DFI.

To request an update, the **dfi\_phyupd\_type** signal must be valid when the **dfi\_phyupd\_req** signal is asserted. The  $t_{phyupd\_typeX}$  parameters indicate the number of cycles of idle time on the DFI control, read and write data interfaces being requested. The **dfi\_phyupd\_ack** signal must assert within  $t_{phyupd\_resp}$  cycles after the assertion of the **dfi\_phyupd\_req** signal.

When the **dfi\_phyupd\_ack** signal is asserted, it must remain asserted until the **dfi\_phyupd\_req** signal de-asserts or until  $t_{phyupd\_typeX}$  cycles have expired. The **dfi\_phyupd\_ack** signal must de-assert following the detection of the **dfi\_phyupd\_req** signal de-assertion. The **dfi\_phyupd\_ack** signal for the previous transaction must be

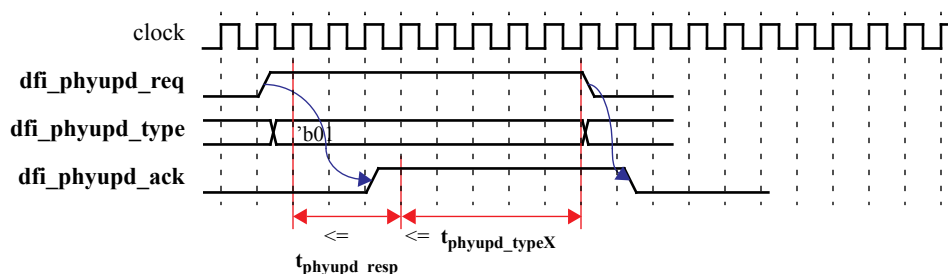


de-asserted before the **dfi\_phyupd\_req** signal can assert. While the **dfi\_phyupd\_ack** signal is asserted, the DFI bus may only be used for commands related to the update process.

Figure 32, “PHY-Initiated Update Timing Diagram” shows that the MC must respond to a PHY update request, unlike MC-initiated updates shown in Figure 30, “MC-Initiated Update Timing Diagram” and Figure 31, “MC-Initiated Update with No Response”.

**FIGURE 32.**

*PHY-Initiated Update Timing Diagram*



### 4.6.3 DFI Idle

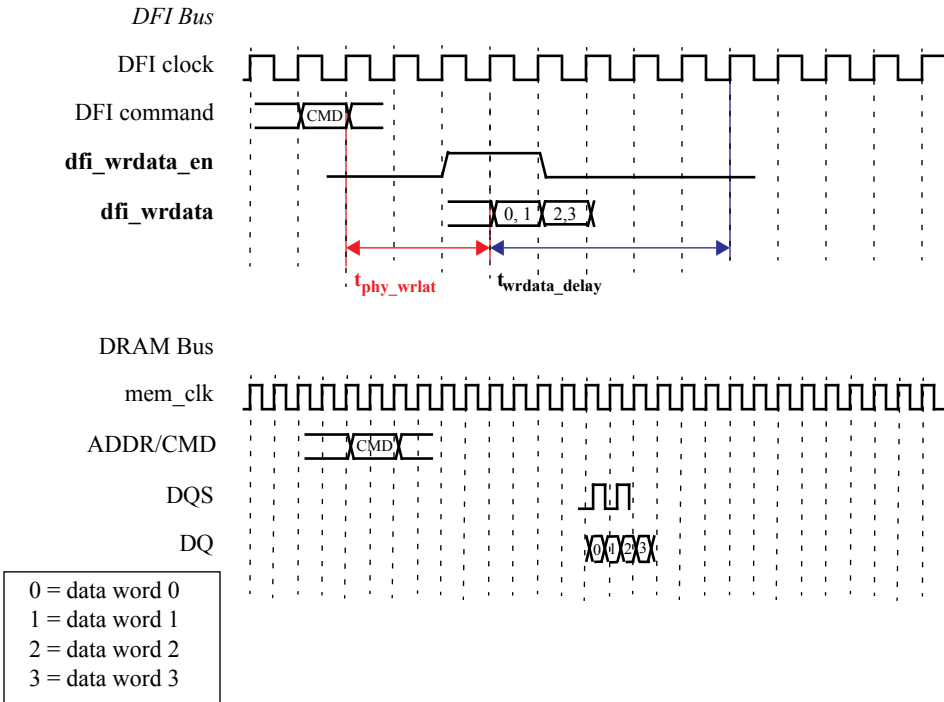
To prevent the condition where a PHY may disrupt the write data transfer on the memory bus, the write data transfer on the memory bus must complete before the DFI idle state is reached.

The  $t_{\text{wrdata\_delay}}$  idle state timing parameter defines the number of DFI clocks from **dfi\_wrdata\_en** to the completion of the write data transfer on the memory bus. Since the requirement for an idle bus state following a write is generally an infrequent event relative to the overall traffic pattern, the accuracy of the setting should not be a performance issue, so it may be set to a larger value.

If a PHY has no dependency between completing a write data transfer on the DFI bus and the idle state, the  $t_{\text{wrdata\_delay}}$  parameter can be set to zero.

When a PHY does have a dependency between completing a write data transfer on the DFI bus and the idle state, the  $t_{\text{wrdata\_delay}}$  parameter should be set to a sufficiently large value to accommodate the write data width, flight time through the PHY, and worst-case timing on the memory bus.

FIGURE 33.

Bus Idle State Timing Parameter -  $t_{\text{wrdata\_delay}}$ 

## 4.7 DFI Clock Disabling

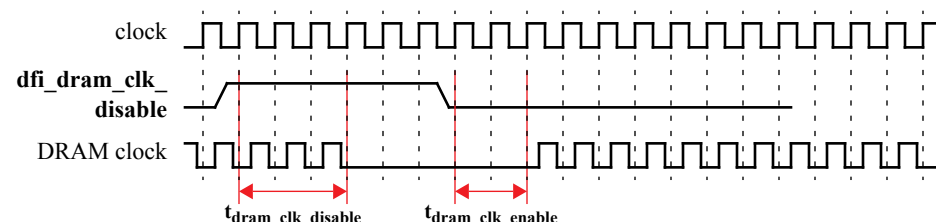
The DFI contains a **dfi\_dram\_clk\_disable** signal which controls the DRAM clock signal to the DRAM device(s). In the default state, the DRAM clock functions normally and the **dfi\_dram\_clk\_disable** bits are all de-asserted. If the system requires the clocks of the memory device(s) to be disabled, then the **dfi\_dram\_clk\_disable** signal is asserted. For more information on the **dfi\_dram\_clk\_disable** signal, refer to Section 3.5, “Status Interface,” on page 41.

Figure 34, “DRAM Clock Disable Behavior” shows that two timing parameters  $t_{\text{dram\_clk\_disable}}$  and  $t_{\text{dram\_clk\_enable}}$  indicate the number of DFI cycles that the PHY requires to respond to the assertion and de-assertion of the **dfi\_dram\_clk\_disable** signal. The  $t_{\text{dram\_clk\_disable}}$  value determines the number of DFI cycles in which a rising edge of the **dfi\_dram\_clk\_disable** signal affects the DRAM clock and

**t<sub>dram\_clk\_enable</sub>** sets the number of cycles required for the DRAM clock to be active again.

**FIGURE 34.**

*DRAM Clock Disable Behavior*



## 4.8 Frequency Ratios Across the DFI

In a DDR memory subsystem, it may be advantageous to operate the PHY at a higher frequency than the MC. If the PHY operates at a multiple of the MC frequency, the PHY transfers data at a higher data rate relative to the DFI clock and the MC has the option to execute multiple commands in a single DFI clock cycle. The DFI is defined at the MC to PHY boundary and therefore operates in the clock frequency domain of the MC.

The MC clock is always the DFI clock and all DFI signals are referenced from the MC clock.

The DFI specification supports a 1:2 or 1:4 MC to PHY frequency ratio, defining the relationship of the reference clocks for the MC and the PHY. The DFI DDR PHY clock is always the same frequency as the DRAM clock, which is 1/2 the data rate for the memory.

DFI signals may be sent or received on the PHY clock, provided the signals reference the rising edge of the DFI clock and the clock is phase aligned. The MC communicates frequency ratio settings to the PHY on the **dfi\_freq\_ratio** signal. This signal is only required for devices using this frequency ratio protocol.

For more information on the frequency ratio clock, refer to Section 4.8.1, “Frequency Ratio Clock Definition,” on page 92.

The frequency ratio protocol affects the write data and read data interfaces, including read data rotation and resynchronization.

For information on how the write data and read data interfaces are affected, refer to Section 4.8.2, “Interface Signals with Frequency Ratio Systems,” on page 92, Section 4.8.3, “Write Data Interface in Frequency Ratio Systems,” on page 96, Section 4.8.4, “Read Data Interface in Frequency Ratio Systems,” on page 98, Section 4.8.4.1, “DFI Read Data Rotation,” on page 105, and Section 4.8.4.1.1, “Read Data Resynchronization,” on page 109.

Frequency ratio also affects CA and CRC parity errors.

For information on how frequency ratio affects CA and CRC parity errors, refer to Section 4.10.2.1, “CA and CRC Parity Errors in Frequency Ratio Systems,” on page 113.

#### 4.8.1 Frequency Ratio Clock Definition

The DFI clock and the DFI PHY clock must be phase-aligned and at a 1:2 or 1:4 frequency ratio relative to one another. Some DFI signals from the MC to the PHY must communicate information about the signal in reference to the DFI PHY clock to maintain the correct timing information. Therefore, the DFI PHY clock is described in terms of phases, where the number of clock phases for a system is the ratio of the DFI PHY clock to the DFI clock.

Figure 35, “Frequency Ratio 1:2 Phase Definition” and Figure 36, “Frequency Ratio 1:4 Phase Definition” show the clock phase definitions for 1:2 and 1:4 frequency ratio systems.

FIGURE 35.

*Frequency Ratio 1:2 Phase Definition*

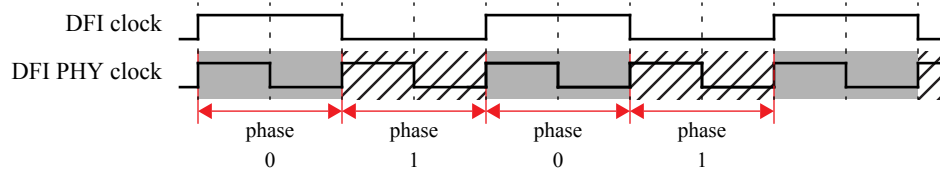
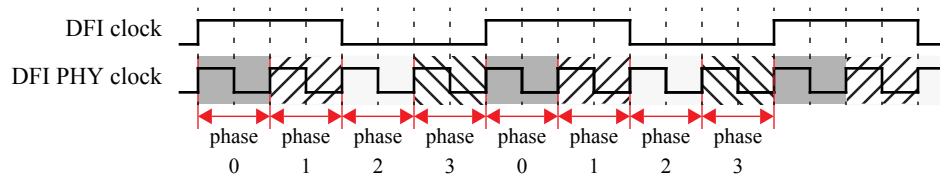


FIGURE 36.

*Frequency Ratio 1:4 Phase Definition*



#### 4.8.2 Interface Signals with Frequency Ratio Systems

Write data and read data signals are defined on a per-phase basis and all signal timing is in reference to the DFI clock. The PHY must account for any assertions based on the DFI clock. Any signals driven by the PHY must only change during phase 0 of the DFI PHY clock to allow the MC the full DFI clock to capture the signal change.

The DFI specification supports the ability to send a unique command on each phase of the DFI PHY clock. To communicate this information to the PHY, the DFI specification defines commands for a frequency ratio system in a vectored format. The PHY must maintain this information to preserve the timing relationships between commands and data. Therefore, for frequency ratio systems, the control signal interface, the write data interface and the read data enable signal are all suffixed with a “\_pN” where N is the phase number.

For a 1:2 frequency ratio system, instead of a single **dfi\_address** signal, there are 2 signals: **dfi\_address\_p0** and **dfi\_address\_p1**. The read data signal, read data valid and read data not valid signals are suffixed with a “\_wN” where N is the DFI data word.

More information on the read data interface for frequency ratio systems is provided in Section 4.8.4, “Read Data Interface in Frequency Ratio Systems”. The phase 0 or DFI data word 0 suffixes are not required.

There is flexibility in system setup for frequency ratio systems. The MC may be implemented to support command output on a single phase or on multiple phases. Even if multiple phases are supported, the MC is not required to implement or drive every phase of a signal. Only phases where a command is sent must be implemented and driven. The exceptions to the rule are the **dfi\_cke\_pN** and **dfi\_odt\_pN** signals. These two signals are not necessarily driven in the same phase as the rest of the command. Therefore, these signals must be implemented for all phases of the clock to allow flexibility in timing.

The PHY must be able to accept a command on all phases to be DFI compliant. If the MC is only using certain phases, the PHY must be appropriately connected to properly interpret the command stream.

There is no requirement that signals must be implemented in the same way across the interfaces. For example, in a 2T implementation, the **dfi\_ras\_n\_pN**, **dfi\_cas\_n\_pN** and **dfi\_we\_n\_pN** signals may be driven by the MC on all clock phases, but the **dfi\_cs\_n\_pN** signal may only be driven by the MC on half of the phases.

Figure 37, “Example 1:2 Frequency Ratio Command Stream” illustrates a command stream for a 1:2 frequency ratio system and shows how the PHY in this system would interpret the DFI signals. In this example, a command is only sent on phase 0; the values of phase 0 and phase 1 commands are different. ODT information is provided on both

phases. PHY timing is shown for illustrative purposes only. The command bus signals are not always the same value and are not always equal to one.

FIGURE 37.

Example 1:2 Frequency Ratio Command Stream

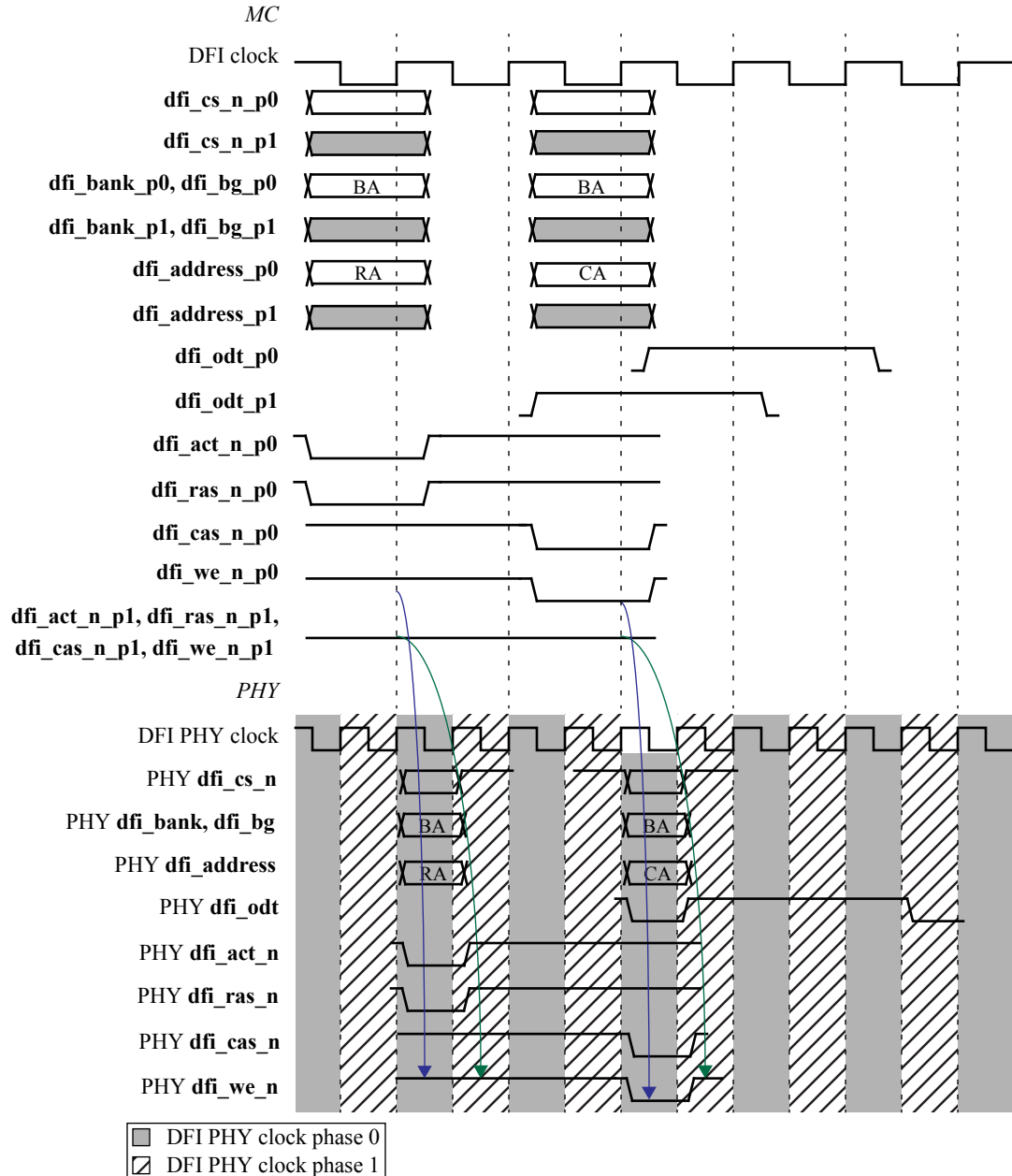
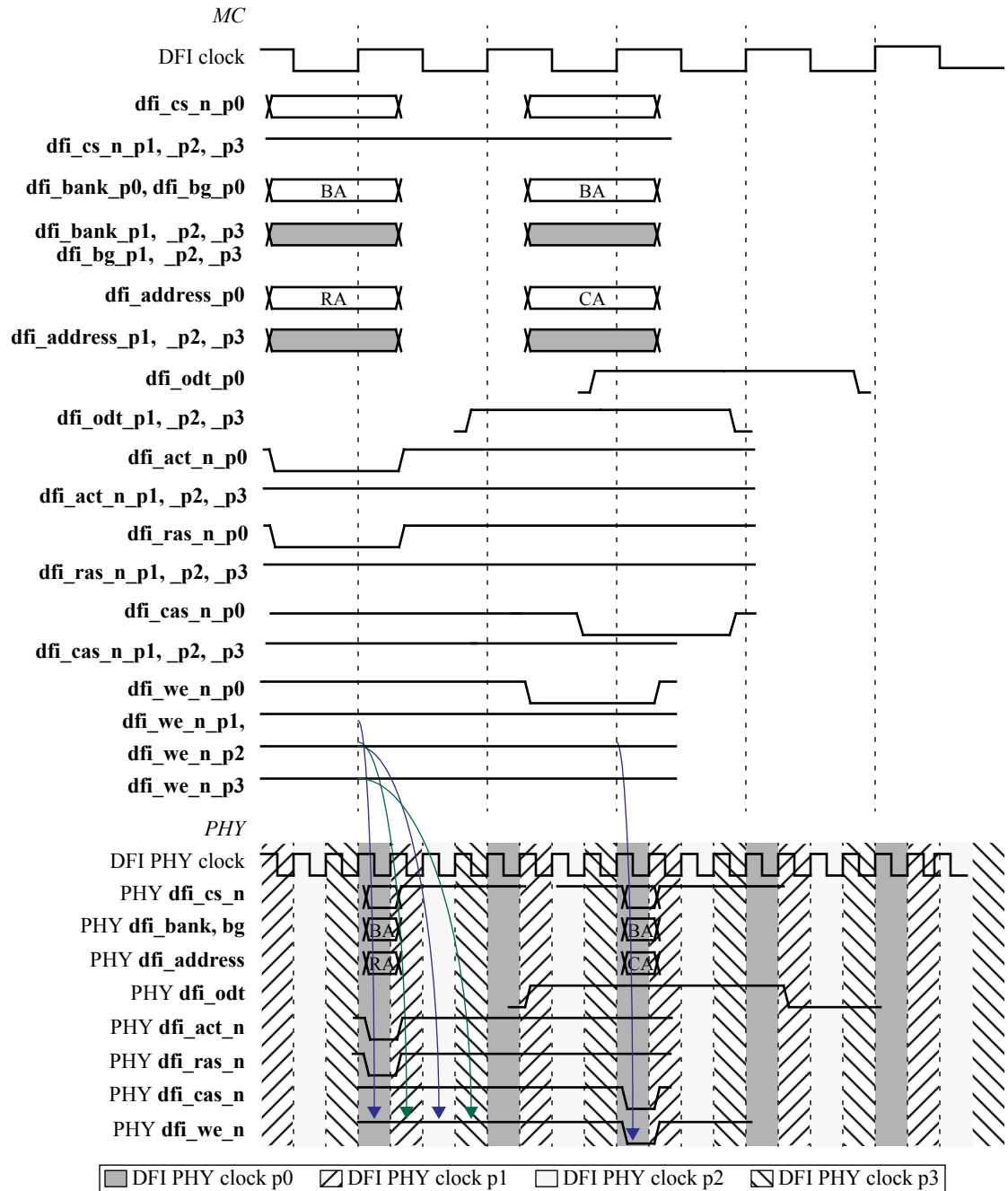


Figure 38, “Example 1:4 Frequency Ratio Command Stream” represents the same example, in a 1:4 frequency ratio system. The command is only sent on phase 0 and

ODT information is provided on all phases. PHY timing is shown for illustrative purposes only.

FIGURE 38.

Example 1:4 Frequency Ratio Command Stream

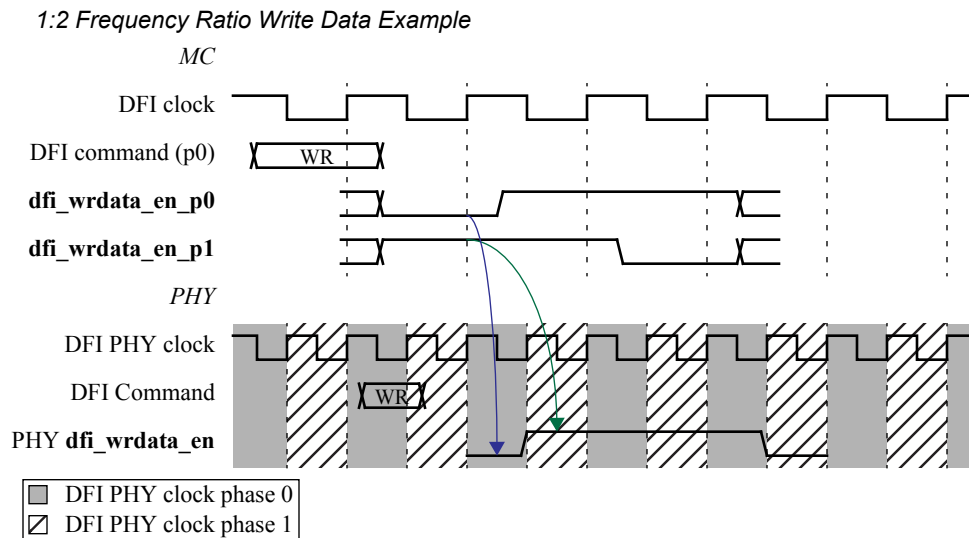


### 4.8.3 Write Data Interface in Frequency Ratio Systems

The write data enable signal (**dfi\_wrddata\_en\_pN**) indicates to the PHY that valid **dfi\_wrddata** will be transmitted in  $t_{\text{phy\_wrddata}}$  cycles. and its width defines the number of data phases of the write. In order to communicate this information to the PHY, the phase information must be encoded within the signal. Therefore, this signal is also vectored into multiple signals based on the frequency ratio. Similar to the DFI command, each signal is associated with a phase of the DFI PHY clock.

Figure 39 demonstrates how a vectored **dfi\_wrddata\_en\_pN** signal is interpreted by the PHY in a 1:2 frequency ratio system. PHY timing is shown for illustrative purposes only.

FIGURE 39.



For matched frequency systems, the DFI write data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, this DFI write data bus width is proportional to the frequency ratio to allow all of the write data that the memory requires to be sent in a single DFI clock cycle. The write data must be delivered with the DFI data words aligned in ascending order.

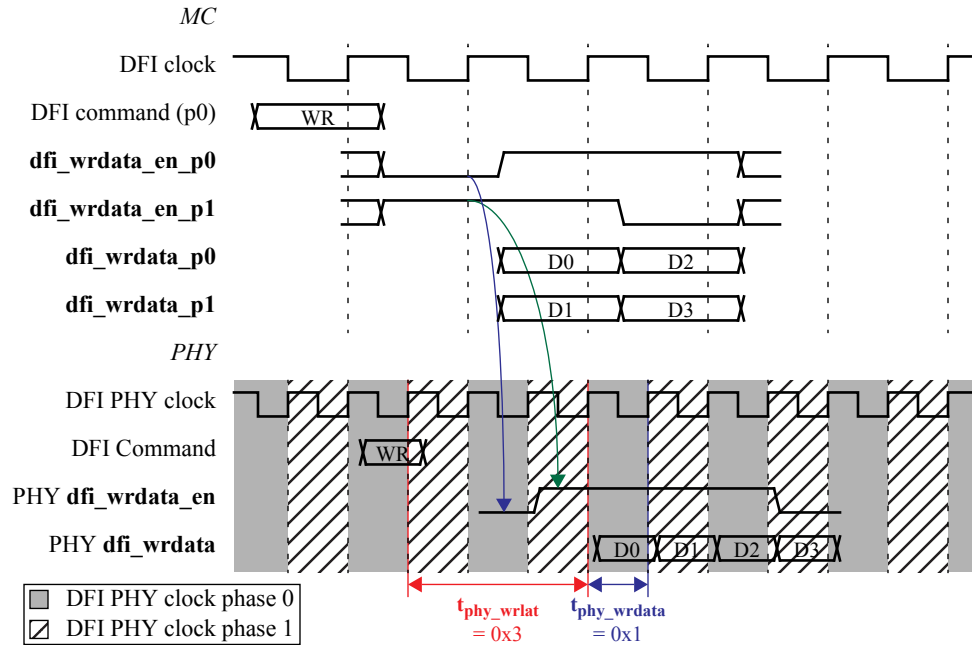
The timing parameters  $t_{\text{phy\_wrlat}}$  and  $t_{\text{phy\_wrddata}}$  apply in frequency ratio systems in the same way as in matched frequency systems. The  $t_{\text{phy\_wrlat}}$  parameter defines the delay from the write command to the **dfi\_wrddata\_en\_pN** signal. The  $t_{\text{phy\_wrddata}}$  parameter defines the delay from the **dfi\_wrddata\_en\_pN** signal to when data is driven on the **dfi\_wrddata\_pN** signal. These timing parameters are defined in terms of DFI PHY clocks and are measured relative to how the PHY interprets the data.



Figure 40 shows how data is received by the PHY in a situation where the data is sent aligned, but the enable signals are not aligned.

FIGURE 40.

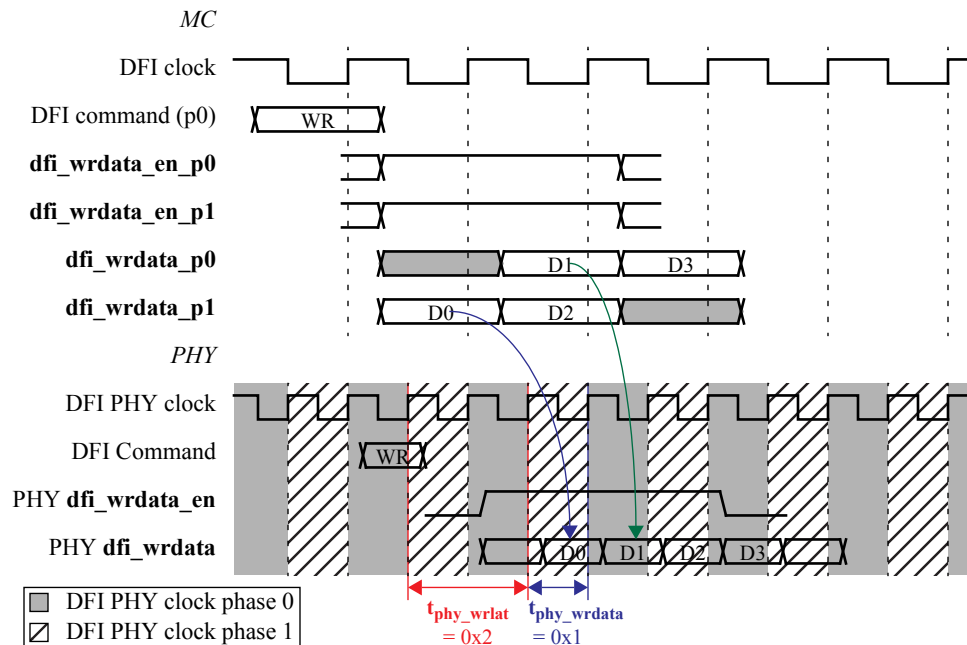
1:2 Frequency Ratio Aligned Write Data Example



In Figure 41, the enable signals are sent aligned, but the data is not aligned. The MC sends the first beat of data on the phase 1 data signal. The write data must be sent unaligned to achieve the proper relationship between the command and data.

FIGURE 41.

1:2 Frequency Ratio Aligned Write Enable Example



#### 4.8.4 Read Data Interface in Frequency Ratio Systems

Similar to the write data enable signal, the read data enable signal (**dfi\_rddata\_en\_pN**) defines the number of clocks between the read command and the read data, and its width defines the number of data phases of the read. The PHY sends read data to the MC on the **dfi\_rddata\_wN** buses whenever read data is available, asserting the associated **dfi\_rddata\_valid\_wN** signals to inform the MC which buses contain valid data. Unlike the read data enable signal which correlates to the phase of the DFI PHY clock, the read data, read data valid and read data not valid signals are all vectored with the DFI data word suffix.

For a 1:2 frequency ratio system, the read data bus is divided into 2 DFI read data words. For a 1:4 frequency ratio system, the read data bus is divided into 4 DFI read data words. Each DFI data word transfers a memory data word, the data associated with one rising and falling DQS. For example, in a 1:4 system with a memory data width of 32 bits, the DFI read data bus would consist of 4 64-bit DFI data words.

On a DFI clock, the PHY is permitted to assert any number of consecutive **dfi\_rddata\_valid\_wN** signals that correspond to valid read data. However, the read data must be returned in a rolling order of DFI data words. For a 1:4 frequency ratio system, if read data is returned on the **dfi\_rddata\_w0** and **dfi\_rddata\_w1** buses on one

DFI clock cycle, the next transaction must return data starting on the **dfi\_rddata\_w2** bus, regardless of the number of DFI data words being returned. If that next transaction returned 2 DFI data words, data must be returned on the **dfi\_rddata\_w2** and **dfi\_rddata\_w3** buses. If that next transaction returned 4 DFI data words, data must be returned on the **dfi\_rddata\_w2**, **dfi\_rddata\_w3**, **dfi\_rddata\_w0** and **dfi\_rddata\_w1** buses - in that order.

For a 1:2 frequency ratio system, read data must be returned in the same manner, in a rolling order of DFI data words. In this case, there are only 2 DFI data words in the DFI read data bus - **dfi\_rddata\_w0** and **dfi\_rddata\_w1**.

The rolling order rule must be followed regardless of whether the subsequent data transfer occurs on the next DFI clock or several clocks later. For LPDDR2 memory systems, the rolling order rule applies to both reads and mode register reads. The order is critical for the PHY and MC to correctly communicate read data. Each DFI data word must be used prior to sending data on the subsequent DFI data word, requiring data to be sent contiguously. The subsequent read data must be returned on the next DFI data word relative to the previous transaction. If the last transaction ended on **dfi\_rddata\_w2**, for example, the next transfer must begin on **dfi\_rddata\_w3**. Similarly, it is not legal to return read data on only the **dfi\_rddata\_w0** and **dfi\_rddata\_w2** buses.

Both the MC and the PHY must track which signals were used in the last transfer in order to interpret the data accurately. At initialization, the DFI data word pointer is set to 0, and the first read data returned is expected on the **dfi\_rddata\_w0** bus. During normal operation, certain procedures may affect the read data rotation, such as frequency changing, data training or gate training. Therefore, any assertion of the **dfi\_init\_start** signal, or a de-assertion of the **dfi\_rdlvl\_en** or **dfi\_rdlvl\_gate\_en** signals must trigger a re-initialization of the DFI data word pointer to 0.

The rotational use of the **dfi\_rddata\_valid\_wN** signals is only required in situations where the system may return less data than the DFI read data bus. If the minimum transfer size is a multiple of the DFI read data bus width, data can always be returned on all DFI data words and the **dfi\_rddata\_valid\_wN** signals are all driven identically. Otherwise, only certain DFI data words of the DFI read data bus are used. In either case, the MC must be able to receive data in a rotating order based on the last transfer to be DFI compliant for frequency ratio. A PHY may optionally be implemented such that it always returns read data on the entire DFI read data bus per transaction.

Regardless of how the signals are vectored, the PHY may only change read data, read data valid and read data not valid signals during phase 0 of the DFI PHY clock to allow the MC the entire DFI clock period to capture the signal and read data.

The timing parameters **t<sub>rddata\_en</sub>** and **t<sub>phy\_rdlat</sub>** apply in frequency ratio systems in the same way as in matched frequency systems. These timing parameters define the delay from the read command to the **dfi\_rddata\_en\_pN** signal, and from the **dfi\_rddata\_en\_pN** signal to when data is returned on the **dfi\_rddata\_wN** bus, respectively. These timing parameters are defined in terms of DFI PHY clocks and are measured relative to how the PHY interprets the data.

Figure 42 demonstrates how a vectored **dfi\_rddata\_en\_pN** signal is interpreted by the PHY in a 1:2 frequency ratio system with an even value for the **t<sub>rddata\_en</sub>** timing parameter, and where all DFI data words are returned on a DFI clock cycle. PHY timing is shown for illustrative purposes only.

**FIGURE 42.**

*1:2 Frequency Ratio Single Read Data Example with Even Read Data to Enable Timing*

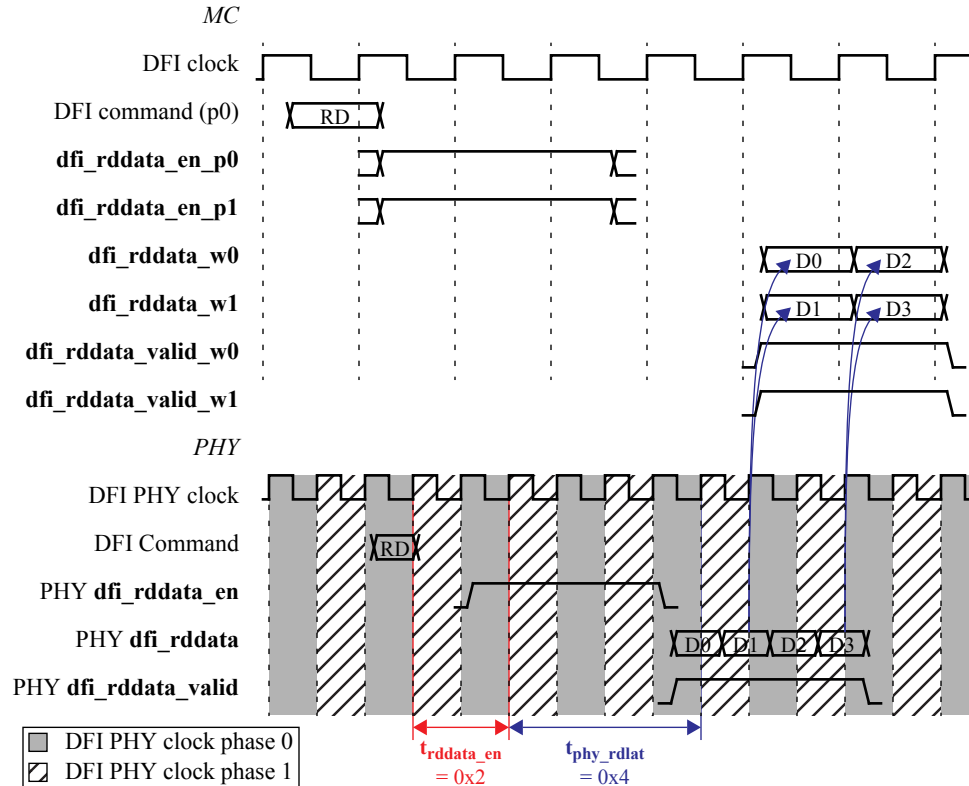


Figure 43 demonstrates how a vectored **dfi\_rddata\_en\_pN** signal is interpreted by the PHY in a 1:2 frequency ratio system with an odd value for the **t<sub>rddata\_en</sub>** timing

parameter, and where all DFI data words are returned on a DFI clock cycle. PHY timing is shown for illustrative purposes only.

**FIGURE 43.** 1:2 Frequency Ratio Single Read Data Example with Odd Read Data to Enable Timing

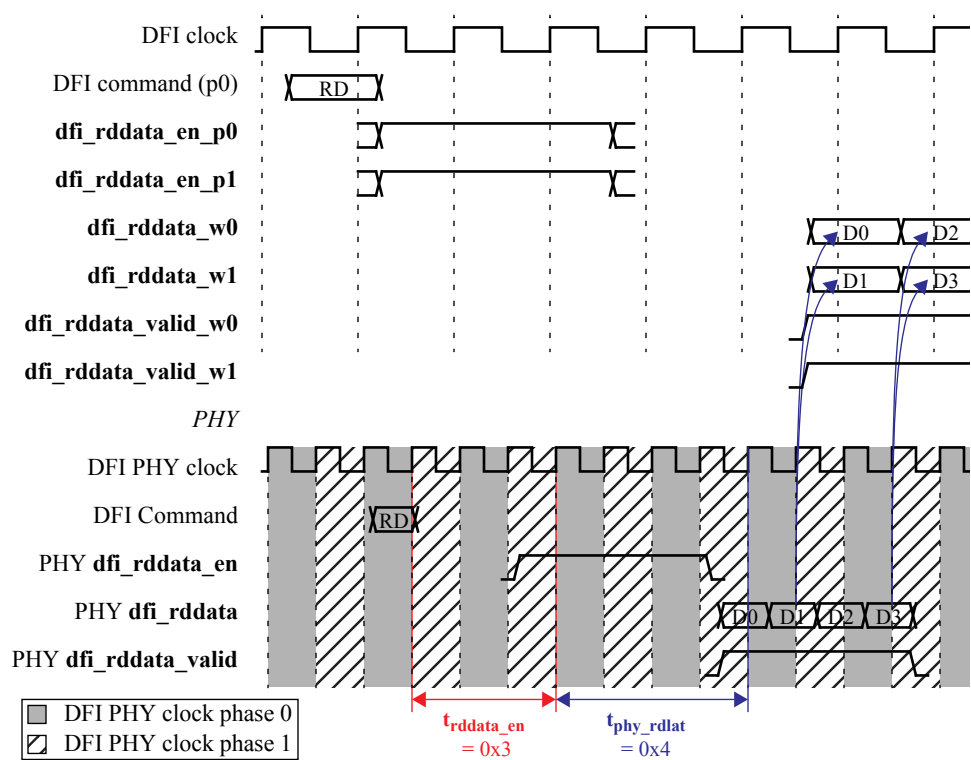


Figure 44 demonstrates how a vectored **dfi\_rddata\_en\_pN** signal is interpreted by the PHY in a 1:4 frequency ratio system where all DFI data words are being returned on a DFI clock cycle. PHY timing is shown for illustrative purposes only.

FIGURE 44.

1:4 Frequency Ratio Single Read Data Example

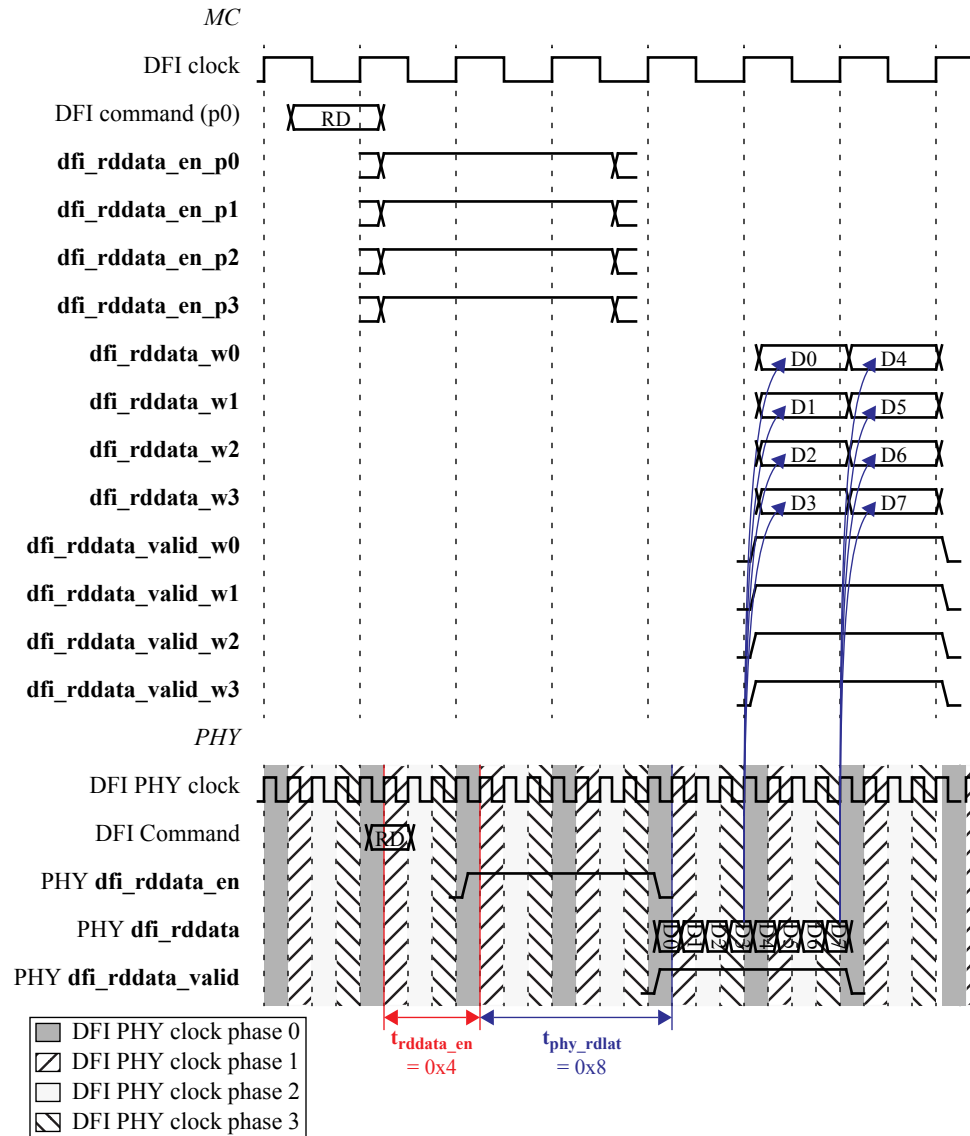
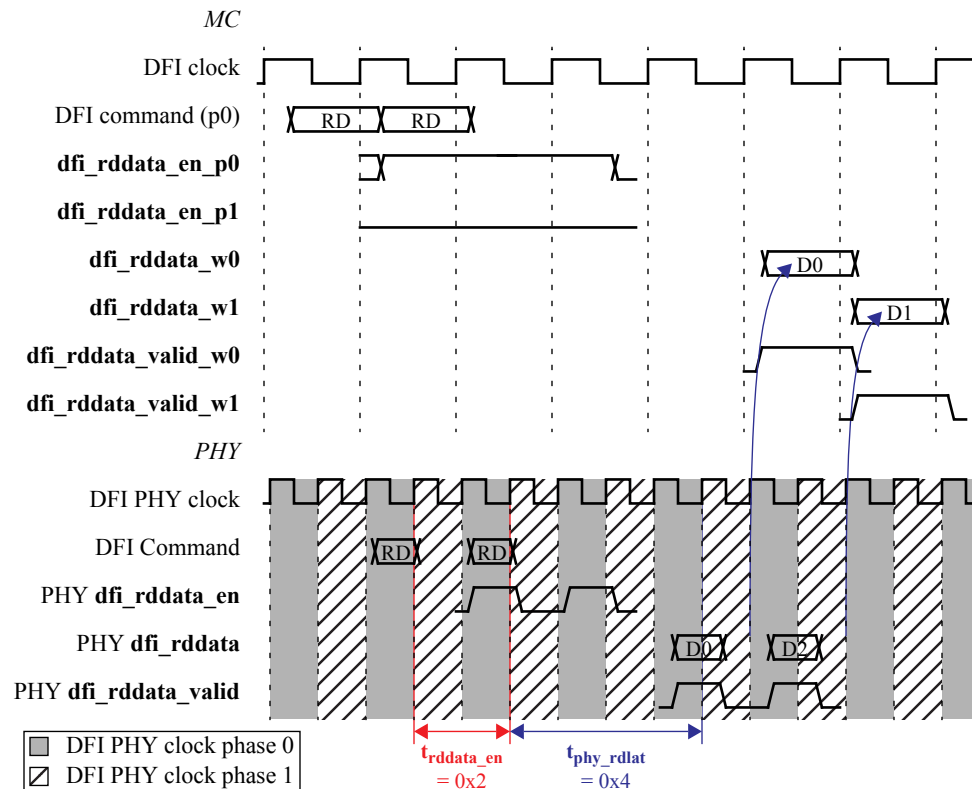


Figure 45 returns a single DFI data word with each command. The data for the second read command is returned on the **dfi\_rddata\_w1** bus following the rotational order rule. PHY timing is shown for illustrative purposes only.

FIGURE 45.

1:2 Frequency Ratio Multiple Read Data Example

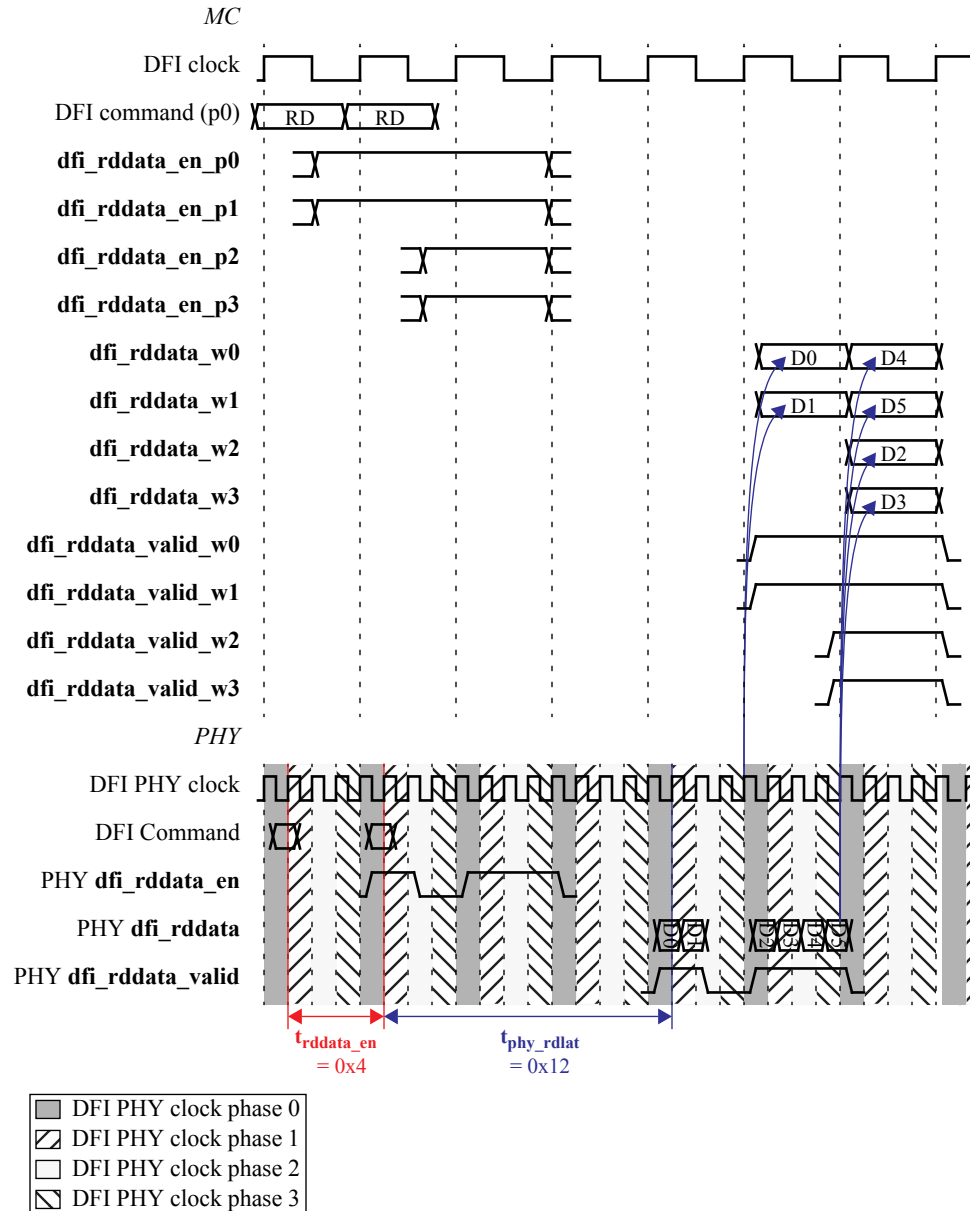


Similar to Figure 45, “1:2 Frequency Ratio Multiple Read Data Example”, Figure 46 shows a burst length 4 followed by a burst length 8 read. The data for the burst length 8

read command is returned starting on the **dfi\_rddata\_w2** bus following the rotational order rule. PHY timing is shown for illustrative purposes only.

FIGURE 46.

1:4 Frequency Ratio Multiple Read Data Example



For matched frequency systems, the DFI read data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, this DFI read data bus width is proportional to the frequency ratio to allow all of the read data that the memory



returns to be sent in a single DFI clock cycle. The read data must be delivered with the DFI data words aligned in ascending order.

#### **4.8.4.1 DFI Read Data Rotation**

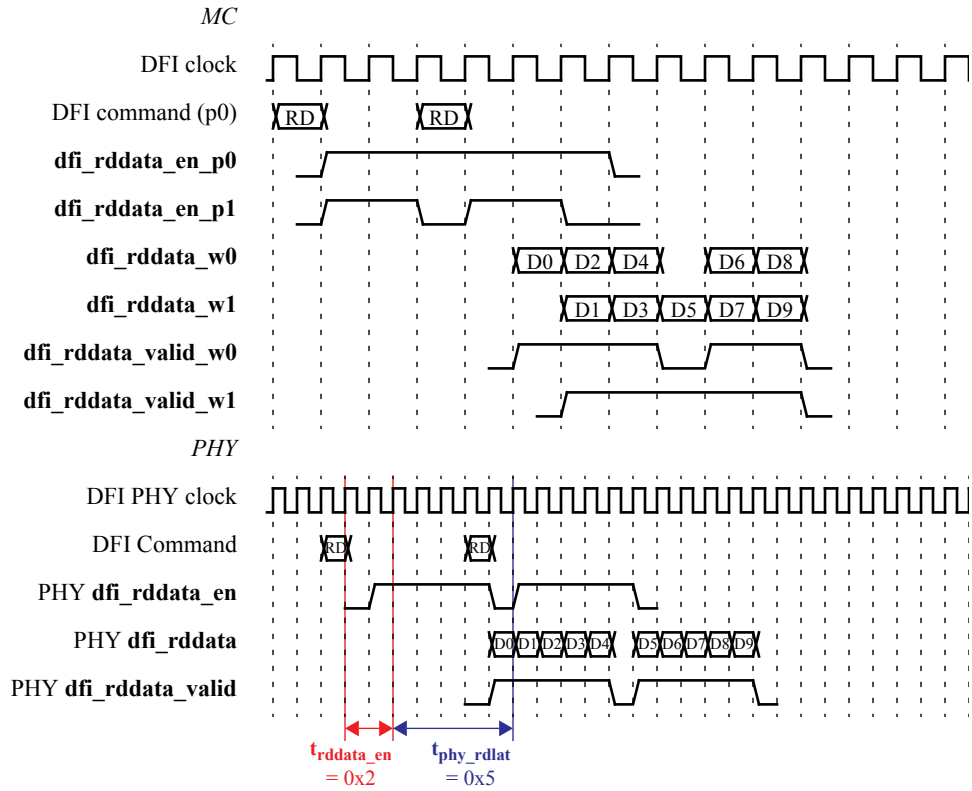
In a frequency ratio system, if a read transfer is not always an even multiple of the **dfi\_rddata** bus, the system must properly adhere to the read data rotation order. The read data is returned on the appropriate **dfi\_rddata\_wN** bus and this data must be returned in a rolling order of DFI data words. For a 1:2 frequency ratio system, if read data is returned on the **dfi\_rddata\_w0** on one DFI clock cycle, the next transaction must return data starting on the **dfi\_rddata\_w1** bus, regardless of the number of DFI data words being returned. This ordering rule must be followed regardless of whether the subsequent data transfer occurs on the next DFI clock or several clocks later.

In some cases, the number of read data words in a burst may not be equal to a multiple of the frequency ratio. For example, with a 4:1 frequency system, a burst of 4 DRAM words of data is transferred on 2 DFI data words. The next access, consequently, could start on **dfi\_rddata\_w2** instead of **dfi\_rddata\_w0**.

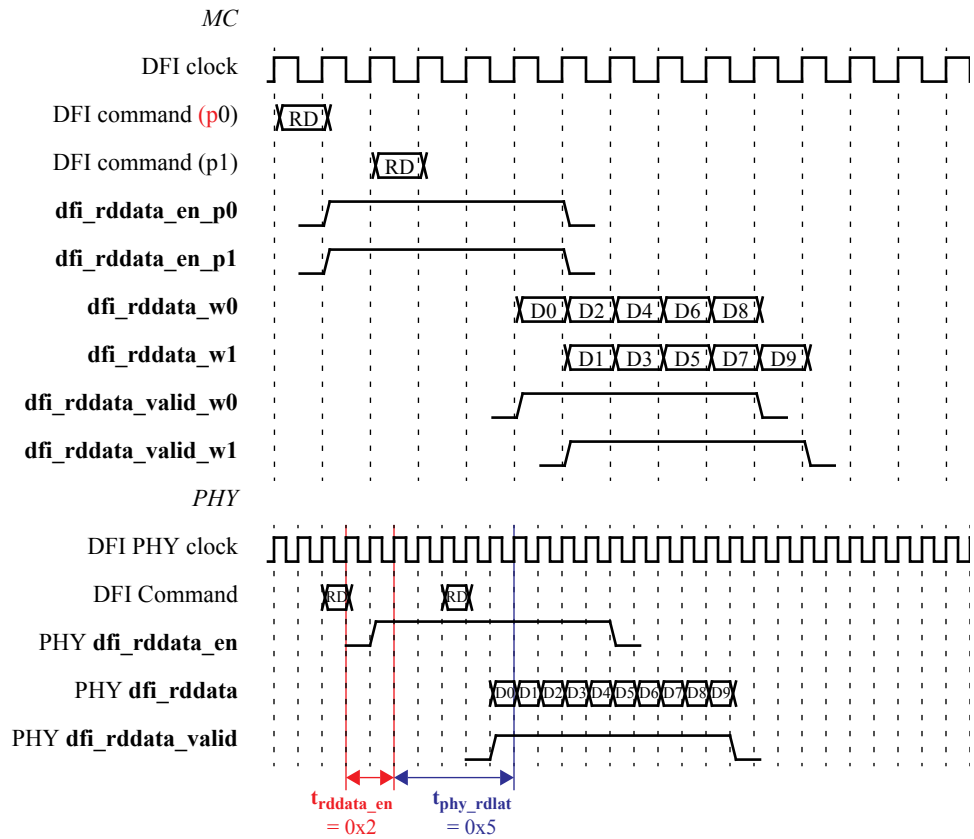
For simplicity, the following four diagrams illustrate different potential timing scenarios with a 1:2 frequency ratio system, transmitting 2 bursts of data, with each burst extended by one DRAM clock cycle. Figure 4.6, “PHY Update” illustrates requirements of the PHY and controller when the number of DFI data words returned is not a multiple of the frequency ratio.

Many DFI systems do not require support for burst transfers that are not a multiple of the frequency ratio. However, if a system does support these burst transfers, the PHY must transfer the read data in a rotating order as shown in Figure 4.6, “PHY Update”, Figure 4.6, “PHY Update”, Figure 4.6, “PHY Update” and Figure 4.6, “PHY Update”. Additionally, the MC must be able to capture this data correctly and correlate it to the proper read command.

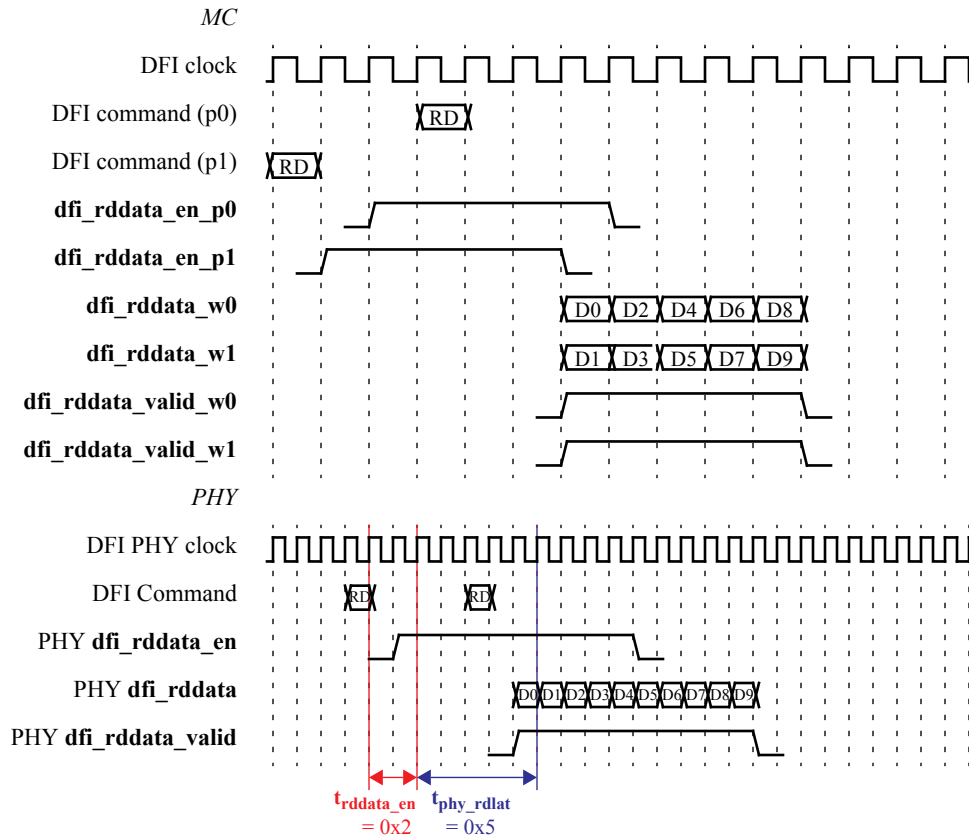
**FIGURE 47.** *DFI Read Data Bus for Two 10UI Bursts, each starting in Phase 0*



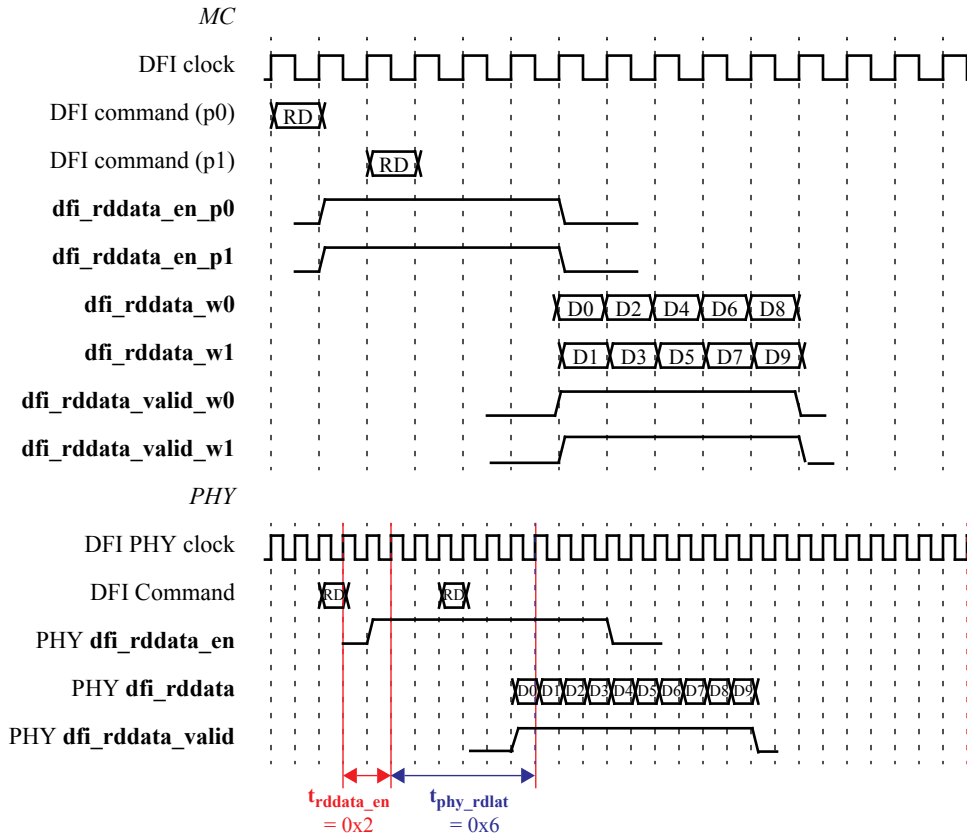
**FIGURE 48.** DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 0 ( $t_{rddata\_en}=2$ ,  $t_{phy\_rdlat}=5$ )



**FIGURE 49.** DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 1



**FIGURE 50.** DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 0 ( $t_{\text{rddata\_en}}=2$ ,  $t_{\text{phy\_rdlat}}=6$ )



#### 4.8.4.1.1 Read Data Resynchronization

When the read data rotation order is applicable, the MC and the PHY must maintain read data synchronization to properly interpret the read data order. If a condition occurs where the read data synchronization may be lost, a mechanism is necessary to resynchronize the devices. Conditions may include training or reporting an error. In order to be able to resynchronize when either the **dfi\_ctrlupd\_req** or **dfi\_phyupd\_ack** signals are asserted, reset the read data in a Frequency Ratio implementation in both the MC and PHY. Following the assertion of either the **dfi\_ctrlupd\_req** or **dfi\_phyupd\_ack** signal, the next read data word is always sent on **dfi\_rddata\_w0** regardless of the location of the previous data word.

## 4.9 Frequency Change

The DFI specification defines a frequency change protocol between the MC and the PHY to allow the devices to change the clock frequency of the memory controller and PHY without completely re-setting the system. The memory specifications define

various memory states in which the clock frequency can be changed safely. The general procedure is to put the memory in one of these states, modify the clock frequency and then re-synchronize the system. When the new clock frequency has been established, the PHY may need to re-initialize various circuits to the new clock frequency prior to resuming normal memory operation. Once complete, the memory system is ready to resume normal operation.

Frequency Change is an optional feature. The system may use a non-DFI frequency change method, or may choose to not support frequency change. However, if both the MC and the PHY intend to use the frequency change protocol, then the MC and PHY must comply with the handshake defined by the DFI specification. The handshaking protocol defines the signals through which the MC and the PHY allow a frequency change to occur and also provides a means to abort the process if the PHY does not respond to a frequency change request. When a frequency change occurs, some of the DFI timing parameters may need to be changed.

NOTE: During the frequency change, the DFI clock must remain valid - either operating at a valid frequency or gated high or low.

The signals used in the frequency change protocol are **dfi\_init\_start**, asserted during initialization and in normal operation, and **dfi\_init\_complete**. For more information on these signals, refer to Section 3.5, “Status Interface”.

#### **4.9.1 Frequency Change Protocol - Acknowledged**

During normal operation, once the **dfi\_init\_start** and **dfi\_init\_complete** signal have been asserted, the system may change the DFI clock frequency. The MC asserts the **dfi\_init\_start** signal to indicate that a clock frequency change is being requested. The PHY should not interpret the initial **dfi\_init\_start** assertion as a frequency change request. When the **dfi\_init\_start** signal is asserted, the MC and the PHY must reset their DFI read data word pointers to 0.

The MC guarantees that the **dfi\_init\_start** signal remains asserted for at least **t<sub>init\_start</sub>** cycles, allowing the PHY time to respond. The PHY may respond or ignore the frequency change request. To acknowledge the request, the **dfi\_init\_complete** signal must be de-asserted within **t<sub>init\_start</sub>** cycles of the assertion of the **dfi\_init\_start** signal, or the opportunity for frequency change is withdrawn until the MC re-asserts this signal. The **dfi\_init\_complete** signal must de-assert at least one cycle before **t<sub>init\_start</sub>** expires.

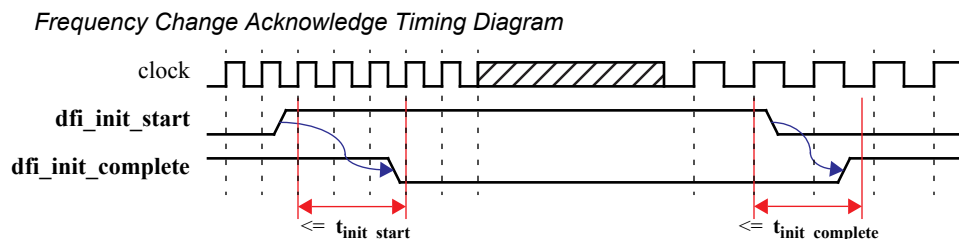
If the frequency change is acknowledged, the MC must hold the **dfi\_init\_start** signal asserted as long as the frequency change continues. Once the frequency change has completed, the MC de-asserts the **dfi\_init\_start** signal. The PHY must then complete any re-initialization required for the new clock frequency and re-assert **dfi\_init\_complete** within **t<sub>init\_complete</sub>** cycles.

During a frequency change operation, the PHY must ensure that the memory interface is maintained at valid and stable levels throughout the operation to ensure that memory protocol is being observed. The MC must also insure that it maintains valid and stable levels on the DFI while **dfi\_init\_start** is asserted or **dfi\_init\_complete** is de-asserted.

Note that no maximum number of cycles for the entire cycle to complete is specified by the DFI.

Figure 51, “Frequency Change Acknowledge Timing Diagram” shows the MC holding the **dfi\_init\_start** signal asserted as long as the frequency change continues and the PHY re-asserting **dfi\_init\_complete** within  $t_{init\_complete}$  cycles.

**FIGURE 51.**

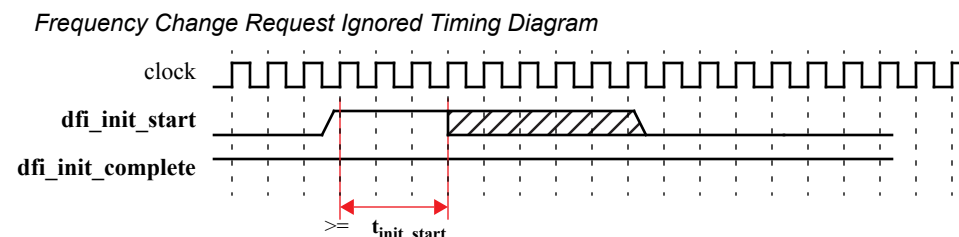


#### 4.9.2 Frequency Change Protocol - Not Acknowledged

The MC must assert the **dfi\_init\_start** signal for at least  $t_{init\_start}$  cycles. It is important to note that the PHY is not required to respond to a frequency change request.

Figure 52, “Frequency Change Request Ignored Timing Diagram” shows the MC asserting the **dfi\_init\_start** signal for  $t_{init\_start}$  cycles.

**FIGURE 52.**



### 4.10 Parity

Parity bits are used in command transmission to verify that the command has been transmitted correctly between master and slave. A single parity bit is sent with each command and identifies if the number of bits set high in the **dfi\_address**, **dfi\_act\_n**, **dfi\_bg**, **dfi\_bank**, **dfi\_cas\_n**, **dfi\_ras\_n** and **dfi\_we\_n** signals is an even or an odd number. If the DRAM receives a command where the number of bits of these signals set to ‘b1’ does not match the even/odd setting of the **dfi\_parity\_in** signal, then an error occurred during transmission.

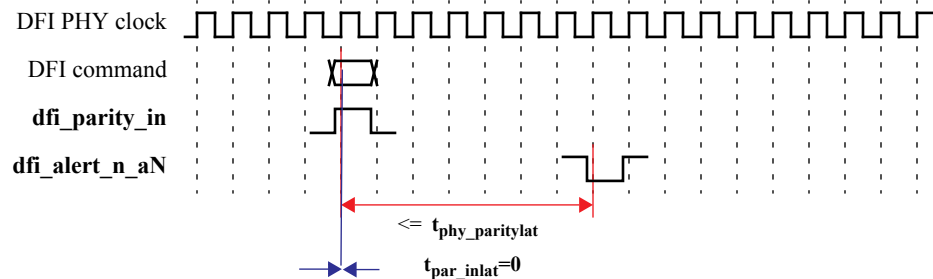
The **dfi\_parity\_in** signal is sent from the MC and is valid for one cycle per command. The command and other DFI signals are reflected on the PHY/DRAM interface  $t_{ctrl\_delay}$  cycles after being sent.

The **dfi\_parity\_in** signal is sent  $t_{par\_inlat}$  cycles after the DFI command; if  $t_{par\_inlat}=0$ , **dfi\_parity\_in** and the DFI command are sent in the same cycle. The memory systems compute parity on the incoming command and compare the computed value with the value driven on the DFI parity signal. If these values do not match, the memory systems assert a parity error output, which is sent back to the PHY. The **dfi\_parity\_error** signal is asserted within  $t_{phy\_paritylat}$  cycles of the associated **dfi\_parity\_in** signal. Since  $t_{phy\_paritylat}$  is a maximum value, the **dfi\_parity\_error** signal can not be correlated to one specific command, but to any command sent within the last  $t_{phy\_paritylat}$  cycles.

Figure 53, “Odd Command Parity Error Example Timing Diagram” shows the timing between the command and error with an odd command parity example.

FIGURE 53.

Odd Command Parity Error Example Timing Diagram



#### 4.10.1 CA Parity Timing

The DFI protocol supports CA parity utilizing the **dfi\_parity\_in** signal to transmit the parity data across the DFI. The MC generates the **dfi\_parity\_in** signal, sends it across the DFI, and transmits the signal through the PHY to the memory subsystem.

In frequency ratio systems, the **dfi\_parity\_in** signal is defined per phase, similar to the CA bus. For example, in a 1:2 frequency ratio system, the parity data is sent on **dfi\_parity\_in\_p0** and **dfi\_parity\_in\_p1**.

To generalize the parity support for current and future parity implementations, the  $t_{parin\_lat}$  parameter, defined in Table 14, “Status Interface Signals,” on page 43, specifies the timing of the **dfi\_parity\_in\_pN** signal relative to the dfi command. The  $t_{parin\_lat}$  parameter, allows the parity data to be sent coincident with the command or on a subsequent cycle.



### 4.10.2 CA and CRC Parity Errors

The DRAM generates both CA and CRC parity errors, and transfers the signals across the DFI bus. The MC must support the **dfi\_alert\_n\_aN** error signal, while the PHY can optionally support the signal.

The active low **dfi\_alert\_n\_aN** signal transmits both write CA and CRC parity errors. The PHY is not required to distinguish between a CA and a CRC parity error, instead, the PHY transmits the error to the MC for evaluation. The PHY holds the current state of the **dfi\_alert\_n\_aN** signal until the PHY error input transitions to a new value. Consequently, the pulse width of **dfi\_alert\_n\_aN** matches the pulse width of the DRAM subsystem error signal, plus or minus any synchronization cycles.

#### 4.10.2.1 CA and CRC Parity Errors in Frequency Ratio Systems

With frequency ratio systems, multiple **dfi\_alert\_n\_aN** outputs from the PHY are required to accurately transfer the error pulse width.

Table 24, “dfi\_alert\_n Signal With Matched and Frequency Ratio Systems,” on page 113 defines the outputs for matched frequency, 1:2 frequency, and 1:4 frequency systems. In all cases, the PHY must synchronize the **dfi\_alert\_n\_aN** outputs to the DFI clock domain. During synchronization, the width of the DRAM error signal may change by a few cycles, and these small changes in the error pulse width are acceptable.

**TABLE 24.** *dfi\_alert\_n Signal With Matched and Frequency Ratio Systems*

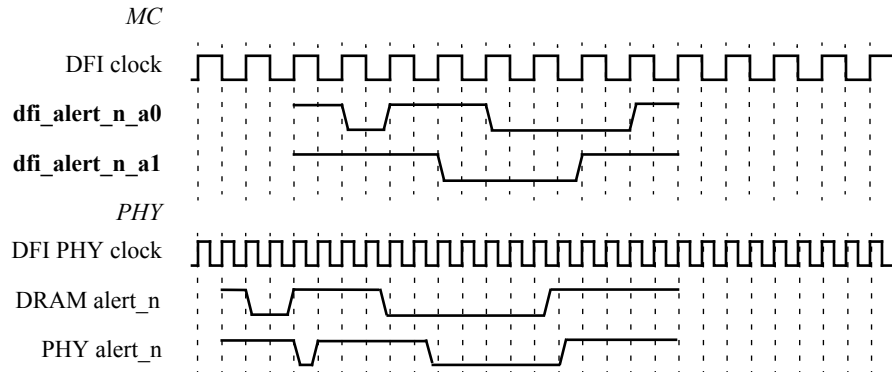
System	Alert Outputs	Description
Matched Frequency	dfi_alert_n	Single Output Width of output indicates width of error pulse +/- synchronization errors.
1:2 Frequency	dfi_alert_n_a0 dfi_alert_n_a1	2 outputs, one for each phase of the DFI clock. Combination of signals is used to determine error pulse width. EXAMPLE: dfi_alert_n_a0 and dfi_alert_n_a1 are both asserted for 1 DFI clock period. The error signal width is 2 DRAM clocks +/- synchronization errors.

System	Alert Outputs	Description
1:4 Frequency	dfi_alert_n_a0 dfi_alert_n_a1 dfi_alert_n_a2 dfi_alert_n_a3	<p>4 outputs, one for each phase of the DFI clock.</p> <p>Combination of signals is used to determine error pulse width.</p> <p>EXAMPLE:</p> <p><b>dfi_alert_n_a0, dfi_alert_n_a1, dfi_alert_n_a2, and dfi_alert_n_a3</b> are all asserted for 1 DFI clock period</p> <p>The error signal width is 4 DRAM clocks +/- synchronization errors.</p> <p>EXAMPLE:</p> <p>Only <b>dfi_alert_n_a1</b> and <b>dfi_alert_n_a2</b> are asserted for 1 DFI clock period</p> <p>The error signal width is 2 DRAM clocks +/- synchronization errors.</p>

In Figure 54, “dfi\_alert\_n\_aN with 1:2 Frequency Ratio”, the 1st assertion of the DRAM error signal (DRAM **alert\_n**) is held for 2 DRAM clocks, but due to synchronization, only **dfi\_alert\_n\_a0** is asserted on the DFI bus, indicating a single DRAM clock period pulse. The 2nd assertion of the DRAM error signal is held for multiple cycles, and the DFI output indicates this functionality by asserting both **dfi\_alert\_n\_a0** and **dfi\_alert\_n\_a1** as required. The **dfi\_alert\_n\_a0** and **dfi\_alert\_n\_a1** signals correlate to the phase of the DFI clock. However, the assertion of **dfi\_alert\_n\_a0** does not directly relate to the phase of assertion on the DRAM bus and therefore the assertion of **dfi\_alert\_n\_a0** is not directly related to the phase of the write data.

FIGURE 54.

**dfi\_alert\_n\_aN with 1:2 Frequency Ratio**



## 4.11 DFI Training Operations

DFI read and write training operations can increase accuracy of signal placement at higher speeds in DDR4, DDR3, and LPDDR2 systems.

The DFI has three training operations to support read training and write leveling. Read training” collectively refers to two operations, gate training and read data eye training.

For more information on the training operations and to identify operations that correspond to specific devices, refer to Section 3.6, “DFI Training Interface,” on page 47.

For DFI compliance, the MC must support both “Non-DFI Mode” and “DFI Training Mode” for the applicable training operations; the PHY may support one mode for each applicable training operation and the mode is set per operation.

Support for the defined state of each programmable parameter must be defined by each device and may be implemented as programmable registers within the device. The parameter is defined as a single enable bit indicating whether or not the corresponding DFI training operation (gate training, read data eye training, or write leveling) is enabled.

In DFI training mode, the MC sets up the DRAM for gate training, read data eye training, or write leveling and periodically issues read or write commands. The PHY is responsible for determining the correct delay programming for each operation. The PHY evaluates the data returned from the commands, adjusts the delays and evaluates the results to locate the appropriate edges. The MC assists by enabling and disabling the leveling logic in the DRAMs and the PHY and by generating the necessary read commands, mode register reads or write strobes. The PHY informs the MC when it has completed training, which triggers the MC to stop generating commands and to return to normal operation.

The MC must complete all transactions in progress to memory prior to initiating any of the training operations. Once any of the enable signals are asserted, the PHY should immediately enable the associated logic. During training, the MC does not use the memory response from the PHY. Therefore the only relevant DFI timing parameters are  $t_{rdlvl\_rr}$  for read training and  $t_{wrlvl\_ww}$  for write leveling. The timing parameter  $t_{rdlvl\_rr}$  defines the minimum number of cycles that the MC should wait between issuing reads for DDR4 and DDR3 memory systems or mode register reads for LPDDR2 memory systems. The timing parameter  $t_{wrlvl\_ww}$  dictates the minimum delay between write strobes. The MC continues to drive subsequent commands every  $t_{rdlvl\_rr}$  cycles, or subsequent write strobes every  $t_{wrlvl\_ww}$  until the PHY drives all bits of the response signal (**dfi\_rdlvl\_resp** or **dfi\_wrlvl\_resp**) high.

Multiple training sequences can be defined, with the sequence information supplied by either the MC or the PHY. The MC must provide flexibility to run training sequences required by the PHY and should not dictate a set of sequences. The PHY determines the sequences necessary to accomplish training. Both the MC and the PHY need to be aware of the defined training sequences and the specific sequence required for each training operation.

Whether the MC or the PHY initiates the training sequence, the MC asserts the enable signal to initiate or accept the training sequence, and the MC holds the enable signal asserted until the current training operation completes. For information on how the MC defines the required training sequence, refer to Section 3.6.1, “Read Training Operation,” on page 48.

NOTE: The DFI training requires the MC to support the training sequences to the PHY by generating MRW commands, toggling the enable parameter, generating the appropriate strobe signals, and evaluating the response. The PHY is responsible for adjusting the DLL delays and evaluating the responses from memory. When the PHY is satisfied with the training sequence, a completion response is sent back to the MC.

For DDR4, training sequence accuracy is increased with a selection of encodings. The MC determines a sequence of up to four unique, non-default Multi-Purpose Register (MPR) values and formats and drives the **dfi\_lvl\_pattern** signal to communicate the sequence to the PHY to indicate the training pattern that is currently active.

In Non-DFI mode, the PHY either does not support training or supports training independent of the DFI signaling. In Non-DFI mode, the associated training interface is not used, and the MC should be capable of generating the required MRS commands to enter or exit the test modes of the DRAMs.

#### 4.11.1 Initiating a Training Operation

The MC or the PHY may initiate any training operation. Training may be executed during initialization, frequency change or during normal operation. The MC is responsible for initiating gate training, read data eye training, and/or write leveling required during initialization or frequency change. The PHY should not request training or leveling during initialization; if the PHY requests training during a frequency change, the PHY must assert it prior to asserting **dfi\_init\_complete**.

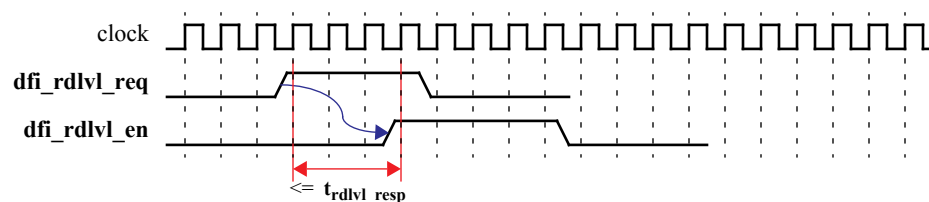
The PHY can request gate training by driving the **dfi\_rdlvl\_gate\_req** signal, read data eye training by driving the **dfi\_rdlvl\_req** signal, or write leveling by driving the **dfi\_wrlvl\_req** signal.

The MC must respond to any of these requests by asserting the appropriate enable (**dfi\_rdlvl\_en**, **dfi\_wrlvl\_en** or **dfi\_rdlvl\_gate\_en**) within the relevant  $t_{rdlvl\_resp}$  or  $t_{wrlvl\_resp}$  cycles.

Figure 55 shows this timing relationship for the data eye training process. The timing is similar for gate training and write leveling.

FIGURE 55.

Read Data Eye Training Request Timing



The MC waits for the response signal to be asserted before disabling the active training logic. The response is always received on the **dfi\_rdlvl\_resp** or **dfi\_wrlvl\_resp** signals.

The DFI specifies maximum times that the system waits for a response on the **dfi\_rdlvl\_resp** or **dfi\_wrlvl\_resp** signals as **t<sub>rdlvl\_max</sub>** and **t<sub>wrlvl\_max</sub>**, respectively.

During read training, when **dfi\_rdlvl\_en** or **dfi\_rdlvl\_gate\_en** is asserted, the MC will drive the target chip select on **dfi\_rddata\_cs\_n**. During write leveling when **dfi\_wrlvl\_en** is asserted, the MC will drive the target chip select on **dfi\_wrdata\_cs\_n**.

A MC supporting the DFI Training mode in a system which supports independent training per chip select must support the data path chip selects **dfi\_rddata\_cs\_n** and **dfi\_wrdata\_cs\_n**, and the training chip select signals **dfi\_phy\_rdlvl\_cs\_n**, **dfi\_phy\_rdlvl\_gate\_cs\_n**, and **dfi\_phy\_wrlvl\_cs\_n**. A PHY asserting the DFI training mode request optionally may support any combination of these signals. Any unused input signals should be tied inactive at the MC.

For more information on write leveling signals, refer to Section 58, “Read Training in DFI Training Mode for LPDDR2 Memory Systems,” on page 119.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 19.

#### **4.11.2 Read Training**

“Read training” collectively refers to gate training and read data eye training.

The goal of gate training is to locate the setting at which the initial read DQS rising edge aligns with the rising edge of the read DQS gate. Once this setting is identified, the read DQS gate can be adjusted to the approximate midpoint of the read DQS preamble prior to the DQS.

To indicate proper alignment of the gate to the first read DQS, the gate training operation requires that the read DQS gate be placed within the bounds of the beginning of the read DQS preamble and the falling edge of the first read DQS. Placing the gate within the bounds of the timing window may require another alignment method or may require running gate training iteratively.

For an example of gate training, refer to Figure 56, “Gate Leading DQS Timing,” on page 118.

The gate training signals are: **dfi\_rddata\_en**, **dfi\_rdlvl\_gate\_en**, **dfi\_rdlvl\_gate\_req**, **dfi\_rdlvl\_resp** and the DFI command bus. The corresponding mode parameter is **phy\_rdlvl\_gate\_en**. When the PHY initiates gate training, the PHY can optionally send the **dfi\_phy\_rdlvl\_gate\_cs\_n** signal to indicate the targeted chip select. The MC transfers the **dfi\_rddata\_gate\_cs\_n** signal to identify the chip select currently being trained.

The goal of data eye training is to identify the delay at which the read DQS rising edge aligns with the beginning and end transitions of the associated DQ data eye. By identifying these delays, the system can calculate the midpoint between the delays and accurately center the read DQS within the DQ data eye.

The read data eye training signals are: **dfi\_rddata\_en**, **dfi\_rdlvl\_en**, **dfi\_rdlvl\_req**, **dfi\_rdlvl\_resp** and the DFI command bus. . The corresponding mode parameter is **PHY\_rdlvl\_en**. When the PHY initiates data eye training, the PHY can optionally send the **phy\_rdlvl\_cs\_n** signal to indicate the targeted chip select. The MC responds by executing training and transfers **dfi\_rddata\_cs\_n** to indicate the chip select being trained.

From the MC perspective, the gate training and read data eye training operations are handled identically so both operations may be issued utilizing a single interface. For more information on the gate training and data eye training operations, refer to Section 3.3, “Read Data Interface,” on page 33 and Section 3.6, “DFI Training Interface,” on page 47.

Figure 56 is an example of gate training.

**FIGURE 56.**

#### Gate Leading DQS Timing

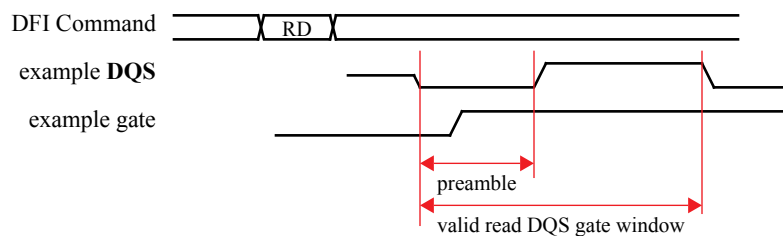
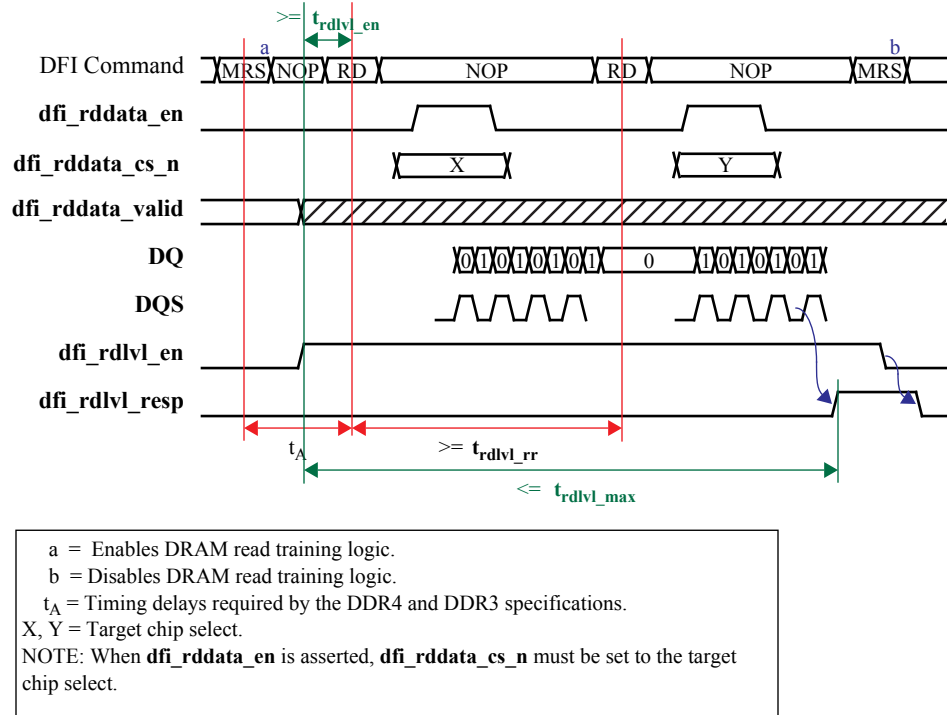


Figure 57 demonstrates read training in DDR4 and DDR3 memory systems. Figure 58 shows read training in LPDDR2 memory systems.

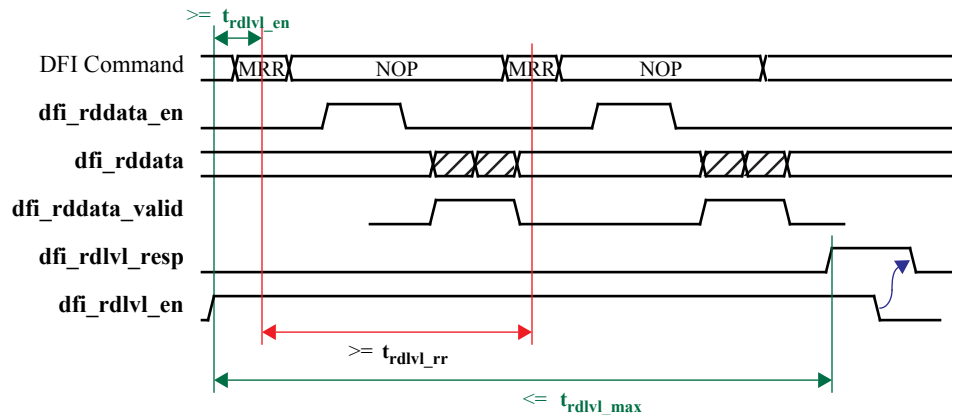
- DDR4, DDR3: MRS commands are used to enable and disable the read training logic in the DRAMs.
- LPDDR2: No MRS commands are required to enable/disable the leveling mode in the DRAMs.

In both cases, the **dfi\_rdlvl\_en** signal is used to enable/disable the read training logic in the PHY. During read training, **dfi\_rddata\_valid** and **dfi\_rddata** are ignored in DDR4 and DDR3 systems. All evaluations and delay changes are handled within the PHY. When the PHY has found the necessary edges and completed read training, the PHY drives the **dfi\_rdlvl\_resp** signal high, which informs the MC that the procedure is done. The MC then de-asserts the **dfi\_rdlvl\_en** signal. Once the **dfi\_rdlvl\_en** signal has de-asserted, the PHY may stop driving the **dfi\_rdlvl\_resp** signal.

**FIGURE 57.** Read Training in DFI Training Mode for DDR4 and DDR3 Memory Systems



**FIGURE 58.** Read Training in DFI Training Mode for LPDDR2 Memory Systems



### 4.11.3 Write Leveling

The goal of write leveling is to locate the delay at which the write DQS rising edge aligns with the rising edge of the memory clock. By identifying this delay, the system can accurately align the write DQS within the memory clock.

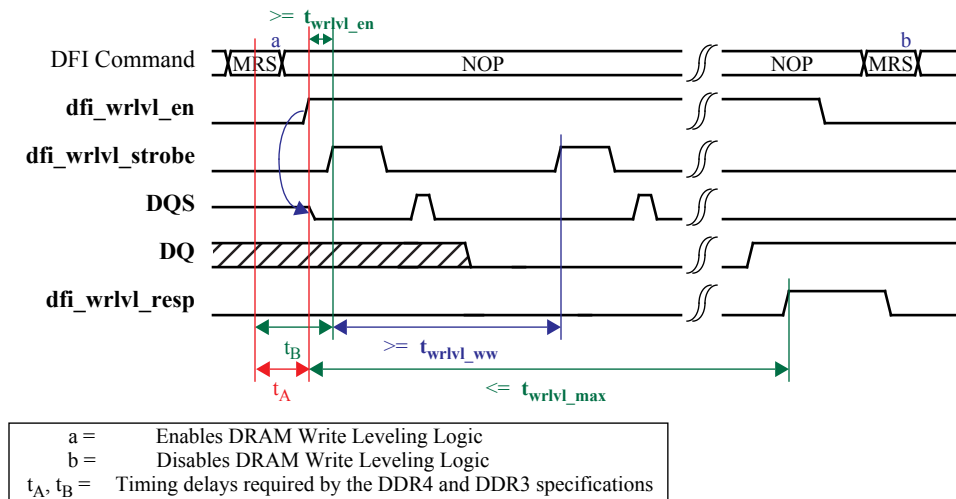
When the PHY initiates write leveling, the PHY can optionally send the **dfi\_phy\_wrlvl\_cs\_n** signal to indicate the targeted chip select. The MC transfers the signal to identify the chip select currently being trained. For more information on the write leveling parameter, refer to Section 3.6.2, “Write Leveling Operation,” on page 48.

The signals used in write leveling are: **dfi\_wrlvl\_en**, **dfi\_wrlvl\_req**, and **dfi\_wrlvl\_strobe**. The corresponding parameter is PHY\_WRLVL\_EN. The write leveling chip select signal is **dfi\_phy\_wrlvl\_cs\_n**. For more information on write leveling signals, refer to Section 3.2, “Write Data Interface,” on page 29.

Figure 59 demonstrates write leveling in DFI Training mode. The MRS commands are used to enable and disable the write leveling logic in the DRAMs and the **dfi\_wrlvl\_en** signal is used to enable/disable the write leveling logic in the PHY.

FIGURE 59.

Write Leveling in DFI Training Mode



#### 4.11.4 **dfi\_lvl\_pattern** Encoding

In DDR4 systems executing read training, the MC drives the **dfi\_lvl\_pattern** signal to define the required training sequence. The **dfi\_lvl\_pattern** signal must be valid when the enable signal is asserted for gate training and data eye training. Similar to the enable signal, the **dfi\_lvl\_pattern** signal may transition when training completes.

The **dfi\_lvl\_pattern** signal encodes the required training sequences for DDR4 DRAMs. The width of **dfi\_lvl\_pattern** is: (4 x DFI Read Leveling PHY I/F Width), with a 4-bit encoding defined per slice. The DDR4 encoding determines which MPR is accessed, which DRAM-defined MPR data format is used, and if a unique, non-default, pattern is utilized. The DFI bus does not define the unique patterns; the MPR signals contain a set of encodings which can be used to define unique patterns, with the MC and the PHY programming determining the specific patterns.



NOTE: The **dfi\_lvl\_pattern** signal must hold its value and not transition throughout the training sequence.

In Figure 60, “dfi\_lvl\_pattern Timing,” on page 121, ‘Sequence X’ can be any valid sequence defined by the valid **dfi\_lvl\_pattern** encodings. This value will indicate the pattern returned by the DRAM and evaluated by the PHY.

NOTE: If multiple sequences are required, the MC can assert **dfi\_rdlvl\_en** and/or **dfi\_rdlvl\_gate\_en** multiple times with different values driven on **dfi\_lvl\_pattern**.

The **dfi\_lvl\_pattern** signal encoding supports both serial and staggered MPR formats without specific support for the parallel format. The non-default MPR value and format encodings can be used to select a parallel format if required. The **dfi\_lvl\_pattern** encodings support up to 4 unique, non-default, MPR values and formats for DDR4. These encodings, ‘b1000 to ‘b1011, can select an MPR number, value, and format to create a unique training sequence. For example, the ‘b1000 encoding, defined as Sequence 0, could select the following training sequence:

- MPR Number: MPR2
- MPR Value: 0x1111\_1110
- MPR Format: Serial

A setting of 4'b0000 will select a DDR3-like MPR setting.

FIGURE 60.

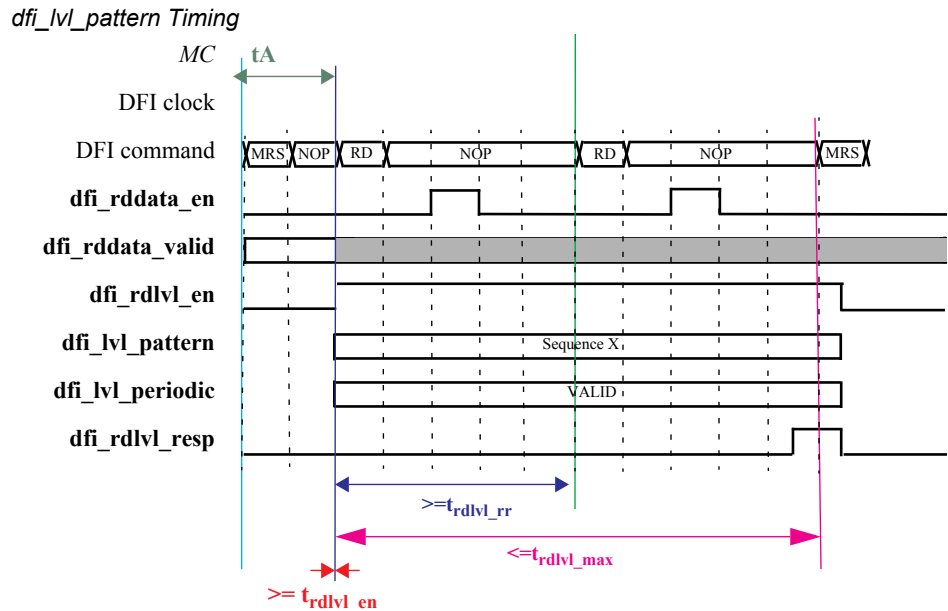


Table 25, “DDR4 Encoding of dfi\_lvl\_pattern,” on page 122 is used for gate training and data eye training for DDR4 DRAMs.

**TABLE 25.** *DDR4 Encoding of dfi\_lvl\_pattern*

dfi_lvl_pattern				Description	
Non-default	Format	MPR			
[3]	[2]	[1]	[0]		
0	0	0	0	Serial format	Access MPR0
0	0	0	1	Default MPR Value	Access MPR1
0	0	1	0		Access MPR2
0	0	1	1		Access MPR3
0	1	0	0		Staggered format Default MPR Value
0	1	0	1	Access starting with MPR1	
0	1	1	0	Access starting with MPR2	
0	1	1	1	Access starting with MPR3	
1	0	0	0	Non-default MPR Value	Sequence 0
1	0	0	1	Any MPR	Sequence 1
1	0	1	0	Any format	Sequence 2
1	0	1	1	All defined programatically	Sequence 3
1	1	0	0	Reserved for future use	
1	1	0	1		
1	1	1	0		
1	1	1	1		

#### 4.11.5 Support for Non-data Commands During Training

A PHY training sequence that exceeds the time the MC allows between refreshes or other required commands requires a method for executing these commands. This sequence must be supported by all MCs and PHYs supporting the DFI training interface for all supported DFI training sequences.

For DDR4 and DDR3, Read Training and Write Leveling require an MRW command to be issued to place memory in a data eye training (MPR) or write leveling operating mode. In either case, the memory specification does not permit any commands other than NOP and MRW while memory is in the special operating mode. Therefore, execution of a refresh will require issuance of an MRW to exit the special operating mode before executing the refresh command.

The sequence required to execute a refresh or other non-data command while running a read or write leveling sequence during training is:

1. Wait for the current command-to-command timing to complete ( $t_{rdlvl\_rr}$  or  $t_{wrlvl\_ww}$ ).
2. If required, execute an MRW to exit the training mode. In all cases, maintain the assertion of the training enable signal (**dfi\_rdlvl\_en**, **dfi\_rdlvl\_gate\_en**, or **dfi\_wrlvl\_en**).
3. Execute a refresh or other non-data command.
4. If required, execute an MRW to re-enter the identical training state previously occupied.
5. Continue training sequence after meeting all timing requirements associated with MRW-to-command timing as defined at the beginning of the sequence.

Maintaining the assertion of the enable signal (**dfi\_rdlvl\_en**, **dfi\_rdlvl\_gate\_en**, or **dfi\_wrlvl\_en**) allows the PHY to distinguish the exit portion of this command sequence from an aborted training sequence and the enter portion of this command sequence from the start of a new sequence.

Figure 61, “Refresh Execution During Read Training Operation” shows that the PHY should continue the training from the point where it was interrupted. Since the PHY did not assert the response signal (**dfi\_rdlvl\_resp** or **dfi\_wrlvl\_resp**), the sequence is not complete.

Figure 62, “Refresh Execution During Read Training Operation With Completion Response” shows that if the response is asserted any time during the refresh sequence, the training sequence should be completed as previously defined.

The training sequences may require the MC to maintain certain signal states while training is in progress. For example, during write leveling the MC may drive ODT. When exiting the training sequence to execute a non-data command such as a refresh, the MC may need to change the state of such signals as appropriate for the commands being executed.

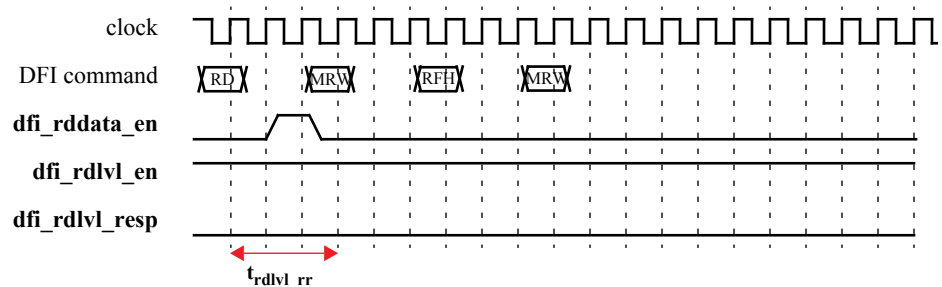
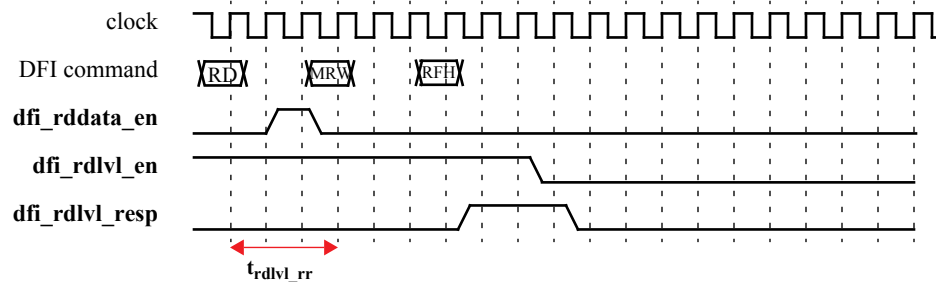
**FIGURE 61.**
*Refresh Execution During Read Training Operation*


FIGURE 62.

*Refresh Execution During Read Training Operation With Completion Response*

## 4.12 Low Power Control Handshaking

If the PHY has knowledge that the DFI will be idle for a period of time, the PHY may be able to enter a MC-initiated low power state. During low power handshaking, the DFI clock must maintain a valid and constant clock operating frequency.

When the MC detects an idle time, the MC asserts the **dfi\_lp\_req** signal to the PHY and the **dfi\_lp\_wakeup** signal with the wakeup time required. The PHY can acknowledge the request and go into low power mode based on the wakeup time required and remain in low power mode as long as the request and acknowledge are both asserted, or the PHY can disregard the request and not change power states even if a low power opportunity request was acknowledged.

If the request is acknowledged through the assertion of the **dfi\_lp\_ack** signal, the PHY may enter a low power mode as long as the **dfi\_lp\_req** signal remains asserted. Once the **dfi\_lp\_req** signal is de-asserted, the PHY must return to normal operating mode within the number of cycles indicated by the **dfi\_lp\_wakeup** signal.

Wakeup time is a specific number of cycles (**t<sub>lp\_wakeup</sub>** cycles) in which the PHY is required to respond to a signal change (the de-assertion of the **dfi\_lp\_req** signal) on the DFI. The DFI specification defines up to 16 different wakeup times; neither the MC nor the PHY are required to support all of the defined wakeup times. Generally, the PHY should enter the lowest supported power state that allows low power exit within the required wakeup time.

The MC may support the **dfi\_lp\_req** signal with or without the **dfi\_lp\_ack** signal. The MC guarantees that **dfi\_lp\_req** will be asserted and the **dfi\_lp\_wakeup** signal will be constant for at least **t<sub>lp\_resp</sub>** cycles, allowing the PHY time to respond. The PHY may respond or ignore the low power mode request. To acknowledge the request, the PHY must assert the **dfi\_lp\_ack** signal within **t<sub>lp\_resp</sub>** clock cycles of the request signal assertion, during which time the MC must hold the **dfi\_lp\_wakeup** signal constant. Once the request has been acknowledged by the PHY, the MC may de-assert the **dfi\_lp\_req** signal. The PHY must de-assert the **dfi\_lp\_ack** signal within **t<sub>lp\_wakeup</sub>**

clock cycles after the **dfi\_lp\_req** signal is de-asserted and be ready for normal operation.

Figure 63, “Low Power Control Handshaking Timing Diagram” shows a sequence in which the request is acknowledged.

FIGURE 63.

Low Power Control Handshaking Timing Diagram

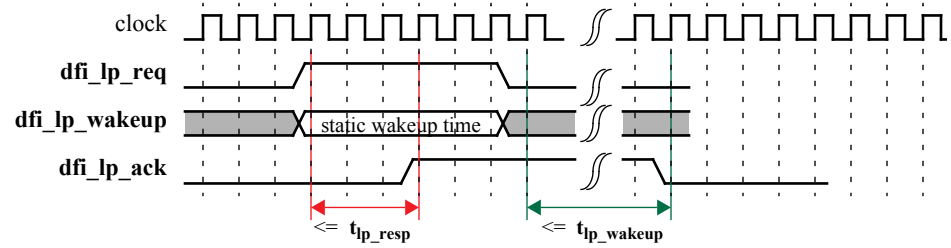
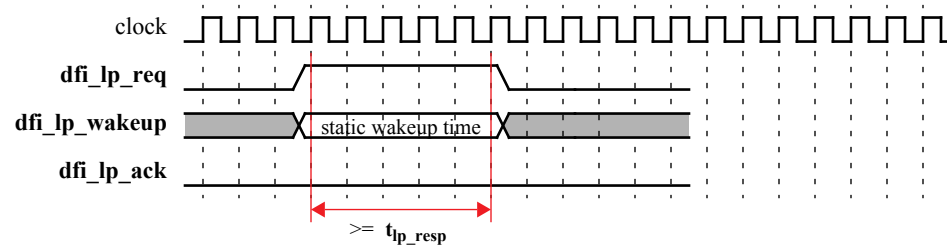


Figure 64, “Low Power Control Request with No Response” shows that the **dfi\_lp\_ack** signal is not required to assert when the **dfi\_lp\_req** signal is asserted. The MC must assert the **dfi\_lp\_req** signal for at least  $t_{lp\_resp}$  cycles. If the **dfi\_lp\_ack** signal is not asserted within  $t_{lp\_resp}$  cycles, the PHY must not assert the acknowledge for the current request. The **dfi\_lp\_req** signal should be de-asserted after  $t_{lp\_resp}$  cycles have elapsed without an acknowledge.

FIGURE 64.

Low Power Control Request with No Response



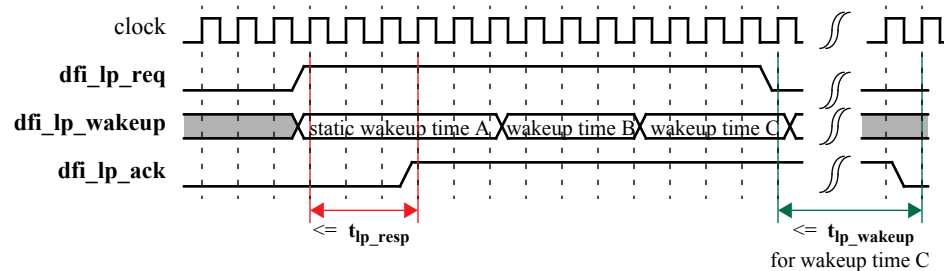
After the request has been acknowledged, the MC may increase the time that the PHY has to respond beyond the time that was initially defined. The MC is allowed to change the **dfi\_lp\_wakeup** signal to a larger value as long as both the **dfi\_lp\_ack** and **dfi\_lp\_req** signals are asserted. This results in a longer  $t_{lp\_wakeup}$  time for the PHY.

The value of the **dfi\_lp\_wakeup** signal when the **dfi\_lp\_req** signal is de-asserted will be used to define the  $t_{lp\_wakeup}$  time.

Figure 4.13, “Error Signaling” shows a scenario with the assumption that the wakeup time is increased with each change.

FIGURE 65.

Low Power Control Handshaking Timing Diagram with Multiple Wakeup Times



### 4.13 Error Signaling

The optional DFI error interface enables the PHY to communicate error information from the PHY to the MC.

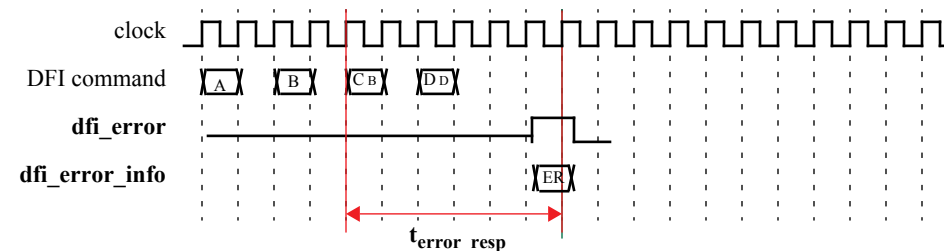
For data errors, the timing parameter is defined as the max delay from **dfi\_wrdata\_en** or **dfi\_rddata\_en** to the assertion of the **dfi\_error** signal.

For command errors, the timing parameter is defined as the max delay from command to the assertion of the **dfi\_error** signal. Since the timing parameter is a maximum delay, it is not always possible to correlate the error with a specific command.

Figure 66, “Example of Error Condition”, shows the error interface for the control signal interface of the PHY. The error condition does not affect RD A and RD B, the error condition may affect RD C and/or RD D.

FIGURE 66.

Example of Error Condition



### **4.13.1 Error Code Definitions**

Table 26, “Error Codes” defines specific error codes, error codes reserved for future use, and error codes available for design-specific definition. Not all defined error codes apply to all systems; all error types are optional unless required as part of another interface.

If multiple errors occur in a single clock cycle, the PHY is responsible for resolving communication through error prioritization, using multiple clocks, or other means.

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**TABLE 26.** *Error Codes*

<b>Error Response Code</b>	<b>Name</b>	<b>Description</b>
0000	General purpose	The PHY indicates a general purpose error.
0001	Internal PHY	The PHY indicates some internal error condition.
0010-0111	Reserved	Reserved for a future definition.
1000 - 1111	User-defined	These error codes are available for user definition.

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## **5.0 Signal Timing**

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The DFI specification does not specify timing values for signaling between the MC and the PHY. The only requirement is that a DFI clock must exist, and all DFI-related signals must be driven by registers referenced to the rising edge of this clock. There are no restrictions on how these signals are received, nor any rules on the source of the DFI clock. Compatibility between the MC and the PHY at given frequencies is dependent on the specification of both the output timing for signals driven and the setup and hold requirements for reception of these signals on the DFI.

However, the DFI signals are categorized into three signal groups that place restrictions on how signals may be driven and captured by DFI devices. All DFI signals may be driven from the DFI clock and captured on the following rising edge of the DFI clock. However, some signals may allow less restrictive timing which may alleviate timing restrictions within the design.

For frequency ratio systems, the PHY must send and receive DFI signals with respect to the rising edge of the DFI clock, even if the signals are driven and captured by registers clocked by the higher frequency DFI PHY clock.

There are three signal groups:

#### **1. Standard Signals**

Standard signals contain timing critical information on a cycle-by-cycle basis and, therefore, must be sent and received on every DFI clock. The Control Interface

signals fall into the standard signal category because the Control Interface signals must be cycle-accurate to properly communicate memory commands.

Standard signals must be sent on the DFI clock and must be received on every DFI clock period for proper operation. All standard signals are required to meet setup and hold time to the DFI clock at the destination. Neither device should have a dependency on the source clock of the other device; the source and destination clock should always be assumed to be the DFI clock.

## **2. State-Retaining Signals**

State retaining signals contain information that is not single cycle-critical because state retaining signals retain a state change until either a signal acknowledge is received or a timing parameter has been satisfied. The Update Interface signals fall into the standard signal category because all signal state changes are defined in terms of signal responses and timing parameters.

State-retaining signals may be sent and received in the same way on every DFI clock period. They may also be sent and/or received by a divided frequency clock; provided that the lower frequency clock is an even multiple ( $\frac{1}{2}$ ,  $\frac{1}{4}$ , etc.) and is phase aligned to the DFI clock.

All state-retaining signals are required to meet setup and hold time to the DFI clock at the destination regardless of whether the signal is generated from the DFI clock or from a lower frequency, phase-aligned clock source. Neither device should have a dependency on the source clock of the other device; the source and destination clock should always be assumed to be the DFI clock. If a lower frequency clock is used, the associated timing parameters must be set to appropriately account for the timing effects of using a lower frequency clock at either the source or destination. The timing parameters are always defined in terms of the DFI clock regardless of the source and destination clock frequency.

## **3. Timer-Based Signals**

Training signals such as the **dfi\_rdlvl\_delay\_x** and **dfi\_rdlvl\_resp** are classified as timer-based signals because the training signals are not valid until the **t<sub>rdlvl\_load</sub>** and **t<sub>rdlvl\_resplat</sub>** timing parameters are met.

Timer-based signals do not have a clock-edge dependency because timer-based signals are either not required to be valid until a timing parameter has been met, another signal has been asserted, or they are expected to be static during normal operation (static signals may be changed during idle times).

Timer-based signals do not have to meet setup and hold time to the DFI clock except on the cycle after meeting the associated timing parameter. Timer-based signals may also be changed during idle times in which case the setup and hold times are irrelevant. For the purpose of timing analysis, timer-based signals may be treated as multi-cycle paths.

Table 27, “Signal Group Divisions.” shows that each DFI signal is categorized into a signal group.



TABLE 27.

*Signal Group Divisions.*

Signal	Signal Group
<b>dfi_act_n</b> (or <b>dfi_act_n_pN</b> )	Standard
<b>dfi_alert_n_aN</b>	Standard
<b>dfi_address</b> (or <b>dfi_address_pN</b> )	Standard
<b>dfi_bank</b> (or <b>dfi_bank_pN</b> )	Standard
<b>dfi_bg</b> (or <b>dfi_bg_pN</b> )	Standard
<b>dfi_cas_n</b> (or <b>dfi_cas_pN</b> )	Standard
<b>dfi_cid</b> (or <b>dfi_cid_pN</b> )	Standard
<b>dfi_cke</b> (or <b>dfi_cke_pN</b> )	Standard
<b>dfi_cs_n</b> (or <b>dfi_cs_pN</b> )	Standard
<b>dfi_ctrlupd_ack</b>	State-Retaining
<b>dfi_ctrlupd_req</b>	State-Retaining
<b>dfi_data_byte_disable</b>	Timer-Based
<b>dfi_dram_clk_disable</b>	Standard
<b>dfi_error</b>	Standard
<b>dfi_error_info</b>	Standard
<b>dfi_freq_ratio</b>	Timer-Based
<b>dfi_init_complete</b>	State-Retaining
<b>dfi_init_start</b>	State-Retaining
<b>dfi_lp_ack</b>	State-Retaining
<b>dfi_lp_req</b>	State-Retaining
<b>dfi_lp_wakeup</b>	State-Retaining
<b>dfi_lvl_pattern</b>	State-Retaining
<b>dfi_lvl_periodic</b>	State-Retaining
<b>dfi_odt</b> (or <b>dfi_odt_pN</b> )	Standard
<b>dfi_parity_error</b>	Standard
<b>dfi_parity_in</b> (or <b>dfi_parity_in_pN</b> )	Standard

Signal	Signal Group
<b>dfi_phy_rdlvl_cs_n</b>	State-Retaining
<b>dfi_phy_rdlvl_gate_cs_n</b>	State-Retaining
<b>dfi_phyupd_ack</b>	State-Retaining
<b>dfi_phyupd_req</b>	State-Retaining
<b>dfi_phyupd_type</b>	State-Retaining
<b>dfi_phy_wrlvl_cs_n</b>	State-Retaining
<b>dfi_ras_n</b> (or <b>dfi_ras_pN</b> )	Standard
<b>dfi_rddata</b> (or <b>dfi_rddata_wN</b> )	Standard
<b>dfi_rddata_cs_n_pN</b>	State-Retaining
<b>dfi_rddata_dbi_n_wN</b>	Standard
<b>dfi_rddata_dnv</b> (or <b>dfi_rddata_dnv_wN</b> )	Standard
<b>dfi_rddata_en</b> (or <b>dfi_rddata_en_pN</b> )	Standard
<b>dfi_rddata_valid</b> (or <b>dfi_rddata_valid_wN</b> )	Standard
<b>dfi_rdlvl_en</b>	State-Retaining
<b>dfi_rdlvl_gate_en</b>	State-Retaining
<b>dfi_rdlvl_gate_req</b>	State-Retaining
<b>dfi_rdlvl_req</b>	State-Retaining
<b>dfi_rdlvl_resp</b>	Timer-Based
<b>dfi_reset_n</b> (or <b>dfi_reset_pN</b> )	Standard
<b>dfi_we_n</b> (or <b>dfi_we_pN</b> )	Standard
<b>dfi_wrdata</b> (or <b>dfi_wrdata_pN</b> )	Standard
<b>dfi_wrdata_cs_n_pN</b>	Standard
<b>dfi_wrdata_en</b> (or <b>dfi_wrdata_en_pN</b> )	Standard
<b>dfi_wrdata_mask</b> (or <b>dfi_wrdata_mask_pN</b> )	Standard
<b>dfi_wrlvl_en</b>	State-Retaining
<b>dfi_wrlvl_req</b>	State-Retaining
<b>dfi_wrlvl_resp</b>	Timer-Based
<b>dfi_wrlvl_strobe</b>	Standard

## 6.0 Glossary

**TABLE 28.** *Glossary of Terms*

Term	Definition
Command Address (CA) Signals	Includes the following control interface signals: <b>dfi_act_n</b> , <b>dfi_address</b> , <b>dfi_bank</b> , <b>dfi_bg</b> , <b>dfi_ras_n</b> , <b>dfi_cas_n</b> , and <b>dfi_we_n</b> . The DRAM class determines the signals applicable to a specific system.
CA Bus	JEDEC defines the CA bus as a double data rate bus containing command, address and bank/row buffer information. The CA bus is specific to LPDDR2 systems.
Command Bus	Includes the following control interface signals: <b>dfi_act_n</b> , <b>dfi_cas_n</b> , <b>dfi_ras_n</b> and <b>dfi_we_n</b> . The DRAM class determines the signals applicable to a specific system.
Column Selection (CAS)	Column address strobe.
Data Bus Inversion (DBI)	A feature of the DRAM that allows read and write data to be inverted selectively before the data is transferred across the DDR data bus.
DFI Width	The width of the bus on the DFI interface. This is generally the same width as the DRAM bus.
DFI Bank Width	The number of bank bits on the DFI interface. This is generally the same number of bits as the number of bank pins on the DRAM device.
DFI Chip Select Width	The number of chip select bits on the DFI interface. This is generally the same number of bits as the number of chip select pins on the DRAM device.
DFI clock frequency	Defines the clock frequency of the MC.
DFI Control Width	The number of bits required to control the DRAMs, usually a single bit.
DFI Data Enable Width	The width of the datapath enable signals on the DFI interface. For PHYs with an 8-bit slice, this is generally 1/16th of the DFI Data Width to provide a single enable bit per memory data slice, but may be 1/4, 1/8, 1/32, or any other ratio. Bit zero corresponds to the lowest segment.
DFI Data Width	The width of the datapath on the DFI interface. This is generally twice the DRAM data width.
DFI data word	One phase of read or write data passed between the MC and the PHY. A DFI data word is twice the width of the bus between the DRAM and the PHY and corresponds to a single memory word transfer across the DFI bus.
<b>dfi<sub>rw</sub>_length</b>	The value of the total number of DFI clocks required to transfer one DFI read or write command worth of data. For a matched frequency system: <b>dfi<sub>rw</sub>_length</b> would typically be equal to (burst length/2). For a frequency ratio system: <b>dfi<sub>rw</sub>_length</b> would typically be equal to ((burst length/2)/frequency ratio).
DFI Read Data Valid Width	The width of the datapath valid signals on the DFI interface. Equivalent to the number of PHY data slices, the same width definition as the <b>dfi_rddata_en</b> signal. Bit zero corresponds to the lowest segment.
DFI Read Training Delay Width	The number of bits required to communicate read delay information to the PHY.
DFI Read Training Gate Delay Width	The number of bits required to communicate gate training delay information to the PHY.

<b>Term</b>	<b>Definition</b>
DFI Read Training MC IF Width	The number of bits used to control the read training interface from the MC perspective. The MC Read training signals are generally fanned out such that a copy of the signal can be sent to each PHY memory data slice.
DFI Read Training PHY IF Width	The number of bits used to control the read training interface from the PHY perspective. The PHY may drive a signal from each memory data slice or combine the signals into a single signal.
DFI Read Training Response Width	The number of bits used to communicate read training status to the MC. The PHY Read Training response may be one bit per memory data slice or one bit per bit on the memory data bus. If this width is the same width as the memory data bus, gate training information should be returned on the lowest bit of each data slice.
DFI Training Interface	Utilized when DFI Training Mode is enabled. The DFI training interface has three operations: gate training, read data eye training, and write leveling. Gate training and read data eye training are referred to collectively as “read training”. The training operation used is determined by the memory type and whether the system is using read signals or write signals.
DFI Write Leveling Delay Width	The number of bits required to communicate write delay information to the PHY.
DFI Write Leveling MC IF Width	The number of bits used to control the write leveling interface from the MC perspective. The MC Write Leveling signals are generally fanned out such that a copy of the signal can be sent to each PHY memory data slice.
DFI Write Leveling PHY IF Width	The number of bits used to control the write leveling interface from the PHY perspective. The PHY may drive a signal from each memory data slice or combine the signals into a single signal.
DFI Write Leveling Response Width	The number of bits used to communicate write leveling status to the MC. The PHY should drive a single bit per memory data slice.
DQ	The bi-directional bus that transfers read and write data to the DRAM.
DQS	The bi-directional data strobe bus transmitted to and from the DRAM.
Frequency Ratio	<p>In a frequency ratio system, the MC and the PHY operate at a common frequency ratio of 1:2 or 1:4; the PHY must be able to accept a command on any and all phases. The frequency ratio depends on the relationship of the reference clocks for the MC and the PHY.</p> <p>Phase-specific signals with a suffix of “_pN” with the phase number N (e.g., <b>dfi_wrdata_pN</b>) replace the matched frequency control, write data, read data and status interface enable signals. Phase-specific signals allow the MC to drive multiple commands in a single clock cycle.</p> <p>Data word-specific signals with a suffix of “_wN” with the DFI data word number N (e.g., <b>dfi_rddata_wN</b>) replace the matched frequency read data interface signals to distinguish how memory words are transferred across the DFI bus.</p> <p>Variable pulse width-specific signals with a suffix of “_aN”, with the PHY clock cycle N (e.g., <b>dfi_alert_n_aN</b>), replace the matched frequency status interface signals to maintain the pulse width during transmission of error signals from the memory system to the PHY.</p> <p>For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional. For more information on frequency ratios, refer to Section 4.8, “Frequency Ratios Across the DFI”.</p> <p>For all signal types, the suffix for phase 0/word 0/clock cycle 0 is optional.</p> <p>For more information on frequency ratios, refer to Section 4.8, “Frequency Ratios Across the DFI”.</p>

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## Glossary

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Term	Definition
Gate Training	An operation utilizing the MPR feature of the DRAM to center the DQS gate in the read data preamble.
Idle	The DFI bus is considered idle when the control interface is not sending any commands and all read and write data has transferred on the DFI bus, reached its destination (DRAM or MC), and the write data transfer has completed on the DRAM bus.
Matched Frequency	In a matched frequency system, the MC and the PHY operate at a common frequency ratio of 1:1.
MC	DDR Memory Controller logic
PHY	DDR Physical Interface logic
PHY Data Word	One phase of read or write data passed between the PHY and the DRAM. A PHY data word is the width of the bus between the PHY and the DRAM and corresponds to a single memory word transfer across the DFI bus. A PHY data word is half the width of a DFI data word.
DFI PHY clock frequency	Defines the period of the clock frequency of the PHY. For matched systems, this is the same as the period of the DFI clock frequency. For frequency ratio systems, the period of the PHY DFI clock frequency must be 1/2 or 1/4 the period of the DFI clock frequency. These clocks must be aligned in phase.
Read data eye training	An operation utilizing the MPR feature of the DRAM to center the DQS in the read data eye.
Read training	May refer to either gate training, data eye training, or both.
Row Selection (RAS)	Row address strobe.
Unit interval (UI)	Half of a data word; the number of DRAM data words in one DRAM burst. NOTE: With DDR DRAM devices, the number of DRAM data words is 2x the number of DFI data words.
Variable pulse width-specific signals	Differentiated with a suffix of “aN”, with the PHY clock cycle N (e.g., <b>dfi_alert_n_aN</b> ), variable pulse width-specific signals replace status interface matched frequency signals to maintain the pulse width during transmission of error signals from the memory system to the PHY.
Write leveling	A feature of the DRAM used to adjust the relationship between the DQS and the DRAM clock.