GSV2011

HDMI2.0 Repeater with TTL/LVDS
Input/Output and Audio Extraction/Insertion

September, 2019

PRODUCT SPECIFICATION

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FIGURES

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Glossary

Term	Definition
DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
I^2S	Integrated Interchip Sound
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
CSC	Color Space Conversion

1 General Information

1.1 General Information

The GSV2011 is a HDMI1.4/2.0 compatible TRX transceiver with LVDS/TTL data bus, and supports HDCP 1.4/2.2. For audio extraction and insertion, GSV2011 can support up to 8-channel I2S/2-channel S/PDIF/TDM.
The HDMI input maximum processing pixel clock frequency is 600MHz which means the video resolution can support up to 4kx2k@60Hz 4:4:4 8-bit. The maximum processing audio sample frequency is 8-channel 192K Hz for non-compression timing.

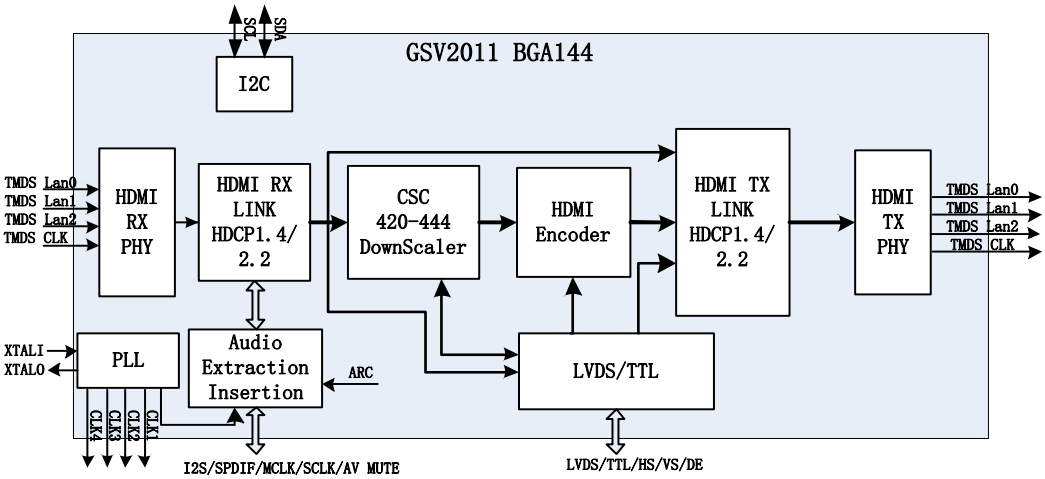


Figure 1. Top Diagram

Internal video processing supports CSC/ Dither/ 420<->444 conversion/ Downscaler/ Deinterlacer/ LVDS and TTL Pin Mapping. Figure 2 is its diagram.

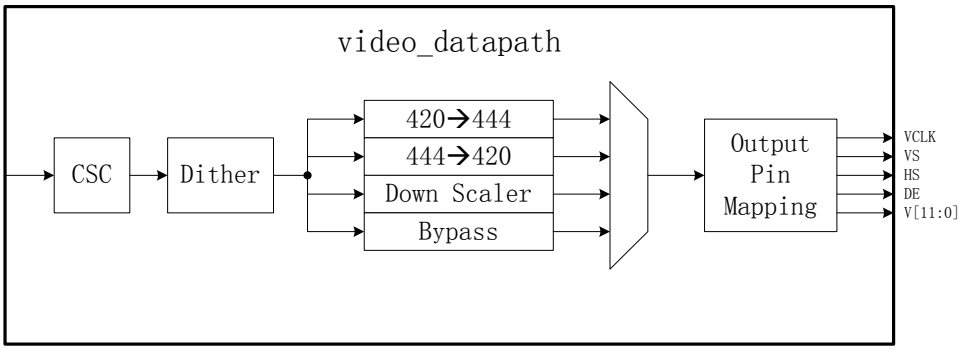


Figure 2. Video Datapath

Audio TTL output pins support audio format listed in Table 1.

Table 1. Supported Audio Format

Packet ID	Packet Type	Sample Frequency or Frame Rate		
		32.0, 44.1, 48.0, 88.2, 96.0, 176.4, and 192.0 kHz	256.0, 352.8, 384.0, 512.0, 705.6, 768.0 kHz	64.0 and 128.0 kHz
0x02	Audio Sample (L-PCM and IEC 61937 compressed formats)	Y	N	Y
0x07	One Bit Audio Sample Packet	Y	N	N
0x08	DST Audio Packet	Y	N	N
0x09	High Bitrate Audio Stream Packet (IEC 61937)	N	Y	N

An internal Clock Generator can be used to generate 4 independent output clocks, which will greatly remove complexity of using dedicated clock device.

1.2 Features

1.2.1 HDMI TRX transceiver

- Compliant with HDMI2.0b, HDMI1.4b
- Compliant with HDCP2.2/2.3 and HDCP1.4
- Data rate up to 18Gbps
- Programmable HDMI Tx output swing, slew-rate, pre-emphasis
- Adaptive receiver equalization
- AC-coupling capable
- UDP bus to support the combination of video/audio/info-frames
- Color Space Converter supports any conversion between different color spaces
- HDR supported (HDR10/HDR12/Dolby Vision/HLG)
- 5V tolerance on DDC/HPD/CEC
- Up to 4 channel clock generators, ranging 25MHz~600MHz

1.2.2 Multi-Port LVDS Transmitter/Receiver

- Bi-directional LVDS, supports video format up to 4K 60 444
- Compatible with series FPGAs' LVDS standard (15 pairs in maximum)
  - Programmable output swing, slew-rate, common voltage and pre-emphasis
  - SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable output phase
  - Data rate up to 1.5Gbps per lane
  - Differential HS/VS/DE available
  - Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Transmitter
  - Programmable output swing , slew-rate , common voltage and pre-emphasis
  - Data rate up to 1.5Gbps per lane

1.2.3 Compatible TTL Transmitter/Receiver

- 48-bit TTL Video Output
  - Programmable drive strength, slew-rate, driver disabled state control
  - SDR/DDR Clock Output with configurable output phase
  - Data rate up to 300Mbps per lane
  - HS/VS/DE available
  - Embedded SAV/EAV mode supported
  - 1.8/2.5/3.3V VCCO compatible.
- 48-bit TTL Video Receiver
  - TTL Schmitt trigger receiver and CMOS receiver selectable
  - SDR/DDR Clock Input available with 0 degree or 90 degree
  - Data rate up to 300Mbps per lane
  - HS/VS/DE available
  - Embedded SAV/EAV mode supported
  - 1.8/2.5/3.3V VCCO compatible.
  -

1.2.4 Audio Input/Output

- SPDIF/I2S/HBR/DSD/TDM Audio Extraction
- SPDIF/I2S/HBR/DSD/TDM Audio Insertion

1.3 Chip Application Modes

1.3.1 HDMI 2.0 TRX with LVDS/TTL output mirroring input

The LVDS/TTL Output are mirrored from input with no internal processing. Downscaler/444-420 converter can be used to guarantee the HDMI Tx has the best 4K/2K compatibility with fixed HDMI Rx input timing.

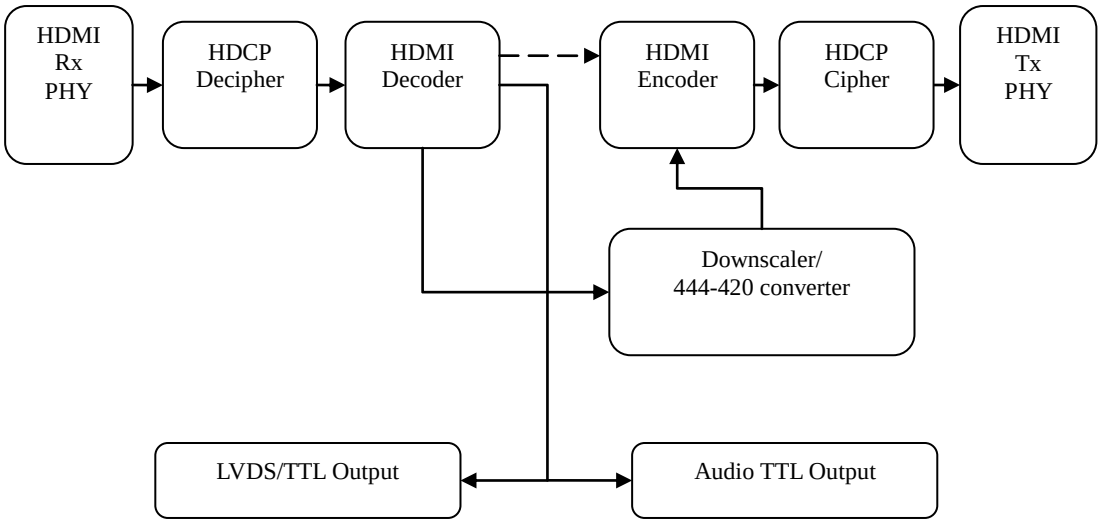


Figure 3. HDMI 2.0 TRX with LVDS/TTL output mirroring input

1.3.2 HDMI 2.0 TRX with LVDS/TTL output using UDP mode

Patented UDP mode is used to combine input video/audio together onto a single universal bus to minimize the pin number.

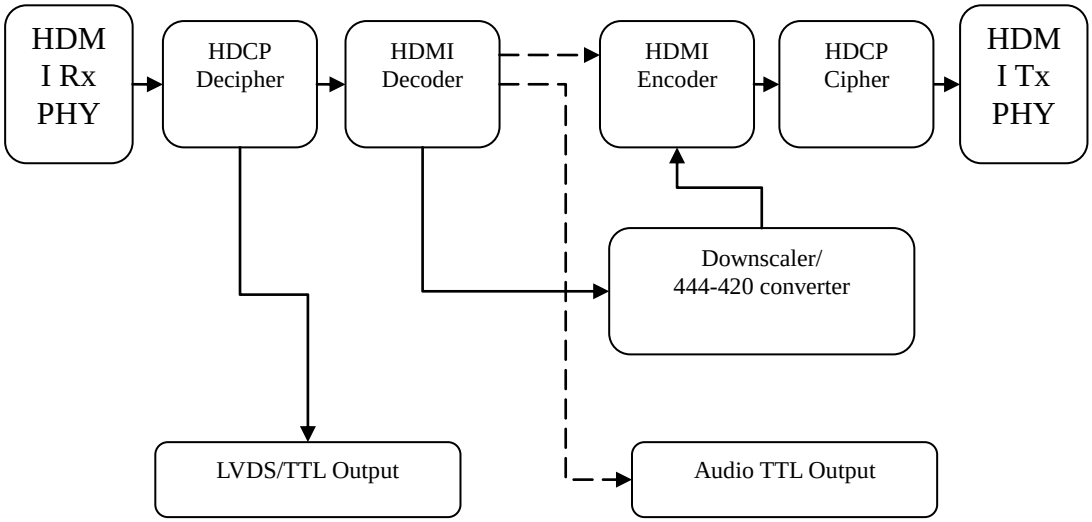


Figure 4. HDMI 2.0 TRX with LVDS/TTL output using UDP mode

1.3.3 HDMI 2.0 TRX with LVDS/TTL output in single color space

Internal IPs could be used to do color space conversion to guarantee the LVDS/TTL output is always in the same color space (either RGB/YCbCr 444/YCbCr422/YCbCr420). If needed, this mode can also downscale all the 4K to 2K for LVDS/TTL Output. This application mode is often used in embedded sync transmission.

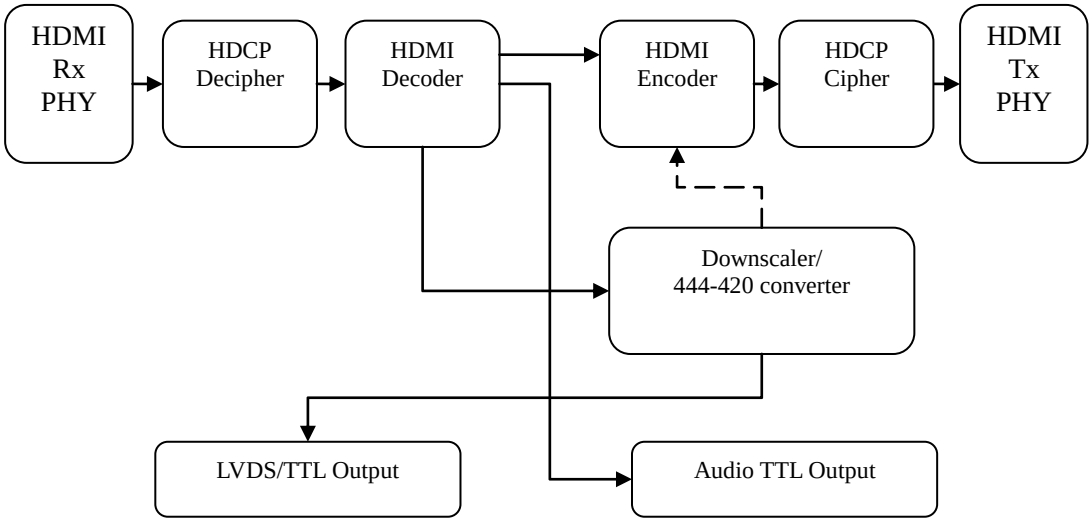


Figure 5. HDMI 2.0 TRX with LVDS/TTL output in single color space

1.3.4 HDMI 2.0 RX with clock generator

When Rx is used to decode input HDMI timing, HDMI Tx PHY can be used to generate 4 different clock outputs.

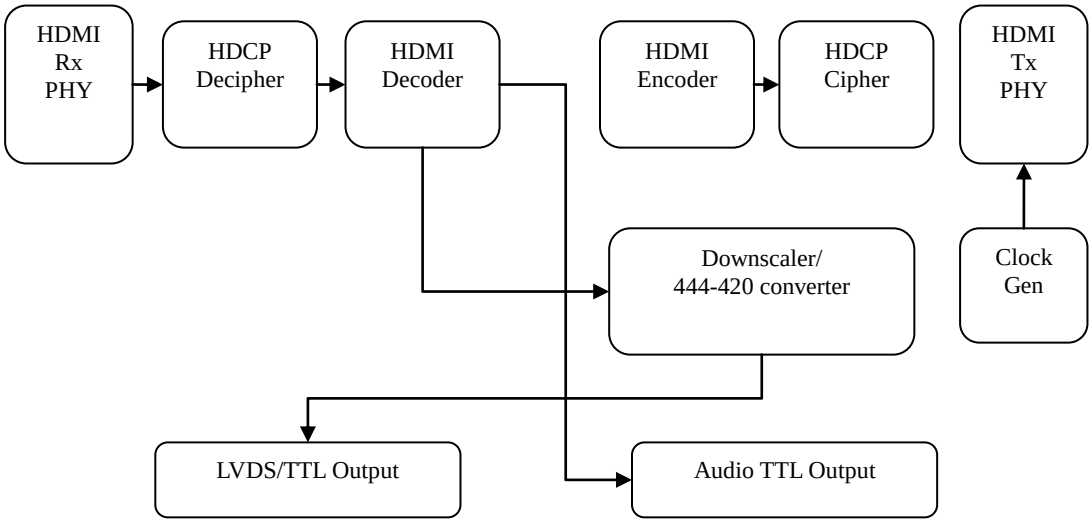


Figure 6. HDMI 2.0 RX with clock generator

1.3.5 HDMI 2.0 TX with LVDS/TTL input

The LVDS/TTL input and Audio TTL input can be combined in HDMI Tx Encoder to generate HDMI 2.0 timing out.

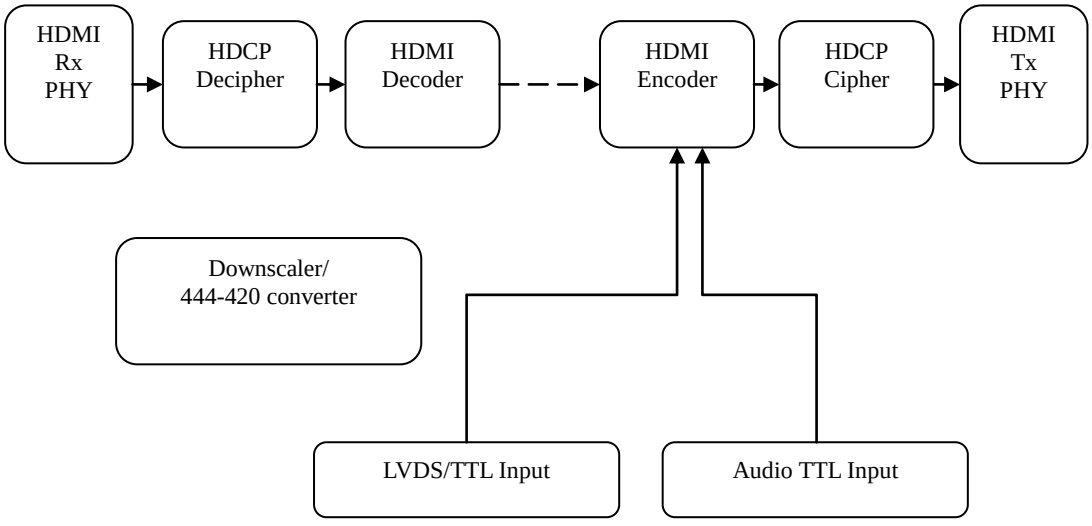


Figure 7. HDMI 2.0 TX with LVDS/TTL input

1.3.6 HDMI 2.0 TX with LVDS/TTL input and CSC

The LVDS/TTL input can convert color space internally before route to HDMI Encoder. In this mode, with different color space from LVDS/TTL input, HDMI Tx

can generate a universal color space.

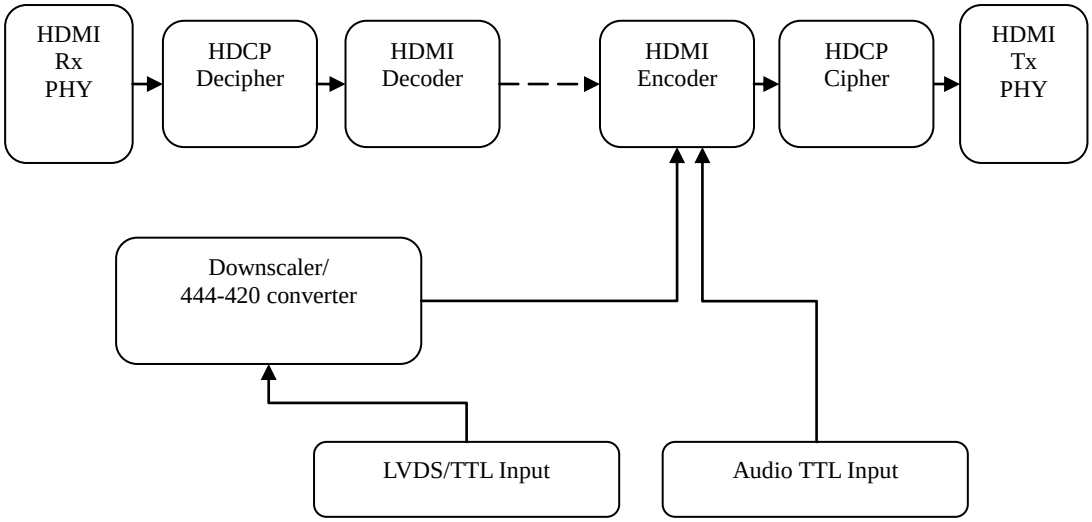


Figure 8. HDMI 2.0 TX with LVDS/TTL input and CSC

1.3.7 HDMI 2.0 TX with LVDS/TTL input using UDP mode

Patented UDP mode is used to drive the input video/audio stream in LVDS/TTL bus to HDMI output to minimize the pin number.

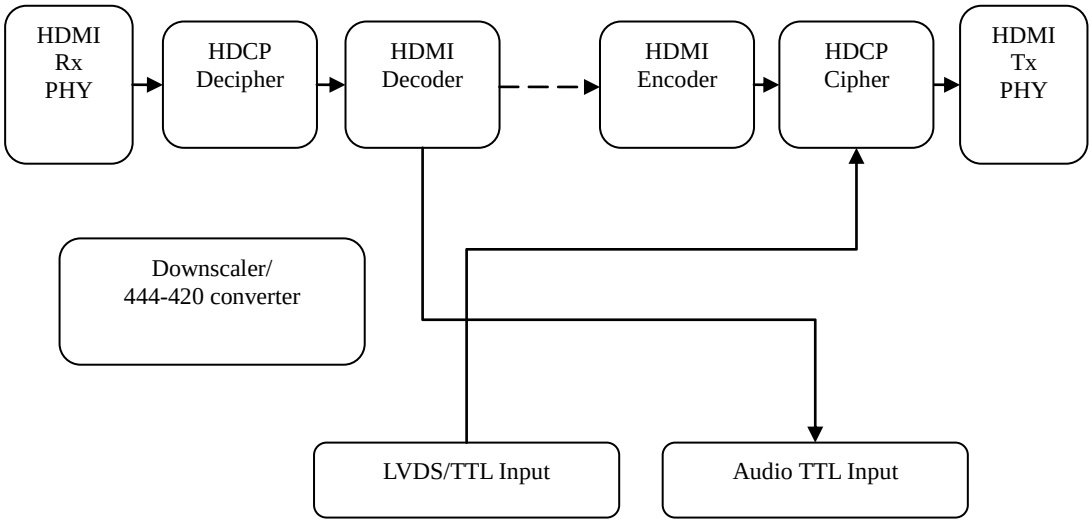


Figure 9. HDMI 2.0 TX with LVDS/TTL input using UDP mode

2 Pin Description

2.1 Pin Diagram

Figure 10. Pin Mapping

2.2 Pin Description

Table 2. Pin Description

Pin Name	Direction	Pin No.	Description
5V Tolerance Pins			
CEC	I/O	D7	5V tolerance CEC PAD
RX_HPD	I/O	D6	RX 5V tolerance HPD PAD
RX_SDA	I/O	D5	RX 5V tolerance DDC SDA PAD
RX_SCL	I	D4	RX 5V tolerance DDC SCL PAD
RX_5V	Power	E4	RX 5V POWER
TX_HPD	I	G4	TX 5V tolerance HPD PAD
TX_SDA	I/O	H4	TX 5V tolerance DDC SDA PAD
TX_SCL	I/O	J4	TX 5V tolerance DDC SCL PAD
TX_UTILITY	I	K4	TX 5V tolerance UTILITY PAD/TXA Audio Return Channel Input

Power/Ground Pins			
TVDD	Power	E3,F3,G3,F4	Analog 3.3V voltage power supply for RX Channel
DVDDIO	Power	F7,F8	Digital 3.3V voltage power supply
VDD1833	Power	H5,H6,H7,H8	LVDS/TTL power supply, 3.3V of LVDS mode and 1.8/2.5/3.3 compatible of TTL mode
RX_AVDD	Power	C5,C6,C7	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	H3,J3,K3	Analog 1.2V voltage power supply for TX Port
PAR_AVDD	Power	K5,K6,K7	Analog 1.2V voltage power supply for LVDS/TTL
DVDD	Power	E7,E8	Digital 1.2V voltage power supply
AVSS	Ground	A2,A4,A6,B4, B6,D1,F1,F2, H1,H2,J5,J6,J7	Analog Ground
OVSS	Ground	G5,G6,G7,G8	LVDS/TTL interface Ground
DVSS	Ground	E5,E6,F5,F6	Digital Ground
RX_PVDD	Power	B8	PLL 1.2V voltage power supply for RX port
RX_PVSS	Ground	A8	PLL Ground for RX port
TX_PVDD	Power	K2	PLL 1.2V voltage power supply for TX port
TX_PVSS	Ground	K1	PLL Ground for TX port
PAR_PVDD	Power	K8	PLL 1.2V voltage power supply for LVDS/TTL
PAR_PVSS	Ground	J8	PLL Ground for LVDS/TTL
MPLL_PVDD	Power	C4	MPLL 1.2V voltage power supply
MPLL_PVSS	Ground	C3	MPLL Ground
TMDS Signal Pins			
RX_CN	I	A7	RX Negative TMDS clock input
RX_CP	I	B7	RX Positive TMDS clock input
RX_0N	I	A5	RX Negative TMDS differential data input [0]
RX_0P	I	B5	RX Negative TMDS differential data input [0]
RX_1N	I	A3	RX Negative TMDS differential data input [1]
RX_1P	I	B3	RX Negative TMDS differential data input [1]
RX_2N	I	A1	RX Negative TMDS differential data input [2]
RX_2P	I	B1	RX Negative TMDS differential data input [2]
TX_CN	O	C1	TX Negative TMDS clock output
TX_CP	O	C2	TX Positive TMDS clock output
TX_0N	O	E1	TX Negative TMDS differential line driver data output [0]
TX_0P	O	E2	TX Positive TMDS differential line driver data output [0]
TX_1N	O	G1	TX Negative TMDS differential line driver data output [1]
TX_1P	O	G2	TX Positive TMDS differential line driver data output [1]
TX_2N	O	J1	TX Negative TMDS differential line driver data output [2]
TX_2P	O	J2	TX Positive TMDS differential line driver data output [2]
LVDS/TTL Signal Pins			
TTL0_LVDS0P	I/O	M1	Video In/Out, TTL Data[0] or Positive LVDS Data[0]
TTL1_LVDS0N	I/O	L1	Video In/Out, TTL Data[1] or Negative LVDS Data[0]
TTL2_LVDS1P	I/O	M2	Video In/Out, TTL Data[2] or Positive LVDS Data[1]
TTL3_LVDS1N	I/O	L2	Video In/Out, TTL Data[3] or Negative LVDS Data[1]
TTL4_LVDS2P	I/O	M3	Video In/Out, TTL Data[4] or Positive LVDS Data[2]
TTL5_LVDS2N	I/O	L3	Video In/Out, TTL Data[5] or Negative LVDS Data[2]
TTL6_LVDS3P	I/O	M4	Video In/Out, TTL Data[6] or Positive LVDS Data[3]
TTL7_LVDS3N	I/O	L4	Video In/Out, TTL Data[7] or Negative LVDS Data[3]
TTL8_LVDS4P	I/O	M5	Video In/Out, TTL Data[8] or Positive LVDS Data[4]
TTL9_LVDS4N	I/O	L5	Video In/Out, TTL Data[9] or Negative LVDS Data[4]
TTL10_LVDS5P	I/O	M6	Video In/Out, TTL Data[10] or Positive LVDS Data[5]
TTL11_LVDS5N	I/O	L6	Video In/Out, TTL Data[11] or Negative LVDS Data[5]

TTL_VS_LVDS_VSP	I/O	M7	Vertical synchronization for Digital Video, TTL VS or Positive LVDS VS
TTL12_LVDS_VSN	I/O	L7	Video In/Out, TTL Data[12] or Negative LVDS VS
TTL_HS_LVDS_HSP	I/O	M8	Horizontal Synchronization for Digital Video, TTLHS or Positive LVDS HS
TTL13_LVDS_HSN	I/O	L8	Video In/Out, TTL Data[13] or Negative LVDS HS
TTL14	I/O	M9	Video In/Out, TTL Data[14]
TTL15	I/O	L9	Video In/Out, TTL Data[15]
TTL16	I/O	M10	Video In/Out, TTL Data[16]
TTL17	I/O	L10	Video In/Out, TTL Data[17]
TTL18	I/O	K9	Video In/Out, TTL Data[18]
TTL19	I/O	J9	Video In/Out, TTL Data[19]
TTL20	I/O	K10	Video In/Out, TTL Data[20]
TTL21	I/O	J10	Video In/Out, TTL Data[21]
TTL_VCLK_LVDSCP	I/O	M12	Video In/Out, TTL Clock or Positive LVDS Clock
TTL22_LVDSCN	I/O	M11	Video In/Out, TTL Data[22] or Negative LVDS Clock
TTL_DE_LVDS_DEP	I/O	L12	Data Enable for Digital Video, TTL DE or Positive LVDS DE
TTL23_LVDS_DEN	I/O	L11	Video In/Out, TTL Data[23] or Negative LVDS DE
TTL24_LVDS6P	I/O	K12	Video In/Out, TTL Data[24] or Positive LVDS Data[6]
TTL25_LVDS6N	I/O	K11	Video In/Out, TTL Data[25] or Negative LVDS Data[6]
TTL26_LVDS7P	I/O	J12	Video In/Out, TTL Data[26] or Positive LVDS Data[7]
TTL27_LVDS7N	I/O	J11	Video In/Out, TTL Data[27] or Negative LVDS Data[7]
TTL28_LVDS8P	I/O	H12	Video In/Out, TTL Data[28] or Positive LVDS Data[8]
TTL29_LVDS8N	I/O	H11	Video In/Out, TTL Data[29] or Negative LVDS Data[8]
TTL30_LVDS9P	I/O	G12	Video In/Out, TTL Data[30] or Positive LVDS Data[9]
TTL31_LVDS9N	I/O	G11	Video In/Out, TTL Data[31] or Negative LVDS Data[9]
TTL32_LVDS10P	I/O	F12	Video In/Out, TTL Data[32] or Positive LVDS Data[10]
TTL33_LVDS10N	I/O	F11	Video In/Out, TTL Data[33] or Negative LVDS Data[10]
TTL34_LVDS11P	I/O	E12	Video In/Out, TTL Data[34] or Positive LVDS Data[11]
TTL35_LVDS11N	I/O	E11	Video In/Out, TTL Data[35] or Negative LVDS Data[11]
TTL36	I/O	D12	Video In/Out, TTL Data[36]
TTL37	I/O	D11	Video In/Out, TTL Data[37]
TTL38	I/O	C12	Video In/Out, TTL Data[38]
TTL39	I/O	C11	Video In/Out, TTL Data[39]
TTL40	I/O	B12	Video In/Out, TTL Data[40]
TTL41	I/O	B11	Video In/Out, TTL Data[41]
TTL42	I/O	A12	Video In/Out, TTL Data[42]
TTL43	I/O	A11	Video In/Out, TTL Data[43]
TTL44	I/O	B10	Video In/Out, TTL Data[44]
TTL45	I/O	A10	Video In/Out, TTL Data[45]
TTL46	I/O	B9	Video In/Out, TTL Data[46]
TTL47	I/O	A9	Video In/Out, TTL Data[47]
Digital pins			
I2C_SDA	I/O	C10	Digital IO for I2C Data
I2C_SCL	I/O	D10	Digital IO for I2C Clock
AUD_D0	I/O	H10	Digital IO PAD for Audio Data0
AUD_D1	I/O	H9	Digital IO PAD for Audio Data1
AUD_D2	I/O	G10	Digital IO PAD for Audio Data2
AUD_D3	I/O	G9	Digital IO PAD for Audio Data3

AUD_D4	I/O	F10	Digital IO PAD for Audio Data4
AUD_D5	I/O	F9	Digital IO PAD for Audio Data5
AUD_SCLK	I/O	E10	Digital IO PAD for Audio SCLK
AUD_MCLK	I/O	E9	Digital IO PAD for Audio MCLK
CSB	I/O	C9	Chip Select Pin.
RESETB	I	D9	Reset Pin
INT	O	C8	Interrupt Output Pin
AVMUTE	O	D8	Avmute Output Pin
REXT400	I/O	B2	External 400 ohm resistor Connected to RX_TVDD
XTALI	I/O	D2	27M Crystal Input
XTALO	I/O	D3	27M Crystal output

3 Electrical Specifications

3.1 LVDS Transmitter

3.1.1 LVDS Transmitter Specification

Table 3. LVDS Driver Specification

Interface Type	Common mode voltage	Differential mode voltage	Max clock frequency	Max data rate per lane
sub-LVDS	900mV	150mV	750MHz	1.5Gbps
LVDS	1.25V	350mV	750MHz	1.5Gbps

3.1.2 LVDS Transmitter Characteristic

Table 4. LVDS Transmitter Characteristic

VCCO Voltage	1.8/2.5/3.3V
Output Current	0.5mA~7.5mA with 0.5mA per step adjustment
Output Swing	● w/o output termination: 50mV~750mV differential swing, 50mV per step ● With 100 ohm (±5%) output termination: 25mV~375mV differential swing, 25mV per step
Common Voltage	800mV~1550mV with 50mV per step adjustment
Termination Impedance	100 ohm (±5%) or off
Output Emphasis	0~-6db de-emphasis factor, -0.5db per/step
Output Slew Rate	4 step slew rate control
Skew Control	0~480ps skew manual control to match PCB skew mismatch (30ps per step)

3.1.3 LVDS Clock Characteristic

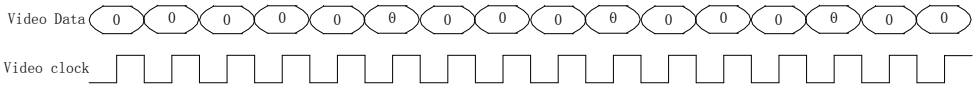
3.1.3.1 Clock Frequency Range

SDR/DDR/xN (N = 1~7) mode supported, max 750MHz per lane

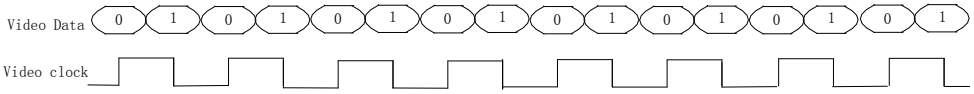
3.1.3.2 Clock Output Phase

Clock output phase selection: Clock edge alignment with data edge or Clock edge alignment with middle of data (default)

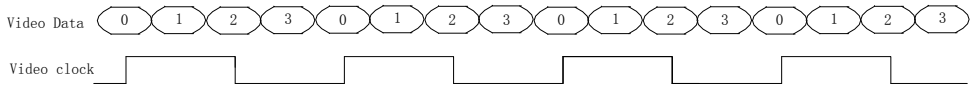
- SDR: Clock rise edge alignment with middle of data



- DDR: Clock rise edge alignment with middle of the first data and Clock fall edge alignment with middle of the second data



- XN: Clock rise edge alignment with middle of the first data



3.2 LVDS Receiver

3.2.1 LVDS Receiver Specification

Table 5. LVDS Receiver Specification

Interface Type	Common mode voltage	Differential mode voltage	Max clock frequency	Max data rate per lane
sub-LVDS	900mV	150mV	750MHz	1.5Gbps
LVDS	1.25V	350mV	750MHz	1.5Gbps

3.2.2 Receiver Characteristic

Table 6. LVDS Receiver Characteristic

Termination Impedance	100 ohm(±5%)
Allowable Input Common Voltage Range	800mV~1350mV
Allowable Input Differential Voltage Range	50mV~1200mV
EQ Character	0~7db boost gain selection @750MHz
Skew Control	● Auto de-skew method to align sample clock and data ● Should be informed input video clock phase (Clock edge alignment with data edge or Clock edge alignment with middle of data)

3.3 TTL Transmitter/Receiver

3.3.1 TTL Transmitter DC Specification

3.3.1.1 VCCO (VDDIO) Voltage

1.8/2.5/3.3V compatible.

3.3.1.2 Driving Strength

Table 7. TTL Driving Strength

Driver Strength	Current Stage	Units
S0	2	mA
S1	4	mA
S2	8	mA
S3	12	mA

3.3.1.3 TTL Output V_{OH}/V_{OL}

Table 8. TTL VOH/VOL

Parameter	Min	Max	Units
V_{OH}	VDDIO-0.4	-	V
V_{OL}	-	0.4	V

3.3.1.4 TTL Output Current

Table 9. TTL Output Current @VDDIO =1.8V

Parameter	Condition	Driver Strength	Min	Typical	Max	Units
IOH	VOH=VDDIO-0.4	S0	3.68	5.62	8.50	mA
		S1	7.37	11.3	17.0	mA
		S2	9.82	15.0	22.7	mA
		S3	13.5	20.6	31.2	mA
IOL	VOL=0.4	S0	4.37	6.87	11.4	mA
		S1	8.74	13.8	22.8	mA
		S2	11.7	18.3	30.4	mA
		S3	16.0	25.2	41.8	mA

Table 10. TTL Output Current @VDDIO =2.5V

Parameter	Condition	Driver Strength	Min	Typical	Max	Units
IOH	VOH=VDDIO-0.4	S0	3.83	5.56	7.90	mA
		S1	5.75	8.34	11.9	mA
		S2	9.58	13.9	19.8	mA
		S3	11.5	16.7	23.7	mA
IOL	VOL=0.4	S0	4.46	6.34	9.72	mA
		S1	6.69	9.52	14.6	mA
		S2	11.1	15.9	24.3	mA
		S3	13.4	19.0	29.2	mA

Table 11. TTL Output Current @VDDIO =3.3V

Parameter	Condition	Driver Strength	Min	Typical	Max	Units
IOH	VOH=VDDIO-0.4	S0	4.93	6.93	9.55	mA
		S1	7.39	10.4	14.3	mA
		S2	12.3	17.3	23.9	mA
		S3	14.8	20.8	28.6	mA
IOL	VOL=0.4	S0	5.52	7.34	10.7	mA
		S1	8.28	11.0	16.1	mA
		S2	13.8	18.3	26.8	mA
		S3	16.6	22.0	32.2	mA

3.3.2 TTL Receiver DC Specification

3.3.2.1 TTL Receiver DC Characteristic

Table 12. TTL Receiver DC Characteristic

Parameter	Description	Min	Typical	Max	Units
VDD	Core voltage	1.2	-	1.32	V
VDDIO	I/O Voltage	2.97	3.3	3.63	V
		2.35	2.5	2.75	V
		1.8	-	1.98	V
Vpad	Voltage at IO	-0.3		VDDIO+0.3	V
VIH	High-level input voltage	0.7*VDDIO		VDDIO+0.3	V
VIL	Low-level input voltage	-0.3		0.3*VDDIO	V

3.3.2.2 TTL Schmitt Receiver Hysteresis

Table 13. TTL Schmitt Receiver Hysteresis

Parameter	Min	Typical	Max	Units
VTR+	0.90	1.04	1.17	V
VTR-	0.36	0.56	0.70	V
VHYS	357	447	570	mV

3.4 TMDS Transmitter

3.4.1 Transmitter DC and AC Specification

Table 14. TMDS DC and AC Characteristics

Item	Value
Single-Ended High Level Voltage Range: Data Channels 0,1,2	AVcc-400mV to AVcc+10mV
Single-Ended Low Level Voltage Range: Data Channels 0,1,2	AVcc-1000mV to AVcc-400mV
Single-Ended High Level Range: Clock Channel	AVcc-400mV to AVcc+10mV
Single-Ended Low Level Voltage Range: Clock Channel	AVcc-1000mV to AVcc-200mV
Single-Ended Swing Voltage: Data Channels 0,1,2	400mV <=Vswing<=600mV
Single-Ended Swing Voltage: Clock Channel	200mV<=Vswing<=600mV

3.4.2 Transmitter Characteristic

3.4.2.1 TMDS Output Current

- Range: 3mA~18mA, 1mA per step;
- Can be increased by 25% and 50%

3.5 Timing Information

3.5.1 Power Up and Reset Timing Diagrams

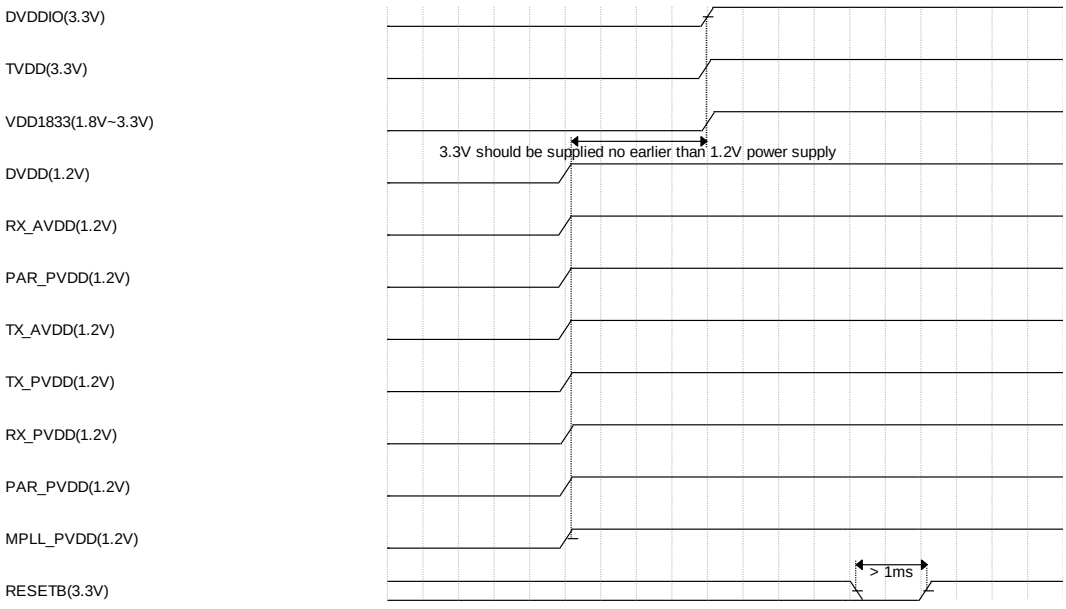


Figure 11. Power Up Sequence

3.5.2 I2C Timing Diagrams

The I2C bus used 8-bit page address and 16-bit register address. For every register, 8-bit data will be accessed.
The I2C write timing is shown below.

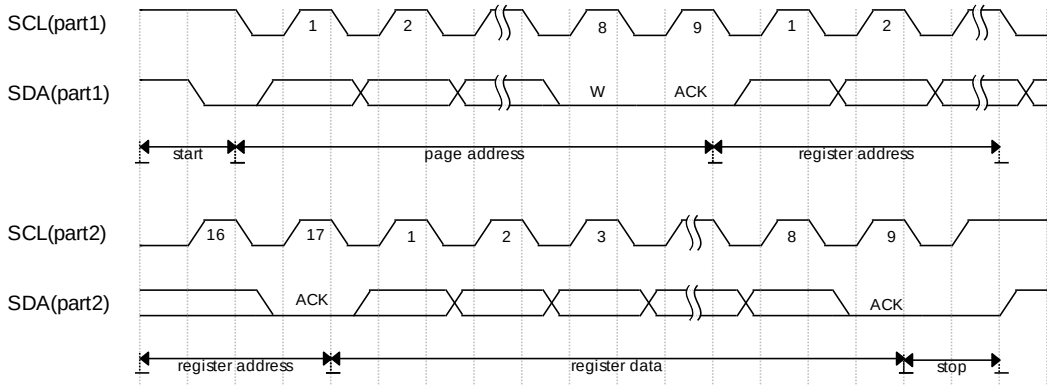


Figure 12. I2C Timing Diagram(Write)

The I2C read timing is shown below.

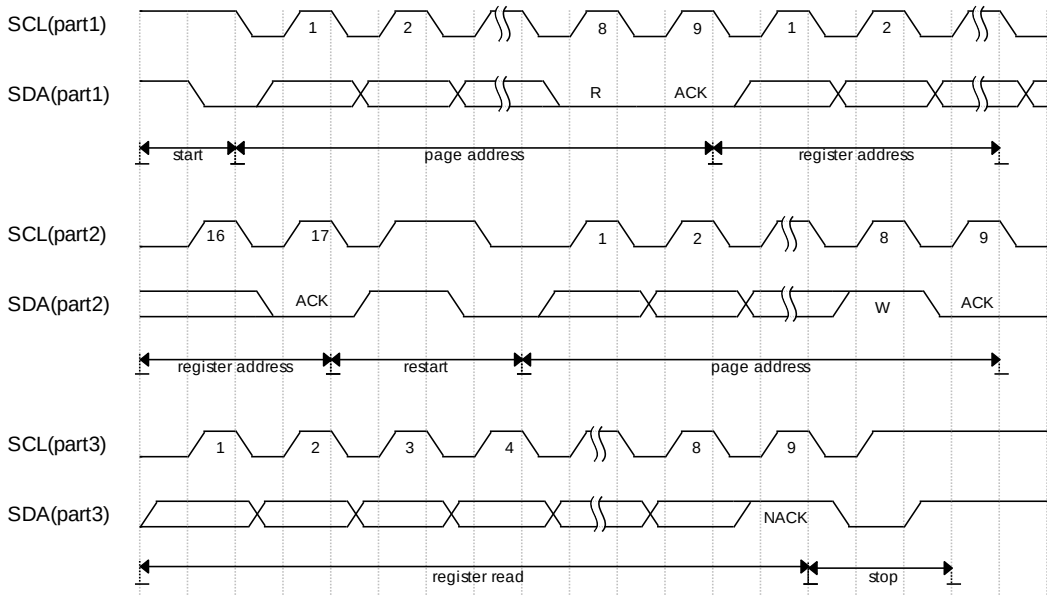


Figure 13. I2C Timing Diagram(Read)

3.6 Operating Conditions

3.6.1 Temperature Conditions

GSV2011's operation temperature range is -20 ℃ to 85 ℃. The maximum junction temperature is at 125 ℃.
GSV2011's junction temperature can be calculated based on Tj = Tc + θJc *PD.
Use Tc and θJc, PD of GSV2011 max power is 2.2W. θJc is 6 ℃/W. Tj can thus be

calculated.
Typical Soldering Profile in GSV2011 Lead-free process is shown below.

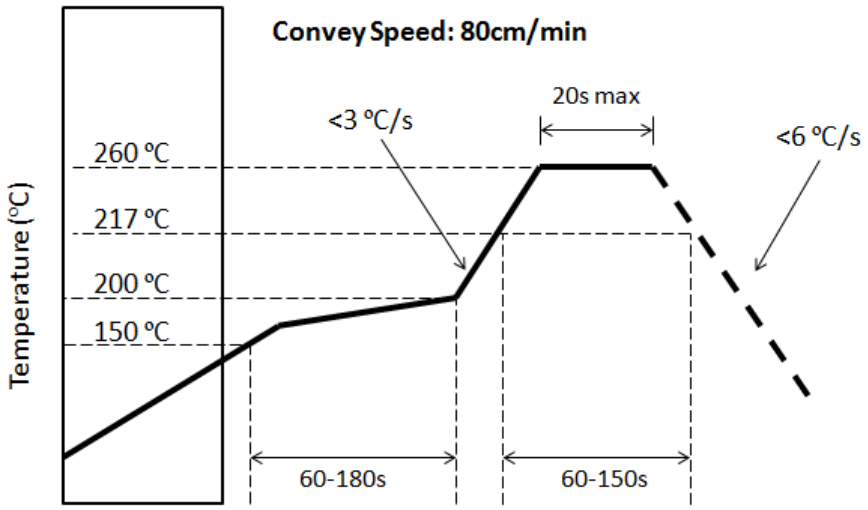


Figure 14. Soldering Profile

3.6.2 Power Conditions

GSV2011's power consumption is related to parallel bus configuration and maximum timing.
A typical 4K60 timing TRX with LVDS is shown below.

Table 15. 4K60 Power Consumption

Power Domain	Symbol	LVDS_OUT_4K60		LVDS_IN_4K60	
		Current(mA)	Consumption（mW）	Current(mA)	Consumption（mW）
1.2V	TX_AVDD	50	60	50	60
	TX_PVDD	40	48	40	48
	RX_AVDD	200	240	-	-
	RX_PVDD	20	24	-	-
	DVDD	305	366	280	336
	MPLL_PVDD	20	24	20	24
	PAR_AVDD	20	24	20	24
	PAR_PVDD	10	12	10	12
	ALL_1V2	665	798	420	504
3.3	TVDD	150	495	50	165
	MPLL	25	82.5	25	82.5
	DVDDIO	<1mA	-	<1mA	-
	VDD1833	250	825	16	52.8
	ALL_3V3	425	1402.5	91	300.3
LVDS_OUT_4K60: HDMI_IN , HDMI_OUT , LVDS_OUT , 4K60with HDCP LVDS_IN_4K60: HDMI_OUT , LVDS_IN , 4K60with HDCP					

A typical 4K30 timing TRX with LVDS is shown below.

Table 16. 4K30 Power Consumption

Power Domain	Symbol	LVDS_OUT_4K30		LVDS_IN_4K30	
		Current(mA)	Consumption（mW）	Current(mA)	Consumption（mW）
1.2V	TX_AVDD	35	42	35	42
	TX_PVDD	40	48	40	48
	RX_AVDD	180	216	-	-
	RX_PVDD	20	24	-	-
	DVDD	195	234	175	210
	MPLL_PVDD	20	24	20	24
	PAR_AVDD	20	24	20	24
	PAR_PVDD	10	12	10	12
	ALL_1V2	520	624	300	360
3.3	TVDD	150	495	50	165
	MPLL	25	82.5	25	82.5
	DVDDIO	<1mA	-	<1mA	-
	VDD1833	150	495	10	33
	ALL_3V3	325	1072.5	85	280.5
LVDS_OUT_4K30: HDMI_IN , HDMI_OUT , LVDS_OUT , 4K30with HDCP LVDS_IN_4K30: HDMI_OUT , LVDS_IN , 4K30with HDCP					

3.6.3 Audio Pin Conditions

GSV2011’s Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

3.6.4 I2C Conditions

GSV2011’s I2C maximum SCL frequency is 400KHz.

3.6.5 ESD Conditions

With RCLAMP0524 as external ESD, Rx TMDS and Tx TMDS can both pass 15kV.

4 Video Output Pin Mapping

4.1 TTL Output Mode

The GSV2011 video TTL output supports multiple modes, the mode register is defined as Table 17. These 3 bytes are the key configuration for different pin mapping types.

Table 17. TTL Mode Register Definition

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Mode CFG 2	N/A	i2c_tx_par_adif_div2_en: Only work when x1/x2/x3 mode 0: not div2 1: div2	i2c_tx_par_multi_pixel_sel[1:0]: 00: 1 pixel per clk 01: 2 pixels per clk 10: 4 pixels per clk 11: Resverd		N/A	i2c_tx_par_clk_ratio[2:0]: Ratio of SDR VCLK/Pixel DIV CLK 000/001: 1 clk 1 pixel = 1x 010: 2 clk 1 pixel = 2x 011: 3 clk 1 pixel = 3x … 111: 7 clk 1 pixel = 7x		
Mode CFG 1	i2c_tx_par_panel_en: 0: Disable 1: Enable	i2c_tx_par_panel_sel: 0: VESA 1: JEIDA	i2c_tx_par_sub_mode[1:0]: 00: Mode A 01: Mode B 10: Mode C 11: Mode D		N/A	i2c_tx_par_422_en: 0: RGB 4:4:4 /CrYCb 4:4:4 /CrYCb 4:2:0 1: 4:2:2	i2c_tx_par_bit_width[1:0]: 00: 6 bits 01: 8 bits 10:10 bits 11:12 bits	
Mode CFG 0	i2c_tx_par_ttl_lvds_sel: 0: TTL 1: LVDS	[6]:i2c_tx_par_his_mode_en [5]:i2c_tx_par_udp_mode_en [4]:i2c_tx_par_sync_mode bit[6:4]: 1XX: HIS mode 01X: UDP mode 001: ITU Embedded Syncs 000: Separate Syncs			N/A	i2c_tx_par_fixed_high_phy_clk_en: 0: Normal 1: Fixed 1.2 Gbps	i2c_tx_par_vclk_divn_en: 0: div 1 1: div N	i2c_tx_par_vclk_ddr_en: 0: SDR 1: DDR

The GSV2011 TTL mode supports video output format modes are listed in Table 18.

- All modes support both SDR and DDR
- All 4:2:2 modes support both separate syncs and embedded syncs (BT.1120, BT.656)

Table 18. TTL Output Modes

Color Space	Video Format	Bit Width	HS/VS	Sampling	VCLK/Pixel_CLK
RGB	4:4:4	24/30/36	Separate	SDR	1x
				DDR	0.5x
		48	Separate	SDR	0.5x
				DDR	0.25x
YCbCr	4:4:4	24/30/36	Separate	SDR	1x
				DDR	0.5x
		48	Separate	SDR	0.5x
				DDR	0.25x
	4:2:2	16/20/24	Separate	SDR	1x
				DDR	0.5x
			Embedded	SDR	1x
				DDR	0.5x
		8/10/12	Separate	SDR	2x
				DDR	1x
			Embedded	SDR	2x
				DDR	1x
		32/40/48	Separate	SDR	0.5x
				DDR	0.25x
			Embedded	SDR	0.5x
				DDR	0.25x

4.1.1 Single Pixel Mode

4.1.1.1 YCbCr/RGB 4:4:4 Mode

Table 19. Single Pixel Mode YCbCr/RGB 4:4:4 Pin Mapping

Mode CFG 2	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Mode CFG 1	0x11	0x01	0x02	0x03	0x13	0x11	0x01	0x02	0x03	0x13
Mode CFG 0										
Color Space	CrYCb					RGB				
Tag	24-Bit 4:4:4 Mode B	24-Bit 4:4:4 Mode A	30-Bit 4:4:4	36-Bit 4:4:4 Mode A	36-Bit 4:4:4 Mode B	24-Bit 4:4:4 Mode B	24-Bit 4:4:4 Mode A	30-Bit 4:4:4	36-Bit 4:4:4 Mode A	36-Bit 4:4:4 Mode B
Standard										
SDR Clock Ratio	1x	1x	1x	1x	1x	1x	1x	1x	1x	1x
DDR Clock Ratio	0.5x	0.5x	0.5x	0.5x	0.5x	0.5x	0.5x	0.5x	0.5x	0.5x
PIN NAME										
V35		Cr7	Cr9	Cr11	Cr9		R7	R9	R11	R9
V34		Cr6	Cr8	Cr10	Cr8		R6	R8	R10	R8
V33		Cr5	Cr7	Cr9	Cr7		R5	R7	R9	R7
V32		Cr4	Cr6	Cr8	Cr6		R4	R6	R8	R6
V31		Cr3	Cr5	Cr7	Cr5		R3	R5	R7	R5
V30		Cr2	Cr4	Cr6	Cr4		R2	R4	R6	R4
V29		Cr1	Cr3	Cr5	Cr3		R1	R3	R5	R3
V28		Cr0	Cr2	Cr4	Cr2		R0	R2	R4	R2
V27		Z	Cr1	Cr3	Cr1		Z	R1	R3	R1
V26		Z	Cr0	Cr2	Cr0		Z	R0	R2	R0
V25		Z	Z	Cr1	Y7		Z	Z	R1	G7
V24		Z	Z	Cr0	Y6		Z	Z	R0	G6
V23	Cr7	Y7	Y9	Y11	Y5	R7	G7	G9	G11	G5
V22	Cr6	Y6	Y8	Y10	Y4	R6	G6	G8	G10	G4
V21	Cr5	Y5	Y7	Y9	Y3	R5	G5	G7	G9	G3
V20	Cr4	Y4	Y6	Y8	Y2	R4	G4	G6	G8	G2
V19	Cr3	Y3	Y5	Y7	Y1	R3	G3	G5	G7	G1
V18	Cr2	Y2	Y4	Y6	Y0	R2	G2	G4	G6	G0
V17	Cr1	Y1	Y3	Y5	Cb11	R1	G1	G3	G5	B11
V16	Cr0	Y0	Y2	Y4	Cb10	R0	G0	G2	G4	B10
V15	Y7	Z	Y1	Y3	Cb9	G7	Z	G1	G3	B9
V14	Y6	Z	Y0	Y2	Cb8	G6	Z	G0	G2	B8
V13	Y5	Z	Z	Y1	Y11	G5	Z	Z	G1	G11
V12	Y4	Z	Z	Y0	Y10	G4	Z	Z	G0	G10
V11	Y3	Cb7	Cb9	Cb11	Cb7	G3	B7	B9	B11	B7
V10	Y2	Cb6	Cb8	Cb10	Cb6	G2	B6	B8	B10	B6
V9	Y1	Cb5	Cb7	Cb9	Cb5	G1	B5	B7	B9	B5
V8	Y0	Cb4	Cb6	Cb8	Cb4	G0	B4	B6	B8	B4
V7	Cb7	Cb3	Cb5	Cb7	Cb3	B7	B3	B5	B7	B3
V6	Cb6	Cb2	Cb4	Cb6	Cb2	B6	B2	B4	B6	B2
V5	Cb5	Cb1	Cb3	Cb5	Cb1	B5	B1	B3	B5	B1
V4	Cb4	Cb0	Cb2	Cb4	Cb0	B4	B0	B2	B4	B0
V3	Cb3	Z	Cb1	Cb3	Cr11	B3	Z	B1	B3	R11
V2	Cb2	Z	Cb0	Cb2	Cr10	B2	Z	B0	B2	R10
V1	Cb1	Z	Z	Cb1	Y9	B1	Z	Z	B1	G9
V0	Cb0	Z	Z	Cb0	Y8	B0	Z	Z	B0	G8
VS	VS	VS	VS	VS	VS	VS	VS	VS	VS	VS
HS	HS	HS	HS	HS	HS	HS	HS	HS	HS	HS
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

Figure 15 shows Mode CFG[2:1] =0x01_03 36-bits YCbCr 4:4:4 detail timing, 24/30-bits just drop 2/4 LSBs of each channel. RGB 4:4:4 is similar as YCbCr 4:4:4 with a mapping of Cr->R, Y->G, Cb->B.

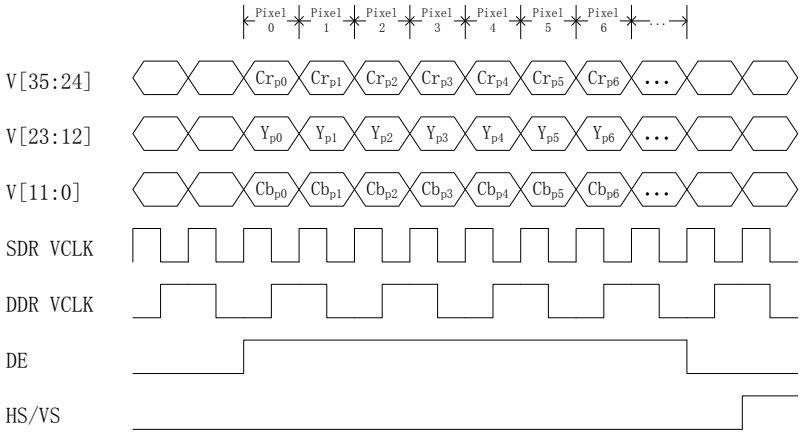


Figure 15. 36-bits YCbCr 4:4:4 Timing Diagram

4.1.1.2 YCbCr 4:2:2 BT.1120 Mode

Table 20. Single Pixel Mode YCbCr 4:2:2 BT.1120 Pin Mapping

Mode CFG 2	0x01	0x01	0x01	0x01	0x01	0x01
Mode CFG 1	0x15	0x05	0x06	0x07	0x17	0x27
Mode CFG 0						
Color Space	CrYCb					
Tag	16-Bit 4:2:2 Mode B	16-Bit 4:2:2 Mode A	20-Bit 4:2:2	24-Bit 4:2:2 Mode A	24-Bit 4:2:2 Mode B	24-Bit 4:2:2 Mode C
Standard	BT. 1120	BT. 1120	BT. 1120	BT. 1120	BT. 1120	BT. 1120
SDR Clock Ratio	1x	1x	1x	1x	1x	1x
DDR Clock Ratio	0. 5x	0. 5x	0. 5x	0. 5x	0. 5x	0. 5x
PIN NAME						
V35					Z	Y3
V34					Z	Y2
V33					C1	Y1
V32					C0	Y0
V31					Z	C3
V30					Z	C2
V29					Y1	C1
V28					Y0	C0
V27					Z	Z
V26					Z	Z
V25					Z	Z
V24					Z	Z
V23		Y7	Y9	Y11	Y11	Y11
V22		Y6	Y8	Y10	Y10	Y10
V21		Y5	Y7	Y9	Y9	Y9
V20		Y4	Y6	Y8	Y8	Y8
V19		Y3	Y5	Y7	Y7	Y7
V18		Y2	Y4	Y6	Y6	Y6
V17	Z	Y1	Y3	Y5	Y5	Y5
V16	Z	Y0	Y2	Y4	Y4	Y4
V15	Y7	Z	Y1	Y3	Y3	Z
V14	Y6	Z	Y0	Y2	Y2	Z
V13	Y5	Z	Z	Y1	Z	Z
V12	Y4	Z	Z	Y0	Z	Z
V11	Y3	C7	C9	C11	C11	C11
V10	Y2	C6	C8	C10	C10	C10
V9	Y1	C5	C7	C9	C9	C9
V8	Y0	C4	C6	C8	C8	C8
V7	C7	C3	C5	C7	C7	C7
V6	C6	C2	C4	C6	C6	C6
V5	C5	C1	C3	C5	C5	C5
V4	C4	C0	C2	C4	C4	C4
V3	C3	Z	C1	C3	C3	Z
V2	C2	Z	C0	C2	C2	Z
V1	C1	Z	Z	C1	Z	Z
V0	C0	Z	Z	C0	Z	Z
VS	VS/Embedded	VS/Embedded	VS/Embedded	VS/Embedded	VS/Embedded	VS/Embedded
HS	HS/Embedded	HS/Embedded	HS/Embedded	HS/Embedded	HS/Embedded	HS/Embedded
DE	DE/Embedded	DE/Embedded	DE/Embedded	DE/Embedded	DE/Embedded	DE/Embedded

Figure 16 ~ Figure 18 show the detail timing of 24-bits YCbCr 4:2:2. 16/20-bits YCbCr 4:2:2 is similar as 24-bits, just drop 4/2 LSBs.

4.1.1.2.1 Separate Sync

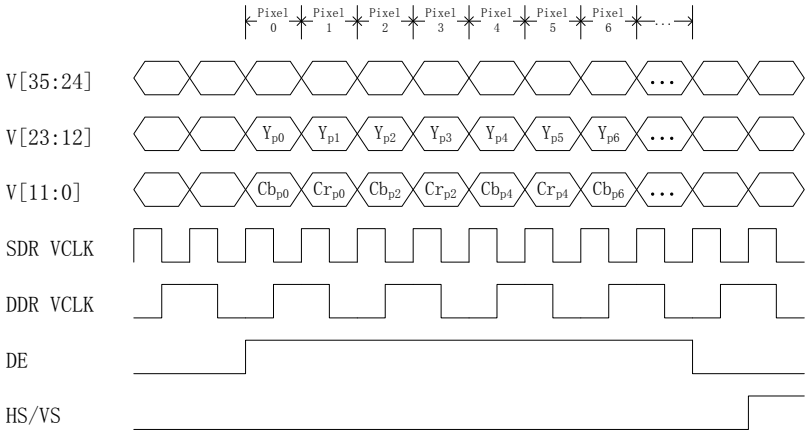


Figure 16. 24-bits YCbCr 4:2:2 BT.1120 Separate Sync Timing Diagram

4.1.1.2.2 Embedded Sync

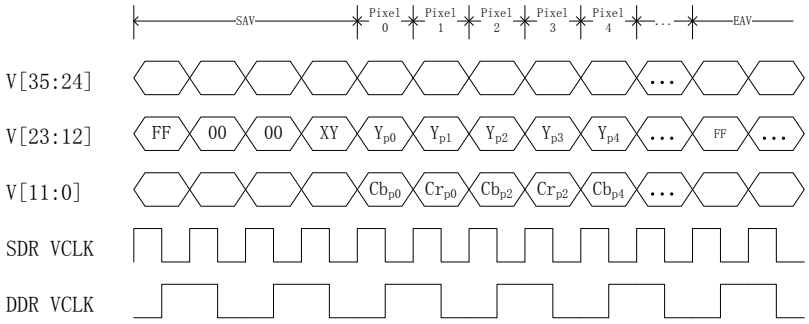


Figure 17. 24-bits YCbCr 4:2:2 BT.1120 Embedded Sync Timing Diagram

4.1.1.2.3 BTA-T1004

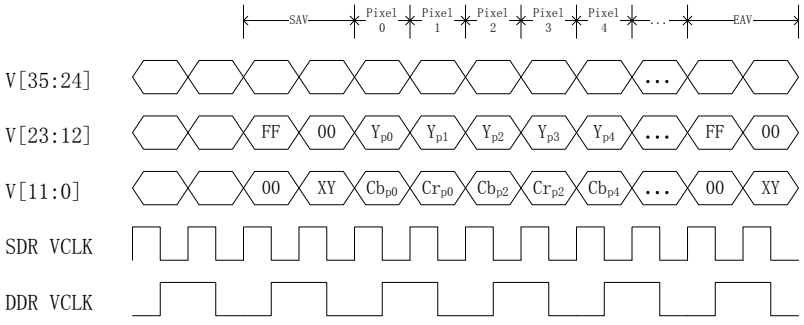


Figure 18. 24-bits YCbCr 4:2:2 BTA-T1004 Embedded Sync Timing Diagram

4.1.1.3 YCbCr 4:2:2 BT.656 Mode

Table 21. Single Pixel Mode YCbCr 4:2:2 BT.656 Pin Mapping

Mode CFG 2	0x02		0x02		0x02		0x02		0x02	
Mode CFG 1	0x05		0x06		0x07		0x17		0x27	
Mode CFG 0										
Color Space										
Tag	8-Bit 4:2:2		10-Bit 4:2:2		12-Bit 4:2:2 Mode A		12-Bit 4:2:2 Mode B		12-Bit 4:2:2 Mode C	
Standard	BT. 656		BT. 656		BT. 656		BT. 656		BT. 656	
SDR Clock Ratio	2x		2x		2x		2x		2x	
DDR Clock Ratio	1x		1x		1x		1x		1x	
PIN NAME	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
V23									C3	Y3
V22									C2	Y2
V21									C1	Y1
V20									C0	Y0
V19									Z	Z
V18									Z	Z
V17							C1	Y1	Z	Z
V16							C0	Y0	Z	Z
V15							Z	Z	Z	Z
V14							Z	Z	Z	Z
V13							Z	Z	Z	Z
V12							Z	Z	Z	Z
V11	C7	Y7	C9	Y9	C11	Y11	C11	Y11	C11	Y11
V10	C6	Y6	C8	Y8	C10	Y10	C10	Y10	C10	Y10
V9	C5	Y5	C7	Y7	C9	Y9	C9	Y9	C9	Y9
V8	C4	Y4	C6	Y6	C8	Y8	C8	Y8	C8	Y8
V7	C3	Y3	C5	Y5	C7	Y7	C7	Y7	C7	Y7
V6	C2	Y2	C4	Y4	C6	Y6	C6	Y6	C6	Y6
V5	C1	Y1	C3	Y3	C5	Y5	C5	Y5	C5	Y5
V4	C0	Y0	C2	Y2	C4	Y4	C4	Y4	C4	Y4
V3	Z	Z	C1	Y1	C3	Y3	C3	Y3	Z	Z
V2	Z	Z	C0	Y0	C2	Y2	C2	Y2	Z	Z
V1	Z	Z	Z	Z	C1	Y1	Z	Z	Z	Z
V0	Z	Z	Z	Z	C0	Y0	Z	Z	Z	Z
VS	VS/Embedded		VS/Embedded		VS/Embedded		VS/Embedded		VS/Embedded	
HS	HS/Embedded		HS/Embedded		HS/Embedded		HS/Embedded		HS/Embedded	
DE	DE/Embedded		DE/Embedded		DE/Embedded		DE/Embedded		DE/Embedded	

Figure 19 ~ Figure 20 show the detail timing of 12-bits YCbCr 4:2:2. 8/10-bits YCbCr 4:2:2 is similar as 12-bits, just drop 4/2 LSBs.

4.1.1.3.1 Separate Syncs

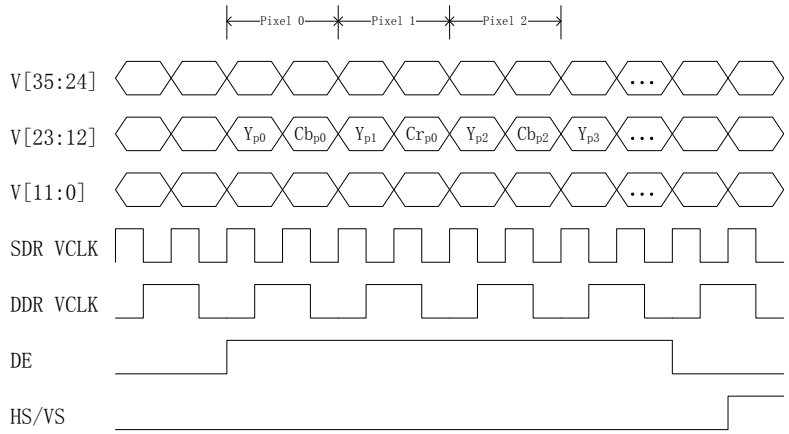


Figure 19. 12-bits YCbCr 4:2:2 BT.656 Separate Sync Timing Diagram

4.1.1.3.2 Embedded Syncs

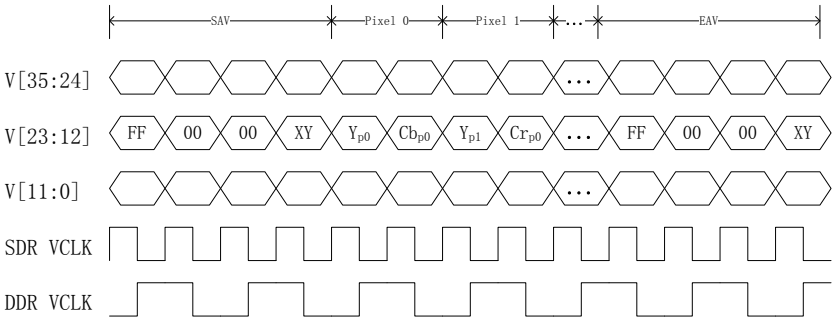


Figure 20. 12-bits YCbCr 4:2:2 BT.656 Embeded Syncs Timing Diagram

4.1.2 Dual Pixel Mode

Dual pixels can be outputted on GSV2011 48 TTL pins, the max data rate can be up to 24-bits@600Mbps.

4.1.2.1 YCbCr/RGB 4:4:4 Mode

Table 22. Dual Pixel Mode YCbCr/RGB 4:4:4 Pin Mapping

Mode CFG 2	0x11	0x11	Mode CFG 2	0x11	0x11
Mode CFG 1	0x01	0x01	Mode CFG 1	0x01	0x01
Mode CFG 0			Mode CFG 0		
Color Space	**CrYCb**	**RGB**	Color Space	**CrYCb**	**RGB**
Tag	48-Bit 4:4:4 Mode A	48-Bit 4:4:4 Mode A	Tag	48-Bit 4:4:4 Mode A	48-Bit 4:4:4 Mode A
Standard			Standard		
SDR Clock Ratio	0.5x	0.5x	SDR Clock Ratio	0.5x	0.5x
DDR Clock Ratio	0.25x	0.25x	DDR Clock Ratio	0.25x	0.25x
PIN NAME			PIN NAME		
V47	P1.Cr7	P1.R7	V23	P0.Cr7	P0.R7
V46	P1.Cr6	P1.R6	V22	P0.Cr6	P0.R6
V45	P1.Cr5	P1.R5	V21	P0.Cr5	P0.R5
V44	P1.Cr4	P1.R4	V20	P0.Cr4	P0.R4
V43	P1.Cr3	P1.R3	V19	P0.Cr3	P0.R3
V42	P1.Cr2	P1.R2	V18	P0.Cr2	P0.R2
V41	P1.Cr1	P1.R1	V17	P0.Cr1	P0.R1
V40	P1.Cr0	P1.R0	V16	P0.Cr0	P0.R0
V39	P1.Y7	P1.G7	V15	P0.Y7	P0.G7
V38	P1.Y6	P1.G6	V14	P0.Y6	P0.G6
V37	P1.Y5	P1.G5	V13	P0.Y5	P0.G5
V36	P1.Y4	P1.G4	V12	P0.Y4	P0.G4
V35	P1.Y3	P1.G3	V11	P0.Y3	P0.G3
V34	P1.Y2	P1.G2	V10	P0.Y2	P0.G2
V33	P1.Y1	P1.G1	V9	P0.Y1	P0.G1
V32	P1.Y0	P1.G0	V8	P0.Y0	P0.G0
V31	P1.Cb7	P1.B7	V7	P0.Cb7	P0.B7
V30	P1.Cb6	P1.B6	V6	P0.Cb6	P0.B6
V29	P1.Cb5	P1.B5	V5	P0.Cb5	P0.B5
V28	P1.Cb4	P1.B4	V4	P0.Cb4	P0.B4
V27	P1.Cb3	P1.B3	V3	P0.Cb3	P0.B3
V26	P1.Cb2	P1.B2	V2	P0.Cb2	P0.B2
V25	P1.Cb1	P1.B1	V1	P0.Cb1	P0.B1
V24	P1.Cb0	P1.B0	V0	P0.Cb0	P0.B0
			VS	VS	VS
			HS	HS	HS
			DE	DE	DE

Table 24 shows the detail timing of Mode CFG[2:1]=0x11_01 48-bits YCbCr 4:4:4, it uses V[47:0].

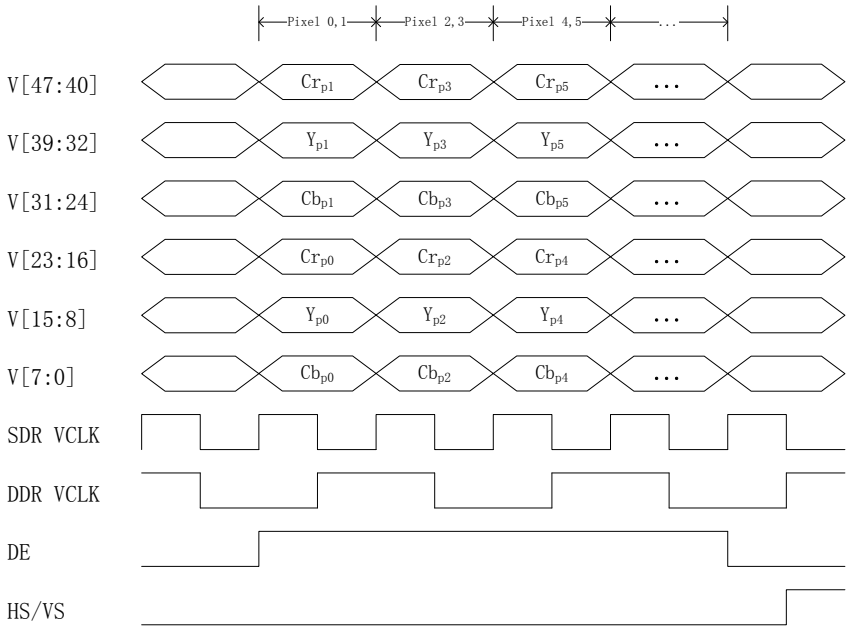


Figure 21. 48-bits YCbCr 4:4:4 Timing Diagram

4.1.2.2 YCbCr 4:2:2 Mode

Table 23. Dual Pixel Mode YCbCr 4:2:2 Pin Mapping[V47:V24]

Mode CFG 2	0x11	0x11	0x11	0x11
Mode CFG 1	0x15	0x05	0x06	0x07
Mode CFG 0				
Color Space	CrYCb			
Tag	32-Bit 4:2:2 Mode B	32-Bit 4:2:2 Mode A	40-Bit 4:2:2	48-Bit 4:2:2
Standard				
SDR Clock Ratio	0.5x	0.5x	0.5x	0.5x
DDR Clock Ratio	0.25x	0.25x	0.25x	0.25x
PIN NAME				
V47		P1.Y7	P1.Y9	P1.Y11
V46		P1.Y6	P1.Y8	P1.Y10
V45		P1.Y5	P1.Y7	P1.Y9
V44		P1.Y4	P1.Y6	P1.Y8
V43		P1.Y3	P1.Y5	P1.Y7
V42		P1.Y2	P1.Y4	P1.Y6
V41		P1.Y1	P1.Y3	P1.Y5
V40		P1.Y0	P1.Y2	P1.Y4
V39		Z	P1.Y1	P1.Y3
V38		Z	P1.Y0	P1.Y2
V37		Z	Z	P1.Y1
V36		Z	Z	P1.Y0
V35	Z	P1.C7	P1.C9	P1.C11
V34	Z	P1.C6	P1.C8	P1.C10
V33	Z	P1.C5	P1.C7	P1.C9
V32	Z	P1.C4	P1.C6	P1.C8
V31	P1.Y7	P1.C3	P1.C5	P1.C7
V30	P1.Y6	P1.C2	P1.C4	P1.C6
V29	P1.Y5	P1.C1	P1.C3	P1.C5
V28	P1.Y4	P1.C0	P1.C2	P1.C4
V27	P1.Y3	Z	P1.C1	P1.C3
V26	P1.Y2	Z	P1.C0	P1.C2
V25	P1.Y1	Z	Z	P1.C1
V24	P1.Y0	Z	Z	P1.C0

Table 24. Dual Pixel Mode YCbCr 4:2:2 Pin Mapping[V23:V0]

Mode CFG 2	0x11	0x11	0x11	0x11
Mode CFG 1	0x15	0x05	0x06	0x07
Mode CFG 0				
Color Space	CrYCb			
Tag	32-Bit 4:2:2 Mode B	32-Bit 4:2:2 Mode A	40-Bit 4:2:2	48-Bit 4:2:2
Standard				
SDR Clock Ratio	0.5x	0.5x	0.5x	0.5x
DDR Clock Ratio	0.25x	0.25x	0.25x	0.25x
PIN NAME				
V23	P1.C7	P0.Y7	P0.Y9	P0.Y11
V22	P1.C6	P0.Y6	P0.Y8	P0.Y10
V21	P1.C5	P0.Y5	P0.Y7	P0.Y9
V20	P1.C4	P0.Y4	P0.Y6	P0.Y8
V19	P1.C3	P0.Y3	P0.Y5	P0.Y7
V18	P1.C2	P0.Y2	P0.Y4	P0.Y6
V17	P1.C1	P0.Y1	P0.Y3	P0.Y5
V16	P1.C0	P0.Y0	P0.Y2	P0.Y4
V15	P0.Y7	Z	P0.Y1	P0.Y3
V14	P0.Y6	Z	P0.Y0	P0.Y2
V13	P0.Y5	Z	Z	P0.Y1
V12	P0.Y4	Z	Z	P0.Y0
V11	P0.Y3	P0.C7	P0.C9	P0.C11
V10	P0.Y2	P0.C6	P0.C8	P0.C10
V9	P0.Y1	P0.C5	P0.C7	P0.C9
V8	P0.Y0	P0.C4	P0.C6	P0.C8
V7	P0.C7	P0.C3	P0.C5	P0.C7
V6	P0.C6	P0.C2	P0.C4	P0.C6
V5	P0.C5	P0.C1	P0.C3	P0.C5
V4	P0.C4	P0.C0	P0.C2	P0.C4
V3	P0.C3	Z	P0.C1	P0.C3
V2	P0.C2	Z	P0.C0	P0.C2
V1	P0.C1	Z	Z	P0.C1
V0	P0.C0	Z	Z	P0.C0
VS	VS/Embedded	VS/Embedded	VS/Embedded	VS/Embedded
HS	HS/Embedded	HS/Embedded	HS/Embedded	HS/Embedded
DE	DE/Embedded	DE/Embedded	DE/Embedded	DE/Embedded

Figure 22 ~ Figure 25 show the detail timing of Mode CFG[2:1]=0x11_15 32-bits YCbCr 4:2:2 mode A and Mode CFG[2:1]=0x11_07 48-bits YCbCr 4:2:2, in dual pixel mode, embedded syncs are supported.

4.1.2.2.1 Separate Syncs

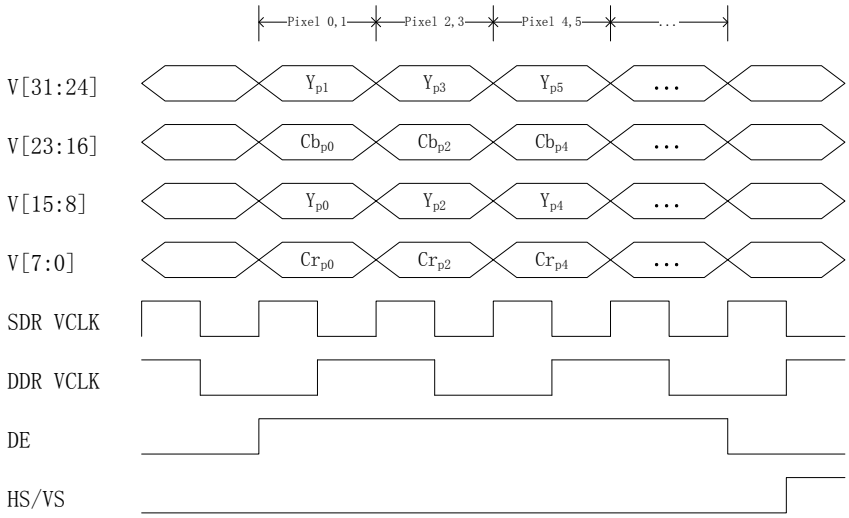


Figure 22. 32-bits YCbCr 4:2:2 Separate Syncs Timing Diagram

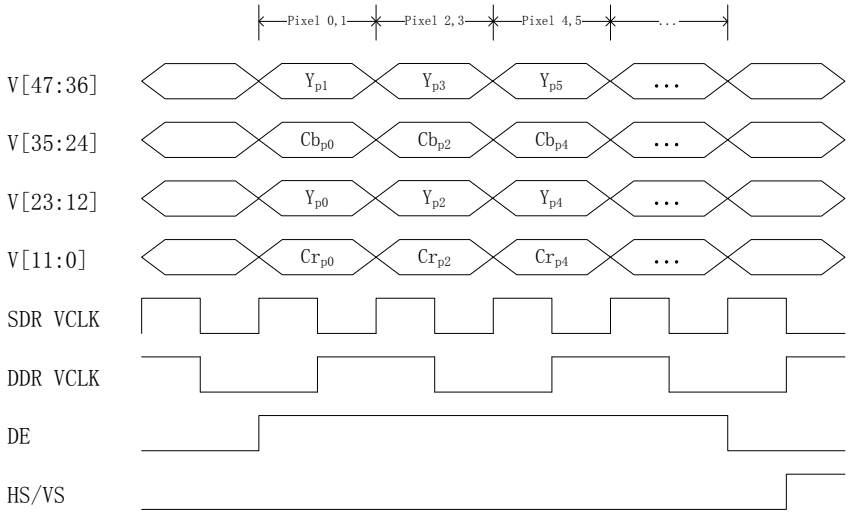


Figure 23. 48-bits YCbCr 4:2:2 Separate Syncs Timing Diagram

4.1.2.2.2 Embedded Syncs

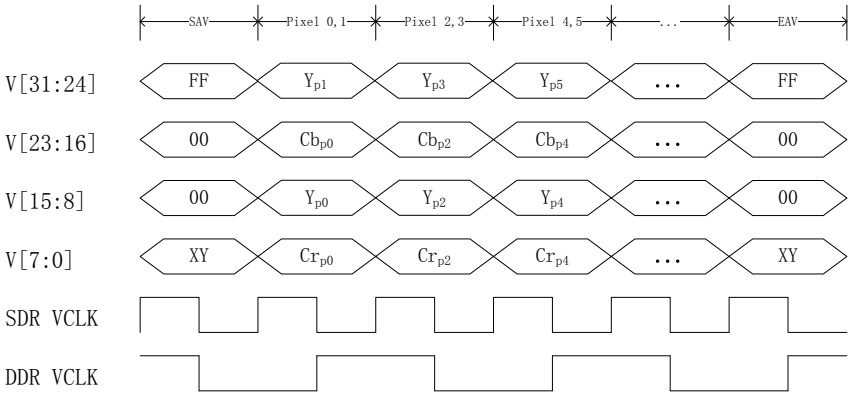


Figure 24. 32-bits YCbCr 4:2:2 Embedded Sync Timing Diagram

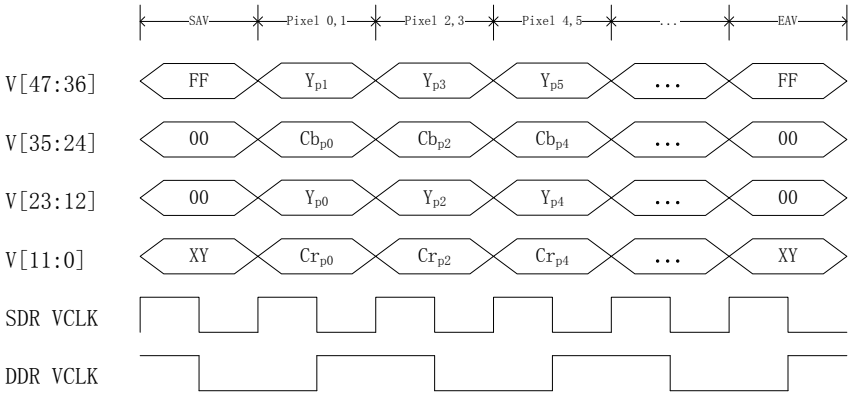


Figure 25. 48-bits YCbCr 4:2:2 Embedded Syncs Timing Diagram

4.1.3 Typical Timing Table

Table 25. Typical Timming Table

Parallel Timing Format	Color Space	Sampling	Channel Number	Pixel Bits	Pixel Clock Frequency	Dual/Single Pixel	Parallel PHY Frequency	TTL Pin Data Rate	Total Data Rate (Mbps)	Used Pins
4K@60	RGB/YCbCr	4:4:4	3	8	594	2	297	297	14256	48
4K@60	YCbCr	4:2:2	2	8	594	2	297	297	9504	32
4K@60	YCbCr	4:2:2	2	10	594	2	297	297	11880	40
4K@60	YCbCr	4:2:2	2	12	594	2	297	297	14256	48
4K@60	YCbCr	4:2:0	3	8	297	1	297	297	7128	24
4K@60	YCbCr	4:2:0	3	10	297	1	297	297	8910	30
4K@60	YCbCr	4:2:0	3	12	297	1	297	297	10692	36
4K@30	RGB/YCbCr	4:4:4	3	8	297	1	297	297	7128	24
4K@30	RGB/YCbCr	4:4:4	3	10	297	1	297	297	8910	30
4K@30	RGB/YCbCr	4:4:4	3	12	297	1	297	297	10692	36
4K@30	RGB/YCbCr	4:4:4	3	8	297	1	297	297	7128	24
4K@30	RGB/YCbCr	4:4:4	3	10	297	1	297	297	8910	30
4K@30	RGB/YCbCr	4:4:4	3	12	297	1	297	297	10692	36
4K@30	YCbCr	4:2:2	2	8	297	1	297	297	4752	16
4K@30	YCbCr	4:2:2	2	10	297	1	297	297	5940	20
4K@30	YCbCr	4:2:2	2	12	297	1	297	297	7128	24
1080P@60	RGB/YCbCr	4:4:4	3	8	148.5	1	148.5	148.5	3564	24
1080P@60	RGB/YCbCr	4:4:4	3	10	148.5	1	148.5	148.5	4455	30
1080P@60	RGB/YCbCr	4:4:4	3	12	148.5	1	148.5	148.5	5346	36
1080P@60	YCbCr	4:2:2	2	8	148.5	1	148.5	148.5	2376	16
1080P@60	YCbCr	4:2:2	2	10	148.5	1	148.5	148.5	2970	20
1080P@60	YCbCr	4:2:2	2	12	148.5	1	148.5	148.5	3564	24
1080P@60	YCbCr	4:2:2	2	8	148.5	1	297	297	2376	8
1080P@60	YCbCr	4:2:2	2	10	148.5	1	297	297	2970	10
1080P@60	YCbCr	4:2:2	2	12	148.5	1	297	297	3564	12

4.2 LVDS Output Mode

The GSV2011 has 12(data) + 3(sync) pairs of LVDS, it can support multiple modes, and the mode registers are shown in Table 26.

Table 26. LVDS Mode Register Definition

.

These 3 bytes are the key configurations for different pin mapping types.

Table 26. LVDS Mode Register Definition

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Mode CFG 2	N/A	i2c_tx_par_adif_div2_en: Only work when x1/x2/x3 mode 0: not div2 1: div2	i2c_tx_par_multi_pixel_sel[1:0]: 00: 1 pixel per clk 01: 2 pixels per clk 10: 4 pixels per clk 11: Resverd		N/A	i2c_tx_par_clk_ratio[2:0]: Ratio of SDR VCLK/Pixel DIV CLK 000/001: 1 clk 1 pixel = 1x 010: 2 clk 1 pixel = 2x 011: 3 clk 1 pixel = 3x … 111: 7 clk 1 pixel = 7x		
Mode CFG 1	i2c_tx_par_panel_en: 0: Disable 1: Enable	i2c_tx_par_panel_sel: 0: VESA 1: JEIDA	i2c_tx_par_sub_mode[1:0]: 00: Mode A 01: Mode B 10: Mode C 11: Mode D		N/A	i2c_tx_par_422_en: 0: RGB 4:4:4 /CrYCb 4:4:4 /CrYCb 4:2:0 1: 4:2:2	i2c_tx_par_bit_width[1:0]: 00: 6 bits 01: 8 bits 10:10 bits 11:12 bits	
Mode CFG 0	i2c_tx_par_ttl_lvds_sel: 0: TTL 1: LVDS	[6]:i2c_tx_par_his_mode_en [5]:i2c_tx_par_udp_mode_en [4]:i2c_tx_par_sync_mode bit[6:4]: 1XX: HIS mode 01X: UDP mode 001: ITU Embedded Syncs 000: Separate Syncs			N/A	i2c_tx_par_fixed_high_phy_clk_en: 0: Normal 1: Fixed 1.2 Gbps	i2c_tx_par_vclk_divn_en: 0: div 1 1: div N	i2c_tx_par_vclk_ddr_en: 0: SDR 1: DDR

Table 27 shows all supported modes in LVDS 12-pairs mode.

Table 27. LVDS 12-pairs Output Modes

Color Space	Video Format	Bit Width	HS/VS	Sampling	VCLK/Pixel_CLK
RGB	4:4:4	8	Separate	SDR	2x
				DDR	1x
		8/10/12	Separate	SDR	3x
				DDR	1.5x
		8/10/12	Separate	SDR	4x
				DDR	2x
YCbCr	4:4:4	8	Separate	SDR	2x
				DDR	1x
		8/10/12	Separate	SDR	3x
				DDR	1.5x
		8/10/12	Separate	SDR	4x
				DDR	2x
	4:2:2	8/10/12	Separate	SDR	2x
				DDR	1x
			Embedded	SDR	2x
				DDR	1x
		8/10/12	Separate	SDR	4x
				DDR	2x

4.2.1 LVDS 2x/3x Mode

4.2.1.1 YCbCr/RGB 4:4:4 Mode

The YCbCr4:4:4 x2/x3 mode pin mapping is shown in Table 28.

Table 28. LVDS 2x/3x YCbCr 4:4:4 Pin Mapping

Mode CFG 2	0x43			0x43			0x43			0x42	
Mode CFG 1	0x01			0x02			0x03			0x11	
Mode CFG 0											
Color Space	CrYCb										
Tag	8-Bit 4:4:4			10-Bit 4:4:4			12-Bit 4:4:4			12-Bit 4:4:4 Mode B	
Standard											
SDR Clock Ratio	3x			3x			3x			2x	
DDR Clock Ratio	1.5x			1.5x			1.5x			1x	
PIN NAME	BIT 0	BIT 1	BIT 2	BIT 0	BIT 1	BIT 2	BIT 0	BIT 1	BIT 2	BIT 0	BIT 1
V11	Cr7	Y7	Cb7	Cr9	Y9	Cb9	Cr11	Y11	Cb11	Cr7	Cb7
V10	Cr6	Y6	Cb6	Cr8	Y8	Cb8	Cr10	Y10	Cb10	Cr6	Cb6
V9	Cr5	Y5	Cb5	Cr7	Y7	Cb7	Cr9	Y9	Cb9	Cr5	Cb5
V8	Cr4	Y4	Cb4	Cr6	Y6	Cb6	Cr8	Y8	Cb8	Cr4	Cb4
V7	Cr3	Y3	Cb3	Cr5	Y5	Cb5	Cr7	Y7	Cb7	Cr3	Cb3
V6	Cr2	Y2	Cb2	Cr4	Y4	Cb4	Cr6	Y6	Cb6	Cr2	Cb2
V5	Cr1	Y1	Cb1	Cr3	Y3	Cb3	Cr5	Y5	Cb5	Cr1	Cb1
V4	Cr0	Y0	Cb0	Cr2	Y2	Cb2	Cr4	Y4	Cb4	Cr0	Cb0
V3	Z	Z	Z	Cr1	Y1	Cb1	Cr3	Y3	Cb3	Y7	Y3
V2	Z	Z	Z	Cr0	Y0	Cb0	Cr2	Y2	Cb2	Y6	Y2
V1	Z	Z	Z	Z	Z	Z	Cr1	Y1	Cb1	Y5	Y1
V0	Z	Z	Z	Z	Z	Z	Cr0	Y0	Cb0	Y4	Y0
VS	VS/Embedded			VS/Embedded			VS/Embedded			VS	
HS	HS/Embedded			HS/Embedded			HS/Embedded			HS	
DE	DE/Embedded			DE/Embedded			DE/Embedded			DE	

Please note:

- In YCbCr4:4:4 8-bit mode (Mode CFG[2:1]=0x42_11), the SDR VCLK is 2 times of video pixel clock.
- In YCbCr4:4:4 8/10/12-bit mode (Mode CFG[2:1]=0x43_01, 0x43_02, 0x43_03), the SDR VCLK is 3 times of video pixel clock.

The RGB 4:4:4 pin mapping is shown in Table 29

Table 29. LVDS 2x/3x RGB 4:4:4 Pin Mapping

Mode CFG 2	0x43			0x43			0x43			0x42	
Mode CFG 1	0x01			0x02			0x03			0x11	
Mode CFG 0											
Color Space	RGB										
Tag	8-Bit 4:4:4			10-Bit 4:4:4			12-Bit 4:4:4			12-Bit 4:4:4 Mode B	
Standard											
SDR Clock Ratio	3x			3x			3x			2x	
DDR Clock Ratio	1.5x			1.5x			1.5x			1x	
PIN NAME	BIT 0	BIT 1	BIT 2	BIT 0	BIT 1	BIT 2	BIT 0	BIT 1	BIT 2	BIT 0	BIT 1
V11	R7	G7	B7	R9	G9	B9	R11	G11	B11	R7	B7
V10	R6	G6	B6	R8	G8	B8	R10	G10	B10	R6	B6
V9	R5	G5	B5	R7	G7	B7	R9	G9	B9	R5	B5
V8	R4	G4	B4	R6	G6	B6	R8	G8	B8	R4	B4
V7	R3	G3	B3	R5	G5	B5	R7	G7	B7	R3	B3
V6	R2	G2	B2	R4	G4	B4	R6	G6	B6	R2	B2
V5	R1	G1	B1	R3	G3	B3	R5	G5	B5	R1	B1
V4	R0	G0	B0	R2	G2	B2	R4	G4	B4	R0	B0
V3	Z	Z	Z	R1	G1	B1	R3	G3	B3	G7	G3
V2	Z	Z	Z	R0	G0	B0	R2	G2	B2	G6	G2
V1	Z	Z	Z	Z	Z	Z	R1	G1	B1	G5	G1
V0	Z	Z	Z	Z	Z	Z	R0	G0	B0	G4	G0
VS	VS			VS			VS			VS	
HS	HS			HS			HS			HS	
DE	DE			DE			DE			DE	

4.2.1.2 YCbCr 4:2:2 Mode

The YCbCr4:2:2 pin mapping is shown in Table 30.

Table 30. LVDS 2x/3x YCbCr 4:2:2 Pin Mapping

Mode CFG 2	0x42		0x42		0x42	
Mode CFG 1	0x05		0x06		0x07	
Mode CFG 0						
Color Space	CrYCb					
Tag	8-Bit 4:2:2		10-Bit 4:2:2		12-Bit 4:2:2 Mode A	
Standard	BT.656		BT.656		BT.656	
SDR Clock Ratio	2x		2x		2x	
DDR Clock Ratio	1x		1x		1x	
PIN NAME	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
V11	C7	Y7	C9	Y9	C11	Y11
V10	C6	Y6	C8	Y8	C10	Y10
V9	C5	Y5	C7	Y7	C9	Y9
V8	C4	Y4	C6	Y6	C8	Y8
V7	C3	Y3	C5	Y5	C7	Y7
V6	C2	Y2	C4	Y4	C6	Y6
V5	C1	Y1	C3	Y3	C5	Y5
V4	C0	Y0	C2	Y2	C4	Y4
V3	Z	Z	C1	Y1	C3	Y3
V2	Z	Z	C0	Y0	C2	Y2
V1	Z	Z	Z	Z	C1	Y1
V0	Z	Z	Z	Z	C0	Y0
VS	VS/Embedded		VS/Embedded		VS/Embedded	
HS	HS/Embedded		HS/Embedded		HS/Embedded	
DE	DE/Embedded		DE/Embedded		DE/Embedded	

In YCbCr4:2:2 mode, the SDR VCLK is 2 times of pixel clock. And it can support both separate syncs and embedded syncs.

4.2.2 LVDS x4 Mode

In GSV2011, LVDS 4x mode can support both single and double pixel modes.
If video pixel clock frequency <= 300MHz, using single pixel mode.
If video pixel clock frequency > 300MHz, using dual pixel mode.

4.2.2.1 Single Pixel Mode

4.2.2.1.1 YCbCr/RGB 4:4:4 Mode

Table 31. LVDS 4x Single Pixel YCbCr/RGB 4:4:4 Pin Mapping

Mode CFG 2	0x04				0x04				0x04			
Mode CFG 1	0x01				0x02				0x03			
Mode CFG 0												
Color Space	CrYCb 4:4:4											
Tag	8-Bit 4:4:4				10-Bit 4:4:4				12-Bit 4:4:4			
SDR Clock Ratio	4x				4x				4x			
DDR Clock Ratio	2x				2x				2x			
PIN NAME	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
V11	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V10	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V9	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V8	Z	Z	Z	Z	Z	Z	Z	Z	Cr1	Cr0	Y1	Y0
V7	Z	Z	Z	Z	Z	Z	Cr1	Cr0	Cb1	Cb0	Cr3	Cr2
V6	Z	Z	Z	Z	Y1	Y0	Cb1	Cb0	Y3	Y2	Cb3	Cb2
V5	Cr7	Cr6	Cr5	Cr4	Cr9	Cr8	Cr7	Cr6	Cr11	Cr10	Cr9	Cr8
V4	Cr3	Cr2	Cr1	Cr0	Cr5	Cr4	Cr3	Cr2	Cr7	Cr6	Cr5	Cr4
V3	Y7	Y6	Y5	Y4	Y9	Y8	Y7	Y6	Y11	Y10	Y9	Y8
V2	Y3	Y2	Y1	Y0	Y5	Y4	Y3	Y2	Y7	Y6	Y5	Y4
V1	Cb7	Cb6	Cb5	Cb4	Cb9	Cb8	Cb7	Cb6	Cb11	Cb10	Cb9	Cb8
V0	Cb3	Cb2	Cb1	Cb0	Cb5	Cb4	Cb3	Cb2	Cb7	Cb6	Cb5	Cb4
VS	VS				VS				VS			
HS	HS				HS				HS			
DE	DE				DE				DE			
Color Space	RGB											
V11	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V10	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V9	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V8	Z	Z	Z	Z	Z	Z	Z	Z	R1	R0	G1	G0
V7	Z	Z	Z	Z	Z	Z	R1	R0	B1	B0	R3	R2
V6	Z	Z	Z	Z	G1	G0	B1	B0	G3	G2	B3	B2
V5	R7	R6	R5	R4	R9	R8	R7	R6	R11	R10	R9	R8
V4	R3	R2	R1	R0	R5	R4	R3	R2	R7	R6	R5	R4
V3	G7	G6	G5	G4	G9	G8	G7	G6	G11	G10	G9	G8
V2	G3	G2	G1	G0	G5	G4	G3	G2	G7	G6	G5	G4
V1	B7	B6	B5	B4	B9	B8	B7	B6	B11	B10	B9	B8
V0	B3	B2	B1	B0	B5	B4	B3	B2	B7	B6	B5	B4
VS	VS				VS				VS			
HS	HS				HS				HS			
DE	DE				DE				DE			

4.2.2.1.2 YCbCr 4:2:2 Mode

Table 32. LVDS 4x Single Pixel YCbCr 4:2:2 Pin Mapping

Mode CFG 2	0x04				0x04				0x04			
Mode CFG 1	0x05				0x06				0x07			
Mode CFG 0												
Color Space	CrYCb 4:2:2											
Tag	8-Bit				10-Bit				12-Bit			
SDR Clock Ratio	4x				4x				4x			
DDR Clock Ratio	2x				2x				2x			
PIN NAME	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
V11	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V10	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V9	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V8	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V7	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V6	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
V5	Z	Z	Z	Z	Z	Z	Z	Z	Y1	Y0	C1	C0
V4	Z	Z	Z	Z	Y1	Y0	C1	C0	Y3	Y2	C3	C2
V3	Y7	Y6	Y5	Y4	Y9	Y8	Y7	Y6	Y11	Y10	Y9	Y8
V2	Y3	Y2	Y1	Y0	Y5	Y4	Y3	Y2	Y7	Y6	Y5	Y4
V1	C7	C6	C5	C4	C9	C8	C7	C6	C11	C10	C9	C8
V0	C3	C2	C1	C0	C5	C4	C3	C2	C7	C6	C5	C4
VS	VS				VS				VS			
HS	HS				HS				HS			
DE	DE				DE				DE			

4.2.2.2 Dual Pixel Mode

4.2.2.2.1 YCbCr/RGB 4:4:4 Mode

When 4K60 4:4:4 8-bits per channel, it should use dual pixel mode, each lane is 594MHz/2 * 4 bits = 1188Mbps.

Table 33. LVDS 4x Dual Pixel YCbCr/RGB 4:4:4 Pin Mapping

Mode CFG 2	0x14			
Mode CFG 1	0x01			
Mode CFG 0				
Color Space	CrYCb 4:4:4			
Tag	8-Bit 4:4:4			
SDR Clock Ratio	4x			
DDR Clock Ratio	2x			
PIN NAME	BIT 3	BIT 2	BIT 1	BIT 0
V11	P1.Cr7	P1.Cr6	P1.Cr5	P1.Cr4
V10	P1.Cr3	P1.Cr2	P1.Cr1	P1.Cr0
V9	P1.Y7	P1.Y6	P1.Y5	P1.Y4
V8	P1.Y3	P1.Y2	P1.Y1	P1.Y0
V7	P1.Cb7	P1.Cb6	P1.Cb5	P1.Cb4
V6	P1.Cb3	P1.Cb2	P1.Cb1	P1.Cb0
V5	P0.Cr7	P0.Cr6	P0.Cr5	P0.Cr4
V4	P0.Cr3	P0.Cr2	P0.Cr1	P0.Cr0
V3	P0.Y7	P0.Y6	P0.Y5	P0.Y4
V2	P0.Y3	P0.Y2	P0.Y1	P0.Y0
V1	P0.Cb7	P0.Cb6	P0.Cb5	P0.Cb4
V0	P0.Cb3	P0.Cb2	P0.Cb1	P0.Cb0
VS	VS			
HS	HS			
DE	DE			
Color Space	RGB			
V11	P1.R7	P1.R6	P1.R5	P1.R4
V10	P1.R3	P1.R2	P1.R1	P1.R0
V9	P1.G7	P1.G6	P1.G5	P1.G4
V8	P1.G3	P1.G2	P1.G1	P1.G0
V7	P1.B7	P1.B6	P1.B5	P1.B4
V6	P1.B3	P1.B2	P1.B1	P1.B0
V5	P0.R7	P0.R6	P0.R5	P0.R4
V4	P0.R3	P0.R2	P0.R1	P0.R0
V3	P0.G7	P0.G6	P0.G5	P0.G4
V2	P0.G3	P0.G2	P0.G1	P0.G0
V1	P0.B7	P0.B6	P0.B5	P0.B4
V0	P0.B3	P0.B2	P0.B1	P0.B0
VS	VS			
HS	HS			
DE	DE			

4.2.2.2.2 YCbCr 4:2:2 Mode

Table 34. LVDS 4x Dual Pixel YCbCr 4:2:2 Pin Mapping

Mode CFG 2	0x14				0x14				0x14			
Mode CFG 1	0x05				0x06				0x07			
Mode CFG 0												
Color Space	CrYCb 4:2:2											
Tag	8-Bit				10-Bit				12-Bit			
SDR Clock Ratio	4x				4x				4x			
DDR Clock Ratio	2x				2x				2x			
PIN NAME	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
V11	Z	Z	Z	Z	Z	Z	Z	Z	P1.Y1	P1.Y0	P1.C1	P1.C0
V10	Z	Z	Z	Z	P1.Y1	P1.Y0	P1.C1	P1.C0	P1.Y3	P1.Y2	P1.C3	P1.C2
V9	P1.Y7	P1.Y6	P1.Y5	P1.Y4	P1.Y9	P1.Y8	P1.Y7	P1.Y6	P1.Y11	P1.Y10	P1.Y9	P1.Y8
V8	P1.Y3	P1.Y2	P1.Y1	P1.Y0	P1.Y5	P1.Y4	P1.Y3	P1.Y2	P1.Y7	P1.Y6	P1.Y5	P1.Y4
V7	P1.C7	P1.C6	P1.C5	P1.C4	P1.C9	P1.C8	P1.C7	P1.C6	P1.C11	P1.C10	P1.C9	P1.C8
V6	P1.C3	P1.C2	P1.C1	P1.C0	P1.C5	P1.C4	P1.C3	P1.C2	P1.C7	P1.C6	P1.C5	P1.C4
V5	Z	Z	Z	Z	Z	Z	Z	Z	P0.Y1	P0.Y0	P0.C1	P0.C0
V4	Z	Z	Z	Z	P0.Y1	P0.Y0	P0.C1	P0.C0	P0.Y3	P0.Y2	P0.C3	P0.C2
V3	P0.Y7	P0.Y6	P0.Y5	P0.Y4	P0.Y9	P0.Y8	P0.Y7	P0.Y6	P0.Y11	P0.Y10	P0.Y9	P0.Y8
V2	P0.Y3	P0.Y2	P0.Y1	P0.Y0	P0.Y5	P0.Y4	P0.Y3	P0.Y2	P0.Y7	P0.Y6	P0.Y5	P0.Y4
V1	P0.C7	P0.C6	P0.C5	P0.C4	P0.C9	P0.C8	P0.C7	P0.C6	P0.C11	P0.C10	P0.C9	P0.C8
V0	P0.C3	P0.C2	P0.C1	P0.C0	P0.C5	P0.C4	P0.C3	P0.C2	P0.C7	P0.C6	P0.C5	P0.C4
VS	VS				VS				VS			
HS	HS				HS				HS			
DE	DE				DE				DE			

4.2.2.3 Typical Timing Example

Some detail information of typical timing in 4x mode, such as 4K60,4K30 and 1080P… are listed in Table 35.

Table 35. LVDS 4x Mode Timing Example

Timing Format	Color Space	Sampling	Channel Number	Pixel Bits	Pixel Clock Frequency (MHz)	Dual /Single Pixel	Digital-PHY Interface Frequency	LVDS Ntol Ratio	Total DataRate (Mbps)	12 Pairs LVDS Lane DataRate	12 Pairs LVDS Total DataRate	Used Pairs	Used DataRate
4K2K@60	YCbCr	4:4:4	3	8	594	2	297	4	14256	1188	14256	12	14256
4K2K@60	YCbCr	4:2:2	2	8	594	2	297	4	9504	1188	14256	8	9504
4K2K@60	YCbCr	4:2:2	2	10	594	2	297	4	11880	1188	14256	10	11880
4K2K@60	YCbCr	4:2:2	2	12	594	2	297	4	14256	1188	14256	12	14256
4K2K@30	YCbCr	4:4:4	3	8	297	1	297	4	7128	1188	14256	6	7128
4K2K@30	YCbCr	4:4:4	3	10	297	1	297	4	8910	1188	14256	8	9504
4K2K@30	YCbCr	4:4:4	3	12	297	1	297	4	10692	1188	14256	9	10692
1080P60	YCbCr	4:4:4	3	8	148.5	1	148.5	4	3564	594	7128	6	3564
1080P60	YCbCr	4:4:4	3	10	148.5	1	148.5	4	4455	594	7128	8	4752
1080P60	YCbCr	4:4:4	3	12	148.5	1	148.5	4	5346	594	7128	9	5346
1080P60	YCbCr	4:2:2	2	8	148.5	1	148.5	4	2376	594	7128	4	2376
1080P60	YCbCr	4:2:2	2	10	148.5	1	148.5	4	2970	594	7128	5	2970
1080P60	YCbCr	4:2:2	2	12	148.5	1	148.5	4	3564	594	7128	6	3564

From Table 35 it shows the highest data rate is around 1.2Gbps. When data rate is higher than 600Mbps, DDR clock mode is recommended.

4.2.3 VESA JEIDA Standard

GSV2011 can support VESA and JEIDA LVDS standard. It can support both 1 channel and 2 channels.
The VESA standard color mapping is shown in Figure 26.

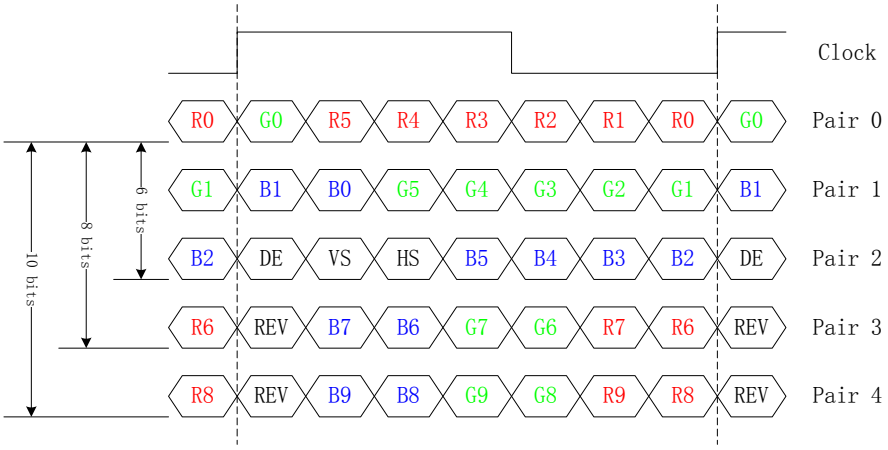


Figure 26. VESA LVDS Color Mapping

The JEIDA standard color mapping is shown in Figure 27.

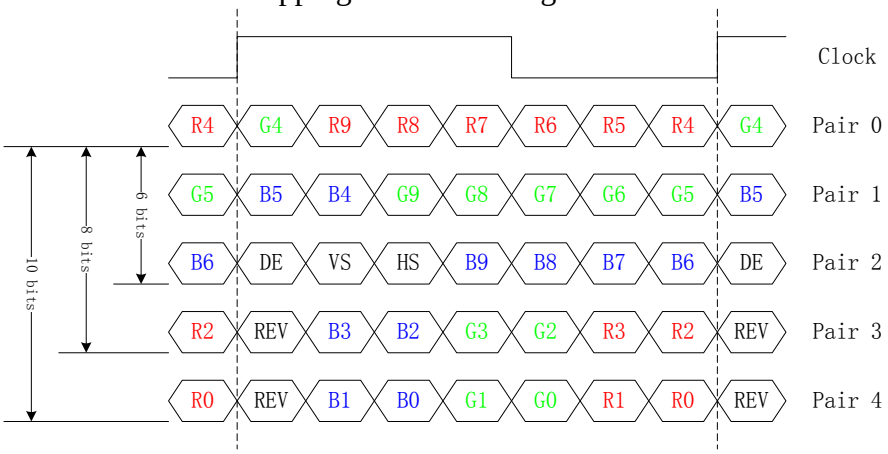


Figure 27. JEIDA LVDS Color Mapping

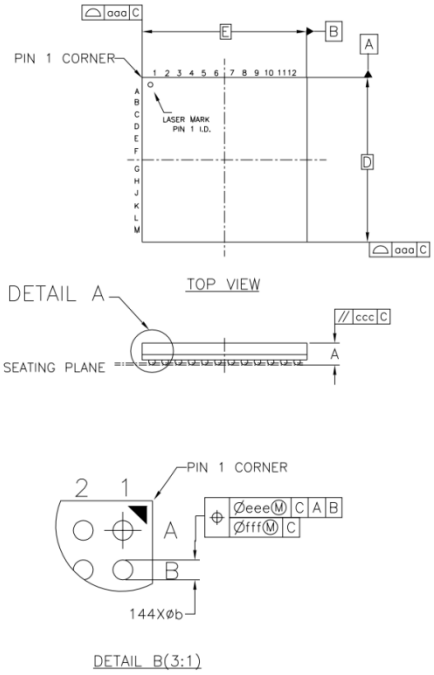
In GSV2011, LVDS max data rate is 1.2Gbps, for the single channel VESA or JEIDA port, the max pixel clock frequency is 171MHz. Means the single channel VESA or JEIDA port can support 1080P60 4:4:4 10-bits. Two channels VESA or JEIDA ports can support 4K30 4:4:4 10-bits

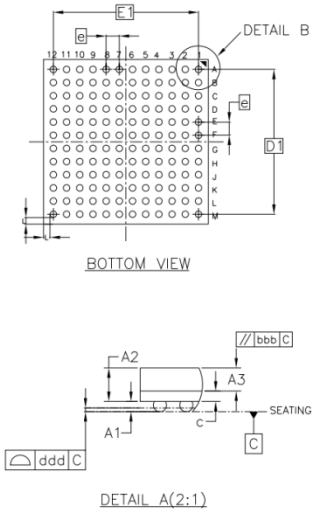
4.2.4 Typical Timing Table

Table 36. Typical Timming Table

Parallel Timing Format	Color Space	Sampling	Channel Number	Pixel Bits	Pixel Clock Frequency	Dual/Single Pixel	Parallel PHY Frequency	LVDS Nto1 Ratio	Total Data Rate (Mbps)	12 Pairs LVDS Lane Data Rate	12 Pairs LVDS Total Data Rate	Used Pairs
4K@60	RGB/YCbCr	4:4:4	3	8	594	2	297	4	14256	1188	14256	12
4K@60	YCbCr	4:2:2	2	8	594	2	297	4	9504	1188	14256	8
4K@60	YCbCr	4:2:2	2	10	594	2	297	4	11880	1188	14256	10
4K@60	YCbCr	4:2:2	2	12	594	2	297	4	14256	1188	14256	12
4K@60	YCbCr	4:2:0	3	8	297	1	297	4	7128	1188	14256	6
4K@60	YCbCr	4:2:0	3	10	297	1	297	4	9504	1188	14256	8
4K@60	YCbCr	4:2:0	3	12	297	1	297	4	10692	1188	14256	9
4K@30	RGB/YCbCr	4:4:4	3	8	297	1	297	4	7128	1188	14256	6
4K@30	RGB/YCbCr	4:4:4	3	10	297	1	297	4	9504	1188	14256	8
4K@30	RGB/YCbCr	4:4:4	3	12	297	1	297	4	10692	1188	14256	9
4K@30	RGB/YCbCr	4:4:4	3	8	297	1	297	3	7128	891	10692	8
4K@30	RGB/YCbCr	4:4:4	3	10	297	1	297	3	8910	891	10692	10
4K@30	RGB/YCbCr	4:4:4	3	12	297	1	297	3	10692	891	10692	12
4K@30	YCbCr	4:2:2	2	8	297	1	297	4	7128	1188	14256	6
4K@30	YCbCr	4:2:2	2	10	297	1	297	4	9504	1188	14256	8
4K@30	YCbCr	4:2:2	2	12	297	1	297	4	10692	1188	14256	9
1080P@60	RGB/YCbCr	4:4:4	3	8	148.5	1	148.5	4	3564	594	7128	6
1080P@60	RGB/YCbCr	4:4:4	3	10	148.5	1	148.5	4	4752	594	7128	8
1080P@60	RGB/YCbCr	4:4:4	3	12	148.5	1	148.5	4	5346	594	7128	9
1080P@60	YCbCr	4:2:2	2	8	148.5	1	148.5	4	2376	594	7128	4
1080P@60	YCbCr	4:2:2	2	10	148.5	1	148.5	4	2970	594	7128	5
1080P@60	YCbCr	4:2:2	2	12	148.5	1	148.5	4	3564	594	7128	6

5 Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.25	1.33	1.41
A1	0.26	0.31	0.36
A2	1.01	1.02	1.11
A3		0.70 BASIC	
c	0.28	0.32	0.36
D	9.90	10.00	10.10
D1		8.80 BASIC	
E	9.90	10.00	10.10
E1		8.80 BASIC	
e		0.80 BASIC	
b	0.35	0.40	0.45
L		0.40 REF	
aaa		0.10	
bbb		0.10	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	

Figure 28. Package Dimensions (BGA144)

6 Ordering Guide

Table 37. Ordering Infomation

Part Number.	Temperature Range	Package Description	Packing Type
GSV2011	−20 ℃ to +85 ℃	BGA144, 0.8 mm ball pitch, 10 mm x 10 mm outline	Tray

7 Revision History

Table 38. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Sep 27, 2019
V0.2	Characteristics values updated, all supported formats are listed in tables.	Jan 8, 2020
V0.3	Characteristics values updated.	Mar 16, 2020
V0.4	Reorganize chapters' order, add TMDS Transmitter and Chip Access Timing Information, add power consumption table.	Jun 28, 2020
V0.5	Add typical timing mapping table.	Dec 3, 2020
V0.6	Add junction temperature calculation formulas.	Feb 19, 2021
V0.7	Add typical soldering profile.	Feb 24, 2021
V0.8	Update maximum junction temperature value.	Apr 8, 2021
V1.0	Reformat the document.	May 8, 2021

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