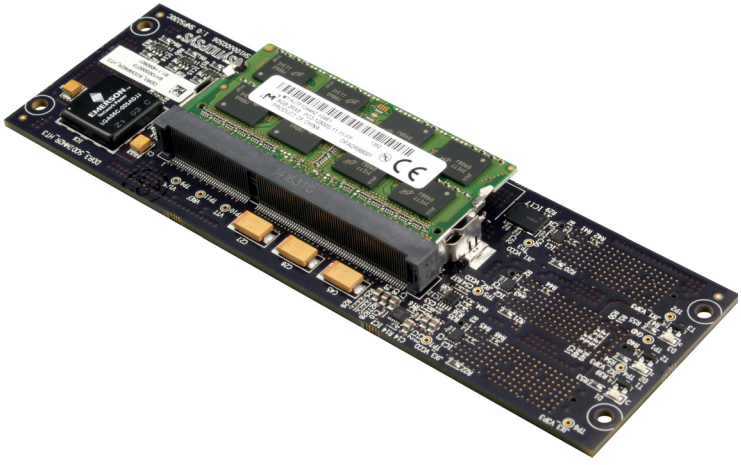
HAPS®
DDR3_SODIMM2R_HT3
Reference Manual

March 2017



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Revision History

Date	Revision	Comment
06/30/13	0	Initial version.
06/30/14	0.1	p. 12 Added alternate DDR3 SODIMM MT16KTF1G64HZ-1G6D1.
06/30/15	0.2	p. 16 Updated pin and signal table.
12/30/15	0.3	p. 18 Added TSS DDR3_SODIMM2R_HT3 information.
06/15/16	0.4	p. 7 Changed maximum operating data rate units from Mbps to MT/s. p. 9, 10, 11, and 17 Updated signal name format for HAPS ProtoCompiler TSS compatibility. p. 12 Added alternate DDR3 SODIMM memories MT16KTF1G64HZ-1G6E1 and MT16KTF1G64HZ-1G9P1
03/21/17	0.5	p. 12 Added alternate DDR3 SODIMM MT16KTF1G64HZ-1G9P2

Contents

DDR3_SODIMM2R_HT3

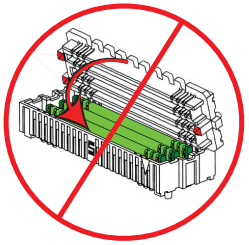
IMPORTANT!

ESD

The DDR3_SODIMM2R_HT3 daughter board, as all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the
DDR3_SODIMM2R_HT3 daughter board:

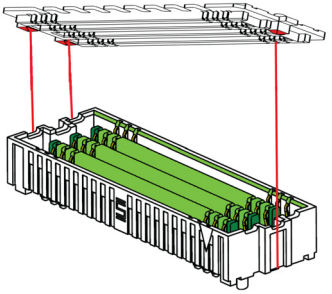
- Transport the adapter board in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

HapsTrak® 3 Connector Considerations



Take care when attaching the HapsTrak 3 (HT3) connectors. If connected improperly, socket pins can become deformed or holding rail ends can become damaged.

When connecting daughter boards and HT3 cable connectors, keep the connectors parallel to one another throughout the mating process.



Overview

This document is the HAPS® DDR3_SODIMM2R_HT3 Reference Manual and describes the functions of the DDR3_SODIMM2R_HT3 daughter board.

For an up-to-date list of HAPS daughter boards and accessories go to www.synopsys.com/haps.

DDR3_SODIMM2R_HT3

The DDR3_SODIMM2R_HT3 daughter board connects a DDR3 SODIMM to a HAPS system. The DDR3_SODIMM2R_HT3 daughter board is equipped with a DDR3 SODIMM socket and module on the top side and three HapsTrak 3 connectors on the bottom side. The DDR3_SODIMM2R_HT3 has a recommended operating data rate of 800 MT/s.

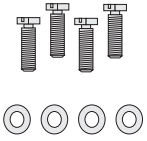
The DDR3_SODIMM2R_HT3 has dual rank support in conjunction with Xilinx MIG controller.

Package Contents

1 DDR3_SODIMM2R_HT3 daughter board
with DDR3 SODIMM

Mounting accessories

- 4 M3x6 Screws
- 4 M3 Washers



Board Layout

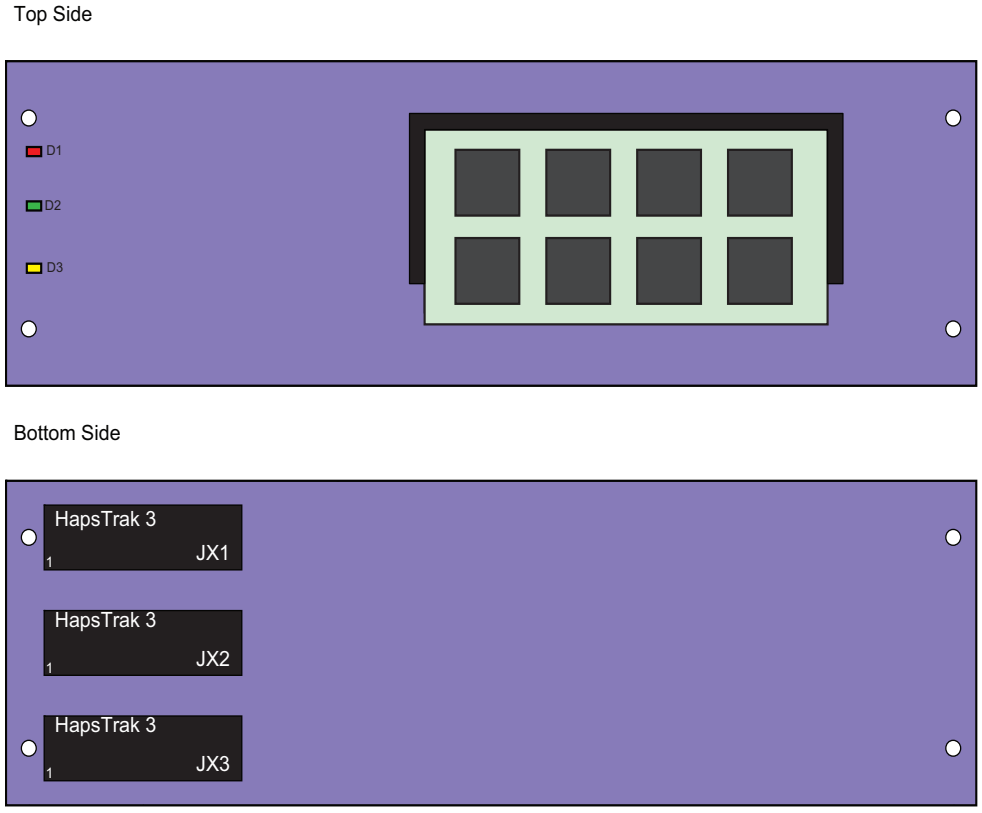


Figure 1: DDR3_SODIMM2R_HT3 Daughter Board Layout

System Interface Diagram

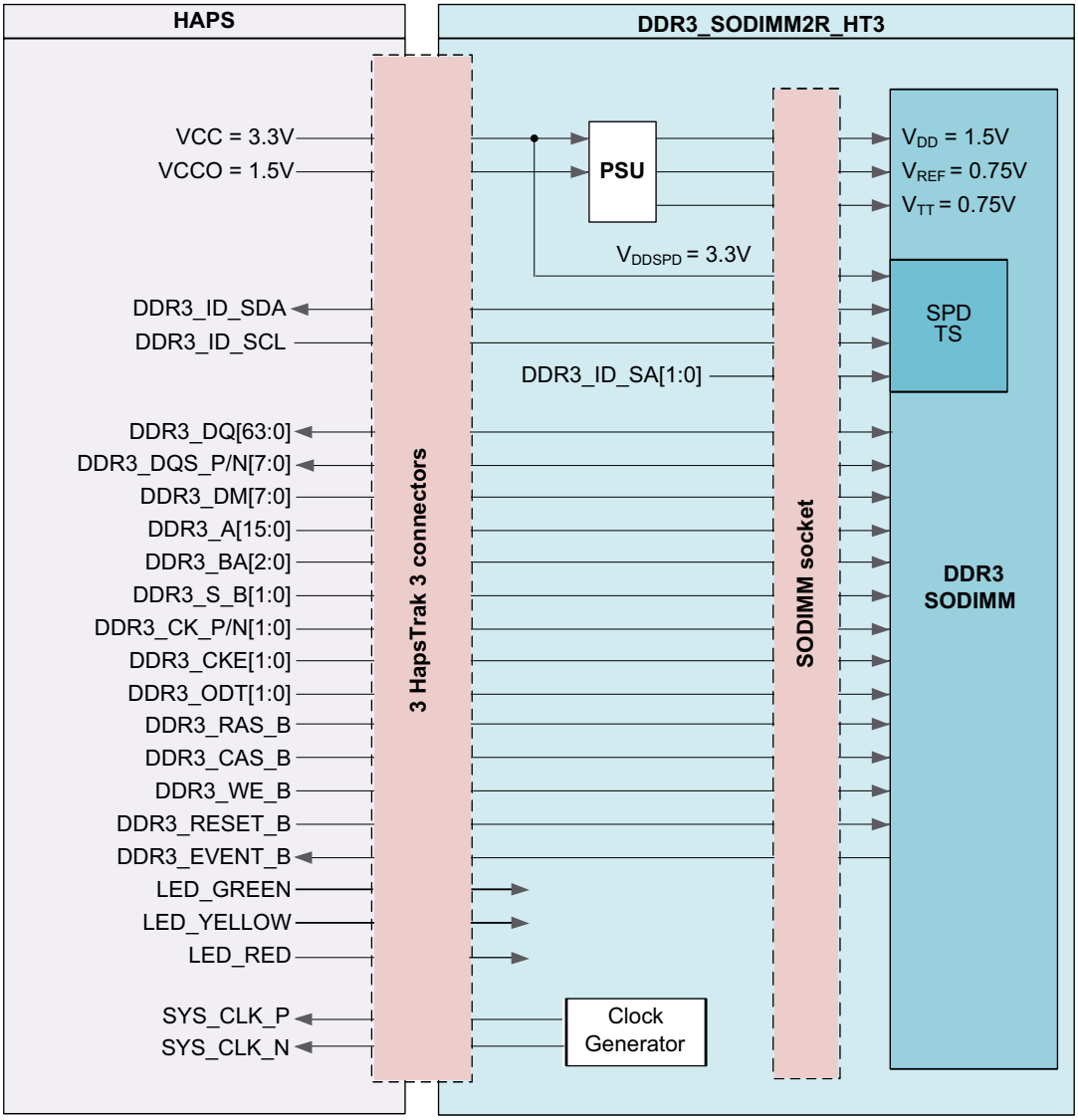


Figure 2: DDR3_SODIMM2R_HT3 System Interface Diagram

Signals

DDR3_SODIMM2R_HT3 Signal Descriptions

Signal	Type	Description
DDR3_DQ[63:0]	I/O	Data
DDR3_DQS_P[7:0] DDR3_DQS_N[7:0]	I/O	Data strobe
DDR3_DM[7:0]	Input	Data mask
DDR3_A[15:0]	Input	Address
DDR3_BA[2:0]	Input	Bank address
DDR3_S_B[1:0]	Input	Chip select
DDR3_CK_P[1:0] DDR3_CK_N[1:0]	Input	Clock
DDR3_CKE[1:0]	Input	Clock enable (pulled to GND)
DDR3_ODT[1:0]	Input	On-die termination
DDR3_RAS_B	Input	Row address strobe
DDR3_CAS _B	Input	Column address strobe
DDR3_WE_B	Input	Write enable
DDR3_RESET_B	Input	Reset (pulled to GND)
DDR3_EVENT_B	Output	Temperature event (pulled to VCCO)
DDR3_ID_SCL	Input	Serial clock for temperature sensor (TS) and SPD EEPROM
DDR3_ID_SDA	I/O	Serial data
DDR3_ID_SA[1:0]	–	Serial address tied to GND by default
SYS_CLK_P SYS_CLK_N	Output	Onboard reference clock
LED_GREEN	Input	User LED green
LED_YELLOW	Input	User LED yellow
LED_RED	Input	User LED red

Voltage Descriptions

Voltage	Type	Description
V_{DD}	Supply	Power supply
V_{DDSPD}	Supply	Temperature sensor and SPD EEPROM power supply
V_{REF}	Supply	Reference voltage for control, command, and address ($V_{DD}/2$)
V_{TT}	Supply	Termination voltage for control, command, and address ($V_{DD}/2$)

Signal Lengths

Signal Group	DDR3 Signals	Length [mm]
Clk/Addr/ Cmd/Ctrl group	DDR3_CK_P[1:0], DDR3_CK_N[1:0], DDR3_A[15:0], DDR3_BA[2:0], DDR3_RAS_B, DDR3_CAS_B, DDR3_WE_B, DDR3_CS_B[3:0], DDR3_CKE[1:0], DDR3_ODT[1:0]	146.4 +/- 1
Data group 0	DDR3_DQ[7:0], DDR3_DM[0], DDR3_DQS_P[0], DDR3_DQS_N[0]	122.5 +/- 0.5
Data group 1	DDR3_DQ[15:8], DDR3_DM[1], DDR3_DQS_P[1], DDR3_DQS_N[1]	123.7 +/- 0.5
Data group 2	DDR3_DQ[23:16], DDR3_DM[2], DDR3_DQS_P[2], DDR3_DQS_N[2]	109.1 +/- 0.5
Data group 3	DDR3_DQ[31:24], DDR3_DM[3], DDR3_DQS_P[3], DDR3_DQS_N[3]	108.8 +/- 0.5
Data group 4	DDR3_DQ[39:32], DDR3_DM[4], DDR3_DQS_P[4], DDR3_DQS_N[4]	84.4 +/- 0.5
Data group 5	DDR3_DQ[47:40], DDR3_ DM[5], DDR3_DQS_P[5], DDR3_DQS_N[5]	81.8 +/- 0.5
Data group 6	DDR3_DQ[55:48], DDR3_DM[6], DDR3_DQS_P[6], DDR3_DQS_N[6]	59.9 +/- 0.5
Data group 7	DDR3_DQ[63:56], DDR3_DM[7], DDR3_DQS_P[7], DDR3_DQS_N[7]	50 +/- 0.5

LEDs

The DDR3_SODIMM2R_HT3 has three user LEDs located on the top side of the daughter board: green, red, and yellow, which can be used for status reporting.

Power and Signal Levels

The DDR3_SODIMM2R_HT3 daughter board receives its power directly through the HapsTrak 3 connector. VCCO of the selected HapsTrak connectors must be set to 1.5 V.

The DDR3_SODIMM2R_HT3 daughter board contains an ID PROM on each HapsTrak 3 connector, which is used for board identification and over-voltage protection. The ID PROMs are used by the system to ensure that the applied VCCO is compliant with the DDR3_SODIMM2R_HT3 daughter board.

Notes:

- DDR3_SODIMM2R_HT3 only supports I/O voltage of 1.5 V.
- Signals are impedance controlled (50 Ohms).
- The reference voltages for the FPGA I/O banks are not generated on the DDR3_SODIMM2R_HT3. The I/O banks in the FPGA must be switched to the banks' internal reference voltages by setting constraint/property INTERNAL_VREF to 0.75.

Memory Module

The DDR3_SODIMM2R_HT3 is shipped with an 8GB dual-rank DDR3 SDRAM SODIMM memory module installed on the daughter board. The memory module is manufactured by Micron Technology; the actual module installed can be any of the following:

Module Part Number	Base Device
MT16JTF1G64HZ-1G6D1	MT41J512M8
MT16KTF1G64HZ-1G6D1	MT41K512M8
MT16KTF1G64HZ-1G6E1	MT41K512M8
MT16KTF1G64HZ-1G9P1	MT41K512M8
MT16KTF1G64HZ-1G9P2	MT41K512M8

Clocking

The DDR3_SODIMM2R_HT3 daughter board includes a clock generator that outputs a differential 200 MHz clock signal (SYS_CLK_P/N) which can be used as an input clock for the memory controller.

Note: Use the I/O standard DIFF_SSTL15_DCI in the FPGA design.

Board Placement

When placing the DDR3_SODIMM2R_HT3 on your HAPS system be aware of the following:

- SLR (Super Logic Region) – For optimal timing of the FPGA design, avoid crossing SLR borders.
- Limited connectors – Some connectors have limited number of signals (for example, no clocks) and fixed I/O voltages.
- Voltage regions – Some HAPS systems have VCCO regions that should be considered when placing the daughter board. Respecting the regions will minimize VCCO dependencies to adjacent connectors.

Note: DDR3_SODIMM2R_HT3 daughter board is NOT stackable.

For information about SLR, limited connectors, and voltage regions, refer to your HAPS system reference manual located at HAPS SupportNet on solvnet.synopsys.com.

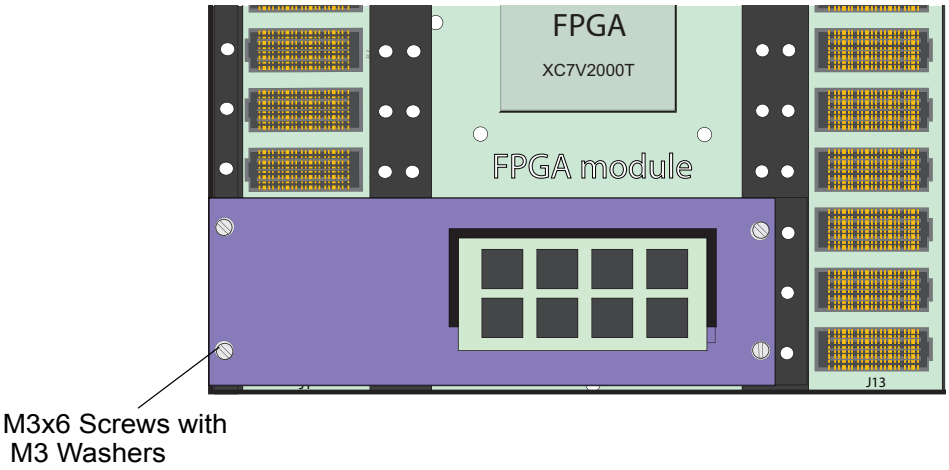


Figure 3: Board Placement Top View

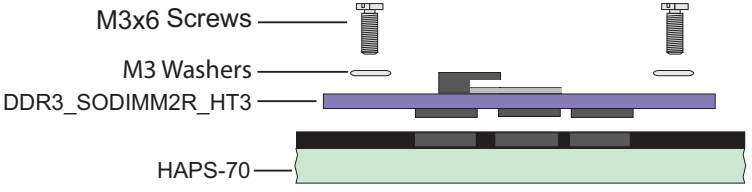


Figure 4: Front View Placing a DDR3_SODIMM2R_HT3

Pin and Signal Tables

HapsTrak 3 Connectors

The HapsTrak 3 connector definitions for the HAPS-70, HAPS-80, and HAPS-DX systems are listed in the following pin diagram. For specific information on connector configuration and limitations, see the corresponding HAPS system reference manual on solvnet.synopsys.com.

8	GND	3.3	GND	3.3	GND	3.3	GND	3.3	1
16	A0	GND	B0	GND	C0	GND	D0	GND	9
24	GND	A2	GND	B2	GND	C2	GND	D2	17
32	A1	GND	B1	GND	C1	GND	D1	GND	25
40	GND	A3	GND	B3	GND	C3	GND	D3	33
48	A4	GND	B4	GND	C4	GND	D4	GND	41
56	GND	A6	GND	B6	GND	C6	GND	D6	49
64	A5	GND	B5	GND	C5	GND	D5	GND	57
72	GND	A7	GND	B7	GND	C7	GND	D7	65
80	A8	GND	B8	GND	C8	GND	D8	GND	73
88	GND	A10	GND	B10	GND	C10	GND	D10	81
96	A9	GND	B9	GND	C9	GND	D9	GND	89
104	GND	A11	GND	B11	GND	C11	GND	D11	97
112	A12	GND	B12	GND	C12	GND	D12	GND	105
120	GND	VRP	GND	C0P	GND	C1P	GND	Rsb	113
128	A13	GND	B13	GND	C13	GND	D13	GND	121
136	GND	VRN	GND	C0N	GND	C1N	GND	Rsb	129
144	IdC	IdA1	Uin0	GND	Uout0	GND	Rsb	GND	137
152	IdA0	IdD	GND	Uin1	GND	Uout1	GND	Reset_n	145
160	Vn	V	Vn	V	Vn	V	Vn	V	153

Legend

Pin	HT3 Spec	HAPS-80	HAPS-70	HAPS-DX7
A12	Normal I/O	Normal I/O	NC	NC
A13	Normal I/O	NC	NC	NC
B12	Normal I/O	NC	NC	NC
B13	Normal I/O	NC	NC	NC
C12	Normal I/O	NC	NC	NC
C13	Normal I/O	NC	NC	NC
D12	Normal I/O	Normal I/O	NC	NC
D13	Normal I/O	NC	NC	NC
xx	I/O, Clock capable	Not available in limited connectors. Refer to the HAPS-70 and HAPS-80 reference manuals*.		I/O, Clock capable
xx	I/O, Clock capable			
xx	I/O*			
Reset_n	Reset			
VRP	Reference pins for DCI I/O-Standards, Normal I/O otherwise.			
VRN				
C0N	Global clocks			
C0P				
C1N				
C1P				
Uin0	LPC UMRBus signals			
Uin1				
Uout0				
Uout1				
Rsb	Reserved for side band signal expansion			
3.3	3.3V			
V	VCCO			
Vn	VCCO negotiation			
Idx	Identification clock, data and address			

* Some restrictions apply for limited connectors. Refer to your HAPS-80 or HAPS-70 system reference manual for information about limited connectors and correct daughter board placement.

Figure 5: HapsTrak Connector Pin Definitions

JX1, JX2, and JX3

JX1	
Pin	Signal
A0	DDR3_DQ[8]
A1	DDR3_DQ[9]
A2	DDR3_DQ[3]
A3	DDR3_DQ[6]
A4	DDR3_DQ[7]
A5	DDR3_DQ[0]
A6	DDR3_DQS_P[0]
A7	DDR3_DQS_N[0]
A8	DDR3_DQ[1]
A9	DDR3_DQ[4]
A10	DDR3_DQ[5]
A11	DDR3_DQ[2]
B0	DDR3_DM[1]
B1	-
B2	DDR3_DQ[11]
B3	DDR3_DQ[14]
B4	DDR3_DQS_P[1]
B5	DDR3_DQS_N[1]
B6	DDR3_DQ[15]
B7	DDR3_DQ[10]
B8	DDR3_DQ[12]
B9	DDR3_DQ[13]
B10	DDR3_DM[0]
B11	-
C0	DDR3_DQ[18]
C1	DDR3_DQ[23]
C2	DDR3_DQS_P[2]
C3	DDR3_DQS_N[2]
C4	DDR3_DQ[17]
C5	DDR3_DQ[20]
C6	DDR3_DQ[21]
C7	DDR3_DQ[16]
C8	DDR3_DM[2]
C9	DDR3_RESET_B
C10	DDR3_DQ[24]
C11	DDR3_DQ[28]
D0	DDR3_DQ[19]
D1	DDR3_DQ[22]
D2	DDR3_DQ[27]
D3	DDR3_DQ[31]
D4	DDR3_DQS_P[3]
D5	DDR3_DQS_N[3]
D6	DDR3_DQ[30]
D7	DDR3_DQ[26]
D8	DDR3_DQ[29]
D9	DDR3_DQ[25]
D10	DDR3_DM[3]
D11	-

JX2	
Pin	Signal
A0	DDR3_CK_P[1]
A1	DDR3_CK_N[1]
A2	-
A3	LED_GREEN
A4	-
A5	-
A6	LED_YELLOW
A7	LED_RED
A8	DDR3_ID_SDA
A9	DDR3_ID_SCL
A10	-
A11	-
B0	DDR3_CK_P[0]
B1	DDR3_CK_N[0]
B2	DDR3_CKE[1]
B3	DDR3_A[15]
B4	DDR3_A[14]
B5	DDR3_A[11]
B6	DDR3_A[6]
B7	DDR3_A[4]
B8	-
B9	DDR3_A[7]
B10	-
B11	-
C0	SYS_CLK_P
C1	SYS_CLK_N
C2	DDR3_CKE[0]
C3	DDR3_BA[2]
C4	DDR3_A[9]
C5	DDR3_A[5]
C6	DDR3_A[12]
C7	DDR3_A[8]
C8	DDR3_A[1]
C9	DDR3_A[3]
C10	DDR3_A[0]
C11	DDR3_A[2]
D0	DDR3_BA[0]
D1	DDR3_EVENT_B
D2	DDR3_S_B[0]
D3	DDR3_ODT[0]
D4	DDR3_BA[1]
D5	DDR3_RAS_B
D6	DDR3_S_B[1]
D7	DDR3_A[13]
D8	DDR3_A[10]
D9	DDR3_CAS_B
D10	DDR3_ODT[1]
D11	DDR3_WE_B

JX3	
Pin	Signal
A0	DDR3_DQ[55]
A1	DDR3_DQ[54]
A2	DDR3_DQ[62]
A3	DDR3_DQ[63]
A4	DDR3_DQ[58]
A5	DDR3_DQ[59]
A6	DDR3_DQS_P[7]
A7	DDR3_DQS_N[7]
A8	DDR3_DQ[61]
A9	DDR3_DQ[56]
A10	DDR3_DQ[60]
A11	DDR3_DQ[57]
B0	DDR3_DM[6]
B1	-
B2	DDR3_DQ[50]
B3	DDR3_DQ[51]
B4	DDR3_DQS_P[6]
B5	DDR3_DQS_N[6]
B6	DDR3_DQ[53]
B7	DDR3_DQ[52]
B8	DDR3_DQ[49]
B9	DDR3_DQ[48]
B10	DDR3_DM[7]
B11	-
C0	DDR3_DQ[47]
C1	DDR3_DQ[46]
C2	DDR3_DQS_P[5]
C3	DDR3_DQS_N[5]
C4	DDR3_DQ[42]
C5	DDR3_DQ[43]
C6	DDR3_DQ[40]
C7	DDR3_DQ[41]
C8	DDR3_DM[5]
C9	-
C10	DDR3_DQ[35]
C11	DDR3_DQ[38]
D0	DDR3_DQ[45]
D1	DDR3_DQ[44]
D2	DDR3_DQ[36]
D3	DDR3_DQ[37]
D4	DDR3_DQS_P[4]
D5	DDR3_DQS_N[4]
D6	DDR3_DQ[32]
D7	DDR3_DQ[33]
D8	DDR3_DQ[34]
D9	DDR3_DQ[39]
D10	DDR3_DM[4]
D11	-

Board Dimensions

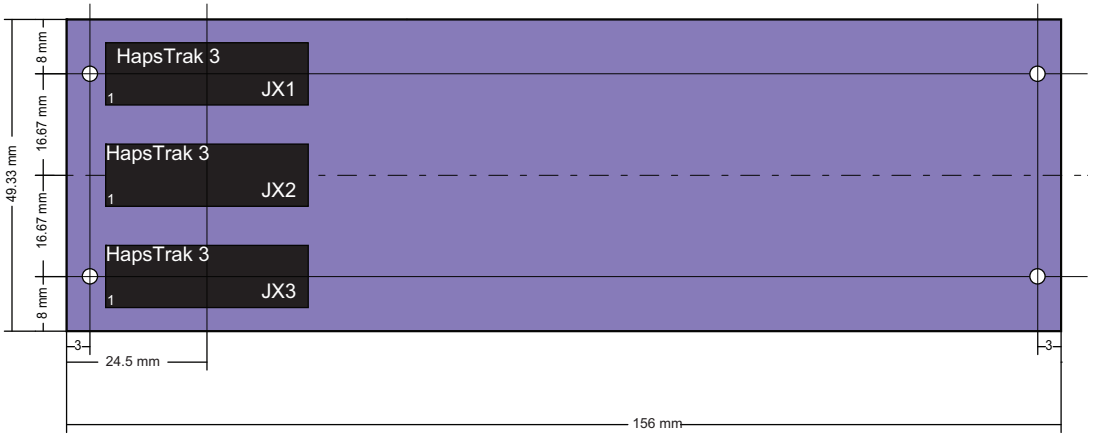


Figure 6: DDR3_SODIMM2R_HT3 Dimensions