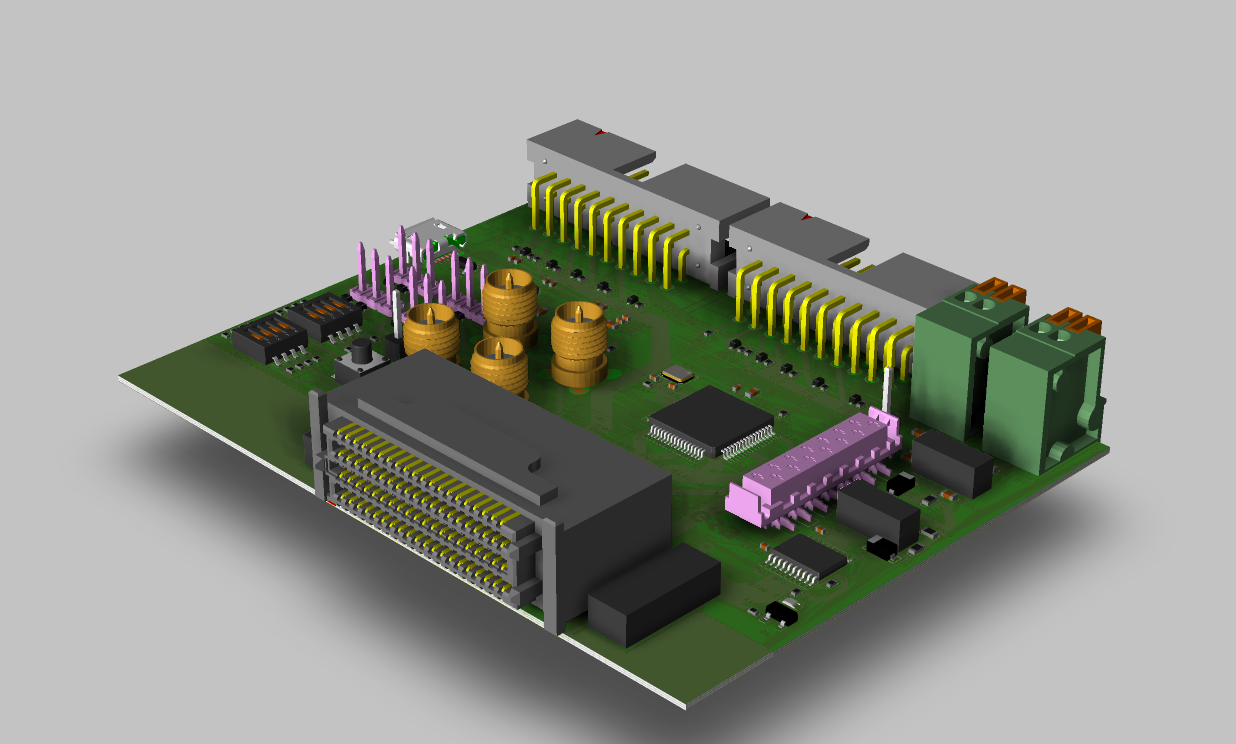
UART/JTAG/IO

HT3 Board

Reference Manual

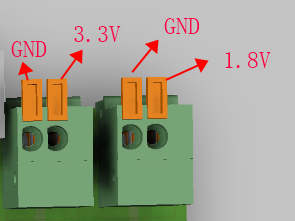


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| --- | --- |
| 项目： | MC20 |
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| 日期： | 2020/12/18 |

1. 硬件配置

板卡支持4路Debug\_UART，8路拨码开关，4路CLK接口，预留10路I/O，2路JTAG，支持UART-IR功能。(TFDU4301)

预留3.3V、1.8V对外供电接口。



1. 使用说明

UART功能通过Micro\_usb，供电。其他供电模块来自HAPAS板卡。

1. HT3 接口说明

|  |  |  |
| --- | --- | --- |
| HT3 PIN | Net Name | Description（VCCO:1.8V） |
| A0 | CLK\_3 | Reserved CLK |
| A1 | CLK\_4 | Reserved CLK |
| A2 | SW\_A2 | Default Hight |
| A3 | FPGA\_UART\_TX0 | UART |
| A4 | FPGA\_UART\_RX0 |
| A5 | FPGA\_UART\_RX1 |
| A6 | FPGA\_UART\_TX1 |
| A7 | FPGA\_UART\_RX3 |
| A8 | FPGA\_UART\_TX2 |
| A9 | FPGA\_UART\_TX3 |
| A10 | FPGA\_UART\_RX2 |
| A11 | FPGA\_IR\_RX\_2 | O |
| A12 | / | NC |
| A13 | / |
| B0 | SW\_B0 | Default Hight |
| B1 | SW\_B1 | Default Hight |
| B2 | SW\_B2 | Default Hight |
| B3 | B3 | I/O |
| B4 | B4 | I/O |
| B5 | TRST\_1 | JTAG\_1 |
| B6 | B6 | I/O |
| B7 | TDI\_1 | JTAG\_1 |
| B8 | TMS\_1 | JTAG\_1 |
| B9 | FPGA\_SD\_2/ | I |
| B10 | TDO\_1 | JTAG\_1 |
| B11 | FPGA\_IR\_TX\_2 | I |
| B12 | / | NC |
| B13 | / |
| C0 | CLK\_1 | Reserved CLK |
| C1 | CLK\_2 | Reserved CLK |
| C2 | SW\_C2 | Default Low |
| C3 | C3 | I/O |
| C4 | C4 | I/O |
| C5 | C5 | I/O |
| C6 | SW\_C6 | Default Low |
| C7 | C7 | I/O |
| C8 | TCLK\_1 | JTAG\_1 |
| C9 | FPGA\_SD\_1 | I |
| C10 | C10 | I/O |
| C11 | FPGA\_IR\_RX\_1 | O |
| C12 | / | NC |
| C13 | / |
| D0 | SW\_D0 | Default Low |
| D1 | TMS\_2 | JTAG\_2 |
| D2 | TCK\_2 | JTAG\_2 |
| D3 | TDO\_2 | JTAG\_2 |
| D4 | TDI\_2 | JTAG\_2 |
| D5 | TRST\_2 | JTAG\_2 |
| D6 | SW\_D6 | Default Low |
| D7 | D7 | I/O |
| D8 | D8 | I/O |
| D9 | FPGA\_IR\_TX\_1 | I |
| D10 | SW\_CTRL | I |
| D11 | LED\_CTRL | O |
| D12 | / | NC |
| D13 | / |