S2C Dual Virtex-7 TAI LM Hardware Reference Manual V1.06

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1. Revision History

Version	Date	Notes	Author
1.00	2012/06/06	Draft	Calfort
1.01	2012/07/23	1. Add chapter 8.7,8.8 2. Update Figure 4-2, Figure 5-2, Figure 6-1, Figure 6-2	Tony
1.02	2012/09/06	1. Update chapter 8.7,8.8 2. Update Figure 4-2, Figure 5-2, Figure 6-1, Figure 6-2 3. Update chapter 7 4. Update table 8-1 5. Update Figure 9-6 and Figure 9-7 6. Update table 8-4	Tony
1.03	2013/2/22	1. Update chapter 3 2. Change Total Available I/O in table 4-1 from 1500 to 1524	Tony
1.04	2013/5/22	1. Add VRN/VRP pin definition on dedicated I/O connector table	Tony
1.05	2014/2/10	1. Modify top side LM connector from Samtec 128-pin connector to Samtec 120-pin connector 2. Add QSH-060-01-F-D-A footprint 3. Add pin location of J1.037, J1.039, J11.037,J11.039 in table 8-2	Calfort
1.06	2014/05/19	1. Add Global Clock Properties usage note under table 8-1 2. Add virtual IO description in sections 8.11	Tony

2. Introduction

The S2C Dual Virtex-7 TAI Logic Module is designed for rapid SoC/ASIC prototyping and support using TAI IP – a configurable FPGA-based IP format – to efficiently create prototype designs. The Dual S2C Virtex-7 TAI Logic Module can hold designs up to 40M ASIC gates with two Xilinx Vitex-7 2000T FPGA devices and has both on-board DDR3 SO-DIMM socket and DDR2 SO-DIMM socket to meet a variety of high-speed memory applications. The Virtex-7 TAI Logic Module now supports 32 channels of high speed Gigabit transceivers capable of running up to 6Gbps for a variety of high-speed interfaces such as PCIe, SATA and XAUI. In addition to our existing USB2.0 port for our widely adopted runtime features such as FPGA download, programmable clock generations and self-test, the new Virtex-7 TAI Logic Module now supports these runtime features through Ethernet interface so you can remotely control your FPGA hardware.. S2C has also added a number of new runtime features such as I/O voltage settings and clock frequency read back through software control.

Figure 2-1 V7 TAI Logic Module - Top View

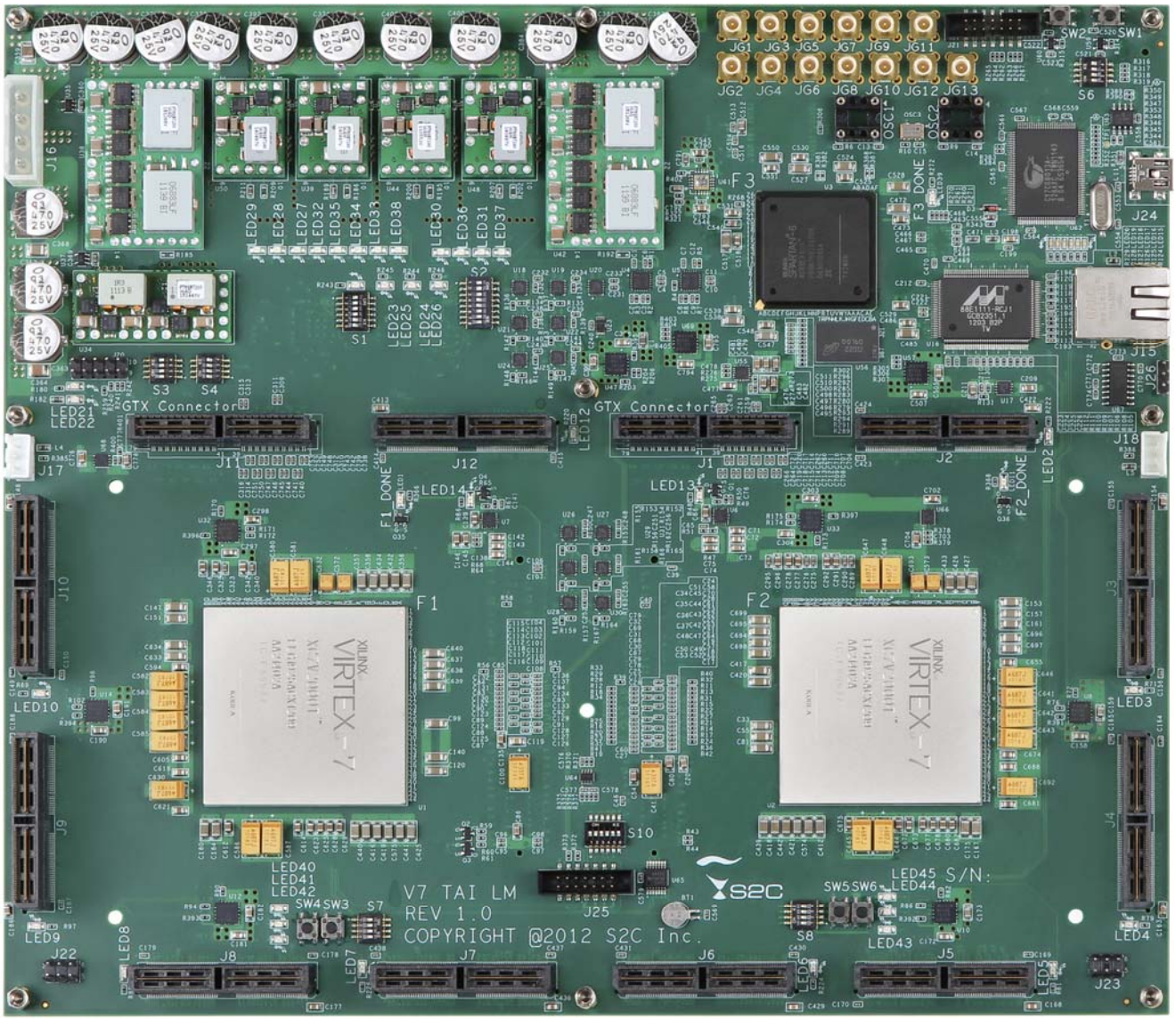
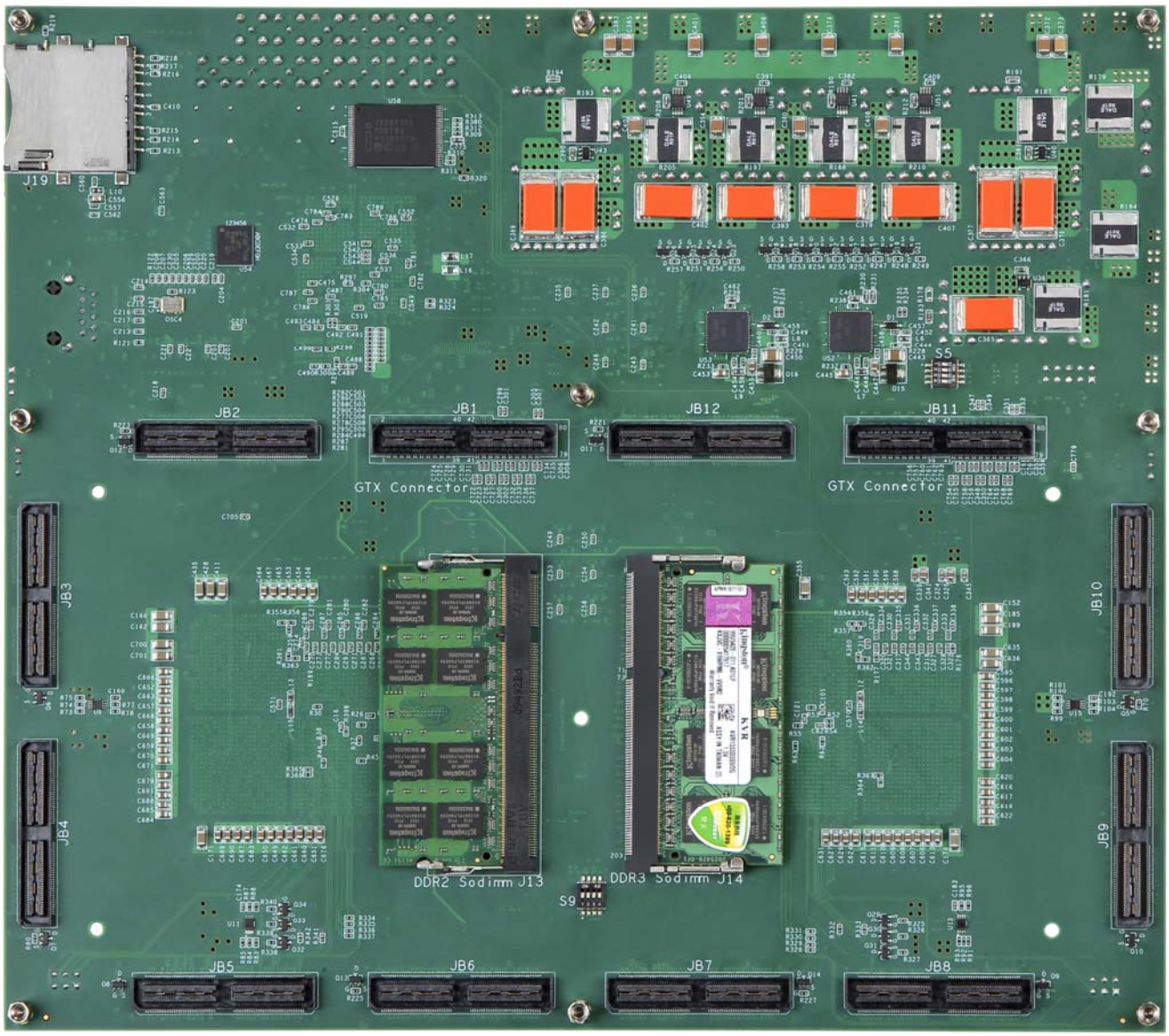


Figure 2-2 V7 TAI Logic Module – Bottom View



The Virtex-7 TAI Logic Module is equipped with XC7V2000TFLG1925. Dual Virtex-7 Logic Module fits up to 40 million ASIC gates; Single Virtex-7 Logic Module fits up to 20 million ASIC gates;

Virtex-7 TAI Logic Module provides a number of prototyping benefits, allowing you to:

- Fully validate your SoC/ASIC designs using FPGA based prototypes
- Start software and firmware development earlier in process using FPGA based prototypes
- Shorten time-to-prototype by eliminating time-consuming design your own FPGA prototype boards
- Avoid operational risk from designing your own FPGA based prototypes
- Lower your cost by buying off-shelf versus building your own FPGA based prototypes
- Stack or tile multiple logic modules for design scalability and expansion
- Reuse multiple times
- Utilize a number of optional features to enhance your design and verification results

2.1 General Features

The Dual Virtex-7 TAI Logic Module hardware's general features are listed as follows:

- Capacity
  - Up to 40M ASIC gates
  - Up to 90Mbits of FPGA internal memory
  - Up to 4320 embedded DSP48E1 slices
  - On-board DDR2 and DDR3 SO-DIMM sockets
  - Can expand through the use of samtec cables, interconnection modules and mother board
- 14 global clocks distributed to 2 FPGA, can be selected from:
  - 6 pairs of differential programmable clock sources (0.16~710MHz)
  - 6 pairs of differential SMB clock inputs
  - 6 pairs of differential feedback clocks from any of the two user FPGAs
  - 2 single-ended oscillator sockets
- 1 Global Reset sourced from push button, SMB or software-control
- Flexible & Powerful I/O
  - Each FPGA can access up to 1002 external I/Os
  - 360 Dedicated I/Os per FPGA
  - 480 Shared I/Os between two FPGAs
  - 50 Inter-FPGA connections between two FPGAs
  - Dedicated I/O voltage can be adjusted to 1.2V, 1.5V, 1.8V through runtime software through GUI
- High Speed Transceivers
  - Each FPGA has 16 Gigabit Transceivers with total of 32 Gigabit Transceivers
  - Gigabit Transceivers can run up to 6Gbps through 4 high speed differential connectors
- Length matched, 50-ohm Single-ended impedance and 100-ohm differential impedance to all Samtec connectors
- Supports PC switching power supply input
- Power On/Off switch on power switch daughter board
- FPGA voltage, current and temperature detection and alarm mechanism
- Push button for FPGA design reset
- Fan cooling on board with PWM control
- FPGA configuration -4 options
  - Xilinx JTAG interface
  - Easy configuration through USB interface from S2C TAI Player runtime software
  - FPGA downloading from on-board SD card
  - FPGA downloading from Ethernet interface
- Self-test program
  - TAI Player runtime software ensure thorough self-test of all pins of each FPGA

- Support Battery back-up encryption key
- TAI Player Runtime software provides a number of useful utilities -
  - Generate programmable clocks Adjust dedicated I/O voltages Software wizard guides user through self-tests
  - Read back global clock frequency Ability to program SD card which could plug directly into your TAI LM

2.2 Technical Support

The S2C technical support center is located in world-wide. Please contact our technical support through one of the methods below. Please have your TAI Logic Module serial number ready when you contact us. The serial number is labeled on the lower right-hand corner of your TAI Logic Module.

- Telephone

For live technical assistance, call our support hotline at +86 (21) 6887-9287 from 9:00 am to 6:00 pm (Shanghai Time), Monday to Friday. Our support engineers speak English and Mandarin Chinese.

- E-mail

You can also send any queries to our e-mail address: support@s2cinc.com. Our support staff will respond within one business day.

In addition, ask your local sales channel about local support services available to you.

US Customers:

- Telephone

For live technical assistance, call our support hotline at +1 (408) 213 8818 extension 820 from 9:00 am to 6:00 pm (PST), Monday to Friday.

- E-mail

You can also send any queries to our e-mail address: support_us@s2cinc.com. Our support staff, in most cases, will respond within one business day.

In addition, ask your local sales channel about local support services available to you.

3. Examining Contents

The S2C Virtex-7 TAI Logic Module package includes:

- One S2C Virtex-7 TAI Logic Module (with two XC7V2000TFLG1925 FPGAs)
- Two S2C I/O testing boards
- One S2C GTX IO testing board
- One S2C DDR22IO board
- One S2C DDR32IO board
- One power switch control board
- One 2-wire external module power output connector
- One 3-wire external module power output connector
- One PC power supply (Input AC 100~240V; Output DC 12V, 16A)
- Two Acrylics with some plastic standards and rubber cap of LM connectors.
- Two cooling fans
- One USB cable
- One SD card
- One Ethernet cable
- One Virtex-7 TAI Logic Module CD containing:

  S2C Virtex-7 TAI Logic Module Hardware Reference Manual

  S2C TAI Player Install Programmer
- One printed Warranty Statement
- One printed S2C Virtex-7 Important Usage Notice
- One S2C Virtex-7 TAI Logic Module packing list
- One printed S2C Virtex-7 TAI Logic Module test report
- One Virtex-7 TAI Logic Module carrying case

4. Hardware Description

4.1 Hardware Specifications

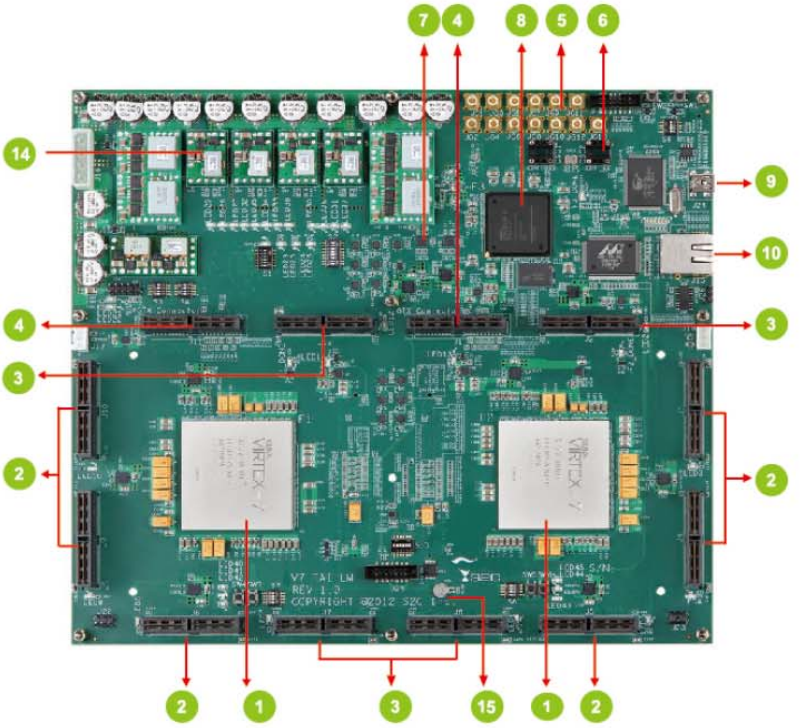
Virtex-7 TAI Logic Module's functional hardware specifications are described in the following table:

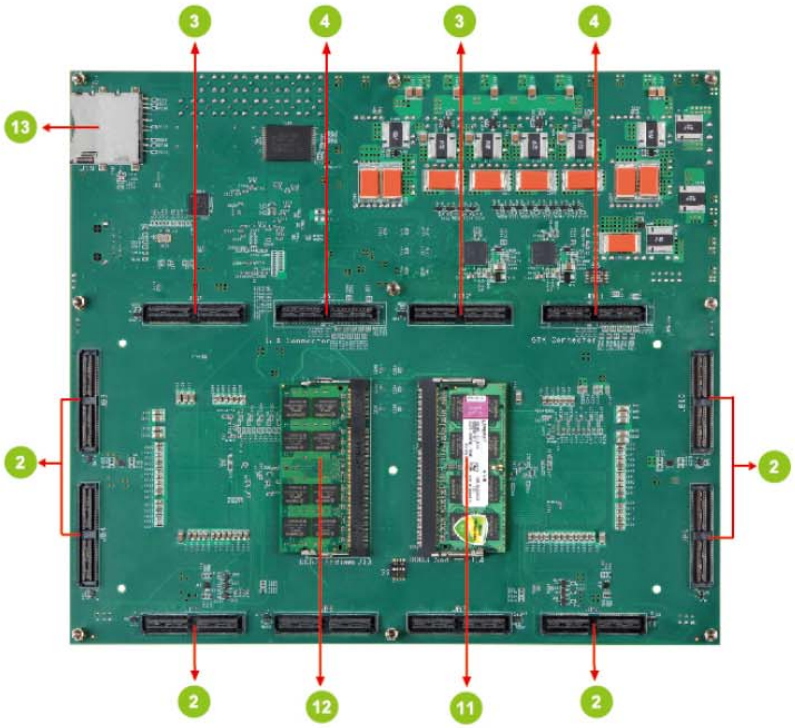
Table 4-1 **Functional Hardware Specifications**

FPGA Device Used	XC7V2000TFLG1925
Input Voltage	12V and 5V
Dedicated I/O Voltage	1.2~1.8V
Shared I/O Voltage	1.8V
Inter-FPGA connection Voltage	1.8V
Dedicated I/O	720
Shared I/O	480
Inter-FPGA connection	50
OSC Clock Input	2
SMB Clock Input	6
Programmable Clock Input	6
Feedback Clock	6
Global Clock	14
Total Available I/O	1524
Total transceiver	32
Size	260.0 mm(L) X 230.0 mm(W)
Power Supply	PC Switching power supply(12V@16A, 5V@16A)

4.2 Hardware Components

Figure 4-1 V7 TAI Logic Module Major Components, Top and Bottom View

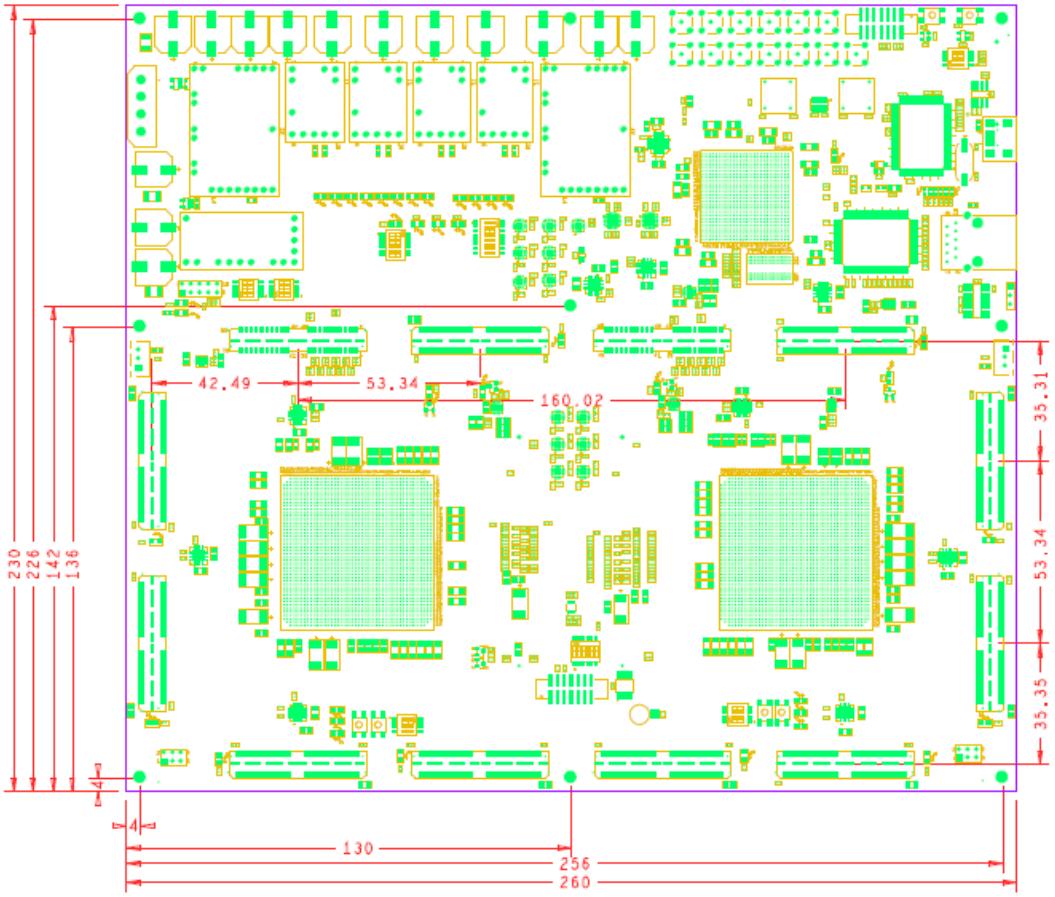




1. Xilinx Virtex-7 FPGA
2. Dedicated I/O
3. Shared I/O
4. GTX Connectors
5. SMB CLK In & Out
6. 2 Oscillator Sockets
7. Programmable Clock Generator
8. LM Controller
9. USB Interface to PC
10. Giga-Ethernet port to PC
11. DDR3 SODIMM Socket
12. DDR2 SODIMM Socket
13. SD Card Socket
14. Power Module
15. Battery for Encryption

4.3 Physical Dimensions

Figure 4-2 V7 TAI Logic Module Physical Dimensions



5. Hardware Architecture

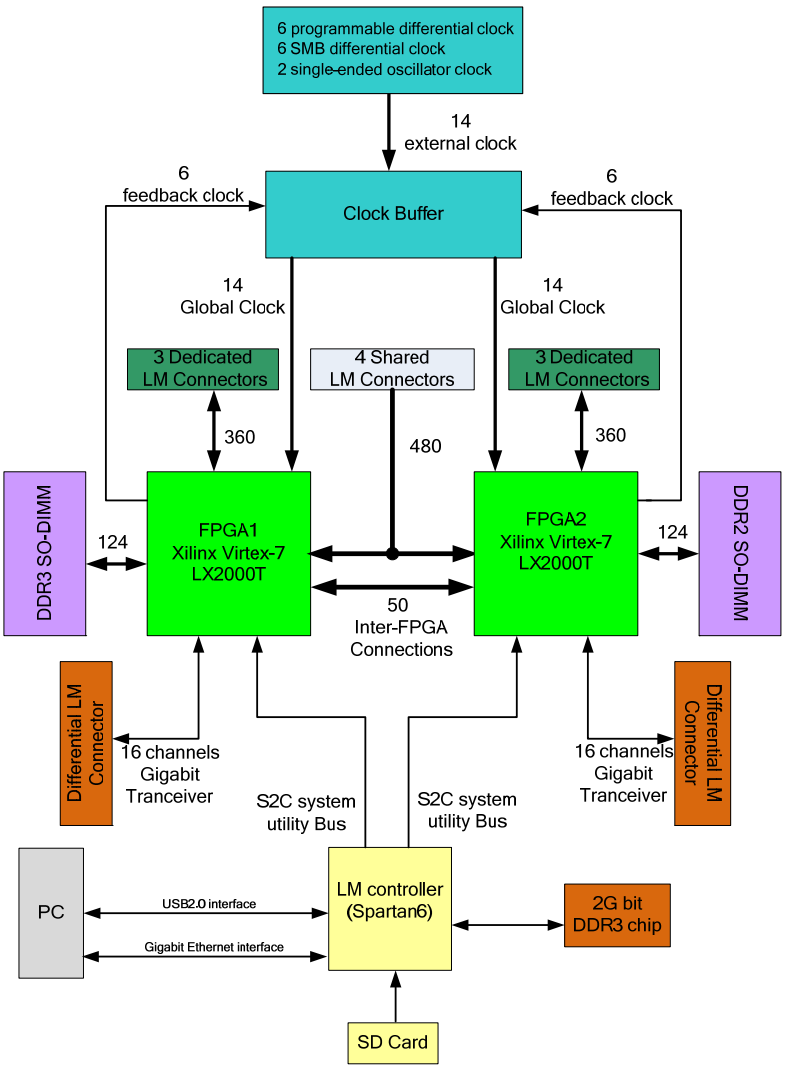
The Virtex-7 TAI Logic Module's hardware architecture is designed with both scalability and flexibility in mind. When only one TAI Logic Module is used, almost all I/Os are brought out for maximum flexibility. When capacity expansion is needed, multiple TAI Logic Modules can expand through the use of Samtec cables, interconnection modules or mother board. In addition, the Virtex-7 TAI Logic Module also includes components that are reserved for the function interface, which enables advanced features such as dynamic interconnect bus technology, embedded integrated logic analyzer, powerful clock generation, co-emulation with simulators, and transaction-based co-modeling.

This section illustrates Virtex-7 TAI Logic Module's general, clock, and I/O architectures.

5.1 General Architecture

The general architecture of the basic system components and their connections are as follows:

Figure 5-1 V7 TAI Logic Module General Architecture



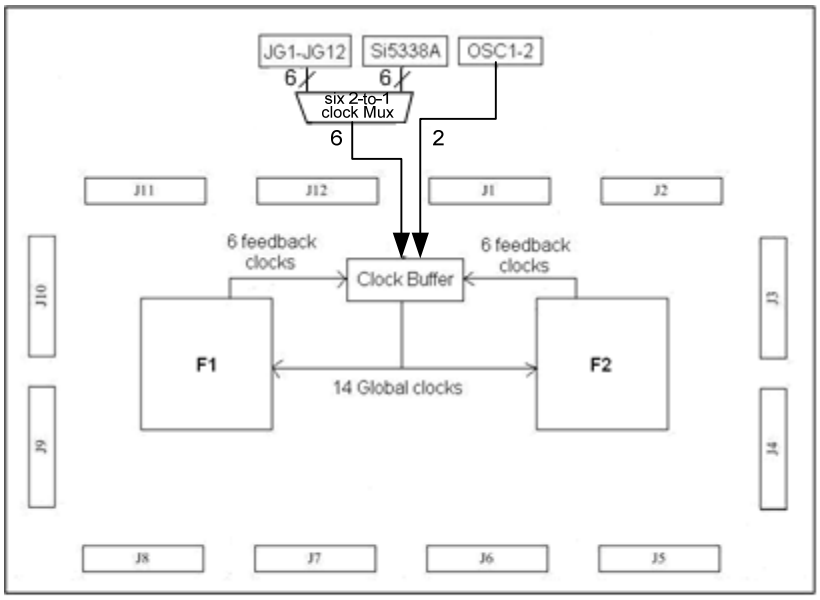
5.2 Clock Architecture

A total of 14 global clocks can be input from 2 oscillator sockets, 6 pairs of programmable differential clocks or 6 pairs of SMB differential clocks, and 6 pairs of feedback differential clocks from any of the two user's FPGAs.

6 pairs of programmable differential clocks and 6 pairs of SMB differential clocks are respectively selected through runtime software in GUI.

6 pairs of feedback differential clocks from any of the two user's FPGAs are also respectively selected through runtime software in GUI.

Figure 5-2 V7 TAI Logic Module External Clock Architecture

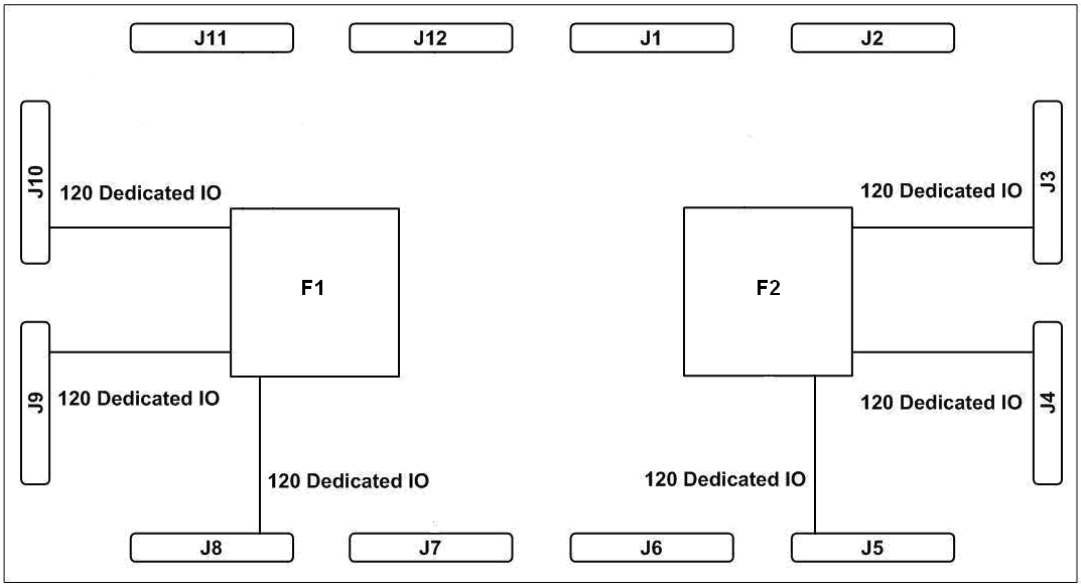


5.3 I/O Architecture

V7 TAI Logic Module contains 6 I/O types: Global clock I/O, Gigabit transceivers I/O, Dedicated I/O, Shared I/O, Inter-FPGA connection and DDR2/DDR3 SO-DIMM I/O.

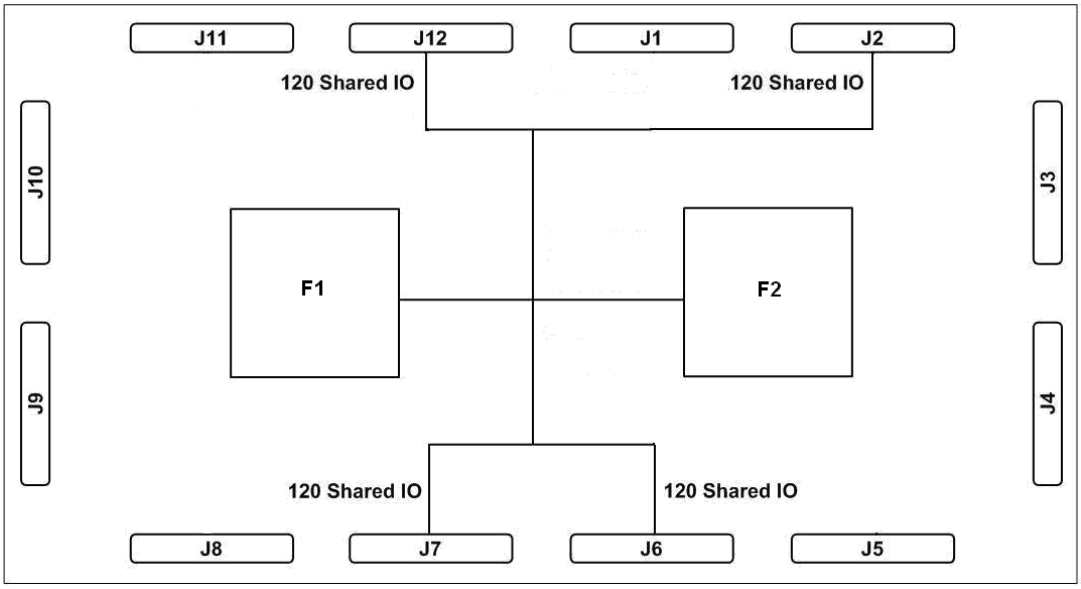
Dedicated I/Os are connected to only one of the two FPGA; each FPGA has 360 dedicated I/Os through three Samtec 120-pin connectors.

Figure 5-3 V7 TAI Logic Module Dedicated I/O Architecture



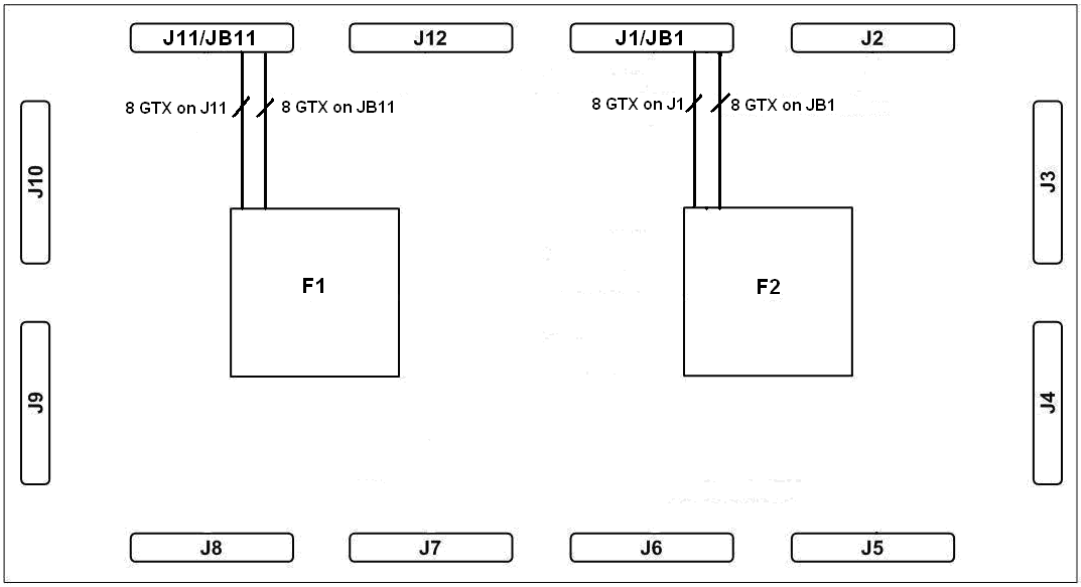
Shared I/Os are connected to both F1 and F2 and also fetched out to four Samtec 120-pin connectors; there are a total of 480 shared I/Os.

Figure 5-4 V7 TAI Logic Module Shared I/O Architecture



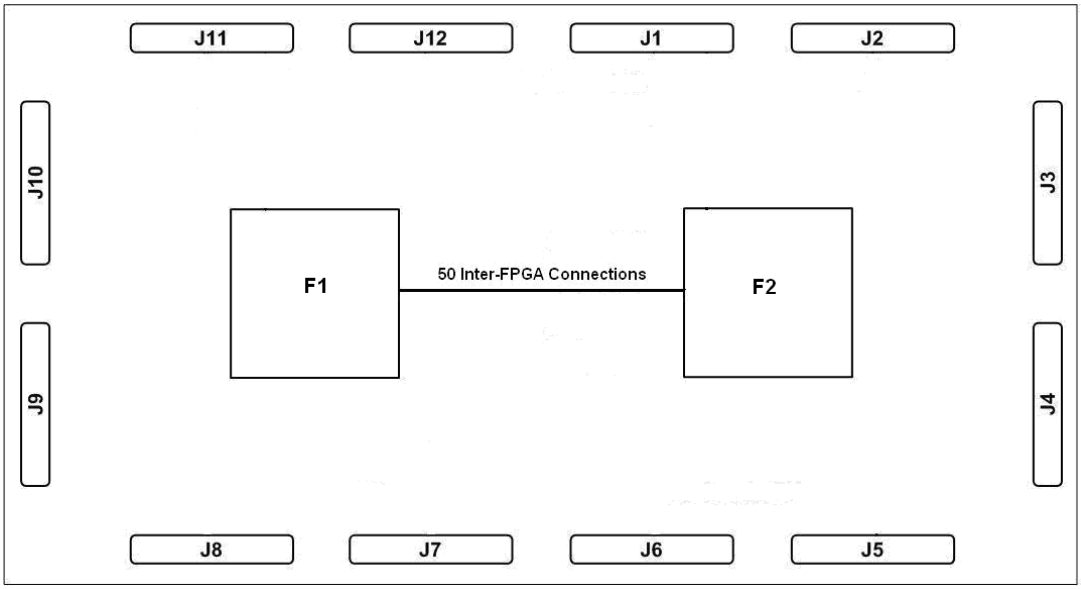
Gigabit transceivers I/O are connected to only one of the two FPGAs; each FPGA has 16 channels gigabit transceivers through two Samtec 80-pin differential connectors. That means J1 and JB1 aren't connected together; J11 and JB11 aren't connected together too.

Figure 5-5 V7 TAI Logic Module Gigabit transceivers I/O Architecture



Inter-FPGA connections are directly connected between F1 and F2; there are a total of 50 Inter-FPGA connections. The voltage of Inter-FPGA connections is fixed to 1.8V. We recommend using LVDS on these Inter-FPGA connections for higher performance requirement.

Figure 5-6 V7 TAI Logic Module Inter-FPGA Connections Architecture



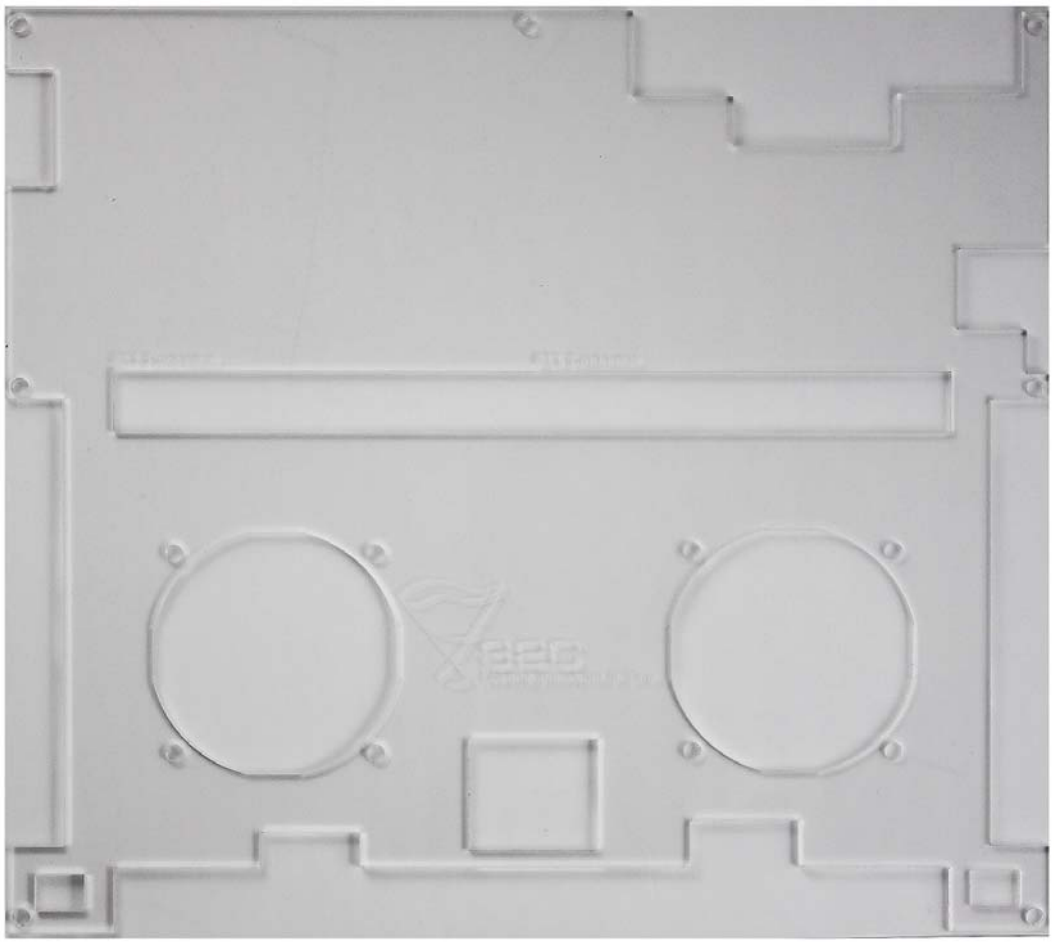
6. Hardware Setup

6.1 Setting Up Hardware

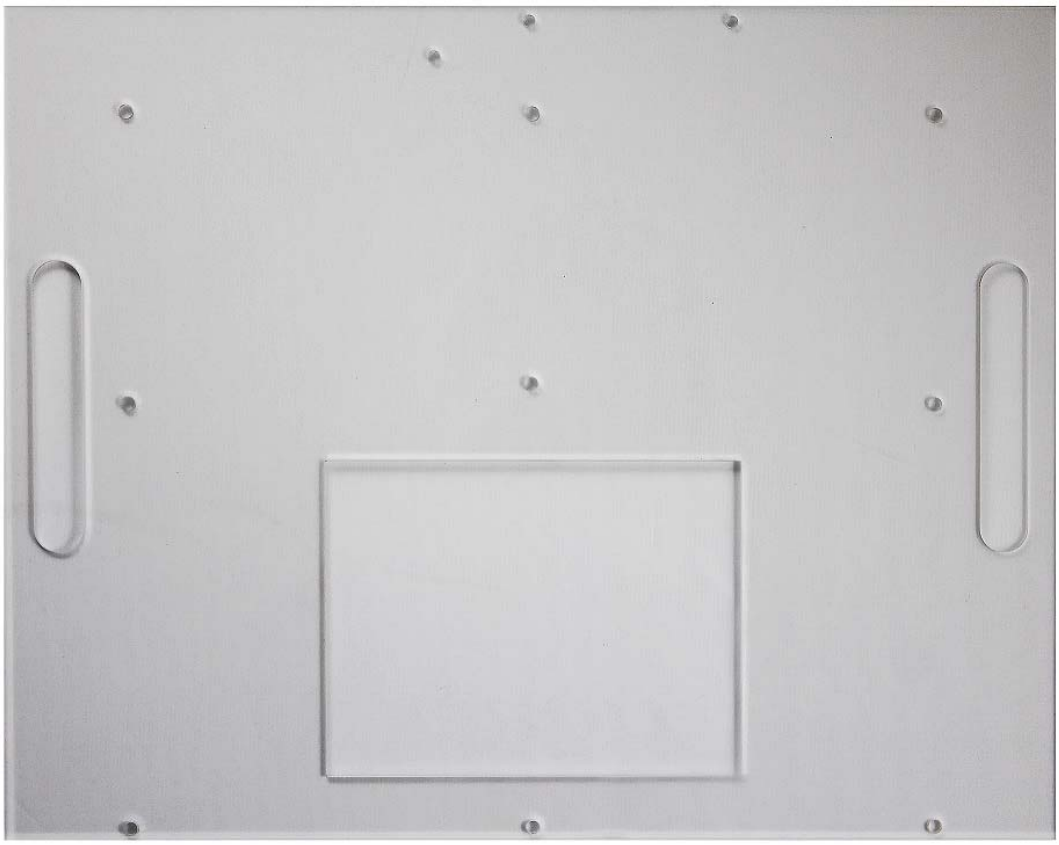
Setting up V7 TAI Logic Module is simple and straightforward.
First, fit a plastic spacer at each corner of the TAI Logic Module. After the spacers are fitted, you need to install acrylic board next. The acrylic board is divided into bottom and top acrylic plates. The top acrylic plate is used to protect the components on the board that are not used by user during normal course of operation, and the bottom acrylic board is meant to firmly hold the main board and power switch daughter board.

After the spacers are fitted, you need to install acrylic board next. The acrylic board is divided into bottom and top acrylic plates. The top acrylic plate is used to fix the fan, and the bottom acrylic board is meant for the main board and power switch daughter board.

Figure 6-1 V7 TAI Logic Module Top Acrylic Board



V7 TAI Logic Module Bottom Acrylic Board

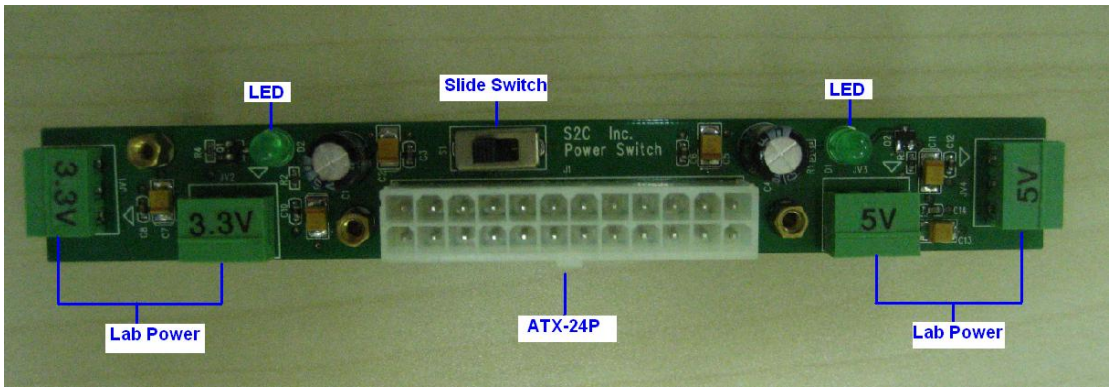


In addition we have two fans with PWM control to cool the two the Virtex-7 FPGAs. These two fans are connected to the J17 and J18.

After the acrylic boards have been fitted, connect the PC Switching power supply to V7 TAI Logic Module and then plug power supply to a power outlet. The power supply supports up to 16A of current. Lastly slides switch S1 (on power switch daughter board) into “on” position to turn on the 12V power source.

The main function of power switch daughter board is to turn on or turn off 12V power source from PC Switching power supply through the mounted slide switch S1. When switch S1 is in “on” position, LED D1 and D2 are illuminated. Additionally this board offers two +3.3V lab power (PV1 & PV2) and two +5V lab power (PV3 & PV4), which could provide power sources to customer’s daughter boards. The pin1 of PV1 & PV2 is +3.3V and pin2 is GND (pin3 is not connected). The pin1 of PV3 & PV4 is +5V and pin2 is GND (pin3 is not connected). The maximum output current of PV1/PV2/PV3/PV4 are around 1A. Figure 5-5 shows the power switch daughter board.

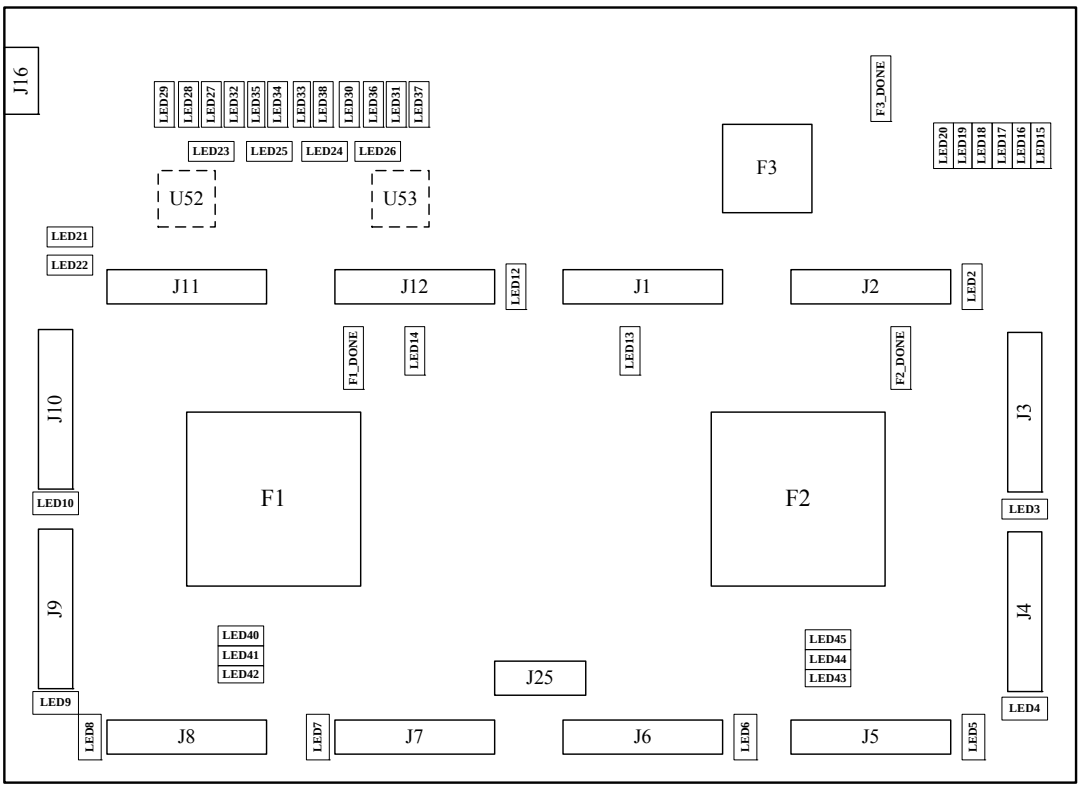
Figure 6-2 Power switch daughter board



After the acrylic plates have been fitted, we should first connect the ATX-24P cable of ATX power supply to the power switch daughter board, and then connect the ATX peripheral cable (4-pin Molex cable) of ATX power supply to TAI Logic Module. Lastly we slide switch S1 (on power switch daughter board) into “on” position to turn on the 12V power source. The 12V power source supports up to 16A of current.

Once the V7 TAI Logic Module is powered on, the power status LED21, LED22 will light up. Then you will find LED39 (F3_DONE) will light up. It indicates that S2C’s bit file has been downloaded to Spartan-6 controller successfully. If any of the red LEDs from LED27, LED28, LED29, LED30, LED31, LED32, LED33, LED34, LED35, LED36, LED37, and LED38 are “ON”, **it indicates a power fault has occurred**. You must shut down the power of V7 TAI LM immediately.

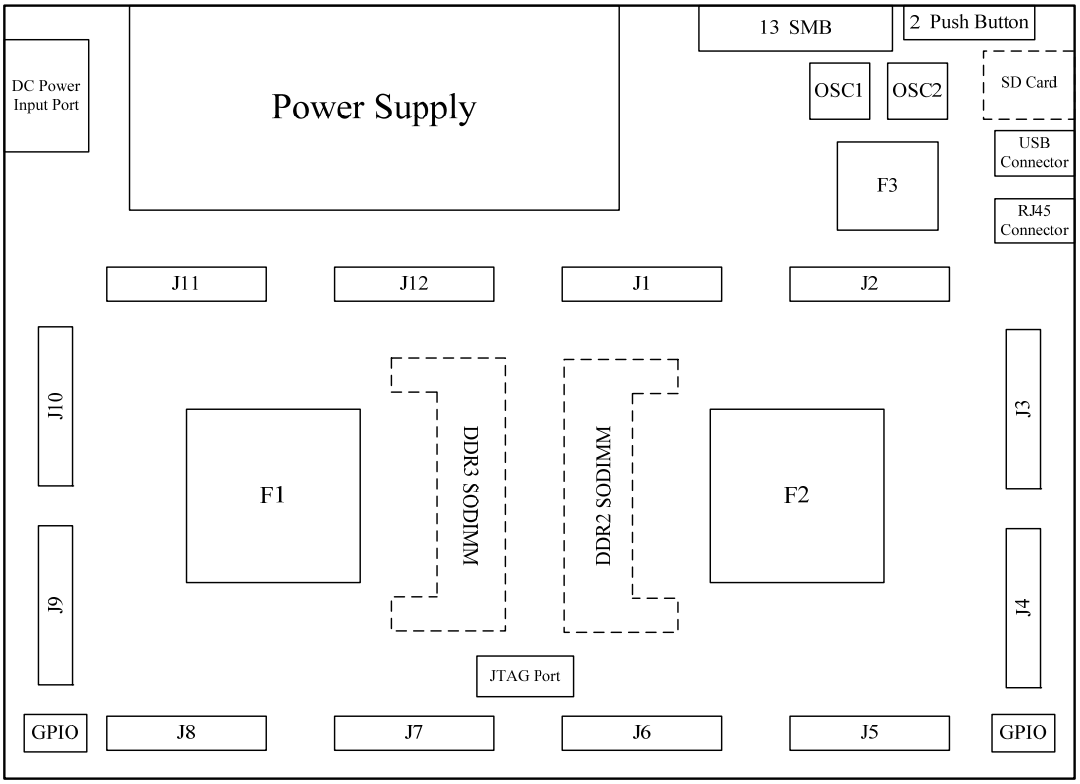
Figure 6-3 V7 TAI Logic Module LED Locations



Please note that when the FPGA is powered on, the temperature may rise. V7 TAI Logic Module supports temperature monitor capability which powers down V7 TAI Logic Module when the temperature surpasses the prescribed limit. Please take adequate care and follow safety

guidelines discussed in Section 10, “Care and Handling”, to avoid Xilinx Virtex-7 FPGA overheating. Contact S2C for support. We will provide you additional solutions for your overheating problem.

Figure 6-4 V7 TAI Logic Module Setup Configuration



If your design requires interfacing with a target board, it can be directly mounted onto V7 TAI Logic Module or connected through a Samtec 120-pin cable (refer to *Figure 8-1 TAI Logic Module External Connector Locations* for more details).

6.2 Dedicated I/O Voltage Adjusting

All 720 dedicated I/O voltages can be easily adjusted to 1.2V, 1.5V or 1.8V through software control. F1 has 360 dedicated I/Os that can be accessed from Samtec 120-pin connectors J8, J9, and J10; F2 also has 360 dedicated I/Os that can be accessed from Samtec 120-pin connectors J3, J4, and J5.

The dedicated I/Os are separated into 4 power regions, each is controlled by Spartan-6 controller. J5 and J8 have different power regions individually; J3 and J4 share the same power region; J9 and J10 share the same power region also. Once powered on, Spartan-6 controller will configure the dedicated I/O voltages according to the last configuration.

6.3 Shared I/O Voltage and Inter-FPGA Connections Voltage

All 480 shared I/Os are fixed to 1.8V and couldn’t be adjusted through runtime software in GUI.

In addition all 50 inter-FPGA connections are fixed to 1.8V and couldn’t be adjusted through runtime software in GUI.

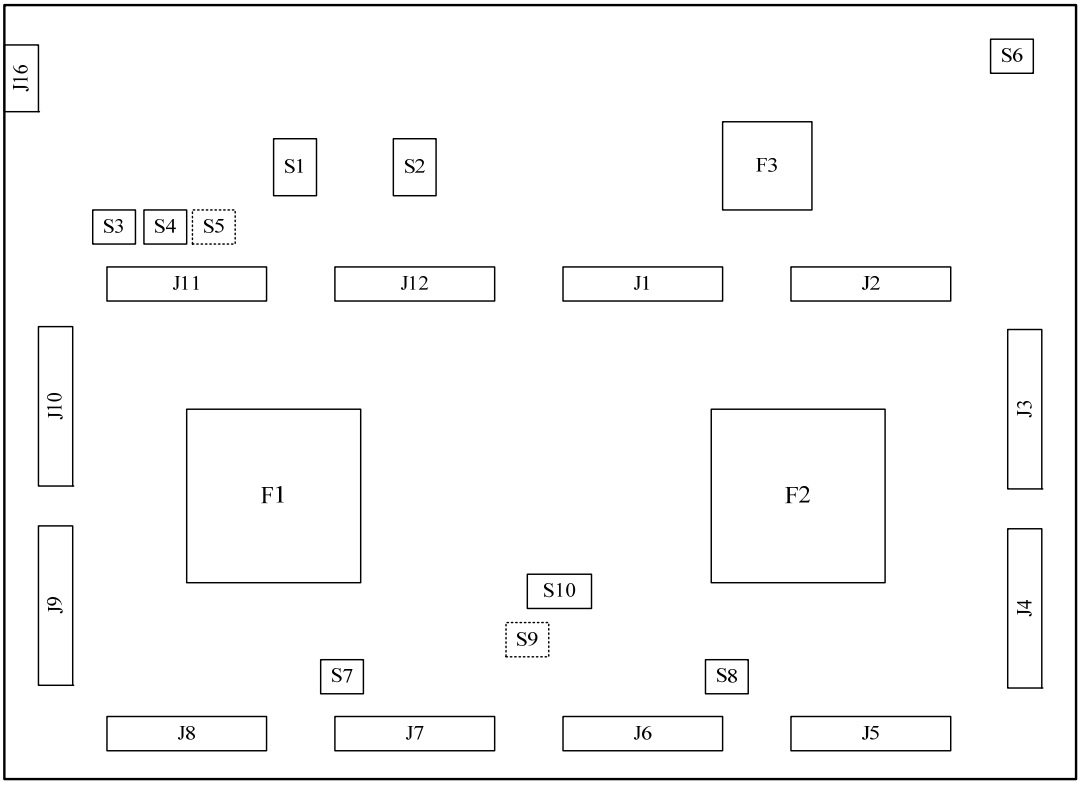
Table 6-1 displays the default configuration for all switches; please do not change the default value unless you have confirmed it with S2C's support team

Table 6-1 **Switch Default Configuration**

Switch	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
S1	ON	ON	ON	ON	ON	ON	—	—
S2	ON	ON	ON	ON	ON	ON	—	—
S3	ON	ON	ON	ON	—	—	—	—
S4	ON	ON	ON	ON	—	—	—	—
S5	ON	ON	ON	ON	—	—	—	—
S6	ON	ON	ON	OFF	—	—	—	—
S7	ON	ON	ON	ON	—	—	—	—
S8	ON	ON	ON	ON	—	—	—	—
S9	OFF	OFF	OFF	OFF	—	—	—	—
S10	ON	OFF	ON	OFF	ON	ON	—	—

Figure 6-6 illustrates the location of every switch on the V7 TAI Logic Module.

Figure 6-5 V7 TAI Logic Module Switch Locations



6.4 Downloading Hardware

You have 4 different options. You can download the design file into FPGA using an USB cable from TAI Player Runtime Software or using Xilinx Download cable or SD card or through remotely through Ethernet interface. For downloading design using USB cable and self-test, please refer to "S2C TAI Player Reference Manual". For downloading using Xilinx Download

cable, plug the Xilinx Download cable into JTAG connector J24 and refer to Xilinx documentation. (For JTAG pins and signal information refer to the appendix). A third option is to program SD card using TAI Player Pro and plug the SD card directly into the V7 TAI LM.

When F1 download is complete, LED1 (F1_DONE) will light up. When F2 download is complete, LED11 (F2_DONE) will light up.

Table 6-2 displays the default status for all LEDs; please check them after power on the V7 TAI Logic Module.

Table 6-2 **LED Default Status**

LED	Status	Description
LED1(Green)	ON	F1 download successfully
LED2(Green)	ON	Power supply of J2 connector is correct
LED3(Green)	ON	Power supply of J3 connector is correct
LED4(Green)	ON	Power supply of J4 connector is correct
LED5(Green)	ON	Power supply of J5 connector is correct
LED6(Green)	ON	Power supply of J6 connector is correct
LED7(Green)	ON	Power supply of J7 connector is correct
LED8(Green)	ON	Power supply of J8 connector is correct
LED9(Green)	ON	Power supply of J9 connector is correct
LED10(Green)	ON	Power supply of J10 connector is correct
LED11(Green)	ON	F2 download successfully
LED12(Green)	ON	Power supply of J12 connector is correct
LED13(Green)	ON	Power supply of DDR2 SO-DIMM is correct
LED14(Green)	ON	Power supply of DDR3 SO-DIMM is correct
LED15(Green)	ON	Ethernet TX status
LED16(Green)	ON	Ethernet RX status
LED17(Green)	ON	Ethernet DUPLEX status
LED18(Green)	ON	Ethernet 1000M link status
LED19(Green)	ON	Ethernet 100M link status
LED20(Green)	ON	Ethernet 10M link status
LED21(Green)	ON	DC 12V input is power good
LED22(Green)	ON	DC 5V input is power good
LED23(Green)	ON	Power supply status1 is correct
LED24(Green)	ON	Power supply status2 is correct
LED25(Green)	ON	Power supply status3 is correct
LED26(Green)	ON	Power supply status4 is correct
LED27(Red)	OFF	Power supply occur fault1
LED28(Red)	OFF	Power supply occur fault2
LED29(Red)	OFF	Power supply occur fault3
LED30(Red)	OFF	Power supply occur fault4
LED31(Red)	OFF	Power supply occur fault5
LED32(Red)	OFF	Power supply occur fault6
LED33(Red)	OFF	Power supply occur fault7
LED34(Red)	OFF	Power supply occur fault8
LED35(Red)	OFF	Power supply occur fault9
LED36(Red)	OFF	Power supply occur fault10

LED37(Red)	OFF	Power supply occur fault11
LED38(Red)	OFF	Power supply occur fault12
LED39(Green)	ON	F3 download successfully
LED40(Green)	OFF	User LED
LED41(Green)	OFF	User LED
LED42(Green)	OFF	User LED
LED43(Green)	OFF	User LED
LED44(Green)	OFF	User LED
LED45(Green)	OFF	User LED

7. TAI Player Runtime and Self-Testing

7.1 System Requirements

CPU:	x86 series, 500MHz or higher, 2GHz is recommended.
Memory:	512M, 1G or more is recommended.
Disk Space:	At least 200M bytes to install the software and firmware. (The majority of required disk space is occupied by working projects and not by the application itself.)
OS:	Microsoft Windows 2000/2003/XP/7 Linux RHEL4-x64(2.6.9-78.Elsmp)/RHEL5-x64(2.6.18-8.e15)

7.2 Third-Party Software Requirements

EDA Tools:	Xilinx ISE (mandatory) and Synplicity Synplify or Synplify Pro (optional).

7.3 TAI Player Installation

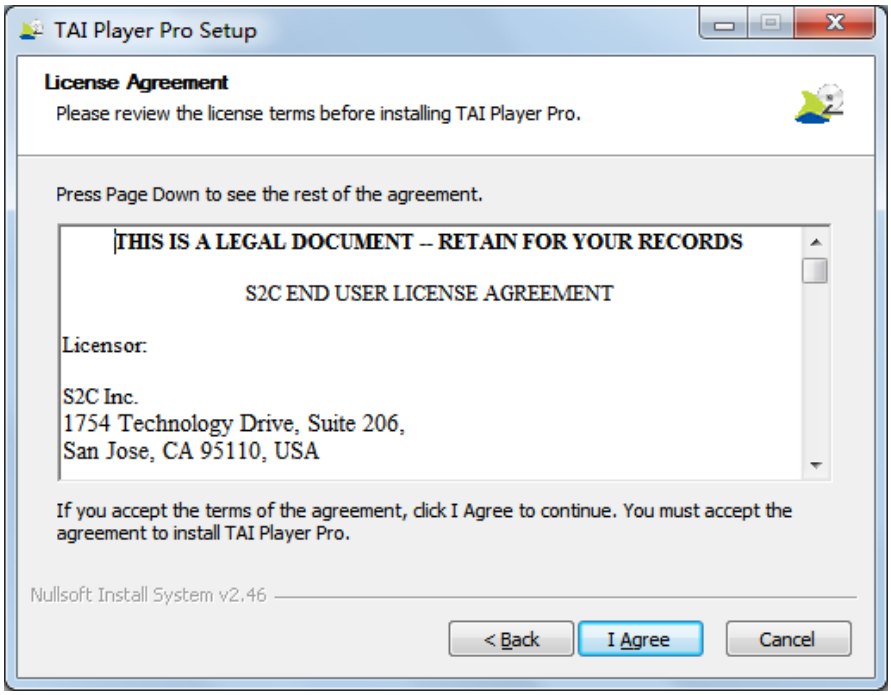
The installation process is illustrated in a step-by-step manner as follows:

Start up the installation executable and the Installation Wizard window will appear as follows:

Figure 7-1 TAI Player Setup Wizard

Press **Next**, and a license agreement page will be displayed:

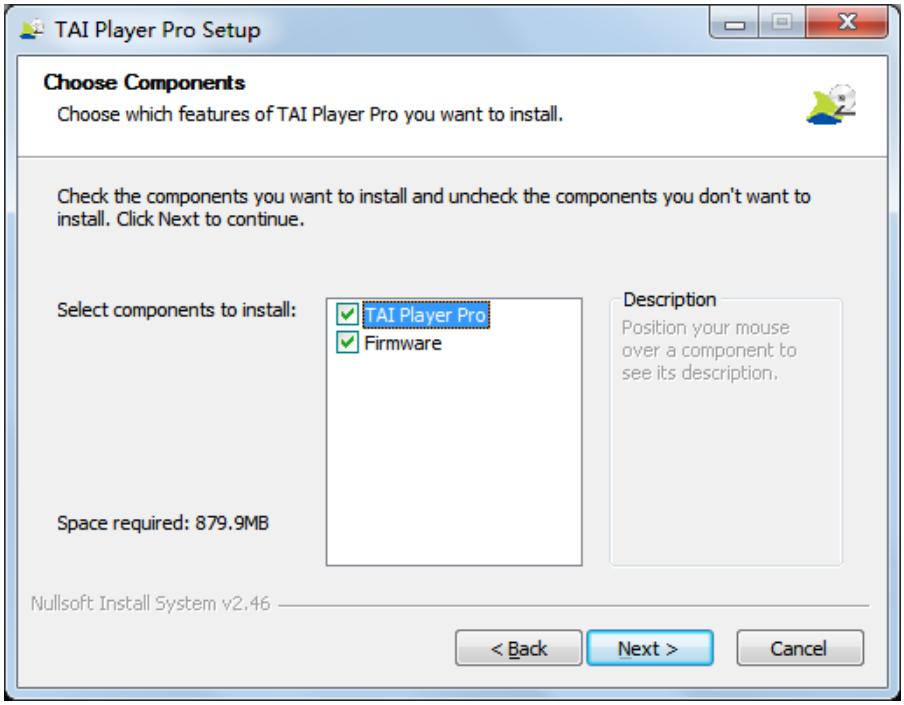
Figure 7-2 TAI Player Setup Wizard – License Agreement



Read the license agreement carefully and press **I Agree** to continue the installation process or **Cancel** to quit.

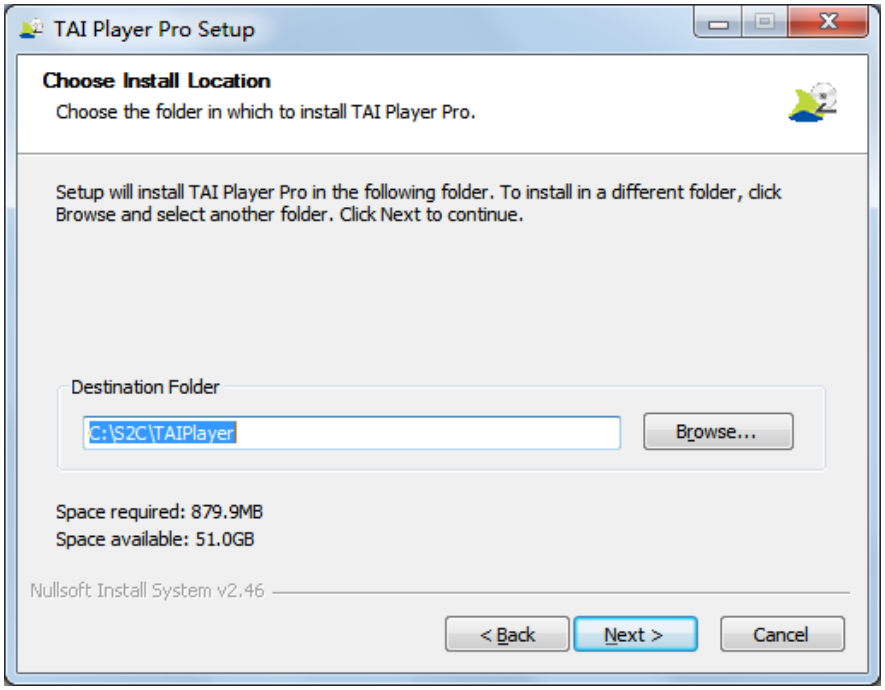
In the Choose Components window, leave the default parameters as is and click **Next** to precede.

Figure 7-3 TAI Player Setup Wizard – Choose Components



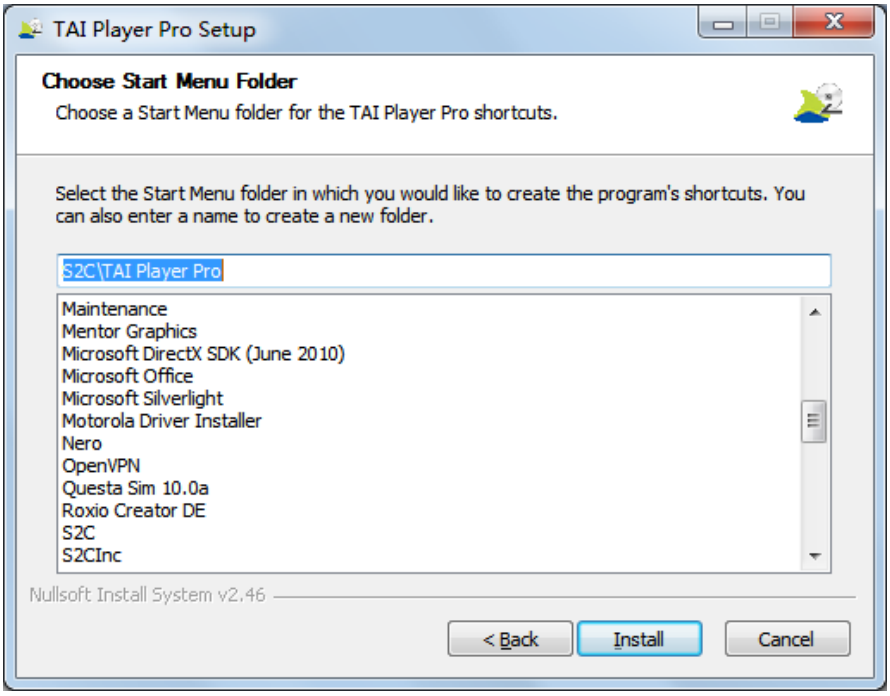
Now in the Choose Installation Location window, select the destination path you wish to save the TAI Player program in by using the **Browse** button, or simply click on **Next** to install into the default directory.

Figure 7-4 TAI Player Setup Wizard – Install Location



In the Choose Start Menu Folder window, click **Install** to begin program installation.

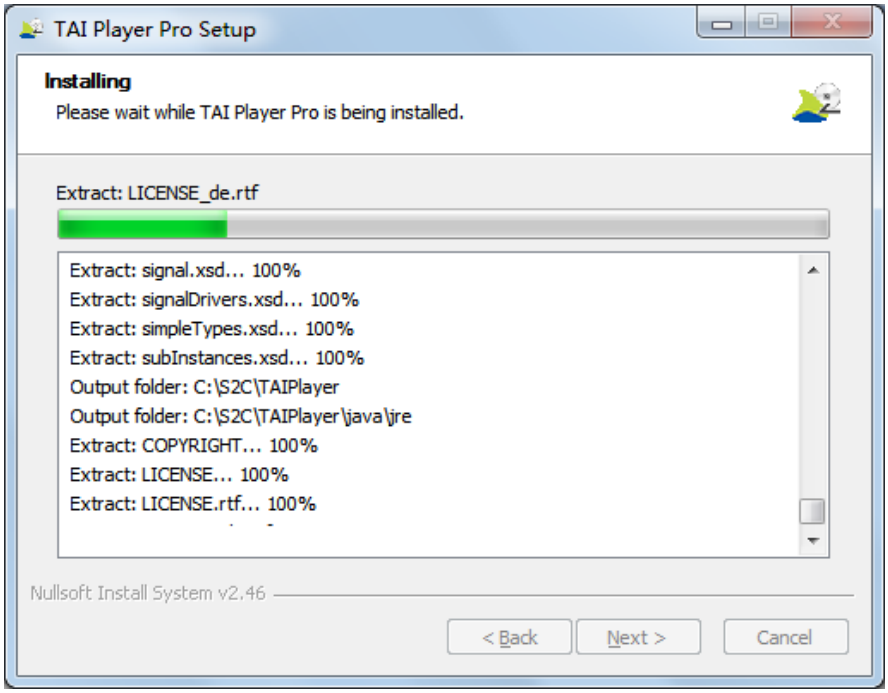
Figure 7-5 TAI Player Setup Wizard – Start Menu Folder



We recommended that you leave the default parameters as is and directly start the file extraction process.

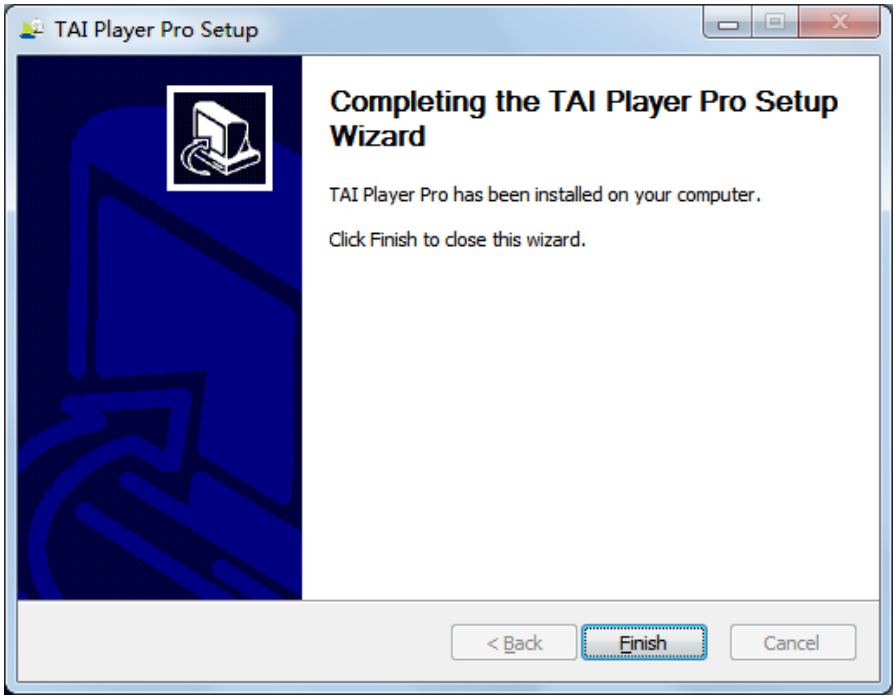
The Install Wizard will extract the program contents into pre-specified directories:

Figure 7-6 TAI Player Setup Wizard – Installing



After the files are extracted, press **Finish** to complete the installation.

Figure 7-7 TAI Player Setup Wizard – Finish



Now you can start TAI Player from the Windows Start menu. If you cannot activate the program, please refer to *Section 7.4: License Management*.

7.4 License Management

TAI Player software is protected by a usage license to ensure that access is provided only to legitimate users. License rights can range from singular use with one specific TAI Logic Module type all the way to a universal use AP-COMPILE license that permits access to all TAI Logic Module types.

7.4.1 Obtaining A License

1. TAI Player's license is bound to the physical address of an Ethernet adapter. So, first ascertain that you have at least one Ethernet card installed on your computer. Then, obtain the card's physical address (please refer to Section 7.4.3: Obtaining the Physical Address of the Ethernet Adapter). If there is more than one Ethernet card on your computer, select the card of your choice and use its physical address.
2. Contact S2C's Technical Support team through the contact information provided in *Section 1.4: Technical Support* and send them the physical address of your computer's Ethernet adapter. The address should be a six-byte (48-bit) hex digit separated by dashes, such as: 00-F6-D4-56-28-9A.
3. Our Technical Support team will then promptly send a license file that will unlock TAI Player's license key.

7.4.2 Registering the License

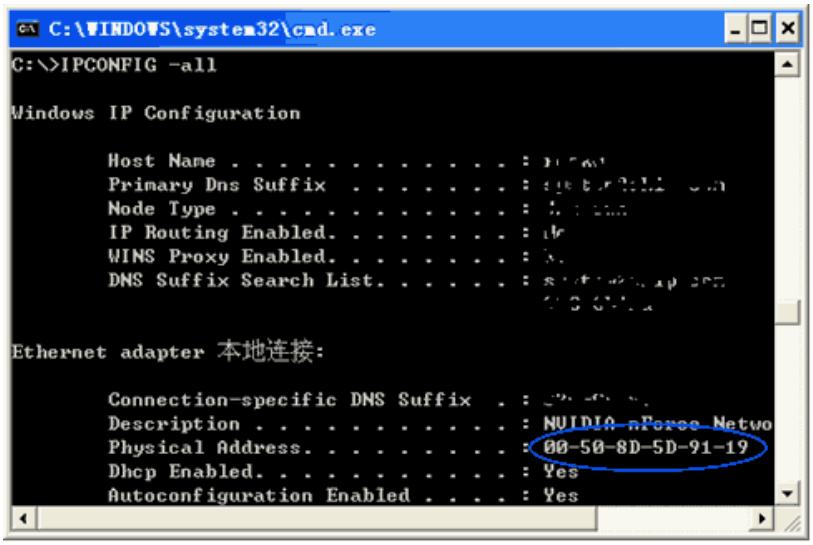
After obtaining the license file, copy it into the installation directory that you selected during the installation process (please refer to Section 7.3: TAI Player Installation).

You can now start TAI Player from the Windows Start menu.

7.4.3 Obtaining the Physical Address of the Ethernet Adapter

There are several ways to obtain the Ethernet adapter's physical address. A relatively simple way is to open a console window, and enter in the command `IPCONFIG –all` to find the address, as shown in the figure below:

Figure 7-8 Obtain the Physical Address



7.5 Running Self-Test

The TAI Logic Module Self-Test program is included in the TAI Logic Module CD. The purpose of the Self-Test program is to identify and isolate any potential connection problems that may exist on the TAI Logic Module board. This serves as a time-saving tool that allows you to work around non-functioning connections and continue working on your design. The Self-Test program contains the following diagnostic tests:

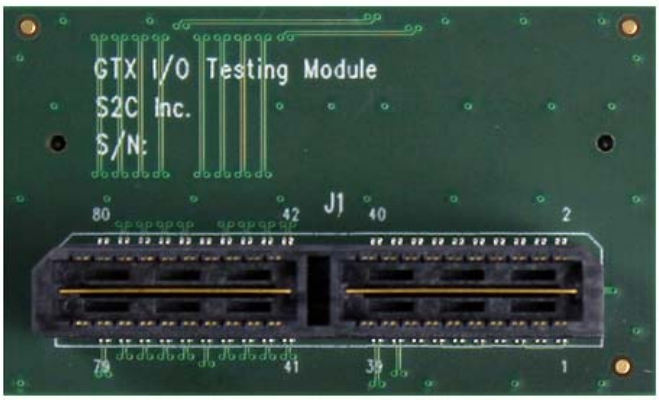
- **TAI BUS Test** – tests the net connections between FPGA F1 and F2
- **Clock Line Test –** tests the two crystal oscillators and six SMB clock inputs, six programmable clock and six feedback clock net that extends from the FPGA feedback line.
- **Connector I/O Test** – tests connectors J1-J12 for any bad connections.
- **SODIMM Test** – tests DDR2 and DDR3 SODIMM sockets for any bad connections.

7.5.4 Hardware Preparation

S2C supplies four type daughter boards to complete Self-Test

- One S2C I/O testing LED board

- One S2C GTX I/O testing LED board



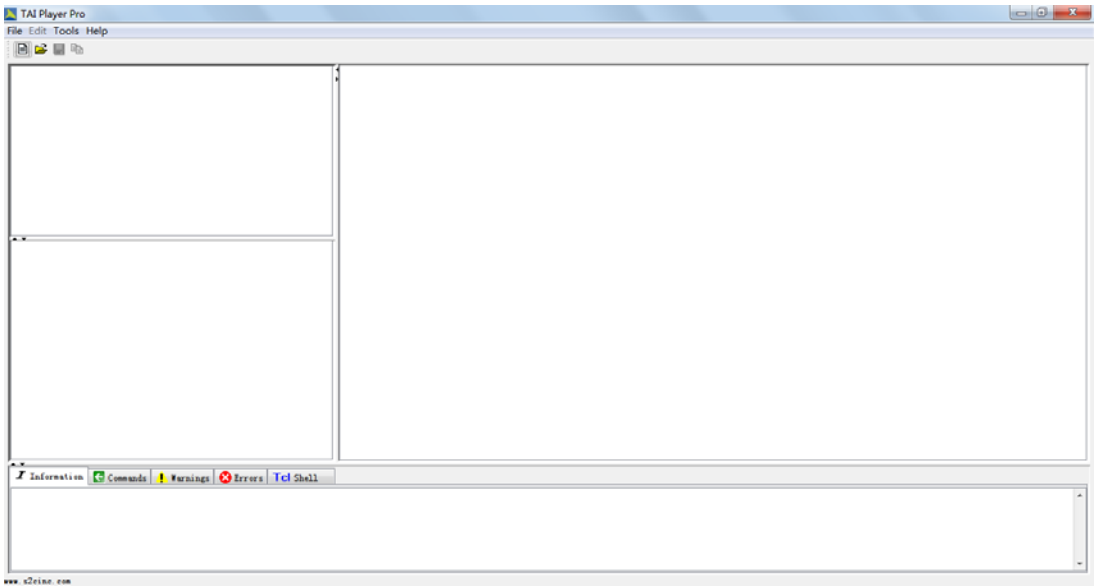
- One SODIMM board for DDR2

- One SODIMM board for DDR3

7.5.5 Software Preparation and Test

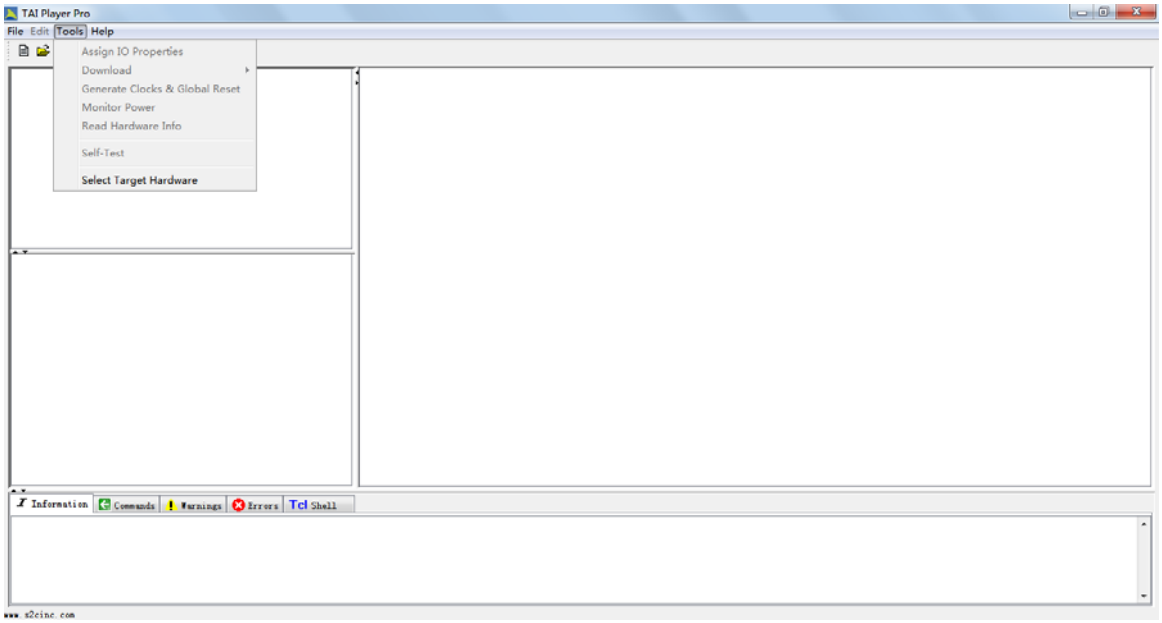
Stack the S2C I/O testing board on any Samtec connector which you want to test. Double click  on desktop to open TAI Player.

Figure 7-9 Open TAI Player



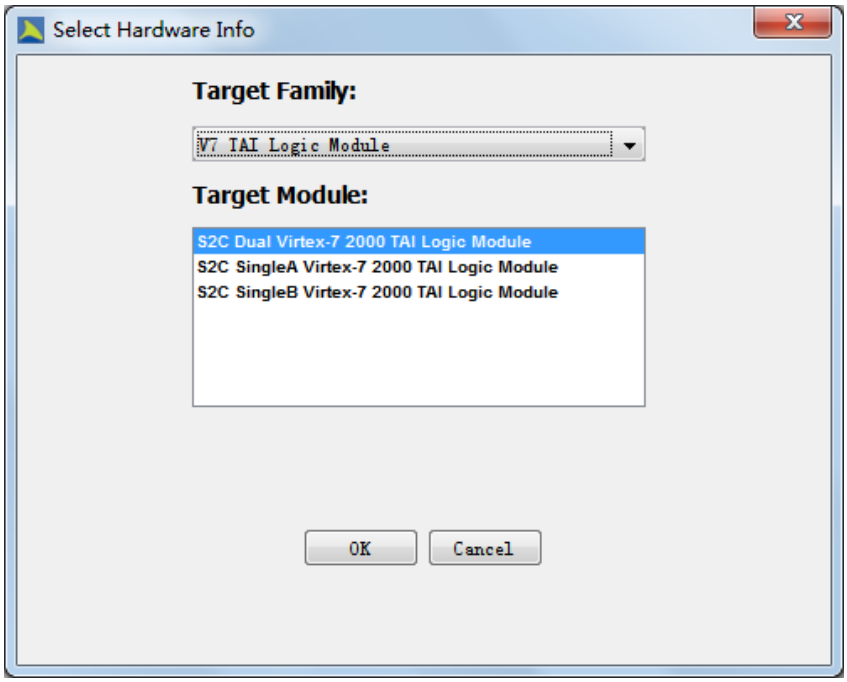
Click “Tool -> Select Target Hardware” then you can select your Target TAI LM to do self-test.

Figure 7-10 Select Target Hardware



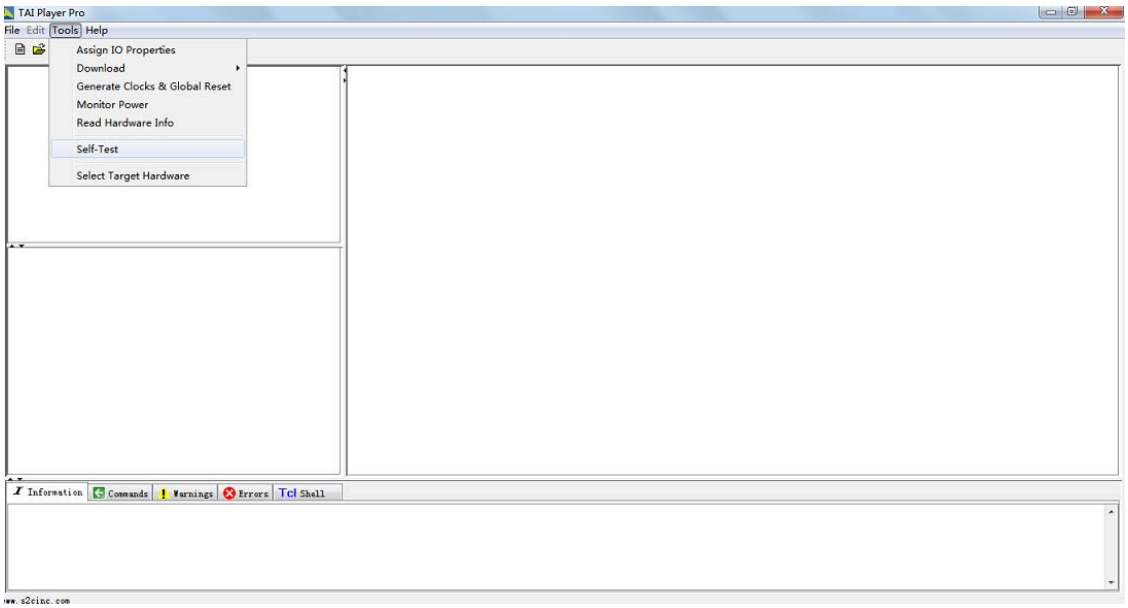
It will pop up a window to let you choose the right target family and target module for your TAI LM.

Figure 7-11 Select Target Family and Target Module



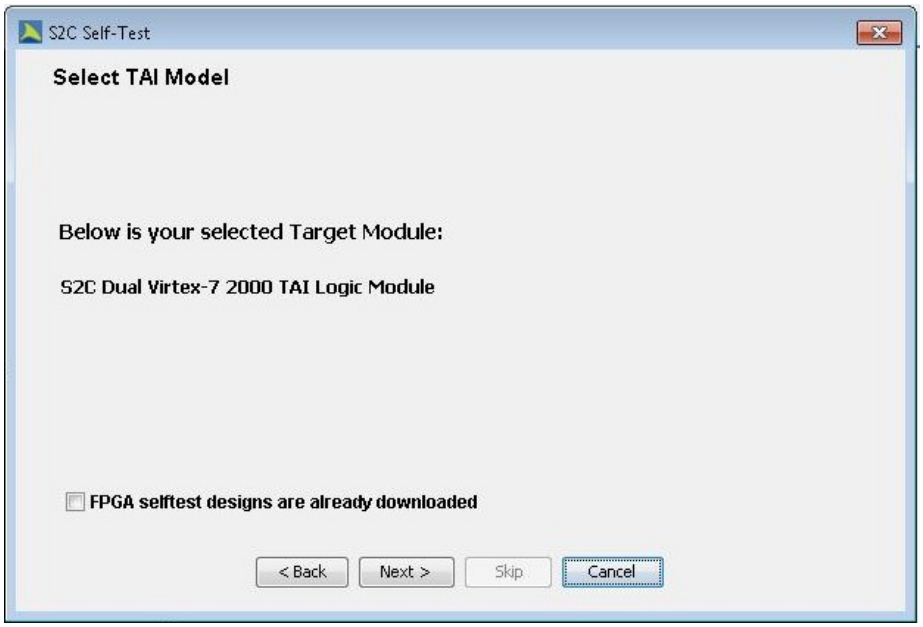
Click “Tool -> Self-Test” then you can begin Self-Test.

Figure 7-12 Begin self-test



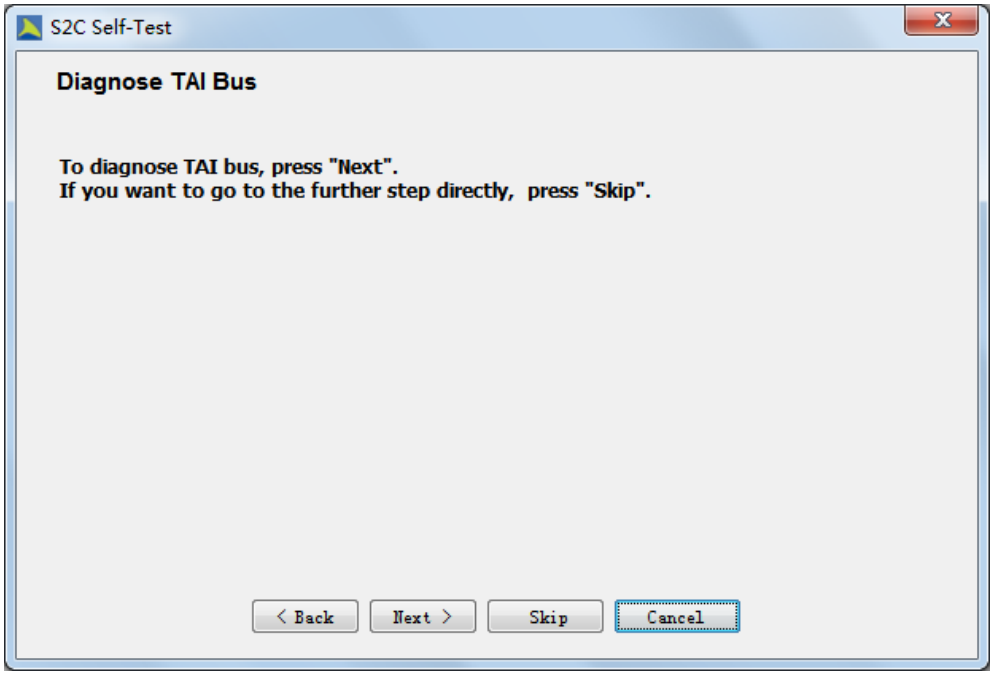
You should choose the Model of the TAI LM which you use now. For example “Dual LM Virtex-7 2000”

Figure 7-13 Select TAI Model



Self- Test contains 3 steps. The first step is TAI Bus test, it can find whether there is any connection problem between two FPGAs.

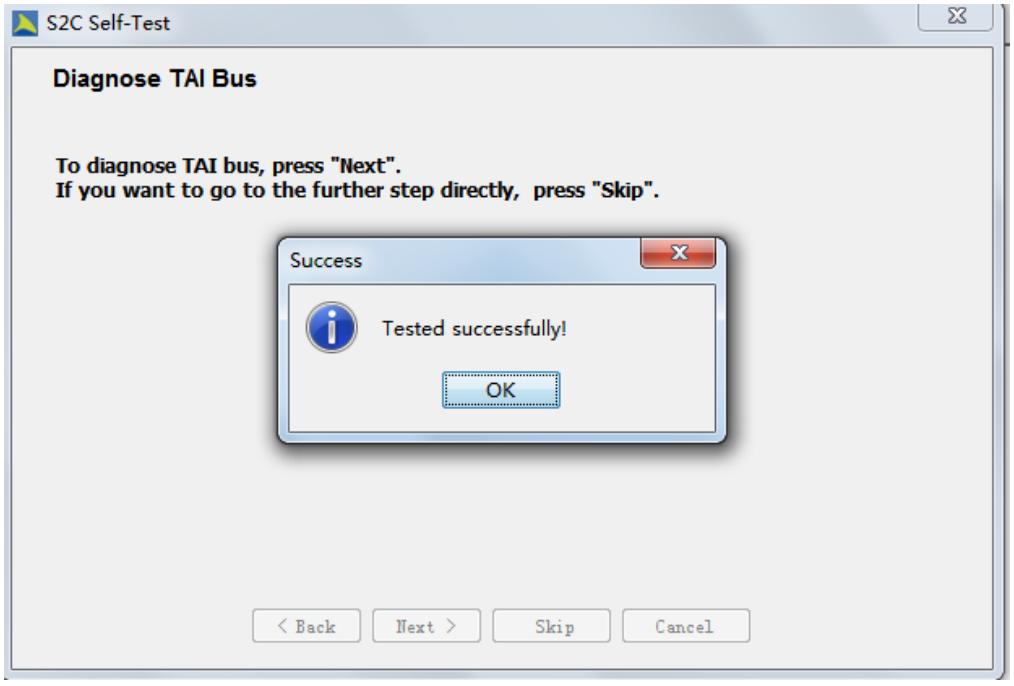
Figure 7-14 Test TAI Bus



First download the Self-Test design into the FPGA on TAI Logic Module using a USB cable that is supply by S2C. LED1 and LED2 will light up.

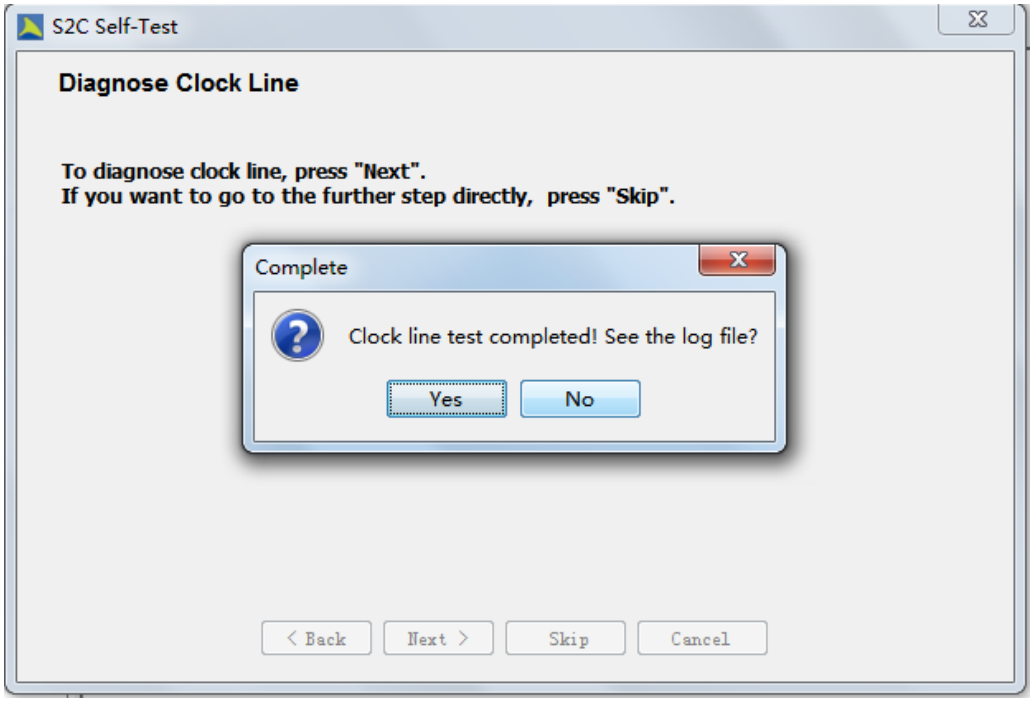
If the connections between F1 and F2 are good, you will see a test success dialogue.

Figure 7-15 TAI BUS test success



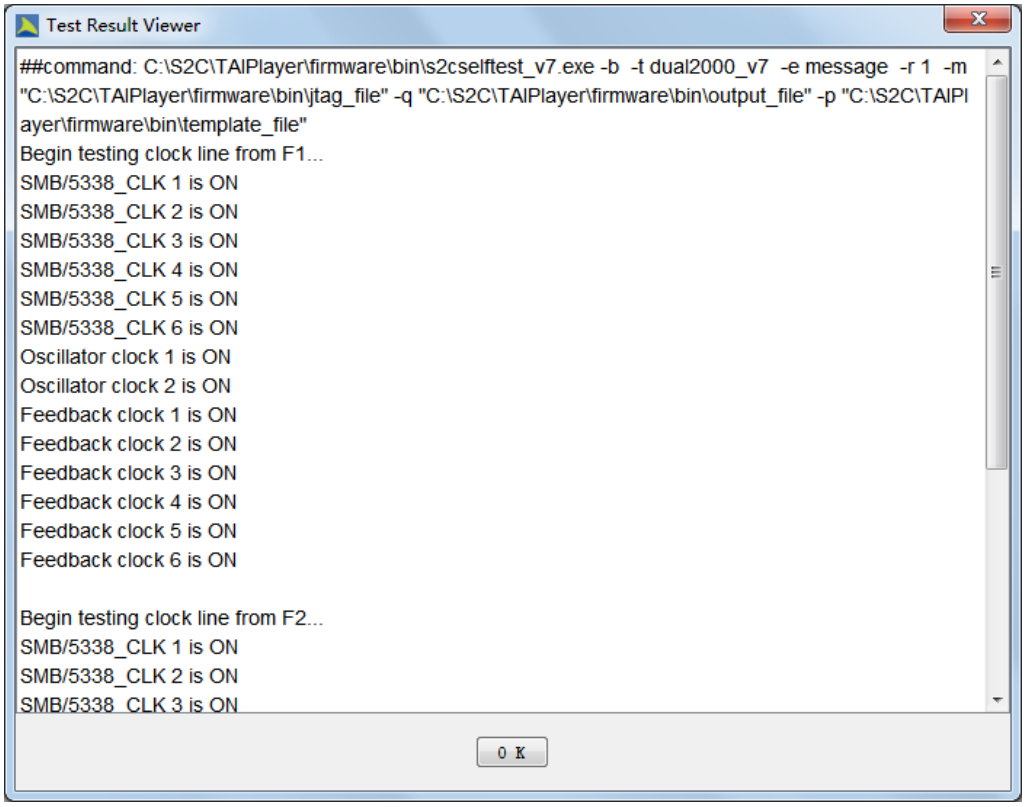
Click “OK” to close the dialogue, then click “next” begin Clock Line test. If successful, the file shows the status of all of the clocks of two FPGAs.

Figure 7-16 Clock Line test success



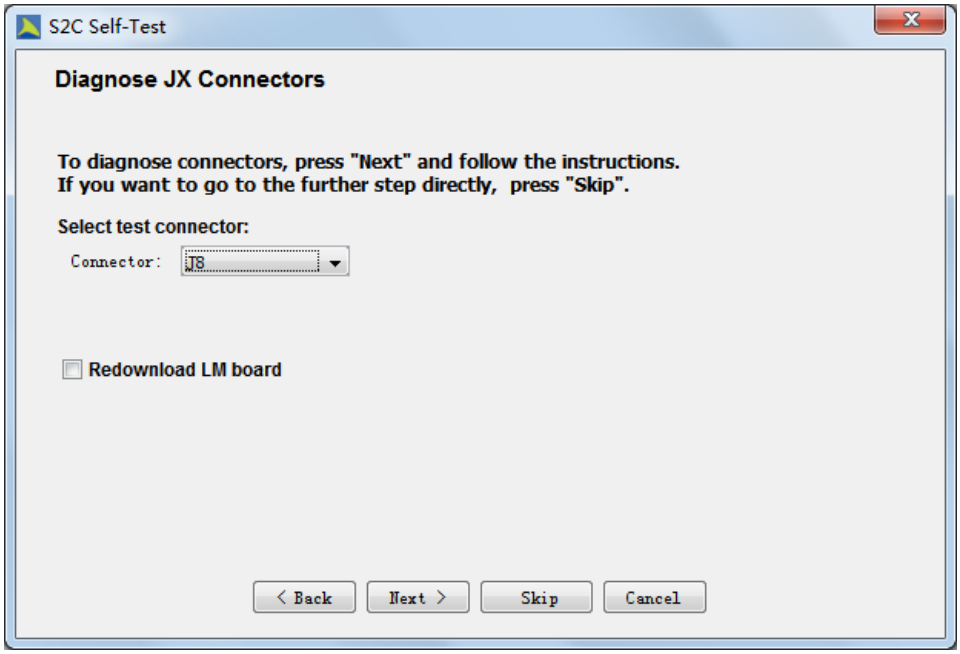
Click “Yes” to see the status of all of the clocks of two FPGAs.

Figure 7-17 Clock Line detail information



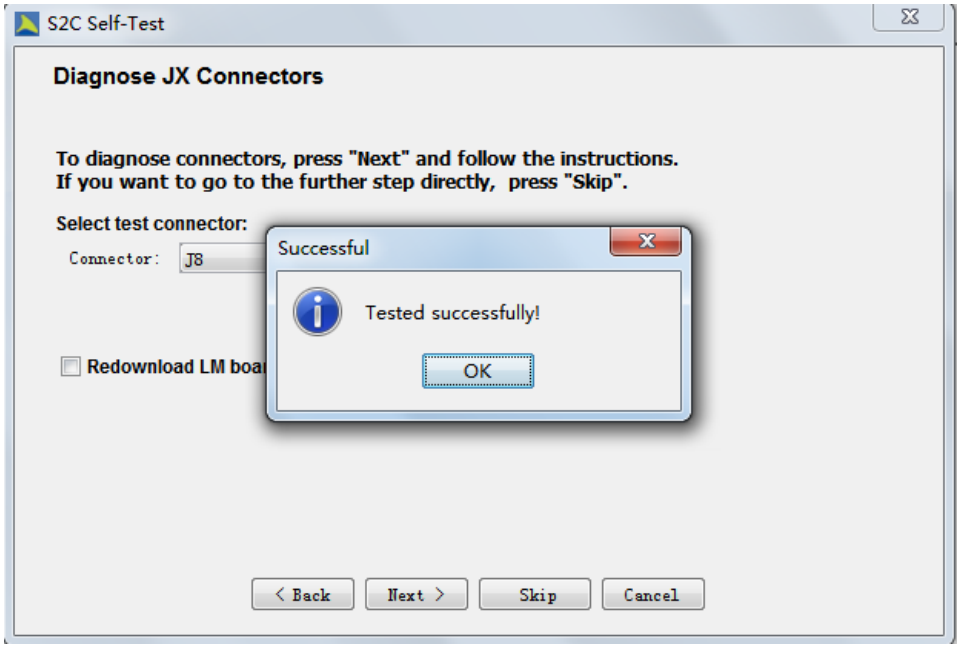
The third step is the connectors test. You can test any of the connectors. Any Error will show in the error Diagnose dialogue.

Figure 7-18 Choose connectors to diagnose



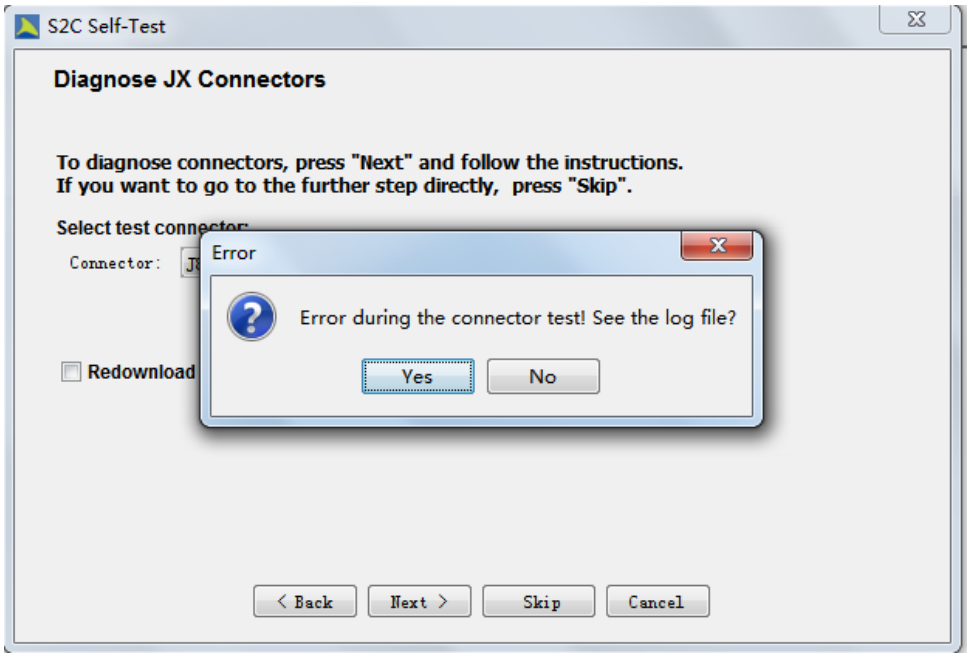
Click next to test the connector you choose. If the connector tests success, it will pop up a test success window below.

Figure 7-19 Connector test success



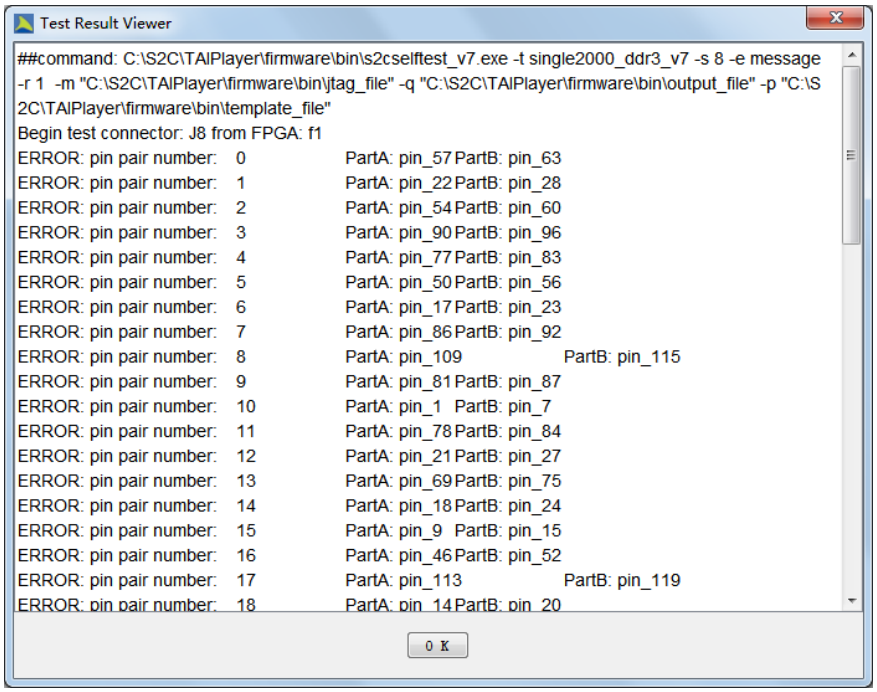
If there's any error is detected during the connector test, if will pop up an error message dialogue below.

Figure 7-20 Connector test error



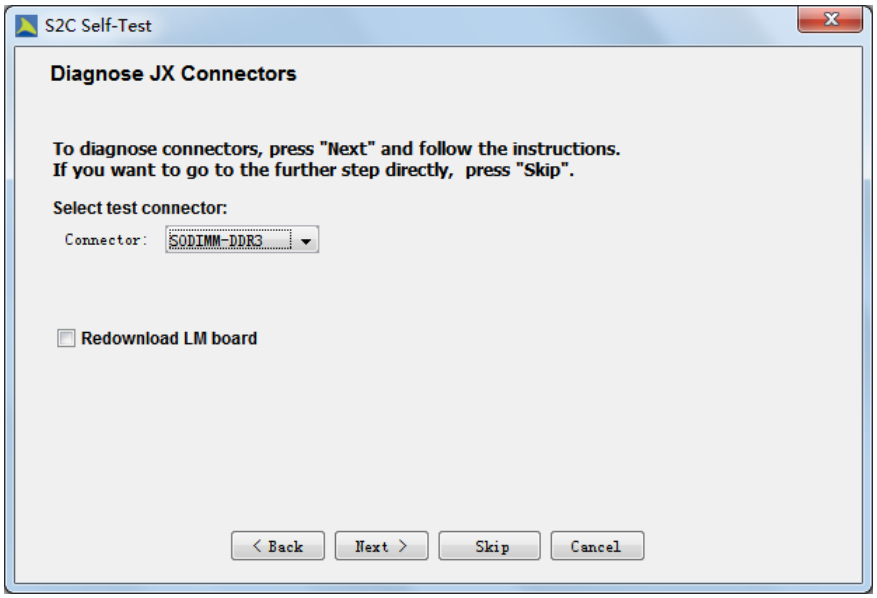
Click “yes” to see the detail error message below.

Figure 7-21 Connector Test Error Detail



In a similar way, you can also test SODIMM. Stack S2C I/O Testing LED board on SODIMM board and insert the group boards into SODIMM sockets. Choose the connector as “SODIMM1” or “SODIMM2”.

Figure 7-22 Choose “SODIMM1”



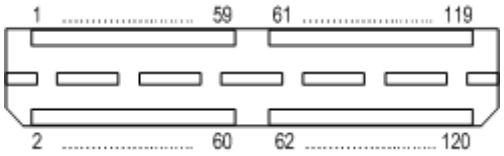
If an error occurs during the self-test process, please contact S2C for help.

8. External Connector Table

Virtex-7 TAI Logic Module has 6 IO types: Global clock I/O, Gigabit transceivers I/O, Dedicated I/O, Shared I/O, Inter-FPGA connection and DDR2/DDR3 SO-DIMM I/O. This section provides the relationship between the various IOs and their corresponding FPGA pinouts.

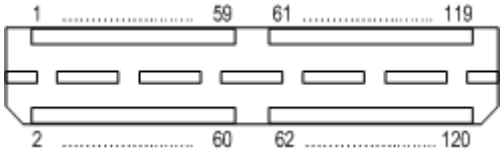
The J2, J3, J4, J5, J6, J7, J8, J9, J10 and J12 use Samtec 120-pin QTH connectors. They are on top side of V7 TAI Logic Module. They have pin orientations corresponding to the layout indicated in the figure below.

Figure 8-1 V7 TAI Logic Module Samtec 120-pin QTH Connector Locations



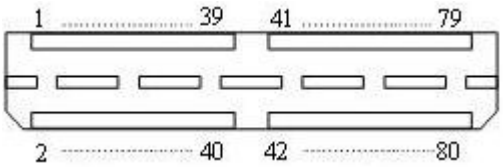
The JB2, JB3, JB4, JB5, JB6, JB7, JB8, JB9, JB10 and JB12 use Samtec 120-pin QSH connectors. They are on bottom side of V7 TAI Logic Module. They have pin orientations corresponding to the layout indicated in the figure below.

Figure 8-2 V7 TAI Logic Module Samtec 120-pin QSH Connector Locations



The J1 and J11 Samtec 80-pin differential connectors on V7 TAI Logic Module have pin orientations corresponding to the layout indicated in the figure below.

Figure 8-3 V7 TAI Logic Module Samtec 80-pin Connector Locations



8.1 Global Clock

A total of 14 global clocks can be input from 2 single ended oscillator sockets, 6 pairs of programmable differential clocks or 6 pairs of SMB differential clocks, and 6 pairs of feedback differential clocks from any of the two user's FPGAs.

6 pairs of programmable differential clocks and 6 pairs of SMB differential clocks are respectively selected through runtime software in GUI.

6 pairs of feedback differential clocks from any of the two user’s FPGA are respectively selected through runtime software in GUI. 6 pairs of feedback differential clocks are FPGA internally generated signals, such as clocks and synchronous resets, which require routing back to the FPGA global clock nets. Using the feedback clock lines will minimize the skew between the two FPGAs.

These 14 global clocks are routed to the 14 MRCC pins of both FPGA. The following table provides the detailed information of the 14 global clocks.

Table 8-1 **Global Clock Properties**

Global Clock	Clock source	F1 Pin No.	F2 Pin No.	Default I/O standard
Programmable clock pair1 or SMB clock pair1	U4.22(P)/U4.21(N) JG1(P)/JG2(N)	F1.L4(P) F1.L3(N)	F2.N4(P) F2.N3(N)	LVDS
Programmable clock pair2 or SMB clock pair2	U4.18(P)/U4.17(N) JG3(P)/JG4(N)	F1.D9(P) F1.C9(N)	F2.AU12(P) F2.AU11(N)	LVDS
Programmable clock pair3 or SMB clock pair3	U4.14(P)/U4.13(N) JG5(P)/JG6(N)	F1.D15(P) F1.D14(N)	F2.AW16(P) F2.AY16(N)	LVDS
Programmable clock pair4 or SMB clock pair4	U5.22(P)/U5.21(N) JG7(P)/JG8(N)	F1.AA38(P) F1.AA39(N)	F2.AA38(P) F2.AA39(N)	LVDS
Programmable clock pair5 or SMB clock pair5	U5.18(P)/U5.17(N) JG9(P)/JG10(N)	F1.K40(P) F1.J40(N)	F2.AU39(P) F2.AU40(N)	LVDS
Programmable clock pair6 or SMB clock pair6	U5.14(P)/U5.13(N) JG11(P)/JG12(N)	F1.D28(P) F1.D29(N)	F2.AR26(P) F2.AR27(N)	LVDS
OSC1	OSC1.3	F1.W4(P) F1.W3(N)	F2.D3(P) F2.C3(N)	LVDS
OSC2	OSC2.3	F1.D20(P) F1.D19(N)	F2.AV19(P) F2.AV18(N)	LVDS
FB Clock pair1	F1.P19(P)/F1.N19(N) F2.AK18(P)/F2.AL18(N)	F1.E6(P) F1.D6(N)	F2.W4(P) F2.W3(N)	LVDS
FB Clock pair2	F1.R20(P)/F1.P20(N) F2.AM20(P)/F2.AN19(N)	F1.G19(P) F1.F19(N)	F2.AR20(P) F2.AT20(N)	LVDS
FB Clock pair3	F1.T20(P)/F1.T19(N) F2.AK17(P)/F2.AL17(N)	F1.AE40(P) F1.AF40(N)	F2.W38(P) F2.W39(N)	LVDS
FB Clock pair4	F1.T18(P)/F1.R18(N) F2.AK20(P)/F2.AL20(N)	F1.AD41(P) F1.AE41(N)	F2.AE40(P) F2.AF40(N)	LVDS
FB Clock pair5	F1.T17(P)/F1.R17(N) F2.AJ20(P)/F2.AJ19(N)	F1.W38(P) F1.W39(N)	F2.AD41(P) F2.AE41(N)	LVDS
FB Clock pair6	F1.P18(P)/F1.N18(N) F2.AL19(P)/F2.AM19(N)	F1.R38(P) F1.P38(N)	F2.AK36(P) F2.AK37(N)	LVDS

▲ NOTES:

User must set the properties of **DIFF_TERM** to "**TRUE**" when they instantiate IBUFDS in FPGA design so that to make the external differential global clocks above work stable in V7 TAI LM.

8.2 Gigabit transceiver I/O

Each FPGA (F1 and F2) has 16 Gigabit transceivers with total of 32 Gigabit Transceivers, which are connected to 4 high speed differential connectors J1, JB1, J11 and JB11. The functions of total 32 GTX transceivers are defined by user. The following tables show the connections for all gigabit transceiver I/O connector pins and their corresponding FPGA pins.

Table 8-2 **GTX I/O Connector Properties**

J1 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
J1.001	F2.AD5	MGTXRXN3_115	Bank115
J1.003	F2.AD6	MGTXRXP3_115	Bank115
J1.005	F2.AE7	MGTXRXN2_115	Bank115
J1.007	F2.AE8	MGTXRXP2_115	Bank115
J1.009	F2.AF5	MGTXRXN1_115	Bank115
J1.011	F2.AF6	MGTXRXP1_115	Bank115
J1.013	F2.AH5	MGTXRXN0_115	Bank115
J1.015	F2.AH6	MGTXRXP0_115	Bank115
J1.017	F2.AG7	MGTREFCLK0N_115	Bank115
J1.019	F2.AG8	MGTREFCLK0P_115	Bank115
J1.021	F2.AJ3	MGTXRXN3_114	Bank114
J1.023	F2.AJ4	MGTXRXP3_114	Bank114
J1.025	F2.AK5	MGTXRXN2_114	Bank114
J1.027	F2.AK6	MGTXRXP2_114	Bank114
J1.029	F2.AM5	MGTXRXN1_114	Bank114
J1.031	F2.AM6	MGTXRXP1_114	Bank114
J1.033	F2.AN3	MGTXRXN0_114	Bank114
J1.035	F2.AN4	MGTXRXP0_114	Bank114
J1.037	F2.AL7	MGTREFCLK0N_114	Bank114
J1.039	F2.AL8	MGTREFCLK0P_114	Bank114
J1.041	F2.M35	IO_L24N_T3_21	Bank21
J1.043	F2.M34	IO_L24P_T3_21	Bank21
J1.045	N.C.		
J1.047	N.C.		
J1.049	F2.P31	IO_L24N_T3_20	Bank20
J1.051	F2.P30	IO_L24P_T3_20	Bank20
J1.053	N.C.		
J1.055	N.C.		
J1.057	F2.P34	IO_L20N_T3_20	Bank20
J1.059	F2.P33	IO_L20P_T3_20	Bank20
J1.061	N.C.		
J1.063	N.C.		
J1.065	F2.R31	IO_L21N_T3_DQS_20	Bank20
J1.067	F2.R30	IO_L21P_T3_DQS_20	Bank20
J1.069	N.C.		
J1.071	N.C.		
J1.073	F2.R33	IO_L22N_T3_20	Bank20
J1.075	F2.R32	IO_L22P_T3_20	Bank20

J1 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
J1.077	F2.T30	IO_L23N_T3_20	Bank20
J1.079	F2.T29	IO_L23P_T3_20	Bank20
J1.002	F2.AD1	MGTXTXN3_115	Bank115
J1.004	F2.AD2	MGTXTXP3_115	Bank115
J1.006	F2.AE3	MGTXTXN2_115	Bank115
J1.008	F2.AE4	MGTXTXP2_115	Bank115
J1.010	F2.AF1	MGTXTXN1_115	Bank115
J1.012	F2.AF2	MGTXTXP1_115	Bank115
J1.014	F2.AG3	MGTXTXN0_115	Bank115
J1.016	F2.AG4	MGTXTXP0_115	Bank115
J1.018	F2.AJ7	MGTREFCLK1N_115	Bank115
J1.020	F2.AJ8	MGTREFCLK1P_115	Bank115
J1.022	F2.AH1	MGTXTXN3_114	Bank114
J1.024	F2.AH2	MGTXTXP3_114	Bank114
J1.026	F2.AK1	MGTXTXN2_114	Bank114
J1.028	F2.AK2	MGTXTXP2_114	Bank114
J1.030	F2.AL3	MGTXTXN1_114	Bank114
J1.032	F2.AL4	MGTXTXP1_114	Bank114
J1.034	F2.AM1	MGTXTXN0_114	Bank114
J1.036	F2.AM2	MGTXTXP0_114	Bank114
J1.038	F2.AN7	MGTREFCLK1N_114	Bank114
J1.040	F2.AN8	MGTREFCLK1P_114	Bank114
J1.042	N.C.		
J1.044	N.C.		
J1.046	N.C.		
J1.048	N.C.		
J1.050	N.C.		
J1.052	N.C.		
J1.054	N.C.		
J1.056	N.C.		
J1.058	N.C.		
J1.060	N.C.		
J1.062	N.C.		
J1.064	N.C.		
J1.066	N.C.		
J1.068	N.C.		
J1.070	N.C.		
J1.072	N.C.		
J1.074	N.C.		
J1.076	N.C.		
J1.078	N.C.		
J1.080	N.C.		

JB1 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**

JB1 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
JB1.001	F2.A35	IO_L1N_T0_22	Bank22
JB1.003	F2.B35	IO_L1P_T0_22	Bank22
JB1.005	N.C.		
JB1.007	N.C.		
JB1.009	F2.A34	IO_L4N_T0_22	Bank22
JB1.011	F2.B34	IO_L4P_T0_22	Bank22
JB1.013	N.C.		
JB1.015	N.C.		
JB1.017	F2.C34	IO_L2N_T0_22	Bank22
JB1.019	F2.D34	IO_L2P_T0_22	Bank22
JB1.021	N.C.		
JB1.023	N.C.		
JB1.025	F2.G35	IO_L2N_T0_21	Bank21
JB1.027	F2.G34	IO_L2P_T0_21	Bank21
JB1.029	N.C.		
JB1.031	N.C.		
JB1.033	F2.J35	IO_L22N_T3_21	Bank21
JB1.035	F2.J34	IO_L22P_T3_21	Bank21
JB1.037	F2.L35	IO_L23N_T3_21	Bank21
JB1.039	F2.L34	IO_L23P_T3_21	Bank21
JB1.041	F2.AP5	MGTXRXN3_113	Bank113
JB1.043	F2.AP6	MGTXRXP3_113	Bank113
JB1.045	F2.AR3	MGTXRXN2_113	Bank113
JB1.047	F2.AR4	MGTXRXP2_113	Bank113
JB1.049	F2.AT5	MGTXRXN1_113	Bank113
JB1.051	F2.AT6	MGTXRXP1_113	Bank113
JB1.053	F2.AV5	MGTXRXN0_113	Bank113
JB1.055	F2.AV6	MGTXRXP0_113	Bank113
JB1.057	F2.AR7	MGTREFCLK0N_113	Bank113
JB1.059	F2.AR8	MGTREFCLK0P_113	Bank113
JB1.061	F2.AW3	MGTXRXN3_112	Bank112
JB1.063	F2.AW4	MGTXRXP3_112	Bank112
JB1.065	F2.AY5	MGTXRXN2_112	Bank112
JB1.067	F2.AY6	MGTXRXP2_112	Bank112
JB1.069	F2.BB5	MGTXRXN1_112	Bank112
JB1.071	F2.BB6	MGTXRXP1_112	Bank112
JB1.073	F2.BD5	MGTXRXN0_112	Bank112
JB1.075	F2.BD6	MGTXRXP0_112	Bank112
JB1.077	F2.AW7	MGTREFCLK0N_112	Bank112
JB1.079	F2.AW8	MGTREFCLK0P_112	Bank112
JB1.002	N.C.		
JB1.004	N.C.		
JB1.006	N.C.		
JB1.008	N.C.		
JB1.010	N.C.		
JB1.012	N.C.		
JB1.014	N.C.		
JB1.016	N.C.		
JB1.018	N.C.		

JB1 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
JB1.020	N.C.		
JB1.022	N.C.		
JB1.024	N.C.		
JB1.026	N.C.		
JB1.028	N.C.		
JB1.030	N.C.		
JB1.032	N.C.		
JB1.034	N.C.		
JB1.036	N.C.		
JB1.038	N.C.		
JB1.040	N.C.		
JB1.042	F2.AP1	MGTXTXN3_113	Bank113
JB1.044	F2.AP2	MGTXTXP3_113	Bank113
JB1.046	F2.AT1	MGTXTXN2_113	Bank113
JB1.048	F2.AT2	MGTXTXP2_113	Bank113
JB1.050	F2.AU3	MGTXTXN1_113	Bank113
JB1.052	F2.AU4	MGTXTXP1_113	Bank113
JB1.054	F2.AV1	MGTXTXN0_113	Bank113
JB1.056	F2.AV2	MGTXTXP0_113	Bank113
JB1.058	F2.AU7	MGTREFCLK1N_113	Bank113
JB1.060	F2.AU8	MGTREFCLK1P_113	Bank113
JB1.062	F2.AY1	MGTXTXN3_112	Bank112
JB1.064	F2.AY2	MGTXTXP3_112	Bank112
JB1.066	F2.BA3	MGTXTXN2_112	Bank112
JB1.068	F2.BA4	MGTXTXP2_112	Bank112
JB1.070	F2.BB1	MGTXTXN1_112	Bank112
JB1.072	F2.BB2	MGTXTXP1_112	Bank112
JB1.074	F2.BC3	MGTXTXN0_112	Bank112
JB1.076	F2.BC4	MGTXTXP0_112	Bank112
JB1.078	F2.BA7	MGTREFCLK1N_112	Bank112
JB1.080	F2.BA8	MGTREFCLK1P_112	Bank112

J11 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
J11.001	F1.AD5	MGTXRXN3_115	Bank115
J11.003	F1.AD6	MGTXRXP3_115	Bank115
J11.005	F1.AE7	MGTXRXN2_115	Bank115
J11.007	F1.AE8	MGTXRXP2_115	Bank115
J11.009	F1.AF5	MGTXRXN1_115	Bank115
J11.011	F1.AF6	MGTXRXP1_115	Bank115
J11.013	F1.AH5	MGTXRXN0_115	Bank115
J11.015	F1.AH6	MGTXRXP0_115	Bank115
J11.017	F1.AG7	MGTREFCLK0N_115	Bank115
J11.019	F1.AG8	MGTREFCLK0P_115	Bank115
J11.021	F1.AJ3	MGTXRXN3_114	Bank114

J11 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
J11.023	F1.AJ4	MGTXRXP3_114	Bank114
J11.025	F1.AK5	MGTXRXN2_114	Bank114
J11.027	F1.AK6	MGTXRXP2_114	Bank114
J11.029	F1.AM5	MGTXRXN1_114	Bank114
J11.031	F1.AM6	MGTXRXP1_114	Bank114
J11.033	F1.AN3	MGTXRXN0_114	Bank114
J11.035	F1.AN4	MGTXRXP0_114	Bank114
J11.037	F1.AL7	MGTREFCLK0N_114	Bank114
J11.039	F1.AL8	MGTREFCLK0P_114	Bank114
J11.041	F1.BC36	IO_L24N_T3_11	Bank11
J11.043	F1.BB36	IO_L24P_T3_11	Bank11
J11.045	N.C.		
J11.047	N.C.		
J11.049	F1.BD34	IO_L23N_T3_11	Bank11
J11.051	F1.BC34	IO_L23P_T3_11	Bank11
J11.053	N.C.		
J11.055	N.C.		
J11.057	F1.BB35	IO_L22N_T3_11	Bank11
J11.059	F1.BA35	IO_L22P_T3_11	Bank11
J11.061	N.C.		
J11.063	N.C.		
J11.065	F1.BD36	IO_L21N_T3_DQS_11	Bank11
J11.067	F1.BD35	IO_L21P_T3_DQS_11	Bank11
J11.069	N.C.		
J11.071	N.C.		
J11.073	F1.AY35	IO_L20N_T3_11	Bank11
J11.075	F1.AW35	IO_L20P_T3_11	Bank11
J11.077	F1.BC37	IO_L16N_T2_11	Bank11
J11.079	F1.BB37	IO_L16P_T2_11	Bank11
J11.002	F1.AD1	MGTXTXN3_115	Bank115
J11.004	F1.AD2	MGTXTXP3_115	Bank115
J11.006	F1.AE3	MGTXTXN2_115	Bank115
J11.008	F1.AE4	MGTXTXP2_115	Bank115
J11.010	F1.AF1	MGTXTXN1_115	Bank115
J11.012	F1.AF2	MGTXTXP1_115	Bank115
J11.014	F1.AG3	MGTXTXN0_115	Bank115
J11.016	F1.AG4	MGTXTXP0_115	Bank115
J11.018	F1.AJ7	MGTREFCLK1N_115	Bank115
J11.020	F1.AJ8	MGTREFCLK1P_115	Bank115
J11.022	F1.AH1	MGTXTXN3_114	Bank114
J11.024	F1.AH2	MGTXTXP3_114	Bank114
J11.026	F1.AK1	MGTXTXN2_114	Bank114
J11.028	F1.AK2	MGTXTXP2_114	Bank114
J11.030	F1.AL3	MGTXTXN1_114	Bank114
J11.032	F1.AL4	MGTXTXP1_114	Bank114
J11.034	F1.AM1	MGTXTXN0_114	Bank114
J11.036	F1.AM2	MGTXTXP0_114	Bank114
J11.038	F1.AN7	MGTREFCLK1N_114	Bank114
J11.040	F1.AN8	MGTREFCLK1P_114	Bank114

J11 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
J11.042	N.C.		
J11.044	N.C.		
J11.046	N.C.		
J11.048	N.C.		
J11.050	N.C.		
J11.052	N.C.		
J11.054	N.C.		
J11.056	N.C.		
J11.058	N.C.		
J11.060	N.C.		
J11.062	N.C.		
J11.064	N.C.		
J11.066	N.C.		
J11.068	N.C.		
J11.070	N.C.		
J11.072	N.C.		
J11.074	N.C.		
J11.076	N.C.		
J11.078	N.C.		
J11.080	N.C.		

JB11 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
JB11.001	F1.AH33	IO_L23N_T3_13	Bank13
JB11.003	F1.AH32	IO_L23P_T3_13	Bank13
JB11.005	N.C.		
JB11.007	N.C.		
JB11.009	F1.AM34	IO_L22N_T3_13	Bank13
JB11.011	F1.AL34	IO_L22P_T3_13	Bank13
JB11.013	N.C.		
JB11.015	N.C.		
JB11.017	F1.AL33	IO_L21N_T3_DQS_13	Bank13
JB11.019	F1.AK33	IO_L21P_T3_DQS_13	Bank13
JB11.021	N.C.		
JB11.023	N.C.		
JB11.025	F1.AV34	IO_L22N_T3_12	Bank12
JB11.027	F1.AU34	IO_L22P_T3_12	Bank12
JB11.029	N.C.		
JB11.031	N.C.		
JB11.033	F1.AU35	IO_L20N_T3_12	Bank12
JB11.035	F1.AT35	IO_L20P_T3_12	Bank12
JB11.037	F1.AP35	IO_L3N_T0_DQS_12	Bank12
JB11.039	F1.AP34	IO_L3P_T0_DQS_12	Bank12
JB11.041	F1.AP5	MGTXRXN3_113	Bank113
JB11.043	F1.AP6	MGTXRXP3_113	Bank113

JB11 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
JB11.045	F1.AR3	MGTXRXN2_113	Bank113
JB11.047	F1.AR4	MGTXRXP2_113	Bank113
JB11.049	F1.AT5	MGTXRXN1_113	Bank113
JB11.051	F1.AT6	MGTXRXP1_113	Bank113
JB11.053	F1.AV5	MGTXRXN0_113	Bank113
JB11.055	F1.AV6	MGTXRXP0_113	Bank113
JB11.057	F1.AR7	MGTREFCLK0N_113	Bank113
JB11.059	F1.AR8	MGTREFCLK0P_113	Bank113
JB11.061	F1.AW3	MGTXRXN3_112	Bank112
JB11.063	F1.AW4	MGTXRXP3_112	Bank112
JB11.065	F1.AY5	MGTXRXN2_112	Bank112
JB11.067	F1.AY6	MGTXRXP2_112	Bank112
JB11.069	F1.BB5	MGTXRXN1_112	Bank112
JB11.071	F1.BB6	MGTXRXP1_112	Bank112
JB11.073	F1.BD5	MGTXRXN0_112	Bank112
JB11.075	F1.BD6	MGTXRXP0_112	Bank112
JB11.077	F1.AW7	MGTREFCLK0N_112	Bank112
JB11.079	F1.AW8	MGTREFCLK0P_112	Bank112
JB11.002	N.C.		
JB11.004	N.C.		
JB11.006	N.C.		
JB11.008	N.C.		
JB11.010	N.C.		
JB11.012	N.C.		
JB11.014	N.C.		
JB11.016	N.C.		
JB11.018	N.C.		
JB11.020	N.C.		
JB11.022	N.C.		
JB11.024	N.C.		
JB11.026	N.C.		
JB11.028	N.C.		
JB11.030	N.C.		
JB11.032	N.C.		
JB11.034	N.C.		
JB11.036	N.C.		
JB11.038	N.C.		
JB11.040	N.C.		
JB11.042	F1.AP1	MGTXTXN3_113	Bank113
JB11.044	F1.AP2	MGTXTXP3_113	Bank113
JB11.046	F1.AT1	MGTXTXN2_113	Bank113
JB11.048	F1.AT2	MGTXTXP2_113	Bank113
JB11.050	F1.AU3	MGTXTXN1_113	Bank113
JB11.052	F1.AU4	MGTXTXP1_113	Bank113
JB11.054	F1.AV1	MGTXTXN0_113	Bank113
JB11.056	F1.AV2	MGTXTXP0_113	Bank113
JB11.058	F1.AU7	MGTREFCLK1N_113	Bank113
JB11.060	F1.AU8	MGTREFCLK1P_113	Bank113
JB11.062	F1.AY1	MGTXTXN3_112	Bank112

JB11 GTX Connector			
Top Con	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
JB11.064	F1.AY2	MGTXTXP3_112	Bank112
JB11.066	F1.BA3	MGTXTXN2_112	Bank112
JB11.068	F1.BA4	MGTXTXP2_112	Bank112
JB11.070	F1.BB1	MGTXTXN1_112	Bank112
JB11.072	F1.BB2	MGTXTXP1_112	Bank112
JB11.074	F1.BC3	MGTXTXN0_112	Bank112
JB11.076	F1.BC4	MGTXTXP0_112	Bank112
JB11.078	F1.BA7	MGTREFCLK1N_112	Bank112
JB11.080	F1.BA8	MGTREFCLK1P_112	Bank112

8.3 Dedicated I/O

Dedicated I/O connectors are those labeled J3, J4, J5, J8, J9, and J10. They are used to connect TAI Logic Module to target board and peripheral extensions. Every I/O is directly wire-linked to one FPGA I/O pin. The following table shows the connections of all dedicated I/O connector pins and their corresponding FPGA pins.

Table 8-3 **Dedicated I/O Connector Properties**

J3 (Odd Pins)					J3 (Even Pins)				
Top Con	**Bottom Con**	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**	**Top Con**	**Bottom Con**	**FPGA Pin No.**	**FPGA Pin Description**	**FPGA Bank**
J3.001	JB3.001	F2.G16	IO_L3N_T0_DQS_41	Bank41	J3.002	JB3.002	F2.N18	IO_L24N_T3_40	Bank40
J3.003	JB3.003	F2.H16	IO_L3P_T0_DQS_41	Bank41	J3.004	JB3.004	F2.P18	IO_L24P_T3_40	Bank40
J3.005	JB3.005	F2.J16	IO_L5N_T0_41	Bank41	J3.006	JB3.006	F2.T19	IO_L21N_T3_DQS_40	Bank40
J3.007	JB3.007	F2.K16	IO_L5P_T0_41	Bank41	J3.008	JB3.008	F2.T20	IO_L21P_T3_DQS_40	Bank40
J3.009	JB3.009	F2.R17	IO_L23N_T3_40	Bank40	J3.010	JB3.010	F2.P20	IO_L20N_T3_40	Bank40
J3.011	JB3.011	F2.T17	IO_L23P_T3_40	Bank40	J3.012	JB3.012	F2.R20	IO_L20P_T3_40	Bank40
J3.013	JB3.013	F2.N19	IO_L19N_T3_VREF_40	Bank40	J3.014	JB3.014	F2.J20	IO_L16N_T2_40	Bank40
J3.015	JB3.015	F2.P19	IO_L19P_T3_40	Bank40	J3.016	JB3.016	F2.K20	IO_L16P_T2_40	Bank40
J3.017	JB3.017	F2.R18	IO_L22N_T3_40	Bank40	J3.018	JB3.018	F2.G20	IO_L17N_T2_40	Bank40
J3.019	JB3.019	F2.T18	IO_L22P_T3_40	Bank40	J3.020	JB3.020	F2.G21	IO_L17P_T2_40	Bank40
J3.021	JB3.021	F2.F19	IO_L13N_T2_MRCC_40	Bank40	J3.022	JB3.022	F2.E20	IO_L14N_T2_SRCC_40	Bank40
J3.023	JB3.023	F2.G19	IO_L13P_T2_MRCC_40	Bank40	J3.024	JB3.024	F2.F20	IO_L14P_T2_SRCC_40	Bank40
J3.025	JB3.025	F2.E18	IO_L18N_T2_40	Bank40	J3.026	JB3.026	F2.G17	IO_L6N_T0_VREF_41	Bank41
J3.027	JB3.027	F2.F18	IO_L18P_T2_40	Bank40	J3.028	JB3.028	F2.H17	IO_L6P_T0_41	Bank41
J3.029	JB3.029	F2.E17	IO_L15N_T2_DQS_41	Bank41	J3.030	JB3.030	F2.D21	IO_L15N_T2_DQS_40	Bank40
J3.031	JB3.031	F2.F17	IO_L15P_T2_DQS_41	Bank41	J3.032	JB3.032	F2.E21	IO_L15P_T2_DQS_40	Bank40
J3.033	JB3.033	F2.D16	IO_L14N_T2_SRCC_41	Bank41	J3.034	JB3.034	F2.D14	IO_L12N_T1_MRCC_41	Bank41
J3.035	JB3.035	F2.E16	IO_L14P_T2_SRCC_41	Bank41	J3.036	JB3.036	F2.D15	IO_L12P_T1_MRCC_41	Bank41
J3.037	JB3.037	F2.C16	IO_L18N_T2_41	Bank41	J3.038	JB3.038	F2.M16	IO_L21N_T3_DQS_41	Bank41
J3.039	JB3.039	F2.C17	IO_L18P_T2_41	Bank41	J3.040	JB3.040	F2.N16	IO_L21P_T3_DQS_41	Bank41
J3.041	JB3.041	F2.A17	IO_L17N_T2_41	Bank41	J3.042	JB3.042	F2.L14	IO_L20N_T3_41	Bank41
J3.043	JB3.043	F2.B17	IO_L17P_T2_41	Bank41	J3.044	JB3.044	F2.M15	IO_L20P_T3_41	Bank41
J3.045	JB3.045	F2.B15	IO_L16N_T2_41	Bank41	J3.046	JB3.046	F2.J15	IO_L1N_T0_41	Bank41
J3.047	JB3.047	F2.B16	IO_L16P_T2_41	Bank41	J3.048	JB3.048	F2.K15	IO_L1P_T0_41	Bank41
J3.049	JB3.049	F2.A14	IO_L10N_T1_41	Bank41	J3.050	JB3.050	F2.H14	IO_L2N_T0_41	Bank41
J3.051	JB3.051	F2.A15	IO_L10P_T1_41	Bank41	J3.052	JB3.052	F2.J14	IO_L2P_T0_41	Bank41
J3.053	JB3.053	F2.P16	IO_L19N_T3_VREF_41	Bank41	J3.054	JB3.054	F2.G14	IO_L4N_T0_41	Bank41

J3 (Odd Pins)					J3 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J3.055	JB3.055	F2.R16	IO_L19P_T3_41	Bank41	J3.056	JB3.056	F2.G15	IO_L4P_T0_41	Bank41
J3.057	JB3.057	F2.A13	IO_L8N_T1_41	Bank41	J3.058	JB3.058	F2.D13	IO_L9N_T1_DQS_41	Bank41
J3.059	JB3.059	F2.B14	IO_L8P_T1_41	Bank41	J3.060	JB3.060	F2.E13	IO_L9P_T1_DQS_41	Bank41
J3.061	JB3.061	F2.E15	IO_L13N_T2_MRCC_41	Bank41	J3.062	JB3.062	F2.D11	IO_L13N_T2_MRCC_42	Bank42
J3.063	JB3.063	F2.F15	IO_L13P_T2_MRCC_41	Bank41	J3.064	JB3.064	F2.E11	IO_L13P_T2_MRCC_42	Bank42
J3.065	JB3.065	F2.F13	IO_L7N_T1_41	Bank41	J3.066	JB3.066	F2.H13	IO_L19N_T3_VREF_42	Bank42
J3.067	JB3.067	F2.F14	IO_L7P_T1_41	Bank41	J3.068	JB3.068	F2.J13	IO_L19P_T3_42	Bank42
J3.069	JB3.069	F2.E12	IO_L15N_T2_DQS_42	Bank42	J3.070	JB3.070	F2.C13	IO_L11N_T1_SRCC_41	Bank41
J3.071	JB3.071	F2.F12	IO_L15P_T2_DQS_42	Bank42	J3.072	JB3.072	F2.C14	IO_L11P_T1_SRCC_41	Bank41
J3.073	JB3.073	F2.G11	IO_L18N_T2_42	Bank42	J3.074	JB3.074	F2.A12	IO_L8N_T1_42	Bank42
J3.075	JB3.075	F2.H11	IO_L18P_T2_42	Bank42	J3.076	JB3.076	F2.B12	IO_L8P_T1_42	Bank42
J3.077	JB3.077	F2.G12	IO_L17N_T2_42	Bank42	J3.078	JB3.078	F2.B10	IO_L9N_T1_DQS_42	Bank42
J3.079	JB3.079	F2.H12	IO_L17P_T2_42	Bank42	J3.080	JB3.080	F2.B11	IO_L9P_T1_DQS_42	Bank42
J3.081	JB3.081	F2.M14	IO_L24N_T3_41	Bank41	J3.082	JB3.082	F2.A9	IO_L10N_T1_42	Bank42
J3.083	JB3.083	F2.N14	IO_L24P_T3_41	Bank41	J3.084	JB3.084	F2.A10	IO_L10P_T1_42	Bank42
J3.085	JB3.085	F2.N13	IO_L1N_T0_42	Bank42	J3.086	JB3.086	F2.C11	IO_L11N_T1_SRCC_42	Bank42
J3.087	JB3.087	F2.P13	IO_L1P_T0_42	Bank42	J3.088	JB3.088	F2.C12	IO_L11P_T1_SRCC_42	Bank42
J3.089	JB3.089	F2.M12	IO_L5N_T0_42	Bank42	J3.090	JB3.090	F2.A8	IO_L7N_T1_42	Bank42
J3.091	JB3.091	F2.N12	IO_L5P_T0_42	Bank42	J3.092	JB3.092	F2.B9	IO_L7P_T1_42	Bank42
J3.093	JB3.093	F2.P11	IO_L6N_T0_VREF_42	Bank42	J3.094	JB3.094	F2.D10	IO_L14N_T2_SRCC_42	Bank42
J3.095	JB3.095	F2.R11	IO_L6P_T0_42	Bank42	J3.096	JB3.096	F2.E10	IO_L14P_T2_SRCC_42	Bank42
J3.097	JB3.097	F2.M11	IO_L3N_T0_DQS_42	Bank42	J3.098	JB3.098	F2.C9	IO_L12N_T1_MRCC_42	Bank42
J3.099	JB3.099	F2.N11	IO_L3P_T0_DQS_42	Bank42	J3.100	JB3.100	F2.D9	IO_L12P_T1_MRCC_42	Bank42
J3.101	JB3.101	F2.R13	IO_L2N_T0_42	Bank42	J3.102	JB3.102	F2.K12	IO_L21N_T3_DQS_42	Bank42
J3.103	JB3.103	F2.T13	IO_L2P_T0_42	Bank42	J3.104	JB3.104	F2.L12	IO_L21P_T3_DQS_42	Bank42
J3.105	JB3.105	F2.R12	IO_L4N_T0_42	Bank42	J3.106	JB3.106	F2.J11	IO_L23N_T3_42	Bank42
J3.107	JB3.107	F2.T12	IO_L4P_T0_42	Bank42	J3.108	JB3.108	F2.K11	IO_L23P_T3_42	Bank42
J3.109	JB3.109	F2.P14	IO_L22N_T3_41	Bank41	J3.110	JB3.110	F2.J10	IO_L20N_T3_42	Bank42
J3.111	JB3.111	F2.P15	IO_L22P_T3_41	Bank41	J3.112	JB3.112	F2.K10	IO_L20P_T3_42	Bank42
J3.113	JB3.113	F2.R15	IO_L23N_T3_41	Bank41	J3.114	JB3.114	F2.F10	IO_L16N_T2_42	Bank42
J3.115	JB3.115	F2.T15	IO_L23P_T3_41	Bank41	J3.116	JB3.116	F2.G10	IO_L16P_T2_42	Bank42
J3.117	JB3.117	F2.F9	IO_L22N_T3_42	Bank42	J3.118	JB3.118	F2.H9	IO_L24N_T3_42	Bank42
J3.119	JB3.119	F2.G9	IO_L22P_T3_42	Bank42	J3.120	JB3.120	F2.J9	IO_L24P_T3_42	Bank42

J4 (Odd Pins)					J4 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J4.001	JB4.001	F2.G26	IO_L10N_T1_18	Bank18	J4.002	JB4.002	F2.N28	IO_L5N_T0_18	Bank18
J4.003	JB4.003	F2.H26	IO_L10P_T1_18	Bank18	J4.004	JB4.004	F2.P28	IO_L5P_T0_18	Bank18
J4.005	JB4.005	F2.H28	IO_L8N_T1_18	Bank18	J4.006	JB4.006	F2.R28	IO_L1N_T0_18	Bank18
J4.007	JB4.007	F2.H27	IO_L8P_T1_18	Bank18	J4.008	JB4.008	F2.T28	IO_L1P_T0_18	Bank18
J4.009	JB4.009	F2.F29	IO_L7N_T1_18	Bank18	J4.010	JB4.010	F2.P26	IO_L2N_T0_18	Bank18
J4.011	JB4.011	F2.G29	IO_L7P_T1_18	Bank18	J4.012	JB4.012	F2.R26	IO_L2P_T0_18	Bank18
J4.013	JB4.013	F2.P25	IO_L6N_T0_VREF_18	Bank18	J4.014	JB4.014	F2.N27	IO_L4N_T0_18	Bank18
J4.015	JB4.015	F2.R25	IO_L6P_T0_18	Bank18	J4.016	JB4.016	F2.N26	IO_L4P_T0_18	Bank18
J4.017	JB4.017	F2.N23	IO_L5N_T0_17	Bank17	J4.018	JB4.018	F2.K27	IO_L20N_T3_18	Bank18
J4.019	JB4.019	F2.P23	IO_L5P_T0_17	Bank17	J4.020	JB4.020	F2.L27	IO_L20P_T3_18	Bank18
J4.021	JB4.021	F2.E28	IO_L12N_T1_MRCC_18	Bank18	J4.022	JB4.022	F2.J28	IO_L22N_T3_18	Bank18

J4 (Odd Pins)					J4 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J4.023	JB4.023	F2.F28	IO_L12P_T1_MRCC_18	Bank18	J4.024	JB4.024	F2.K28	IO_L22P_T3_18	Bank18
J4.025	JB4.025	F2.R23	IO_L2N_T0_17	Bank17	J4.026	JB4.026	F2.L28	IO_L19N_T3_VREF_18	Bank18
J4.027	JB4.027	F2.T23	IO_L2P_T0_17	Bank17	J4.028	JB4.028	F2.M27	IO_L19P_T3_18	Bank18
J4.029	JB4.029	F2.R27	IO_L3N_T0_DQS_18	Bank18	J4.030	JB4.030	F2.E27	IO_L11N_T1_SRCC_18	Bank18
J4.031	JB4.031	F2.T27	IO_L3P_T0_DQS_18	Bank18	J4.032	JB4.032	F2.E26	IO_L11P_T1_SRCC_18	Bank18
J4.033	JB4.033	F2.N24	IO_L1N_T0_17	Bank17	J4.034	JB4.034	F2.D29	IO_L13N_T2_MRCC_18	Bank18
J4.035	JB4.035	F2.P24	IO_L1P_T0_17	Bank17	J4.036	JB4.036	F2.D28	IO_L13P_T2_MRCC_18	Bank18
J4.037	JB4.037	F2.M26	IO_L24N_T3_18	Bank18	J4.038	JB4.038	F2.C28	IO_L14N_T2_SRCC_18	Bank18
J4.039	JB4.039	F2.M25	IO_L24P_T3_18	Bank18	J4.040	JB4.040	F2.C27	IO_L14P_T2_SRCC_18	Bank18
J4.041	JB4.041	F2.L24	IO_L21N_T3_DQS_17	Bank17	J4.042	JB4.042	F2.A28	IO_L18N_T2_18	Bank18
J4.043	JB4.043	F2.M24	IO_L21P_T3_DQS_17	Bank17	J4.044	JB4.044	F2.A27	IO_L18P_T2_18	Bank18
J4.045	JB4.045	F2.K25	IO_L21N_T3_DQS_18	Bank18	J4.046	JB4.046	F2.B27	IO_L16N_T2_18	Bank18
J4.047	JB4.047	F2.L25	IO_L21P_T3_DQS_18	Bank18	J4.048	JB4.048	F2.B26	IO_L16P_T2_18	Bank18
J4.049	JB4.049	F2.J26	IO_L23N_T3_18	Bank18	J4.050	JB4.050	F2.F27	IO_L9N_T1_DQS_18	Bank18
J4.051	JB4.051	F2.K26	IO_L23P_T3_18	Bank18	J4.052	JB4.052	F2.G27	IO_L9P_T1_DQS_18	Bank18
J4.053	JB4.053	F2.P21	IO_L6N_T0_VREF_17	Bank17	J4.054	JB4.054	F2.F25	IO_L10N_T1_17	Bank17
J4.055	JB4.055	F2.R21	IO_L6P_T0_17	Bank17	J4.056	JB4.056	F2.G25	IO_L10P_T1_17	Bank17
J4.057	JB4.057	F2.H23	IO_L7N_T1_17	Bank17	J4.058	JB4.058	F2.F24	IO_L9N_T1_DQS_17	Bank17
J4.059	JB4.059	F2.J23	IO_L7P_T1_17	Bank17	J4.060	JB4.060	F2.G24	IO_L9P_T1_DQS_17	Bank17
J4.061	JB4.061	F2.E23	IO_L12N_T1_MRCC_17	Bank17	J4.062	JB4.062	F2.C23	IO_L13N_T2_MRCC_17	Bank17
J4.063	JB4.063	F2.F23	IO_L12P_T1_MRCC_17	Bank17	J4.064	JB4.064	F2.D23	IO_L13P_T2_MRCC_17	Bank17
J4.065	JB4.065	F2.A22	IO_L17N_T2_17	Bank17	J4.066	JB4.066	F2.K23	IO_L19N_T3_VREF_17	Bank17
J4.067	JB4.067	F2.A23	IO_L17P_T2_17	Bank17	J4.068	JB4.068	F2.L23	IO_L19P_T3_17	Bank17
J4.069	JB4.069	F2.C24	IO_L14N_T2_SRCC_17	Bank17	J4.070	JB4.070	F2.C26	IO_L15N_T2_DQS_18	Bank18
J4.071	JB4.071	F2.D24	IO_L14P_T2_SRCC_17	Bank17	J4.072	JB4.072	F2.D26	IO_L15P_T2_DQS_18	Bank18
J4.073	JB4.073	F2.E22	IO_L11N_T1_SRCC_17	Bank17	J4.074	JB4.074	F2.A25	IO_L17N_T2_18	Bank18
J4.075	JB4.075	F2.F22	IO_L11P_T1_SRCC_17	Bank17	J4.076	JB4.076	F2.B25	IO_L17P_T2_18	Bank18
J4.077	JB4.077	F2.B22	IO_L15N_T2_DQS_17	Bank17	J4.078	JB4.078	F2.A24	IO_L18N_T2_17	Bank17
J4.079	JB4.079	F2.C22	IO_L15P_T2_DQS_17	Bank17	J4.080	JB4.080	F2.B24	IO_L18P_T2_17	Bank17
J4.081	JB4.081	F2.B21	IO_L10N_T1_40	Bank40	J4.082	JB4.082	F2.D25	IO_L16N_T2_17	Bank17
J4.083	JB4.083	F2.C21	IO_L10P_T1_40	Bank40	J4.084	JB4.084	F2.E25	IO_L16P_T2_17	Bank17
J4.085	JB4.085	F2.A20	IO_L8N_T1_40	Bank40	J4.086	JB4.086	F2.G22	IO_L20N_T3_17	Bank17
J4.087	JB4.087	F2.B20	IO_L8P_T1_40	Bank40	J4.088	JB4.088	F2.H22	IO_L20P_T3_17	Bank17
J4.089	JB4.089	F2.A18	IO_L7N_T1_40	Bank40	J4.090	JB4.090	F2.H21	IO_L24N_T3_17	Bank17
J4.091	JB4.091	F2.A19	IO_L7P_T1_40	Bank40	J4.092	JB4.092	F2.J21	IO_L24P_T3_17	Bank17
J4.093	JB4.093	F2.L19	IO_L6N_T0_VREF_40	Bank40	J4.094	JB4.094	F2.K21	IO_L23N_T3_17	Bank17
J4.095	JB4.095	F2.M19	IO_L6P_T0_40	Bank40	J4.096	JB4.096	F2.K22	IO_L23P_T3_17	Bank17
J4.097	JB4.097	F2.B19	IO_L9N_T1_DQS_40	Bank40	J4.098	JB4.098	F2.D19	IO_L12N_T1_MRCC_40	Bank40
J4.099	JB4.099	F2.C19	IO_L9P_T1_DQS_40	Bank40	J4.100	JB4.100	F2.D20	IO_L12P_T1_MRCC_40	Bank40
J4.101	JB4.101	F2.C18	IO_L11N_T1_SRCC_40	Bank40	J4.102	JB4.102	F2.L22	IO_L22N_T3_17	Bank17
J4.103	JB4.103	F2.D18	IO_L11P_T1_SRCC_40	Bank40	J4.104	JB4.104	F2.M22	IO_L22P_T3_17	Bank17
J4.105	JB4.105	F2.H19	IO_L5N_T0_40	Bank40	J4.106	JB4.106	F2.L20	IO_L4N_T0_40	Bank40
J4.107	JB4.107	F2.J19	IO_L5P_T0_40	Bank40	J4.108	JB4.108	F2.M20	IO_L4P_T0_40	Bank40
J4.109	JB4.109	F2.H18	IO_L3N_T0_DQS_40	Bank40	J4.110	JB4.110	F2.H24	IO_L8N_T1_17	Bank17
J4.111	JB4.111	F2.J18	IO_L3P_T0_DQS_40	Bank40	J4.112	JB4.112	F2.J24	IO_L8P_T1_17	Bank17
J4.113	JB4.113	F2.K18	IO_L2N_T0_40	Bank40	J4.114	JB4.114	F2.N21	IO_L3N_T0_DQS_17	Bank17
J4.115	JB4.115	F2.L18	IO_L2P_T0_40	Bank40	J4.116	JB4.116	F2.N22	IO_L3P_T0_DQS_17	Bank17
J4.117	JB4.117	F2.K17	IO_L1N_T0_40	Bank40	J4.118	JB4.118	F2.R22	IO_L4N_T0_17	Bank17
J4.119	JB4.119	F2.L17	IO_L1P_T0_40	Bank40	J4.120	JB4.120	F2.T22	IO_L4P_T0_17	Bank17

J5 (Odd Pins)					J5 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J5.001	JB5.001	F2.N37	IO_L2N_T0_20	Bank20	J5.002	JB5.002	F2.T38	IO_L9N_T1_DQS_20	Bank20
J5.003	JB5.003	F2.N36	IO_L2P_T0_20	Bank20	J5.004	JB5.004	F2.T37	IO_L9P_T1_DQS_20	Bank20
J5.005	JB5.005	F2.N43	IO_L15N_T2_DQS_20	Bank20	J5.006	JB5.006	F2.N42	IO_L10N_T1_20	Bank20
J5.007	JB5.007	F2.P43	IO_L15P_T2_DQS_20	Bank20	J5.008	JB5.008	F2.P41	IO_L10P_T1_20	Bank20
J5.009	JB5.009	F2.P40	IO_L11N_T1_SRCC_20	Bank20	J5.010	JB5.010	F2.P38	IO_L12N_T1_MRCC_20	Bank20
J5.011	JB5.011	F2.P39	IO_L11P_T1_SRCC_20	Bank20	J5.012	JB5.012	F2.R38	IO_L12P_T1_MRCC_20	Bank20
J5.013	JB5.013	F2.T34	IO_L19N_T3_VREF_20	Bank20	J5.014	JB5.014	F2.J44	IO_L18N_T2_21	Bank21
J5.015	JB5.015	F2.T33	IO_L19P_T3_20	Bank20	J5.016	JB5.016	F2.J43	IO_L18P_T2_21	Bank21
J5.017	JB5.017	F2.T44	IO_L18N_T2_20	Bank20	J5.018	JB5.018	F2.L44	IO_L17N_T2_21	Bank21
J5.019	JB5.019	F2.U44	IO_L18P_T2_20	Bank20	J5.020	JB5.020	F2.M44	IO_L17P_T2_21	Bank21
J5.021	JB5.021	F2.N44	IO_L17N_T2_20	Bank20	J5.022	JB5.022	F2.T40	IO_L7N_T1_20	Bank20
J5.023	JB5.023	F2.P44	IO_L17P_T2_20	Bank20	J5.024	JB5.024	F2.T39	IO_L7P_T1_20	Bank20
J5.025	JB5.025	F2.M37	IO_L21N_T3_DQS_21	Bank21	J5.026	JB5.026	F2.M40	IO_L6N_T0_VREF_20	Bank20
J5.027	JB5.027	F2.M36	IO_L21P_T3_DQS_21	Bank21	J5.028	JB5.028	F2.M39	IO_L6P_T0_20	Bank20
J5.029	JB5.029	F2.L40	IO_L8N_T1_21	Bank21	J5.030	JB5.030	F2.R42	IO_L14N_T2_SRCC_20	Bank20
J5.031	JB5.031	F2.L39	IO_L8P_T1_21	Bank21	J5.032	JB5.032	F2.T42	IO_L14P_T2_SRCC_20	Bank20
J5.033	JB5.033	F2.K38	IO_L10N_T1_21	Bank21	J5.034	JB5.034	F2.R41	IO_L13N_T2_MRCC_20	Bank20
J5.035	JB5.035	F2.L38	IO_L10P_T1_21	Bank21	J5.036	JB5.036	F2.R40	IO_L13P_T2_MRCC_20	Bank20
J5.037	JB5.037	F2.K42	IO_L14N_T2_SRCC_21	Bank21	J5.038	JB5.038	F2.R43	IO_L16N_T2_20	Bank20
J5.039	JB5.039	F2.K41	IO_L14P_T2_SRCC_21	Bank21	J5.040	JB5.040	F2.T43	IO_L16P_T2_20	Bank20
J5.041	JB5.041	F2.R35	IO_L3N_T0_DQS_20	Bank20	J5.042	JB5.042	F2.M41	IO_L8N_T1_20	Bank20
J5.043	JB5.043	F2.T35	IO_L3P_T0_DQS_20	Bank20	J5.044	JB5.044	F2.N41	IO_L8P_T1_20	Bank20
J5.045	JB5.045	F2.P36	IO_L1N_T0_20	Bank20	J5.046	JB5.046	F2.K43	IO_L15N_T2_DQS_21	Bank21
J5.047	JB5.047	F2.P35	IO_L1P_T0_20	Bank20	J5.048	JB5.048	F2.L43	IO_L15P_T2_DQS_21	Bank21
J5.049	JB5.049	F2.R37	IO_L5N_T0_20	Bank20	J5.050	JB5.050	F2.H39	IO_L3N_T0_DQS_21	Bank21
J5.051	JB5.051	F2.R36	IO_L5P_T0_20	Bank20	J5.052	JB5.052	F2.J39	IO_L3P_T0_DQS_21	Bank21
J5.053	JB5.053	F2.J36	IO_L19N_T3_VREF_21	Bank21	J5.054	JB5.054	F2.K37	IO_L20N_T3_21	Bank21
J5.055	JB5.055	F2.K36	IO_L19P_T3_21	Bank21	J5.056	JB5.056	F2.L37	IO_L20P_T3_21	Bank21
J5.057	JB5.057	F2.N39	IO_L4N_T0_20	Bank20	J5.058	JB5.058	F2.G42	IO_L7N_T1_21	Bank21
J5.059	JB5.059	F2.N38	IO_L4P_T0_20	Bank20	J5.060	JB5.060	F2.G41	IO_L7P_T1_21	Bank21
J5.061	JB5.061	F2.J40	IO_L12N_T1_MRCC_21	Bank21	J5.062	JB5.062	F2.L42	IO_L13N_T2_MRCC_21	Bank21
J5.063	JB5.063	F2.K40	IO_L12P_T1_MRCC_21	Bank21	J5.064	JB5.064	F2.M42	IO_L13P_T2_MRCC_21	Bank21
J5.065	JB5.065	F2.E43	IO_L24N_T3_22	Bank22	J5.066	JB5.066	F2.H37	IO_L6N_T0_VREF_21	Bank21
J5.067	JB5.067	F2.F42	IO_L24P_T3_22	Bank22	J5.068	JB5.068	F2.H36	IO_L6P_T0_21	Bank21
J5.069	JB5.069	F2.H38	IO_L5N_T0_21	Bank21	J5.070	JB5.070	F2.H41	IO_L11N_T1_SRCC_21	Bank21
J5.071	JB5.071	F2.J38	IO_L5P_T0_21	Bank21	J5.072	JB5.072	F2.J41	IO_L11P_T1_SRCC_21	Bank21
J5.073	JB5.073	F2.E42	IO_L20N_T3_22	Bank22	J5.074	JB5.074	F2.E35	IO_L6N_T0_VREF_22	Bank22
J5.075	JB5.075	F2.E41	IO_L20P_T3_22	Bank22	J5.076	JB5.076	F2.F35	IO_L6P_T0_22	Bank22
J5.077	JB5.077	F2.C44	IO_L22N_T3_22	Bank22	J5.078	JB5.078	F2.H43	IO_L9N_T1_DQS_21	Bank21
J5.079	JB5.079	F2.C43	IO_L22P_T3_22	Bank22	J5.080	JB5.080	F2.H42	IO_L9P_T1_DQS_21	Bank21
J5.081	JB5.081	F2.B42	IO_L17N_T2_22	Bank22	J5.082	JB5.082	F2.G40	IO_L1N_T0_21	Bank21
J5.083	JB5.083	F2.C42	IO_L17P_T2_22	Bank22	J5.084	JB5.084	F2.G39	IO_L1P_T0_21	Bank21
J5.085	JB5.085	F2.A42	IO_L15N_T2_DQS_22	Bank22	J5.086	JB5.086	F2.F44	IO_L23N_T3_22	Bank22
J5.087	JB5.087	F2.B41	IO_L15P_T2_DQS_22	Bank22	J5.088	JB5.088	F2.F43	IO_L23P_T3_22	Bank22
J5.089	JB5.089	F2.C41	IO_L13N_T2_MRCC_22	Bank22	J5.090	JB5.090	F2.F39	IO_L9N_T1_DQS_22	Bank22
J5.091	JB5.091	F2.D41	IO_L13P_T2_MRCC_22	Bank22	J5.092	JB5.092	F2.F38	IO_L9P_T1_DQS_22	Bank22
J5.093	JB5.093	F2.E40	IO_L19N_T3_VREF_22	Bank22	J5.094	JB5.094	F2.D40	IO_L14N_T2_SRCC_22	Bank22
J5.095	JB5.095	F2.F40	IO_L19P_T3_22	Bank22	J5.096	JB5.096	F2.D39	IO_L14P_T2_SRCC_22	Bank22
J5.097	JB5.097	F2.B40	IO_L16N_T2_22	Bank22	J5.098	JB5.098	F2.C39	IO_L12N_T1_MRCC_22	Bank22

J5 (Odd Pins)					J5 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J5.099	JB5.099	F2.B39	IO_L16P_T2_22	Bank22	J5.100	JB5.100	F2.C38	IO_L12P_T1_MRCC_22	Bank22
J5.101	JB5.101	F2.B37	IO_L10N_T1_22	Bank22	J5.102	JB5.102	F2.A40	IO_L18N_T2_22	Bank22
J5.103	JB5.103	F2.C37	IO_L10P_T1_22	Bank22	J5.104	JB5.104	F2.A39	IO_L18P_T2_22	Bank22
J5.105	JB5.105	F2.A38	IO_L8N_T1_22	Bank22	J5.106	JB5.106	F2.G37	IO_L4N_T0_21	Bank21
J5.107	JB5.107	F2.A37	IO_L8P_T1_22	Bank22	J5.108	JB5.108	F2.G36	IO_L4P_T0_21	Bank21
J5.109	JB5.109	F2.D38	IO_L11N_T1_SRCC_22	Bank22	J5.110	JB5.110	F2.E37	IO_L7N_T1_22	Bank22
J5.111	JB5.111	F2.E38	IO_L11P_T1_SRCC_22	Bank22	J5.112	JB5.112	F2.E36	IO_L7P_T1_22	Bank22
J5.113	JB5.113	F2.B36	IO_L5N_T0_22	Bank22	J5.114	JB5.114	F2.G44	IO_L16N_T2_21	Bank21
J5.115	JB5.115	F2.C36	IO_L5P_T0_22	Bank22	J5.116	JB5.116	F2.H44	IO_L16P_T2_21	Bank21
J5.117	JB5.117	F2.D36	IO_L3N_T0_DQS_22	Bank22	J5.118	JB5.118	F2.D44	IO_L21N_T3_DQS_22	Bank22
J5.119	JB5.119	F2.D35	IO_L3P_T0_DQS_22	Bank22	J5.120	JB5.120	F2.D43	IO_L21P_T3_DQS_22	Bank22

J8 (Odd Pins)					J8 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J8.001	JB8.001	F1.AW39	IO_L15N_T2_DQS_11	Bank11	J8.002	JB8.002	F1.AR36	IO_L5N_T0_12	Bank12
J8.003	JB8.003	F1.AW38	IO_L15P_T2_DQS_11	Bank11	J8.004	JB8.004	F1.AR35	IO_L5P_T0_12	Bank12
J8.005	JB8.005	F1.AY37	IO_L18N_T2_11	Bank11	J8.006	JB8.006	F1.AU37	IO_L21N_T3_DQS_12	Bank12
J8.007	JB8.007	F1.AY36	IO_L18P_T2_11	Bank11	J8.008	JB8.008	F1.AU36	IO_L21P_T3_DQS_12	Bank12
J8.009	JB8.009	F1.BA38	IO_L14N_T2_SRCC_11	Bank11	J8.010	JB8.010	F1.AV37	IO_L24N_T3_12	Bank12
J8.011	JB8.011	F1.BA37	IO_L14P_T2_SRCC_11	Bank11	J8.012	JB8.012	F1.AV36	IO_L24P_T3_12	Bank12
J8.013	JB8.013	F1.BB34	IO_L19N_T3_VREF_11	Bank11	J8.014	JB8.014	F1.BD41	IO_L8N_T1_11	Bank11
J8.015	JB8.015	F1.BA34	IO_L19P_T3_11	Bank11	J8.016	JB8.016	F1.BD40	IO_L8P_T1_11	Bank11
J8.017	JB8.017	F1.AV39	IO_L23N_T3_12	Bank12	J8.018	JB8.018	F1.BD39	IO_L10N_T1_11	Bank11
J8.019	JB8.019	F1.AV38	IO_L23P_T3_12	Bank12	J8.020	JB8.020	F1.BC39	IO_L10P_T1_11	Bank11
J8.021	JB8.021	F1.BA39	IO_L13N_T2_MRCC_11	Bank11	J8.022	JB8.022	F1.AT40	IO_L14N_T2_SRCC_12	Bank12
J8.023	JB8.023	F1.AY38	IO_L13P_T2_MRCC_11	Bank11	J8.024	JB8.024	F1.AT39	IO_L14P_T2_SRCC_12	Bank12
J8.025	JB8.025	F1.BD38	IO_L17N_T2_11	Bank11	J8.026	JB8.026	F1.BB42	IO_L6N_T0_VREF_11	Bank11
J8.027	JB8.027	F1.BC38	IO_L17P_T2_11	Bank11	J8.028	JB8.028	F1.BA42	IO_L6P_T0_11	Bank11
J8.029	JB8.029	F1.BB40	IO_L11N_T1_SRCC_11	Bank11	J8.030	JB8.030	F1.AY42	IO_L5N_T0_11	Bank11
J8.031	JB8.031	F1.BB39	IO_L11P_T1_SRCC_11	Bank11	J8.032	JB8.032	F1.AY41	IO_L5P_T0_11	Bank11
J8.033	JB8.033	F1.BC43	IO_L9N_T1_DQS_11	Bank11	J8.034	JB8.034	F1.BA40	IO_L12N_T1_MRCC_11	Bank11
J8.035	JB8.035	F1.BC42	IO_L9P_T1_DQS_11	Bank11	J8.036	JB8.036	F1.AY40	IO_L12P_T1_MRCC_11	Bank11
J8.037	JB8.037	F1.BC41	IO_L7N_T1_11	Bank11	J8.038	JB8.038	F1.AW41	IO_L1N_T0_11	Bank11
J8.039	JB8.039	F1.BB41	IO_L7P_T1_11	Bank11	J8.040	JB8.040	F1.AW40	IO_L1P_T0_11	Bank11
J8.041	JB8.041	F1.BB44	IO_L4N_T0_11	Bank11	J8.042	JB8.042	F1.AV41	IO_L15N_T2_DQS_12	Bank12
J8.043	JB8.043	F1.BA44	IO_L4P_T0_11	Bank11	J8.044	JB8.044	F1.AU41	IO_L15P_T2_DQS_12	Bank12
J8.045	JB8.045	F1.BA43	IO_L2N_T0_11	Bank11	J8.046	JB8.046	F1.AV42	IO_L17N_T2_12	Bank12
J8.047	JB8.047	F1.AY43	IO_L2P_T0_11	Bank11	J8.048	JB8.048	F1.AU42	IO_L17P_T2_12	Bank12
J8.049	JB8.049	F1.AW44	IO_L3N_T0_DQS_11	Bank11	J8.050	JB8.050	F1.AU44	IO_L16N_T2_12	Bank12
J8.051	JB8.051	F1.AW43	IO_L3P_T0_DQS_11	Bank11	J8.052	JB8.052	F1.AT44	IO_L16P_T2_12	Bank12
J8.053	JB8.053	F1.AT38	IO_L19N_T3_VREF_12	Bank12	J8.054	JB8.054	F1.AN38	IO_L2N_T0_12	Bank12
J8.055	JB8.055	F1.AT37	IO_L19P_T3_12	Bank12	J8.056	JB8.056	F1.AN37	IO_L2P_T0_12	Bank12
J8.057	JB8.057	F1.AV44	IO_L18N_T2_12	Bank12	J8.058	JB8.058	F1.AR41	IO_L11N_T1_SRCC_12	Bank12
J8.059	JB8.059	F1.AV43	IO_L18P_T2_12	Bank12	J8.060	JB8.060	F1.AR40	IO_L11P_T1_SRCC_12	Bank12
J8.061	JB8.061	F1.AU40	IO_L13N_T2_MRCC_12	Bank12	J8.062	JB8.062	F1.AT42	IO_L12N_T1_MRCC_12	Bank12
J8.063	JB8.063	F1.AU39	IO_L13P_T2_MRCC_12	Bank12	J8.064	JB8.064	F1.AR42	IO_L12P_T1_MRCC_12	Bank12
J8.065	JB8.065	F1.AR38	IO_L1N_T0_12	Bank12	J8.066	JB8.066	F1.AP36	IO_L6N_T0_VREF_12	Bank12

J8 (Odd Pins)					J8 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J8.067	JB8.067	F1.AR37	IO_L1P_T0_12	Bank12	J8.068	JB8.068	F1.AN36	IO_L6P_T0_12	Bank12
J8.069	JB8.069	F1.AP39	IO_L4N_T0_12	Bank12	J8.070	JB8.070	F1.AT43	IO_L10N_T1_12	Bank12
J8.071	JB8.071	F1.AP38	IO_L4P_T0_12	Bank12	J8.072	JB8.072	F1.AR43	IO_L10P_T1_12	Bank12
J8.073	JB8.073	F1.AP40	IO_L7N_T1_12	Bank12	J8.074	JB8.074	F1.AH38	IO_L8N_T1_13	Bank13
J8.075	JB8.075	F1.AN39	IO_L7P_T1_12	Bank12	J8.076	JB8.076	F1.AH37	IO_L8P_T1_13	Bank13
J8.077	JB8.077	F1.AP41	IO_L9N_T1_DQS_12	Bank12	J8.078	JB8.078	F1.AK38	IO_L10N_T1_13	Bank13
J8.079	JB8.079	F1.AN41	IO_L9P_T1_DQS_12	Bank12	J8.080	JB8.080	F1.AJ38	IO_L10P_T1_13	Bank13
J8.081	JB8.081	F1.AP44	IO_L8N_T1_12	Bank12	J8.082	JB8.082	F1.AK37	IO_L12N_T1_MRCC_13	Bank13
J8.083	JB8.083	F1.AP43	IO_L8P_T1_12	Bank12	J8.084	JB8.084	F1.AK36	IO_L12P_T1_MRCC_13	Bank13
J8.085	JB8.085	F1.AN44	IO_L17N_T2_13	Bank13	J8.086	JB8.086	F1.AL38	IO_L11N_T1_SRCC_13	Bank13
J8.087	JB8.087	F1.AN43	IO_L17P_T2_13	Bank13	J8.088	JB8.088	F1.AL37	IO_L11P_T1_SRCC_13	Bank13
J8.089	JB8.089	F1.AM44	IO_L18N_T2_13	Bank13	J8.090	JB8.090	F1.AM37	IO_L9N_T1_DQS_13	Bank13
J8.091	JB8.091	F1.AL44	IO_L18P_T2_13	Bank13	J8.092	JB8.092	F1.AM36	IO_L9P_T1_DQS_13	Bank13
J8.093	JB8.093	F1.AJ40	IO_L6N_T0_VREF_13	Bank13	J8.094	JB8.094	F1.AL43	IO_L16N_T2_13	Bank13
J8.095	JB8.095	F1.AJ39	IO_L6P_T0_13	Bank13	J8.096	JB8.096	F1.AL42	IO_L16P_T2_13	Bank13
J8.097	JB8.097	F1.AJ44	IO_L4N_T0_13	Bank13	J8.098	JB8.098	F1.AM41	IO_L13N_T2_MRCC_13	Bank13
J8.099	JB8.099	F1.AJ43	IO_L4P_T0_13	Bank13	J8.100	JB8.100	F1.AM40	IO_L13P_T2_MRCC_13	Bank13
J8.101	JB8.101	F1.AH44	IO_L2N_T0_13	Bank13	J8.102	JB8.102	F1.AK43	IO_L3N_T0_DQS_13	Bank13
J8.103	JB8.103	F1.AH43	IO_L2P_T0_13	Bank13	J8.104	JB8.104	F1.AK42	IO_L3P_T0_DQS_13	Bank13
J8.105	JB8.105	F1.AL40	IO_L5N_T0_13	Bank13	J8.106	JB8.106	F1.AN42	IO_L15N_T2_DQS_13	Bank13
J8.107	JB8.107	F1.AK40	IO_L5P_T0_13	Bank13	J8.108	JB8.108	F1.AM42	IO_L15P_T2_DQS_13	Bank13
J8.109	JB8.109	F1.AK41	IO_L1N_T0_13	Bank13	J8.110	JB8.110	F1.AM39	IO_L14N_T2_SRCC_13	Bank13
J8.111	JB8.111	F1.AJ41	IO_L1P_T0_13	Bank13	J8.112	JB8.112	F1.AL39	IO_L14P_T2_SRCC_13	Bank13
J8.113	JB8.113	F1.AM35	IO_L24N_T3_13	Bank13	J8.114	JB8.114	F1.AJ36	IO_L7N_T1_13	Bank13
J8.115	JB8.115	F1.AL35	IO_L24P_T3_13	Bank13	J8.116	JB8.116	F1.AH36	IO_L7P_T1_13	Bank13
J8.117	JB8.117	F1.AK35	IO_L20N_T3_13	Bank13	J8.118	JB8.118	F1.AJ34	IO_L19N_T3_VREF_13	Bank13
J8.119	JB8.119	F1.AJ35	IO_L20P_T3_13	Bank13	J8.120	JB8.120	F1.AJ33	IO_L19P_T3_13	Bank13

J9 (Odd Pins)					J9 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J9.001	JB9.001	F1.AV22	IO_L9N_T1_DQS_34	Bank34	J9.002	JB9.002	F1.BA18	IO_L8N_T1_33	Bank33
J9.003	JB9.003	F1.AU22	IO_L9P_T1_DQS_34	Bank34	J9.004	JB9.004	F1.AY18	IO_L8P_T1_33	Bank33
J9.005	JB9.005	F1.AW18	IO_L10N_T1_33	Bank33	J9.006	JB9.006	F1.BD18	IO_L4N_T0_33	Bank33
J9.007	JB9.007	F1.AW19	IO_L10P_T1_33	Bank33	J9.008	JB9.008	F1.BC18	IO_L4P_T0_33	Bank33
J9.009	JB9.009	F1.AU19	IO_L11N_T1_SRCC_33	Bank33	J9.010	JB9.010	F1.BD19	IO_L5N_T0_33	Bank33
J9.011	JB9.011	F1.AT19	IO_L11P_T1_SRCC_33	Bank33	J9.012	JB9.012	F1.BC19	IO_L5P_T0_33	Bank33
J9.013	JB9.013	F1.BB19	IO_L6N_T0_VREF_33	Bank33	J9.014	JB9.014	F1.BD20	IO_L3N_T0_DQS_33	Bank33
J9.015	JB9.015	F1.BA19	IO_L6P_T0_33	Bank33	J9.016	JB9.016	F1.BD21	IO_L3P_T0_DQS_33	Bank33
J9.017	JB9.017	F1.AY20	IO_L9N_T1_DQS_33	Bank33	J9.018	JB9.018	F1.BC21	IO_L1N_T0_33	Bank33
J9.019	JB9.019	F1.AW20	IO_L9P_T1_DQS_33	Bank33	J9.020	JB9.020	F1.BB21	IO_L1P_T0_33	Bank33
J9.021	JB9.021	F1.AV18	IO_L12N_T1_MRCC_33	Bank33	J9.022	JB9.022	F1.BD23	IO_L5N_T0_34	Bank34
J9.023	JB9.023	F1.AV19	IO_L12P_T1_MRCC_33	Bank33	J9.024	JB9.024	F1.BC23	IO_L5P_T0_34	Bank34
J9.025	JB9.025	F1.AY21	IO_L7N_T1_33	Bank33	J9.026	JB9.026	F1.BA23	IO_L6N_T0_VREF_34	Bank34
J9.027	JB9.027	F1.AW21	IO_L7P_T1_33	Bank33	J9.028	JB9.028	F1.BA22	IO_L6P_T0_34	Bank34

J9 (Odd Pins)					J9 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J9.029	JB9.029	F1.AY23	IO_L10N_T1_34	Bank34	J9.030	JB9.030	F1.BC22	IO_L4N_T0_34	Bank34
J9.031	JB9.031	F1.AY22	IO_L10P_T1_34	Bank34	J9.032	JB9.032	F1.BB22	IO_L4P_T0_34	Bank34
J9.033	JB9.033	F1.AW23	IO_L7N_T1_34	Bank34	J9.034	JB9.034	F1.AW24	IO_L12N_T1_MRCC_34	Bank34
J9.035	JB9.035	F1.AV23	IO_L7P_T1_34	Bank34	J9.036	JB9.036	F1.AV24	IO_L12P_T1_MRCC_34	Bank34
J9.037	JB9.037	F1.AT22	IO_L15N_T2_DQS_34	Bank34	J9.038	JB9.038	F1.BB20	IO_L2N_T0_33	Bank33
J9.039	JB9.039	F1.AR22	IO_L15P_T2_DQS_34	Bank34	J9.040	JB9.040	F1.BA20	IO_L2P_T0_33	Bank33
J9.041	JB9.041	F1.AN23	IO_L18N_T2_34	Bank34	J9.042	JB9.042	F1.BD25	IO_L3N_T0_DQS_34	Bank34
J9.043	JB9.043	F1.AN22	IO_L18P_T2_34	Bank34	J9.044	JB9.044	F1.BD24	IO_L3P_T0_DQS_34	Bank34
J9.045	JB9.045	F1.AN21	IO_L21N_T3_DQS_34	Bank34	J9.046	JB9.046	F1.BC24	IO_L1N_T0_34	Bank34
J9.047	JB9.047	F1.AM21	IO_L21P_T3_DQS_34	Bank34	J9.048	JB9.048	F1.BB24	IO_L1P_T0_34	Bank34
J9.049	JB9.049	F1.AM22	IO_L23N_T3_34	Bank34	J9.050	JB9.050	F1.BD26	IO_L1N_T0_AD4N_35	Bank35
J9.051	JB9.051	F1.AL22	IO_L23P_T3_34	Bank34	J9.052	JB9.052	F1.BC26	IO_L1P_T0_AD4P_35	Bank35
J9.053	JB9.053	F1.AM24	IO_L19N_T3_VREF_34	Bank34	J9.054	JB9.054	F1.BD29	IO_L4N_T0_35	Bank35
J9.055	JB9.055	F1.AL24	IO_L19P_T3_34	Bank34	J9.056	JB9.056	F1.BD28	IO_L4P_T0_35	Bank35
J9.057	JB9.057	F1.AK22	IO_L20N_T3_34	Bank34	J9.058	JB9.058	F1.BC29	IO_L2N_T0_AD12N_35	Bank35
J9.059	JB9.059	F1.AK21	IO_L20P_T3_34	Bank34	J9.060	JB9.060	F1.BB29	IO_L2P_T0_AD12P_35	Bank35
J9.061	JB9.061	F1.AT24	IO_L13N_T2_MRCC_34	Bank34	J9.062	JB9.062	F1.AU27	IO_L12N_T1_MRCC_35	Bank35
J9.063	JB9.063	F1.AT23	IO_L13P_T2_MRCC_34	Bank34	J9.064	JB9.064	F1.AU26	IO_L12P_T1_MRCC_35	Bank35
J9.065	JB9.065	F1.AJ24	IO_L24N_T3_34	Bank34	J9.066	JB9.066	F1.BC28	IO_L6N_T0_VREF_35	Bank35
J9.067	JB9.067	F1.AJ23	IO_L24P_T3_34	Bank34	J9.068	JB9.068	F1.BC27	IO_L6P_T0_35	Bank35
J9.069	JB9.069	F1.AR23	IO_L14N_T2_SRCC_34	Bank34	J9.070	JB9.070	F1.BB25	IO_L2N_T0_34	Bank34
J9.071	JB9.071	F1.AP23	IO_L14P_T2_SRCC_34	Bank34	J9.072	JB9.072	F1.BA24	IO_L2P_T0_34	Bank34
J9.073	JB9.073	F1.AL23	IO_L22N_T3_34	Bank34	J9.074	JB9.074	F1.BA25	IO_L8N_T1_34	Bank34
J9.075	JB9.075	F1.AK23	IO_L22P_T3_34	Bank34	J9.076	JB9.076	F1.AY25	IO_L8P_T1_34	Bank34
J9.077	JB9.077	F1.AT25	IO_L16N_T2_34	Bank34	J9.078	JB9.078	F1.BB27	IO_L3N_T0_DQS_AD5N_35	Bank35
J9.079	JB9.079	F1.AR25	IO_L16P_T2_34	Bank34	J9.080	JB9.080	F1.BB26	IO_L3P_T0_DQS_AD5P_35	Bank35
J9.081	JB9.081	F1.AY27	IO_L8N_T1_AD14N_35	Bank35	J9.082	JB9.082	F1.AU25	IO_L11N_T1_SRCC_34	Bank34
J9.083	JB9.083	F1.AY26	IO_L8P_T1_AD14P_35	Bank35	J9.084	JB9.084	F1.AU24	IO_L11P_T1_SRCC_34	Bank34
J9.085	JB9.085	F1.AW26	IO_L10N_T1_AD15N_35	Bank35	J9.086	JB9.086	F1.BA28	IO_L5N_T0_AD13N_35	Bank35
J9.087	JB9.087	F1.AV26	IO_L10P_T1_AD15P_35	Bank35	J9.088	JB9.088	F1.BA27	IO_L5P_T0_AD13P_35	Bank35
J9.089	JB9.089	F1.AP24	IO_L17N_T2_34	Bank34	J9.090	JB9.090	F1.BA29	IO_L7N_T1_AD6N_35	Bank35
J9.091	JB9.091	F1.AN24	IO_L17P_T2_34	Bank34	J9.092	JB9.092	F1.AY28	IO_L7P_T1_AD6P_35	Bank35
J9.093	JB9.093	F1.AN26	IO_L19N_T3_VREF_35	Bank35	J9.094	JB9.094	F1.AW29	IO_L9N_T1_DQS_AD7N_35	Bank35
J9.095	JB9.095	F1.AM26	IO_L19P_T3_35	Bank35	J9.096	JB9.096	F1.AW28	IO_L9P_T1_DQS_AD7P_35	Bank35
J9.097	JB9.097	F1.AM27	IO_L23N_T3_35	Bank35	J9.098	JB9.098	F1.AR27	IO_L13N_T2_MRCC_35	Bank35
J9.099	JB9.099	F1.AL27	IO_L23P_T3_35	Bank35	J9.100	JB9.100	F1.AR26	IO_L13P_T2_MRCC_35	Bank35
J9.101	JB9.101	F1.AN28	IO_L18N_T2_35	Bank35	J9.102	JB9.102	F1.AV28	IO_L11N_T1_SRCC_35	Bank35
J9.103	JB9.103	F1.AN27	IO_L18P_T2_35	Bank35	J9.104	JB9.104	F1.AV27	IO_L11P_T1_SRCC_35	Bank35
J9.105	JB9.105	F1.AM25	IO_L21N_T3_DQS_35	Bank35	J9.106	JB9.106	F1.AP26	IO_L17N_T2_35	Bank35
J9.107	JB9.107	F1.AL25	IO_L21P_T3_DQS_35	Bank35	J9.108	JB9.108	F1.AP25	IO_L17P_T2_35	Bank35
J9.109	JB9.109	F1.AL28	IO_L20N_T3_35	Bank35	J9.110	JB9.110	F1.AU29	IO_L16N_T2_35	Bank35
J9.111	JB9.111	F1.AK27	IO_L20P_T3_35	Bank35	J9.112	JB9.112	F1.AT29	IO_L16P_T2_35	Bank35
J9.113	JB9.113	F1.AK26	IO_L22N_T3_35	Bank35	J9.114	JB9.114	F1.AT28	IO_L14N_T2_SRCC_35	Bank35
J9.115	JB9.115	F1.AJ26	IO_L22P_T3_35	Bank35	J9.116	JB9.116	F1.AT27	IO_L14P_T2_SRCC_35	Bank35
J9.117	JB9.117	F1.AK25	IO_L24N_T3_35	Bank35	J9.118	JB9.118	F1.AR28	IO_L15N_T2_DQS_35	Bank35
J9.119	JB9.119	F1.AJ25	IO_L24P_T3_35	Bank35	J9.120	JB9.120	F1.AP28	IO_L15P_T2_DQS_35	Bank35

J10 (Odd Pins)	J10 (Even Pins)

Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J10.001	JB10.001	F1.AU10	IO_L15N_T2_DQS_31	Bank31	J10.002	JB10.002	F1.AJ10	IO_L2N_T0_31	Bank31
J10.003	JB10.003	F1.AT10	IO_L15P_T2_DQS_31	Bank31	J10.004	JB10.004	F1.AJ11	IO_L2P_T0_31	Bank31
J10.005	JB10.005	F1.AJ15	IO_L23N_T3_32	Bank32	J10.006	JB10.006	F1.BD10	IO_L22N_T3_31	Bank31
J10.007	JB10.007	F1.AJ16	IO_L23P_T3_32	Bank32	J10.008	JB10.008	F1.BD11	IO_L22P_T3_31	Bank31
J10.009	JB10.009	F1.AK12	IO_L4N_T0_31	Bank31	J10.010	JB10.010	F1.AL12	IO_L3N_T0_DQS_31	Bank31
J10.011	JB10.011	F1.AK13	IO_L4P_T0_31	Bank31	J10.012	JB10.012	F1.AL13	IO_L3P_T0_DQS_31	Bank31
J10.013	JB10.013	F1.AK10	IO_L6N_T0_VREF_31	Bank31	J10.014	JB10.014	F1.AT13	IO_L8N_T1_31	Bank31
J10.015	JB10.015	F1.AK11	IO_L6P_T0_31	Bank31	J10.016	JB10.016	F1.AR13	IO_L8P_T1_31	Bank31
J10.017	JB10.017	F1.AM10	IO_L5N_T0_31	Bank31	J10.018	JB10.018	F1.AP14	IO_L20N_T3_32	Bank32
J10.019	JB10.019	F1.AL10	IO_L5P_T0_31	Bank31	J10.020	JB10.020	F1.AN14	IO_L20P_T3_32	Bank32
J10.021	JB10.021	F1.AT12	IO_L12N_T1_MRCC_31	Bank31	J10.022	JB10.022	F1.AL14	IO_L24N_T3_32	Bank32
J10.023	JB10.023	F1.AR12	IO_L12P_T1_MRCC_31	Bank31	J10.024	JB10.024	F1.AL15	IO_L24P_T3_32	Bank32
J10.025	JB10.025	F1.AM11	IO_L1N_T0_31	Bank31	J10.026	JB10.026	F1.BB10	IO_L19N_T3_VREF_31	Bank31
J10.027	JB10.027	F1.AM12	IO_L1P_T0_31	Bank31	J10.028	JB10.028	F1.BA10	IO_L19P_T3_31	Bank31
J10.029	JB10.029	F1.AR10	IO_L7N_T1_31	Bank31	J10.030	JB10.030	F1.AK15	IO_L21N_T3_DQS_32	Bank32
J10.031	JB10.031	F1.AP10	IO_L7P_T1_31	Bank31	J10.032	JB10.032	F1.AK16	IO_L21P_T3_DQS_32	Bank32
J10.033	JB10.033	F1.AN11	IO_L9N_T1_DQS_31	Bank31	J10.034	JB10.034	F1.AU11	IO_L13N_T2_MRCC_31	Bank31
J10.035	JB10.035	F1.AN12	IO_L9P_T1_DQS_31	Bank31	J10.036	JB10.036	F1.AU12	IO_L13P_T2_MRCC_31	Bank31
J10.037	JB10.037	F1.AY10	IO_L17N_T2_31	Bank31	J10.038	JB10.038	F1.AN16	IO_L17N_T2_32	Bank32
J10.039	JB10.039	F1.AW10	IO_L17P_T2_31	Bank31	J10.040	JB10.040	F1.AN17	IO_L17P_T2_32	Bank32
J10.041	JB10.041	F1.AY11	IO_L16N_T2_31	Bank31	J10.042	JB10.042	F1.AV11	IO_L14N_T2_SRCC_31	Bank31
J10.043	JB10.043	F1.AW11	IO_L16P_T2_31	Bank31	J10.044	JB10.044	F1.AV12	IO_L14P_T2_SRCC_31	Bank31
J10.045	JB10.045	F1.AR11	IO_L11N_T1_SRCC_31	Bank31	J10.046	JB10.046	F1.AW14	IO_L8N_T1_32	Bank32
J10.047	JB10.047	F1.AP11	IO_L11P_T1_SRCC_31	Bank31	J10.048	JB10.048	F1.AV14	IO_L8P_T1_32	Bank32
J10.049	JB10.049	F1.AP13	IO_L10N_T1_31	Bank31	J10.050	JB10.050	F1.AY13	IO_L18N_T2_31	Bank31
J10.051	JB10.051	F1.AN13	IO_L10P_T1_31	Bank31	J10.052	JB10.052	F1.AW13	IO_L18P_T2_31	Bank31
J10.053	JB10.053	F1.AM16	IO_L19N_T3_VREF_32	Bank32	J10.054	JB10.054	F1.BA12	IO_L21N_T3_DQS_31	Bank31
J10.055	JB10.055	F1.AM17	IO_L19P_T3_32	Bank32	J10.056	JB10.056	F1.AY12	IO_L21P_T3_DQS_31	Bank31
J10.057	JB10.057	F1.AU14	IO_L10N_T1_32	Bank32	J10.058	JB10.058	F1.BC12	IO_L23N_T3_31	Bank31
J10.059	JB10.059	F1.AT14	IO_L10P_T1_32	Bank32	J10.060	JB10.060	F1.BB12	IO_L23P_T3_31	Bank31
J10.061	JB10.061	F1.AU15	IO_L13N_T2_MRCC_32	Bank32	J10.062	JB10.062	F1.AY16	IO_L12N_T1_MRCC_32	Bank32
J10.063	JB10.063	F1.AT15	IO_L13P_T2_MRCC_32	Bank32	J10.064	JB10.064	F1.AW16	IO_L12P_T1_MRCC_32	Bank32
J10.065	JB10.065	F1.BB14	IO_L4N_T0_32	Bank32	J10.066	JB10.066	F1.BA13	IO_L6N_T0_VREF_32	Bank32
J10.067	JB10.067	F1.BB15	IO_L4P_T0_32	Bank32	J10.068	JB10.068	F1.BA14	IO_L6P_T0_32	Bank32
J10.069	JB10.069	F1.BD15	IO_L5N_T0_32	Bank32	J10.070	JB10.070	F1.AP15	IO_L15N_T2_DQS_32	Bank32
J10.071	JB10.071	F1.BD16	IO_L5P_T0_32	Bank32	J10.072	JB10.072	F1.AP16	IO_L15P_T2_DQS_32	Bank32
J10.073	JB10.073	F1.BC16	IO_L3N_T0_DQS_32	Bank32	J10.074	JB10.074	F1.AT17	IO_L16N_T2_32	Bank32
J10.075	JB10.075	F1.BC17	IO_L3P_T0_DQS_32	Bank32	J10.076	JB10.076	F1.AR17	IO_L16P_T2_32	Bank32
J10.077	JB10.077	F1.BB16	IO_L1N_T0_32	Bank32	J10.078	JB10.078	F1.BA17	IO_L7N_T1_32	Bank32
J10.079	JB10.079	F1.BB17	IO_L1P_T0_32	Bank32	J10.080	JB10.080	F1.AY17	IO_L7P_T1_32	Bank32
J10.081	JB10.081	F1.BA15	IO_L9N_T1_DQS_32	Bank32	J10.082	JB10.082	F1.AL17	IO_L21N_T3_DQS_33	Bank33
J10.083	JB10.083	F1.AY15	IO_L9P_T1_DQS_32	Bank32	J10.084	JB10.084	F1.AK17	IO_L21P_T3_DQS_33	Bank33
J10.085	JB10.085	F1.AW15	IO_L11N_T1_SRCC_32	Bank32	J10.086	JB10.086	F1.AR21	IO_L15N_T2_DQS_33	Bank33
J10.087	JB10.087	F1.AV16	IO_L11P_T1_SRCC_32	Bank32	J10.088	JB10.088	F1.AP21	IO_L15P_T2_DQS_33	Bank33
J10.089	JB10.089	F1.AM14	IO_L22N_T3_32	Bank32	J10.090	JB10.090	F1.AP19	IO_L17N_T2_33	Bank33
J10.091	JB10.091	F1.AM15	IO_L22P_T3_32	Bank32	J10.092	JB10.092	F1.AP20	IO_L17P_T2_33	Bank33
J10.093	JB10.093	F1.AL18	IO_L19N_T3_VREF_33	Bank33	J10.094	JB10.094	F1.AN19	IO_L20N_T3_33	Bank33
J10.095	JB10.095	F1.AK18	IO_L19P_T3_33	Bank33	J10.096	JB10.096	F1.AM20	IO_L20P_T3_33	Bank33
J10.097	JB10.097	F1.AT20	IO_L13N_T2_MRCC_33	Bank33	J10.098	JB10.098	F1.AM19	IO_L24N_T3_33	Bank33
J10.099	JB10.099	F1.AR20	IO_L13P_T2_MRCC_33	Bank33	J10.100	JB10.100	F1.AL19	IO_L24P_T3_33	Bank33
J10.101	JB10.101	F1.AU20	IO_L14N_T2_SRCC_33	Bank33	J10.102	JB10.102	F1.AL20	IO_L22N_T3_33	Bank33

J10 (Odd Pins)					J10 (Even Pins)				
Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank	Top Con	Bottom Con	FPGA Pin No.	FPGA Pin Description	FPGA Bank
J10.103	JB10.103	F1.AU21	IO_L14P_T2_SRCC_33	Bank33	J10.104	JB10.104	F1.AK20	IO_L22P_T3_33	Bank33
J10.105	JB10.105	F1.AR15	IO_L18N_T2_32	Bank32	J10.106	JB10.106	F1.AJ19	IO_L23N_T3_33	Bank33
J10.107	JB10.107	F1.AR16	IO_L18P_T2_32	Bank32	J10.108	JB10.108	F1.AJ20	IO_L23P_T3_33	Bank33
J10.109	JB10.109	F1.AU16	IO_L14N_T2_SRCC_32	Bank32	J10.110	JB10.110	F1.BC11	IO_L20N_T3_31	Bank31
J10.111	JB10.111	F1.AU17	IO_L14P_T2_SRCC_32	Bank32	J10.112	JB10.112	F1.BB11	IO_L20P_T3_31	Bank31
J10.113	JB10.113	F1.AP18	IO_L16N_T2_33	Bank33	J10.114	JB10.114	F1.BD13	IO_L24N_T3_31	Bank31
J10.115	JB10.115	F1.AN18	IO_L16P_T2_33	Bank33	J10.116	JB10.116	F1.BC13	IO_L24P_T3_31	Bank31
J10.117	JB10.117	F1.AT18	IO_L18N_T2_33	Bank33	J10.118	JB10.118	F1.BD14	IO_L2N_T0_32	Bank32
J10.119	JB10.119	F1.AR18	IO_L18P_T2_33	Bank33	J10.120	JB10.120	F1.BC14	IO_L2P_T0_32	Bank32

8.4 Shared I/O

Shared I/O connectors are those labeled J2, J6, J7 and J12, which are linked to the I/O pins of both FPGA F1 and F2. Any shared I/O could be used as I/O for one FPGA, take care in assigning connections to avoid I/O conflicts. The shared I/O voltages are fixed to1.8V. The shared I/O connector properties are listed below:

Table 8-4 **Shared I/O Connector Properties**

J2 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J2.001	JB2.001	F1.A18	IO_L7N_T1_40	Bank40	F2.E8	IO_L1N_T0_39	Bank39
J2.003	JB2.003	F1.A19	IO_L7P_T1_40	Bank40	F2.F8	IO_L1P_T0_39	Bank39
J2.005	JB2.005	F1.B19	IO_L9N_T1_DQS_40	Bank40	F2.E7	IO_L3N_T0_DQS_39	Bank39
J2.007	JB2.007	F1.C19	IO_L9P_T1_DQS_40	Bank40	F2.F7	IO_L3P_T0_DQS_39	Bank39
J2.009	JB2.009	F1.C18	IO_L11N_T1_SRCC_40	Bank40	F2.F5	IO_L5N_T0_39	Bank39
J2.011	JB2.011	F1.D18	IO_L11P_T1_SRCC_40	Bank40	F2.G5	IO_L5P_T0_39	Bank39
J2.013	JB2.013	F1.M16	IO_L21N_T3_DQS_41	Bank41	F2.C4	IO_L14N_T2_SRCC_39	Bank39
J2.015	JB2.015	F1.N16	IO_L21P_T3_DQS_41	Bank41	F2.D4	IO_L14P_T2_SRCC_39	Bank39
J2.017	JB2.017	F1.G17	IO_L6N_T0_VREF_41	Bank41	F2.E3	IO_L21N_T3_DQS_39	Bank39
J2.019	JB2.019	F1.H17	IO_L6P_T0_41	Bank41	F2.F3	IO_L21P_T3_DQS_39	Bank39
J2.021	JB2.021	F1.E15	IO_L13N_T2_MRCC_41	Bank41	F2.B2	IO_L15N_T2_DQS_39	Bank39
J2.023	JB2.023	F1.F15	IO_L13P_T2_MRCC_41	Bank41	F2.C2	IO_L15P_T2_DQS_39	Bank39
J2.025	JB2.025	F1.E17	IO_L15N_T2_DQS_41	Bank41	F2.C1	IO_L17N_T2_39	Bank39
J2.027	JB2.027	F1.F17	IO_L15P_T2_DQS_41	Bank41	F2.D1	IO_L17P_T2_39	Bank39
J2.029	JB2.029	F1.D16	IO_L14N_T2_SRCC_41	Bank41	F2.E1	IO_L23N_T3_39	Bank39
J2.031	JB2.031	F1.E16	IO_L14P_T2_SRCC_41	Bank41	F2.E2	IO_L23P_T3_39	Bank39
J2.033	JB2.033	F1.C13	IO_L11N_T1_SRCC_41	Bank41	F2.H2	IO_L20N_T3_39	Bank39
J2.035	JB2.035	F1.C14	IO_L11P_T1_SRCC_41	Bank41	F2.H3	IO_L20P_T3_39	Bank39
J2.037	JB2.037	F1.A17	IO_L17N_T2_41	Bank41	F2.F2	IO_L22N_T3_39	Bank39
J2.039	JB2.039	F1.B17	IO_L17P_T2_41	Bank41	F2.G2	IO_L22P_T3_39	Bank39
J2.041	JB2.041	F1.C16	IO_L18N_T2_41	Bank41	F2.G1	IO_L24N_T3_39	Bank39
J2.043	JB2.043	F1.C17	IO_L18P_T2_41	Bank41	F2.H1	IO_L24P_T3_39	Bank39
J2.045	JB2.045	F1.B15	IO_L16N_T2_41	Bank41	F2.H6	IO_L6N_T0_VREF_39	Bank39
J2.047	JB2.047	F1.B16	IO_L16P_T2_41	Bank41	F2.J6	IO_L6P_T0_39	Bank39
J2.049	JB2.049	F1.G14	IO_L4N_T0_41	Bank41	F2.K6	IO_L2N_T0_38	Bank38

J2 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J2.051	JB2.051	F1.G15	IO_L4P_T0_41	Bank41	F2.K7	IO_L2P_T0_38	Bank38
J2.053	JB2.053	F1.H14	IO_L2N_T0_41	Bank41	F2.K5	IO_L4N_T0_38	Bank38
J2.055	JB2.055	F1.J14	IO_L2P_T0_41	Bank41	F2.L5	IO_L4P_T0_38	Bank38
J2.057	JB2.057	F1.E12	IO_L15N_T2_DQS_42	Bank42	F2.J4	IO_L8N_T1_38	Bank38
J2.059	JB2.059	F1.F12	IO_L15P_T2_DQS_42	Bank42	F2.J5	IO_L8P_T1_38	Bank38
J2.061	JB2.061	F1.A12	IO_L8N_T1_42	Bank42	F2.M4	IO_L11N_T1_SRCC_38	Bank38
J2.063	JB2.063	F1.B12	IO_L8P_T1_42	Bank42	F2.M5	IO_L11P_T1_SRCC_38	Bank38
J2.065	JB2.065	F1.B10	IO_L9N_T1_DQS_42	Bank42	F2.L7	IO_L6N_T0_VREF_38	Bank38
J2.067	JB2.067	F1.B11	IO_L9P_T1_DQS_42	Bank42	F2.L8	IO_L6P_T0_38	Bank38
J2.069	JB2.069	F1.A9	IO_L10N_T1_42	Bank42	F2.M1	IO_L15N_T2_DQS_38	Bank38
J2.071	JB2.071	F1.A10	IO_L10P_T1_42	Bank42	F2.M2	IO_L15P_T2_DQS_38	Bank38
J2.073	JB2.073	F1.A8	IO_L7N_T1_42	Bank42	F2.N1	IO_L17N_T2_38	Bank38
J2.075	JB2.075	F1.B9	IO_L7P_T1_42	Bank42	F2.N2	IO_L17P_T2_38	Bank38
J2.077	JB2.077	F1.C11	IO_L11N_T1_SRCC_42	Bank42	F2.P1	IO_L16N_T2_38	Bank38
J2.079	JB2.079	F1.C12	IO_L11P_T1_SRCC_42	Bank42	F2.R1	IO_L16P_T2_38	Bank38
J2.081	JB2.081	F1.D11	IO_L13N_T2_MRCC_42	Bank42	F2.N6	IO_L20N_T3_38	Bank38
J2.083	JB2.083	F1.E11	IO_L13P_T2_MRCC_42	Bank42	F2.P6	IO_L20P_T3_38	Bank38
J2.085	JB2.085	F1.G12	IO_L17N_T2_42	Bank42	F2.R2	IO_L18N_T2_38	Bank38
J2.087	JB2.087	F1.H12	IO_L17P_T2_42	Bank42	F2.R3	IO_L18P_T2_38	Bank38
J2.089	JB2.089	F1.D10	IO_L14N_T2_SRCC_42	Bank42	F2.P3	IO_L14N_T2_SRCC_38	Bank38
J2.091	JB2.091	F1.E10	IO_L14P_T2_SRCC_42	Bank42	F2.P4	IO_L14P_T2_SRCC_38	Bank38
J2.093	JB2.093	F1.J10	IO_L20N_T3_42	Bank42	F2.U6	IO_L1N_T0_37	Bank37
J2.095	JB2.095	F1.K10	IO_L20P_T3_42	Bank42	F2.U7	IO_L1P_T0_37	Bank37
J2.097	JB2.097	F1.F9	IO_L22N_T3_42	Bank42	F2.V7	IO_L3N_T0_DQS_37	Bank37
J2.099	JB2.099	F1.G9	IO_L22P_T3_42	Bank42	F2.V8	IO_L3P_T0_DQS_37	Bank37
J2.101	JB2.101	F1.H9	IO_L24N_T3_42	Bank42	F2.V9	IO_L5N_T0_37	Bank37
J2.103	JB2.103	F1.J9	IO_L24P_T3_42	Bank42	F2.V10	IO_L5P_T0_37	Bank37
J2.105	JB2.105	F1.B2	IO_L15N_T2_DQS_39	Bank39	F2.T4	IO_L8N_T1_37	Bank37
J2.107	JB2.107	F1.C2	IO_L15P_T2_DQS_39	Bank39	F2.T5	IO_L8P_T1_37	Bank37
J2.109	JB2.109	F1.A3	IO_L18N_T2_39	Bank39	F2.T2	IO_L10N_T1_37	Bank37
J2.111	JB2.111	F1.B4	IO_L18P_T2_39	Bank39	F2.T3	IO_L10P_T1_37	Bank37
J2.113	JB2.113	F1.C4	IO_L14N_T2_SRCC_39	Bank39	F2.U1	IO_L7N_T1_37	Bank37
J2.115	JB2.115	F1.D4	IO_L14P_T2_SRCC_39	Bank39	F2.U2	IO_L7P_T1_37	Bank37
J2.117	JB2.117	F1.A4	IO_L16N_T2_39	Bank39	F2.V1	IO_L9N_T1_DQS_37	Bank37
J2.119	JB2.119	F1.A5	IO_L16P_T2_39	Bank39	F2.V2	IO_L9P_T1_DQS_37	Bank37
J2.002	JB2.002	F1.A20	IO_L8N_T1_40	Bank40	F2.H7	IO_L2N_T0_39	Bank39
J2.004	JB2.004	F1.B20	IO_L8P_T1_40	Bank40	F2.H8	IO_L2P_T0_39	Bank39
J2.006	JB2.006	F1.B21	IO_L10N_T1_40	Bank40	F2.G6	IO_L4N_T0_39	Bank39
J2.008	JB2.008	F1.C21	IO_L10P_T1_40	Bank40	F2.G7	IO_L4P_T0_39	Bank39
J2.010	JB2.010	F1.A14	IO_L10N_T1_41	Bank41	F2.F4	IO_L19N_T3_VREF_39	Bank39
J2.012	JB2.012	F1.A15	IO_L10P_T1_41	Bank41	F2.G4	IO_L19P_T3_39	Bank39
J2.014	JB2.014	F1.A13	IO_L8N_T1_41	Bank41	F2.C8	IO_L8N_T1_39	Bank39
J2.016	JB2.016	F1.B14	IO_L8P_T1_41	Bank41	F2.D8	IO_L8P_T1_39	Bank39
J2.018	JB2.018	F1.D13	IO_L9N_T1_DQS_41	Bank41	F2.A7	IO_L10N_T1_39	Bank39
J2.020	JB2.020	F1.E13	IO_L9P_T1_DQS_41	Bank41	F2.B7	IO_L10P_T1_39	Bank39
J2.022	JB2.022	F1.F13	IO_L7N_T1_41	Bank41	F2.B5	IO_L9N_T1_DQS_39	Bank39
J2.024	JB2.024	F1.F14	IO_L7P_T1_41	Bank41	F2.B6	IO_L9P_T1_DQS_39	Bank39

J2 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J2.026	JB2.026	F1.L14	IO_L20N_T3_41	Bank41	F2.A4	IO_L16N_T2_39	Bank39
J2.028	JB2.028	F1.M15	IO_L20P_T3_41	Bank41	F2.A5	IO_L16P_T2_39	Bank39
J2.030	JB2.030	F1.R15	IO_L23N_T3_41	Bank41	F2.A3	IO_L18N_T2_39	Bank39
J2.032	JB2.032	F1.T15	IO_L23P_T3_41	Bank41	F2.B4	IO_L18P_T2_39	Bank39
J2.034	JB2.034	F1.P16	IO_L19N_T3_VREF_41	Bank41	F2.C6	IO_L7N_T1_39	Bank39
J2.036	JB2.036	F1.R16	IO_L19P_T3_41	Bank41	F2.C7	IO_L7P_T1_39	Bank39
J2.038	JB2.038	F1.P14	IO_L22N_T3_41	Bank41	F2.D6	IO_L12N_T1_MRCC_39	Bank39
J2.040	JB2.040	F1.P15	IO_L22P_T3_41	Bank41	F2.E6	IO_L12P_T1_MRCC_39	Bank39
J2.042	JB2.042	F1.M14	IO_L24N_T3_41	Bank41	F2.D5	IO_L11N_T1_SRCC_39	Bank39
J2.044	JB2.044	F1.N14	IO_L24P_T3_41	Bank41	F2.E5	IO_L11P_T1_SRCC_39	Bank39
J2.046	JB2.046	F1.J16	IO_L5N_T0_41	Bank41	F2.K8	IO_L1N_T0_38	Bank38
J2.048	JB2.048	F1.K16	IO_L5P_T0_41	Bank41	F2.L9	IO_L1P_T0_38	Bank38
J2.050	JB2.050	F1.G16	IO_L3N_T0_DQS_41	Bank41	F2.M6	IO_L3N_T0_DQS_38	Bank38
J2.052	JB2.052	F1.H16	IO_L3P_T0_DQS_41	Bank41	F2.M7	IO_L3P_T0_DQS_38	Bank38
J2.054	JB2.054	F1.J15	IO_L1N_T0_41	Bank41	F2.M9	IO_L5N_T0_38	Bank38
J2.056	JB2.056	F1.K15	IO_L1P_T0_41	Bank41	F2.M10	IO_L5P_T0_38	Bank38
J2.058	JB2.058	F1.F10	IO_L16N_T2_42	Bank42	F2.J3	IO_L10N_T1_38	Bank38
J2.060	JB2.060	F1.G10	IO_L16P_T2_42	Bank42	F2.K3	IO_L10P_T1_38	Bank38
J2.062	JB2.062	F1.G11	IO_L18N_T2_42	Bank42	F2.J1	IO_L9N_T1_DQS_38	Bank38
J2.064	JB2.064	F1.H11	IO_L18P_T2_42	Bank42	F2.K1	IO_L9P_T1_DQS_38	Bank38
J2.066	JB2.066	F1.H13	IO_L19N_T3_VREF_42	Bank42	F2.K2	IO_L7N_T1_38	Bank38
J2.068	JB2.068	F1.J13	IO_L19P_T3_42	Bank42	F2.L2	IO_L7P_T1_38	Bank38
J2.070	JB2.070	F1.R13	IO_L2N_T0_42	Bank42	F2.L3	IO_L12N_T1_MRCC_38	Bank38
J2.072	JB2.072	F1.T13	IO_L2P_T0_42	Bank42	F2.L4	IO_L12P_T1_MRCC_38	Bank38
J2.074	JB2.074	F1.R12	IO_L4N_T0_42	Bank42	F2.N7	IO_L21N_T3_DQS_38	Bank38
J2.076	JB2.076	F1.T12	IO_L4P_T0_42	Bank42	F2.P8	IO_L21P_T3_DQS_38	Bank38
J2.078	JB2.078	F1.P11	IO_L6N_T0_VREF_42	Bank42	F2.N8	IO_L19N_T3_VREF_38	Bank38
J2.080	JB2.080	F1.R11	IO_L6P_T0_42	Bank42	F2.N9	IO_L19P_T3_38	Bank38
J2.082	JB2.082	F1.N13	IO_L1N_T0_42	Bank42	F2.P5	IO_L22N_T3_38	Bank38
J2.084	JB2.084	F1.P13	IO_L1P_T0_42	Bank42	F2.R5	IO_L22P_T3_38	Bank38
J2.086	JB2.086	F1.M11	IO_L3N_T0_DQS_42	Bank42	F2.P9	IO_L23N_T3_38	Bank38
J2.088	JB2.088	F1.N11	IO_L3P_T0_DQS_42	Bank42	F2.P10	IO_L23P_T3_38	Bank38
J2.090	JB2.090	F1.M12	IO_L5N_T0_42	Bank42	F2.R6	IO_L24N_T3_38	Bank38
J2.092	JB2.092	F1.N12	IO_L5P_T0_42	Bank42	F2.R7	IO_L24P_T3_38	Bank38
J2.094	JB2.094	F1.K12	IO_L21N_T3_DQS_42	Bank42	F2.R8	IO_L2N_T0_37	Bank37
J2.096	JB2.096	F1.L12	IO_L21P_T3_DQS_42	Bank42	F2.T9	IO_L2P_T0_37	Bank37
J2.098	JB2.098	F1.J11	IO_L23N_T3_42	Bank42	F2.T7	IO_L4N_T0_37	Bank37
J2.100	JB2.100	F1.K11	IO_L23P_T3_42	Bank42	F2.T8	IO_L4P_T0_37	Bank37
J2.102	JB2.102	F1.C1	IO_L17N_T2_39	Bank39	F2.V3	IO_L11N_T1_SRCC_37	Bank37
J2.104	JB2.104	F1.D1	IO_L17P_T2_39	Bank39	F2.V4	IO_L11P_T1_SRCC_37	Bank37
J2.106	JB2.106	F1.C3	IO_L13N_T2_MRCC_39	Bank39	F2.Y2	IO_L15N_T2_DQS_37	Bank37
J2.108	JB2.108	F1.D3	IO_L13P_T2_MRCC_39	Bank39	F2.Y3	IO_L15P_T2_DQS_37	Bank37
J2.110	JB2.110	F1.E1	IO_L23N_T3_39	Bank39	F2.U4	IO_L12N_T1_MRCC_37	Bank37
J2.112	JB2.112	F1.E2	IO_L23P_T3_39	Bank39	F2.U5	IO_L12P_T1_MRCC_37	Bank37
J2.114	JB2.114	F1.F2	IO_L22N_T3_39	Bank39	F2.W5	IO_L14N_T2_SRCC_37	Bank37
J2.116	JB2.116	F1.G2	IO_L22P_T3_39	Bank39	F2.Y5	IO_L14P_T2_SRCC_37	Bank37
J2.118	JB2.118	F1.G1	IO_L24N_T3_39	Bank39	F2.U9	IO_L6N_T0_VREF_37	Bank37

J2 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J2.120	JB2.120	F1.H1	IO_L24P_T3_39	Bank39	F2.U10	IO_L6P_T0_37	Bank37

J6 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J6.001	JB6.001	F1.Y43	IO_L16N_T2_16	Bank16	F2.AC29	IO_L23N_T3_FWE_B_15	Bank15
J6.003	JB6.003	F1.Y42	IO_L16P_T2_16	Bank16	F2.AD29	IO_L23P_T3_FOE_B_15	Bank15
J6.005	JB6.005	F1.W44	IO_L18N_T2_16	Bank16	F2.AD31	IO_L24N_T3_RS0_15	Bank15
J6.007	JB6.007	F1.W43	IO_L18P_T2_16	Bank16	F2.AD30	IO_L24P_T3_RS1_15	Bank15
J6.009	JB6.009	F1.V44	IO_L17N_T2_16	Bank16	F2.AC32	IO_L20N_T3_A19_15	Bank15
J6.011	JB6.011	F1.V43	IO_L17P_T2_16	Bank16	F2.AC31	IO_L20P_T3_A20_15	Bank15
J6.013	JB6.013	F1.U42	IO_L15N_T2_DQS_16	Bank16	F2.AC37	IO_L9N_T1_DQS_AD3N_15	Bank15
J6.015	JB6.015	F1.U41	IO_L15P_T2_DQS_16	Bank16	F2.AC36	IO_L9P_T1_DQS_AD3P_15	Bank15
J6.017	JB6.017	F1.U40	IO_L9N_T1_DQS_16	Bank16	F2.AB30	IO_L19N_T3_A21_VREF_15	Bank15
J6.019	JB6.019	F1.U39	IO_L9P_T1_DQS_16	Bank16	F2.AB29	IO_L19P_T3_A22_15	Bank15
J6.021	JB6.021	F1.H19	IO_L5N_T0_40	Bank40	F2.AB36	IO_L4N_T0_15	Bank15
J6.023	JB6.023	F1.J19	IO_L5P_T0_40	Bank40	F2.AB35	IO_L4P_T0_15	Bank15
J6.025	JB6.025	F1.E18	IO_L18N_T2_40	Bank40	F2.AA34	IO_L2N_T0_AD8N_15	Bank15
J6.027	JB6.027	F1.F18	IO_L18P_T2_40	Bank40	F2.AB34	IO_L2P_T0_AD8P_15	Bank15
J6.029	JB6.029	F1.R42	IO_L14N_T2_SRCC_20	Bank20	F2.Y38	IO_L10N_T1_16	Bank16
J6.031	JB6.031	F1.T42	IO_L14P_T2_SRCC_20	Bank20	F2.Y37	IO_L10P_T1_16	Bank16
J6.033	JB6.033	F1.N44	IO_L17N_T2_20	Bank20	F2.V37	IO_L8N_T1_16	Bank16
J6.035	JB6.035	F1.P44	IO_L17P_T2_20	Bank20	F2.V36	IO_L8P_T1_16	Bank16
J6.037	JB6.037	F1.N43	IO_L15N_T2_DQS_20	Bank20	F2.W40	IO_L11N_T1_SRCC_16	Bank16
J6.039	JB6.039	F1.P43	IO_L15P_T2_DQS_20	Bank20	F2.Y40	IO_L11P_T1_SRCC_16	Bank16
J6.041	JB6.041	F1.N42	IO_L10N_T1_20	Bank20	F2.V29	IO_L24N_T3_16	Bank16
J6.043	JB6.043	F1.P41	IO_L10P_T1_20	Bank20	F2.W29	IO_L24P_T3_16	Bank16
J6.045	JB6.045	F1.M41	IO_L8N_T1_20	Bank20	F2.Y31	IO_L23N_T3_16	Bank16
J6.047	JB6.047	F1.N41	IO_L8P_T1_20	Bank20	F2.Y30	IO_L23P_T3_16	Bank16
J6.049	JB6.049	F1.R41	IO_L13N_T2_MRCC_20	Bank20	F2.W31	IO_L22N_T3_16	Bank16
J6.051	JB6.051	F1.R40	IO_L13P_T2_MRCC_20	Bank20	F2.W30	IO_L22P_T3_16	Bank16
J6.053	JB6.053	F1.M40	IO_L6N_T0_VREF_20	Bank20	F2.Y33	IO_L21N_T3_DQS_16	Bank16
J6.055	JB6.055	F1.M39	IO_L6P_T0_20	Bank20	F2.Y32	IO_L21P_T3_DQS_16	Bank16
J6.057	JB6.057	F1.N39	IO_L4N_T0_20	Bank20	F2.W34	IO_L3N_T0_DQS_16	Bank16
J6.059	JB6.059	F1.N38	IO_L4P_T0_20	Bank20	F2.W33	IO_L3P_T0_DQS_16	Bank16
J6.061	JB6.061	F1.T34	IO_L19N_T3_VREF_20	Bank20	F2.U42	IO_L15N_T2_DQS_16	Bank16
J6.063	JB6.063	F1.T33	IO_L19P_T3_20	Bank20	F2.U41	IO_L15P_T2_DQS_16	Bank16
J6.065	JB6.065	F1.P31	IO_L24N_T3_20	Bank20	F2.U40	IO_L9N_T1_DQS_16	Bank16
J6.067	JB6.067	F1.P30	IO_L24P_T3_20	Bank20	F2.U39	IO_L9P_T1_DQS_16	Bank16
J6.069	JB6.069	F1.R31	IO_L21N_T3_DQS_20	Bank20	F2.V39	IO_L7N_T1_16	Bank16
J6.071	JB6.071	F1.R30	IO_L21P_T3_DQS_20	Bank20	F2.V38	IO_L7P_T1_16	Bank16
J6.073	JB6.073	F1.T30	IO_L23N_T3_20	Bank20	F2.U37	IO_L4N_T0_16	Bank16
J6.075	JB6.075	F1.T29	IO_L23P_T3_20	Bank20	F2.U36	IO_L4P_T0_16	Bank16
J6.077	JB6.077	F1.G42	IO_L7N_T1_21	Bank21	F2.N33	IO_L4N_T0_19	Bank19
J6.079	JB6.079	F1.G41	IO_L7P_T1_21	Bank21	F2.N32	IO_L4P_T0_19	Bank19
J6.081	JB6.081	F1.H41	IO_L11N_T1_SRCC_21	Bank21	F2.L33	IO_L2N_T0_19	Bank19

J6 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J6.083	JB6.083	F1.J41	IO_L11P_T1_SRCC_21	Bank21	F2.L32	IO_L2P_T0_19	Bank19
J6.085	JB6.085	F1.G40	IO_L1N_T0_21	Bank21	F2.K33	IO_L23N_T3_19	Bank19
J6.087	JB6.087	F1.G39	IO_L1P_T0_21	Bank21	F2.K32	IO_L23P_T3_19	Bank19
J6.089	JB6.089	F1.H39	IO_L3N_T0_DQS_21	Bank21	F2.J30	IO_L21N_T3_DQS_19	Bank19
J6.091	JB6.091	F1.J39	IO_L3P_T0_DQS_21	Bank21	F2.K30	IO_L21P_T3_DQS_19	Bank19
J6.093	JB6.093	F1.H38	IO_L5N_T0_21	Bank21	F2.M29	IO_L3N_T0_DQS_19	Bank19
J6.095	JB6.095	F1.J38	IO_L5P_T0_21	Bank21	F2.N29	IO_L3P_T0_DQS_19	Bank19
J6.097	JB6.097	F1.G37	IO_L4N_T0_21	Bank21	F2.M31	IO_L1N_T0_19	Bank19
J6.099	JB6.099	F1.G36	IO_L4P_T0_21	Bank21	F2.M30	IO_L1P_T0_19	Bank19
J6.101	JB6.101	F1.H37	IO_L6N_T0_VREF_21	Bank21	F2.M32	IO_L6N_T0_VREF_19	Bank19
J6.103	JB6.103	F1.H36	IO_L6P_T0_21	Bank21	F2.N31	IO_L6P_T0_19	Bank19
J6.105	JB6.105	F1.G35	IO_L2N_T0_21	Bank21	F2.L30	IO_L5N_T0_19	Bank19
J6.107	JB6.107	F1.G34	IO_L2P_T0_21	Bank21	F2.L29	IO_L5P_T0_19	Bank19
J6.109	JB6.109	F1.J35	IO_L22N_T3_21	Bank21	F2.J31	IO_L22N_T3_19	Bank19
J6.111	JB6.111	F1.J34	IO_L22P_T3_21	Bank21	F2.K31	IO_L22P_T3_19	Bank19
J6.113	JB6.113	F1.J36	IO_L19N_T3_VREF_21	Bank21	F2.H32	IO_L19N_T3_VREF_19	Bank19
J6.115	JB6.115	F1.K36	IO_L19P_T3_21	Bank21	F2.H31	IO_L19P_T3_19	Bank19
J6.117	JB6.117	F1.K37	IO_L20N_T3_21	Bank21	F2.H33	IO_L20N_T3_19	Bank19
J6.119	JB6.119	F1.L37	IO_L20P_T3_21	Bank21	F2.J33	IO_L20P_T3_19	Bank19
J6.002	JB6.002	F1.Y38	IO_L10N_T1_16	Bank16	F2.AB32	IO_L22N_T3_A16_15	Bank15
J6.004	JB6.004	F1.Y37	IO_L10P_T1_16	Bank16	F2.AB31	IO_L22P_T3_A17_15	Bank15
J6.006	JB6.006	F1.W40	IO_L11N_T1_SRCC_16	Bank16	F2.AA37	IO_L8N_T1_AD10N_15	Bank15
J6.008	JB6.008	F1.Y40	IO_L11P_T1_SRCC_16	Bank16	F2.AB37	IO_L8P_T1_AD10P_15	Bank15
J6.010	JB6.010	F1.W41	IO_L14N_T2_SRCC_16	Bank16	F2.AA33	IO_L6N_T0_VREF_15	Bank15
J6.012	JB6.012	F1.Y41	IO_L14P_T2_SRCC_16	Bank16	F2.AA32	IO_L6P_T0_15	Bank15
J6.014	JB6.014	F1.V42	IO_L13N_T2_MRCC_16	Bank16	F2.AA30	IO_L21N_T3_DQS_A18_15	Bank15
J6.016	JB6.016	F1.V41	IO_L13P_T2_MRCC_16	Bank16	F2.AA29	IO_L21P_T3_DQS_15	Bank15
J6.018	JB6.018	F1.J20	IO_L16N_T2_40	Bank40	F2.AD36	IO_L5N_T0_AD9N_15	Bank15
J6.020	JB6.020	F1.K20	IO_L16P_T2_40	Bank40	F2.AD35	IO_L5P_T0_AD9P_15	Bank15
J6.022	JB6.022	F1.G20	IO_L17N_T2_40	Bank40	F2.AD34	IO_L3N_T0_DQS_AD1N_15	Bank15
J6.024	JB6.024	F1.G21	IO_L17P_T2_40	Bank40	F2.AD33	IO_L3P_T0_DQS_AD1P_15	Bank15
J6.026	JB6.026	F1.D21	IO_L15N_T2_DQS_40	Bank40	F2.AC34	IO_L1N_T0_AD0N_15	Bank15
J6.028	JB6.028	F1.E21	IO_L15P_T2_DQS_40	Bank40	F2.AC33	IO_L1P_T0_AD0P_15	Bank15
J6.030	JB6.030	F1.R37	IO_L5N_T0_20	Bank20	F2.W41	IO_L14N_T2_SRCC_16	Bank16
J6.032	JB6.032	F1.R36	IO_L5P_T0_20	Bank20	F2.Y41	IO_L14P_T2_SRCC_16	Bank16
J6.034	JB6.034	F1.T40	IO_L7N_T1_20	Bank20	F2.Y43	IO_L16N_T2_16	Bank16
J6.036	JB6.036	F1.T39	IO_L7P_T1_20	Bank20	F2.Y42	IO_L16P_T2_16	Bank16
J6.038	JB6.038	F1.P40	IO_L11N_T1_SRCC_20	Bank20	F2.Y36	IO_L5N_T0_16	Bank16
J6.040	JB6.040	F1.P39	IO_L11P_T1_SRCC_20	Bank20	F2.Y35	IO_L5P_T0_16	Bank16
J6.042	JB6.042	F1.T44	IO_L18N_T2_20	Bank20	F2.W36	IO_L6N_T0_VREF_16	Bank16
J6.044	JB6.044	F1.U44	IO_L18P_T2_20	Bank20	F2.W35	IO_L6P_T0_16	Bank16
J6.046	JB6.046	F1.R43	IO_L16N_T2_20	Bank20	F2.V32	IO_L19N_T3_VREF_16	Bank16
J6.048	JB6.048	F1.T43	IO_L16P_T2_20	Bank20	F2.V31	IO_L19P_T3_16	Bank16
J6.050	JB6.050	F1.T38	IO_L9N_T1_DQS_20	Bank20	F2.V34	IO_L1N_T0_16	Bank16
J6.052	JB6.052	F1.T37	IO_L9P_T1_DQS_20	Bank20	F2.V33	IO_L1P_T0_16	Bank16
J6.054	JB6.054	F1.N37	IO_L2N_T0_20	Bank20	F2.U35	IO_L2N_T0_16	Bank16
J6.056	JB6.056	F1.N36	IO_L2P_T0_20	Bank20	F2.U34	IO_L2P_T0_16	Bank16

J6 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J6.058	JB6.058	F1.P36	IO_L1N_T0_20	Bank20	F2.U31	IO_L20N_T3_16	Bank16
J6.060	JB6.060	F1.P35	IO_L1P_T0_20	Bank20	F2.U30	IO_L20P_T3_16	Bank16
J6.062	JB6.062	F1.R35	IO_L3N_T0_DQS_20	Bank20	F2.W44	IO_L18N_T2_16	Bank16
J6.064	JB6.064	F1.T35	IO_L3P_T0_DQS_20	Bank20	F2.W43	IO_L18P_T2_16	Bank16
J6.066	JB6.066	F1.P34	IO_L20N_T3_20	Bank20	F2.V42	IO_L13N_T2_MRCC_16	Bank16
J6.068	JB6.068	F1.P33	IO_L20P_T3_20	Bank20	F2.V41	IO_L13P_T2_MRCC_16	Bank16
J6.070	JB6.070	F1.R33	IO_L22N_T3_20	Bank20	F2.V44	IO_L17N_T2_16	Bank16
J6.072	JB6.072	F1.R32	IO_L22P_T3_20	Bank20	F2.V43	IO_L17P_T2_16	Bank16
J6.074	JB6.074	F1.M37	IO_L21N_T3_DQS_21	Bank21	F2.E30	IO_L14N_T2_SRCC_19	Bank19
J6.076	JB6.076	F1.M36	IO_L21P_T3_DQS_21	Bank21	F2.F30	IO_L14P_T2_SRCC_19	Bank19
J6.078	JB6.078	F1.L40	IO_L8N_T1_21	Bank21	F2.E32	IO_L11N_T1_SRCC_19	Bank19
J6.080	JB6.080	F1.L39	IO_L8P_T1_21	Bank21	F2.F32	IO_L11P_T1_SRCC_19	Bank19
J6.082	JB6.082	F1.L42	IO_L13N_T2_MRCC_21	Bank21	F2.B29	IO_L18N_T2_19	Bank19
J6.084	JB6.084	F1.M42	IO_L13P_T2_MRCC_21	Bank21	F2.C29	IO_L18P_T2_19	Bank19
J6.086	JB6.086	F1.L44	IO_L17N_T2_21	Bank21	F2.C31	IO_L13N_T2_MRCC_19	Bank19
J6.088	JB6.088	F1.M44	IO_L17P_T2_21	Bank21	F2.D30	IO_L13P_T2_MRCC_19	Bank19
J6.090	JB6.090	F1.K43	IO_L15N_T2_DQS_21	Bank21	F2.B32	IO_L9N_T1_DQS_19	Bank19
J6.092	JB6.092	F1.L43	IO_L15P_T2_DQS_21	Bank21	F2.C32	IO_L9P_T1_DQS_19	Bank19
J6.094	JB6.094	F1.K42	IO_L14N_T2_SRCC_21	Bank21	F2.A33	IO_L15N_T2_DQS_19	Bank19
J6.096	JB6.096	F1.K41	IO_L14P_T2_SRCC_21	Bank21	F2.A32	IO_L15P_T2_DQS_19	Bank19
J6.098	JB6.098	F1.G44	IO_L16N_T2_21	Bank21	F2.G30	IO_L24N_T3_19	Bank19
J6.100	JB6.100	F1.H44	IO_L16P_T2_21	Bank21	F2.H29	IO_L24P_T3_19	Bank19
J6.102	JB6.102	F1.J44	IO_L18N_T2_21	Bank21	F2.G32	IO_L8N_T1_19	Bank19
J6.104	JB6.104	F1.J43	IO_L18P_T2_21	Bank21	F2.G31	IO_L8P_T1_19	Bank19
J6.106	JB6.106	F1.H43	IO_L9N_T1_DQS_21	Bank21	F2.E33	IO_L10N_T1_19	Bank19
J6.108	JB6.108	F1.H42	IO_L9P_T1_DQS_21	Bank21	F2.F33	IO_L10P_T1_19	Bank19
J6.110	JB6.110	F1.L35	IO_L23N_T3_21	Bank21	F2.C33	IO_L7N_T1_19	Bank19
J6.112	JB6.112	F1.L34	IO_L23P_T3_21	Bank21	F2.D33	IO_L7P_T1_19	Bank19
J6.114	JB6.114	F1.M35	IO_L24N_T3_21	Bank21	F2.B31	IO_L16N_T2_19	Bank19
J6.116	JB6.116	F1.M34	IO_L24P_T3_21	Bank21	F2.B30	IO_L16P_T2_19	Bank19
J6.118	JB6.118	F1.K38	IO_L10N_T1_21	Bank21	F2.A30	IO_L17N_T2_19	Bank19
J6.120	JB6.120	F1.L38	IO_L10P_T1_21	Bank21	F2.A29	IO_L17P_T2_19	Bank19

J7 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J7.001	JB7.001	F1.BD33	IO_L1N_T0_36	Bank36	F2.BB19	IO_L6N_T0_VREF_33	Bank33
J7.003	JB7.003	F1.BC33	IO_L1P_T0_36	Bank36	F2.BA19	IO_L6P_T0_33	Bank33
J7.005	JB7.005	F1.BB32	IO_L3N_T0_DQS_36	Bank36	F2.BA18	IO_L8N_T1_33	Bank33
J7.007	JB7.007	F1.BB31	IO_L3P_T0_DQS_36	Bank36	F2.AY18	IO_L8P_T1_33	Bank33
J7.009	JB7.009	F1.BA33	IO_L5N_T0_36	Bank36	F2.AW18	IO_L10N_T1_33	Bank33
J7.011	JB7.011	F1.BA32	IO_L5P_T0_36	Bank36	F2.AW19	IO_L10P_T1_33	Bank33
J7.013	JB7.013	F1.AY33	IO_L7N_T1_36	Bank36	F2.AP36	IO_L6N_T0_VREF_12	Bank12
J7.015	JB7.015	F1.AW33	IO_L7P_T1_36	Bank36	F2.AN36	IO_L6P_T0_12	Bank12
J7.017	JB7.017	F1.AY32	IO_L9N_T1_DQS_36	Bank36	F2.AV34	IO_L22N_T3_12	Bank12
J7.019	JB7.019	F1.AY31	IO_L9P_T1_DQS_36	Bank36	F2.AU34	IO_L22P_T3_12	Bank12

J7 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J7.021	JB7.021	F1.AV32	IO_L11N_T1_SRCC_36	Bank36	F2.AU35	IO_L20N_T3_12	Bank12
J7.023	JB7.023	F1.AU32	IO_L11P_T1_SRCC_36	Bank36	F2.AT35	IO_L20P_T3_12	Bank12
J7.025	JB7.025	F1.AT32	IO_L14N_T2_SRCC_36	Bank36	F2.AU37	IO_L21N_T3_DQS_12	Bank12
J7.027	JB7.027	F1.AR32	IO_L14P_T2_SRCC_36	Bank36	F2.AU36	IO_L21P_T3_DQS_12	Bank12
J7.029	JB7.029	F1.AT30	IO_L18N_T2_36	Bank36	F2.AT38	IO_L19N_T3_VREF_12	Bank12
J7.031	JB7.031	F1.AR30	IO_L18P_T2_36	Bank36	F2.AT37	IO_L19P_T3_12	Bank12
J7.033	JB7.033	F1.AP33	IO_L16N_T2_36	Bank36	F2.AR41	IO_L11N_T1_SRCC_12	Bank12
J7.035	JB7.035	F1.AN33	IO_L16P_T2_36	Bank36	F2.AR40	IO_L11P_T1_SRCC_12	Bank12
J7.037	JB7.037	F1.AN32	IO_L20N_T3_36	Bank36	F2.AT40	IO_L14N_T2_SRCC_12	Bank12
J7.039	JB7.039	F1.AN31	IO_L20P_T3_36	Bank36	F2.AT39	IO_L14P_T2_SRCC_12	Bank12
J7.041	JB7.041	F1.AM31	IO_L22N_T3_36	Bank36	F2.AV41	IO_L15N_T2_DQS_12	Bank12
J7.043	JB7.043	F1.AM30	IO_L22P_T3_36	Bank36	F2.AU41	IO_L15P_T2_DQS_12	Bank12
J7.045	JB7.045	F1.AN29	IO_L24N_T3_36	Bank36	F2.AT42	IO_L12N_T1_MRCC_12	Bank12
J7.047	JB7.047	F1.AM29	IO_L24P_T3_36	Bank36	F2.AR42	IO_L12P_T1_MRCC_12	Bank12
J7.049	JB7.049	F1.AC29	IO_L23N_T3_FWE_B_15	Bank15	F2.AP39	IO_L4N_T0_12	Bank12
J7.051	JB7.051	F1.AD29	IO_L23P_T3_FOE_B_15	Bank15	F2.AP38	IO_L4P_T0_12	Bank12
J7.053	JB7.053	F1.AA30	IO_L21N_T3_A18_15	Bank15	F2.AN38	IO_L2N_T0_12	Bank12
J7.055	JB7.055	F1.AA29	IO_L21P_T3_15	Bank15	F2.AN37	IO_L2P_T0_12	Bank12
J7.057	JB7.057	F1.AB30	IO_L19N_T3_A21_15	Bank15	F2.AJ36	IO_L7N_T1_13	Bank13
J7.059	JB7.059	F1.AB29	IO_L19P_T3_A22_15	Bank15	F2.AH36	IO_L7P_T1_13	Bank13
J7.061	JB7.061	F1.AA40	IO_L14N_T2_SRCC_15	Bank15	F2.AJ34	IO_L19N_T3_VREF_13	Bank13
J7.063	JB7.063	F1.AB40	IO_L14P_T2_SRCC_15	Bank15	F2.AJ33	IO_L19P_T3_13	Bank13
J7.065	JB7.065	F1.AA43	IO_L16N_T2_A27_15	Bank15	F2.AL33	IO_L21N_T3_DQS_13	Bank13
J7.067	JB7.067	F1.AA42	IO_L16P_T2_A28_15	Bank15	F2.AK33	IO_L21P_T3_DQS_13	Bank13
J7.069	JB7.069	F1.AB39	IO_L11N_T1_SRCC_15	Bank15	F2.AM34	IO_L22N_T3_13	Bank13
J7.071	JB7.071	F1.AC39	IO_L11P_T1_SRCC_15	Bank15	F2.AL34	IO_L22P_T3_13	Bank13
J7.073	JB7.073	F1.AC37	IO_L9N_T1_AD3N_15	Bank15	F2.AK35	IO_L20N_T3_13	Bank13
J7.075	JB7.075	F1.AC36	IO_L9P_T1_AD3P_15	Bank15	F2.AJ35	IO_L20P_T3_13	Bank13
J7.077	JB7.077	F1.AA37	IO_L8N_T1_AD10N_15	Bank15	F2.AM35	IO_L24N_T3_13	Bank13
J7.079	JB7.079	F1.AB37	IO_L8P_T1_AD10P_15	Bank15	F2.AL35	IO_L24P_T3_13	Bank13
J7.081	JB7.081	F1.AB36	IO_L4N_T0_15	Bank15	F2.AM37	IO_L9N_T1_DQS_13	Bank13
J7.083	JB7.083	F1.AB35	IO_L4P_T0_15	Bank15	F2.AM36	IO_L9P_T1_DQS_13	Bank13
J7.085	JB7.085	F1.AA34	IO_L2N_T0_AD8N_15	Bank15	F2.AL38	IO_L11N_T1_SRCC_13	Bank13
J7.087	JB7.087	F1.AB34	IO_L2P_T0_AD8P_15	Bank15	F2.AL37	IO_L11P_T1_SRCC_13	Bank13
J7.089	JB7.089	F1.AA33	IO_L6N_T0_VREF_15	Bank15	F2.AM39	IO_L14N_T2_SRCC_13	Bank13
J7.091	JB7.091	F1.AA32	IO_L6P_T0_15	Bank15	F2.AL39	IO_L14P_T2_SRCC_13	Bank13
J7.093	JB7.093	F1.V29	IO_L24N_T3_16	Bank16	F2.AL40	IO_L5N_T0_13	Bank13
J7.095	JB7.095	F1.W29	IO_L24P_T3_16	Bank16	F2.AK40	IO_L5P_T0_13	Bank13
J7.097	JB7.097	F1.W31	IO_L22N_T3_16	Bank16	F2.AK43	IO_L3N_T0_DQS_13	Bank13
J7.099	JB7.099	F1.W30	IO_L22P_T3_16	Bank16	F2.AK42	IO_L3P_T0_DQS_13	Bank13
J7.101	JB7.101	F1.U31	IO_L20N_T3_16	Bank16	F2.AK41	IO_L1N_T0_13	Bank13
J7.103	JB7.103	F1.U30	IO_L20P_T3_16	Bank16	F2.AJ41	IO_L1P_T0_13	Bank13
J7.105	JB7.105	F1.V39	IO_L7N_T1_16	Bank16	F2.AC38	IO_L10N_T1_AD11N_15	Bank15
J7.107	JB7.107	F1.V38	IO_L7P_T1_16	Bank16	F2.AD38	IO_L10P_T1_AD11P_15	Bank15
J7.109	JB7.109	F1.V37	IO_L8N_T1_16	Bank16	F2.AD40	IO_L7N_T1_AD2N_15	Bank15
J7.111	JB7.111	F1.V36	IO_L8P_T1_16	Bank16	F2.AD39	IO_L7P_T1_AD2P_15	Bank15
J7.113	JB7.113	F1.U37	IO_L4N_T0_16	Bank16	F2.AB41	IO_L13N_T2_MRCC_15	Bank15

J7 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J7.115	JB7.115	F1.U36	IO_L4P_T0_16	Bank16	F2.AC41	IO_L13P_T2_MRCC_15	Bank15
J7.117	JB7.117	F1.U35	IO_L2N_T0_16	Bank16	F2.AC44	IO_L17N_T2_A25_15	Bank15
J7.119	JB7.119	F1.U34	IO_L2P_T0_16	Bank16	F2.AC43	IO_L17P_T2_A26_15	Bank15
J7.002	JB7.002	F1.BC32	IO_L2N_T0_36	Bank36	F2.AY21	IO_L7N_T1_33	Bank33
J7.004	JB7.004	F1.BC31	IO_L2P_T0_36	Bank36	F2.AW21	IO_L7P_T1_33	Bank33
J7.006	JB7.006	F1.BD31	IO_L4N_T0_36	Bank36	F2.AY20	IO_L9N_T1_DQS_33	Bank33
J7.008	JB7.008	F1.BD30	IO_L4P_T0_36	Bank36	F2.AW20	IO_L9P_T1_DQS_33	Bank33
J7.010	JB7.010	F1.BB30	IO_L6N_T0_VREF_36	Bank36	F2.AV37	IO_L24N_T3_12	Bank12
J7.012	JB7.012	F1.BA30	IO_L6P_T0_36	Bank36	F2.AV36	IO_L24P_T3_12	Bank12
J7.014	JB7.014	F1.AY30	IO_L8N_T1_36	Bank36	F2.AV44	IO_L18N_T2_12	Bank12
J7.016	JB7.016	F1.AW30	IO_L8P_T1_36	Bank36	F2.AV43	IO_L18P_T2_12	Bank12
J7.018	JB7.018	F1.AW31	IO_L10N_T1_36	Bank36	F2.AV42	IO_L17N_T2_12	Bank12
J7.020	JB7.020	F1.AV31	IO_L10P_T1_36	Bank36	F2.AU42	IO_L17P_T2_12	Bank12
J7.022	JB7.022	F1.AU31	IO_L12N_T1_MRCC_36	Bank36	F2.AU44	IO_L16N_T2_12	Bank12
J7.024	JB7.024	F1.AU30	IO_L12P_T1_MRCC_36	Bank36	F2.AT44	IO_L16P_T2_12	Bank12
J7.026	JB7.026	F1.AT33	IO_L15N_T2_DQS_36	Bank36	F2.AT43	IO_L10N_T1_12	Bank12
J7.028	JB7.028	F1.AR33	IO_L15P_T2_DQS_36	Bank36	F2.AR43	IO_L10P_T1_12	Bank12
J7.030	JB7.030	F1.AK31	IO_L21N_T3_DQS_36	Bank36	F2.AP44	IO_L8N_T1_12	Bank12
J7.032	JB7.032	F1.AK30	IO_L21P_T3_DQS_36	Bank36	F2.AP43	IO_L8P_T1_12	Bank12
J7.034	JB7.034	F1.AM32	IO_L19N_T3_VREF_36	Bank36	F2.AV39	IO_L23N_T3_12	Bank12
J7.036	JB7.036	F1.AL32	IO_L19P_T3_36	Bank36	F2.AV38	IO_L23P_T3_12	Bank12
J7.038	JB7.038	F1.AP30	IO_L17N_T2_36	Bank36	F2.AP40	IO_L7N_T1_12	Bank12
J7.040	JB7.040	F1.AP29	IO_L17P_T2_36	Bank36	F2.AN39	IO_L7P_T1_12	Bank12
J7.042	JB7.042	F1.AL30	IO_L23N_T3_36	Bank36	F2.AP41	IO_L9N_T1_DQS_12	Bank12
J7.044	JB7.044	F1.AL29	IO_L23P_T3_36	Bank36	F2.AN41	IO_L9P_T1_DQS_12	Bank12
J7.046	JB7.046	F1.AD31	IO_L24N_T3_RS0_15	Bank15	F2.AR36	IO_L5N_T0_12	Bank12
J7.048	JB7.048	F1.AD30	IO_L24P_T3_RS1_15	Bank15	F2.AR35	IO_L5P_T0_12	Bank12
J7.050	JB7.050	F1.AB32	IO_L22N_T3_A16_15	Bank15	F2.AP35	IO_L3N_T0_DQS_12	Bank12
J7.052	JB7.052	F1.AB31	IO_L22P_T3_A17_15	Bank15	F2.AP34	IO_L3P_T0_DQS_12	Bank12
J7.054	JB7.054	F1.AC32	IO_L20N_T3_A19_15	Bank15	F2.AR38	IO_L1N_T0_12	Bank12
J7.056	JB7.056	F1.AC31	IO_L20P_T3_A20_15	Bank15	F2.AR37	IO_L1P_T0_12	Bank12
J7.058	JB7.058	F1.AD34	IO_L3N_T0_AD1N_15	Bank15	F2.AH33	IO_L23N_T3_13	Bank13
J7.060	JB7.060	F1.AD33	IO_L3P_T0_AD1P_15	Bank15	F2.AH32	IO_L23P_T3_13	Bank13
J7.062	JB7.062	F1.AD36	IO_L5N_T0_AD9N_15	Bank15	F2.AN42	IO_L15N_T2_DQS_13	Bank13
J7.064	JB7.064	F1.AD35	IO_L5P_T0_AD9P_15	Bank15	F2.AM42	IO_L15P_T2_DQS_13	Bank13
J7.066	JB7.066	F1.AC34	IO_L1N_T0_AD0N_15	Bank15	F2.AN44	IO_L17N_T2_13	Bank13
J7.068	JB7.068	F1.AC33	IO_L1P_T0_AD0P_15	Bank15	F2.AN43	IO_L17P_T2_13	Bank13
J7.070	JB7.070	F1.AC38	IO_L10N_T1_AD11N_15	Bank15	F2.AM41	IO_L13N_T2_MRCC_13	Bank13
J7.072	JB7.072	F1.AD38	IO_L10P_T1_AD11P_15	Bank15	F2.AM40	IO_L13P_T2_MRCC_13	Bank13
J7.074	JB7.074	F1.AD40	IO_L7N_T1_AD2N_15	Bank15	F2.AM44	IO_L18N_T2_13	Bank13
J7.076	JB7.076	F1.AD39	IO_L7P_T1_AD2P_15	Bank15	F2.AL44	IO_L18P_T2_13	Bank13
J7.078	JB7.078	F1.AB41	IO_L13N_T2_MRCC_15	Bank15	F2.AL43	IO_L16N_T2_13	Bank13
J7.080	JB7.080	F1.AC41	IO_L13P_T2_MRCC_15	Bank15	F2.AL42	IO_L16P_T2_13	Bank13
J7.082	JB7.082	F1.AC44	IO_L17N_T2_A25_15	Bank15	F2.AJ40	IO_L6N_T0_VREF_13	Bank13
J7.084	JB7.084	F1.AC43	IO_L17P_T2_A26_15	Bank15	F2.AJ39	IO_L6P_T0_13	Bank13
J7.086	JB7.086	F1.AB42	IO_L15N_T2_ADV_B_15	Bank15	F2.AK38	IO_L10N_T1_13	Bank13
J7.088	JB7.088	F1.AC42	IO_L15P_T2_DQS_15	Bank15	F2.AJ38	IO_L10P_T1_13	Bank13

J7 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J7.090	JB7.090	F1.AA44	IO_L18N_T2_A23_15	Bank15	F2.AH38	IO_L8N_T1_13	Bank13
J7.092	JB7.092	F1.AB44	IO_L18P_T2_A24_15	Bank15	F2.AH37	IO_L8P_T1_13	Bank13
J7.094	JB7.094	F1.Y31	IO_L23N_T3_16	Bank16	F2.AJ44	IO_L4N_T0_13	Bank13
J7.096	JB7.096	F1.Y30	IO_L23P_T3_16	Bank16	F2.AJ43	IO_L4P_T0_13	Bank13
J7.098	JB7.098	F1.Y33	IO_L21N_T3_DQS_16	Bank16	F2.AH44	IO_L2N_T0_13	Bank13
J7.100	JB7.100	F1.Y32	IO_L21P_T3_DQS_16	Bank16	F2.AH43	IO_L2P_T0_13	Bank13
J7.102	JB7.102	F1.V32	IO_L19N_T3_VREF_16	Bank16	F2.AB42	IO_L15N_T2_ADV_B_15	Bank15
J7.104	JB7.104	F1.V31	IO_L19P_T3_16	Bank16	F2.AC42	IO_L15P_T2_15	Bank15
J7.106	JB7.106	F1.W34	IO_L3N_T0_DQS_16	Bank16	F2.AA44	IO_L18N_T2_A23_15	Bank15
J7.108	JB7.108	F1.W33	IO_L3P_T0_DQS_16	Bank16	F2.AB44	IO_L18P_T2_A24_15	Bank15
J7.110	JB7.110	F1.V34	IO_L1N_T0_16	Bank16	F2.AA43	IO_L16N_T2_A27_15	Bank15
J7.112	JB7.112	F1.V33	IO_L1P_T0_16	Bank16	F2.AA42	IO_L16P_T2_A28_15	Bank15
J7.114	JB7.114	F1.Y36	IO_L5N_T0_16	Bank16	F2.AA40	IO_L14N_T2_SRCC_15	Bank15
J7.116	JB7.116	F1.Y35	IO_L5P_T0_16	Bank16	F2.AB40	IO_L14P_T2_SRCC_15	Bank15
J7.118	JB7.118	F1.W36	IO_L6N_T0_VREF_16	Bank16	F2.AB39	IO_L11N_T1_SRCC_15	Bank15
J7.120	JB7.120	F1.W35	IO_L6P_T0_16	Bank16	F2.AC39	IO_L11P_T1_SRCC_15	Bank15

J12 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J12.001	JB12.001	F1.C8	IO_L8N_T1_39	Bank39	F2.AA9	IO_L20N_T3_37	Bank37
J12.003	JB12.003	F1.D8	IO_L8P_T1_39	Bank39	F2.AA10	IO_L20P_T3_37	Bank37
J12.005	JB12.005	F1.H7	IO_L2N_T0_39	Bank39	F2.AA7	IO_L22N_T3_37	Bank37
J12.007	JB12.007	F1.H8	IO_L2P_T0_39	Bank39	F2.AA8	IO_L22P_T3_37	Bank37
J12.009	JB12.009	F1.B5	IO_L9N_T1_DQS_39	Bank39	F2.Y6	IO_L24N_T3_37	Bank37
J12.011	JB12.011	F1.B6	IO_L9P_T1_DQS_39	Bank39	F2.Y7	IO_L24P_T3_37	Bank37
J12.013	JB12.013	F1.G6	IO_L4N_T0_39	Bank39	F2.AA4	IO_L17N_T2_37	Bank37
J12.015	JB12.015	F1.G7	IO_L4P_T0_39	Bank39	F2.AA5	IO_L17P_T2_37	Bank37
J12.017	JB12.017	F1.F5	IO_L5N_T0_39	Bank39	F2.AA2	IO_L18N_T2_37	Bank37
J12.019	JB12.019	F1.G5	IO_L5P_T0_39	Bank39	F2.AA3	IO_L18P_T2_37	Bank37
J12.021	JB12.021	F1.D5	IO_L11N_T1_SRCC_39	Bank39	F2.BD18	IO_L4N_T0_33	Bank33
J12.023	JB12.023	F1.E5	IO_L11P_T1_SRCC_39	Bank39	F2.BC18	IO_L4P_T0_33	Bank33
J12.025	JB12.025	F1.H2	IO_L20N_T3_39	Bank39	F2.BB20	IO_L2N_T0_33	Bank33
J12.027	JB12.027	F1.H3	IO_L20P_T3_39	Bank39	F2.BA20	IO_L2P_T0_33	Bank33
J12.029	JB12.029	F1.M9	IO_L5N_T0_38	Bank38	F2.AW14	IO_L8N_T1_32	Bank32
J12.031	JB12.031	F1.M10	IO_L5P_T0_38	Bank38	F2.AV14	IO_L8P_T1_32	Bank32
J12.033	JB12.033	F1.K8	IO_L1N_T0_38	Bank38	F2.BA15	IO_L9N_T1_DQS_32	Bank32
J12.035	JB12.035	F1.L9	IO_L1P_T0_38	Bank38	F2.AY15	IO_L9P_T1_DQS_32	Bank32
J12.037	JB12.037	F1.L7	IO_L6N_T0_VREF_38	Bank38	F2.BA13	IO_L6N_T0_VREF_32	Bank32
J12.039	JB12.039	F1.L8	IO_L6P_T0_38	Bank38	F2.BA14	IO_L6P_T0_32	Bank32
J12.041	JB12.041	F1.K6	IO_L2N_T0_38	Bank38	F2.BD14	IO_L2N_T0_32	Bank32
J12.043	JB12.043	F1.K7	IO_L2P_T0_38	Bank38	F2.BC14	IO_L2P_T0_32	Bank32
J12.045	JB12.045	F1.M4	IO_L11N_T1_SRCC_38	Bank38	F2.BB14	IO_L4N_T0_32	Bank32
J12.047	JB12.047	F1.M5	IO_L11P_T1_SRCC_38	Bank38	F2.BB15	IO_L4P_T0_32	Bank32
J12.049	JB12.049	F1.J4	IO_L8N_T1_38	Bank38	F2.BD15	IO_L5N_T0_32	Bank32

J12 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J12.051	JB12.051	F1.J5	IO_L8P_T1_38	Bank38	F2.BD16	IO_L5P_T0_32	Bank32
J12.053	JB12.053	F1.N3	IO_L13N_T2_MRCC_38	Bank38	F2.BC16	IO_L3N_T0_DQS_32	Bank32
J12.055	JB12.055	F1.N4	IO_L13P_T2_MRCC_38	Bank38	F2.BC17	IO_L3P_T0_DQS_32	Bank32
J12.057	JB12.057	F1.J3	IO_L10N_T1_38	Bank38	F2.BB16	IO_L1N_T0_32	Bank32
J12.059	JB12.059	F1.K3	IO_L10P_T1_38	Bank38	F2.BB17	IO_L1P_T0_32	Bank32
J12.061	JB12.061	F1.P1	IO_L16N_T2_38	Bank38	F2.AM16	IO_L19N_T3_VREF_32	Bank32
J12.063	JB12.063	F1.R1	IO_L16P_T2_38	Bank38	F2.AM17	IO_L19P_T3_32	Bank32
J12.065	JB12.065	F1.R2	IO_L18N_T2_38	Bank38	F2.AL14	IO_L24N_T3_32	Bank32
J12.067	JB12.067	F1.R3	IO_L18P_T2_38	Bank38	F2.AL15	IO_L24P_T3_32	Bank32
J12.069	JB12.069	F1.N8	IO_L19N_T3_VREF_38	Bank38	F2.AK15	IO_L21N_T3_DQS_32	Bank32
J12.071	JB12.071	F1.N9	IO_L19P_T3_38	Bank38	F2.AK16	IO_L21P_T3_DQS_32	Bank32
J12.073	JB12.073	F1.P9	IO_L23N_T3_38	Bank38	F2.AJ15	IO_L23N_T3_32	Bank32
J12.075	JB12.075	F1.P10	IO_L23P_T3_38	Bank38	F2.AJ16	IO_L23P_T3_32	Bank32
J12.077	JB12.077	F1.U9	IO_L6N_T0_VREF_37	Bank37	F2.AP13	IO_L10N_T1_31	Bank31
J12.079	JB12.079	F1.U10	IO_L6P_T0_37	Bank37	F2.AN13	IO_L10P_T1_31	Bank31
J12.081	JB12.081	F1.R8	IO_L2N_T0_37	Bank37	F2.AR10	IO_L7N_T1_31	Bank31
J12.083	JB12.083	F1.T9	IO_L2P_T0_37	Bank37	F2.AP10	IO_L7P_T1_31	Bank31
J12.085	JB12.085	F1.T7	IO_L4N_T0_37	Bank37	F2.AR11	IO_L11N_T1_SRCC_31	Bank31
J12.087	JB12.087	F1.T8	IO_L4P_T0_37	Bank37	F2.AP11	IO_L11P_T1_SRCC_31	Bank31
J12.089	JB12.089	F1.U6	IO_L1N_T0_37	Bank37	F2.AU10	IO_L15N_T2_DQS_31	Bank31
J12.091	JB12.091	F1.U7	IO_L1P_T0_37	Bank37	F2.AT10	IO_L15P_T2_DQS_31	Bank31
J12.093	JB12.093	F1.U4	IO_L12N_T1_MRCC_37	Bank37	F2.AT12	IO_L12N_T1_MRCC_31	Bank31
J12.095	JB12.095	F1.U5	IO_L12P_T1_MRCC_37	Bank37	F2.AR12	IO_L12P_T1_MRCC_31	Bank31
J12.097	JB12.097	F1.T4	IO_L8N_T1_37	Bank37	F2.AV11	IO_L14N_T2_SRCC_31	Bank31
J12.099	JB12.099	F1.T5	IO_L8P_T1_37	Bank37	F2.AV12	IO_L14P_T2_SRCC_31	Bank31
J12.101	JB12.101	F1.V3	IO_L11N_T1_SRCC_37	Bank37	F2.AY10	IO_L17N_T2_31	Bank31
J12.103	JB12.103	F1.V4	IO_L11P_T1_SRCC_37	Bank37	F2.AW10	IO_L17P_T2_31	Bank31
J12.105	JB12.105	F1.T2	IO_L10N_T1_37	Bank37	F2.AY11	IO_L16N_T2_31	Bank31
J12.107	JB12.107	F1.T3	IO_L10P_T1_37	Bank37	F2.AW11	IO_L16P_T2_31	Bank31
J12.109	JB12.109	F1.U1	IO_L7N_T1_37	Bank37	F2.BB10	IO_L19N_T3_VREF_31	Bank31
J12.111	JB12.111	F1.U2	IO_L7P_T1_37	Bank37	F2.BA10	IO_L19P_T3_31	Bank31
J12.113	JB12.113	F1.V1	IO_L9N_T1_DQS_37	Bank37	F2.BC11	IO_L20N_T3_31	Bank31
J12.115	JB12.115	F1.V2	IO_L9P_T1_DQS_37	Bank37	F2.BB11	IO_L20P_T3_31	Bank31
J12.117	JB12.117	F1.Y2	IO_L15N_T2_DQS_37	Bank37	F2.BD10	IO_L22N_T3_31	Bank31
J12.119	JB12.119	F1.Y3	IO_L15P_T2_DQS_37	Bank37	F2.BD11	IO_L22P_T3_31	Bank31
J12.002	JB12.002	F1.E8	IO_L1N_T0_39	Bank39	F2.W9	IO_L19N_T3_VREF_37	Bank37
J12.004	JB12.004	F1.F8	IO_L1P_T0_39	Bank39	F2.W10	IO_L19P_T3_37	Bank37
J12.006	JB12.006	F1.C6	IO_L7N_T1_39	Bank39	F2.W8	IO_L23N_T3_37	Bank37
J12.008	JB12.008	F1.C7	IO_L7P_T1_39	Bank39	F2.Y8	IO_L23P_T3_37	Bank37
J12.010	JB12.010	F1.E7	IO_L3N_T0_DQS_39	Bank39	F2.V6	IO_L21N_T3_DQS_37	Bank37
J12.012	JB12.012	F1.F7	IO_L3P_T0_DQS_39	Bank39	F2.W6	IO_L21P_T3_DQS_37	Bank37
J12.014	JB12.014	F1.H6	IO_L6N_T0_VREF_39	Bank39	F2.W1	IO_L16N_T2_37	Bank37
J12.016	JB12.016	F1.J6	IO_L6P_T0_39	Bank39	F2.Y1	IO_L16P_T2_37	Bank37
J12.018	JB12.018	F1.A7	IO_L10N_T1_39	Bank39	F2.BD19	IO_L5N_T0_33	Bank33
J12.020	JB12.020	F1.B7	IO_L10P_T1_39	Bank39	F2.BC19	IO_L5P_T0_33	Bank33
J12.022	JB12.022	F1.F4	IO_L19N_T3_VREF_39	Bank39	F2.BD20	IO_L3N_T0_DQS_33	Bank33
J12.024	JB12.024	F1.G4	IO_L19P_T3_39	Bank39	F2.BD21	IO_L3P_T0_DQS_33	Bank33

J12 Connector							
Top CON	Bottom CON	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
J12.026	JB12.026	F1.E3	IO_L21N_T3_DQS_39	Bank39	F2.BC21	IO_L1N_T0_33	Bank33
J12.028	JB12.028	F1.F3	IO_L21P_T3_DQS_39	Bank39	F2.BB21	IO_L1P_T0_33	Bank33
J12.030	JB12.030	F1.J1	IO_L9N_T1_DQS_38	Bank38	F2.AM14	IO_L22N_T3_32	Bank32
J12.032	JB12.032	F1.K1	IO_L9P_T1_DQS_38	Bank38	F2.AM15	IO_L22P_T3_32	Bank32
J12.034	JB12.034	F1.K2	IO_L7N_T1_38	Bank38	F2.AP14	IO_L20N_T3_32	Bank32
J12.036	JB12.036	F1.L2	IO_L7P_T1_38	Bank38	F2.AN14	IO_L20P_T3_32	Bank32
J12.038	JB12.038	F1.M1	IO_L15N_T2_DQS_38	Bank38	F2.AU14	IO_L10N_T1_32	Bank32
J12.040	JB12.040	F1.M2	IO_L15P_T2_DQS_38	Bank38	F2.AT14	IO_L10P_T1_32	Bank32
J12.042	JB12.042	F1.N1	IO_L17N_T2_38	Bank38	F2.AU15	IO_L13N_T2_MRCC_32	Bank32
J12.044	JB12.044	F1.N2	IO_L17P_T2_38	Bank38	F2.AT15	IO_L13P_T2_MRCC_32	Bank32
J12.046	JB12.046	F1.P5	IO_L22N_T3_38	Bank38	F2.BA17	IO_L7N_T1_32	Bank32
J12.048	JB12.048	F1.R5	IO_L22P_T3_38	Bank38	F2.AY17	IO_L7P_T1_32	Bank32
J12.050	JB12.050	F1.K5	IO_L4N_T0_38	Bank38	F2.AW15	IO_L11N_T1_SRCC_32	Bank32
J12.052	JB12.052	F1.L5	IO_L4P_T0_38	Bank38	F2.AV16	IO_L11P_T1_SRCC_32	Bank32
J12.054	JB12.054	F1.M6	IO_L3N_T0_DQS_38	Bank38	F2.AU16	IO_L14N_T2_SRCC_32	Bank32
J12.056	JB12.056	F1.M7	IO_L3P_T0_DQS_38	Bank38	F2.AU17	IO_L14P_T2_SRCC_32	Bank32
J12.058	JB12.058	F1.N7	IO_L21N_T3_DQS_38	Bank38	F2.AT17	IO_L16N_T2_32	Bank32
J12.060	JB12.060	F1.P8	IO_L21P_T3_DQS_38	Bank38	F2.AR17	IO_L16P_T2_32	Bank32
J12.062	JB12.062	F1.N6	IO_L20N_T3_38	Bank38	F2.AR15	IO_L18N_T2_32	Bank32
J12.064	JB12.064	F1.P6	IO_L20P_T3_38	Bank38	F2.AR16	IO_L18P_T2_32	Bank32
J12.066	JB12.066	F1.P3	IO_L14N_T2_SRCC_38	Bank38	F2.AP15	IO_L15N_T2_DQS_32	Bank32
J12.068	JB12.068	F1.P4	IO_L14P_T2_SRCC_38	Bank38	F2.AP16	IO_L15P_T2_DQS_32	Bank32
J12.070	JB12.070	F1.R6	IO_L24N_T3_38	Bank38	F2.AN16	IO_L17N_T2_32	Bank32
J12.072	JB12.072	F1.R7	IO_L24P_T3_38	Bank38	F2.AN17	IO_L17P_T2_32	Bank32
J12.074	JB12.074	F1.W1	IO_L16N_T2_37	Bank37	F2.AM11	IO_L1N_T0_31	Bank31
J12.076	JB12.076	F1.Y1	IO_L16P_T2_37	Bank37	F2.AM12	IO_L1P_T0_31	Bank31
J12.078	JB12.078	F1.AA2	IO_L18N_T2_37	Bank37	F2.AK12	IO_L4N_T0_31	Bank31
J12.080	JB12.080	F1.AA3	IO_L18P_T2_37	Bank37	F2.AK13	IO_L4P_T0_31	Bank31
J12.082	JB12.082	F1.AA7	IO_L22N_T3_37	Bank37	F2.AL12	IO_L3N_T0_DQS_31	Bank31
J12.084	JB12.084	F1.AA8	IO_L22P_T3_37	Bank37	F2.AL13	IO_L3P_T0_DQS_31	Bank31
J12.086	JB12.086	F1.W9	IO_L19N_T3_VREF_37	Bank37	F2.AJ10	IO_L2N_T0_31	Bank31
J12.088	JB12.088	F1.W10	IO_L19P_T3_37	Bank37	F2.AJ11	IO_L2P_T0_31	Bank31
J12.090	JB12.090	F1.AA9	IO_L20N_T3_37	Bank37	F2.AK10	IO_L6N_T0_VREF_31	Bank31
J12.092	JB12.092	F1.AA10	IO_L20P_T3_37	Bank37	F2.AK11	IO_L6P_T0_31	Bank31
J12.094	JB12.094	F1.V6	IO_L21N_T3_DQS_37	Bank37	F2.AM10	IO_L5N_T0_31	Bank31
J12.096	JB12.096	F1.W6	IO_L21P_T3_DQS_37	Bank37	F2.AL10	IO_L5P_T0_31	Bank31
J12.098	JB12.098	F1.W5	IO_L14N_T2_SRCC_37	Bank37	F2.AN11	IO_L9N_T1_DQS_31	Bank31
J12.100	JB12.100	F1.Y5	IO_L14P_T2_SRCC_37	Bank37	F2.AN12	IO_L9P_T1_DQS_31	Bank31
J12.102	JB12.102	F1.W8	IO_L23N_T3_37	Bank37	F2.BC12	IO_L23N_T3_31	Bank31
J12.104	JB12.104	F1.Y8	IO_L23P_T3_37	Bank37	F2.BB12	IO_L23P_T3_31	Bank31
J12.106	JB12.106	F1.AA4	IO_L17N_T2_37	Bank37	F2.BA12	IO_L21N_T3_DQS_31	Bank31
J12.108	JB12.108	F1.AA5	IO_L17P_T2_37	Bank37	F2.AY12	IO_L21P_T3_DQS_31	Bank31
J12.110	JB12.110	F1.Y6	IO_L24N_T3_37	Bank37	F2.BD13	IO_L24N_T3_31	Bank31
J12.112	JB12.112	F1.Y7	IO_L24P_T3_37	Bank37	F2.BC13	IO_L24P_T3_31	Bank31
J12.114	JB12.114	F1.V7	IO_L3N_T0_DQS_37	Bank37	F2.AY13	IO_L18N_T2_31	Bank31
J12.116	JB12.116	F1.V8	IO_L3P_T0_DQS_37	Bank37	F2.AW13	IO_L18P_T2_31	Bank31
J12.118	JB12.118	F1.V9	IO_L5N_T0_37	Bank37	F2.AT13	IO_L8N_T1_31	Bank31
J12.120	JB12.120	F1.V10	IO_L5P_T0_37	Bank37	F2.AR13	IO_L8P_T1_31	Bank31

8.5 Interconnection I/O

Inter-FPGA connections are directly connected between F1 and F2; there are a total of 50 Inter-FPGA connections. The voltage of Inter-FPGA connections is fixed to 1.8V. We recommend using LVDS on these Inter-FPGA connections for higher performance requirement.

Interconnection No.	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
INTER_BUS1	F1.F34	IO_0_VRN_22	Bank22	F2.AW34	IO_25_VRP_11	Bank11
INTER_BUS2	F1.B35	IO_L1P_T0_22	Bank22	F2.BB36	IO_L24P_T3_11	Bank11
INTER_BUS3	F1.A35	IO_L1N_T0_22	Bank22	F2.BC36	IO_L24N_T3_11	Bank11
INTER_BUS4	F1.D34	IO_L2P_T0_22	Bank22	F2.BC34	IO_L23P_T3_11	Bank11
INTER_BUS5	F1.C34	IO_L2N_T0_22	Bank22	F2.BD34	IO_L23N_T3_11	Bank11
INTER_BUS6	F1.D35	IO_L3P_T0_DQS_22	Bank22	F2.BA35	IO_L22P_T3_11	Bank11
INTER_BUS7	F1.D36	IO_L3N_T0_DQS_22	Bank22	F2.BB35	IO_L22N_T3_11	Bank11
INTER_BUS8	F1.B34	IO_L4P_T0_22	Bank22	F2.BD35	IO_L21P_T3_DQS_11	Bank11
INTER_BUS9	F1.A34	IO_L4N_T0_22	Bank22	F2.BD36	IO_L21N_T3_DQS_11	Bank11
INTER_BUS10	F1.C36	IO_L5P_T0_22	Bank22	F2.AW35	IO_L20P_T3_11	Bank11
INTER_BUS11	F1.B36	IO_L5N_T0_22	Bank22	F2.AY35	IO_L20N_T3_11	Bank11
INTER_BUS12	F1.F35	IO_L6P_T0_22	Bank22	F2.BA34	IO_L19P_T3_11	Bank11
INTER_BUS13	F1.E35	IO_L6N_T0_VREF_22	Bank22	F2.BB34	IO_L19N_T3_VREF_11	Bank11
INTER_BUS14	F1.E36	IO_L7P_T1_22	Bank22	F2.AY36	IO_L18P_T2_11	Bank11
INTER_BUS15	F1.E37	IO_L7N_T1_22	Bank22	F2.AY37	IO_L18N_T2_11	Bank11
INTER_BUS16	F1.A37	IO_L8P_T1_22	Bank22	F2.BC38	IO_L17P_T2_11	Bank11
INTER_BUS17	F1.A38	IO_L8N_T1_22	Bank22	F2.BD38	IO_L17N_T2_11	Bank11
INTER_BUS18	F1.F38	IO_L9P_T1_DQS_22	Bank22	F2.BB37	IO_L16P_T2_11	Bank11
INTER_BUS19	F1.F39	IO_L9N_T1_DQS_22	Bank22	F2.BC37	IO_L16N_T2_11	Bank11
INTER_BUS20	F1.C37	IO_L10P_T1_22	Bank22	F2.AW38	IO_L15P_T2_DQS_11	Bank11
INTER_BUS21	F1.B37	IO_L10N_T1_22	Bank22	F2.AW39	IO_L15N_T2_DQS_11	Bank11
INTER_BUS22	F1.E38	IO_L11P_T1_SRCC_22	Bank22	F2.BA37	IO_L14P_T2_SRCC_11	Bank11
INTER_BUS23	F1.D38	IO_L11N_T1_SRCC_22	Bank22	F2.BA38	IO_L14N_T2_SRCC_11	Bank11
INTER_BUS24	F1.C38	IO_L12P_T1_MRCC_22	Bank22	F2.AY38	IO_L13P_T2_MRCC_11	Bank11
INTER_BUS25	F1.C39	IO_L12N_T1_MRCC_22	Bank22	F2.BA39	IO_L13N_T2_MRCC_11	Bank11
INTER_BUS26	F1.D41	IO_L13P_T2_MRCC_22	Bank22	F2.AY40	IO_L12P_T1_MRCC_11	Bank11
INTER_BUS27	F1.C41	IO_L13N_T2_MRCC_22	Bank22	F2.BA40	IO_L12N_T1_MRCC_11	Bank11
INTER_BUS28	F1.D39	IO_L14P_T2_SRCC_22	Bank22	F2.BB39	IO_L11P_T1_SRCC_11	Bank11
INTER_BUS29	F1.D40	IO_L14N_T2_SRCC_22	Bank22	F2.BB40	IO_L11N_T1_SRCC_11	Bank11
INTER_BUS30	F1.B41	IO_L15P_T2_DQS_22	Bank22	F2.BC39	IO_L10P_T1_11	Bank11
INTER_BUS31	F1.A42	IO_L15N_T2_DQS_22	Bank22	F2.BD39	IO_L10N_T1_11	Bank11
INTER_BUS32	F1.B39	IO_L16P_T2_22	Bank22	F2.BC42	IO_L9P_T1_DQS_11	Bank11
INTER_BUS33	F1.B40	IO_L16N_T2_22	Bank22	F2.BC43	IO_L9N_T1_DQS_11	Bank11
INTER_BUS34	F1.C42	IO_L17P_T2_22	Bank22	F2.BD40	IO_L8P_T1_11	Bank11
INTER_BUS35	F1.B42	IO_L17N_T2_22	Bank22	F2.BD41	IO_L8N_T1_11	Bank11
INTER_BUS36	F1.A39	IO_L18P_T2_22	Bank22	F2.BB41	IO_L7P_T1_11	Bank11
INTER_BUS37	F1.A40	IO_L18N_T2_22	Bank22	F2.BC41	IO_L7N_T1_11	Bank11
INTER_BUS38	F1.F40	IO_L19P_T3_22	Bank22	F2.BA42	IO_L6P_T0_11	Bank11
INTER_BUS39	F1.E40	IO_L19N_T3_VREF_22	Bank22	F2.BB42	IO_L6N_T0_VREF_11	Bank11
INTER_BUS40	F1.E41	IO_L20P_T3_22	Bank22	F2.AY41	IO_L5P_T0_11	Bank11
INTER_BUS41	F1.E42	IO_L20N_T3_22	Bank22	F2.AY42	IO_L5N_T0_11	Bank11
INTER_BUS42	F1.D43	IO_L21P_T3_DQS_22	Bank22	F2.BA44	IO_L4P_T0_11	Bank11
INTER_BUS43	F1.D44	IO_L21N_T3_DQS_22	Bank22	F2.BB44	IO_L4N_T0_11	Bank11

Interconnection No.	F1 Pin No.	FPGA Pin Description	F1 Bank	F2 Pin No.	FPGA Pin Description	F2 Bank
INTER_BUS44	F1.C43	IO_L22P_T3_22	Bank22	F2.AW43	IO_L3P_T0_DQS_11	Bank11
INTER_BUS45	F1.C44	IO_L22N_T3_22	Bank22	F2.AW44	IO_L3N_T0_DQS_11	Bank11
INTER_BUS46	F1.F43	IO_L23P_T3_22	Bank22	F2.AY43	IO_L2P_T0_11	Bank11
INTER_BUS47	F1.F44	IO_L23N_T3_22	Bank22	F2.BA43	IO_L2N_T0_11	Bank11
INTER_BUS48	F1.F42	IO_L24P_T3_22	Bank22	F2.AW40	IO_L1P_T0_11	Bank11
INTER_BUS49	F1.E43	IO_L24N_T3_22	Bank22	F2.AW41	IO_L1N_T0_11	Bank11
INTER_BUS50	F1.F37	IO_25_VRP_22	Bank22	F2.AW36	IO_0_VRN_11	Bank11

8.6 SO-DIMM I/O

The DDR3 SO-DIMM J14 is used to plug DDR3 memory modules into the SO-DIMM sockets. It support up to 8G bytes capacity DDR3 SO-DIMM memory module. Pin connections and functions are described in Table 8-5.

Table 8-5 **DDR3 SO-DIMM Pin Properties**

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
A0	J14.98	F1.D26	IO_L15P_T2_DQS_18	Bank18
A1	J14.97	F1.C26	IO_L15N_T2_DQS_18	Bank18
A2	J14.96	F1.G26	IO_L10N_T1_18	Bank18
A3	J14.95	F1.B26	IO_L16P_T2_18	Bank18
A4	J14.92	F1.G27	IO_L9P_T1_DQS_18	Bank18
A5	J14.91	F1.A25	IO_L17N_T2_18	Bank18
A6	J14.90	F1.H26	IO_L10P_T1_18	Bank18
A7	J14.86	F1.P26	IO_L2N_T0_18	Bank18
A8	J14.89	F1.B25	IO_L17P_T2_18	Bank18
A9	J14.85	F1.H27	IO_L8P_T1_18	Bank18
A10	J14.107	F1.H28	IO_L8N_T1_18	Bank18
A11	J14.84	F1.R27	IO_L3N_T0_DQS_18	Bank18
A12	J14.83	F1.N26	IO_L4P_T0_18	Bank18
A13	J14.119	F1.R28	IO_L1N_T0_18	Bank18
A14	J14.80	F1.R25	IO_L6P_T0_18	Bank18
A15	J14.78	F1.R26	IO_L2P_T0_18	Bank18
BA0	J14.109	F1.F27	IO_L9N_T1_DQS_18	Bank18
BA1	J14.108	F1.B27	IO_L16N_T2_18	Bank18
BA2	J14.79	F1.T27	IO_L3P_T0_DQS_18	Bank18
CAS_B	J14.115	F1.G29	IO_L7P_T1_18	Bank18
RAS_B	J14.110	F1.A27	IO_L18P_T2_18	Bank18
WE_B	J14.113	F1.N27	IO_L4N_T0_18	Bank18
CKE0	J14.73	F1.E26	IO_L11P_T1_SRCC_18	Bank18
CKE1	J14.74	F1.E27	IO_L11N_T1_SRCC_18	Bank18
CLKN0	J14.103	F1.E28	IO_L12N_T1_MRCC_18	Bank18
CLKN1	J14.104	F1.C28	IO_L14N_T2_SRCC_18	Bank18
CLKP0	J14.101	F1.F28	IO_L12P_T1_MRCC_18	Bank18
CLKP1	J14.102	F1.C27	IO_L14P_T2_SRCC_18	Bank18

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
DM0	J14.11	F1.P23	IO_L5P_T0_17	Bank17
DM1	J14.28	F1.H24	IO_L8N_T1_17	Bank17
DM2	J14.46	F1.A22	IO_L17N_T2_17	Bank17
DM3	J14.63	F1.H21	IO_L24N_T3_17	Bank17
DM4	J14.136	F1.M31	IO_L1N_T0_19	Bank19
DM5	J14.153	F1.C33	IO_L7N_T1_19	Bank19
DM6	J14.170	F1.B30	IO_L16P_T2_19	Bank19
DM7	J14.187	F1.J31	IO_L22N_T3_19	Bank19
DQ0	J14.5	F1.R23	IO_L2N_T0_17	Bank17
DQ1	J14.7	F1.T23	IO_L2P_T0_17	Bank17
DQ2	J14.15	F1.T22	IO_L4P_T0_17	Bank17
DQ3	J14.17	F1.N24	IO_L1N_T0_17	Bank17
DQ4	J14.4	F1.R21	IO_L6P_T0_17	Bank17
DQ5	J14.6	F1.R22	IO_L4N_T0_17	Bank17
DQ6	J14.16	F1.N23	IO_L5N_T0_17	Bank17
DQ7	J14.18	F1.P24	IO_L1P_T0_17	Bank17
DQ8	J14.21	F1.J23	IO_L7P_T1_17	Bank17
DQ9	J14.23	F1.G25	IO_L10P_T1_17	Bank17
DQ10	J14.33	F1.F25	IO_L10N_T1_17	Bank17
DQ11	J14.35	F1.E22	IO_L11N_T1_SRCC_17	Bank17
DQ12	J14.22	F1.H23	IO_L7N_T1_17	Bank17
DQ13	J14.24	F1.J24	IO_L8P_T1_17	Bank17
DQ14	J14.34	F1.F23	IO_L12P_T1_MRCC_17	Bank17
DQ15	J14.36	F1.F22	IO_L11P_T1_SRCC_17	Bank17
DQ16	J14.39	F1.D23	IO_L13P_T2_MRCC_17	Bank17
DQ17	J14.41	F1.C24	IO_L14N_T2_SRCC_17	Bank17
DQ18	J14.51	F1.A23	IO_L17P_T2_17	Bank17
DQ19	J14.53	F1.B24	IO_L18P_T2_17	Bank17
DQ20	J14.40	F1.E25	IO_L16P_T2_17	Bank17
DQ21	J14.42	F1.D24	IO_L14P_T2_SRCC_17	Bank17
DQ22	J14.50	F1.D25	IO_L16N_T2_17	Bank17
DQ23	J14.52	F1.C23	IO_L13N_T2_MRCC_17	Bank17
DQ24	J14.57	F1.K21	IO_L23N_T3_17	Bank17
DQ25	J14.59	F1.K22	IO_L23P_T3_17	Bank17
DQ26	J14.67	F1.H22	IO_L20P_T3_17	Bank17
DQ27	J14.69	F1.G22	IO_L20N_T3_17	Bank17
DQ28	J14.56	F1.L22	IO_L22N_T3_17	Bank17
DQ29	J14.58	F1.M22	IO_L22P_T3_17	Bank17
DQ30	J14.68	F1.J21	IO_L24P_T3_17	Bank17
DQ31	J14.70	F1.L23	IO_L19P_T3_17	Bank17
DQ32	J14.129	F1.N33	IO_L4N_T0_19	Bank19
DQ33	J14.131	F1.N32	IO_L4P_T0_19	Bank19
DQ34	J14.141	F1.L29	IO_L5P_T0_19	Bank19

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
DQ35	J14.143	F1.L30	IO_L5N_T0_19	Bank19
DQ36	J14.130	F1.M30	IO_L1P_T0_19	Bank19
DQ37	J14.132	F1.N31	IO_L6P_T0_19	Bank19
DQ38	J14.140	F1.L32	IO_L2P_T0_19	Bank19
DQ39	J14.142	F1.L33	IO_L2N_T0_19	Bank19
DQ40	J14.147	F1.G31	IO_L8P_T1_19	Bank19
DQ41	J14.149	F1.E32	IO_L11N_T1_SRCC_19	Bank19
DQ42	J14.157	F1.F32	IO_L11P_T1_SRCC_19	Bank19
DQ43	J14.159	F1.F33	IO_L10P_T1_19	Bank19
DQ44	J14.146	F1.E31	IO_L12P_T1_MRCC_19	Bank19
DQ45	J14.148	F1.G32	IO_L8N_T1_19	Bank19
DQ46	J14.158	F1.E33	IO_L10N_T1_19	Bank19
DQ47	J14.160	F1.D33	IO_L7P_T1_19	Bank19
DQ48	J14.163	F1.A30	IO_L17N_T2_19	Bank19
DQ49	J14.165	F1.A29	IO_L17P_T2_19	Bank19
DQ50	J14.175	F1.D30	IO_L13P_T2_MRCC_19	Bank19
DQ51	J14.177	F1.C31	IO_L13N_T2_MRCC_19	Bank19
DQ52	J14.164	F1.C29	IO_L18P_T2_19	Bank19
DQ53	J14.166	F1.B31	IO_L16N_T2_19	Bank19
DQ54	J14.174	F1.E30	IO_L14N_T2_SRCC_19	Bank19
DQ55	J14.176	F1.F30	IO_L14P_T2_SRCC_19	Bank19
DQ56	J14.181	F1.H29	IO_L24P_T3_19	Bank19
DQ57	J14.183	F1.G30	IO_L24N_T3_19	Bank19
DQ58	J14.191	F1.K31	IO_L22P_T3_19	Bank19
DQ59	J14.193	F1.J33	IO_L20P_T3_19	Bank19
DQ60	J14.180	F1.H33	IO_L20N_T3_19	Bank19
DQ61	J14.182	F1.H31	IO_L19P_T3_19	Bank19
DQ62	J14.192	F1.K33	IO_L23N_T3_19	Bank19
DQ63	J14.194	F1.K32	IO_L23P_T3_19	Bank19
DQSN0	J14.10	F1.N21	IO_L3N_T0_DQS_17	Bank17
DQSN1	J14.27	F1.F24	IO_L9N_T1_DQS_17	Bank17
DQSN2	J14.45	F1.B22	IO_L15N_T2_DQS_17	Bank17
DQSN3	J14.62	F1.L24	IO_L21N_T3_DQS_17	Bank17
DQSN4	J14.135	F1.M29	IO_L3N_T0_DQS_19	Bank19
DQSN5	J14.152	F1.B32	IO_L9N_T1_DQS_19	Bank19
DQSN6	J14.169	F1.A33	IO_L15N_T2_DQS_19	Bank19
DQSN7	J14.186	F1.J30	IO_L21N_T3_DQS_19	Bank19
DQSP0	J14.12	F1.N22	IO_L3P_T0_DQS_17	Bank17
DQSP1	J14.29	F1.G24	IO_L9P_T1_DQS_17	Bank17
DQSP2	J14.47	F1.C22	IO_L15P_T2_DQS_17	Bank17
DQSP3	J14.64	F1.M24	IO_L21P_T3_DQS_17	Bank17
DQSP4	J14.137	F1.N29	IO_L3P_T0_DQS_19	Bank19
DQSP5	J14.154	F1.C32	IO_L9P_T1_DQS_19	Bank19

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
DQSP6	J14.171	F1.A32	IO_L15P_T2_DQS_19	Bank19
DQSP7	J14.188	F1.K30	IO_L21P_T3_DQS_19	Bank19
ODT0	J14.116	F1.F29	IO_L7N_T1_18	Bank18
ODT1	J14.120	F1.P28	IO_L5P_T0_18	Bank18
S0_B	J14.114	F1.N28	IO_L5N_T0_18	Bank18
S1_B	J14.121	F1.T28	IO_L1P_T0_18	Bank18
RESET_B	J14.30	F1.B29	IO_L18N_T2_19	Bank19
EVENT_B	J14.198	F1.A28	IO_L18N_T2_18	Bank18
SCL	J14.202	F1.N17	IO_25_VRP_40	Bank40
SDA	J14.200	F1.M17	IO_0_VRN_40	Bank40
SA0	J14.197	Tied to Low		
SA1	J14.201	Tied to Low		

The DDR2 SO-DIMM J13 is used to plug DDR2 memory modules into the SO-DIMM sockets. It support up to 2G bytes capacity DDR2 SO-DIMM memory module. Pin connections and functions are described in Table 8-6.

Table 8-6 **DDR2 SO-DIMM Pin Properties**

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
A0	J13.102	F2.BC27	IO_L6P_T0_35	Bank35
A1	J13.101	F2.BC26	IO_L1P_T0_AD4P_35	Bank35
A2	J13.100	F2.BD26	IO_L1N_T0_AD4N_35	Bank35
A3	J13.99	F2.BB26	IO_L3P_T0_DQS_AD5P_35	Bank35
A4	J13.98	F2.AT29	IO_L16P_T2_35	Bank35
A5	J13.97	F2.AY28	IO_L7P_T1_AD6P_35	Bank35
A6	J13.94	F2.BA27	IO_L5P_T0_AD13P_35	Bank35
A7	J13.92	F2.AY27	IO_L8N_T1_AD14N_35	Bank35
A8	J13.93	F2.AW29	IO_L9N_T1_DQS_AD7N_35	Bank35
A9	J13.91	F2.AY26	IO_L8P_T1_AD14P_35	Bank35
A10	J13.105	F2.BB27	IO_L3N_T0_DQS_AD5N_35	Bank35
A11	J13.90	F2.AW26	IO_L10N_T1_AD15N_35	Bank35
A12	J13.89	F2.AW28	IO_L9P_T1_DQS_AD7P_35	Bank35
A13	J13.116	F2.BD29	IO_L4N_T0_35	Bank35
A14	J13.86	F2.AV26	IO_L10P_T1_AD15P_35	Bank35
A15	J13.84	F2.AR28	IO_L15N_T2_DQS_35	Bank35
BA0	J13.107	F2.BA29	IO_L7N_T1_AD6N_35	Bank35
BA1	J13.106	F2.BD28	IO_L4P_T0_35	Bank35
BA2	J13.85	F2.AP28	IO_L15P_T2_DQS_35	Bank35
CAS_B	J13.113	F2.BB29	IO_L2P_T0_AD12P_35	Bank35
RAS_B	J13.108	F2.BC29	IO_L2N_T0_AD12N_35	Bank35
WE_B	J13.109	F2.BA28	IO_L5N_T0_AD13N_35	Bank35
CKE0	J13.79	F2.AV27	IO_L11P_T1_SRCC_35	Bank35
CKE1	J13.80	F2.AV28	IO_L11N_T1_SRCC_35	Bank35

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
CLKN0	J13.32	F2.AU27	IO_L12N_T1_MRCC_35	Bank35
CLKN1	J13.166	F2.AT28	IO_L14N_T2_SRCC_35	Bank35
CLKP0	J13.30	F2.AU26	IO_L12P_T1_MRCC_35	Bank35
CLKP1	J13.164	F2.AT27	IO_L14P_T2_SRCC_35	Bank35
DM0	J13.10	F2.BC23	IO_L5P_T0_34	Bank34
DM1	J13.26	F2.AV24	IO_L12P_T1_MRCC_34	Bank34
DM2	J13.52	F2.AT23	IO_L13P_T2_MRCC_34	Bank34
DM3	J13.67	F2.AK23	IO_L22P_T3_34	Bank34
DM4	J13.130	F2.BC32	IO_L2N_T0_36	Bank36
DM5	J13.147	F2.AW33	IO_L7P_T1_36	Bank36
DM6	J13.170	F2.AR32	IO_L14P_T2_SRCC_36	Bank36
DM7	J13.185	F2.AN32	IO_L20N_T3_36	Bank36
DQ0	J13.5	F2.BA22	IO_L6P_T0_34	Bank34
DQ1	J13.7	F2.BB22	IO_L4P_T0_34	Bank34
DQ2	J13.17	F2.BB24	IO_L1P_T0_34	Bank34
DQ3	J13.19	F2.BB25	IO_L2N_T0_34	Bank34
DQ4	J13.4	F2.BC22	IO_L4N_T0_34	Bank34
DQ5	J13.6	F2.BD23	IO_L5N_T0_34	Bank34
DQ6	J13.14	F2.BC24	IO_L1N_T0_34	Bank34
DQ7	J13.16	F2.BA24	IO_L2P_T0_34	Bank34
DQ8	J13.23	F2.AU25	IO_L11N_T1_SRCC_34	Bank34
DQ9	J13.25	F2.AU24	IO_L11P_T1_SRCC_34	Bank34
DQ10	J13.35	F2.AW23	IO_L7N_T1_34	Bank34
DQ11	J13.37	F2.AY23	IO_L10N_T1_34	Bank34
DQ12	J13.20	F2.AY22	IO_L10P_T1_34	Bank34
DQ13	J13.22	F2.AV23	IO_L7P_T1_34	Bank34
DQ14	J13.36	F2.AY25	IO_L8P_T1_34	Bank34
DQ15	J13.38	F2.BA25	IO_L8N_T1_34	Bank34
DQ16	J13.43	F2.AN24	IO_L17P_T2_34	Bank34
DQ17	J13.45	F2.AN22	IO_L18P_T2_34	Bank34
DQ18	J13.55	F2.AP24	IO_L17N_T2_34	Bank34
DQ19	J13.57	F2.AT24	IO_L13N_T2_MRCC_34	Bank34
DQ20	J13.44	F2.AP23	IO_L14P_T2_SRCC_34	Bank34
DQ21	J13.46	F2.AR23	IO_L14N_T2_SRCC_34	Bank34
DQ22	J13.56	F2.AR25	IO_L16P_T2_34	Bank34
DQ23	J13.58	F2.AT25	IO_L16N_T2_34	Bank34
DQ24	J13.61	F2.AL24	IO_L19P_T3_34	Bank34
DQ25	J13.63	F2.AL23	IO_L22N_T3_34	Bank34
DQ26	J13.73	F2.AJ24	IO_L24N_T3_34	Bank34
DQ27	J13.75	F2.AK22	IO_L20N_T3_34	Bank34
DQ28	J13.62	F2.AL22	IO_L23P_T3_34	Bank34
DQ29	J13.64	F2.AM22	IO_L23N_T3_34	Bank34
DQ30	J13.74	F2.AJ23	IO_L24P_T3_34	Bank34
DQ31	J13.76	F2.AK21	IO_L20P_T3_34	Bank34
DQ32	J13.123	F2.BD30	IO_L4P_T0_36	Bank36

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
DQ33	J13.125	F2.BA30	IO_L6P_T0_36	Bank36
DQ34	J13.135	F2.BD33	IO_L1N_T0_36	Bank36
DQ35	J13.137	F2.BA32	IO_L5P_T0_36	Bank36
DQ36	J13.124	F2.BC31	IO_L2P_T0_36	Bank36
DQ37	J13.126	F2.BD31	IO_L4N_T0_36	Bank36
DQ38	J13.134	F2.BA33	IO_L5N_T0_36	Bank36
DQ39	J13.136	F2.BC33	IO_L1P_T0_36	Bank36
DQ40	J13.141	F2.AW31	IO_L10N_T1_36	Bank36
DQ41	J13.143	F2.AY33	IO_L7N_T1_36	Bank36
DQ42	J13.151	F2.AU32	IO_L11P_T1_SRCC_36	Bank36
DQ43	J13.153	F2.AU30	IO_L12P_T1_MRCC_36	Bank36
DQ44	J13.140	F2.AY30	IO_L8N_T1_36	Bank36
DQ45	J13.142	F2.AW30	IO_L8P_T1_36	Bank36
DQ46	J13.152	F2.AV31	IO_L10P_T1_36	Bank36
DQ47	J13.154	F2.AV32	IO_L11N_T1_SRCC_36	Bank36
DQ48	J13.157	F2.AT32	IO_L14N_T2_SRCC_36	Bank36
DQ49	J13.159	F2.AP30	IO_L17N_T2_36	Bank36
DQ50	J13.173	F2.AP29	IO_L17P_T2_36	Bank36
DQ51	J13.175	F2.AN33	IO_L16P_T2_36	Bank36
DQ52	J13.158	F2.AR31	IO_L13N_T2_MRCC_36	Bank36
DQ53	J13.160	F2.AR30	IO_L18P_T2_36	Bank36
DQ54	J13.174	F2.AP31	IO_L13P_T2_MRCC_36	Bank36
DQ55	J13.176	F2.AP33	IO_L16N_T2_36	Bank36
DQ56	J13.179	F2.AN31	IO_L20P_T3_36	Bank36
DQ57	J13.181	F2.AN29	IO_L24N_T3_36	Bank36
DQ58	J13.189	F2.AL32	IO_L19P_T3_36	Bank36
DQ59	J13.191	F2.AM31	IO_L22N_T3_36	Bank36
DQ60	J13.180	F2.AM29	IO_L24P_T3_36	Bank36
DQ61	J13.182	F2.AM30	IO_L22P_T3_36	Bank36
DQ62	J13.192	F2.AL29	IO_L23P_T3_36	Bank36
DQ63	J13.194	F2.AL30	IO_L23N_T3_36	Bank36
DQSN0	J13.11	F2.BD25	IO_L3N_T0_DQS_34	Bank34
DQSN1	J13.29	F2.AV22	IO_L9N_T1_DQS_34	Bank34
DQSN2	J13.49	F2.AT22	IO_L15N_T2_DQS_34	Bank34
DQSN3	J13.68	F2.AN21	IO_L21N_T3_DQS_34	Bank34
DQSN4	J13.129	F2.BB32	IO_L3N_T0_DQS_36	Bank36
DQSN5	J13.146	F2.AY32	IO_L9N_T1_DQS_36	Bank36
DQSN6	J13.167	F2.AT33	IO_L15N_T2_DQS_36	Bank36
DQSN7	J13.186	F2.AK31	IO_L21N_T3_DQS_36	Bank36
DQSP0	J13.13	F2.BD24	IO_L3P_T0_DQS_34	Bank34
DQSP1	J13.31	F2.AU22	IO_L9P_T1_DQS_34	Bank34
DQSP2	J13.51	F2.AR22	IO_L15P_T2_DQS_34	Bank34
DQSP3	J13.70	F2.AM21	IO_L21P_T3_DQS_34	Bank34
DQSP4	J13.131	F2.BB31	IO_L3P_T0_DQS_36	Bank36
DQSP5	J13.148	F2.AY31	IO_L9P_T1_DQS_36	Bank36

Net Name	SO-DIMM Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank
DQSP6	J13.169	F2.AR33	IO_L15P_T2_DQS_36	Bank36
DQSP7	J13.188	F2.AK30	IO_L21P_T3_DQS_36	Bank36
ODT0	J13.114	F2.AP26	IO_L17N_T2_35	Bank35
ODT1	J13.119	F2.AN27	IO_L18P_T2_35	Bank35
S0_B	J13.110	F2.AU29	IO_L16N_T2_35	Bank35
S1_B	J13.115	F2.AP25	IO_L17P_T2_35	Bank35
SCL	J13.197	F2.AK26	IO_L22N_T3_35	Bank35
SDA	J13.195	F2.AJ26	IO_L22P_T3_35	Bank35
SA0	J13.198	Tied to Low		
SA1	J13.200	Tied to Low		

8.7 Global control push button

One Dual Virtex-7 TAI Logic Module it provides two special global control push-buttons. One push buttons for user to use as global reset, the other push button is reserved for FPGA re-download by SD card as following function:

Table 8-7 **Push Button Properties**

Push button	FPGA IO Pin		I/O Supply	Remarks
	F1	F2		
SW1	AP31	E31	1.8V	It's connected to general IO on F1 and F2
SW2	N/A	N/A	1.8V	When push this button, SD card will re-download the FPGA design to F1 and F2

▲ NOTES:

The default value of the push buttons is "1"; when pressed, "0" should be accessed.

8.8 SD Card configuration address settings

One Dual Virtex-7 TAI Logic Module provides four sets of SD Card download configuration address. When user insert one programmed FPGA image SD card(Please refer TAI Player reference manual to know how to make programmed FPGA image SD card) into TAI Logic Module, it will automatic load FPGA image from one of the SD Card configuration address into TAI Logic module regarding to the Switch S6.1 and S6.2 settings on TAI Logic Module.

Table 8-8 **SD Card download settings**

Jumper		Configuration address	Remarks
S6.2	S6.1		
ON	ON	Suit0	load FPGA image from SD Card configuration Suit0
ON	OFF	Suit1	load FPGA image from SD Card configuration Suit1
OFF	ON	Suit2	load FPGA image from SD Card configuration Suit2
OFF	OFF	Suit3	load FPGA image from SD Card configuration Suit3

▲ NOTES:

The default setting of S6.2 and S6.1 is “ON ON” which means load FPGA image from SD Card configuration Suit0

8.9 RS232 interface

One Dual Virtex-7 TAI Logic Module it provides one RS232 interface (J26) for user to use. User can access the RS232 interface with F1 or F2. Regarding to the Switch S6.4 settings on TAI Logic Module, user will enable the RS232 interface of F1(set S6.4 to “OFF”) or F2(set S6.4 to “ON”)

Table 8-9 **RS232 Interface Properties**

Jumper J26	FPGA IO Pin		I/O Supply	Remarks
	F1	F2		
J26.1(TX)	E20	AU20	1.8V	It’s TX pin of RS232 interface
J26.2(RX)	F20	AU21	1.8V	It’s RX pin of RS232 interface
J26.3(GND)	N/A	N/A	N/A	It’s ground of RS232 interface

▲ NOTES:

The default setting of S6.4 is “OFF” which means it will enable the RS232 interface of F1

8.10 Test Area

Dual V7 TAI LM has two test areas for user debugging. Each FPGA (F1 and F2) has one test area which includes: 2 push buttons, 3 LEDs, 4 switches and 5 GPIOs. Pin connections and functions are described in Table 8-6 and Table 8-7.

Table 8-10 **Test area for F1**

Net Name	FPGA I/O Pin	Test I/O Pin	I/O Supply	Function
F1_TEST1	F1.E23/Bank17	S7.1	1.5V	Input signal. When switch is “ON”, the signal is “L”; when switch is “OFF”, the signal is “H”.
F1_TEST2	F1.A24/Bank17	S7.2	1.5V	
F1_TEST3	F1.M27/Bank18	S7.3	1.5V	
F1_TEST4	F1.L27/Bank18	S7.4	1.5V	
F1_TEST5	F1.K27/Bank18	SW3	1.5V	Input signal. When push the button, the signal is “L”; otherwise the signal is “H”.
F1_TEST6	F1.L25/Bank18	SW4	1.5V	
F1_TEST7	F1.K25/Bank18	LED40	1.5V	Output signal. When output is “H”, the LED will light; when output is “L”, the LED won’t light.
F1_TEST8	F1.K28/Bank18	LED41	1.5V	
F1_TEST9	F1.J28/Bank18	LED42	1.5V	
F1_TEST10	F1.K26/Bank18	J22.1	1.5V	GPIO signal.
F1_TEST11	F1.J26/Bank18	J22.3	1.5V	
F1_TEST12	F1.M25/Bank18	J22.5	1.5V	
F1_TEST13	F1.M26/Bank18	J22.2	1.5V	
F1_TEST14	F1.D31/Bank19	J22.4	1.5V	

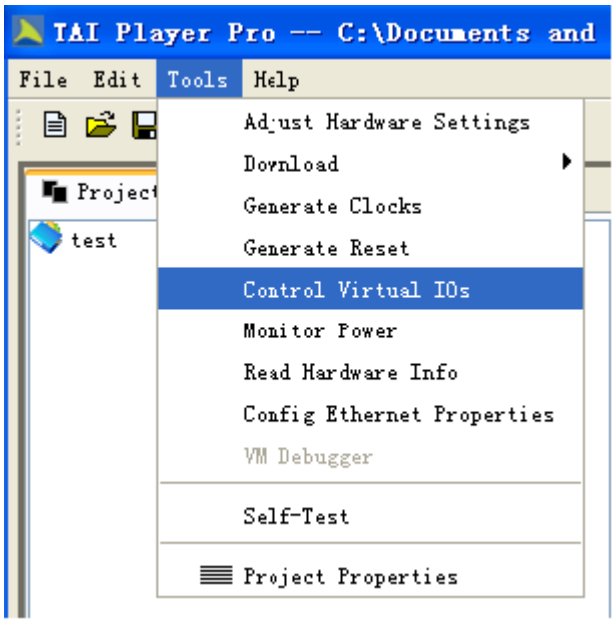
Table 8-11 **Test area for F2**

Net Name	FPGA I/O Pin	Test I/O Pin	I/O Supply	Function
F2_TEST1	F2.AW24/Bank34	S8.1	1.8V	Input signal. When switch is “ON”, the signal is “L”; when switch is “OFF”, the signal is “H”.
F2_TEST2	F2.AN23/Bank34	S8.2	1.8V	
F2_TEST3	F2.AN28/Bank35	S8.3	1.8V	
F2_TEST4	F2.AM26/Bank35	S8.4	1.8V	
F2_TEST5	F2.AK27/Bank35	SW5	1.8V	Input signal. When push the button, the signal is “L”; otherwise the signal is “H”.
F2_TEST6	F2.AL28/Bank35	SW6	1.8V	
F2_TEST7	F2.AL25/Bank35	LED43	1.8V	Output signal. When output is “H”, the LED will light; when output is “L”, the LED won’t light.
F2_TEST8	F2.AM25/Bank35	LED44	1.8V	
F2_TEST9	F2.AL27/Bank35	LED45	1.8V	
F2_TEST10	F2.AM27/Bank35	J23.1	1.8V	GPIO signal.
F2_TEST11	F2.AJ25/Bank35	J23.3	1.8V	
F2_TEST12	F2.AK25/Bank35	J23.5	1.8V	
F2_TEST13	F2.AU31/Bank36	J23.2	1.8V	
F2_TEST14	F2.AT30/Bank36	J23.4	1.8V	

8.11 Control Virtual IOs

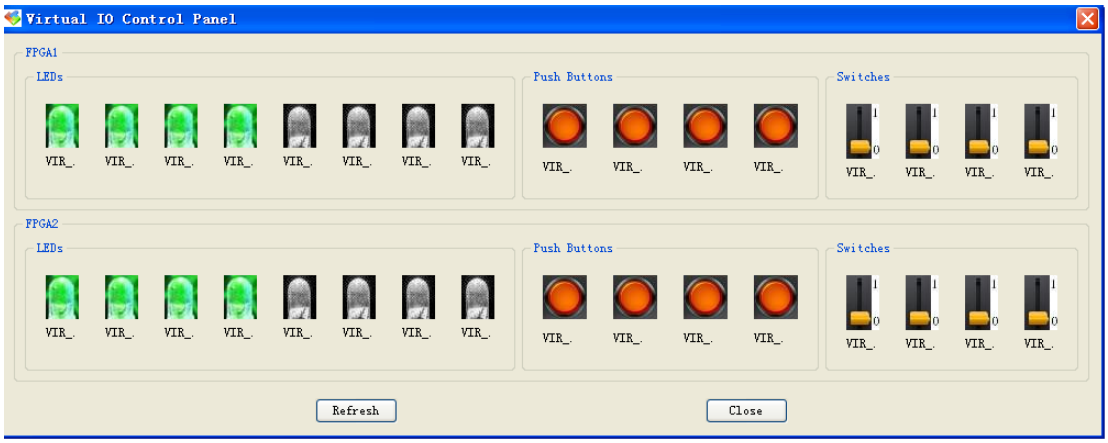
Dual Virtex-7 TAI Logic Module has two Virtual IOs areas for user debugging their TAI Logic Module in TAI Player Pro Runtime software through USB or Ethernet. Each FPGA (F1 and F2) has one group of Virtual IOs including four push buttons, four switches and eight LEDs. The figure below shows how to Control Virtual IOs in TAI Player Pro Runtime software

Figure 8-4 Control Virtual IOs in TAI Player Pro Runtime software



Select **Control Virtual IOs** menu item, which brings up Virtual IO Control Panel dialog as shown in the figure below.

Figure 8-5 Virtual IOs Control Panel



You can easily control the Virtual IOs in the Virtual IOs Control Panel above. For more detail of how to control Virtual IOs in the Virtual IOs Control Panel, pls refer to TAI Player Pro reference manual.Pin connections and functions of Virtual IOs are described in Table 8-11, Table 8-12 below.

***Table 8-12* Virtual I/O of F1**

Net Name	FPGA I/O Pin	Virtual I/O Pin	I/O Supply	Function
F1_V1	F1. AF42	Switch_F1.1	1.8V	Input signal. When switch is “ON”, the signal is “H”; when switch is “OFF”, the signal is “L”.
F1_V2	F1. AE43	Switch_F1.2	1.8V	
F1_V3	F1. AF43	Switch_F1.3	1.8V	
F1_V4	F1. AF44	Switch_F1.4	1.8V	
F1_V5	F1. AG44	Button_F1.1	1.8V	Input signal. When push the button, the signal is “L”; otherwise the signal is “H”.
F1_V6	F1. AG29	Button _F1.2	1.8V	
F1_V7	F1. AG30	Button _F1.3	1.8V	
F1_V8	F1. AE30	Button _F1.4	1.8V	
F1_V9	F1. AE31	LED_F1.1	1.8V	Output signal. When output is “H”, the LED will light; when output is “L”, the LED won’t light.
F1_V10	F1. AH28	LED_F1.2	1.8V	
F1_V11	F1. AH29	LED_F1.3	1.8V	
F1_V12	F1. AF29	LED_F1.4	1.8V	
F1_V13	F1. AF30	LED_F1.5	1.8V	
F1_V14	F1. AJ29	LED_F1.6	1.8V	
F1_V15	F1. AJ30	LED_F1.7	1.8V	
F1_V16	F1. AG31	LED_F1.8	1.8V	

***Table 8-13* Virtual I/O of F2**

Net Name	FPGA I/O Pin	Virtual I/O Pin	I/O Supply	Function
F2_V1	F2. AF42	Switch_F2.1	1.8V	Input signal. When switch is “ON”, the signal is “H”; when switch is “OFF”, the signal is “L”.
F2_V2	F2. AE43	Switch_F2.2	1.8V	
F2_V3	F2. AF43	Switch_F2.3	1.8V	
F2_V4	F2. AF44	Switch_F2.4	1.8V	
F2_V5	F2. AG44	Button_F2.1	1.8V	Input signal. When push the button, the signal is “L”; otherwise the signal is “H”.
F2_V6	F2. AG29	Button _F2.2	1.8V	

F2_V7	F2. AG30	Button _F2.3	1.8V	
F2_V8	F2. AE30	Button _F2.4	1.8V	
F2_V9	F2. AE31	LED_F2.1	1.8V	Output signal. When output is “H”, the LED will light; when output is “L”, the LED won’t light.
F2_V10	F2. AH28	LED_F2.2	1.8V	
F2_V11	F2. AH29	LED_F2.3	1.8V	
F2_V12	F2. AF29	LED_F2.4	1.8V	
F2_V13	F2. AF30	LED_F2.5	1.8V	
F2_V14	F2. AJ29	LED_F2.6	1.8V	
F2_V15	F2. AJ30	LED_F2.7	1.8V	
F2_V16	F2. AG31	LED_F2.8	1.8V	

9. Mating Connectors and Cables

This section provides information on TAI Logic Module-compatible connectors and cables. You can either directly purchase these parts from the vendor or contact S2C sales on how to order them.

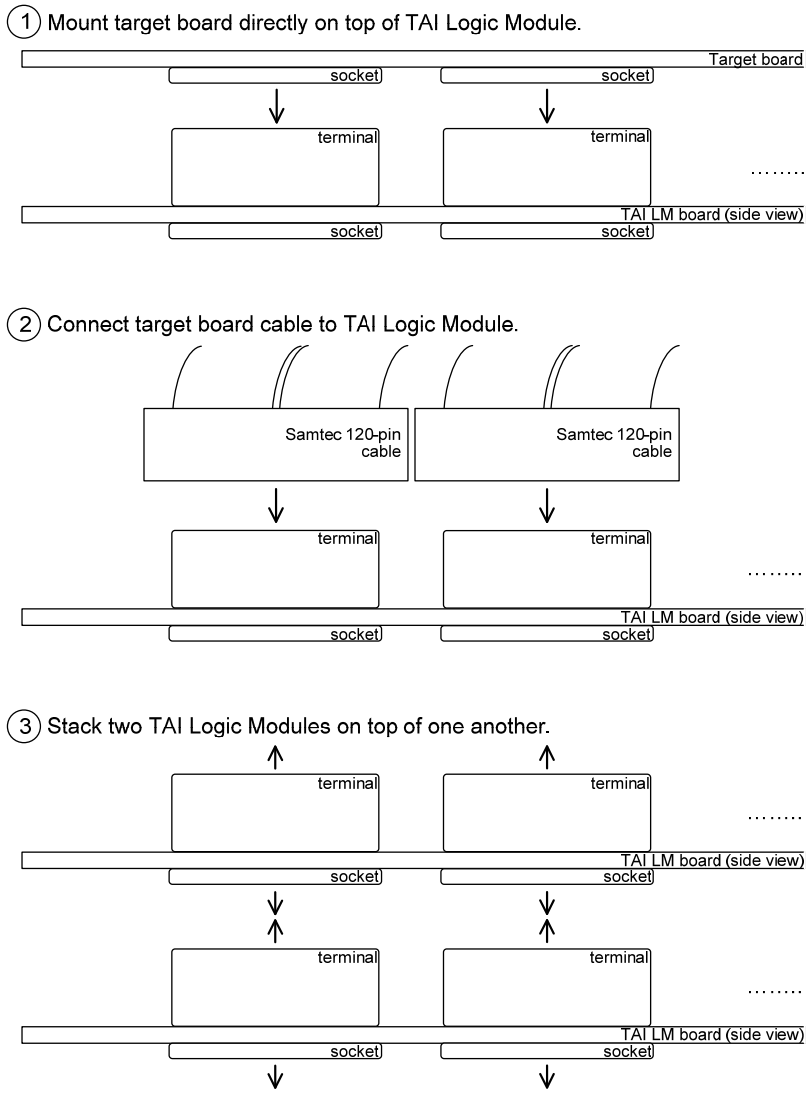
9.1 EXT Clock SMB

You can input 6 pairs of clocks using standard SMB connectors and cables.

9.2 External I/O (JX & JBX Connectors)

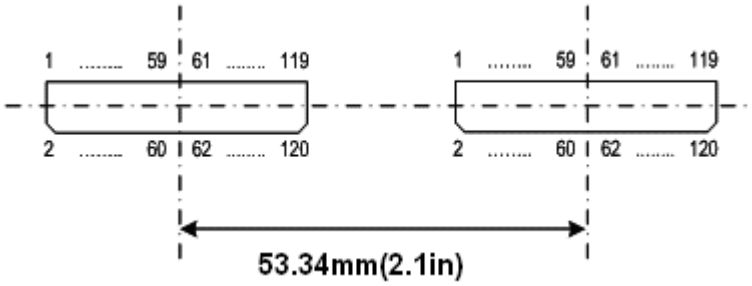
TAI Logic Module common I/O uses Samtec's Micro High Speed Interfaces QTH/QSH-060 connectors. These connectors allow you to connect TAI Logic Module to other hardware in three ways: (i) directly mount a target board onto TAI Logic Module, (ii) connect a target board and TAI Logic Module by cable, and (iii) stack multiple TAI Logic Modules together.

Figure 9-1 Board Connection Methods



All I/O connectors (including both dedicated and shared I/O connectors) keep the same relative spacing between each other. If your target board requires mounting on multiple I/O connectors, the spatial relationship among the connectors is as follows:

Figure 9-2 TAI Logic Module JX Connector Spacing



The specifications of the components needed to mate the external I/O connectors are as follows:

Top side (Terminal connector; use socket connector to mate or cable to mate)

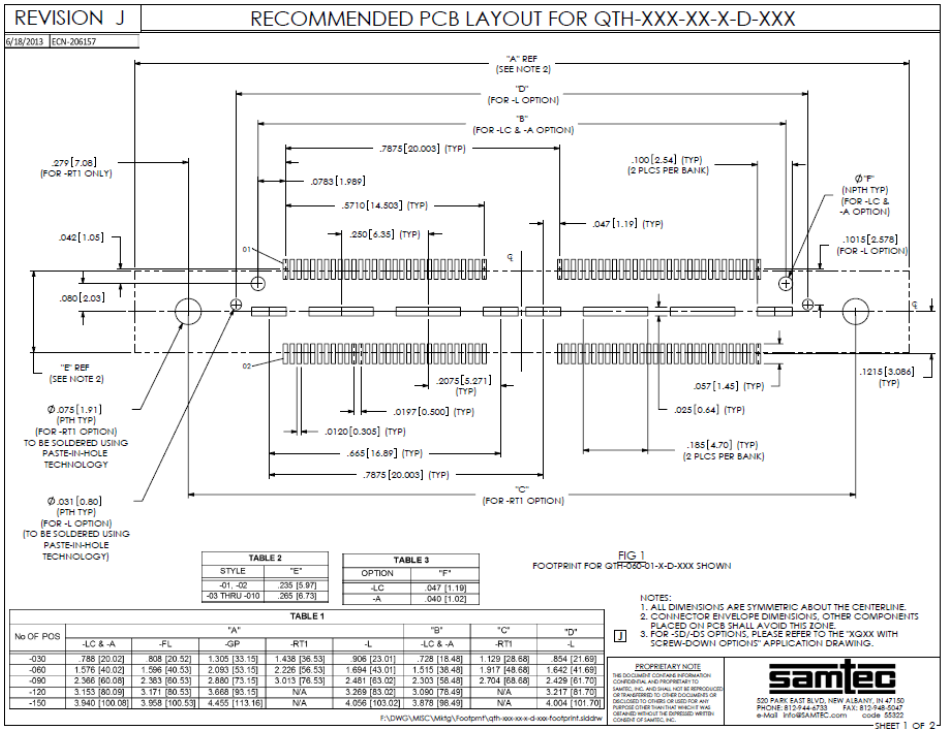
Manufacturer: Samtec

Part Number: QTH-060-05-F-D-A

Mates With: QSH-060-01-F-D-A

When you want to design a mother board to be stacked by TAI LM board, we recommend you choosing QTH-060-05-F-D-A, you can place QTH-060-05-F-D-A on the top side of the mother board, and it is high enough for stacking. The specification of QTH-060-05-F-D-A is shown on Figure 9-3.

Figure 9-3 QTH-060-05-F-D-A specification



Bottom side (Socket connector; use terminal connector)

Manufacturer: Samtec

Part Number: QSH-060-01-F-D-A

Mates With: QTH-060-01-F-D-A, QTH-060-05-F-D-A

We recommend using QSH-060-01-F-D-A for designing daughter board; you can place QSH-060-01-F-D-A on the bottom side of the daughter board. The daughter board can be stacked on JX on top side of TAI LM board. The specification of QSH-060-01-F-D-A is shown on Figure 9-4:

Figure 9-4 QSH-060-01-F-D-A specification

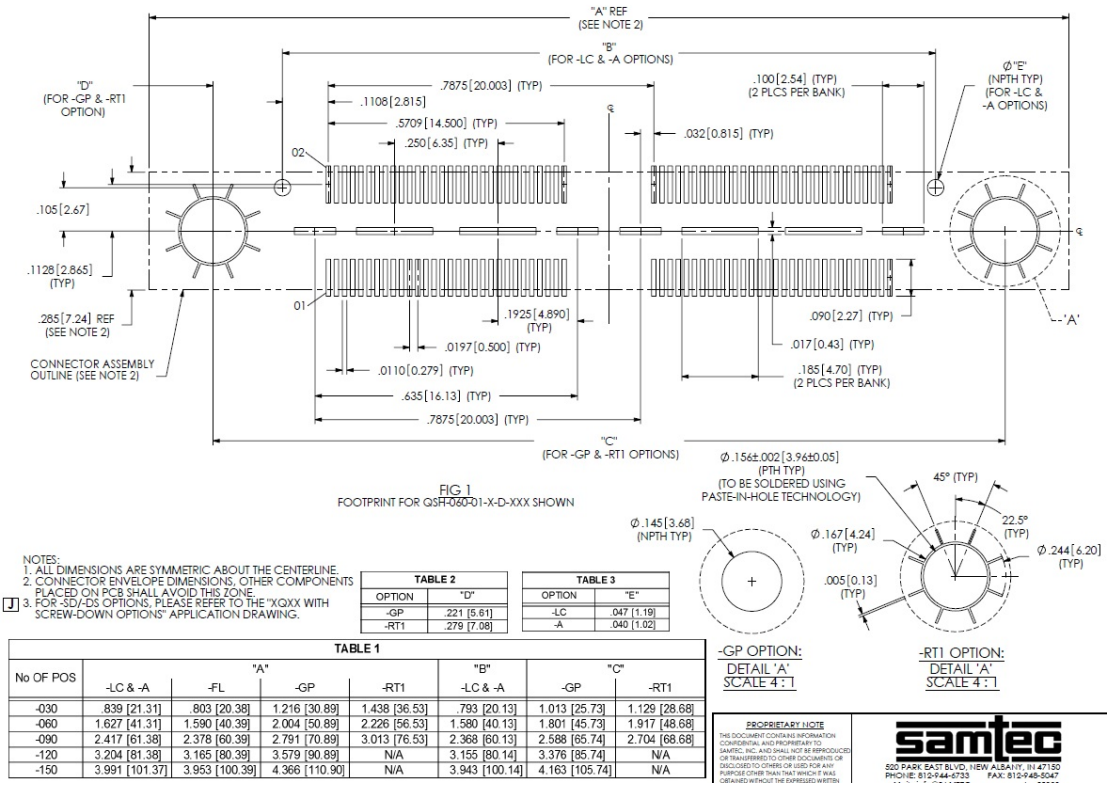


FIG 1
FOOTPRINT FOR QSH-060-01-X-D-XXX SHOWN

NOTES:
1. ALL DIMENSIONS ARE SYMMETRIC ABOUT THE CENTERLINE.
2. CONNECTOR ENVELOPE DIMENSIONS, OTHER COMPONENTS PLACED ON PCB SHALL AVOID THIS ZONE.
3. FOR -SD/-DS OPTIONS, PLEASE REFER TO THE "XQXX WITH SCREW-DOWN OPTIONS" APPLICATION DRAWING.

TABLE 2	
OPTION	"D"
-GP	.221 [5.61]
-RT1	.279 [7.08]

TABLE 3	
OPTION	"E"
-LC	.047 [1.19]
-A	.040 [1.02]

TABLE 1

No OF POS	"A"				"B"	"C"	
	-LC & -A	-FL	-GP	-RT1	-LC & -A	-GP	-RT1
-030	.839 [21.31]	.803 [20.38]	1.216 [30.89]	1.438 [36.53]	.793 [20.13]	1.013 [25.73]	1.129 [28.68]
-060	1.627 [41.31]	1.590 [40.39]	2.004 [50.89]	2.226 [56.53]	1.580 [40.13]	1.801 [45.73]	1.917 [48.68]
-090	2.417 [61.38]	2.378 [60.39]	2.791 [70.89]	3.013 [76.53]	2.368 [60.13]	2.588 [65.74]	2.704 [68.68]
-120	3.204 [81.38]	3.165 [80.39]	3.579 [90.89]	N/A	3.155 [80.14]	3.376 [85.74]	N/A
-150	3.991 [101.37]	3.953 [100.39]	4.366 [110.90]	N/A	3.943 [100.14]	4.163 [105.74]	N/A

samtec
520 PARK EAST BLVD, NEW ALBANY, IN 47150
PHONE: 812-944-6733 FAX: 812-945-5047

TAI Logic Module GTX connector uses Samtec's Micro High Speed Interfaces – QTH/QSH series 80-pin differential connectors. These connectors allow you to connect TAI Logic Module to other hardware in three ways: (i) directly mount a target board onto TAI Logic Module, (ii) stack multiple TAI Logic Modules together. All I/O connectors keep the same relative spacing between each other.

The specifications of the components needed to mate the external I/O connectors are as follows:

Top side (Terminal connector; use socket connector to mate)

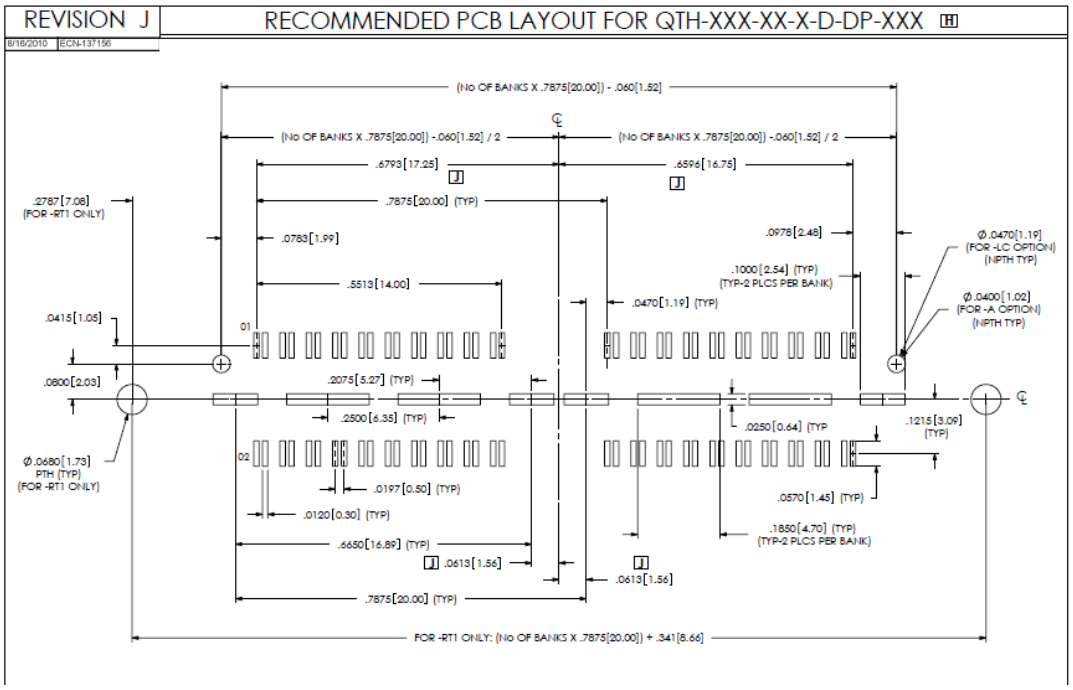
Manufacturer: Samtec

Part Number: QTH-040-05-F-D-DP-A or **QTH-040-01-F-D-DP-A**

Mates With: QSH-040-01-F-D-DP-A

We recommend using QSH-040-01-F-D-DP-A on the bottom side of the daughter board. The daughter board can be stacked on GTX connector on top side of TAI LM board. The figure below shows PCB layout recommendation for QTH-XXX-XX-X-D-DP-XXX.

Figure 9-5 QTH-XXX-XX-X-D-DP-XXX PCB layout recommendation



Bottom side (Socket connector; use terminal connector to mate)

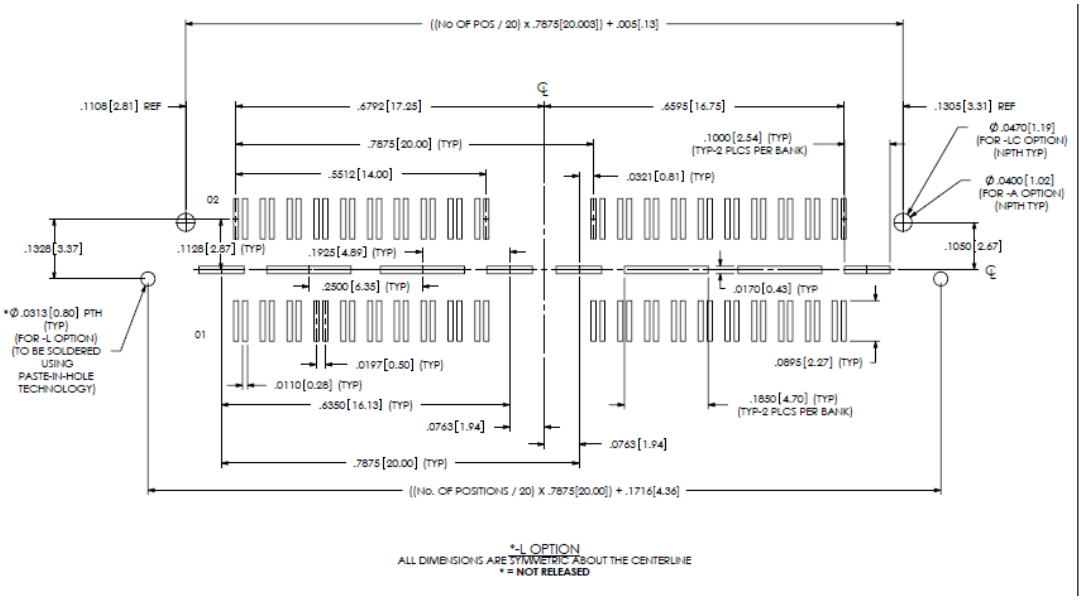
Manufacturer: Samtec

Part Number: QSH-040-01-F-D-DP-A

Mates With: **QTH-040-05-F-D-DP-A** or **QTH-040-01-F-D-DP-A**

We recommend using QTH-040-01-F-D-DP-A for designing daughter board; you can place QTH-040-01-F-D-DP-A on the top side of the daughter board. The daughter board can be stacked on GTX connector on bottom side of TAI LM board. The figure below shows PCB layout recommendation for QSH-XXX-XX-X-D-DP-XXX.

Figure 9-6 QSH-XXX-01-X-D-DP-XXX PCB layout recommendation



10. Care and Handling

Please take the following safety precautions in the care and handling of your TAI Logic Module:

10.1 Safety Precautions

- TAI Logic Module supports only 12V DC power inputs, through the ATX 4-pin Molex power connector. Applying any voltage above 12V may damage your TAI Logic Module.
- Before powering up the TAI Logic Module, you MUST install and use the fans which are included in the package to cool the FPGA devices on the TAI Logic Module.
- If you use OSC1 and/or OSC2 for clock inputs, please ensure that the oscillators are inserted with the right directions before powering up the TAI Logic Module.
- If the statuses of LED are not consistent with the LED default statuses described in the reference manual when you power on TAI Logic Module, please power down TAI Logic Module immediately to prevent further damage caused by possible power shorting.
- Do not plug or unplug the following components when TAI Logic Module is powered on:
  - Xilinx JTAG cable
  - Oscillators in the OSC socket
  - TAI LM connectors
  - SODIMM socket
- Do not adjust any of the switches on TAI Logic Module when it is powered on.
- If the daughter/mother boards that connect to TAI Logic Modules use different power source with TAI logic modules, the correct power on sequence is:
  - Connect your mother/daughter boards with TAI Logic Module when all of them are powered off
  - Power on TAI Logic Module
  - Download TAI Logic Module FPGA
  - Power on daughter/mother board

  And the correct power off sequence is:
  - Power off daughter/mother board
  - Power off TAI LM
- All V7 TAI LM FPGA I/O are directly drawn out to optimize application flexibility and performance, and thus do NOT have any protection. As such, any voltage above 1.8V or logic short may lead to permanent FPGA I/O pin damage (GTX I/O on V7 TAI LM can support up to 2.5V I/O voltage). Do not connect TAI Logic Module's I/Os to any target device with a voltage above 1.8V. Also make sure that all I/O connectors are securely connected before powering on.
- Do not insert daughter card mounted with 120-pin Samtec connector to 80-pin GTX

connector on V7 TAI LM. Likewise do not insert daughter card mounted with 80-pin GTX connector onto 120-pin Samtec connector on V7 TAI LM.

- When using GTX connector on V7 TAI LM, please make sure
  - The interface on daughter card matches with Virtex-7 GTX I/O requirement
  - There are 12 common I/Os in each GTX connector. The common I/Os support up to 1.8V. Refer To ‘V7 TAI LM Hardware Reference Manual’ for pin information.
- When probing TAI Logic Module I/Os with a logic analyzer or an oscilloscope, make sure that the probing tool does not touch adjacent pins, which may cause a short circuit, and that the test equipment has the same ground as that of TAI Logic Module.
- Do not place TAI Logic Module on any electrical conducting surface. TAI Logic Module’s spacers are used to pass both 12V and ground when multiple TAI Logic Modules are stacked together.
- Make sure that you work in an anti-static environment and observe all necessary anti-static handling precautions before unpacking and operating TAI Logic Module.
- Pressure and/or shaking may damage TAI Logic Module. High temperatures, high voltages, moisture, dust, static, and magnetization should also be avoided.
- TAI Logic Module should not be cleaned with or come into contact with any liquids.

10.2 Electrostatic Handling Considerations

- TAI Logic Module is packaged in antistatic or conductive containers. Before taking it out of its container, make sure the module is in a static-free workstation (location).
- TAI Logic Module must remain in its protective packaging unless it is being used in a static-free location. Transport the module only in its original container to avoid any potential damage to the pins.
- Before removing TAI Logic Module from its packaging, place the package on a grounded bench top, ensure a wrist strap is snugly worn around your wrist and is properly plugged into the ground receptacle, and then ground your hands by placing them in contact with the conductive bench top.
- A conductive shoe strap with conductive tiles or mats may be used instead of the wrist strap.
- Once you leave the workstation, you must still follow the previous procedures when you return to work with the module at the static-free location.
- Do not place TAI Logic Module in contact with plastic snow polystyrene foam, Styrofoam peanuts, or other high-dielectric materials, unless these materials have been treated with an antistatic agent (treated materials appear pink and generate less than 100V).
- Do not transport TAI Logic Module or store it in trays, tote boxes, vials, or other containers made of untreated plastic, unless it is protected within its original packaging.

▲ **NOTE:** Please save the original packaging for future shipment needs.

11. Appendix

11.1 JTAG information

Figure 11-1 JTAG Signal and Pin Number

JTAG Signal & Pin Num						
2. VREF	4.TMS	6.TCK	8.TDO	10.TDI	12.NC	14.NC
1. GND	3. GND	5. GND	7. GND	9. GND	11. GND	13. GND

Figure 11-2 Xilinx Platform Cable USB