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**Low Power Double Data Rate 5
(LPDDR5)**

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Contents

1	Scope.....	1
2	Overview	2
2.1	Features	2
2.2	Functional Description	2
2.2.1	Pad Definition and Description	2
2.2.2	Pin per byte	3
2.2.3	LPDDR5 Bank Architecture	4
2.2.3.1	Block diagram of bank configuration and Read operation outline	5
2.2.3.1.1	4 Bank / 4 Bank Groups Configuration.....	5
2.2.3.1.2	8 Bank Mode Configuration.....	6
2.2.3.1.3	16 Bank Mode Configuration.....	7
2.2.3.2	Address mapping.....	7
2.2.3.3	Bank architecture transition.....	7
2.2.3.4	Burst Operation	7
2.2.4	LPDDR5 SDRAM Addressing.....	13
2.2.5	Speed Grades	19
2.2.6	Burst Sequence	20
3	WCK Clocking.....	21
4	Initialization and Training	24
4.1	Power-up, Initialization and Power-off Procedure.....	24
4.1.1	Voltage Ramp and Device Initialization.....	24
4.1.2	Reset Initialization with Stable Power	28
4.1.3	Power-off Sequence.....	28
4.1.4	Uncontrolled Power-off Sequence.....	28
4.2	Training	29
4.2.1	ZQ Calibration	29
4.2.1.1	Calibration	29
4.2.1.1.1	Calibration During Powerup and Initialization.....	29
4.2.1.1.2	Background Calibration	29
4.2.1.1.3	Latching ZQ Calibration Results in Background Calibration Mode	30
4.2.1.1.4	Command-Based Calibration	31
4.2.1.1.5	Latching ZQ Calibration Results in Command-Based Calibration Mode	31
4.2.1.1.6	Maintaining Accurate Calibration - Background Calibration Mode.....	32
4.2.1.1.7	Maintaining Accurate Calibration - Command-Based Calibration Mode.....	32
4.2.1.1.8	Changing between Calibration Modes	33
4.2.1.1.8.1	Changing between Calibration Modes when DVFSQ is not active	33
4.2.1.1.8.2	Changing between Calibration Modes when DVFSQ is active	34
4.2.1.2	ZQ Stop Functionality.....	35
4.2.1.2.1	ZQ Resistor Sharing by Another Device(s)	35
4.2.1.2.1.1	ZQ Resistor Sharing in Background Calibration Mode	35
4.2.1.2.1.2	ZQ Resistor Sharing in Command-Based Calibration Mode	35
4.2.1.2.2	Stopping Background Calibration when DVFSQ is active	35
4.2.1.2.3	Stopping Background Calibration when VDDQ is Powered Off	36
4.2.1.3	ZQ Reset.....	37
4.2.1.4	Multi-die Package Considerations	38
4.2.1.4.1	Other Considerations in Background Calibration Mode	38
4.2.1.5	Other Considerations in Command-Based Calibration Mode	38
4.2.1.6	ZQ External Resistor, Tolerance, and Capacitive Loading	38

Contents (cont'd)

4.2.1.7	Flow Chart Examples	39
4.2.2	Command Bus Training	44
4.2.2.1	Command Bus Training Mode1	45
4.2.2.2	Command Bus Training Mode2	52
4.2.3	CA VREF Training.....	60
4.2.4	DQ VREF Training	60
4.2.5	WCK2CK Leveling	60
4.2.5.1	WCK2CK Leveling Mode (write-leveling called in LPDDR4)	60
4.2.5.2	WCK2CK Leveling Procedure and Related AC parameters	61
4.2.6	Duty Cycle Adjuster (DCA)	63
4.2.6.1	Duty Cycle Adjuster Range	63
4.2.6.2	The relationship between WCK waveform and DCA Code Change	64
4.2.6.3	The relationship between DCA Code Change and DQ output/RDQS timing	65
4.2.7	Duty Cycle Monitor (DCM)	66
4.2.7.1	DCM Functional Description.....	66
4.2.7.2	DCM Sequence	66
4.2.8	READ DQ Calibration.....	68
4.2.8.1	READ DQ Calibration Training Procedure.....	68
4.2.8.2	READ DQ Calibration Example	70
4.2.8.3	READ DQ Calibration after Power Down Exit	71
4.2.9	WCK-DQ Training	72
4.2.9.1	Training procedure	72
4.2.9.2	WCK-RDQS_t/Parity Training.....	73
4.2.9.3	FIFO Pointer Reset and Synchronism	74
4.2.9.4	Command constraints for Write/Read FIFO command.....	79
4.2.10	RDQS toggle mode	81
4.2.11	Enhanced RDQS training mode	82
5	Simplified LPDDR5 State Diagram	85
6	Mode Register Definition	90
6.1	Mode Register Assignment and Definition in LPDDR5 SDRAM	90
6.2	Mode Register Definition	93
6.2.1	Mode Register definition	93
7	Operating	137
7.1	Truth Table.....	137
7.1.1	Command Truth Table	137
7.2	WCK Operation	140
7.2.1	WCK2CK Synchronization operation	140
7.2.1.1	WCK2CK Synchronization	140
7.2.1.2	CAS Command with WCK2CK Synchronization Bits	140
7.2.1.3	WCK2CK Sync operation followed by a WRITE command	141
7.2.1.4	WCK2CK Sync operation followed by a READ command	143
7.2.1.5	WCK2CK Sync operation with CAS(WS_FAST=1)	146
7.2.1.6	Rank to rank WCK2CK Sync operation.....	148
7.2.2	WCK2CK SYNC Off Timing Definition	149
7.2.3	Write Clock Free Running mode	159
7.3	Row operation	162
7.3.1	Active Command	162
7.3.1.1	8 Bank mode SDRAM Operation	164
7.3.1.2	BG mode SDRAM Operation	164

Contents (cont'd)

7.3.2	Pre-Charge Operation	165
7.3.2.1	Pre-Charge Operation	165
7.3.2.2	Auto-Precharge Operation	169
7.3.2.2.1	Delay time from Write to Read with Auto Precharge	170
7.3.2.2.2	Burst Read with Auto-Precharge	171
7.3.2.2.3	Burst Write with Auto-Precharge	172
7.4	Read/Write Operation.....	174
7.4.1	Read and Write Access Operations.....	174
7.4.2	Read Preamble and Postamble	174
7.4.3	Burst Read Operation.....	174
7.4.3.1	Read Timing.....	174
7.4.3.2	Read to Read Operation without additional WCK2CK-sync	176
7.4.3.3	Read to Read Operation with additional WCK2CK-sync	177
7.4.3.4	Read operation followed by write operation	177
7.4.4	READ Burst end to PRECHARGE Delay (tRBTP).....	178
7.4.5	RDQS Mode	179
7.4.5.1	RDQS Timing	179
7.4.5.2	RDQS Related Functionalities	180
7.4.5.3	Mode Registers for RDQS	181
7.4.5.4	RDQS Pattern Definition	182
7.4.6	Write Preamble and Postamble	185
7.4.7	Burst Write Operation.....	185
7.4.7.1	Write Timing	185
7.4.7.2	Write to Write Operation without additional WCK2CK-sync	187
7.4.7.3	Write to Write Operation with additional WCK2CK-sync	188
7.4.7.4	Write operation followed by read operation	188
7.4.8	Read and Write Latency	189
7.4.8.1	Read and Read-to-Precache Latencies	189
7.4.8.2	Write Latency	190
7.4.8.3	Write Recovery time	193
7.4.9	Masked Write	195
7.4.10	Data Mask (DM) and Data Bus Inversion (DBI-DC) Function	200
7.4.10.1	DMI Pin Behavior with Write Related Commands.....	201
7.4.10.2	DMI Pin Behavior with Read Related Commands	203
7.5	Refresh operation	204
7.5.1	Refresh command	204
7.5.2	Refresh Requirement	211
7.5.3	Self Refresh Operation	212
7.5.3.1	Power Down Entry and Exit during Self refresh.....	214
7.5.3.2	Command input Timing after Power Down Exit during Self Refresh.....	216
7.5.3.3	Self Refresh AC Timing Table	217
7.5.3.4	MRR, MRW, RFF, WFF, RDC, MPC Command during tXSR	218
7.5.4	Partial Array Self Refresh (PASR)	219
7.5.4.1	PASR Segment Masking.....	219
7.5.5	Power Down	220
7.5.6	Power-Down Entry and Exit	220
7.5.7	Sleep Mode	226
7.6	Other Operation.....	228
7.6.1	Mode Register Read	228

Contents (cont'd)

7.6.1.1	MRR after Read and Write Command	230
7.6.1.2	MRR after Power-Down Exit.....	232
7.6.2	Mode Register Write	233
7.6.2.1	Mode Register Write Disable control for Byte Mode device	233
7.6.3	Frequency Set Point.....	234
7.6.3.1	Frequency set point update Timing	235
7.6.3.2	Frequency set point update Timing for DVFSQ and DVFSQ	236
7.6.4	On-Die Termination (ODT)	239
7.6.4.1	On-Die Termination for Command/Address Bus.....	239
7.6.4.1.1	ODT Mode Register and ODT State Table for Command/Address Bus	239
7.6.4.1.2	ODT Mode Register and ODT Characteristics for Command/Address Bus	241
7.6.4.1.3	ODT update time for Command/Address Bus	242
7.6.4.2	On-Die Termination for Data Bus	243
7.6.4.2.1	ODT Mode Register for Data Bus	243
7.6.4.2.2	Asynchronous ODT for Data Bus	243
7.6.4.2.3	ODT Mode Register and ODT Characteristics for Data Bus.....	245
7.6.4.3	On-Die Termination for WCK_t and WCK_c	247
7.6.4.3.1	ODT Mode Register for WCK_t/c	247
7.6.4.3.2	ODT during WCK2CK training	247
7.6.5	Non-target ODT	248
7.6.5.1	Non-target DRAM ODT control	249
7.6.5.2	Asynchronous NT-ODT	252
7.6.5.3	Timing diagram of Write case	256
7.6.5.4	Timing diagram of Read case	257
7.6.6	Input Clock Stop and Frequency Change.....	257
7.6.7	V _{REF} Current Generator (VRCG)	258
7.6.8	Thermal Offset	259
7.6.9	Temperature Sensor.....	259
7.6.10	Multi-Purpose Command (MPC)	261
7.6.11	tWCK2DQ Interval Oscillator	261
7.6.11.1	Interval Oscillator Matching Error	264
7.7	Specific features, Reliability & Power-optimization	265
7.7.1	Dynamic Voltage and Frequency Scaling (DVFS)	265
7.7.1.1	DVFSQ Mode	265
7.7.1.2	DVFSQ Mode.....	267
7.7.1.2.1	DVFSQ High-to-Low Transition	268
7.7.1.2.2	DVFSQ Low-to-High Transition without VRCG during VDDQ ramp	269
7.7.1.2.3	DVFSQ Low-to-High Transition with VRCG	270
7.7.2	Data Copy Low Power Function.....	271
7.7.2.1	Write Data Copy Function	271
7.7.2.2	Read Data Copy Function.....	273
7.7.2.3	Read Data Copy Function with Read DBI Enable	274
7.7.3	Write X operation	274
7.7.4	Post Package Repair (PPR)	278
7.7.4.1	Guard Key Protection	279
7.7.4.2	PPR Fail Row Address Repair	280
7.7.5	Target Row Refresh	281
7.7.5.1	TRR Mode Operation	282
7.7.6	Decision Feedback Equalization (DFE).....	283

Contents (cont'd)

7.7.7	Link ECC	284
7.7.8	Single-ended mode for Clock, Write Clock and RDQS	291
7.7.8.1	Restriction of Single-ended mode	292
7.7.8.2	Switching sequence between Single-ended and Differential	293
7.7.8.3	VRCG Enable timing	294
7.7.8.4	AC parameters for Single Ended (SE)	295
7.7.8.5	Command bus training procedure	295
8	Command Constraint and AC timing	296
8.1	Effective Burst Length (BL/n) Definition	296
8.1.1	Auto Precharge Command Timing Constraints	304
8.1.2	CAS Command Timing Constraints	308
8.1.3	Training related timing constraints.....	317
8.1.4	MRR/MRW Timing Constraints	318
8.1.5	Rank to Rank Command Timing Constraints	320
9	AC Timing	323
9.1	Core AC Timing Parameters by Speed Grade	323
9.1.1	Timing table for x16, DVFSC Disabled & Link ECC Disabled	323
9.1.1.1	Timing Table for x8 (Byte Mode) SDRAM	324
9.1.1.2	Timing Table for Link ECC is enabled	325
9.1.1.3	Timing Table for x8 (Byte Mode) SDRAM and Link ECC is enabled..	326
9.1.2	Timing table for x16, DVFSC Enabled & Link ECC Disabled	327
9.1.2.1	Timing Table for x8 (Byte Mode) SDRAM	327
9.2	Core AC Temperature derating for AC Timing	328
10	Absolute Maximum DC Ratings	329
11	AC and DC Operating Condition	330
11.1	Recommended DC Operating Conditions	330
11.2	Input Leakage Current.....	332
11.3	Input/Output Leakage Current	332
11.4	Operating Temperature Range	332
11.4.1	Operating Temperature Range (Automotive spec addendum only)	333
11.5	Electrostatic Discharge Sensitivity Characteristics	333
12	AC and DC Input/Output Measurement levels	334
12.1	1.05V High speed LVCMOS	334
12.1.1	Standard specifications	334
12.1.2	Input Level for Reset_n	334
12.1.3	Input Level for CS	334
12.1.4	AC Overshoot / Undershoot	334
12.1.4.1	AC Overshoot / Undershoot	334
12.1.4.2	AC Overshoot / Undershoot for LVSTL	334
12.2	Differential Input Voltage.....	335
12.2.1	Differential Input Voltage for CK.....	335
12.2.1.1	Peak Voltage Calculation Method	336
12.2.1.2	Single ended Input Voltage for CK	337
12.2.1.3	Differential Input Slew Rate Definition for CK.....	338
12.2.1.4	Differential Input Cross Point Voltage for CK	339
12.2.2	Differential Input Voltage for WCK.....	340
12.2.2.1	Peak Voltage Calculation Method	341
12.2.2.2	Single ended Input Voltage for WCK	342
12.2.2.3	Differential Input Slew Rate Definition for WCK.....	343

Contents (cont'd)

12.2.2.4	Differential Input Cross Point Voltage for WCK	344
12.3	Output Slew Rate	345
12.3.1	Single Ended Output Slew Rate.....	345
12.3.2	Differential Output Slew Rate	346
12.4	Driver Output Timing Reference load.....	346
12.5	Single Ended WCK	347
12.5.1	Single Ended WCK input definitions	347
12.5.2	Single Ended Mode WCK Pulse Definitions	347
12.6	Single Ended CK	348
12.6.1	Single Ended CK input definitions	348
12.6.2	Single Ended Mode CK Pulse Definitions.....	349
12.7	Read Timing tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation	350
12.7.1	tLZ(RDQS) tLZ(DQ) tHZ(RDQS) tHZ(DQ).....	350
12.7.1.1	tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment)	350
12.7.1.2	tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)	352
13	Input / Output Capacitance	355
14	IDD Specification Parameters and Test Conditions	356
14.1	IDD Measurement Conditions.....	356
14.2	IDD Specifications	366
15	Electrical Characteristics and AC Timing	370
15.1	Clock Specification.....	370
15.1.1	Definition for tCK(avg) and nCK.....	370
15.1.2	Definition for tCK(abs)	370
15.1.3	Definition for tCH(avg) and tCL(avg)	370
15.1.4	Definition for tCH(abs) and tCL(abs)	371
15.1.5	Definition for tJIT(per).....	371
15.1.6	Definition for tJIT(cc)	371
15.1.7	Clock Timing	371
15.2	Write Clock Specification	373
15.2.1	Definition for tWCK(avg) and nWCK.....	373
15.2.2	Definition for tWCK(abs)	373
15.2.3	Definition for tWCH(avg) and tWCL(avg)	373
15.2.4	Definition for tWCH(abs) and tWCL(abs)	374
15.2.5	Definition for tJIT(per).....	374
15.2.6	Definition for tJIT(cc)	374
15.2.7	Definition for tERR(2per).....	374
15.2.8	Definition for tERR(3per).....	374
15.2.9	Definition for tERR(4per).....	375
15.2.10	Write Clock Timing	375
15.3	tWCK2DQ AC parameters	377
15.4	DQ Tx Jitter Spec	377
15.5	CS Rx specification.....	380
15.5.1	CS Rx mask and single pulse definition for Synchronous mode	380
15.5.2	CS Rx input level definition for Asynchronous mode	381
15.5.3	Synchronous mode CS Rx mask / single pulse spec and Asynchronous mode CS input ...	382
15.6	CA Rx specification	383
15.6.1	CA Rx mask and single pulse definition	383
15.6.2	CA Rx mask and single pulse spec.	385
15.7	DQ, DMI, Parity and DBI Rx specification	386

Contents (cont'd)

15.7.1	DQ, DMI, Parity and DBI Rx mask and single pulse definition.....	386
15.7.2	DQ, DMI, Parity and DBI Rx mask and single pulse spec.....	389
15.8	Pull Up/Pull Down Driver Characteristics and Calibration	390
15.9	Output Driver and Termination Resistance Temperature and Voltage Sensitivity	391
16	Die configuration, Package ballout & Pin Definition	393
16.1	Package Configuration	393
16.1.1	Package Considerations for Byte-Mode Devices.....	393
16.2	Pad Order.....	394
16.3	Package Ballout	395
16.4	Package Die Layout	395
16.5	Package Configuration	395
16.6	ZQ Wiring	396

Figures

Figure 1 — BG Mode Configuration Example (One Channel Shown).....	5
Figure 2 — 8B Mode Configuration Example (One Channel Shown)	6
Figure 3— 16B Mode Configuration Example (One Channel Shown)	7
Figure 4 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=16.....	8
Figure 5 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=32.....	9
Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32	10
Figure 7 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=16	11
Figure 8 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=32	12
Figure 9 — Clocking and Interface Relationship	21
Figure 10 — Block Diagram of an example system.....	22
Figure 11 — DRAM internal WCK2CK auto-sync process	23
Figure 12 — Requirement for Voltage Ramp Control	25
Figure 13 — Power Ramp and Initialization Sequence	26
Figure 14 — Background ZQ Calibration Timing	30
Figure 15 — Background to Command-based Switching when DVFSQ is not active.....	33
Figure 16 — Command-based to Background Switching when DVFSQ is not active	33
Figure 17 — Background to Command-based Switching when DVFSQ is active.....	34
Figure 18 — Command-based to Background Switching when DVFSQ is active.....	34
Figure 19 — ZQCal Timing	37
Figure 20 — Initialization to Background Calibration Flow Chart, no DVFSQ support.....	39
Figure 21 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 1 (check Master)	40
Figure 22 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 2 (ignore Master).....	41
Figure 23 — Initialization to Background Calibration Flow Chart, with DVFSQ support	42
Figure 24 — Initialization to Command-based Calibration Flow Chart, with DVFSQ support	43
Figure 25 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change)	48
Figure 26 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Fixed WCK Frequency)	49
Figure 27 — Exiting Command Bus Training Mode	50
Figure 28 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (WCK Frequency change)	55
Figure 29 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Fixed WCK Frequency)	56
Figure 30 — CA pattern Input/Output to Vref setting Input.....	57
Figure 31 — Consecutive CA training pattern Input/Output	57
Figure 32 — Exiting Command Bus Training Mode	58

Contents (cont'd)

Figure 33 — WCK2CK Leveling Entry	61
Figure 34 — WCK2CK Leveling Exit	61
Figure 35 — Relationship between WCK waveform and DCA Code Change (Example)	64
Figure 36 — Relationship between WCK waveform and DQS_t/c and DQ output (Example)	65
Figure 37 — DCM timing example	67
Figure 38 — Read DQ Calibration Timing: Read to Read DQ Calibration	69
Figure 39 — Read DQ Calibration Timing: Read DQ Calibration to Read DQ Calibration	70
Figure 40 — READ DQ CALIBRATION following Power Down State	71
Figure 41 — Consecutive Write FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1	75
Figure 42 — Consecutive Read FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1	76
Figure 43 — Consecutive Write FIFO Operation timing: Parity Data input for BG mode: CKR (WCK vs. CK) = 4:1.....	77
Figure 44 — Consecutive Read FIFO Operation timing: Parity Data output for BG mode: CKR (WCK vs. CK) = 4:1	78
Figure 45 — Write FIFO to Read FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1	79
Figure 46 — Read FIFO to Write FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1	80
Figure 47 — RDQS toggle mode entry timing example.....	81
Figure 48 — RDQS toggle mode exit timing example	82
Figure 49 — Enhanced RDQS training mode entry timing	83
Figure 50 — Enhanced RDQS training mode exit timing	83
Figure 51 — Read operation during Enhanced RDQS training mode	84
Figure 52 — LPDDR5: Simplified Bus Interface State Diagram	86
Figure 53 — Sub-State Diagram-1 related with MRR, MRW, CAS, WFF, RFF, RDC and MPC Command	87
Figure 54 — Sub-State Diagram-2: related with MPC State	88
Figure 55 — Aligned WCK/2_0 to CK (Left) & Miss-Aligned WCK/2_0 to CK (Right).....	140
Figure 56 — LPDDR5 WCK2CK Sync operation by CAS command with WCK2CK Sync operand enabled	141
Figure 57 — WCK2CK Sync operation followed by a WRITE command	142
Figure 58 — WCK2CK Sync operation followed by a READ command	143
Figure 59 — Minimum latency WCK2CK Sync operation for CAS(WS_FAST=1)	146
Figure 60 — WCK2CK sync operation for Read Operation with CAS(WS_FAST=1) with command gap	146
Figure 61 — Minimum gap rank to rank read operation with WCK2CK Sync after completing DQ burst in one rank.....	148
Figure 62 — Simultaneous WCK2CK Sync process for multi-ranks (especially two ranks)	148
Figure 63 — Write sync off timing BG Mode, CKR (WCK vs. CK) = 4:1, BL=16.....	154
Figure 64 — Write sync off timing (WCK2CK Sync is expired), BG Mode, CKR (WCK vs. CK) = 4:1, BL=16	154
Figure 65 — Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32.....	155
Figure 66 — Masked Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16	155
Figure 67 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16, tRPST=2.5nWCK	156
Figure 68 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR = 4:1, BL=16, tRPST=2.5nWCK	156
Figure 69 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16, tRPST=4.5nWCK	157
Figure 70 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR = 4:1, BL=16, tRPST=4.5nWCK	157
Figure 71 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=2.5nWCK	158
Figure 72 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=4.5nWCK	158
Figure 73 — WCK free running mode starting with WCK2CK-sync operation followed by a write command.....	160
Figure 74 — Figure 2. WCK free running mode starting with WCK2CK-sync operation followed by a read command	160

Contents (cont'd)

Figure 75 — CAS Command based WCK Buffer off following write command min(tWCKOFF) = RU(max(tWCKDQO)/tCK) + BL/n + 1, where n=8 in WCK:CK=4:1 mode and n=4 in WCK:CK=2:1 mode	161
Figure 76 — CAS Command based WCK Buffer off following read command min(tWCKOFF) = RU(max(tWCKDQO)/tCK) + BL/n + 1, where n=8 in WCK:CK=4:1 mode and n=4 in WCK:CK=2:1 mode	161
Figure 77 — Activate command for 8B/16B mode	162
Figure 78 — Activate Command with Activate1 and Activate-2 spacing for 8B/16B mode.....	163
Figure 79 — Activate command for BG mode	163
Figure 80 — 8 Bank tFAW Timing	164
Figure 81 — BG mode tFAW timing	164
Figure 82 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=16.....	167
Figure 83 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=32.....	168
Figure 84 — Burst Write Followed by Precharge: 16B Mode, CKR = 4:1, BL=16.....	169
Figure 85 — Command Input Timing with RAS lock	170
Figure 86 — Delay time from Write to Read with Auto Precharge: 16B mode.....	170
Figure 87 — Burst Read with Auto-Precharge: 16B mode	171
Figure 88 — Burst Write with Auto- Precharge: 16B mode	172
Figure 89 — Burst Read Operation	175
Figure 90 — Back to back read operation with tCCD(min) = 2tCK.....	176
Figure 91 — Back to back read operation with tCCD ≤ RL + BL/n	176
Figure 92 — Back to back read operation requiring a new WCK2CK-sync sequence.....	177
Figure 93 — Read operation followed by write operation without additional WCK2CK-sync sequence ..	177
Figure 94 — Read operation followed by write operation with additional WCK2CK-sync sequence	177
Figure 95 — Example of READ burst end to PRECHARGE command delay for same banks	178
Figure 96 — Example of READ burst end to PRECHARGE command delay for same banks	178
Figure 97 — Example of READ burst end to PRECHARGE command delay for same banks	178
Figure 98 — Example of READ burst end to PRECHARGE command delay for same banks	179
Figure 99 — Read timing with RDQS and related timing parameters	180
Figure 100 — 4 All the possible types of RDQS	181
Figure 101 — READ16 to READ16 2nCK Gap Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK	182
Figure 102 — BG Mode Read32 Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK	182
Figure 103 — Burst Write Operation.....	186
Figure 104 — Back to back write operation with tCCD(min) = 2tCK	187
Figure 105 — Back to back write operation with tCCD ? WL + BL/n (n=4 at WCK:CLK=2:1, n=8 at WCK:CLK=4:1).....	187
Figure 106 — Back to back write operation requiring a new WCK2CK-sync sequence	188
Figure 107 — Write operation followed by read operation	188
Figure 108 — Write Latency Timing	192
Figure 109 — Write Recovery Latency Timing	194
Figure 110 — Masked Write Command – Same Bank Operation Timing without any other DQ operation commands in 4 Bank/4BG or 16 Bank mode.....	196
Figure 111 — Masked Write Command – Different Bank Group Operation Timing in 4 Bank/4BG mode	197
Figure 112 — Masked Write Command – Different Bank Operation Timing in 8 Bank Mode (BL32 only)	198
Figure 113 — Masked Write Command – 16 Bank Mode (WCK:CK = 2:1)	199
Figure 114 — All-Bank Refresh Operation	208
Figure 115 — Per-Bank Refresh Operation	208
Figure 116 — Postponing Refresh Commands (Example).....	210
Figure 117 — Pulling-in Refresh Commands (Example).....	211
Figure 118 — Self Refresh Entry/Exit Timing	213
Figure 119 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit.....	214

Contents (cont'd)

Figure 120 — Self Refresh Entry with PD="1" Timing	215
Figure 121 — Command input timing after Power Down Exit during Self Refresh	216
Figure 122 — MRR, MRW, WFF, RFF, RDC and MPC Commands Issuing Timing during tXSR	218
Figure 123 — Basic Power-Down Entry and Exit Timing	221
Figure 124 — Read and Read with Auto Precharge to Power-Down Entry	221
Figure 125 — Write and Mask Write to Power-Down Entry.....	222
Figure 126 — Write with Auto Precharge and Mask Write with Auto Precharge to Power-Down Entry ..	222
Figure 127 — Refresh Entry to Power-Down Entry	223
Figure 128 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit.....	223
Figure 129 — Activate Command to Power-Down Entry.....	223
Figure 130 — Precharge Command to Power-Down Entry.....	224
Figure 131 — Mode Register Read to Power-Down Entry	224
Figure 132 — Mode Register Write to Power-Down Entry	224
Figure 133 — Multi Purpose Command for Start ZQ Calibration to Power-Down Entry	225
Figure 134 — Deep Sleep Mode state diagram	226
Figure 135 — Deep Sleep Mode Entry in IDLE state and Exit Timing	227
Figure 136 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing	227
Figure 137 — Mode Register Read Operation	229
Figure 138 — READ to MRR Timing	230
Figure 139 — WRITE to MRR Timing.....	231
Figure 140 — MRR Following Power-Down	232
Figure 141 — Mode Register Write Timing.....	233
Figure 142 — Frequency Set Point Switching Timing	235
Figure 143 — Training Three Frequency Set-Points	237
Figure 144 — Switching Between Two Trained Frequency Set-Points (Example)	238
Figure 145 — Switching to a Third Trained Frequency Set-Point (Example).....	238
Figure 146 — Functional Representation of Command/Address bus ODT	239
Figure 147 — On Die Termination for Command/Address Bus.....	241
Figure 148 — ODT for Command/Address setting update timing	242
Figure 149 — Functional Representation of Data bus ODT	243
Figure 150 — Asynchronous ODTon/ODToff Timing	245
Figure 151 — On Die Termination for Data Bus	245
Figure 152 — Functional Representation of WCK ODT	247
Figure 153 — DRAM ODT configuration of Non-target DRAM ODT mode	248
Figure 154 — ODT Control on Non-target DRAM for Write.....	256
Figure 155 — ODT Control on Non-target DRAM for Read	257
Figure 156 — VRCG Enable Timing	258
Figure 157 — VRCG Disable Timing	258
Figure 158 — Temp Sensor Timing	260
Figure 159 — Interval oscillator offset	264
Figure 160 — DVFS High (VDD2H) to Low (VDD2L) Transition	265
Figure 161 — DVFS Low (VDD2L) to High (VDD2H) Transition	266
Figure 162 — Example DVFS Block Diagram.....	266
Figure 163 — DVFSQ High (VDDQ) to Low Transition Flow Chart.....	268
Figure 164 — DVFSQ High (VDDQ) to Low Transition Timing	268
Figure 165 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart without VRCG.....	269
Figure 166 — DVFSQ Low (VDDQ) to High Transition Timing without VRCG during VDDQ ramp	269
Figure 167 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart with VRCG.....	270
Figure 168 — DVFSQ Low (VDDQ) to High Transition with VRCG	270
Figure 169 — Data copy granularity and reference data configuration in BL32.....	271
Figure 170 — Example of Write Data Copy Function Timing Diagram	273
Figure 171 — Example of Read Data Copy Function Timing Diagram	274
Figure 172 — Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16.....	275

Contents (cont'd)

Figure 173 — Consecutive Write and Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16.....	276
Figure 174 — Consecutive Write and Write X timing at Sync: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16.....	276
Figure 175 — Write w/ write X issuing timing at Sync state.....	277
Figure 176 — CAS_WRX Command timing after WCK2CK sync state is expired.....	277
Figure 177 — Guard Key Timing Diagram.....	279
Figure 178 — PPR Timing	280
Figure 179 — Target Row Refresh Mode	283
Figure 180 — DFE pre-drive requirement.....	284
Figure 181 — Write command showing link ECC transfer	285
Figure 182 — Read command showing Link ECC transfer	285
Figure 183 — Data flow on a memory Write operation.....	289
Figure 184 — Data flow on a memory Read operation	290
Figure 185 — SE to Differential CK and Write DQS -FSP Switching Timing	293
Figure 186 — Differential to SE CK and Write DQS -FSP Switching Timing	293
Figure 187 — VRCG status change to high current mode: Single-ended Clock Case	294
Figure 188 — VRCG status change to high current mode: Differential Clock Case	294
Figure 189 — Write Timing Diagram (BG mode, CKR=4:1, BL32) Example for BL/n, BL/n_min and BL/n_max	297
Figure 190 — DC Voltage Range	331
Figure 191 — VDDQ Tolerance Definition in Allowable Range.....	331
Figure 192 — Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component).....	331
Figure 193 — Overshoot and Undershoot Definition	335
Figure 194 — CK Differential Input Voltage.....	335
Figure 195 — Definition of differential Clock Peak Voltage	336
Figure 196 — Clock Single ended Input Voltage	337
Figure 197 — Differential Input Slew Rate Definition for CK_t, CK_c	338
Figure 198 — Differential Input Slew Rate Definition for CK_t, CK_c	339
Figure 199 — WCK Differential Input Voltage	340
Figure 200 — Definition of differential WCK Peak Voltage.....	341
Figure 201 — WCK Single ended Input Voltage.....	342
Figure 202 — Differential Input Slew Rate Definition for WCK_t, WCK_c	343
Figure 203 — Vix Definition (WCK)	344
Figure 204 — Single Ended Output Slew Rate Definition	345
Figure 205 — Differential Output Slew Rate Definition.....	346
Figure 206 — Driver Output Reference Load for Timing and Slew Rate	346
Figure 207 — Single Ended Mode WCK input Voltage	347
Figure 208 — Single Ended Mode WCK pulse.....	347
Figure 209 — Single Ended Mode CK input Voltage.....	348
Figure 210 — Single Ended Mode CK pulse	349
Figure 211 — tLZ(RDQS) method for calculating transitions and end point	350
Figure 212 — tHZ(RDQS) method for calculating transitions and end point	351
Figure 213 — tLZ(DQ) method for calculating transitions and end point	352
Figure 214 — tHZ(DQ) method for calculating transitions and end point	353
Figure 215 — DQ to RDQS 0UI read data timing example	377
Figure 216 — DQ to RDQS 3UI read data timing example	377
Figure 217 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 0 UI mismatch	378
Figure 218 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 3UI mismatch	378
Figure 219 — Synchronous mode CS Rx Mask definition.....	380
Figure 220 — Synchronous mode CS Rx single pulse definition	380

Contents (cont'd)

Figure 221 — Synchronous mode CS Timings at the DRAM Pin.....	381
Figure 222 — Asynchronous mode ViHPD and ViLPD at Power Down Exit.....	381
Figure 223 — CA Rx Mask definition	383
Figure 224 — CA Rx single pulse definition	383
Figure 225 — CA timings at the DRAM Pins	384
Figure 226 — DQ, DMI, Parity and DBI Rx Mask definition	386
Figure 227 — DQ to WCK tWCK2DQI and tDQ2DQ Timings at the DRAM pins referenced from the internal latch	387
Figure 228 — DQ, DMI, Parity and DBI Rx single pulse definition	388
Figure 229 — Example of rank assignment for a single-channel dual-rank package	393

Tables

Table 1 — Pad Definition and Description	2
Table 2 — Pins Per-Byte Signal List/Description for Link Protection disabled	3
Table 3 — Pins Per-Byte Signal List/Description for Link Protection enabled.....	3
Table 4 — Address Array mapping	7
Table 5 — LPDDR5 SDRAM x16 mode Addressing for BG Mode (4Banks/4Bank Groups)	13
Table 6 — LPDDR5 SDRAM x8 mode Addressing for BG Mode	14
Table 7 — LPDDR5 SDRAM x16 mode Addressing for 8B Mode.....	15
Table 8 — LPDDR5 SDRAM x8 mode Addressing for 8B Mode.....	16
Table 9 — LPDDR5 SDRAM x16 mode Addressing for 16B Mode.....	17
Table 10 — LPDDR5 SDRAM x8 mode Addressing for 16B Mode	18
Table 11 — LPDDR5 Speed Grades	19
Table 12 — Burst Sequence for READ (8 bank mode)	20
Table 13 — Burst Sequence for READ (4 bank/ 4Bank Group mode or 16Bank mode)	20
Table 14 — Burst sequence for Write	20
Table 15 — Example Clock and Interface Signal Frequency Relationship	22
Table 16 — MRS Default setting	24
Table 17 — Voltage Ramp Conditions.....	24
Table 18 — Initialization Timing Parameters	27
Table 19 — Reset Timing Parameter	28
Table 20 — Power Supply Conditions	28
Table 21 — Power Supply Conditions	28
Table 22 — ZQ Calibration Timing Parameters.....	36
Table 23 — Mapping of CA Input pin and DQ Output pin.....	45
Table 24 — Command Bus Training Mode1 AC Timing Table	51
Table 25 — Mapping of MR12 OP Code and DQ Numbers	53
Table 26 — Mapping of CA Input pin and DQ Output pin.....	53
Table 27 — Command Bus Training Mode2 AC Timing Table	59
Table 28 — WCK2CK Leveling Timing Parameters	62
Table 29 — DCA Range	63
Table 30 — Duty Cycle Adjuster Range	63
Table 31 — Duty cycle monitor timing	67
Table 32 — Invert Mask or output data fix0 Assignments in X16 Mode	69
Table 33 — Invert Mask or output data fix0 Assignments in X8 Mode	69
Table 34 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DQ	70
Table 35 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DMI	71
Table 36 — Enhanced RQDS training mode entry and exit timings.....	84
Table 37 — Mode Register Assignment in LPDDR5 SDRAM	90
Table 38 — MR0 Register Information (MA [7:0] = 00 _H)	93
Table 39 — MR0 definition.....	93
Table 40 — MR1 Register Information (MA[5:0] = 01 _H).....	94
Table 41 — MR1 definition.....	94

Contents (cont'd)

Table 42 — MR2 Register Information (MA[7:0] = 02 _H).....	96
Table 43 — MR2 Definition	96
Table 44 — MR3 Register Information (MA[7:0] = 03 _H).....	98
Table 45 — MR3 Definition	98
Table 46 — MR4 Register Information (MA[7:0] = 04 _H).....	99
Table 47 — MR4 Definition	99
Table 48 — MR5 Register Information (MA[7:0] = 05 _H).....	100
Table 49 — MR5 Definition	100
Table 50 — MR6 Register Information (MA[7:0] = 06 _H).....	100
Table 51 — MR6 Definition	100
Table 52 — MR7 Register Information (MA[7:0] = 07 _H).....	100
Table 53 — MR7 Definition	100
Table 54 — MR8 Register Information (MA[7:0] = 08 _H).....	101
Table 55 — MR8 Definition	101
Table 56 — MR9 Register Information (MA[7:0] = 09 _H).....	101
Table 57 — MR9 Definition	101
Table 58 — MR10 Register Information (MA [7:0] = 0A _H)	102
Table 59 — MR10 Definition	102
Table 60 — MR11 Register Information (MA[7:0] = 0B _H)	103
Table 61 — MR11 Definition	103
Table 62 — MR12 Register Information (MA[5:0] = 0C _H)	104
Table 63 — MR12 Definition	104
Table 64 — MR12 V _{REF} (CA) Settings	105
Table 65 — MR13 Register Information (MA[5:0] = 0D _H)	106
Table 66 — MR13 Definition	106
Table 67 — MR14 Register Information (MA[7:0] = 0E _H)	107
Table 68 — MR14 definition.....	107
Table 69 — MR14 V _{REF} (DQ[7:0]) Settings	108
Table 70 — MR15 Register Information (MA[7:0] = 0F _H)	109
Table 71 — MR15 definition.....	109
Table 72 — MR15 VREF(DQ[15:8]) Settings	110
Table 73 — MR16 Register Information (MA[5:0] = 10 _H).....	111
Table 74 — MR16 definition.....	111
Table 75 — MR17 Register Information (MA[5:0] = 11 _H).....	112
Table 76 — MR17 definition.....	112
Table 77 — MR18 Register Information (MA[7:0] = 12 _H).....	113
Table 78 — MR18 Definition.....	113
Table 79 — MR19 Register Information (MA[7:0] = 13 _H).....	114
Table 80 — MR19 Definition.....	114
Table 81 — MR20 Register Information (MA[7:0] = 14 _H).....	115
Table 82 — MR20 definition.....	115
Table 83 — MR21 Register Information (MA[7:0] = 15 _H).....	116
Table 84 — MR21 Definition.....	116
Table 85 — MR22 Register Information (MA[7:0] = 16 _H).....	117
Table 86 — MR22 Definition	117
Table 87 — MR23 Register Information (MA[5:0] = 17H).....	117
Table 88 — MR23 Definition	117
Table 89 — Row Address of Masked Segment for x16 Mode.....	117
Table 90 — Row Address of Masked Segment for x8 Mode	117
Table 91 — MR24 Register Information (MA[5:0] = 18H).....	118
Table 92 — MR24 Definition	118
Table 93 — MR25 Register Information (MA[7:0] = 19 _H).....	119
Table 94 — MR25 Definition	119
Table 95 — MR26 Register Information (MA[7:0] = 1A _H)	119

Contents (cont'd)

Table 96 — MR26 definition.....	119
Table 97 — MR27 Register Information (MA[7:0] = 1B _H)	120
Table 98 — MR27 Definition	120
Table 99 — MR28 Register Information (MA[7:0] = 1C _H)	121
Table 100 — MR28 Definition	121
Table 101 — MR29 Register Information (MA[7:0] = 1DH)	122
Table 102 — MR29 Definition	122
Table 103 — MR30 Register Information (MA[5:0] = 1E _H)	123
Table 104 — MR30 Definition.....	123
Table 105 — MR31 Register Information (MA[7:0] = 1F _H)	124
Table 106 — MR31 Definition	124
Table 107 — MR31 Invert Register Pin Mapping	124
Table 108 — MR32 Register Information (MA[7:0] = 20 _H).....	125
Table 109 — MR32 definition	125
Table 110 — MR32 Invert Register Pin Mapping	125
Table 111 — MR33 Register Information (MA[7:0] = 21 _H).....	126
Table 112 — MR33 Definition	126
Table 113 — MR34 Register Information (MA[7:0] = 22 _H).....	126
Table 114 — MR34 Definition	126
Table 115 — MR35 Register Information (MA[7:0] = 23 _H).....	127
Table 116 — MR35 Definition	127
Table 117 — MR36 Register Information (MA[7:0] = 24 _H).....	127
Table 118 — MR36 Definition	127
Table 119 — MR37 Register Information (MA[7:0] = 25 _H).....	128
Table 120 — MR37 Definition	128
Table 121 — MR38 Register Information (MA[7:0] = 26 _H).....	129
Table 122 — MR38 Definition	129
Table 123 — MR39 Register Information (MA[7:0] = 27 _H).....	129
Table 124 — MR39 Definition	129
Table 125 — MR40 Register Information (MA[7:0] = 28 _H).....	130
Table 126 — MR40 Definition	130
Table 127 — MR41 Register Information (MA[7:0] = 29 _H).....	131
Table 128 — MR42 Register Information (MA[7:0] = 2A _H)	131
Table 129 — MR42 definition	131
Table 130 — MR43 Register Information (MA[7:0] = 2B _H)	132
Table 131 — MR43 definition	132
Table 132 — MR44 Register Information (MA[7:0] = 2C _H)	133
Table 133 — MR44 definition	133
Table 134 — MR45 Register Information (MA[7:0] = 2D _H)	134
Table 135 — MR45 definition	134
Table 136 — MR46 Register Information (MA[5:0] = 2E _H)	134
Table 137 — MR46 definition	134
Table 138 — MR47 Register Information (MA[7:0] = 2F _H)	135
Table 139 — MR47 Definition	135
Table 140 — MR48 Register Information (MA[7:0] = 30 _H).....	135
Table 141 — MR48 Definition	135
Table 142 — MR49 Register Information (MA[7:0] = 31 _H)	135
Table 143 — MR49 Definition	135
Table 144 — MR50 Register Information (MA[7:0] = 32 _H)	135
Table 145 — MR50 Definition	135
Table 146 — MR51 Register Information (MA[7:0] = 33 _H)	135
Table 147 — MR51 Definition	135
Table 148 — MR52 Register Information (MA[7:0] = 34 _H)	136
Table 149 — MR52 Definition	136

Contents (cont'd)

Table 150 — MR53 Register Information (MA[7:0] = 35 _H).....	136
Table 151 — MR53 Definition	136
Table 152 — MR54 Register Information (MA[7:0] = 36H).....	136
Table 153 — MR54 Definition	136
Table 154 — Command Truth Table	137
Table 155 — Allowable CAS command operand(s) combination	139
Table 156 — CAS command with WCK2CK Synchronization bits	140
Table 157 — WCK2CK Sync AC Parameters for WRITE operation	142
Table 158 — WCK2CK Sync AC Parameters for Read operation	144
Table 159 — WCK2CK Sync AC Parameters for Read operation	145
Table 160 — WCK2CK Sync AC Parameters for Read operation	145
Table 161 — WCK2CK Sync AC Parameters for CAS(WS_FAST)	147
Table 162 — WCK2CK SYNC Off Timing Definition (16B Mode) for WR16/32, RD16/32 and MWR.....	149
Table 163 — WCK2CK SYNC Off Timing Definition (BG Mode) for WR16/32, RD16/32 and MWR.....	150
Table 164 — WCK2CK SYNC Off Timing Definition (8B Mode) for WR16/32, RD16/32 and MWR.....	151
Table 165 — WCK2CK SYNC Off Timing Definition for MRR	152
Table 166 — WCK2CK SYNC Off Timing Definition for Training Commands	153
Table 167 — WCK buffer off CAS command (Allowed only when MR18 OP[4]=1)	161
Table 168 — Precharge Bank Selection 8 Bank mode	165
Table 169 — Precharge Bank Selection 4 Bank / 4 Bank Group mode	166
Table 170 — Precharge Bank Selection 16 Banks mode.....	166
Table 171 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE) : DQ ODT is Disable.....	173
Table 172 — Core Timing (tRBTP)	178
Table 173 — RDQS Timing Parameters.....	182
Table 174 — RDQS Pattern Definition in case READ to READ command timing is BL/n + k*nCK (k=1, 2)	183
Table 175 — RDQS Pattern Definition in case READ to READ command timing delay is BL/n + k*nCK (k=1, 2, 3)	184
Table 176 — Read Latencies for Link ECC off case (DVFSC disabled)	189
Table 177 — Read Latencies for Link ECC off case (DVFSC enabled).....	190
Table 178 — Write Latency: DVFSC Disabled	191
Table 179 — Write Latency: DVFSC Enabled	191
Table 180 — nWR Latency	193
Table 181 — tCCDMW	195
Table 182 — DMI pin behavior by command and support function setting	201
Table 183 — DMI pin behavior by command and support function setting	203
Table 184 — Bank and Refresh counter increment behavior on the 4Bank/4BG mode or 16Bank mode	205
Table 185 — Bank and Refresh counter increment behavior on the 8bank mode.....	206
Table 186 — REFRESH Command Scheduling Separation requirements for 4Bank /4BG mode or 16Bank mode	207
Table 187 — REFRESH Command Scheduling Separation requirements for 8Bank mode	208
Table 188 — REFRESH Command Timing Constraints	210
Table 189 — Refresh Requirement Parameters for BG mode or 16Bank mode	211
Table 190 — Refresh Requirement Parameters for 8Bank mode	212
Table 191 — Self Refresh AC Timing	217
Table 192 — Self Refresh Exit (SRX) Command Timing Constraints	218
Table 193 — Example of Segment Masking use in LPDDR5 SDRAM	219
Table 194 — Mode Register Read/Write AC Timing	225
Table 195 — Deep Sleep Mode AC Timing Table.....	227

Contents (cont'd)

Table 196 — DQ Output Mapping for lower byte	228
Table 197 — DQ Output Mapping for upper byte	229
Table 198 — Mode Register Read/Write AC Timing	232
Table 199 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)	233
Table 200 — Mode Register Function with three physical registers	234
Table 201 — Relation between MR Setting and DRAM Operation	235
Table 202 — Frequency Set Point AC Timing Table	236
Table 203 — tFC value mapping	236
Table 204 — tFC value mapping example	236
Table 205 — Command/Address Bus ODT State	240
Table 206 — ODT DC Electrical Characteristics, assuming $R_{ZQ} = 240\Omega \pm 1\%$ over the entire operating temperature range after a proper ZQ calibration	241
Table 207 — ODT Command/Address bus AC timing parameter	242
Table 208 — ODT _{On} and ODT _{Off} Latency Values	244
Table 209 — Asynchronous ODT Turn On and Turn Off Timing	245
Table 210 — ODT DC Electrical Characteristics, assuming $R_{ZQ} = 240\Omega \pm 1\%$ over the entire operating temperature range after a proper ZQ calibration	246
Table 211 — Non-target and Target ODT status depending on DRAM state	248
Table 212 — Normal Mode vs. NT-ODT Mode for Write Operation	249
Table 213 — Normal Mode vs. NT-ODT Mode for Read Operation	249
Table 214 — Combination of Target ODT, Non-target ODT and SoC ODT	250
Table 215 — DQ ODT setting example for Write Operation in NT-ODT Mode	251
Table 216 — ODT _{On} and ODT _{Off} Latency Values for Write	253
Table 217 — Asynchronous NT-ODT Turn On and Turn off Timing for Write	253
Table 218 — ODT _{On_RD} and ODT _{Off_RD} Latency Values for Read with RDQS disabled	254
Table 219 — ODT _{On_RD} and ODT _{Off_RD} Latency Values for Read with RDQS enabled & MR10 OP[5:4]=00 _B , 01 _B , 10 _B	255
Table 220 — ODT _{On_RD} and ODT _{Off_RD} Latency Values for Read with RDQS enabled & MR10 OP[5:4]=11 _B	256
Table 221 — Asynchronous NT-ODT Turn On and Turn Off Timing	256
Table 222 — VRCG Enable / Disable Timing	258
Table 223 — Temperature Sensor	260
Table 224 — MPC Command Definition	261
Table 225 — MPC Command Definition for OP[7:0]	261
Table 226 — WCK Oscillator Matching Error Specification	264
Table 227 — VDDQ Ramp Rates	271
Table 228 — Reference data S[7:0] bit mapping	272
Table 229 — Write data copy hit or miss operands (DC0 – DC3) of CAS command	272
Table 230 — Read data copy function	273
Table 231 — CAS command with write X (zero) enable bits	275
Table 232 — AC Timing	278
Table 233 — MR29 OP[7:0] Register Information	278
Table 234 — Combination of PPR Resource for CA Input	278
Table 235 — Guard Key Encoding for MR42	279
Table 236 — PPR Timing Parameters	281
Table 237 — ECC Check Matrix for Data	286
Table 238 — ECC Check Matrix for DMI	287
Table 239 — Allowable combination among CK_t/c, WCK_t/c and RDQS_t/c	291
Table 240 — Restriction of Single-ended mode for MR1 and MR20	292
Table 241 — SE from/to Differential FSP and additional period for MRW AC timing	295
Table 242 — Delta CK and DQS Specification	295
Table 243 — Effective Burst Length (BL/n) Definition	296
Table 244 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is disabled)	297

Contents (cont'd)

Table 245 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT is disabled).....	298
Table 246 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is disabled)	298
Table 247 — Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is disabled).....	299
Table 248 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is disabled).....	299
Table 249 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is disabled).....	300
Table 250 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is disabled).....	300
Table 251 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is enabled).....	301
Table 252 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT is enabled).....	301
Table 253 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is enabled).....	301
Table 254 — Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is enabled)	302
Table 255 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is enabled)	302
Table 256 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is enabled)	303
Table 257 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is enabled)	303
Table 258 — Auto Precharge Command Timing Constraints for Same Banks in Same Bank Group	304
Table 259 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT Disabled)	304
Table 260 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT Disabled)	304
Table 261 — Command Timing Constraints for Same Banks in 8B Mode.....	305
Table 262 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT Disabled)	305
Table 263 — Command Timing Constraints for Same Banks in 16B Mode.....	305
Table 264 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT Disabled)	306
Table 265 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT Enabled)	306
Table 266 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT Enabled)	306
Table 267 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT Enabled)	307
Table 268 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT Enabled)	307
Table 269 — CAS (WS_FS) Command Timing Constraints	308
Table 270 — CAS (WS_WR) Command Timing Constraints	309
Table 271 — CAS (WS_RD) Command Timing Constraints	310
Table 272 — CAS (WS_OFF) Command Timing Constraints	311
Table 273 — CAS (DC0-3), CAS (WRX) Command Timing Constraints	312
Table 274 — CAS (B3) Command Timing Constraints	313
Table 275 — CAS(WS_FS), CAS(WS_WR), CAS(WS_RD), CAS(WS_OFF) Command Timing Constraints	314

Contents (cont'd)

Table 276 — CAS(DC0-3), CAS(WRX) Command Timing Constraints	315
Table 277 — CAS (B3) Command Timing Constraints	316
Table 278 — Training-Related Timing Constraints.....	317
Table 279 — MRR/MRW Timing Constraints: DQ ODT is Disable	318
Table 280 — MRR/MRW Timing Constraints: DQ ODT is Enable	319
Table 281 — Command Timing Constraints in case of Different Ranks, ODT ON, CAS-WS_FS Broadcast ON	320
Table 282 — Command Timing Constraints in case of Different Ranks, ODT OFF, CAS-WS_FS Broadcast ON	321
Table 283 — Command Timing Constraints in case of Different Ranks, ODT ON, CAS-WS_FS Broadcast OFF	322
Table 284 — Command Timing Constraints in case of Different Ranks, ODT OFF, CAS-WS_FS Broadcast OFF	322
Table 285 — x16 Core Timing for BG mode: DVFS Disabled & Link ECC Disabled	323
Table 286 — x16 Core Timing for 16B mode: DVFS Disabled & Link ECC Disabled	323
Table 287 — x16 Core Timing for 8B mode: DVFS Disabled & Link ECC Disabled	323
Table 288 — Byte Mode Core Timing for BG mode: DVFS Disabled & Link ECC Disabled	324
Table 289 — Byte Mode Core Timing for 16B mode: DVFS Disabled & Link ECC Disabled.....	324
Table 290 — Byte Mode Core Timing for 8B mode: DVFS Disabled & Link ECC Disabled.....	324
Table 291 — x16 Core Timing for BG mode: DVFS Disabled & Link ECC Enabled	325
Table 292 — x16 Core Timing for 16B mode: DVFS Disabled & Link ECC Enabled	325
Table 293 — x16 Core Timing for 8B mode: DVFS Disabled & Link ECC Enabled	325
Table 294 — Byte Mode Core Timing for BG mode: DVFS Disabled & Link ECC Enabled.....	326
Table 295 — Byte Mode Core Timing for 16B mode: DVFS Disabled & Link ECC Enabled	326
Table 296 — Byte Mode Core Timing for 8B mode: DVFS Disabled & Link ECC Enabled	326
Table 297 — x16 Core Timing for 16B mode: DVFS Enabled & Link ECC Disabled	327
Table 298 — x16 Core Timing for 8B mode: DVFS Enabled & Link ECC Disabled	327
Table 299 — Byte Mode Core Timing for 16B mode: DVFS Enabled & Link ECC Disabled	327
Table 300 — Byte Mode Core Timing for 8B mode: DVFS Enabled & Link ECC Disabled	327
Table 301 — Temperature Derating AC Timing	328
Table 302 — Absolute Maximum DC Ratings	329
Table 303 — Recommended DC Operating Conditions.....	330
Table 304 — Input Leakage Current.....	332
Table 305 — Input/Output Leakage Current.....	332
Table 306 — Operating Temperature Range	332
Table 307 — Operating Temperature Range	333
Table 308 — Electrostatic Discharge Sensitivity Characteristics	333
Table 309 — Reset input level specification	334
Table 310 — LPDDR5 Input Level for CS	334
Table 311 — AC Overshoot / Undershoot	334
Table 312 — LPDDR5 AC Overshoot / Undershoot for LVSTL.....	334
Table 313 — CK Differential Input Voltage	336
Table 314 — Clock Single-Ended Input Voltage.....	337
Table 315 — Differential Input Slew Rate Definition for CK_t, CK_c	338
Table 316 — Differential Input Level for CK_t, CK_c	338
Table 317 — Differential Input Slew Rate for CK_t, CK_c.....	338
Table 318 — Cross point voltage for differential input signals (Clock)	339
Table 319 — WCK differential input voltage	340
Table 320 — WCK Single-Ended Input Voltage	342
Table 321 — Differential Input Slew Rate Definition for WCK_t, WCK_c.....	343
Table 322 — Differential Input Level for WCK_t, WCK_c.....	343
Table 323 — Differential Input Slew Rate for WCK_t, WCK_c.....	343
Table 324 — Cross point voltage for differential input signals (WCK).....	344
Table 325 — Output Slew Rate (single-ended)	345

Contents (cont'd)

Table 326 — Differential Output Slew Rate	346
Table 327 — Single Ended WCK parameters	348
Table 328 — Single Ended CK parameters.....	349
Table 329 — Reference Voltage for tLZ(RDQS), tHZ(RDQS) Timing Measurements.....	351
Table 330 — Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements	353
Table 331 — Read AC Timing	354
Table 332 — Input / Output Capacitance.....	355
Table 333 — Definition of Switching for CA Input Signals	356
Table 334 — CA Pattern for IDD4R @ BG mode.....	356
Table 335 — CA Pattern for IDD4R @ 16B mode.....	357
Table 336 — CA Pattern for IDD4R @ 8B mode.....	357
Table 337 — CA Pattern for IDD4W@ BG mode	358
Table 338 — CA Pattern for IDD4W @ 16B mode.....	358
Table 339 — CA Pattern for IDD4W@ 8B mode.....	359
Table 340 — Data Pattern for IDD4R @ DBI Off.....	360
Table 341 — Data Pattern for IDD4W @ DBI Off.....	362
Table 342 — Data Pattern for IDD4R @ DBI On.....	363
Table 343 — Data Pattern for IDD4W @ DBI On.....	365
Table 344 — LPDDR5 IDD Specification Parameters and Operating Conditions.....	366
Table 345 — Clock AC Timings for 5/10/67/133MHz	371
Table 346 — Clock AC Timings for 200/267/344/400MHz	372
Table 347 — Clock AC Timings for 467/533/600/688	372
Table 348 — Clock AC Timings for 750/800MHz	372
Table 349 — Write Clock AC Timings for 266/533/800/1067MHz.....	375
Table 350 — Write Clock AC Timings for 1375/1600/1867/2134MHz	376
Table 351 — Write Clock AC Timings for 2400/2750/3000/3200MHz	376
Table 352 — DRAM DQ output timing	379
Table 353 — CS Rx Specification.....	382
Table 354 — CA Rx Specification.....	385
Table 355 — DQ, DMI, Parity and DBI Rx Specification	389
Table 356 — Pull-down Driver Characteristics, with ZQ Calibration	390
Tables	
Table 357 — Pull-Up Characteristics, with ZQ Calibration	390
Table 358 — Valid Calibration Points	390
Table 359 — Un-terminated Pull Up Characteristics	390
Table 360 — Worst Case Output Driver and Termination Resistance	391
Table 361 — Worst Case Output high voltage	391
Table 362 — Output Driver and Termination Resistance Temperature and Voltage Sensitivity.....	392
Table 363 — LPDDR5 Pad order	394
Table 364 — Package configuration example	395

LOW POWER DOUBLE DATA RATE (LPDDR) 5

(From JEDEC Board Ballet JCB-18-50, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This document defines the LPDDR5 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant x16 one channel SDRAM device and x8 one channel SDRAM device. LPDDR5 device density ranges from 2 Gb through 32 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3) and LPDDR4 (JESD209-4).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR5 standard.

2 Overview

2.1 Features

TBD

2.2 Functional Description

2.2.1 Pad Definition and Description

Table 1 — Pad Definition and Description

Symbol	Type	Description	Note
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c).	
CS	Input	Chip Select: CS is part of the command code, and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.	
CA[6:0]	Input	Command/Address Inputs: CA signals provide the Command and Address input according to the Command Truth Table	
DQ[15:0]	I/O	Data Input/Output: Bi-direction data bus.	
WCK[1:0]_t WCK[1:0]_c	Input	Data Clocks: WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.	
RDQS [1:0]_t , RDQS[1:0]_c	RDQS_t :I/O, RDQS_c :Output	Read Data Strobe: RDQS_t and RDQS_c are the differential output clock signals used to strobe data during a READ operation. And RDQS_t is also used as a Parity pin at Write with Link Protection enabled.	1
DMI[1:0]	I/O	Data Mask Inversion: DMI achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and DMI is a bi-directional signal and each byte of data has a DMI signal.	1
ZQ	Reference	ZQ: ZQ is used to calibrate the output drive strength and the termination resistance as calibration reference. There is one ZQ pad per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor.	
VDDQ, VDD1, VDD2H, VDD2L	Supply	Power Supplies: Isolated on the die for improved noise immunity.	
VSS	GND	Ground Reference: Power supply ground reference	
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets the die. Reset_n is an asynchronous signal.	

NOTE 1 See Table 2 and Table 3, Per-Byte Signal List/Description, for multi-function definition for these pins.

2.2.2 Pin per byte

Table 2 — Pins Per-Byte Signal List/Description for Link Protection disabled

Pin Name	DBI Enable	SE RDQS		SE RDQS		Diff RDQS	
		Link Protection disabled					
		(MR20 OP[1:0]=01)		(MR20 OP[1:0]=11)		(MR20 OP[1:0]=10)	
#11 DMI	No	Write	Read	Write	Read	Write	Read
	Yes	DM	N/A	DM	N/A	DM	N/A
#12 RDQS_t	No	N/A	RDQS_t	N/A	N/A	N/A	RDQS_t
	Yes	N/A	RDQS_t	N/A	N/A	N/A	RDQS_t
#13 RDQS_c	No	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c
	Yes	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c

Table 3 — Pins Per-Byte Signal List/Description for Link Protection enabled

Pin Name	DBI Enable	SE RDQS		SE RDQS		Diff RDQS	
		Link Protection enabled					
		(MR20 OP[1:0]=01)		(MR20 OP[1:0]=11)		(MR20 OP[1:0]=10)	
#11 DMI	No	Write	Read	Write	Read	Write	Read
	Yes	DM	parity	DM	parity	DM	parity
#12 RDQS_t	No	parity	RDQS_t	parity	N/A	parity	RDQS_t
	Yes	parity	RDQS_t	parity	N/A	parity	RDQS_t
#13 RDQS_c	No	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c
	Yes	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c

2.2.3 LPDDR5 Bank Architecture

LPDDR5 SDRAM supports three bank architectures to provide optimal access methods for varied system configurations. The native burst length determined by data prefetch size depends on which bank architecture is enabled.

Each architecture name is abbreviated as follows:

- BG Mode = 4 banks, 4 bank groups.
- 8B Mode = 8 banks, no bank groups.
- 16B Mode = 16 banks, no bank groups.

The supported operation data rate for each Bank/Bank Group Organization is as follows:

- BG Mode for more than 3200 Mbps (>3200 Mbps).
- 8B Mode for all data rate range.
- 16B Mode for equal or less than 3200 Mbps (≤ 3200 Mbps).

The bank architecture is selected by MR3 OP[4:3]. This mode register is replicated for each frequency set point.

The BG and 16B modes support burst lengths of 16 or 32, while 8B mode supports only burst length 32.

2.2.3.1 Block diagram of bank configuration and Read operation outline

Here are the block diagrams of each architecture.

2.2.3.1.1 4Banks / 4Bank Groups Configuration

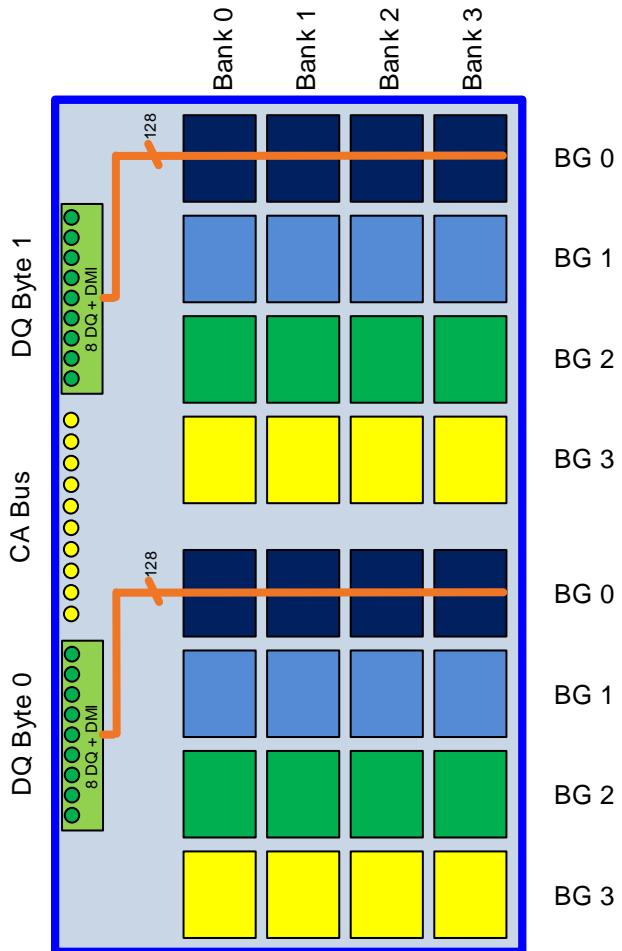


Figure 1 — BG Mode Configuration Example (One Channel Shown)

2.2.3.1.2 8Banks Mode Configuration

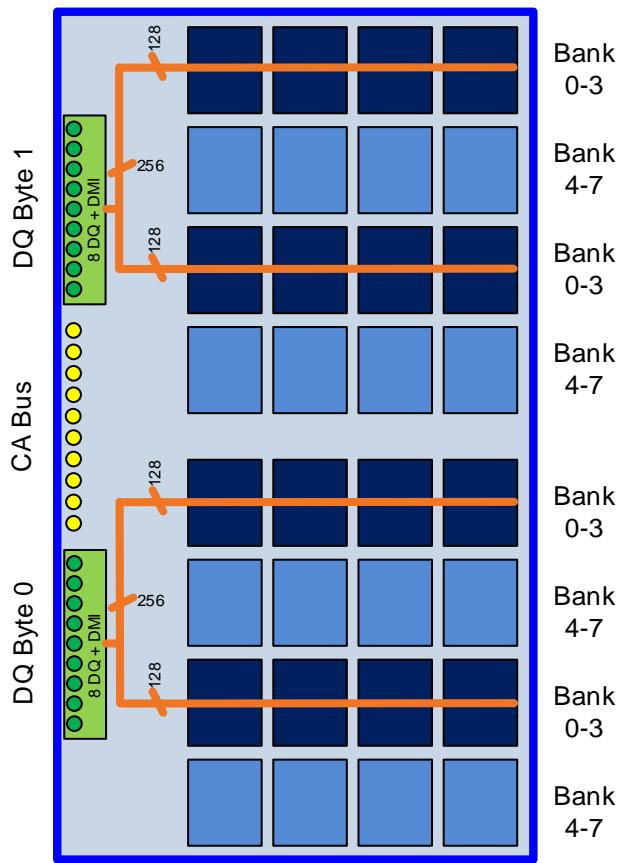


Figure 2 — 8B Mode Configuration Example (One Channel Shown)

2.2.3.1.3 16Banks Mode Configuration

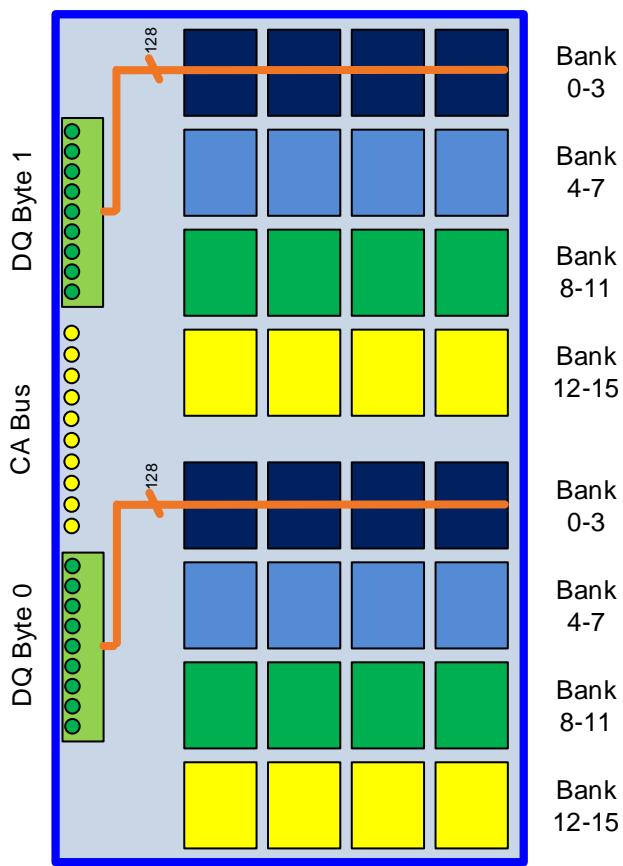


Figure 3— 16B Mode Configuration Example (One Channel Shown)

2.2.3.2 Address mapping

The DRAM array mapping in these three modes is shown in Table 4.

Table 4 — Address Array mapping

Bank Architecture	BG	BA0	BA1	BG0	BG1
8B		BA0	BA1	BA2	B4
16B		BA0	BA1	BA2	BA3

NOTE 1 BA0-3: Bank Address, BG0-1: Bank Group address, B4: Burst Starting Address.

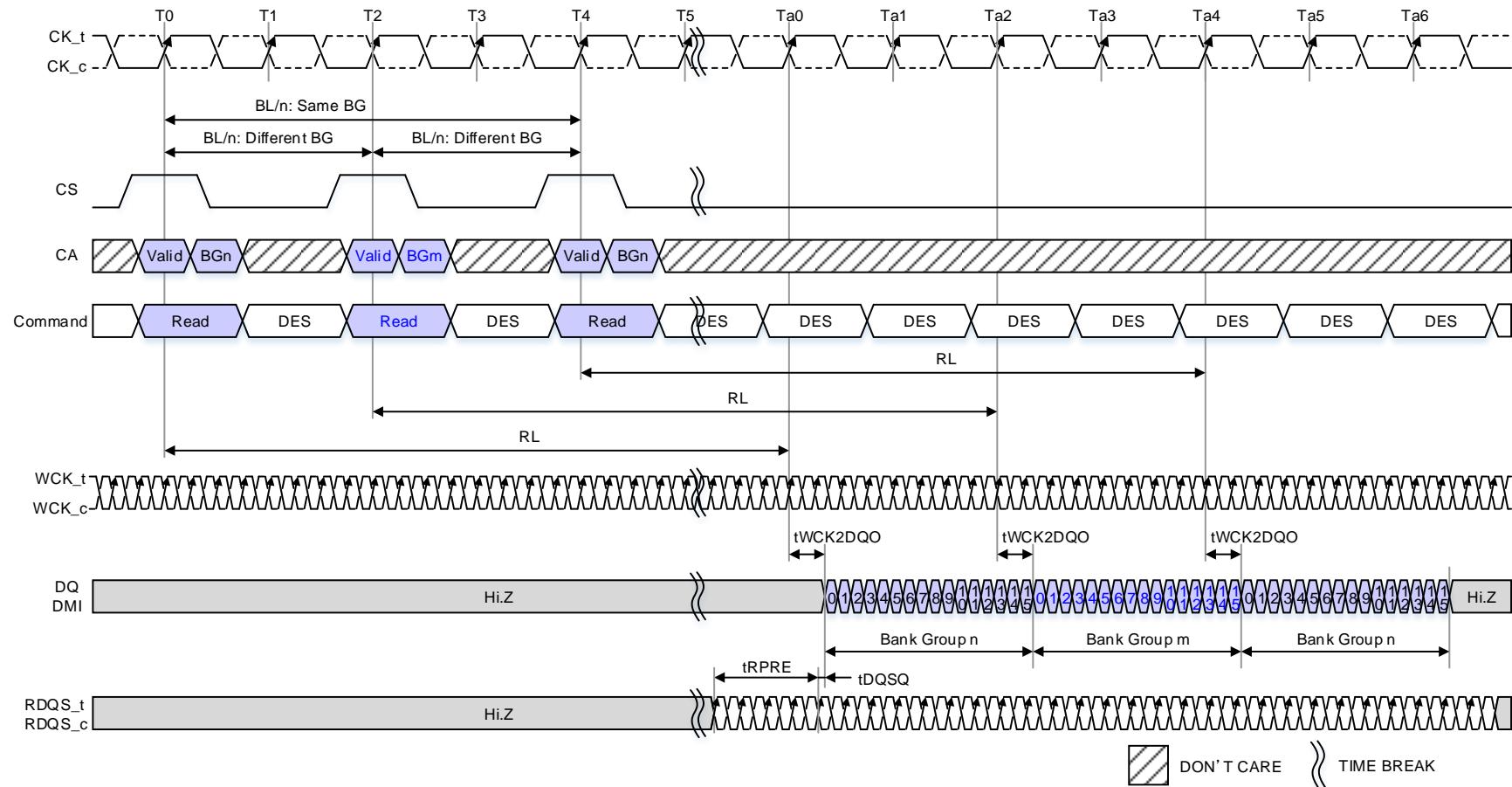
2.2.3.3 Bank architecture transition

The three bank modes can be selected by Mode Register change. The mode register that defines the bank mode is applied Frequency Set Point (FSP) function.

2.2.3.4 Burst Operation

The Read/Write command behavior depends on the bank architecture. Read behavior is described in the following figures for example. These figures focus on Read data output behavior. Therefore, the other part, for example CAS command, WCK input is omitted. Refer to 7.4, Read and Write Operation, for details.

2.2.3.4 Burst Operation (Cont'd)



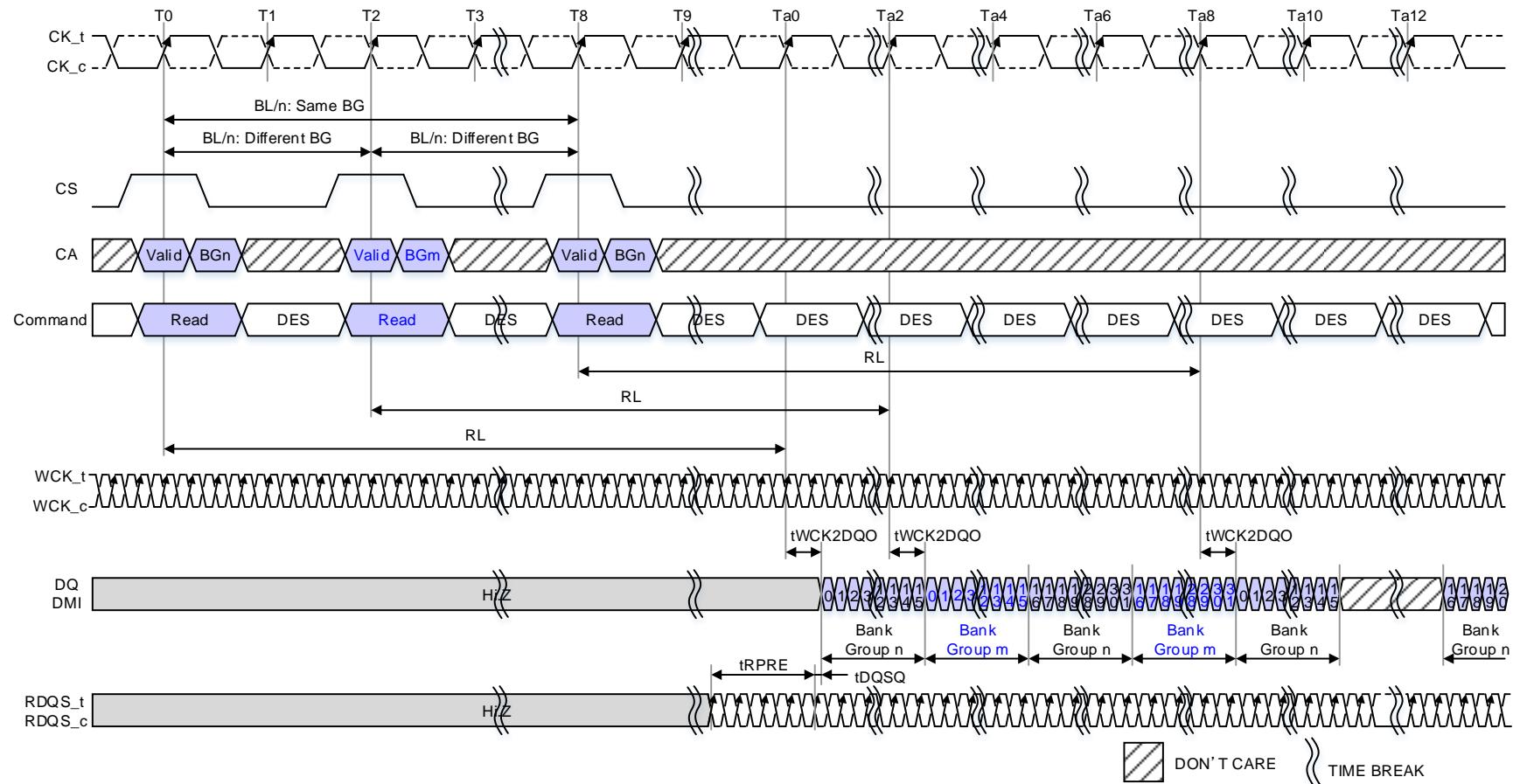
NOTE 1 MR3 OP[4:3]=00_B: BG Mode, MR18 OP[7]=0_B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 4 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=16

2.2.3.4 Burst Operation (Cont'd)



NOTE 1 MR3 OP[4:3]=00_B: BG mode, MR18 OP[7]=0_B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

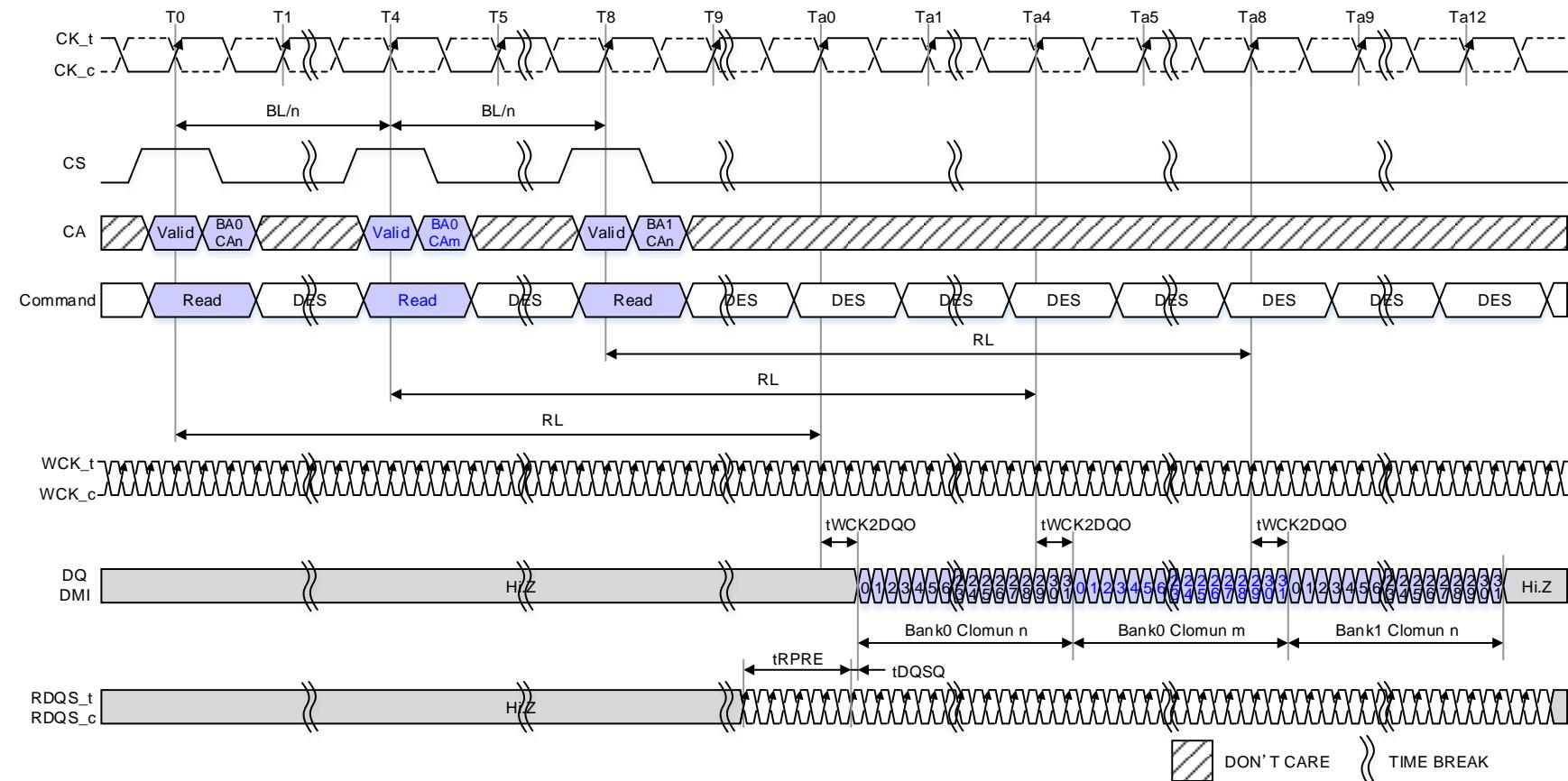
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 5 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=32

The BG Mode architecture only supports BL32 in an interleaved fashion when the WCK and CK ratio is 4:1. BL32 interleaved Reads will output the first word of DQ[15:0] after certain latency from the Read command. The second word consisting of DQ[31:16] will begin to be driven after an 8tWCK gap from the end of the first word. Figure 5 depicts BG mode Read operations for BL32 including the interleaving between bank groups. If correctly implemented, Read(BL16) command and Read32(BL32) commands can be mixed, however once a Read32(BL32) command is issued, issuing Read(BL16)/Read32(BL32) command after 3 clocks is prohibited, to avoid read data conflict.

2.2.3.4 Burst Operation (Cont'd)

The relationship between preceding Write32(BL32) and Write(BL16)/Write32(BL32) is the same as preceding Read32(BL32) and Read(BL16)/Read32(BL32).



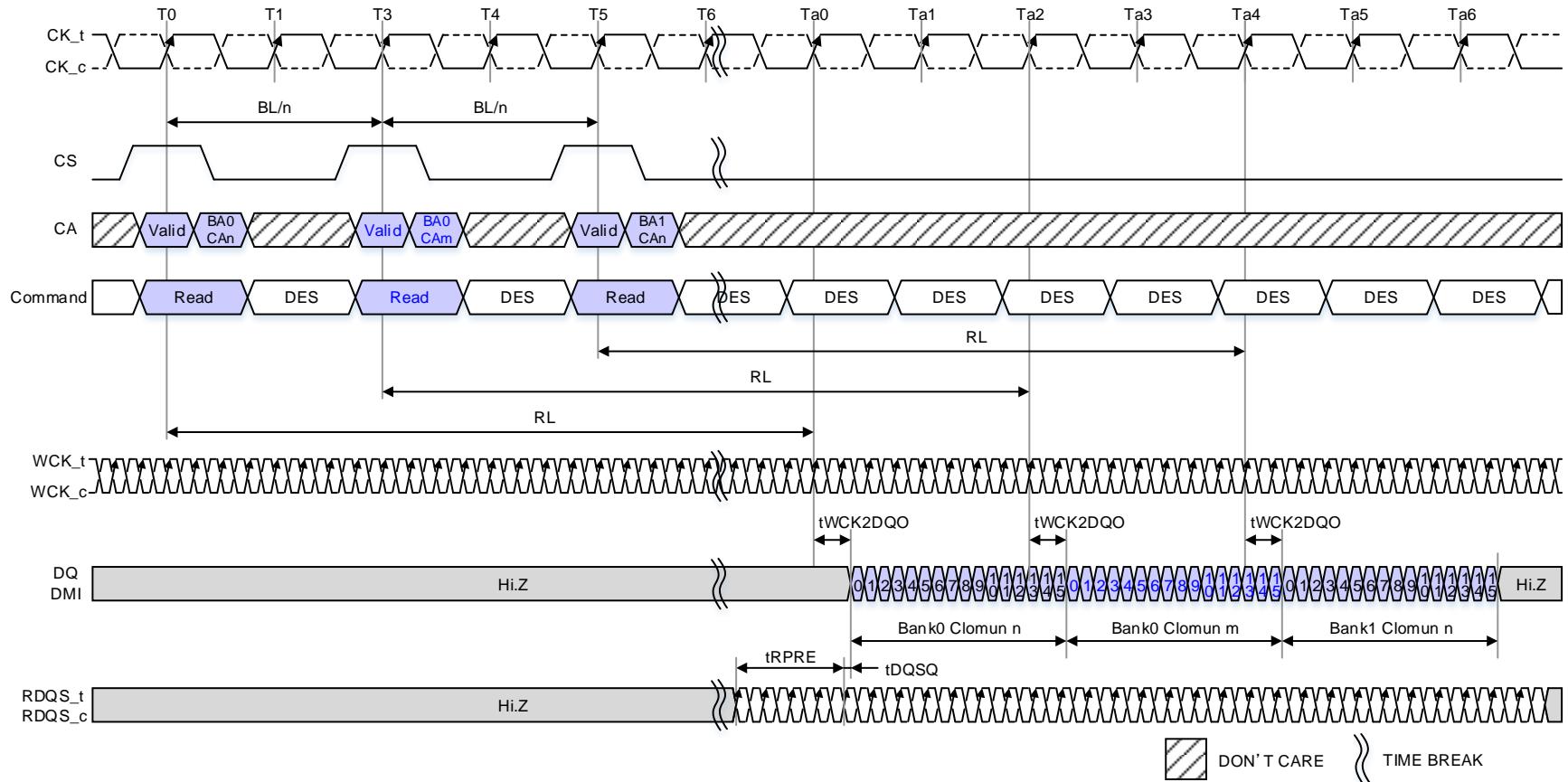
NOTE 1 MR3 OP[4:3]=01_B: 8B mode, MR18 OP[7]=0_B: CKR (WCK vs. CK)= 4:1

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32

2.2.3.4 Burst Operation (Cont'd)



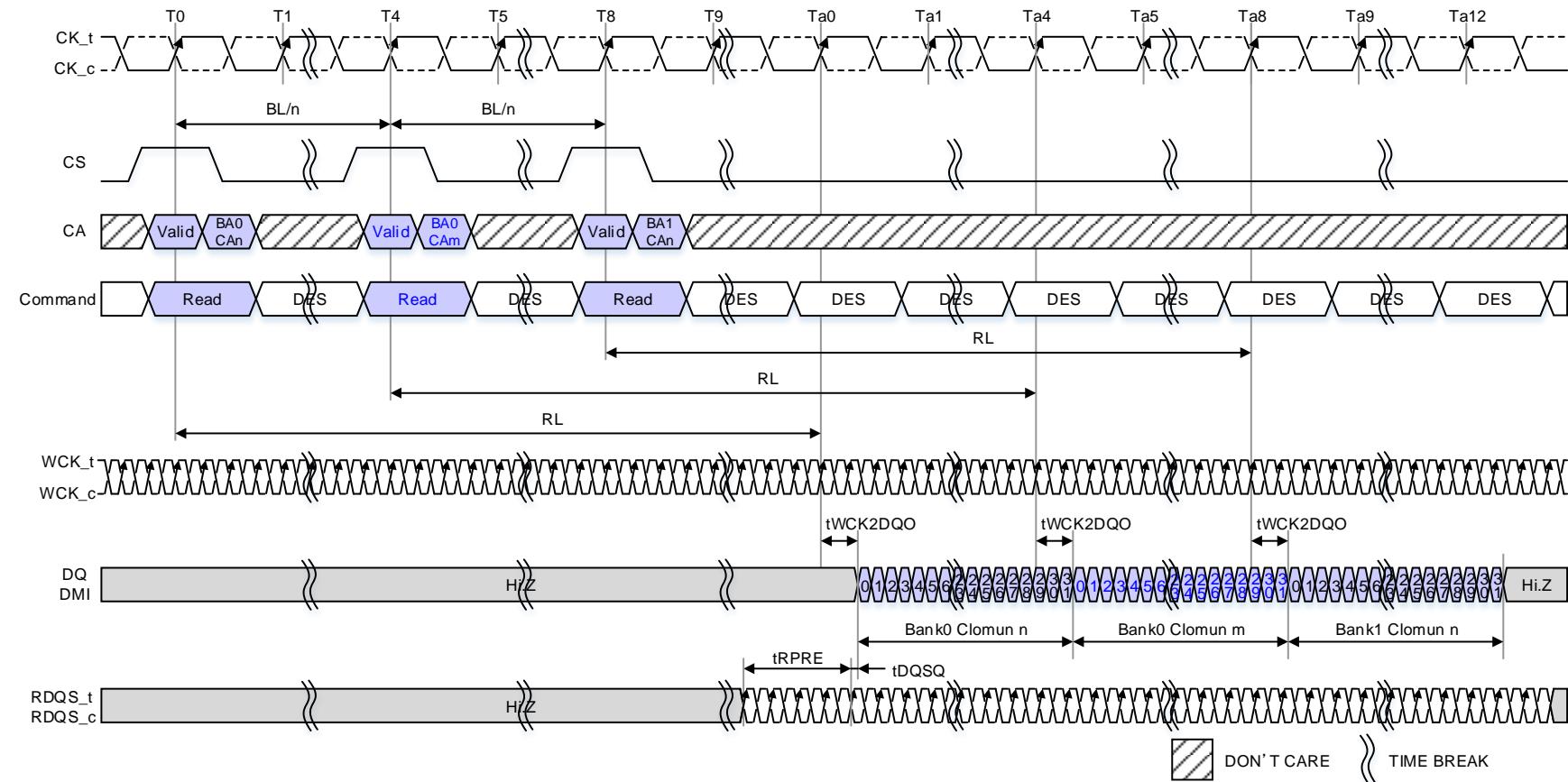
NOTE 1 MR3 OP[4:3]=10B: 16B Mode, MR18 OP[7]=0B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 7 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=16

2.2.3.4 Burst Operation (Cont'd)



NOTE 1 MR3 OP[4:3]=10B: 16B mode, MR18 OP[7]=0B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 8 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=32

2.2.4 LPDDR5 SDRAM Addressing

Table 5 — LPDDR5 SDRAM x16 mode Addressing for BG Mode (4Banks/4Bank Groups)

2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 6 — LPDDR5 SDRAM x8 mode Addressing for BG Mode

Memory Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Configuration	16Mb x 8DQ x 4 BG x 4 banks	24Mb x 8DQ x 4 BG x 4 banks	32Mb x 8DQ x 4 BG x 4 banks	48Mb x 8DQ x 4 BG x 4 banks	64Mb x 8DQ x 4 BG x 4 banks	96Mb x 8DQ x 4 BG x 4 banks	128Mb x 8DQ x 4 BG x 4 banks	196Mb x 8DQ x 4 BG x 4 banks	256Mb x 8DQ x 4 BG x 4 banks
Number of Banks in BG	4	4	4	4	4	4	4	4	4
Number of Bank Groups	4	4	4	4	4	4	4	4	4
Array Pre-Fetch	128	128	128	128	128	128	128	128	128
Number of Rows	16,384	24,576	32,768	49,152	65,536	98,304	131,072	196,608	262,144
Number of Columns (fetch boundaries)	64	64	64	64	64	64	64	64	64
Page Size (Bytes)	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
Density	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1
Bank Group Addresses	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1
Row Addresses	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16	R0 - R17 (R16=0 when R17=1)	R0 - R17
Column Addresses	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5
Burst Addresses	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3
Burst Starting Address Boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit
Native Burst Length	16	16	16	16	16	16	16	16	16

NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.

NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.

NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

NOTE 4 The row address input which violates the restriction described in Note 3 in this table may result in undefined or vendor specific behavior. Consult the memory vendor for more information.

2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 7 — LPDDR5 SDRAM x16 mode Addressing for 8B Mode

Memory Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Configuration	16Mb x 16DQ x 8 banks	24Mb x 16DQ x 8 banks	32Mb x 16DQ x 8 banks	48Mb x 16DQ x 8 banks	64Mb x 16DQ x 8 banks	96Mb x 16DQ x 8 banks	128Mb x 16DQ x 8 banks	192Mb x 16DQ x 8 banks	256Mb x 16DQ x 8 banks
Number of Banks	8	8	8	8	8	8	8	8	8
Array Pre-Fetch	512	512	512	512	512	512	512	512	512
Number of Rows	8,192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of Columns (fetch boundaries)	64	64	64	64	64	64	64	64	64
Page Size (Bytes)	4,096	4,096	4,096	4,096	4,096	4,096	4,096	4,096	4,096
Density	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2
Row Addresses	R0 - R12	R0 - R13 (R12=0 when R13=1)	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16
Column Addresses	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5
Burst Addresses	B0-B4	B0-B4	B0-B4	B0-B4	B0-B4	B0-B4	B0-B4	B0-B4	B0-B4
Burst Starting Address Boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit
Native Burst Length	32	32	32	32	32	32	32	32	32

NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.

NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.

NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

NOTE 4 The row address input which violates the restriction described in Note 3 in this table may result in undefined or vendor specific behavior. Consult the memory vendor for more information.

2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 8 — LPDDR5 SDRAM x8 mode Addressing for 8B Mode

2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 9 — LPDDR5 SDRAM x16 mode Addressing for 16B Mode

2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 10 — LPDDR5 SDRAM x8 mode Addressing for 16B Mode

2.2.5 Speed Grades

Table 11 — LPDDR5 Speed Grades

OPERATING MODE / SPEED GRADE			LPDDR5-5500	LPDDR5-6400	Unit	
DVFSC ²	WCK:CK Ratio ³	Banks ⁴	Maximum Data Rate ¹			
Disabled	4:1	BG	5500	6400	Mbps	
Disabled	4:1	8B	5500	6400		
Disabled	4:1	16B	3200	3200		
Disabled	2:1	BG	Not Supported			
Disabled	2:1	8B	3200	3200		
Disabled	2:1	16B	3200	3200		
Enabled	4:1	BG	Not Supported			
Enabled	4:1	8B	1600	1600		
Enabled	4:1	16B	1600	1600		
Enabled	2:1	BG	Not Supported			
Enabled	2:1	8B	1600	1600		
Enabled	2:1	16B	1600	1600		
Link ECC Feature support by DRAM			Optional	Required		
<p>NOTE 1 Speed grades represent the maximum data rate capability of the device. Higher speed grade devices can be operated at lower data rates. Achieving maximum data rates requires appropriate latency settings.</p> <p>NOTE 2 DVFSC is enabled/disabled in MR19 OP[1:0] and MR13 OP[7].</p> <p>NOTE 3 WCK:CK ratio is set in MR18 OP[7].</p> <p>NOTE 4 Bank organization (BG, 8B or 16B) is set in MR3 OP[4:3].</p> <p>NOTE 5 DVFSQ is supported up to TBD Mbps for all speed grades.</p>						

2.2.6 Burst Sequence

Table 12 — Burst Sequence for READ (8bank mode)

Burst Length	Burst Type	B4	B3	B2	B1	B0	Burst Cycle Number and Burst Address Sequence																																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32						
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
		0	1	0	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		1	0	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	1	0	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7

NOTE 1 B0-B2 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 128-bit (8n) boundaries.

Table 13 — Burst Sequence for READ (4bank/ 4Bank Group mode or 16Bank mode)

Burst Length	Burst Type	C0	B3	B2	B1	B0	Burst Cycle Number and Burst Address Sequence																																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32						
16	SEQ	V	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	1	0	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
32	SEQ	0	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	1	0	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		1	0	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	1	0	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7

NOTE 1 B0-B2 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 128-bit (8n) boundaries.

Table 14 — Burst sequence for Write

Burst Length	Burst Type	C0/B4	B3	B2	B1	B0	Burst Cycle Number and Burst Address Sequence																														
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32				
16	SEQ	V	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F														
		0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

NOTE 1 B0-B2 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 256-bit (16n) boundaries for burst length 16 and 512-bit (32n) boundaries for Burst length 32.

NOTE 3 B3 shall be set to '0' for all Write operations.

NOTE 4 C0 shall be set to '0' for all Write operations in BL32 mode.

3 WCK Clocking

LPDDR5 command and address interface operates from a differential clock (CK_t and CK_c). Commands and addresses are registered single data rate (SDR) at every rising edge of CK.

LPDDR5 uses a DDR data interface. The data interface uses two differential forwarded clocks (WCK_t/WCK_c) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c. WCK_t and WCK_c operate at twice the frequency of the command/address clock (CK_t/CK_c).

WCK_t/WCK_c is used to sample DQ data for write operation and toggle DQ data for read operation. WCK_t/WCK_c must start toggle before starting write or read DQ data burst. Any commands that require DQ data burst initiate WCK2CK auto-sync sequence in LPDDR5 SDRAM. WCK2CK auto-sync sequence is illustrated in **Figure 11**. After WCK2CK auto-sync sequence, DRAM internal WCK0 is aligned with CK to get ready for DQ data burst. This DRAM internal WCK2CK auto-sync sequence is hidden to memory controller, not requiring any extra MRW or commands.

If MR-x OP[x] is enabled then RDQS mode is enabled, in which a read data strobe (RDQS) will be sent on the EDC pins along with the data. EDC pins may act as a read strobe. See RDQS mode for more detail (TBD).

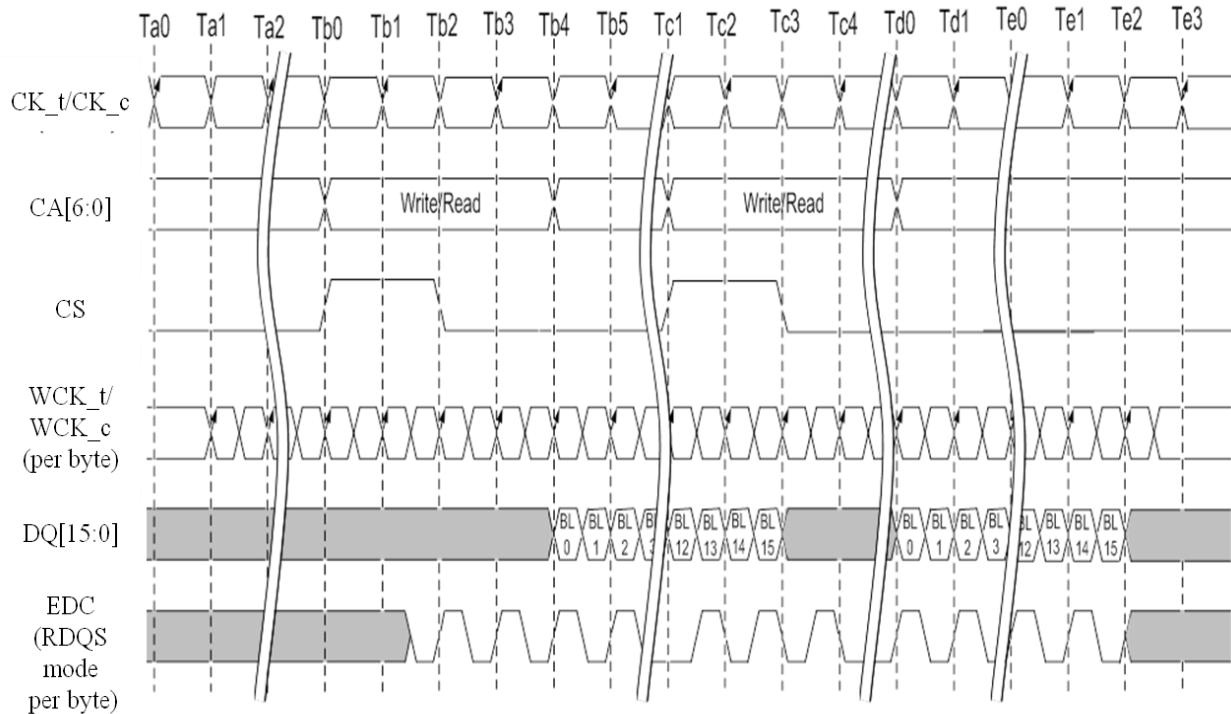


Figure 9 — Clocking and Interface Relationship

3 WCK Clocking (Cont'd)

Table 15 — Example Clock and Interface Signal Frequency Relationship

PIN	Speed	Unit
CK_t, CK_c	1.6	GHz
Command / Address	1.6	Gbps/pin
WCK_t, WCK_c	3.2	GHz
DQ, DMI	6.4	Gbps/pin
EDC (RDQS mode)	3.2	GHz

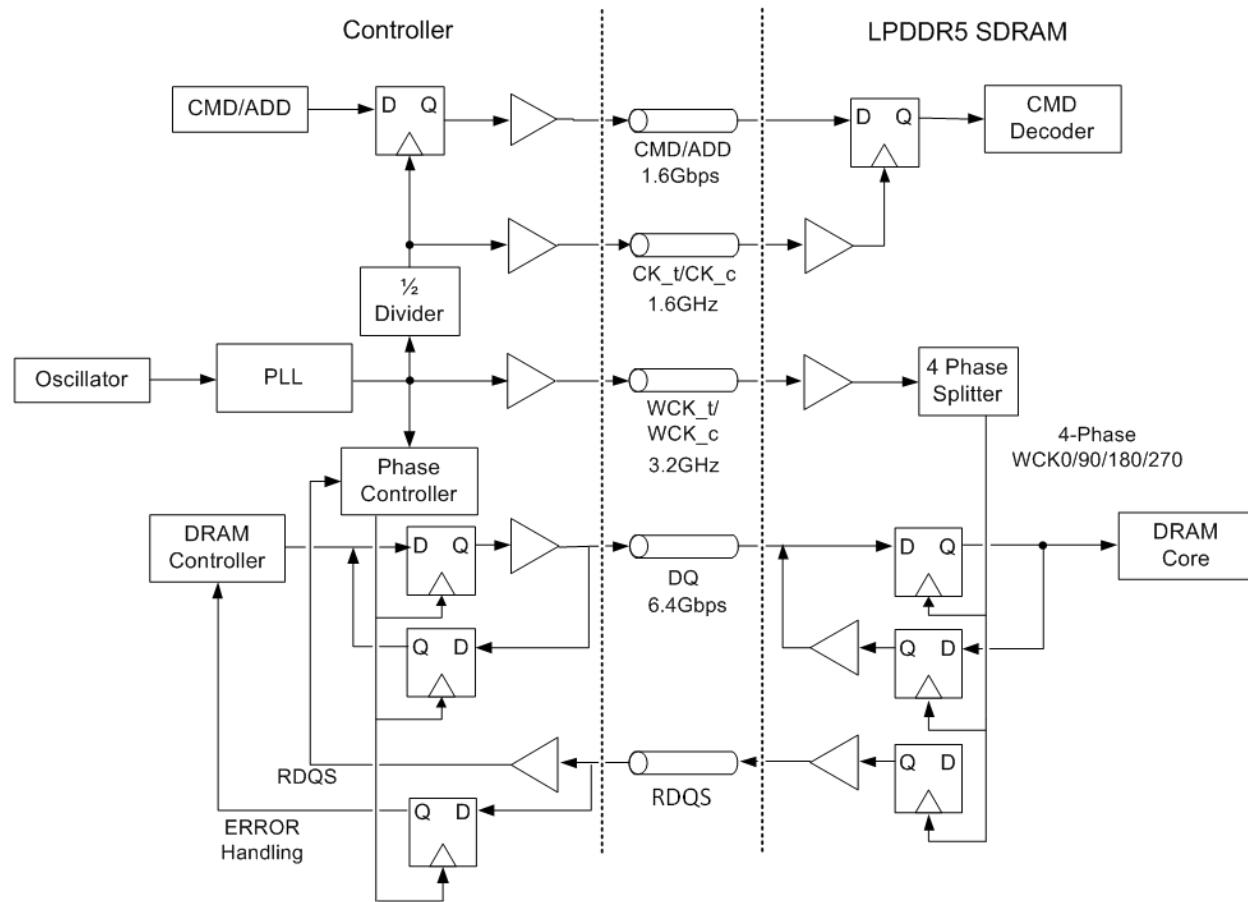


Figure 10 — Block Diagram of an example system

3 WCK Clocking (Cont'd)

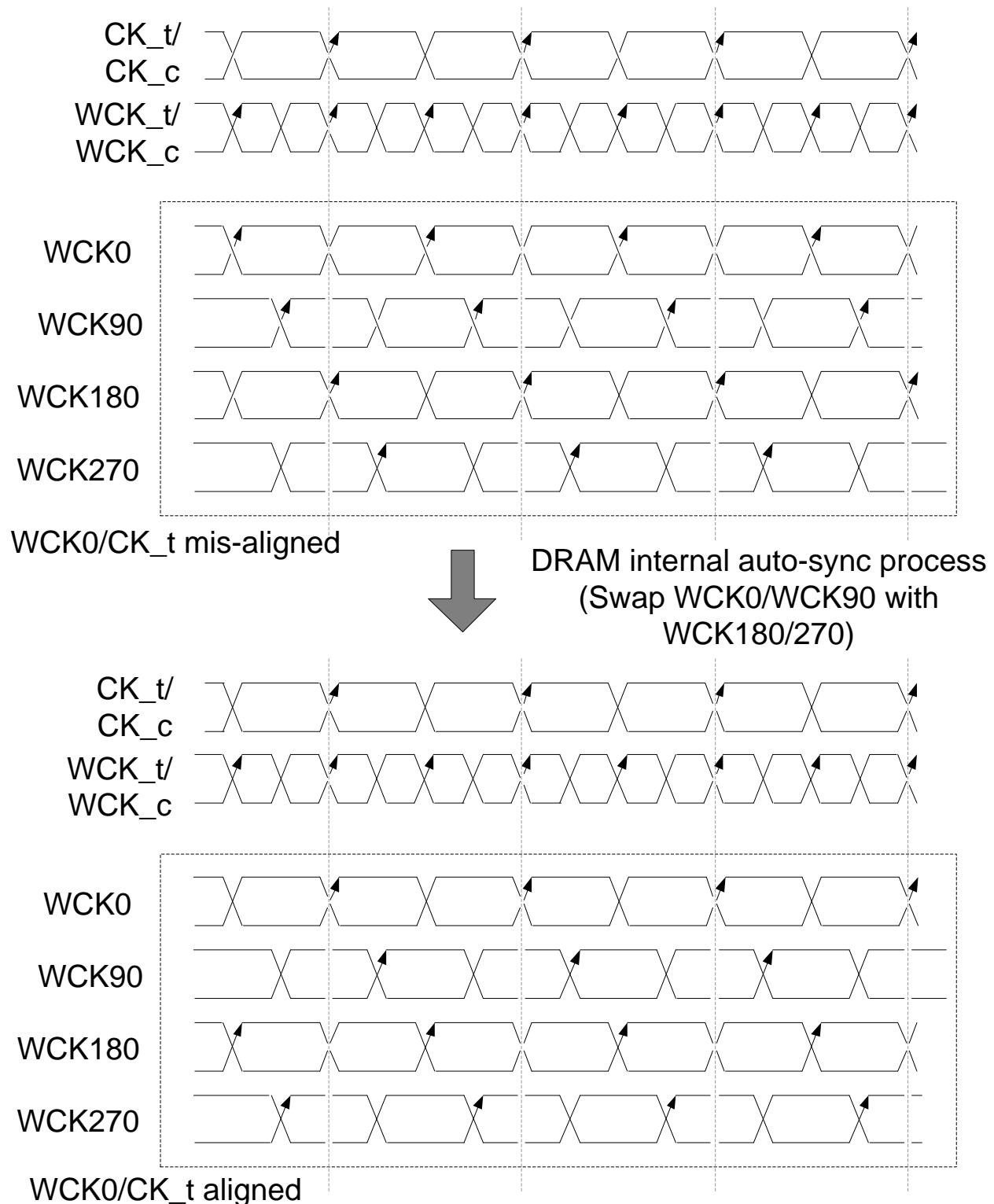


Figure 11 — DRAM internal WCK2CK auto-sync process

4 Initialization and Training

4.1 Power-up, Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as Table 16.

Table 16 — MRS Default setting

Item	MRS	Default Setting	Description
FSP-OP/WR	MR16 OP[3:0]	0000 _B	FSP-OP/WR[0] is enabled
WLS	MR3 OP[5]	0 _B	Write Latency Set A is selected
WL	MR1 OP[7:4]	0000 _B	WL = 4
RL	MR2 OP[3:0]	0000 _B	RL = 6, nRBTP = 0
nWR	MR2 OP[7:4]	0000 _B	nWR = 5
DBI-WR/RD	MR3 OP[7:6]	00 _B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000 _B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000 _B	DQ ODT is disabled
Vref (CA) Value	MR12 OP[6:0]	1010000 _B	VREF(CA): 50.0% of VDDQ
Vref (DQ) Value	MR14 OP[6:0] MR15 OP[6:0]	1010000 _B 1010000 _B	VREF(DQ): 50.0% of VDDQ
Dual VDD2	MR13 OP[7]	0 _B	Dual VDD2 rail (1.05V & 0.9V) used ¹⁾
CKR	MR18 OP[7]	1 _B	2:1 ratio
ZQ Mode	MR28 OP[5]	0 _B	Background ZQ Calibration
NOTE 1 DRAM can be powered up in either dual rail or single rail mode with the default setting. MR13 OP[7] shall be set correctly prior to CBT.			

4.1.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR5 SDRAM. Unless specified otherwise, these steps are mandatory.

- 1) While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times VDD2H$) and all other inputs shall be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 17. VDD1 must ramp at the same time or earlier than VDD2H. VDD2H must ramp at the same time or earlier than VDD2L. VDD2L must ramp at the same time or earlier than VDDQ.

Table 17 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2H
	VDD2H must be equal to or greater than VDD2L
	VDD2L must be greater than VDDQ-200mV
NOTE 1 Ta is the point when any power supply first reaches 300mV.	
NOTE 2 Voltage ramp conditions in Table 17 apply between Ta and power-off (controlled or uncontrolled).	
NOTE 3 Tb is the point at which all supply voltages are within their defined ranges.	
NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.	

4.1.1 Voltage Ramp and Device Initialization (Cont'd)

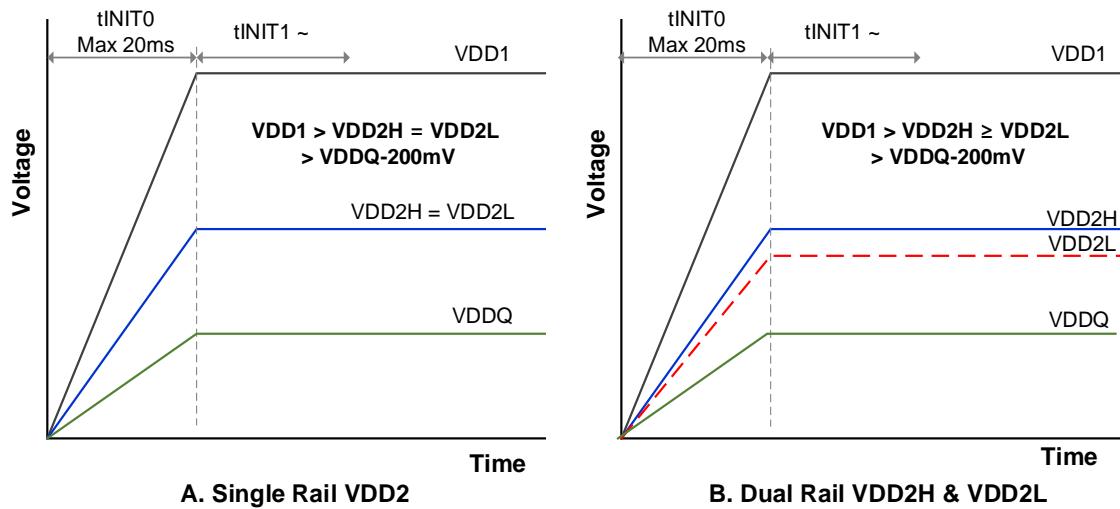
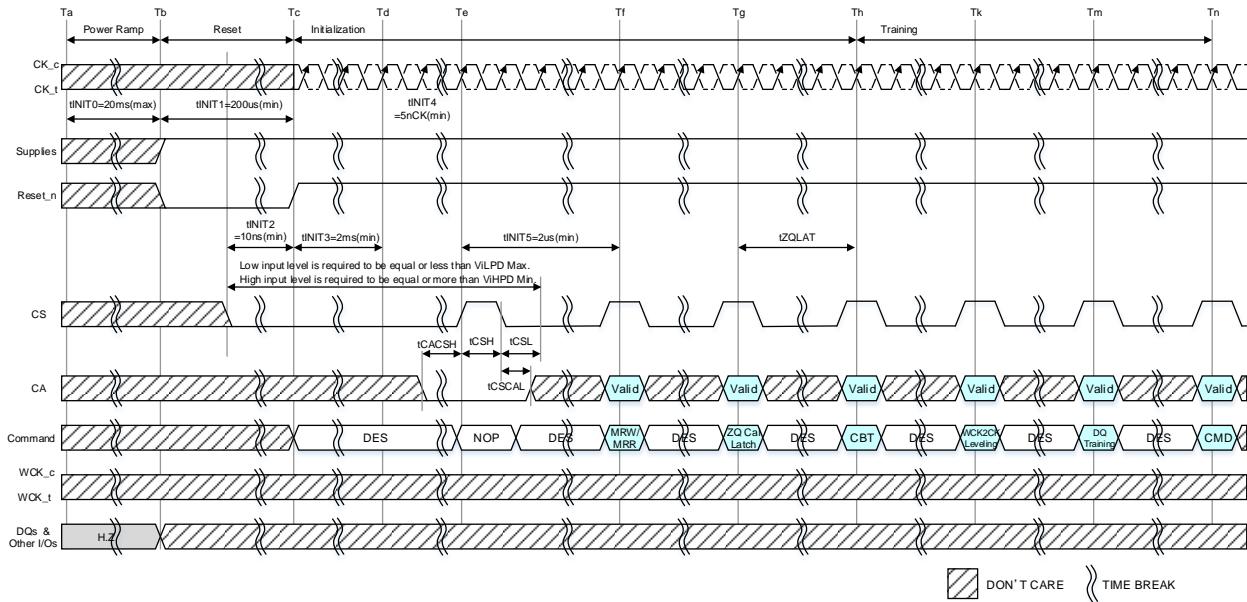


Figure 12 — Requirement for Voltage Ramp Control

- 2) Following the completion of the voltage ramp (T_b), RESET_n must be maintained LOW. DQ, DMI, WCK_t and WCK_c, RDQS_t, CK_t, CK_c and CA voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. CS level is required to be equal or less than ViLPD Max to prevent malfunction before a starting point of tINIT2.
- 3) Beginning at T_b , RESET_n must remain LOW for at least tINIT1(T_c), after which RESET_n can be de-asserted to HIGH(T_c).

4.1.1 Voltage Ramp and Device Initialization (Cont'd)



NOTE 1 Training is optional and may be done at the system architect's direction. The training sequence after ZQ_CAL latch in this figure (Th) is simplified recommendation and actual training sequence may vary depending on systems.

NOTE 2 Initial ZQ Calibration is started automatically by DRAM when RESET_n goes high after tINIT1 and is completed before Td.

NOTE 3 For the single VDD2 rail system, it is recommended to set MR13 OP[7] 1_B to switch VDD2 mode right after the time any MRW/MRR can be asserted(Tf) prior to CBT.

Figure 13 — Power Ramp and Initialization Sequence

- 4) Almost at the same time when RESET_n is de-asserted, CK_t and CK_c need to be toggle or valid to be complementary level.
- 5) CK_t and CK_c are required to be toggling (Td) and stabilized for tINIT4 before CS receives one toggling (Te).
- 6) After tINIT4, wait minimum of tINIT5 to issue any MRR or MRW commands (Tf). When issuing the first command (Tf), the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tWCKCK) could have relaxed timings (such as tWCKCKb) before the system is appropriately configured.

4.1.1 Voltage Ramp and Device Initialization (Cont'd)

- 7) Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, and VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

NOTE 1 The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.2.2 for information on how to enter/exit the training mode.

- 8) After command bus training, DRAM controller must perform WCK2CK leveling. WCK2CK leveling mode is enabled when MR18-OP[6] is high (Ti). See 4.2.5.2 for detailed description of WCK2CK leveling entry and exit sequence. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.
- 9) After WCK2CK leveling, the DQ Bus (internal VREF(DQ), WCK, and DQ) should be trained for high-speed operation using the training commands (RD FIFO / WT FIFO / RD DQ Calibration) described in command truth table and by issuing MRW commands to adjust VREF(DQ)(Ti). The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The Read DQ Calibration command is used together with FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See 4.2.9 for detailed DQ Bus Training sequence.
- 10) At Tk, the LPDDR5 SDRAM is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table 18 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Max voltage-ramp time at power-up
tINIT1	200		μs	Min Reset_n low time after completion of voltage ramp
tINIT2	10		ns	Min CS low time before RESET_n high
tINIT3	2		ms	Min CS low time after RESET_n high
tINIT4	5		tCK	Min stable clock before first CS high
tINIT5	2		μs	Min idle time before first MRW/MRR command
tZQLAT	Max(30ns, 4nCK)		ns	ZQCAL latch quiet time
tCKb	Note 1,2	Note 1,2	ns	Clock cycle time during boot

NOTE 1 Min tCKb guaranteed by DRAM test is 18ns.

NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

4.1.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

- 1) Assert RESET_n below $0.2 \times VDD2H$ anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CS must be pulled LOW ($\leq VILPD$) at least 10ns before de-asserting RESET_n.
- 2) Repeat steps 4 to 9 in 4.1.1, Voltage Ramp and Device Initialization.

Table 19 — Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100		ns	Min RESET_n low time for Reset initialization with stable power

4.1.3 Power-off Sequence

The following procedure is required to power off the SDRAM.

While powering off, CS must be held LOW ($\leq VILPD$) and all other inputs must be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while CS is held LOW. DQ, DMI, WCK_t and WCK_c, RDQS_t, CK_t, CK_c and CA voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. RESET_n input levels must be between VSS and VDD2H during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the SDRAM is powered off.

Table 20 — Power Supply Conditions

Between	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2H
	VDD2H must be equal to or greater than VDD2L
	VDD2L must be greater than VDDQ-200mV

4.1.4 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the SDRAM must power off. Between Tx and Tz the relative voltage between power supplies is uncontrolled. VDD1, VDD2H and VDD2L must decrease with a slope lower than $0.5V/\mu s$ between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the SDRAM.

Table 21 — Power Supply Conditions

Parameter	Value		Unit	Comment
	Min	Max		
tUNCTL_POFF	-	2	s	Maximum Power-Off ramp down time

4.2 Training

4.2.1 ZQ Calibration

Two ZQ calibration modes are supported - Background Calibration or Command-Based Calibration. In Background Calibration mode, calibration of the output driver and CA/DQ ODT impedance across process, temperature, and voltage occurs in the background of device operation and is designed to eliminate any need for coordination among channels (that is, it allows for channel independence) within a single package. Systems may also select Command-Based Calibration mode, which operates in a fashion similar to LPDDR4 devices. Command-Based Calibration mode is selected by setting MR28 OP[5]=1_B.

ZQ re-calibration may be required as the LPDDR5 SDRAM voltage and/or temperature changes due to changes in the system environment. ZQ calibration can only be performed when the VDDQ voltage is set to nominal 0.5v DC or above (i.e., when DVFSQ is not active). In Background Calibration mode, the calibration shall be halted by the memory controller setting ZQ Stop when VDDQ is set to a nominal DC level below 0.5v or when VDDQ is being slewed between levels (i.e., when DVFSQ is active). In Command-Based mode, ZQCal Start commands are illegal when DVFSQ is active unless ZQ Stop is set. See 4.2.1.2, ZQ Stop Functionality, for more information.

Changing CA ODT values (MR11-OP[6:4]) and/or DQ ODT values (MR11-OP[2:0]) will not alter the existing recalibration scheme, therefore there is no need for immediate recalibration.

4.2.1.1 Calibration

4.2.1.1.1 Calibration During Powerup and Initialization

ZQ calibration is automatically performed by all LPDDR5 die during the initialization/powerup sequence before Td shown in **Figure 13**

Figure 13, in the Power-up, Initialization, and Power-off Procedure section of this standard. A ZQCal Latch command shall be issued to all LPDDR5 die on or after Tg regardless of the state of ZQUF. ZQ Calibration mode selection may be changed any time after Tf. For more details about changing ZQ Calibration modes see 4.2.1.1.8.

4.2.1.1.2 Background Calibration

In this mode pull-down/ODT and pull-up/VOH calibration will be performed in the background and kept up-to-date by the DRAM. Re-calibration will be performed by the LPDDR5 SDRAM within the time interval, tZQINT, specified in MR28 OP[3:2]. No ZQCal Start commands are required, and any ZQCal Start commands received by the DRAM will be ignored.

Pull-down/ODT calibration is controlled by each DRAM die using an external ZQ resistor connected between VDDQ and a package ball or pin (ZQ resources). These ZQ resources may be shared among a number of DRAM die up to a maximum of NZQ. Calibration will be automatically performed as part of power-up/initialization and after RESET_n assertion. Subsequent re-calibration will be kept up-to-date by the DRAM. Self-arbitration by the DRAM insures that up to NZQ die within a package can share a common external ZQ resistor and avoid conflicts. Noise immunity will not be compromised when sharing the external ZQ calibration resistor.

4.2.1.1.2 Background Calibration (Cont'd)

When automatic pull-down/ODT calibration is complete, pull-up/VOH calibration will start automatically. At the completion of pull-down/ODT and pull-up/VOH calibration, MR4 OP[5] bit (ZQUF) will be set if the new calibration codes do not match the currently latched codes. An MRR of this bit will notify the system that new calibration results are available and that a ZQCAL Latch command (following ZQCAL Latch timing constraints) should be issued to ensure accurate calibration of Pull-down, ODT and VOH is consistently maintained. Setting of ZQUF is unique to each die regardless of configuration or sharing of the ZQ pin or pins. Alternatively, the memory controller may choose not to monitor ZQUF and periodically issue ZQCAL Latch commands.

Setting the MR28 OP[1]=ZQ Stop will halt all background calibration activity. Re-setting MR28 OP[1] to zero will immediately start a calibration sequence, where all DRAM die sharing the ZQ resource will re-calibrate in a serial fashion. This enables rapid recalibration when exiting from DVFSQ-active mode where recalibration was not possible.

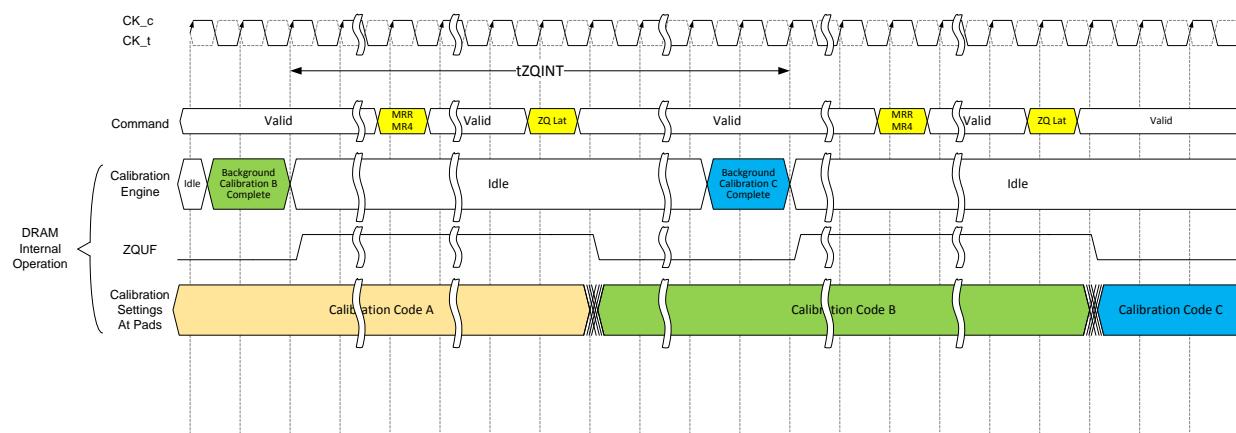


Figure 14 — Background ZQ Calibration Timing

4.2.1.1.3 Latching ZQ Calibration Results in Background Calibration Mode

Latching ZQ calibration results is accomplished with the MPC ZQCAL Latch command. This command loads new calibration results into the pull-down/ODT devices and pull-up drivers.

A ZQCAL Latch command may be issued anytime outside of power-down when there are no DQ operations pending or in progress. The results from the most-recently completed calibration will always be latched with each ZQCAL Latch command. If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQLAT to allow CA ODT calibration settings to be updated. In any case, operations that initiate DQ operations are always dis-allowed during tZQLAT.

The DQ and CA ODT calibration values will not be updated until ZQCAL Latch command is performed and tZQLAT has been met, with the following exceptions:

- ZQ calibration will automatically occur for each LPDDR5 die on power up/initialization and after Reset_n pin assertion. A ZQCAL Latch command shall be issued to all LPDDR5 die on or after Tg.
- Calibration results are automatically applied when switching to a new Frequency Set Point. The new calibration values will be loaded into the pull-down/ODT devices and pull-up drivers before the expiration of tFC.

When a ZQCAL Latch command is executed, the ZQUF bit will be reset to 0 before expiration of tZQLAT.

4.2.1.1.4 Command-Based Calibration

When Command-based calibration mode is selected, a ZQCal Start command may be periodically issued to the ZQ master die or dice in each DRAM package to maintain accurate calibration. ZQCal Start commands may only be issued when DVFSQ is not active. The memory controller may read MR4 OP[6] to determine which DRAM die in a package is designated as ZQ Master. The designation of ZQ Master is hard-coded by the DRAM vendor. ZQCal Start commands issued to DRAM die that are not designated ZQ Master will be ignored.

When the ZQ master die is placed in power down or deep sleep mode, ZQCal Start commands will be ignored and re-calibration will not occur for all die sharing the ZQ resources. All die will be re-calibrated only when the ZQ master die exits power down or deep sleep mode and receives a subsequent ZQCal Start command.

When the ZQ Master die remains in an active mode and receives a valid ZQCal Start command, any slave die sharing ZQ resources that are in power down or deep sleep mode will also recalibrate normally. Systems where DRAM die sharing ZQ resources can operate in a mixed fashion (some die operating, some in power down or deep sleep mode) should note the ZQ master die designation when determining configuration if re-calibration will be required in mixed mode.

4.2.1.1.5 Latching ZQ Calibration Results in Command-Based Calibration Mode

In Command-based calibration mode, following a ZQCal Start command a ZQCal Latch command should be issued to each die after tZQCAL4, tZQCAL8 or tZQCAL16 has been met. tZQCAL4 applies to LPDDR5 DRAM die where the ZQ resource is shared among four or fewer DRAM die. tZQCAL8 applies to LPDDR5 DRAM die where the ZQ resource is shared among four and up to eight DRAM die. tZQCAL16 applies to LPDDR5 DRAM die where the ZQ resource is shared among more than eight DRAM die, up to the maximum of sixteen (NZQ).

The ZQCal Latch command will load the most recent calibration results to the LPDDR5 output driver and ODT devices. In cases where the correct tZQCAL4, tZQCAL8, or tZQCAL16 delay time is not met, the LPDDR5 DRAM may latch a previous valid calibration result but in no case shall latch an invalid result. As in background calibration mode, a ZQCal Latch command may be issued anytime outside of power-down when there are no DQ operations pending or in progress. The value of ZQUF is undefined when Command-Based Calibration mode has been selected.

If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQLAT to allow CA ODT calibration settings to be updated. In any case operations that initiate DQ operations are always dis-allowed during tZQLAT.

The DQ and CA ODT calibration values will not be updated until ZQCal Latch is performed and tZQLAT has been met, with the following exceptions:

- ZQ calibration will automatically occur for each LPDDR5 die on power up/initialization and after Reset_n pin assertion. A ZQCal Latch command shall be issued to all LPDDR5 die on or after Tg.
- Calibration results are automatically applied when switching to a new Frequency Set Point. The new calibration values will be loaded into the pull-down/ODT devices and pull-up drivers before the expiration of tFC.

4.2.1.1.6 Maintaining Accurate Calibration - Background Calibration Mode

To maintain Pull-down/ODT calibration and Voh calibration when DVFSQ is not active:

- 1) Periodically, based on tZQINT, issue an MRR to MR4 to check the ZQUF OP[5] bit status for each LPDDR5 die.
- 2) If MR4 OP[5]=1, issue a ZQCal Latch command.

Repeat 1-2 as needed. Alternatively the memory controller may choose not to monitor ZQUF and periodically issue ZQCal Latch commands. In this case the most-recently-completed calibration results will always be latched, and will be no older than tZQINT.

It may be permissible for the memory controller to ignore ZQUF and not issue ZQCal Latch commands if both of the following are true:

- CA ODT is disabled
- The LPDDR5 SDRAM is in an idle state, or in Self Refresh or Power Down mode.

Re-calibration will still occur in the background to ensure accurate driver/ODT settings are available should they be needed. In this case, the memory controller should ensure a ZQCal Latch command is performed prior to resuming data traffic if ZQUF is set.

When DVFSQ is active, MR28 OP[1] ZQ Stop shall be set for each LPDDR5 die to ensure recalibrations are inhibited. When DVFSQ is no longer active, ZQ Stop may be de-asserted, which will immediately begin a recalibration and enable subsequent periodic background calibrations. When the memory controller de-asserts ZQ Stop it shall reset MR28 OP[1] to zero for all die sharing the ZQ resource within 100ns as described in 4.2.1.2.2. The ZQUF will be updated and results from the recalibration can be latched after the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) has been satisfied.

4.2.1.1.7 Maintaining Accurate Calibration - Command-Based Calibration Mode

To maintain Pull-down/ODT calibration and VOH calibration when DVFSQ is not active:

- 1) Periodically, as system conditions warrant, issue a ZQCal Start command to the ZQ Master die.
- 2) After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16), issue a ZQCal Latch command to each die.

Repeat 1-2 as needed.

When DVFSQ is active no recalibration may be performed.

4.2.1.1.8 Changing between Calibration Modes

Changing between calibration modes may be performed any time after powerup and initialization time T_f when the device is not in power-down or deep sleep mode.

4.2.1.1.8.1 Changing between Calibration Modes when DVFSQ is not active

To change from Background Calibration Mode to Command-Based Calibration mode for all die sharing a ZQ resource when DVFSQ is not active:

- 1) Write the ZQ Master die MR28 OP[5] = 1B. MR28 OP[5] may also be updated on ZQ Slave die but it is not required as this bit is ignored by the LPDDR5 ZQ Slave die.
- 2) Wait t_{ZQCALx}
- 3) Begin to issue ZQCal Start commands to the ZQ Master die and subsequent ZQ Latch commands to all die to begin periodic command-based calibration as described in 4.2.1.1.7.

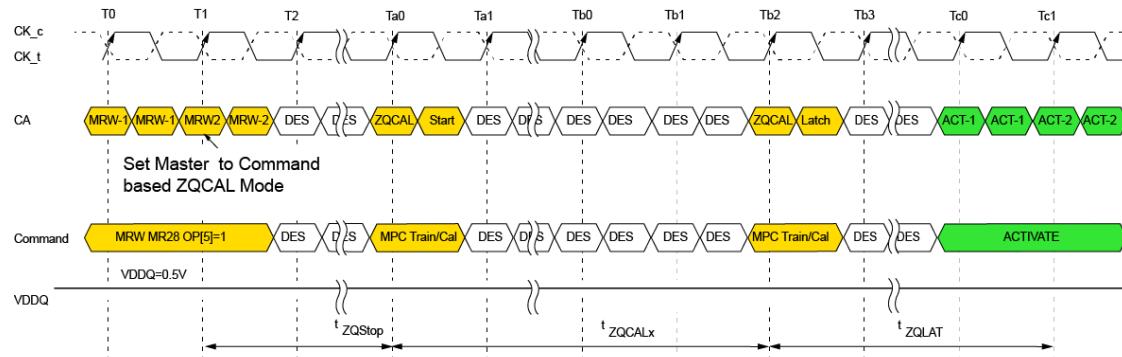


Figure 15 — Background to Command-based Switching when DVFSQ is not active

To change from Command-Based Calibration mode to Background Calibration mode for all die sharing a ZQ resource when DVFSQ is not active:

- 1) Ensure t_{ZQCALx} has been met from any previous ZQCal Start command.
- 2) Write the ZQ Master die MR28 OP[5] = 0B. MR28 OP[5] may also be set to 0B on ZQ Slave die if desired.
- 3) Issue ZQCal Latch commands as described in 4.2.1.1.6.

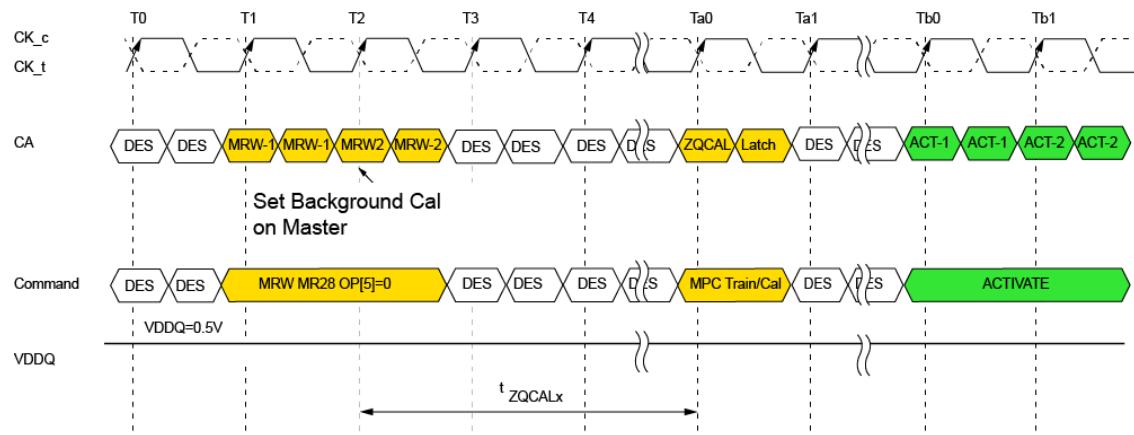


Figure 16 — Command-based to Background Switching when DVFSQ is not active

4.2.1.1.8.2 Changing between Calibration Modes when DVFSQ is active

To change from Background Calibration Mode to Command-Based Calibration mode for all die sharing a ZQ resource when DVFSQ is active:

- 1) Write the ZQ Master die MR28 OP[5] = 1B. MR28 may also be updated on ZQ Slave die but it is not required as this bit is ignored by the LPDDR5 ZQ Slave die.
- 2) MR28 OP[1] ZQ Stop shall be written to 0B for all die sharing the ZQ resource. This may occur simultaneously with the write to MR28 OP[5], or at any time at least tZQSTOP before a ZQCal Start command may be issued to the ZQ Master die (when DVFSQ is no longer active).

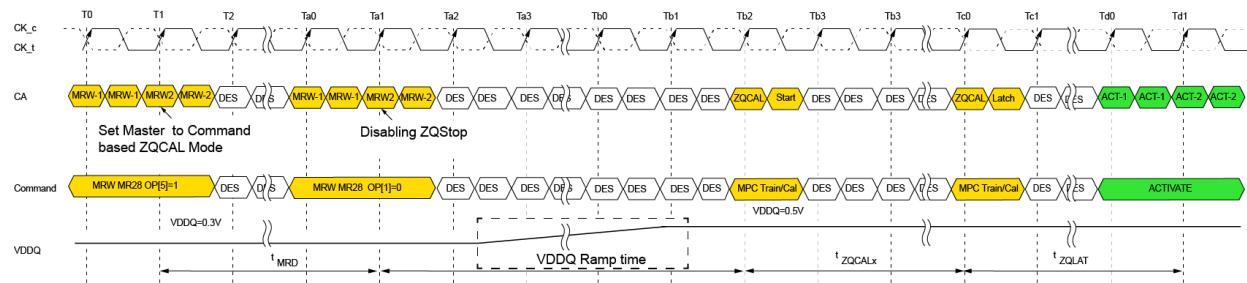


Figure 17 — Background to Command-based Switching when DVFSQ is active

To change from Command-Based Calibration mode to Background Calibration mode for all die sharing a ZQ resource when DVFSQ is active:

- 1) Write all ZQ Slave die MR28 OP[1] = 1_B.
- 2) Write the ZQ Master die MR28 OP[5] = 0_B and MR28 OP[1] = 1_B. These writes should occur simultaneously - if not simultaneously MR28 OP[1] shall be written first.
- 3) After DVFSQ is no longer active MR28 OP[1] shall be written to 0_B for all die sharing the ZQ resource.

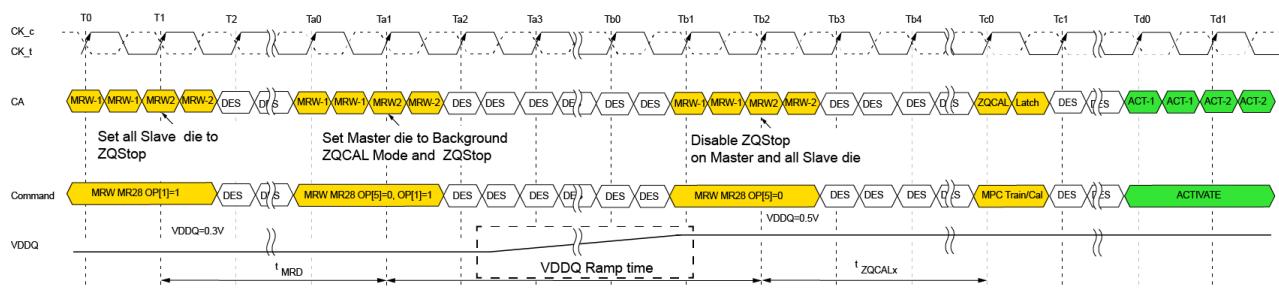


Figure 18 — Command-based to Background Switching when DVFSQ is active

4.2.1.2 ZQ Stop Functionality

4.2.1.2.1 ZQ Resistor Sharing by Another Device(s)

4.2.1.2.1.1 ZQ Resistor Sharing in Background Calibration Mode

In Background Calibration mode, a ZQ Stop function is provided to enable another device or devices to share the ZQ resistor. This function is enabled by MR28 OP[1]=ZQ Stop. When another device needs use of the ZQ resistor, MR28 OP[1] shall be set to 1 for all LPDDR5 devices that share ZQ resources. This will halt background calibration operations within delay time tZQSTOP (see Table 22) for each LPDDR5 device. Once tZQSTOP has expired for all LPDDR5 devices that share the ZQ resource another device may use the resource. When the ZQ resource is no longer needed by the other device or devices the ZQ Stop MR bit should be reset to 0 to allow background calibrations to continue normally. When the ZQ Stop MR bit is reset to 0 periodic background calibrations will be restarted.

Since ZQ Stop inhibits the LPDDR5 devices from recalibrating, note that changing system conditions while the ZQ Stop MR bit is set may cause the LPDDR5 ZQ calibration accuracy to deviate from specification. To ensure continued accurate calibration as discussed above, the ZQ Stop MR bit shall not be set for longer than tZQINT when set to background calibration mode, or the normal application-specific ZQCal Start command interval when set to command-based calibration mode.

4.2.1.2.1.2 ZQ Resistor Sharing in Command-Based Calibration Mode

In command-based calibration mode, ZQCal Start commands shall not be issued to the ZQ master die while the ZQ resistor is being used by any other device unless the ZQ Stop is set. The memory controller shall ensure tZQCAL4, tZQCAL8 or tZQCAL16 from the most-recent ZQCal Start command has been met before allowing any device to use the ZQ resistor unless the ZQ Stop bit is set. The LPDDR5 device will ignore ZQCal Start commands received when MR28 OP[1] ZQ Stop is set to 1_B.

4.2.1.2.2 Stopping Background Calibration when DVFSQ is active

In Background Calibration mode, the calibration shall be halted by setting ZQ Stop before DVFSQ is entered. ZQ Stop may be reset to 0 when DVFSQ is no longer active (when VDDQ is returned to a 0.5v nominal level). Resetting of ZQ Stop will start background calibration(s) immediately. After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) from resetting of ZQ Stop on the ZQ Master die, the memory controller may check the ZQUF flags, or may issue a ZQCal Latch command to all die sharing the ZQ resource. To guarantee recalibration of all die sharing the ZQ resource within tZQCAL, the MR28 OP[1] ZQ Stop bit shall be reset for all slave die sharing the ZQ resource either before, or no later than 100ns after, the MR28 OP[1] ZQ Stop bit is reset on the ZQ master die.

4.2.1.2.3 Stopping Background Calibration when VDDQ is Powered Off

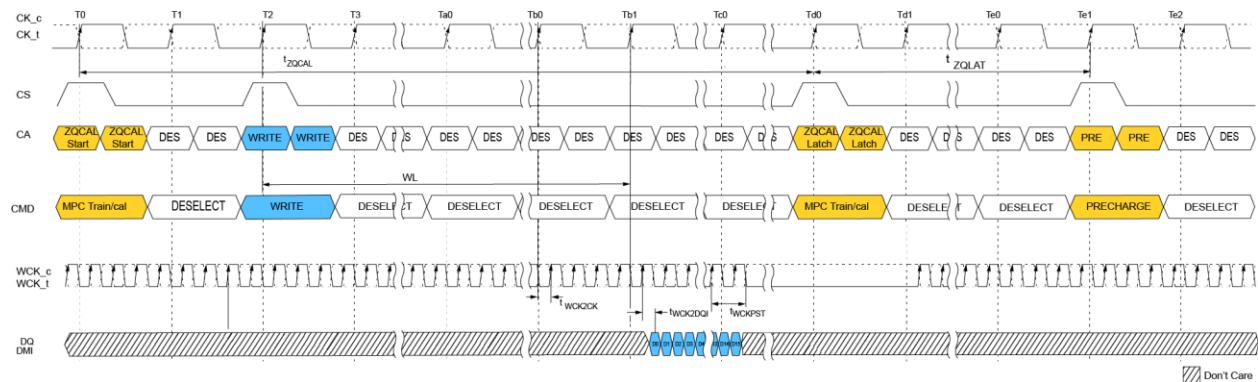
In Background Calibration mode, before entering Power-down mode, the calibration shall be halted by setting ZQ Stop when VDDQ is going to be powered off. When Power-down mode is exited ZQ Stop should be reset to 0 to re-enable background calibration. Resetting of ZQ Stop on the ZQ Master die will start background calibration(s) immediately. After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) from resetting of ZQ Stop, the memory controller may check the ZQUF flags, or may issue a ZQCal Latch command to each die sharing the ZQ resource. To guarantee recalibration of all die sharing the ZQ resource within tZQCAL, the MR28 OP[1] ZQ Stop bit shall be reset for all slave die sharing the ZQ resource either before, or no later than 100ns after, the MR28 OP[1] ZQ Stop bit is reset on the ZQ master die.

Table 22 — ZQ Calibration Timing Parameters

Parameter	Symbol	Min/ Max	Value	Units
ZQ Calibration Command to Latch Time, $NZQ \leq 4$	tZQCAL4	Min	1.5	μs
ZQ Calibration Command to Latch Time, $4 < NZQ \leq 8$	tZQCAL8	Min	3	μs
ZQ Calibration Command to Latch Time, $NZQ 8 < NZQ \leq 16$	tZQCAL16	Min	6	μs
ZQ Calibration Latch Time	tZQLAT	Min	MAX(30ns,4nCK)	ns
ZQ Calibration Reset Time	tZQRESET	Min	MAX(50ns,3nCK)	ns
Delay Time from ZQ Stop Bit Set to ZQ Resistor Available	tZQSTOP	Max	30	ns
Background Calibration Interval	tZQINT	Max	Programmable, 32, 64, 128, or 256	ms
Maximum Number of LPDDR5 Devices (die) Connected to a Single ZQ Resistor	NZQ	Max	16	Die
Maximum Capacitive Load on ZQ Network	CZQ	Max	TBD	pF

4.2.1.3 ZQ Reset

Setting the ZQ Reset MR bit resets the output impedance calibration to a default accuracy of $\pm 30\%$ across process, voltage, and temperature. The ZQ Reset command is executed by writing MR28-OP[0] = 1_B. The ZQ Reset command will also reset the ZQ Stop MR28 OP[1] and ZQUF MR4 OP[5] bits to 0. ZQ Reset will not change the state of the ZQ Mode or ZQ Interval MR bits MR28 OP[5] or OP[3:2]. If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQRESET to allow CA ODT calibration settings to be updated. In any case, operations that initiate DQ operations are always dis-allowed during tZQRESET. The ZQ Reset MR bit shall be reset to 0_B by the DRAM after tZQRESET. To reset the ODT and output impedance in a multi-die package, the ZQ Reset function shall be issued to all die regardless of ZQ Master or ZQ Slave designation.



NOTE 1 WRITE and PRECHARGE operations are shown for illustrative purposes. Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.

NOTE 2 Before the ZQCAL Latch command can be executed, any prior commands that utilize the DQ bus shall have completed.

Figure 19 — ZQCAL Timing

WRITE commands with DQ termination shall be given enough time to turn off the DQ ODT before issuing the ZQCAL Latch command. See 7.6.4 for ODT timing.

4.2.1.4 Multi-die Package Considerations

Up to NZQ LPDDR5 devices within a single package may connect to the same ZQ resistor. ZQCAL Start commands (when in command-based calibration mode) are required for the master die and may be issued to other memory die sharing a ZQ resource asynchronously or simultaneously. ZQCAL Start commands to non-master die are ignored. ZQCAL Latch commands, when required, are necessary for each die. When multiple die share a ZQ resource and a ZQ master die is managing calibration (when DVFSQ is inactive, either in background mode or by accepting ZQCAL Start commands), the MR28 OP[1] ZQ Stop bit shall be set to 0B for all ZQ slave die sharing the ZQ resource. No other arbitration considerations are required.

4.2.1.4.1 Other Considerations in Background Calibration Mode

Each LPDDR5 die includes a single ZQ pin and associated ZQ calibration circuitry. Calibration values from this circuit will be generated and used according to the following protocol:

- Setting of the ZQ Stop bit always has priority over background calibration processes.
- If the ZQ Stop MR bit is set to 1 while a background ZQ calibration is in progress, the background calibration will be interrupted.
- A background calibration will start immediately when the ZQ Stop MR bit is reset to 0.
- A background calibration will not start while the ZQ Stop MR bit is set to 1.
- The ZQUF bit will not be reset by setting of the ZQ Stop bit to 1.
- The ZQUF bit will be reset only by a ZQCAL Latch command or ZQ Reset.
- The ZQUF bit will be set if calibration codes do not match the currently latched codes even when the device is in Self-refresh or Power-down mode, providing ZQ Stop is not set.

4.2.1.5 Other Considerations in Command-Based Calibration Mode

Packages include one or more ZQ pin(s) and associated ZQ calibration circuitry. Calibration values from this circuit or circuits will be generated and used according to the following protocol:

- ZQCAL Latch commands that do not meet the corresponding tZQCAL4, tZQCAL8 or tZQCAL16 may latch the results of the previous most recently completed ZQ calibration.

4.2.1.6 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm, $\pm 1\%$ tolerance external resistor shall be connected between the ZQ pin and VDDQ.

The total capacitive loading on the ZQ pin shall be limited to CZQ.

4.2.1.7 Flow Chart Examples

These example flow charts are representative only of one set of LPDDR5 die that share a single ZQ resource. These are examples only, there may be other valid methods of operation.

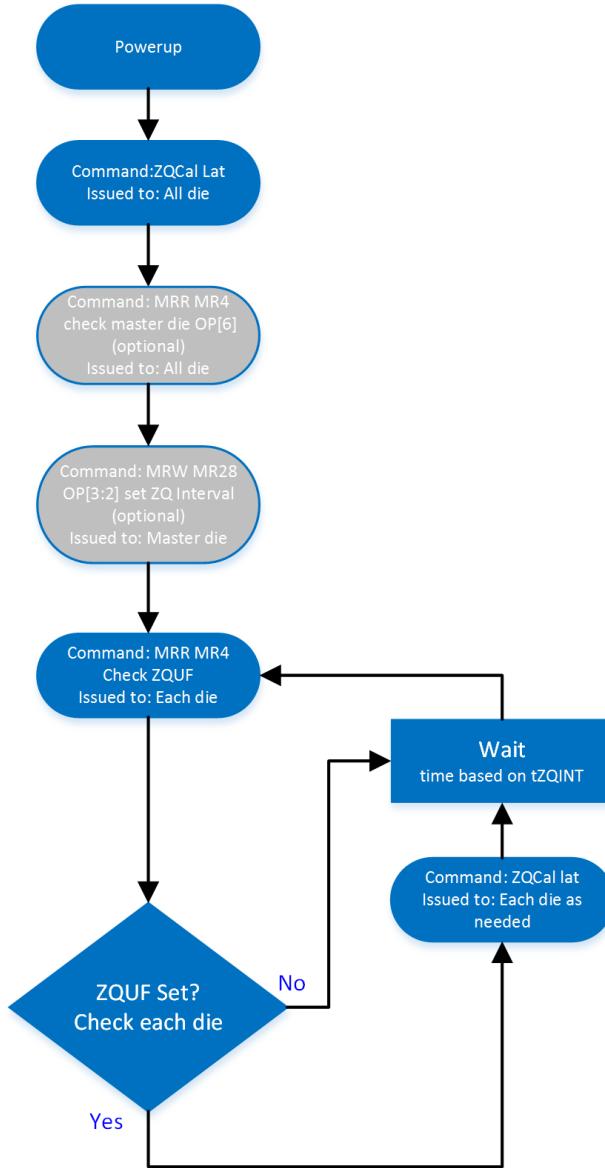


Figure 20 — Initialization to Background Calibration Flow Chart, no DVFSQ support

4.2.1.7 Flow Chart Examples (Cont'd)

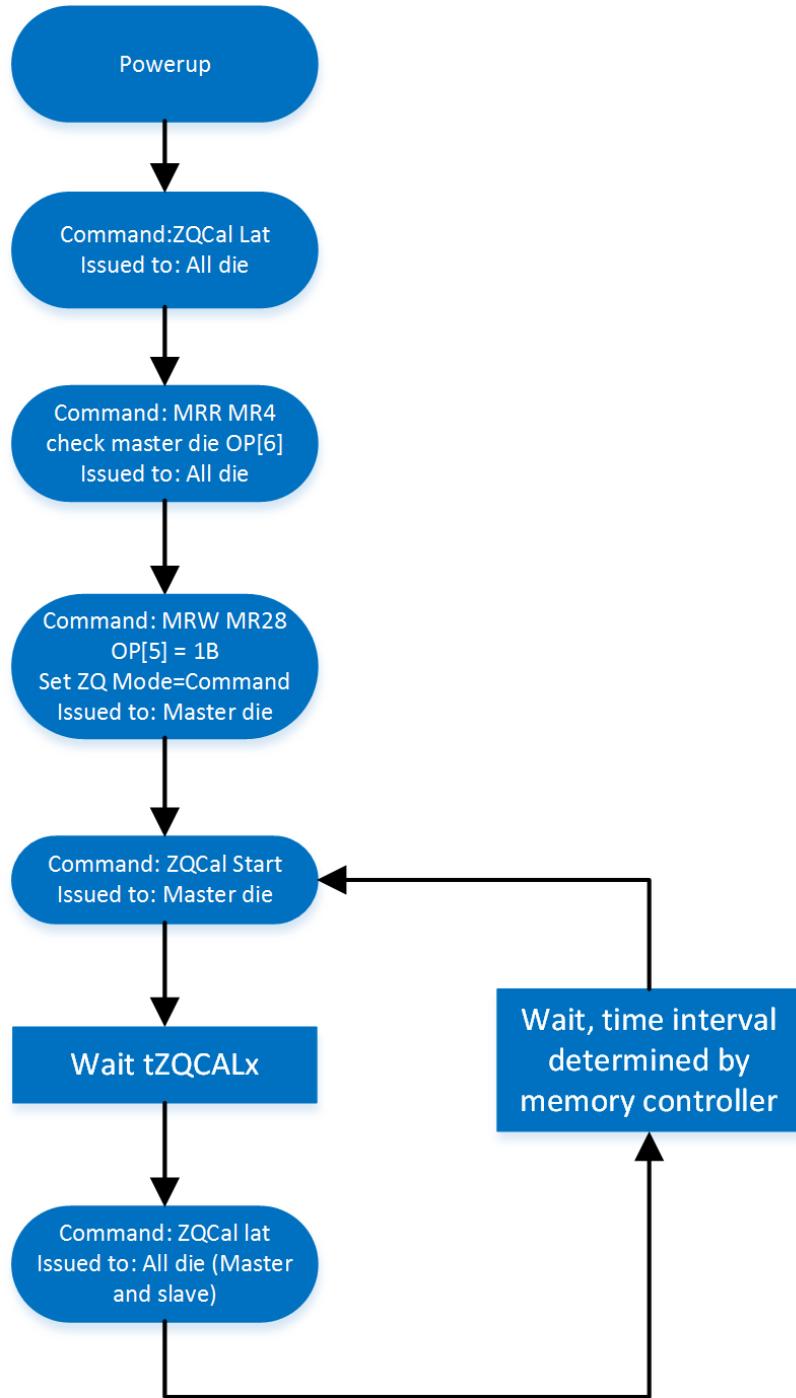


Figure 21 — Initialization to Command-based Calibration Flow Chart,
no DVFSQ support, option 1 (check Master)

4.2.1.7 Flow Chart Examples (Cont'd)

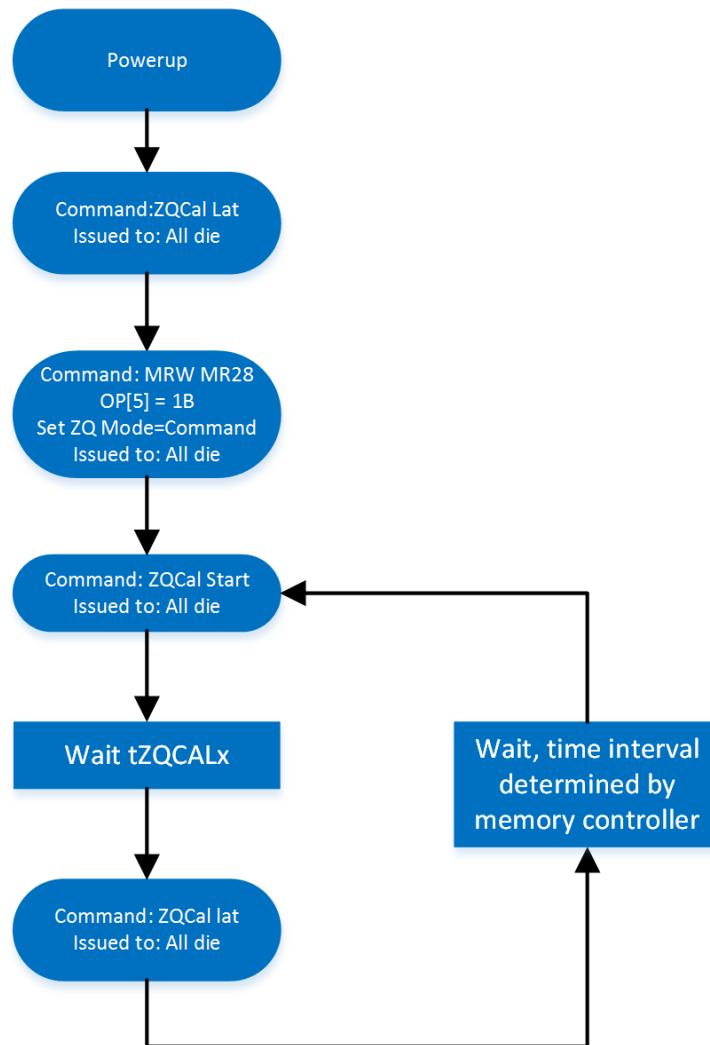


Figure 22 — Initialization to Command-based Calibration Flow Chart,
no DVFSQ support, option 2 (ignore Master)

4.2.1.7 Flow Chart Examples (Cont'd)

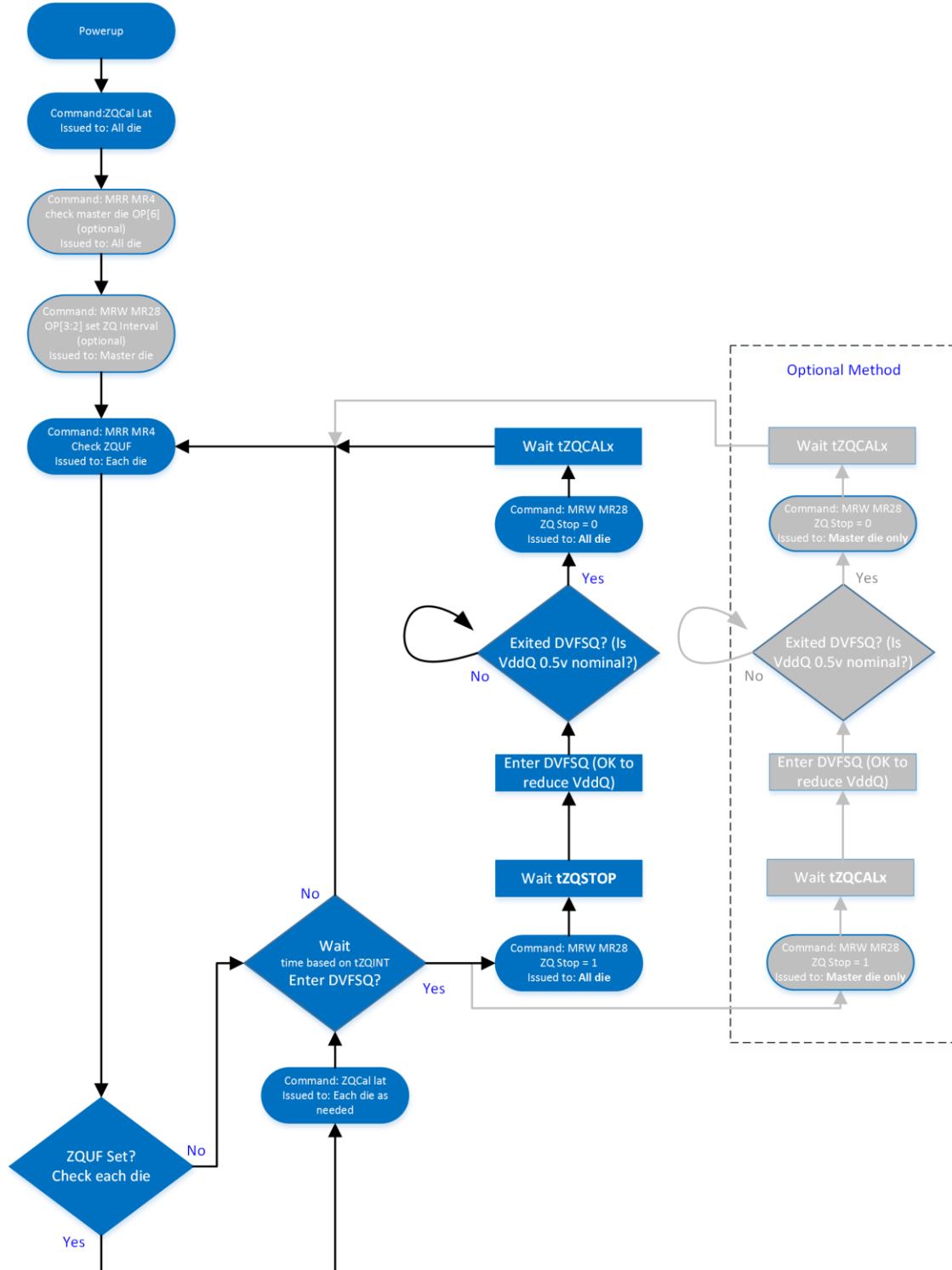


Figure 23 — Initialization to Background Calibration Flow Chart, with DVFSQ support

4.2.1.7 Flow Chart Examples (Cont'd)

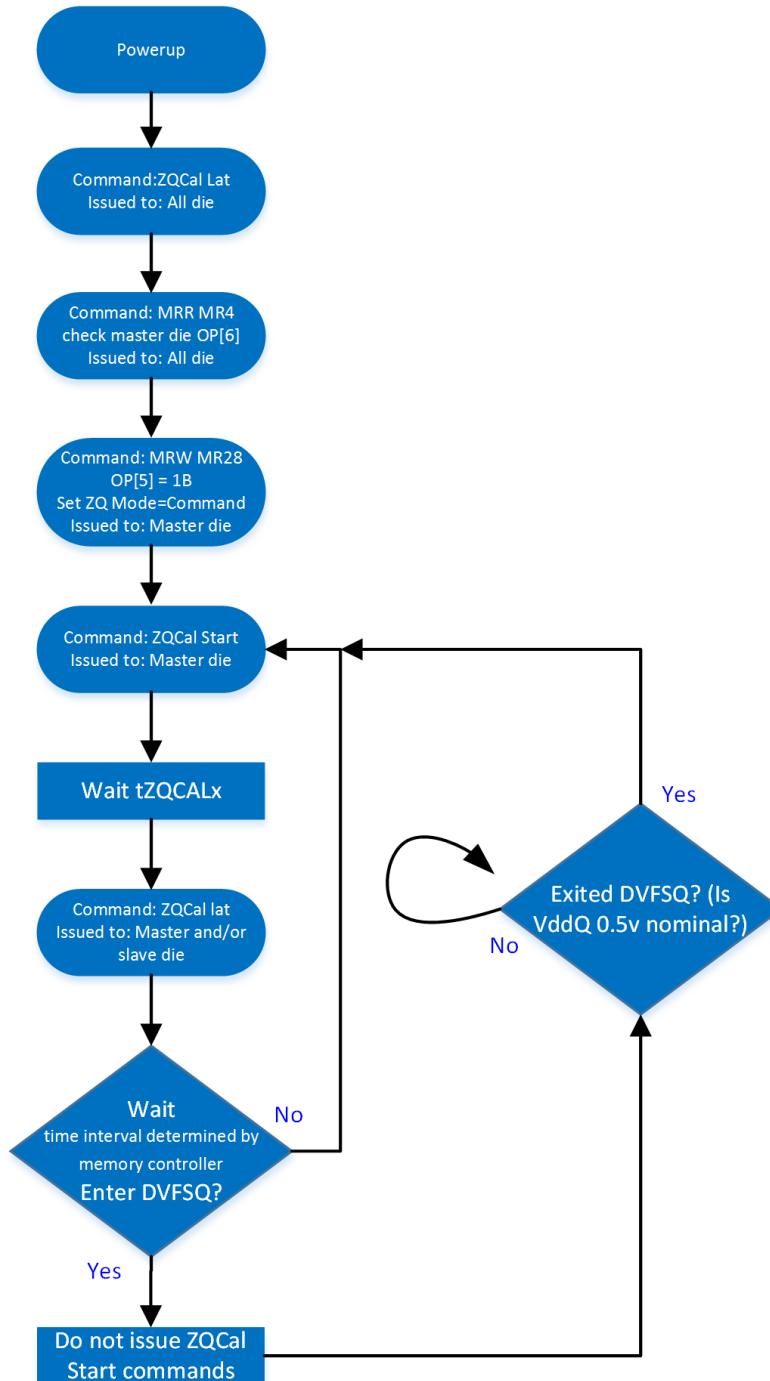


Figure 24 — Initialization to Command-based Calibration Flow Chart, with DVFSQ support

4.2.2 Command Bus Training

The LPDDR5 SDRAM command bus must be trained before enabling termination for high-frequency or mid-frequency operation. LPDDR5 provides an internal VREF(CA) that default level is suitable for un-terminated, low-frequency operation, but the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency or mid-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. For the training sequence simplicity and difficulty to capture CA inputs prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training.

The LPDDR5 SDRAM supports two Command Bus Training modes and their feature is as follows. CBT mode is selected by MR13 OP[6] (CBT mode1 : MR13 OP[6] = 0, CBT mode2 : MR13 OP[6] =1).

In multi-rank/channel system sharing the CS/CA bus, the terminated die should be trained first, followed by the nonterminated die(s). See 7.6.4, ODT, for more information.

The Corresponding DQ pins in this definition may differ depending on the package configuration. For example, in case of a package which contains Byte-mode devices, DQ[15:8] and DMI[1] balls can be connected to DQ[7:0] and DMI[0] pads of byte-mode device.

4.2.2.1 Command Bus Training Mode1

The LPDDR5 SDRAM uses Frequency Set Points to enable multiple operating settings for the die. The LPDDR5 SDRAM is initiated to FSP-OP[0] at power-up, which has the default settings to operate in unterminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR16 OP[1:0] for FSP-WR (Frequency Set Point Write Enable), setting all other mode register bits for FSP-OP (Frequency Set Point Operation Mode) to make the desired settings for high-frequency or mid-frequency operation, and setting MR16 OP[5:4] for Command Bus Training Mode selection.

Prior to entering Command Bus Training, the LPDDR5 SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when DQ[7] is driven HIGH, the LPDDR5 SDRAM will automatically switch to the alternate FSP register set FSP-OP[y] or FSP-OP[z] according to MR16 OP[5:4] and use the alternate register settings during training (See Figure 25, Note 4, for more information on FSP-OP register sets). Upon Command Bus Training exit when DQ[7] is driven LOW, the LPDDR5 SDRAM will automatically switch back to the original FSP register set FSP-OP[x], returning to the “known-good” state that was operating prior to training. The training values for VREF(CA) are not retained by the DRAM in FSP-OP[y] or FSP-OP[z] registers, and must be written to the registers after training exit.

LPDDR5 SDRAM can select the Command Bus Training CA phase by MR16 OP[7] setting. If MR16 OP[7] is LOW, DQ outputs CA pattern latched by CK rising edge. If MR16 OP[7] is HIGH, DQ outputs CA pattern latched by CK falling edge.

- 1) Set MR13 OP[6]=0 for Command Bus Training Mode1.
- 2) To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR16 OP[5:4] for the CBT mode selection and drive LOW to DQ[7], WCK_t and drive HIGH to WCK_c. WCK_t, WCK_c are input pins for capturing DQ[7] level by its toggling. WCK ODT value is fixed regardless of MR18 setting. WCK_t and WCK_c have to toggle tWCK2DQ7H before DQ[7] goes HIGH. DQ ODT state is off during CBT mode.
- 3) DQ[7] is driven HIGH and when LPDDR5 SDRAM samples HIGH level of DQ[7] by WCK, the LPDDR5 SDRAM switches from FSP-OP[x] to FSP-OP[y] or FSP-OP[z] completing the entry into Command Bus Training mode.
- 4) At time tCAENT later, LPDDR5 SDRAM can accept to input CA training pattern via CA bus.
- 5) To verify that the receiver has the correct VREF(CA) setting and to further train the CA eye relative to clock(CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
- 6) To exit Command Bus Training mode, drive DQ[7] LOW and after time tDQ7LWCK + tVREFCA_LONG issue the MRW command to set MR16 OP[5:4] = 00B. After time tMRD the LPDDR5 SDRAM is ready for normal operation. After training exit, the LPDDR5 SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may be entered from IDLE or Self Refresh states. When entering CBT, the SDRAM must not be in a Power Down state or Deep Sleep Mode. Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

Table 23 — Mapping of CA Input pin and DQ Output pin

Mapping							
CA Number	CA6	CA5	CA4	CA3	CA2	CA1	CA0
DQ Number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

4.2.2.1 Command Bus Training Mode1 (Cont'd)

Training Sequence for single-rank systems

Note that an example shown here is assuming an initial low-frequency, untermination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency; the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition: Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point "Y" (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- 5) Drive DQ[7] HIGH, and then change CK frequency to the high frequency operating point.
- 6) Perform Command Bus Training (CS and CA).
- 7) Exit training by driving DQ[7] LOW, change CK frequency to the low frequency operating point prior to driving DQ[7] Low, and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 8) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained and other training or normal operation can be executed.

Training Sequence for multi-rank systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency; the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition: Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation.

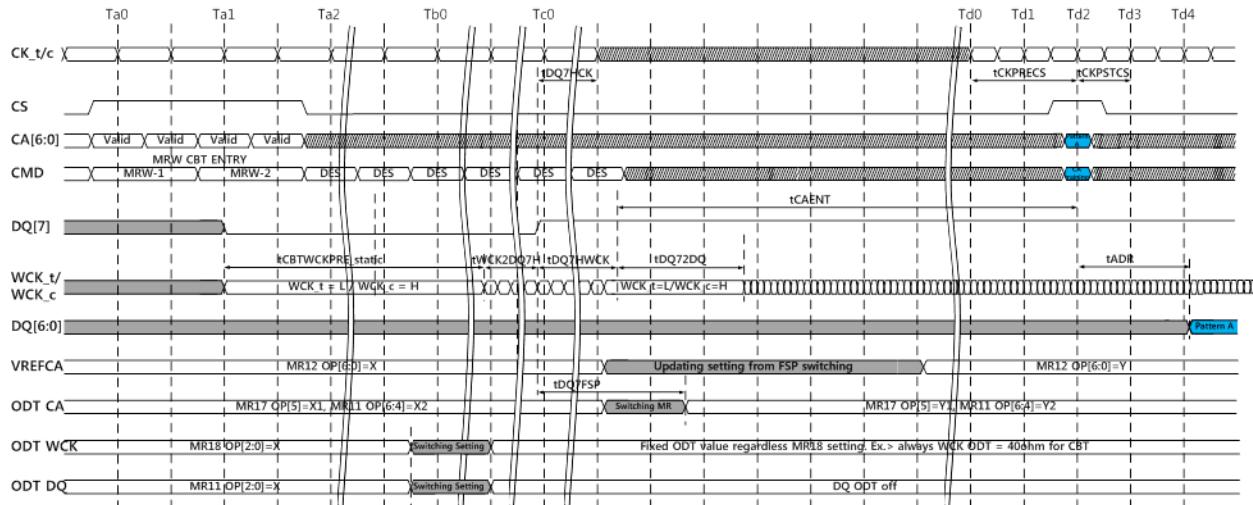
- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point "Y" (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
- 5) Drive DQ[7] HIGH on the terminating rank (or all ranks), and then change CK frequency to the high frequency operating point.
- 6) Perform Command Bus Training on the terminating rank (CS and CA).
- 7) Exit training by driving DQ[7] LOW on the terminating rank, change CK frequency to the low frequency operating point prior to driving DQ[7] Low, and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 8) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.

4.2.2.1 Command Bus Training Mode1 (Cont'd)

- 9) Issue MRW-1 and MRW-2 commands to enter training mode on the non-terminating rank (but, keep DQ[7] LOW).
- 10) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operating point.
- 11) Drive DQ[7] HIGH on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y].
- 12) Perform Command Bus Training on the non-terminating rank (CS and CA).
- 13) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] to turn off termination.
- 14) Exit training by driving DQ[7] LOW on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 15) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 16) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained for both ranks and other training or normal operation can be executed.

4.2.2.1 Command Bus Training Mode1 (Cont'd)

The basic timing diagrams of Command Bus Training Mode1 are shown in Figure 25, Figure 26, and Figure 27.



NOTE 1 After tDQ7HCK, clock can be stopped or frequency changed any time.

NOTE 2 The input clock condition should be satisfied tCKPRECS.

NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.

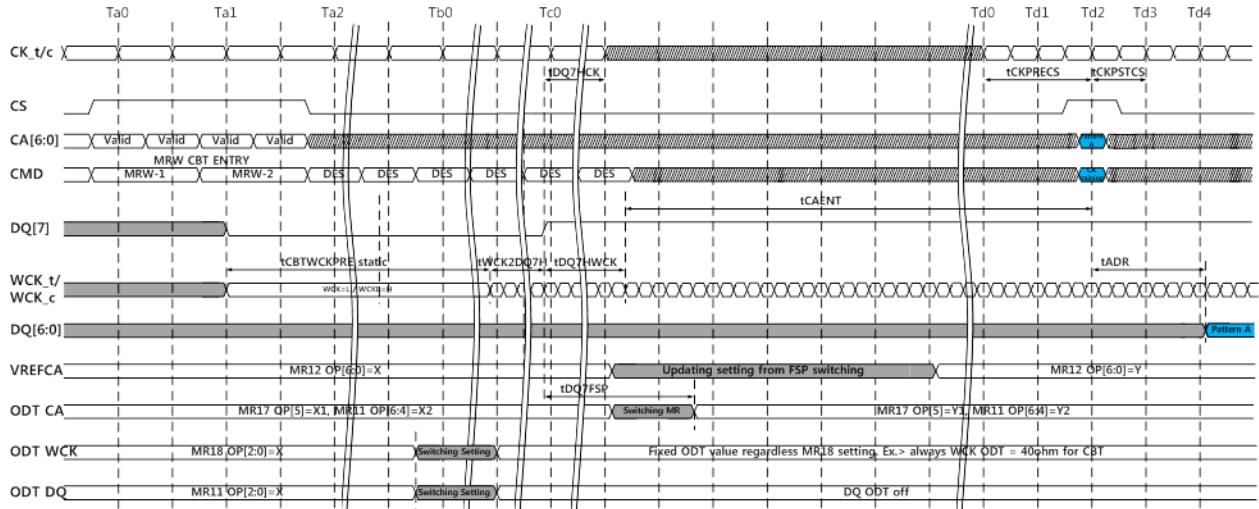
NOTE 4 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate(i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled then termination will not enable in CA Bus Training mode.

NOTE 5 WCK/DQ ODT states are set one fixed ODT state during CBT operation.

NOTE 6 During tDQ72DQ, WCK can be stop and changed frequency after FSP change.

Figure 25 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change)

4.2.2.1 Command Bus Training Mode1 (Cont'd)



NOTE 1 After tDQ7HCK, clock can be stopped or frequency changed any time.

NOTE 2 The input clock condition should be satisfied tCKPRECS.

NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH

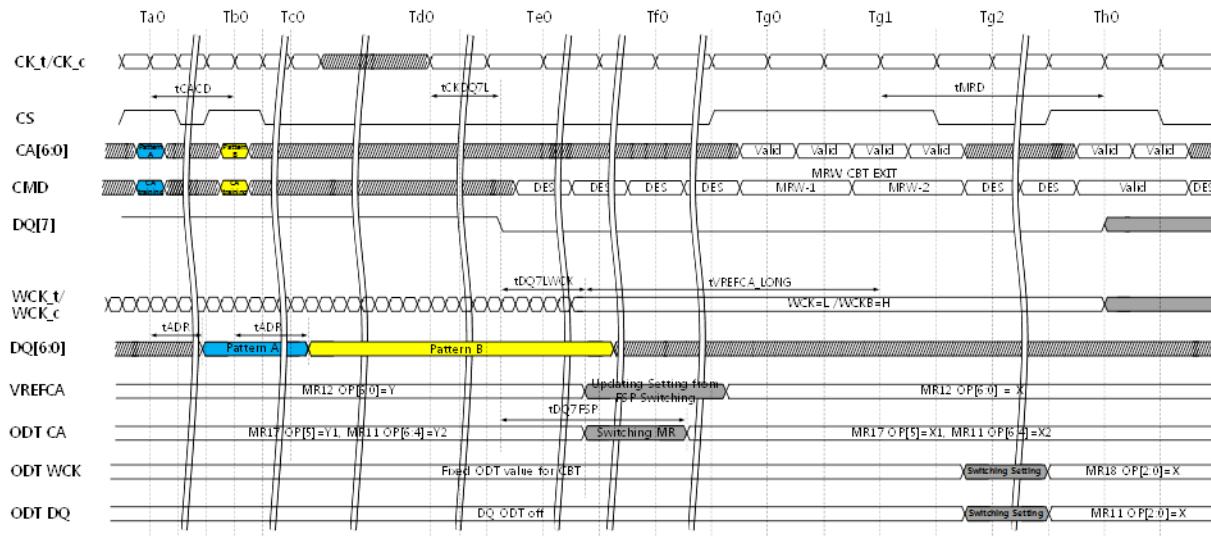
NOTE 4 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate(i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled then termination will not enable in CA Bus Training mode.

NOTE 5 WCK/DQ ODT states are set one fixed ODT state during CBT operation.

NOTE 6 Set fixed WCK frequency during CBT operation regardless of CK:WCK ratio.

Figure 26 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Fixed WCK Frequency)

4.2.2.1 Command Bus Training Mode1 (Cont'd)



NOTE 1 CK must meet tCDKQ7L before DQ[7] is driven low.

NOTE 2 Keep valid state of DQ[7] and WCK until CBT exit is finished by MRW.

NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).

Example: If the SDRAM was using FSP-OP [1] for training, then it will switch to FS-OP[0] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.

NOTE 4 Training values are not retained by the SDRAM , and must be written to the FSP-OP register set before returning to the operation at the trained frequency, Example: VREFCA will return to the value programmed in the original set point.

Figure 27 — Exiting Command Bus Training Mode

4.2.2.1 Command Bus Training Mode1 (Cont'd)

Table 24 — Command Bus Training Mode1 AC Timing Table

4.2.2.2 Command Bus Training Mode2

The LPDDR5 SDRAM uses Frequency Set Points to enable multiple operating settings for the die. The LPDDR5 SDRAM is initiated to FSP-OP[0] at power-up, which has the default settings to operate in unterminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR16 OP[1:0] for FSP-WR (Frequency Set Point Write Enable), setting all other mode register bits for FSP-OP (Frequency Set Point Operation Mode) to make the desired settings for high-frequency or mid-frequency operation, and setting MR16 OP[5:4] for Command Bus Training Mode selection.

Prior to entering Command Bus Training, the LPDDR5 SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when DQ[7] is driven HIGH, the LPDDR5 SDRAM will automatically switch to the alternate FSP register set FSP-OP[y] or FSP-OP[z] according to MR16 OP[5:4] and use the alternate register settings during training (See Figure 28, Note 6 for more information on FSP-OP register sets). Upon Command Bus Training exit when DQ[7] is driven LOW, the LPDDR5 SDRAM will automatically switch back to the original FSP register set FSP-OP[x], returning to the “known-good” state that was operating prior to training. The training values for VREF(CA) are not retained by the DRAM in FSP-OP[y] or FSP-OP[z] registers, and must be written to the registers after training exit.

LPDDR5 SDRAM can select the Command Bus Training CA phase by MR16 OP[7] setting. If MR16 OP[7] is LOW, DQ outputs CA pattern latched by CK rising edge. If MR16 OP[7] is HIGH, DQ outputs CA pattern latched by CK falling edge.

- 1) Set MR13 OP[6]=1 for Command Bus Training Mode2.
- 2) To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR16 OP[5:4] for the CBT mode selection and drive LOW to DQ[7], DMI[0], WCK_t and drive HIGH to WCK_c. WCK_t, WCK_c are input pins for capturing DQ[7], DMI[0] levels by its toggling. WCK ODT value is fixed regardless of MR18 setting. WCK_t and WCK_c have to toggle tWCK2DQ7H before DQ[7] goes HIGH. DQ ODT state is off during CBT mode.

DQ[7] is driven HIGH and when LPDDR5 SDRAM samples HIGH level of DQ[7] by WCK, the LPDDR5 SDRAM switches from FSP-OP[x] to FSP-OP[y] or FSP-OP[z] completing the entry into Command Bus Training mode. DQ[6:0] become input pins for setting VREF(CA) level during tDStrain + tDHtrain period.

DQ[6:0] become output pins to feedback its capturing value via command address bus by CS HIGH until the LOW level of DMI[0] is sampled by WCK.

DMI[0] is used as a strobe pin for VREF(CA) setting update via DQ[6:0] and also used as a DQ[6:0] output-mode-off switch. When the HIGH level of DMI[0] is sampled by WCK, LPDDR5 SDRAM samples DQ[6:0] levels by the internal DMI[0] rising edge and updates VREF(CA) setting. When the LOW level of DMI[0] is sampled by WCK, DQ[6:0] output mode is turned-off and changes to input mode. Until Completing to latch specific patterns driven by LPDDR5 SDRAM DQ[6:0], DMI[0] should be maintained “HIGH”.

- 3) After tDQ72DQ, LPDDR5 SDRAM can accept to change its VREF(CA) value using input signals of DQ[6:0] and the internal DMI[0] signal which LPDDR5 SDRAM samples DMI[0] by WCK from existing value that is setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQs is shown in Table 25. At least one VREF(CA) setting is required before proceed to next training steps.
- 4) The new VREF(CA) value must “settle” for time tVREF_LONG before attempting to latch CA information.
- 5) To verify that the receiver has the correct VREF(CA) setting and to further train the CA eye relative to clock(CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.

4.2.2.2 Command Bus Training Mode2 (Cont'd)

- 6) To exit Command Bus Training mode, drive DQ[7] LOW and after time tDQ7LWCK + tVREFCA_LONG issue the MRW command to set MR16 OP[5:4] = 00B. After time tMRD the LPDDR5 SDRAM is ready for normal operation. After training exit, the LPDDR5 SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may be entered from IDLE or Self Refresh states. When entering CBT, the SDRAM must not be in a Power Down state or Deep Sleep Mode. Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

Table 25 — Mapping of MR12 OP Code and DQ Numbers

Mapping							
MR12 OP code	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

Table 26 — Mapping of CA Input pin and DQ Output pin

Mapping							
CA Number	CA6	CA5	CA4	CA3	CA2	CA1	CA0
DQ Number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

Training Sequence for single-rank systems

Note that an example shown here is assuming an initial low-frequency, untermination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency; the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition: Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point "Y" (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- 5) Drive DQ[7] HIGH, and then change CK frequency to the high frequency operating point.
- 6) Perform Command Bus Training (VREF(CA), CS and CA).
- 7) Exit training by driving DQ[7] LOW, change CK frequency to the low frequency operating point prior to driving DQ[7] Low, and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 8) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained and other training or normal operation can be executed.

4.2.2.2 Command Bus Training Mode2 (Cont'd)

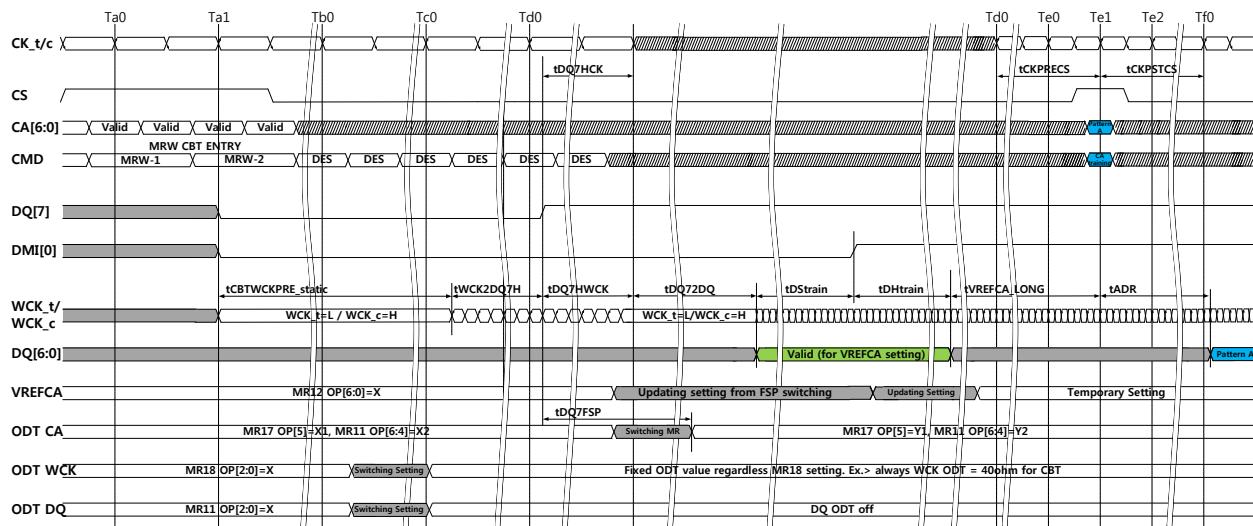
Training Sequence for multi-rank systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency; the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point "Y" (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
- 5) Drive DQ[7] HIGH on the terminating rank (or all ranks), and then change CK frequency to the high frequency operating point.
- 6) Perform Command Bus Training on the terminating rank (VREF(CA), CS and CA).
- 7) Exit training by driving DQ[7] LOW on the terminating rank, change CK frequency to the low frequency operating point prior to driving DQ[7] Low, and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 8) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to enter training mode on the non-terminating rank (but, keep DQ[7] LOW).
- 10) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operating point.
- 11) Drive DQ[7] HIGH on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y].
- 12) Perform Command Bus Training on the non-terminating rank (VREF(CA), CS and CA).
- 13) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] to turn off termination.
- 14) Exit training by driving DQ[7] LOW on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 15) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 16) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained for both ranks and other training or normal operation can be executed.

4.2.2.2 Command Bus Training Mode2 (Cont'd)

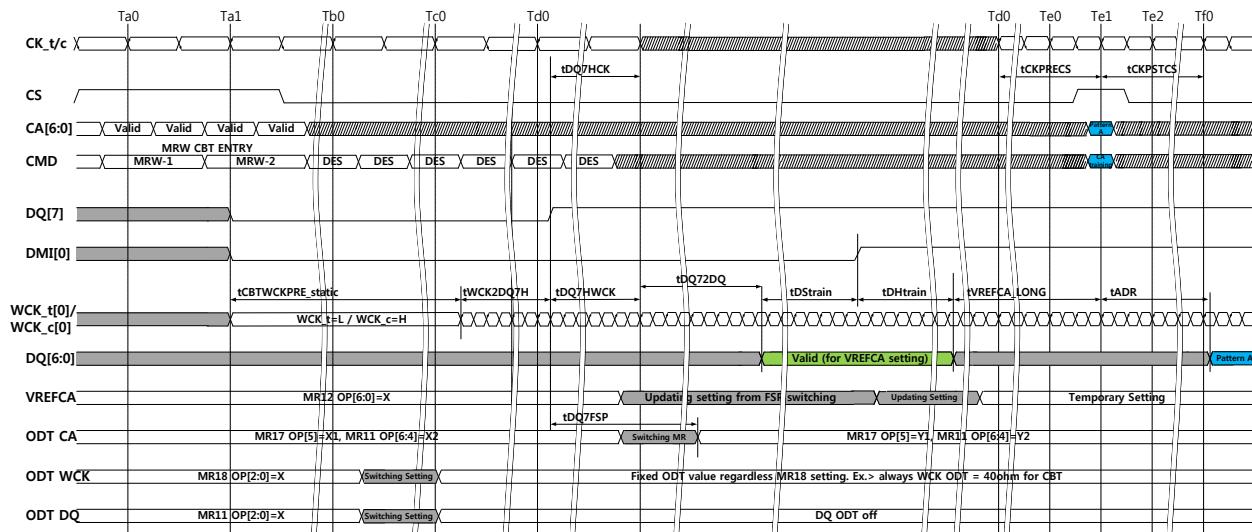
The basic timing diagrams of Command Bus Training Mode2 are shown in following figures.



- NOTE 1 After tDQ7HCK, clock can be stopped or frequency changed any time.
- NOTE 2 The input clock condition should be satisfied tCKPRECS.
- NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.
- NOTE 4 The value of the DQ[6:0] signal level is sampled by the DMI[0] rising edge. The DRAM updates its VREFCA setting of MR12 temporary, after time tVREFCA_long.
- NOTE 5 tVREFCA_long may be reduced to tVREFCA_short.
- NOTE 6 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate(i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/LW/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled then termination will not enable in CA Bus Training mode.
- NOTE 7 WCK/DQ ODT states are set one fixed ODT state during CBT operation.
- NOTE 8 During tDQ72DQ, WCK can be stop and changed frequency after FSP change.

Figure 28 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (WCK Frequency change)

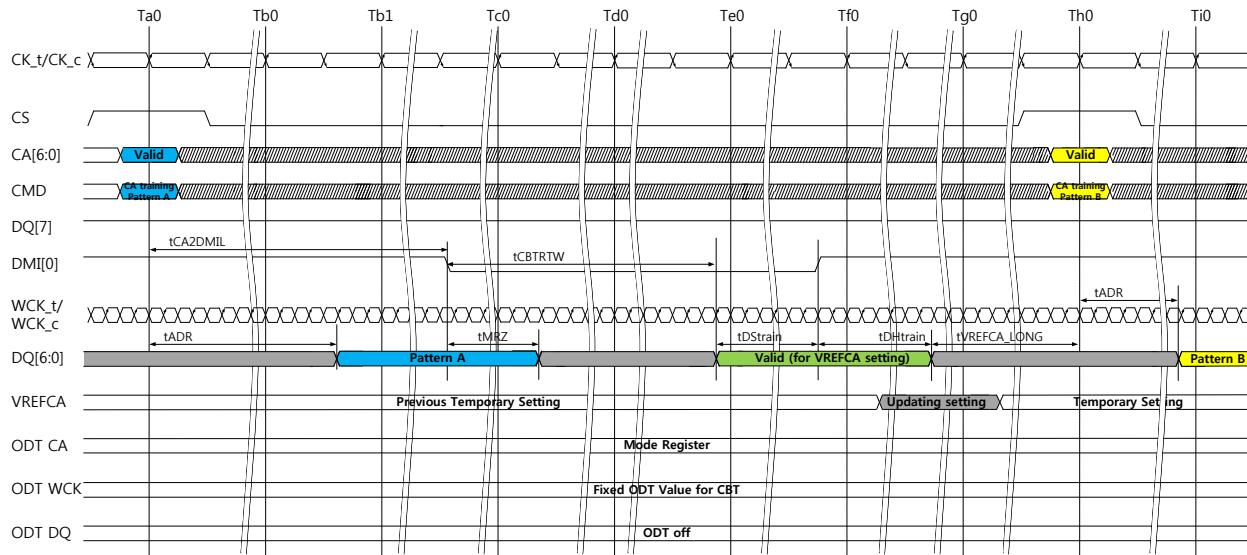
4.2.2.2 Command Bus Training Mode2 (Cont'd)



- NOTE 1 After tDQ7HCK, clock can be stopped or frequency changed any time.
 NOTE 2 The input clock condition should be satisfied tCKPRECS.
 NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.
 NOTE 4 The value of the DQ[6:0] signal level is sampled by the DMI[0] rising edge. The DRAM updates its VREFCA setting of MR12 temporary, after time tVREFCA_long.
 NOTE 5 tVREFCA_long may be reduced to tVREFCA_short.
 NOTE 6 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate(i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled then termination will not enable in CA Bus Training mode.
 NOTE 7 WCK/DQ ODT states are set one fixed ODT state during CBT operation.
 NOTE 8 Set fixed WCK frequency during CBT operation regardless of CK:WCK ratio

Figure 29 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Fixed WCK Frequency)

4.2.2.2 Command Bus Training Mode2 (Cont'd)



NOTE 1 The value of the DQ[6:0] signal level is sampled by DMI[0] rising edge. The DRAM updates its VREFCA setting of MR12 temporary, after time tVREFCA_long.

NOTE 2 To change read mode to write mode for DQ pins, DMI[0] has to be driven LOW.

NOTE 3 tVREFCA_long may be reduced to tVREFCA_short.

Figure 30 — CA pattern Input/Output to Vref setting Input

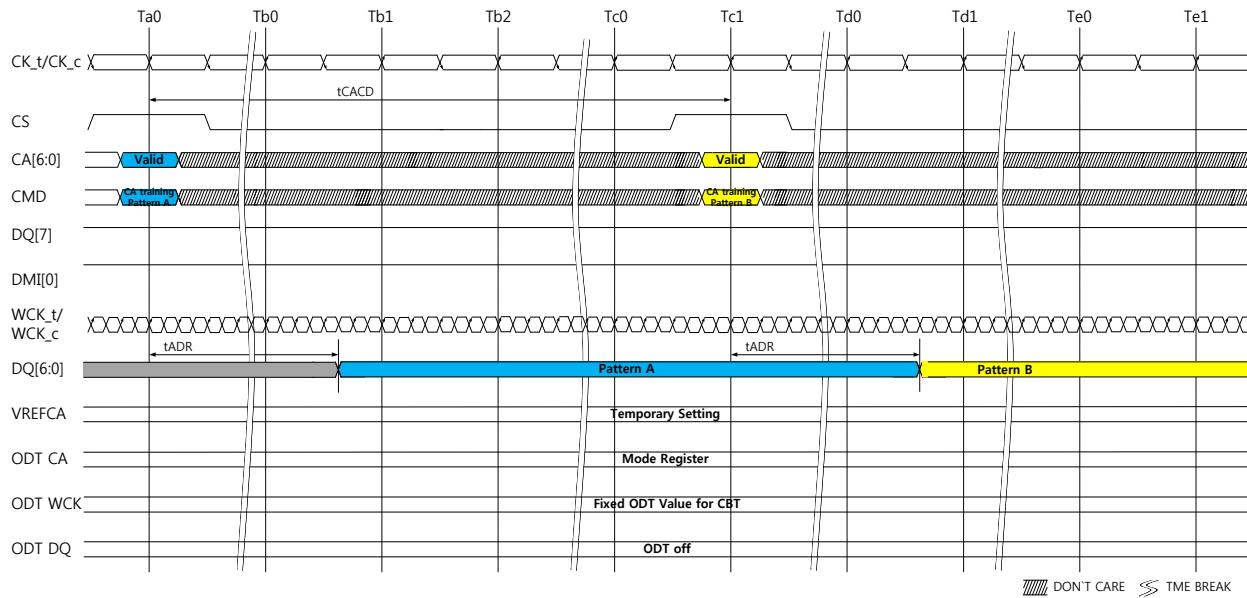
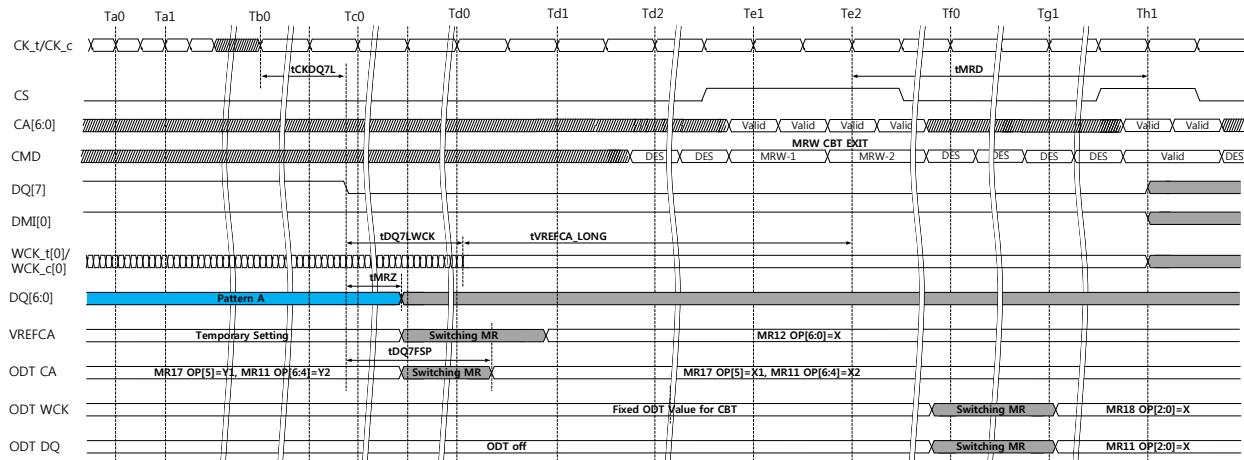


Figure 31 — Consecutive CA training pattern Input/Output

4.2.2.2 Command Bus Training Mode2 (Cont'd)



NOTE 1 CK must meet tCDKQ7L before DQ[7] is driven low.

NOTE 2 Keep valid state of DQ[7], DMI[0], and WCK until CBT exit is finished by MRW.

NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).

Example: If the SDRAM was using FSP-OP [1] for training, then it will switch to FS-OP[0] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.

NOTE 4 Training values are not retained by the SDRAM , and must be written to the FSP-OP register set before returning to the operation at the trained frequency

Example: VREFCA will return to the value programmed in the original set point.

Figure 32 — Exiting Command Bus Training Mode

4.2.2.2 Command Bus Training Mode2 (Cont'd)

Table 27 — Command Bus Training Mode2 AC Timing Table

Parameter	Symbol	Min/ Max	Data Rate												Unit	Note
			533	1066	1600	2133	2710	3200	3733	4266	4800	5420	6000	6400		
Command Bus Training Timing																
Static WCK period (CBT entry to WCK toggling start)	tCBTWCKPRE_static	Min.	Max(20ns, 2nCK)										ns			
Set-up margin between DQ7 and WCK	tWCK2DQ7H	Min.	Max(5ns, 12nWCK)										ns			
Hold margin between DQ7 and WCK	tDQ7HWCK	Min.	Max(5ns, 12nWCK)										ns			
Clock and Command Valid after DQ7 High	tDQ7HCK	Min.	Max(5ns, 3nCK)										ns			
ODT CA change latency after DQ7 High	tDQ7FSP	Max..	20										ns			
DQ7 High to valid DQ[6:0] input for VREFCA setting	tDQ72DQ	Min.	250										ns			
Valid Clock Requirement before CS High	tCKPRECS	Min.	2tCK + tXP (tXP = Max(7.5ns, 3nCK))										ns			
Valid Clock Requirement after CS High	tCKPSTCS	Min.	Max(7.5ns, 3nCK)										ns			
VREF Step Time – Long	tVREFCA_long	Max.	250										ns	2		
VREF Step Time – Short	tVREFCA_short	Max.	200										ns	3		
Data Setup for Vref Training Mode	tDStrain	Min.	Max(5ns, 12nWCK)										ns			
Data Hold for Vref Training Mode	tDHtrain	Min.	Max(5ns, 12nWCK)										ns			
Asynchronous Data Read	tADR	Max.	20										ns			
CBT Command input to DMI Low	tCA2DMIL	Min.	30										ns			
DMI Low to DQ driver off	tMRZ	Min.	1.5										ns			
DMI Low to Valid DQ input for VREFCA setting	tCBTRTW	Min.	Max(20ns, 12nWCK)										ns			
CA Bus Training Command to CA Bus Training Command delay	tCACD	Min.	RU(tADR/tCK)										tCK			
CK and Command Valid before DQ7 Low	tCKDQ7L	Min.	Max(5ns, 3nCK)										ns			
DQ7 Low to static WCK	tDQ7LWCK	Min.	Max(5ns, 12nWCK)										ns			

4.2.3 CA VREF Training

TBD

4.2.4 DQ VREF Training

TBD

4.2.5 WCK2CK Leveling

4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4)

To adjust CK-to-WCK relationship and guarantee WCK2CK-Sync operation, the LPDDR5 SDRAM provides a WCK2CK Leveling feature to compensate CK-to-WCK timing skew affecting WCK2CK-Sync operation. The DRAM compares the phase of the rising edge of WCK and the rising edge of CK, then asynchronously feeds back to the memory controller for the WCK2CK phase detection result. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync operation will be performed with the optimized margin.

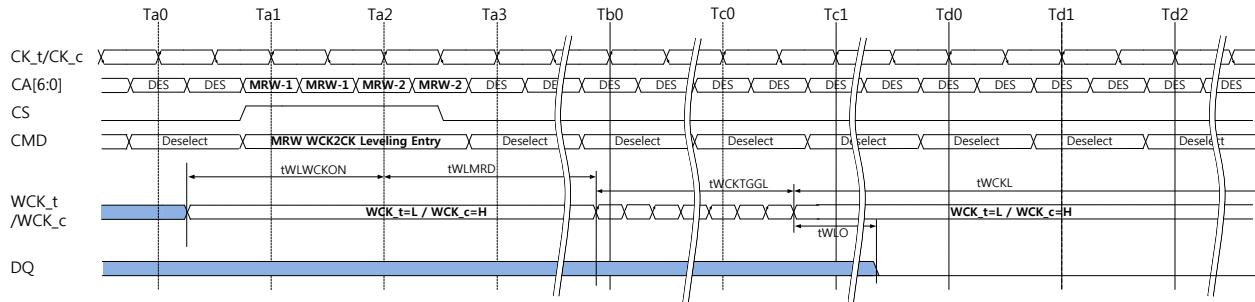
The memory controller references WCK2CK-Sync feedback to adjust CK-to-WCK relationship for each WCK_t/WCK_c signal pair. All data bits (DQ[7:0] for WCK_t[0]/WCK_c[0], and DQ[15:8] for WCK_t[1]/WCK_c[1]) carry the training feedback to the controller.

The LPDDR5 SDRAM enters into WCK2CK Leveling mode when mode register MR18-OP[6] is set HIGH. When WCK2CK Leveling mode is entered, the state of the DQ pins is undefined. During WCK2CK Leveling mode, only DESELECT commands are allowed, or MRW command to exit the WCK2CK Leveling operation. Upon completion of the WCK2CK Leveling, the DRAM exits from WCK2CK Leveling mode when MR18-OP[6] is reset LOW.

WCK2CK Leveling should be performed before write training.

WCK2CK Leveling examples are shown in Figure 33 and Figure 34, and the specific descriptions for the figures will be provided in the following section.

4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters

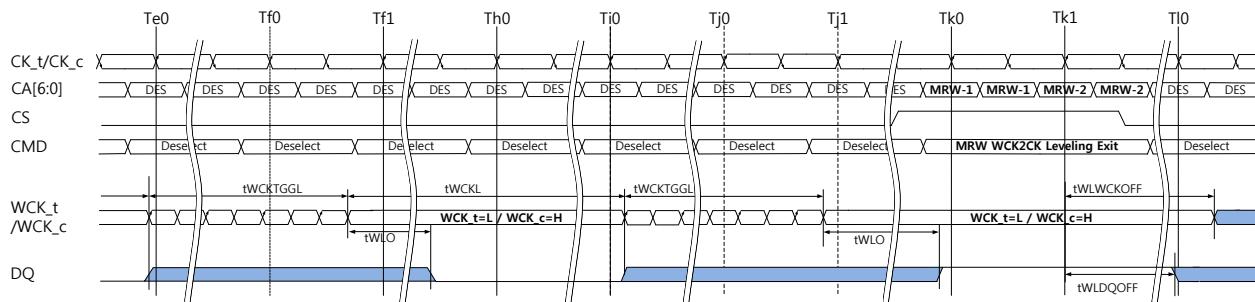


NOTE 1 WCK must be driven tWLWCKON earlier than WCK2CK leveling entry.

NOTE 2 WCK must toggle exactly 8 cycles (tWCKTGGL=8tWCK).

NOTE 3 WCK2CK phase detection result on DQ bus is low because WCK phase is earlier than CK phase.

Figure 33 — WCK2CK Leveling Entry



NOTE 1 DQ output transit from low to high when WCK phase starts to be later than CK phase.

NOTE 2 Controller is allowed to change WCK phase only when it is driving WCK_t=L/WCK_c=H.

Figure 34 — WCK2CK Leveling Exit

1. Start to drive WCK_t LOW and WCK_c High.
2. Enter into WCK2CK Leveling mode by setting MR18-OP[6]=1. In WCK2CK leveling mode, the WCK to CK frequency ratio must be 2:1, because the frequency of WCK preamble is 2 times of CK regardless of WCK2CK mode (4:1 or 2:1).
3. Wait for a time tWLMRD before providing the first WCK signal toggle input. The delay time tWLMRD(MAX) is controller dependent.
4. Toggle WCK signal 8 cycles for WCK2CK phase detection. DRAM may or may not capture the first rising edge of WCK_t due to an unstable first rising edge. Hence providing exactly 8 pulses of WCK signal input is required in every WCK input signal during WCK2CK training mode.
DRAM provides asynchronous feedback of last captured WCK2CK phase information during WCK toggles, on all the DQ bits after time tWLO. DQ output is low if WCK phase is earlier than CK phase and high if WCK phase is later than CK phase. The controller must sample the phase relation result on DQ after satisfying tWLO.
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the WCK_t and WCK_c delay setting. The controller can adjust the WCK delay setting only when it drives WCK_t LOW and WCK_c HIGH to prevent any glitches in WCK signal. WCK search range from controller is defined as tWCK2CK_leveling ac parameter. Refer to the tWCK2CK_leveling value in Table 28.
6. Repeat step 4 through step 5 until the proper WCK_t/WCK_c delay is established.
7. Exit from WCK2CK Leveling mode by setting MR18-OP[6]=0.

4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters (Cont'd)

Table 28 — WCK2CK Leveling Timing Parameters

Parameter	Symbol	Min/ Max	Value	Units	Notes	
WCK_t/WCK_c drive start to WCK2CK leveling mode entry	tWLWCKON	Min	2	tCK		
First WCK_t/WCK_c edge After WCK2CK leveling mode is programmed	tWLMRD	Min	Max(14ns,5tCK)	ns		
Write Leveling output delay	tWLO	Min	0	ns		
		Max	Max(2tCK,20ns)	ns		
WCK off delay after write leveling mode exit	tWLWCKOFF	Max	Max(14ns,5tCK)	ns		
DQ off delay after write leveling mode exit	tWLDQOFF	Max	Max(14ns,5tCK)	ns		
WCK cycle per WCK2CK phase detection	tWCKTGGL	Min	7.5	tWCK	1	
		Max	7.5	tWCK	1	
WCK to CK phase offset	tWCK2CK	Min	Max(-0.5*tWCK,-TBDps)	ps	2	
			Max(-0.25*tWCK,TBDps)		3	
		Max	Min(0.5*tWCK,TBDps)	ps	2	
			Min(0.25*tWCK,TBDps)		3	
WCK2CK leveling phase search range	tWCK2CK_Leveling	Min	Max(-0.5*tWCK,-TBDps)	ps	4	
		Max	Min(0.5*tWCK,TBDps)	ps	4	
NOTE 1 8 WCK pulses are required per WCK2CK phase detection.						
NOTE 2 Applied when CKR is 4:1 mode(MR18 OP[7]=0).						
NOTE 3 Applied when CKR is 2:1 mode(MR18 OP[7]=1).						
NOTE 4 SDRAM will return correct tWCK2CK phase relation information in WCK2CK leveling mode within the range specified. However, the maximum WCK to CK phase shift allowed for DRAM normal operation may be limited by tWCK2CK.						

4.2.6 Duty Cycle Adjuster (DCA)

LPDDR5 SDRAM supports a mode-register-adjustable WCK DCA to allow the memory controller to adjust the DRAM internal WCK clock tree duty cycle to compensate for systemic duty cycle error. A separate DCA is provided for each byte, (DCAL for the Lower Byte adjustment and DCAU for the Upper Byte adjustment.).

The WCK DCA is located before the WCK divider or equivalent place. The WCK DCA will affect WCK duty cycle during the following operations:

- Read
- Read32
- Write
- Write32
- Masked Write
- Mode Register Read
- Read FIFO
- Write FIFO
- Read DQ Calibration
- Duty Cycle Monitor

The controller can adjust the duty cycle through the MR30 OP[3:0] for DCAL and MR30 OP[7:4] for DCAU setting and can determine the optimal Mode Register setting for DCA in multiple different ways.

This function adjusts the SDRAM internal WCK duty cycle (Static).

4.2.6.1 Duty Cycle Adjuster Range

The step range between the step 0 to 7 (-7) is as follows. The difference of actual value between step N and step N+1 cannot be defined, since the variation of duty cycle by changing DCA code is not linear.

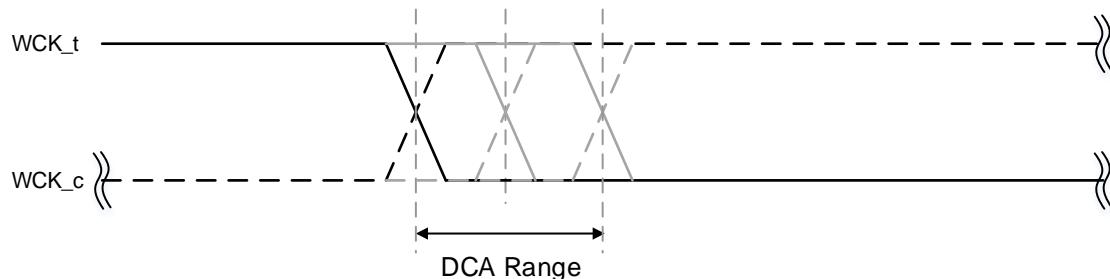
Table 29 — DCA Range

Parameter	Min/Avg./Max	Value	Unit	Notes
Duty Cycle Adjuster Range	Min	TBD	ps	1
	Max	TBD		

NOTE 1 These values are guaranteed by design.

Table 30 — Duty Cycle Adjuster Range

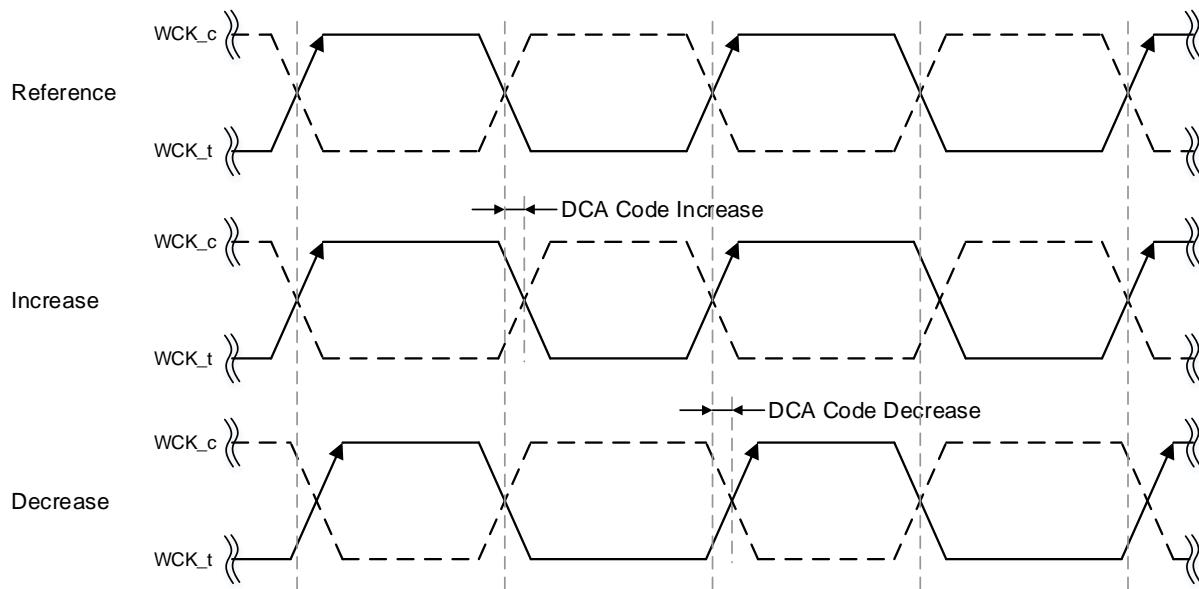
Step 0 Step 3 Step 7



4.2.6.2 Relationship between WCK waveform and DCA Code Change

The basic operation of the DAC code change is as follows.

After DCA code change, it is recommended to re-execute WCK2CK leveling.



NOTE 1 Refer to the write clock specification section, 15.2, for the definition of tWCKH(avg) and tWCK(avg)

Figure 35 — Relationship between WCK waveform and DCA Code Change (Example)

4.2.6.3 The relationship between DCA Code Change and DQ output/RDQS timing

The WCK DCA code change effect to DQ Output and RDQS are as follows. The rising edge of WCK_t affects to the rising edge of RDQS_t and the even data output. The falling edge of WCK_t affects to the falling edge of RDQS_t and the odd data output. The complimentary signal (WCK_c and RDQS_c) is the same as the true signal.

The relationship between the DCA code change and delay time variation (Delay_R/F) only can define in a qualitative manner.

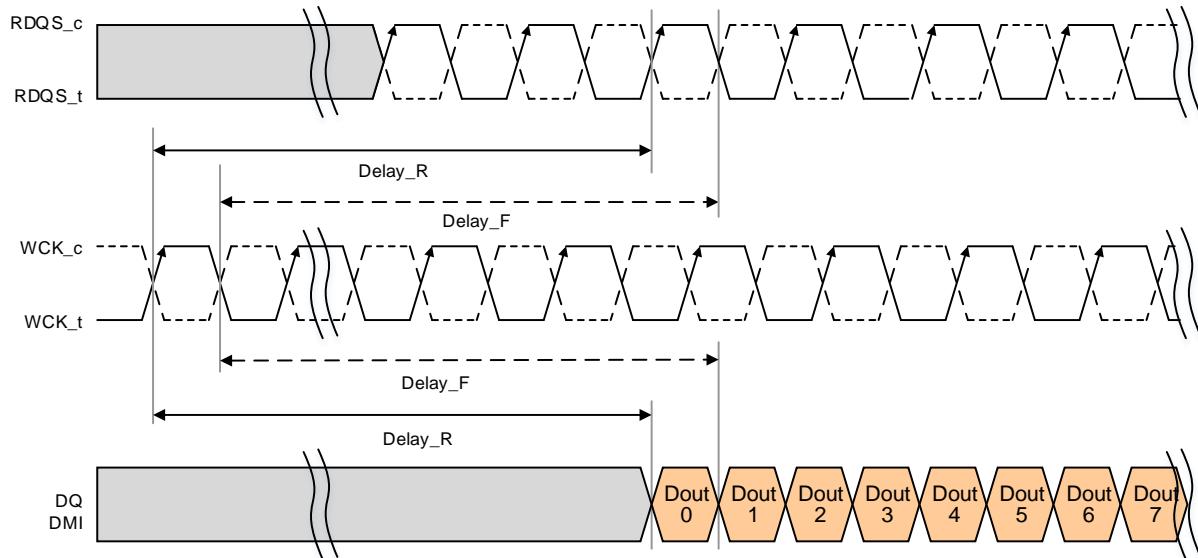


Figure 36 — Relationship between WCK waveform and DQS_t/c and DQ output (Example)

4.2.7 Duty Cycle Monitor (DCM)

4.2.7.1 DCM Functional Description

LPDDR5 SDRAM devices feature a duty cycle monitor (DCM) to allow the memory controller to monitor WCK duty cycle distortion in the DRAM internal WCK clock tree. Both lower and upper bytes perform the DCM function simultaneously when DCM is enabled. Two separate duty cycle results are provided for each byte: DCML0 and DCML1 for the Lower Byte and DCMU0 and DCMU1 for the Upper Byte.

DCM operation is initiated by writing MR26 OP[0] = 1_B. Setting MR26 OP[0] = 0_B terminates DCM operation. Prior to initiating DCM operation, WCK2CK SYNC – Fast Sync operation shall be performed in accordance with 7.2.1. Continuous toggling WCK input is required while DCM operation is enabled until TBD after DCM operation is halted by writing MR26 OP[0] = 0_B.

DCM results may be inaccurate if DCM circuit hysteresis is present. To increase the accuracy of this function, the DCM supports flipping the input by setting MR26 OP[1] to the opposite state and then repeating the measurement.

MRW[DCM Flip] and MRW[DCM Stop] will capture the DCM results. The DCM result is determined by the state of DCM Flip bit (MR26 OP[1]).

- DCM Flip = 0: DCML0 and DCMU0 will be used
- DCM Flip = 1: DCML1 and DCMU1 will be used

The DCM circuit monitors both read/write WCK clock path. DCM requires higher than 800MHz WCK.

4.2.7.2 DCM Sequence

DCM training is expected to be done after CBT and WCK2CK Leveling to ensure that MRW and MRR operation can be reliably performed. Below is a DCM sequence that examines the duty cycle of the WCK path:

1. Update the FSP settings.
2. Issue a CAS command with WS_FS=1 to toggle WCK at full-rate before DCM starts.
3. Issue MRW-1 and MRW-2 to start DCM.
4. Wait tDCMM for the DCM to complete duty cycle measurement.
5. Issue MRW-1 and MRW-2 to switch MRx OP[1] to flip the inputs of DCM.
 - 5.1. Transitioning the flip bit from a logic low to a logic high will automatically:
 - 5.1.1. Capture the current DCM results
 - 5.1.2. Store the DCM results in MR26 OP[2]/MR26 OP[4]
 - 5.1.3. Reset and restart the DCM
 - 5.2. Transitioning the flip bit from a logic high to a logic low will automatically:
 - 5.2.1. Capture the current DCM results
 - 5.2.2. Store the DCM results in MR26 OP[3]/MR26 OP[5]
 - 5.2.3. Reset and restart the DCM
6. Wait tDCMM for the DCM to complete duty cycle measurement with the flipped inputs
7. Exit DCM by issuing MRW-1 and MRW-2 to the LPDDR5 SDRAM device.
 - 7.1. This automatically captures and stores the current DCM results in MR26 OP[2]/MR26 OP[4] when MR26 OP[1] is a logic low.
 - 7.2. This automatically captures and stores the current DCM results in MR26 OP[3]/MR26 OP[5] when MR26 OP[1] is a logic high.
8. MR26 OP[5:2] can be read out by issuing an MRR after Tf0 using normal MRR timing.

4.2.7.2 DCM Sequence (Cont'd)

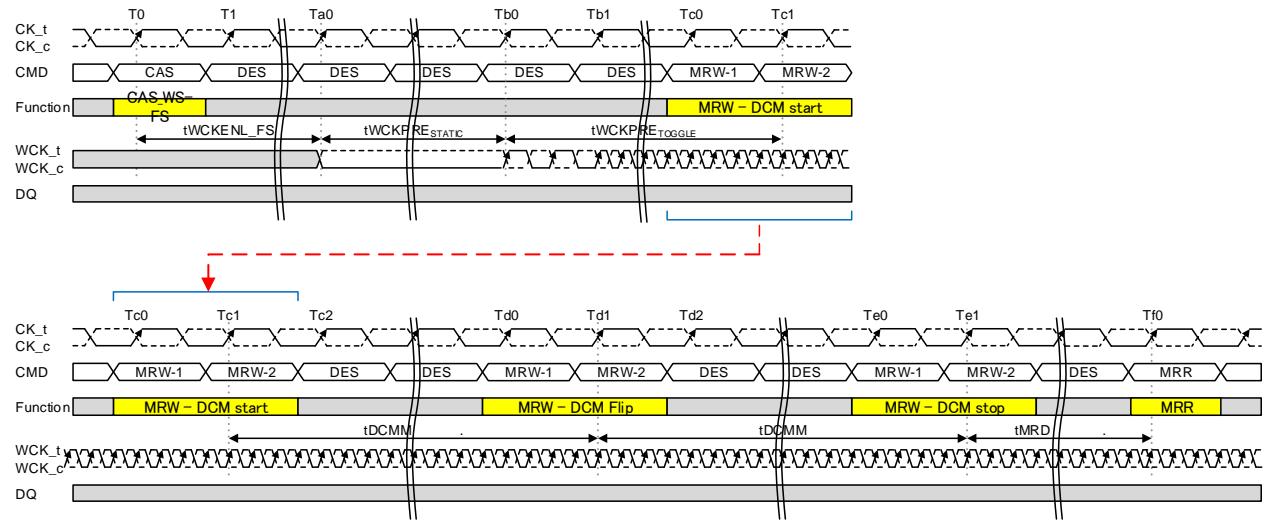


Figure 37 — DCM timing example

Table 31 — Duty cycle monitor timing

Parameter	Symbol	Min/ Max	WCK Frequency (MHz)										Unit	Note
			800	1067	1375	1600	1867	2134	2400	2750	3000	3200		
Duty Cycle Monitor Measurement time	tDCMM	MIN							2				μs	

4.2.8 READ DQ Calibration

The LPDDR5 SDRAM devices feature a READ DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. READ DQ Calibration is initiated by issuing a READ DQ CALIBRATION (RDC) command, cause the LPDDR5 SDRAM to drive the contents of MR33 followed by the contents of MR34 on each of DQ[15:0] and DMI[1:0]. The pattern can be either inverted or low-fixed on selected DQ pins according to user-defined invert masks or output data fix0 written to MR31 and MR32. The selection of either inverted or low-fixed is decided based on MR20.

4.2.8.1 READ DQ Calibration Training Procedure

The procedure for executing READ DQ Calibration is:

- Issue MRW commands to write MR33 (first eight bits), MR34 (second eight bits), MR20 (selection of either inverted or output fix0), MR31/32 (eight-bit invert mask or output data fix0 for byte0/1).
 - Optionally this step could be skipped to use the default patterns.
 - MR31 default = 55_H
 - MR32 default = 55_H
 - MR33 default = 5A_H
 - MR34 default = 3C_H
- RD DQ Calibration is initiated by issuing Read DQ Calibration (RDC) command while in a WCK2CK SYNC state.
 - Each time an RDC command is received by the LPDDR5 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR33 followed by the eight bits programmed in MR34 on all I/O pins. CAS command (WS_RD = 1) is not required as long as WCK2CK-sync state is kept.
 - When MR20 OP[7] = 0, the data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
 - When MR20 OP[7] = 1, the data pattern will be low-fixed for IO pins with a '1' programmed in the corresponding output data fix0 mode register bit (see Table 32 and Table 33). The DMI pattern will be low-fixed when MR20 OP[6] = 1.
 - Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
 - The RDC command can be issued every tCCD seamlessly, and tRTRRD delay is required between Array Read command and the RDC command as well the delay required between the RDC command and an array read.
 - The operands received with the CAS command must be driven LOW except WS_RD.
 - The function set by previous CAS operands is ignored. (DC0~3 and B3 are ignored.)
- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF without Power Down.
- In case of byte mode, MR31 is valid only for lower byte selected device, and MR32 is valid only for upper byte selected device.

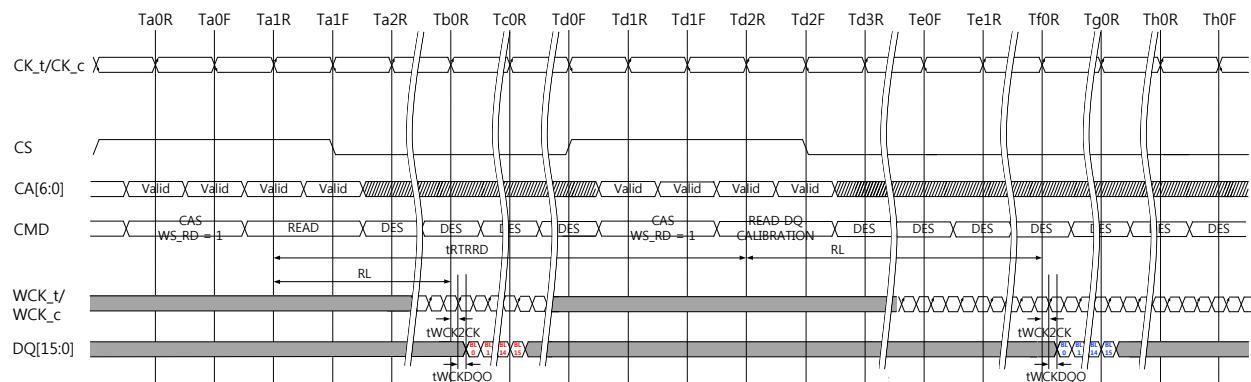
4.2.8.1 READ DQ Calibration Training Procedure (Cont'd)

Table 32 — Invert Mask or output data fix0 Assignments in X16 Mode

DQ Pin	Pattern selects MR20 OP[7]	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
MR31	0	DQ0 invert	DQ1 invert	DQ2 invert	DQ3 invert	DQ4 invert	DQ5 invert	DQ6 invert	DQ7 invert
	1	DQ0 Fix0	DQ1 Fix0	DQ2 Fix0	DQ3 Fix0	DQ4 Fix0	DQ5 Fix0	DQ6 Fix0	DQ7 Fix0
MR32	0	DQ8 invert	DQ9 invert	DQ10 invert	DQ11 invert	DQ12 invert	DQ13 invert	DQ14 invert	DQ15 invert
	1	DQ8 Fix0	DQ9 Fix0	DQ10 Fix0	DQ11 Fix0	DQ12 Fix0	DQ13 Fix0	DQ14 Fix0	DQ15 Fix0

Table 33 — Invert Mask or output data fix0 Assignments in X8 Mode

DQ Pin	Pattern select MR20 OP[7]	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
MR31	0	DQ0 invert	DQ1 invert	DQ2 invert	DQ3 invert	DQ4 invert	DQ5 invert	DQ6 invert	DQ7 invert
	1	DQ0 Fix0	DQ1 Fix0	DQ2 Fix0	DQ3 Fix0	DQ4 Fix0	DQ5 Fix0	DQ6 Fix0	DQ7 Fix0



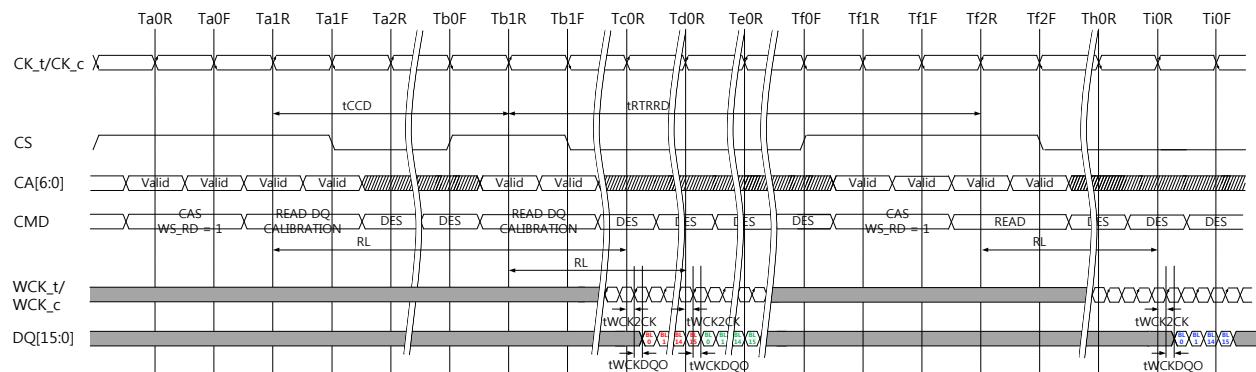
NOTES - 1. READ to READ DQ CALIBRATION operation is shown as an example of command to command timing.
Timing from READ to READ DQ CALIBRATION is tRTRRD.

DON'T CARE TIME BREAK

2. READ DQ CALIBRATION uses the same command to data timing relationship as READ command.
3. If WCK_t/WCK_c have been Hi-Z state prior to issuing READ DQ CALIBRATION command, WCK2CK Sync operation must be executed. READ DQ CALIBRATION uses the same timing relationship with the WCK2CK Sync operation as READ command.
4. BL=16.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 38 — Read DQ Calibration Timing: Read to Read DQ Calibration

4.2.8.1 READ DQ Calibration Training Procedure (Cont'd)



NOTES - 1. READ DQ CALIBRATION to READ DQ CALIBRATION operation is shown as an example of command to command timing. Seamless READ DQ CALIBRATION commands may be executed by repeating the command every tCCD time.
 2. READ DQ CALIBRATION to READ operation is shown as an example of command to command timing.
 Timing from READ DQ CALIBRATION to READ is tRTRRD.
 3. READ DQ CALIBRATION uses the same command to data timing relationship as READ command.
 4. If WCK_t/WCK_c have been Hi-Z state prior to issuing READ DQ CALIBRATION command, WCK2CK Sync operation must be executed. READ DQ CALIBRATION uses the same timing relationship with the WCK2CK Sync operation as READ command.
 5. BL=16.
 6. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 39 — Read DQ Calibration Timing: Read DQ Calibration to Read DQ Calibration

4.2.8.2 READ DQ Calibration Example

An example of READ DQ Calibration Training output is shown in Table 34 and Table 35. This shows the 16-bit data pattern that will be driven on each DQ when one READ DQ CALIBRATION command is executed. This output assumes the following mode register values are used.

- MR31 default = 55_H
- MR32 default = 55_H
- MR33 default = 1C_H
- MR34 default = 59_H

Table 34 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DQ

PIN	MR20 OP[7]	DQ Invert	DQ output Data fix0	Bit Sequence															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQx	0	Yes	-	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
		No	-	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
	1	-	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		-	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

4.2.8.2 READ DQ Calibration Example (Cont'd)

Table 35 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DMI

PIN	MR 20 OP [6]	DMI output Data fix0	Bit Sequence →															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMI	0	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
	1	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE 1 The patterns contained in MR33 and MR34 are transmitted on DQ[15:0] and DMI[1:0] when READ DQ Calibration is initiated by a READ DQ CALIBRATION command. The pattern transmitted serially on each data lane, organized that the low-order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111(→).

NOTE 2 MR31 and MR32 may be used to invert the MR33/ MR34 data pattern on the DQ pins. See MR31 (Table 106) and MR32 (Table 109) for more information. There is no inversion function for DMI[1:0] pin data streams.

NOTE 3 No Data Bus Inversion (DBI) function is enacted during READ DQ CALIBRATION, even if DBI is enabled.

4.2.8.3 READ DQ Calibration after Power Down Exit

Following the power down state, an additional time, tMRRI, is required prior to issuing the READ DQ CALIBRATION command. This additional time (equivalent to tRCD) is required in order to be able to maximize power down current savings by allowing more power-up time for the Read DQ data in MR33 and MR34 data path after exit from standby, power down mode.

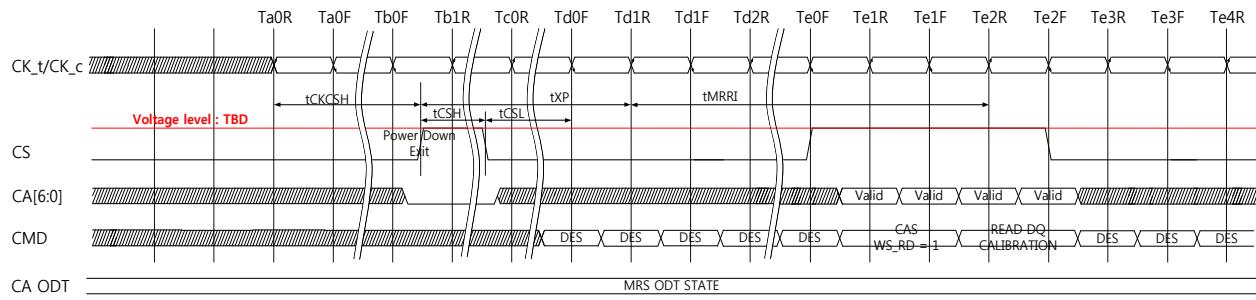


Figure 40 — READ DQ CALIBRATION following Power Down State

4.2.9 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad, and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

The LPDDR5 SDRAM provides a Command-based FIFO Write/Read training operation using user specific pattern. DMI will be treated the same as DQs. It means that the Write Data send to FIFO for DMI by WFF command and these data can be read-out from FIFO for DMI by RFF command.

4.2.9.1 Training procedure

To perform Write Training, the controller is required to be issued the CAS command with WS_WR=1 followed immediately by the Write FIFO command to write data into the FIFO. Timing for the CAS and the Write FIFO command are identical to the CAS and the Write command. Up to 8 consecutive Write FIFO commands with user defined patterns may be issued to the SDRAM to store up to 128 values (BL16 x 8) per pin that can be read back via the Read FIFO command.

The burst length of the Write FIFO and the Read FIFO command is limited to BL16 regardless Bank architecture: BG, 16B and 8B mode.

The Write/Read FIFO Pointer operation is described later in this section.

After writing data to the SDRAM with the Write FIFO command, the data can be read back with the Read FIFO command and results compared with “expect” data to see if further training is needed. To read back the data, the controller is required to issue a CAS command with WS_RD=1 followed immediately by the Read FIFO command to read back data from FIFO. Timing for the CAS and the Read FIFO command are identical to the CAS and the Read command.

The Read FIFO operation is non-destructive to the data captured in the FIFO, so data may be read continuously until it is overwritten by the Write FIFO command. For example: If 8 Write FIFO commands are executed sequentially, then a series of Read FIFO commands will read valid data from FIFO[0], FIFO[1]....FIFO[7], and will then wrap back to FIFO[0] on the next Read FIFO. If fewer than 8 Write FIFO commands were executed, then unwritten registers will have un-defined (but valid) data when read back. For instance, if fewer than 8 Write FIFO commands are executed sequentially (example=3), then a series of Read FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], however the next (8-3) Read FIFO commands will return un-defined data for FIFO[3] through FIFO[7] before wrapping back to the valid data in FIFO[0].

4.2.9.1 Training Procedure (Cont'd)

During WCK-DQ Training, only the following commands are allowed, to prevent an overwrite of the Write and Read FIFO and to simplify this training procedure.

- Read FIFO
- Write FIFO
- DES
- NOP
- Refresh (All bank and Per bank)
- Mode Register Write for FSP-WR: MR16 OP[1:0], FSP-OP: MR16 OP[3:2] and VRCG: MR16 OP[6].

The Link-ECC function, Data Mask Inversion and Data Bus Inversion are required to be disabled before issuing the Write FIFO command.

WCK-DQ Training can be started at Idle, Bank active, during refresh or Self Refresh of the SDRAM. WCK-DQ Training can be ended when the FIFO pointer is the same value between Write and Read FIFO.

4.2.9.2 WCK-RDQS_t/Parity Training

When Link ECC is enabled, the RDQS_t pin will have two different functions:

- 1) During Read operations, RDQS_t will function as RDQS_t, and
- 2) During Write operations RDQS_t will function as Parity.

Hence the RDQS_t pin cannot be used as the data output pin during normal WCK-DQ Training procedure defined in 4.2.9.1.

To train the RDQS_t pin, the Read and Write FIFO commands are used with MRxx OP[y] is set to "1". With this bit set, a Write FIFO command will allow data to be written through the RDQS_t pin. The data written via the RDQS_t pin can then be read back via the DMI by a Read FIFO command.

To return to normal operation, MRxx OP[y] must be set to "0".

4.2.9.3 FIFO Pointer Reset and Synchronism

The Read and Write FIFO pointers are reset under the following conditions:

- Power-up initialization,
- RESET_n asserted,
- Power-down entry,
- Deep Sleep Mode entry, and
- Self Refresh Power-Down entry.

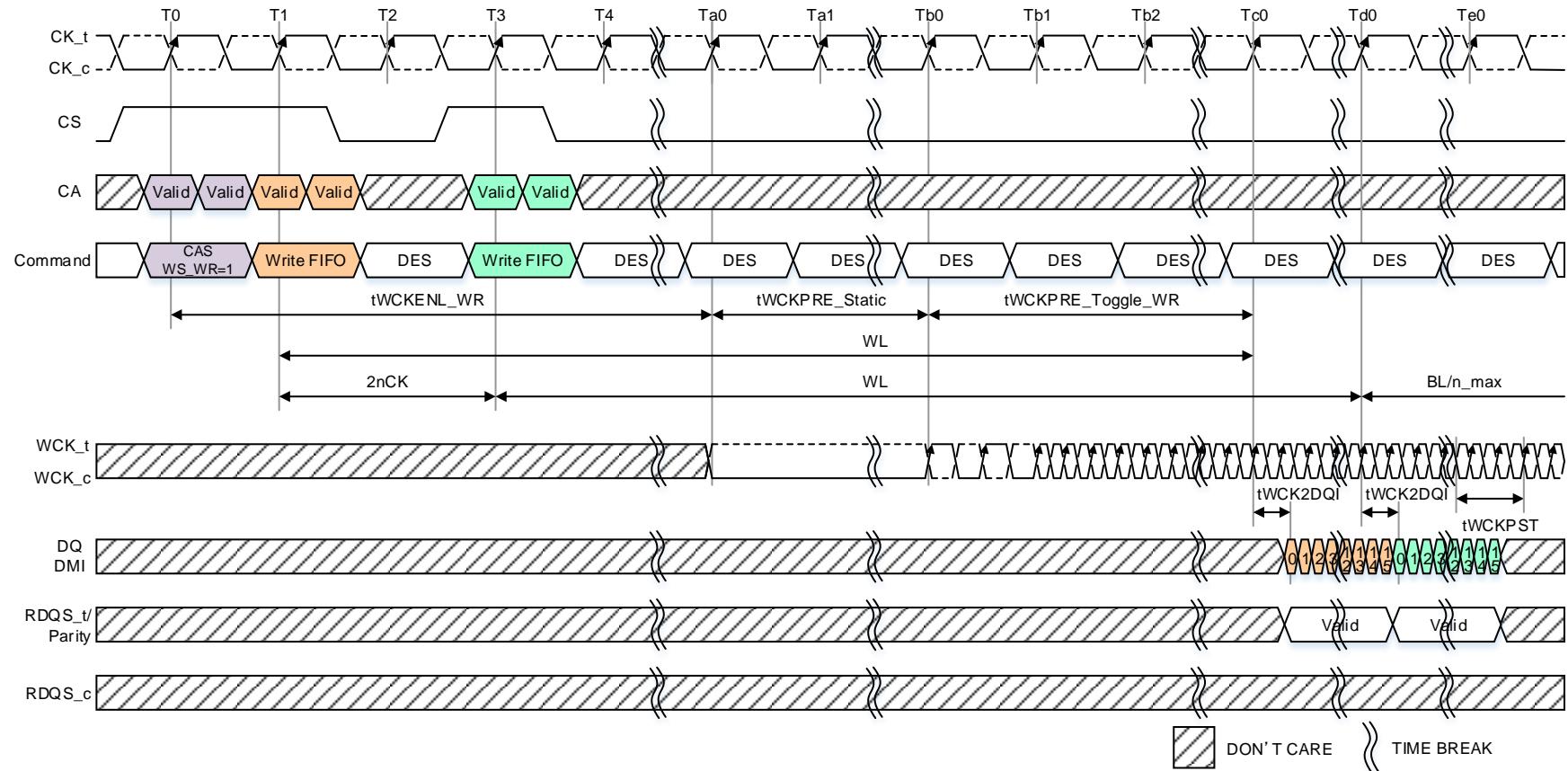
The Write FIFO command advances the Write-FIFO pointer, and the Read FIFO command advances the Read-FIFO pointer. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of WCK-DQ Training period:

$$b = a + (n \times c)$$

where:

- 'a' is the number of Write FIFO commands
- 'b' is the number of Read FIFO commands
- 'c' is the FIFO depth (=8 for LPDDR5)
- 'n' is a positive integer, ≥ 0

4.2.9.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

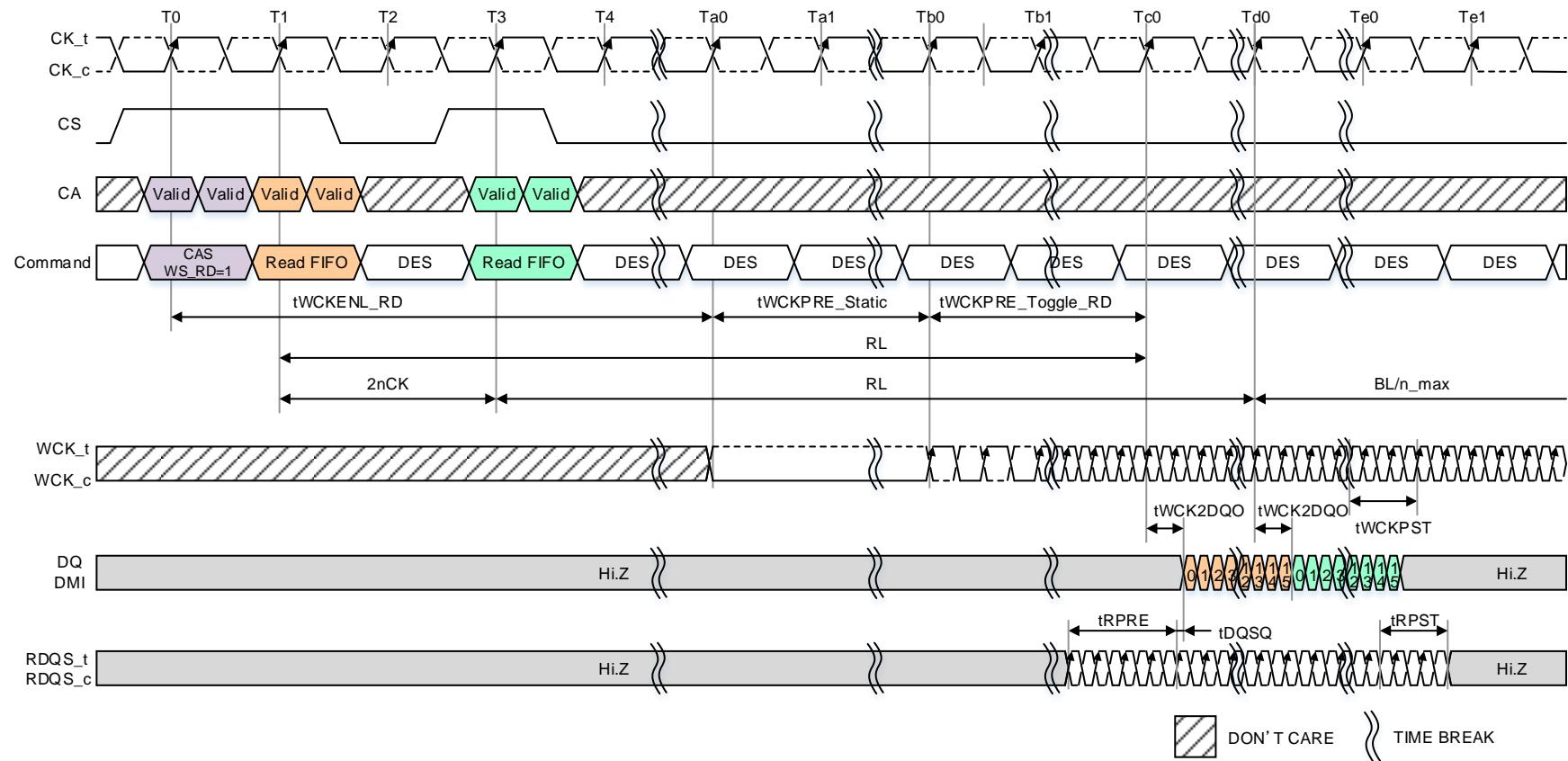
NOTE 2 The end of both WL and tWCKPRE_Toggle_WR are the same timing in this instance.

NOTE 3 The (8 + 1) Write FIFO command will overwrite the FIFO data from the first command. If fewer than 8 Write FIFO commands are executed, then the remaining FIFO locations will contain undefined data.

NOTE 4 CAS command is needed before a Write FIFO command when a WCK synchronization will expire.

Figure 41 — Consecutive Write FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1

4.2.9.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1 $tWCK2CK$ is 0ps in this instance.

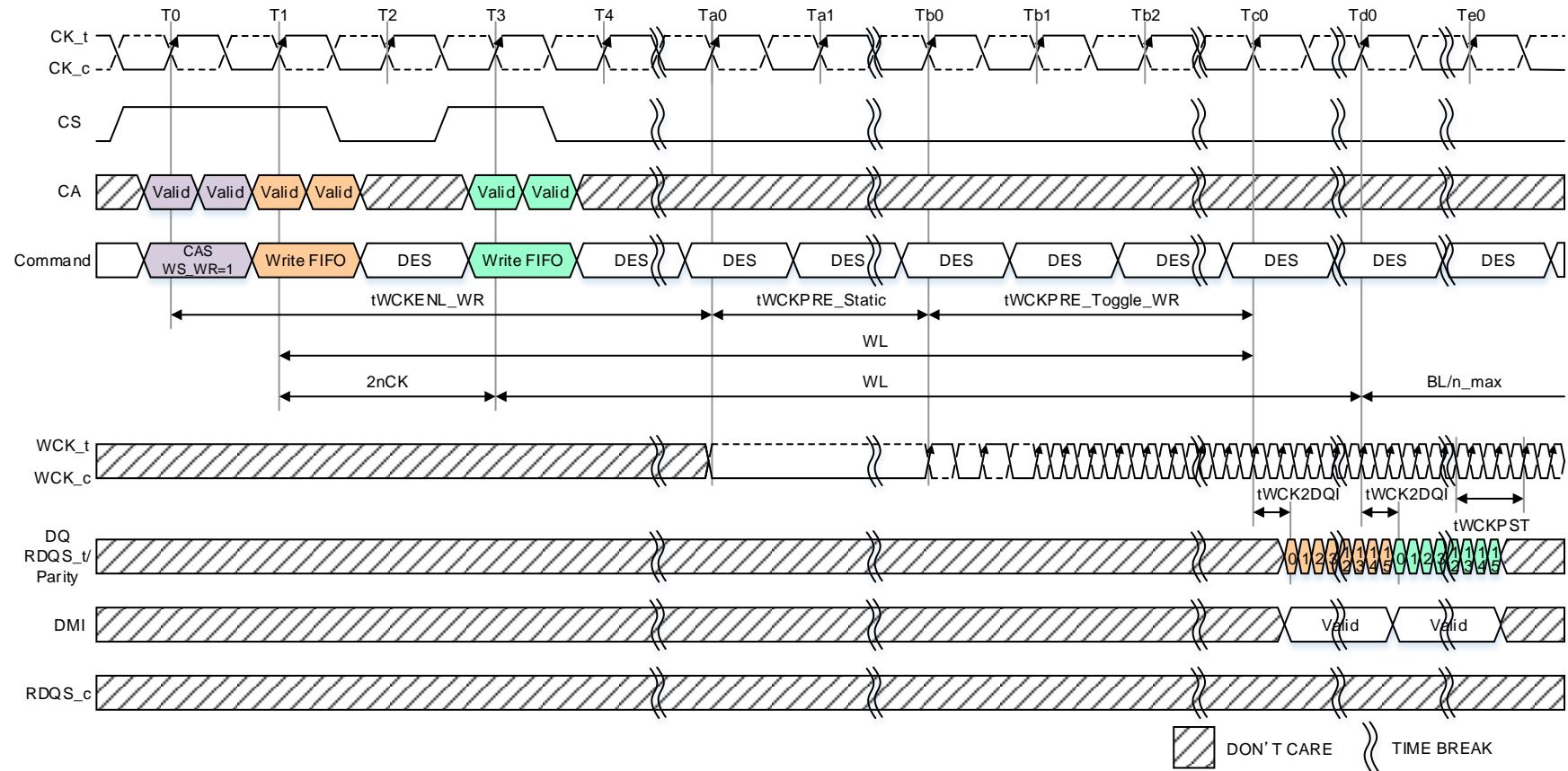
NOTE 2 The end of both RL and $tWCKPRE_Toggle_RD$ are the same timing in this instance.

NOTE 3 Data may be continuously read from the FIFO without any data corruption. After 8 Read-FIFO commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing.

NOTE 4 CAS command is needed before a Read FIFO command when a WCK synchronization will expire.

Figure 42 — Consecutive Read FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1

4.2.9.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1 Parity input activate is enabled: MRx OP[y] =1

NOTE 2 tWCK2CK is 0ps in this instance.

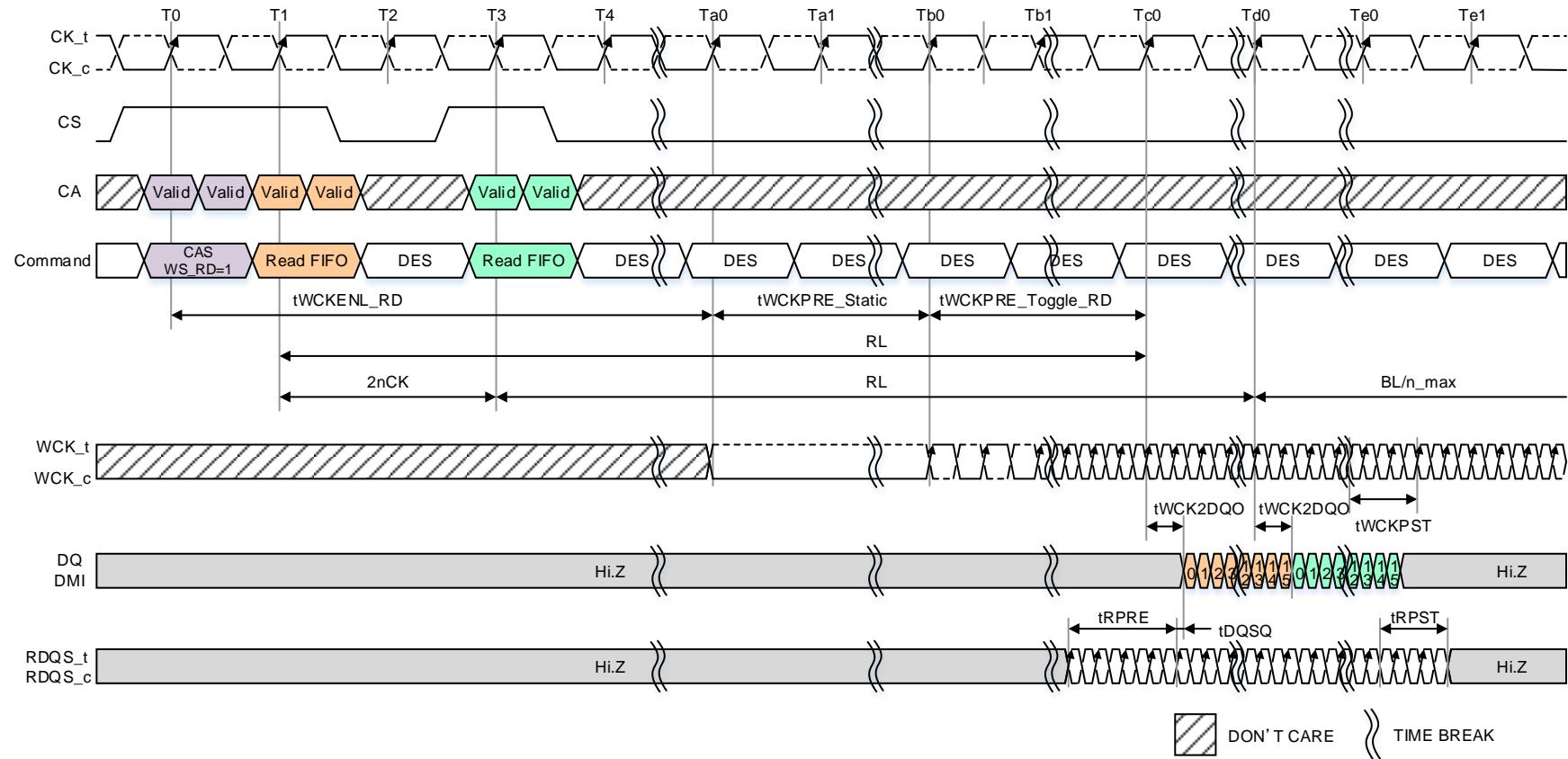
NOTE 3 The end of both WL and tWCKPRE_Toggle_WR are the same timing in this instance.

NOTE 4 The (8 +1) Write FIFO command will overwrite the FIFO data from the first command. If fewer than 8 Write-FIFO commands are executed, then the remaining FIFO locations will contain undefined data.

NOTE 5 CAS command is needed before a Write FIFO command when a WCK synchronization will expire.

Figure 43 — Consecutive Write FIFO Operation timing: Parity Data input for BG mode: CKR (WCK vs. CK) = 4:1

4.2.9.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1 Parity input activate is enabled: MRx OP[y] =1

NOTE 2 DMI pin outputs the data which written to FIFO through the Parity pin by the Write FIFO command.

NOTE 3 tWCK2CK is 0ps in this instance.

NOTE 4 The end of both RL and tWCKPRE_Toggle_RD are the same timing in this instance.

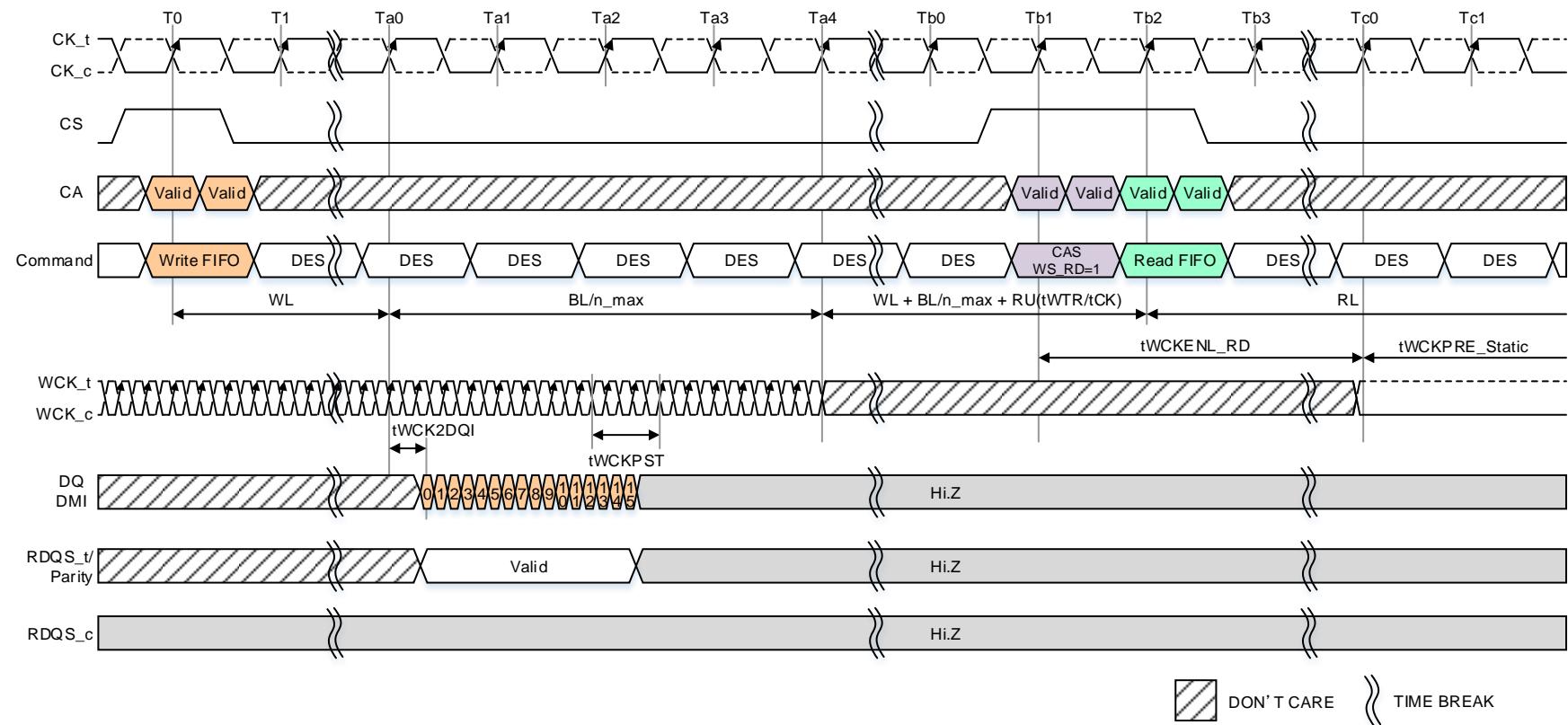
NOTE 5 Data may be continuously read from the FIFO without any data corruption. After 8 Read FIFO commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing.

NOTE 6 CAS command is needed before a Read FIFO command when a WCK synchronization will expire.

Figure 44 — Consecutive Read FIFO Operation timing: Parity Data output for BG mode: CKR (WCK vs. CK) = 4:1

4.2.9.4 Command constraints for Write/Read FIFO command

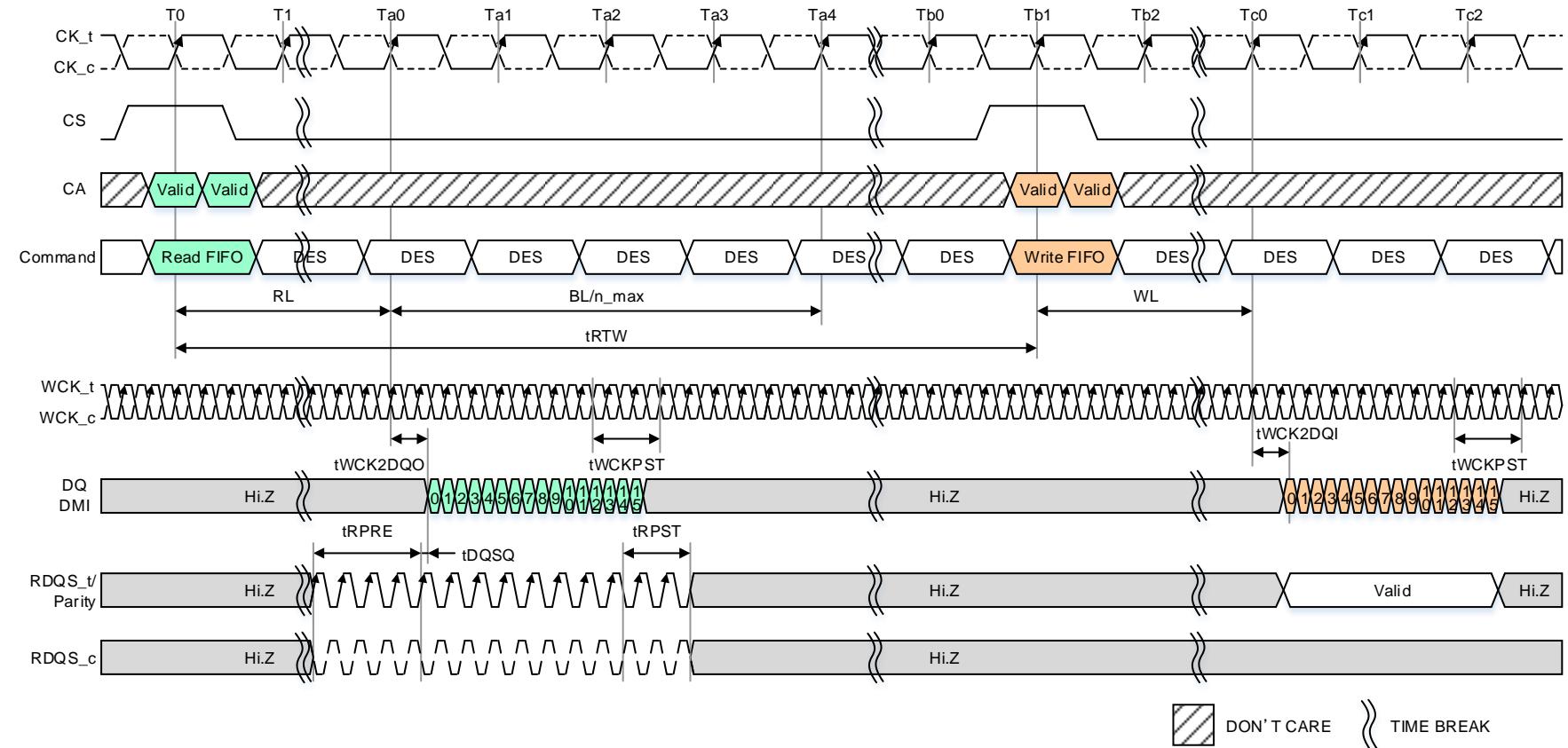
The command constraints between CAS (WS_WR), CAS (WS_RD), Write FIFO and Read FIFO are shown in 8.1.2, the command constraint section.



NOTE 1 tWCK2CK is 0ps in this instance.

Figure 45 — Write FIFO to Read FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1

4.2.9.4 Command constraints for Write/Read FIFO command (Cont'd)



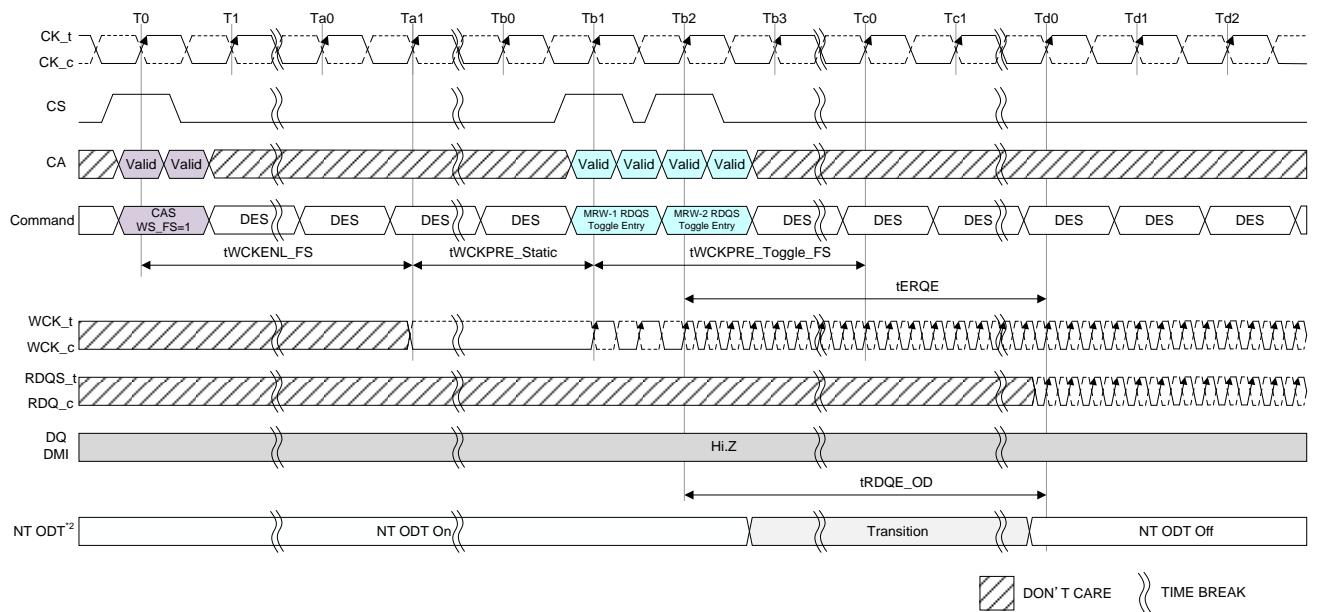
NOTE 1 tWCK2CK is 0ps in this instance.

Figure 46 — Read FIFO to Write FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1

4.2.10 RDQS toggle mode

LPDDR5 devices feature a RDQS toggle mode that outputs continuous-toggle pattern on the RDQS pins. Before issuing MRW commands, a CAS-WS_FS command is required. After “tWCKENL_FS + tWCKPRE_static”, a MRW[RDQS toggle start] has to be issued to enable the RDQS toggle mode. After “tERQE” passed after MRW-2[RDQS toggle start], LPDDR5 device will start driving RDQS_t and RDQS_c. LPDDR5 device exits the RDQS toggle mode by issuing a MRW[RDQS toggle stop]. After “tERQX” has passed from MRW-2[RDQS toggle stop], LPDDR5 RQDS will transit to a Hi-impedance state. During tERQX period, WCK has to continue toggling. Refer to LPDDR5 enhanced RDQS training mode about tERQE, tERQX and ODT related timing.

During the RDQS toggle mode, Power Down, SREF, Deep sleep, MRR, Write, Mask Write, Read, Write FIFO, Read FIFO and RDC are not allowed, but NOP, DES, ACT-1, ACT-2, PREpb, PREab, REFpb, REFab, MRW-1, MRW-2 and MPC can be issued. It is not allowed to adjust WCK duty cycle during the RDQS toggle mode through MR30 OP[3:0] for DCAL and MR30 OP[7:4] for DCAU setting.

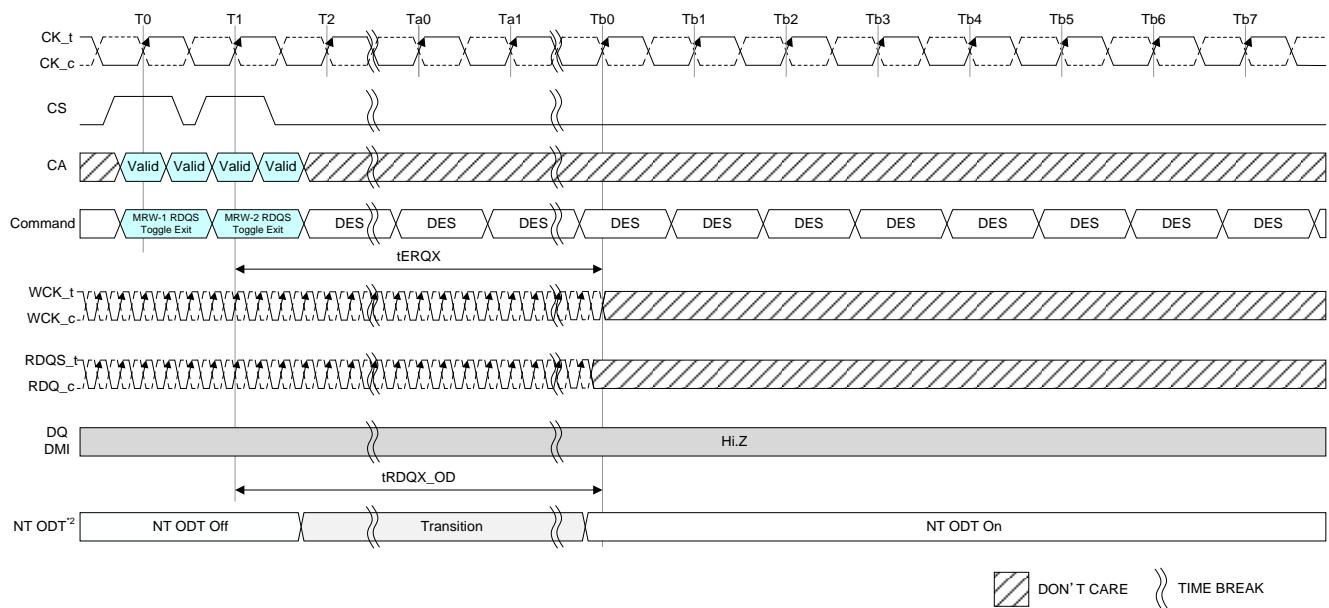


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 "NT ODT" illustrates the On/Off status of NT-ODT for RDQS_t/c, DQ and/or DMI in case of NT-ODT enabled.

Figure 47 — RDQS toggle mode entry timing example

4.2.10 RDQS toggle mode (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 "NT ODT" illustrates the On/Off status of NT-ODT for RDQS_t/c, DQ and/or DMI in case of NT-ODT enabled.

Figure 48 — RDQS toggle mode exit timing example

4.2.11 Enhanced RDQS training mode

LPDDR5 will enter Enhanced RDQS training mode by setting MRx OP[y] Enhanced RDQS training mode enable. Before issuing MRW command, CAS WS_FS is required. After WCKENL_FS+tWCKPRE static, MRW commands have to be issued to enable Enhanced RDQS training mode. tERQE after MRW, the LPDDR5 will start driving RDQS_t = low and RDQS_c =high.

To keep RDQS low-impedance, during enhanced RDQS training mode WCK has to continue toggling.

When the LPDDR5 receives a Read Command, the LPDDR5 will output RDQS and data. The RDQS preamble and postamble are followed MR10 OP[7:4]. After a burst read operation, the LPDDR5 will keep RDQS low-Z while in this mode.

LPDDR5 exits Enhanced RDQS training mode by setting MRx OP[y] Enhanced RDQS training mode disable. After tERQX has passed from MRW, LPDDR5 RDQS will transit to a Hi-impedance state. During tERQX period, WCK has to continue toggling.

During Enhanced RDQS training mode, Power Down and Deep sleep and are not allowed. During Enhanced RDQS mode, Read data training mode, ACT-1, ACT-2, PREpb, REFpb, RD, RD32, MRW-1, MRW-2, MRR, MPC and RDC can be issued.

RDQS_t and RDQS_c drive follow MR20 OP[1:0].

RDQS ODT is disabled after tRDQE_OD passed after enhanced RDQS enable MRW. RDQS ODT is enabled after tRDQX_OD passed after enhanced RDQS disable MRW.

4.2.11 Enhanced RDQS training mode (Cont'd)

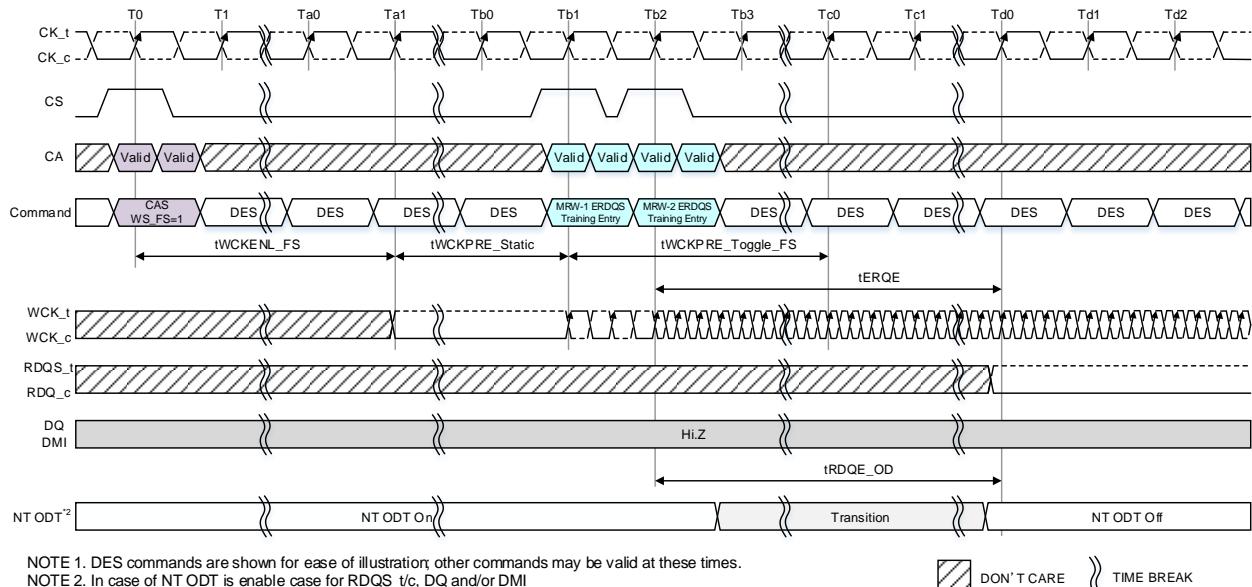


Figure 49 — Enhanced RDQS training mode entry timing

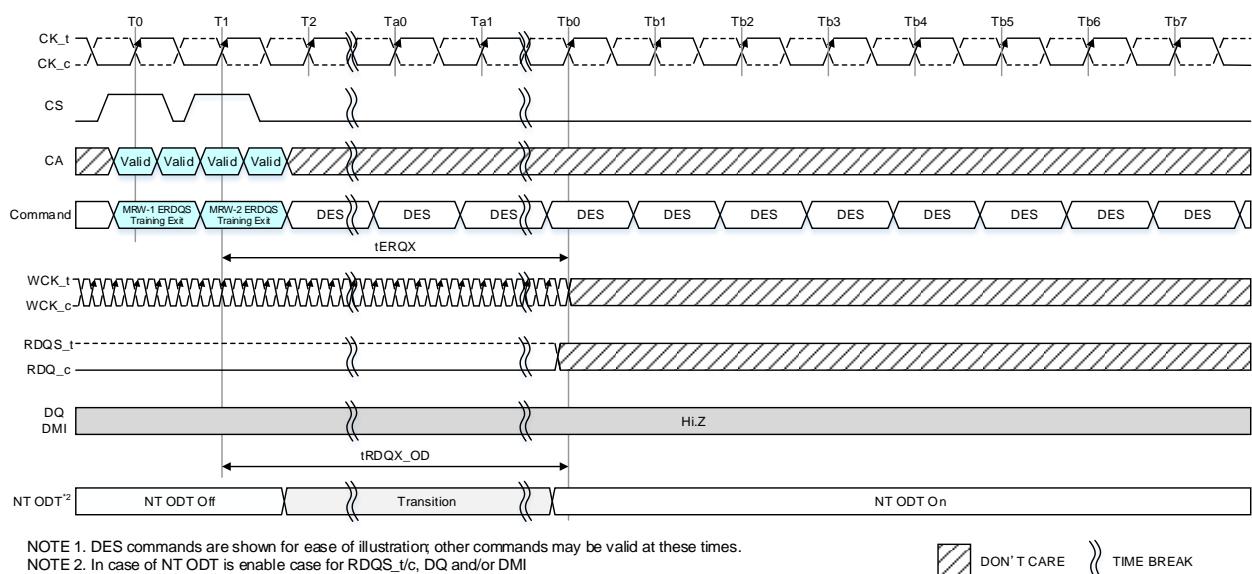


Figure 50 — Enhanced RDQS training mode exit timing

4.2.11 Enhanced RDQS training mode (Cont'd)

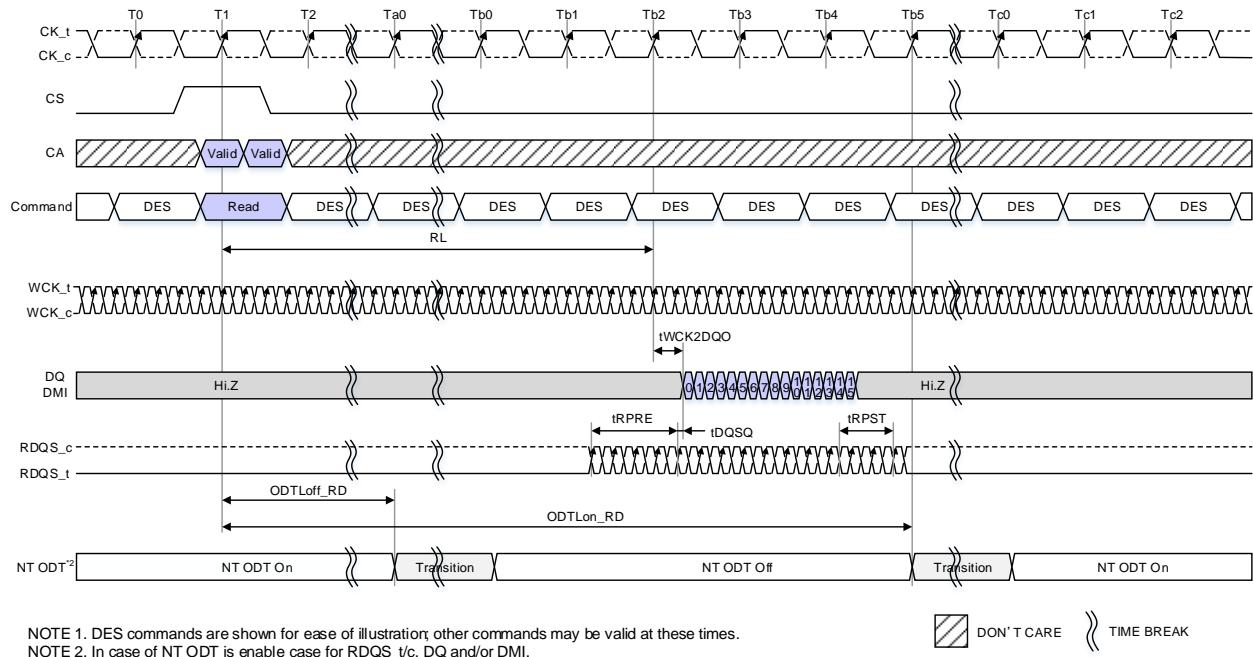


Figure 51 — Read operation during Enhanced RDQS training mode

Table 36 — Enhanced RDQS training mode entry and exit timings

Parameter	Symbol	Min/Max	Value	Unit	Note
Enhanced RDQS toggle mode entry	tERQE	Max	Max (35ns, 4nCK)	ns	
Enhanced RDQS toggle mode exit	tERQX	Max	Max (35ns, 4nCK)	ns	
ODT disable from Enhanced RDQS toggle mode entry	tRDQE_OD	Max	Max (35ns, 4nCK)	ns	
ODT enable from Enhanced RDQS toggle mode exit	tRDQX_OD	Max	Max (35ns, 4nCK)	ns	

5 Simplified LPDDR5 State Diagram

LPDDR5 SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

For the command definition, see 7.1.1.

5 Simplified LPDDR5 State Diagram (Cont'd)

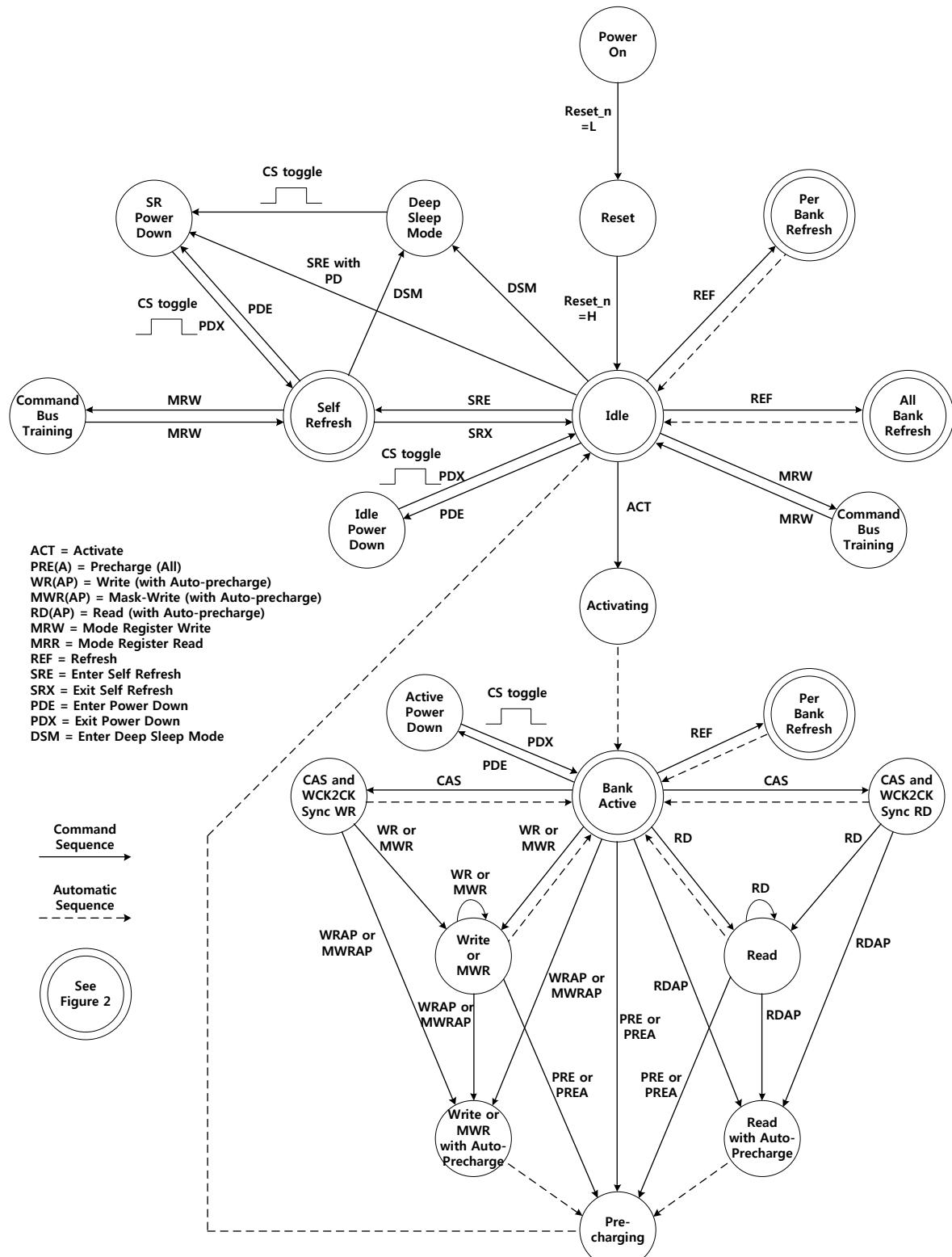


Figure 52 — LPDDR5: Simplified Bus Interface State Diagram

5 Simplified LPDDR5 State Diagram (Cont'd)

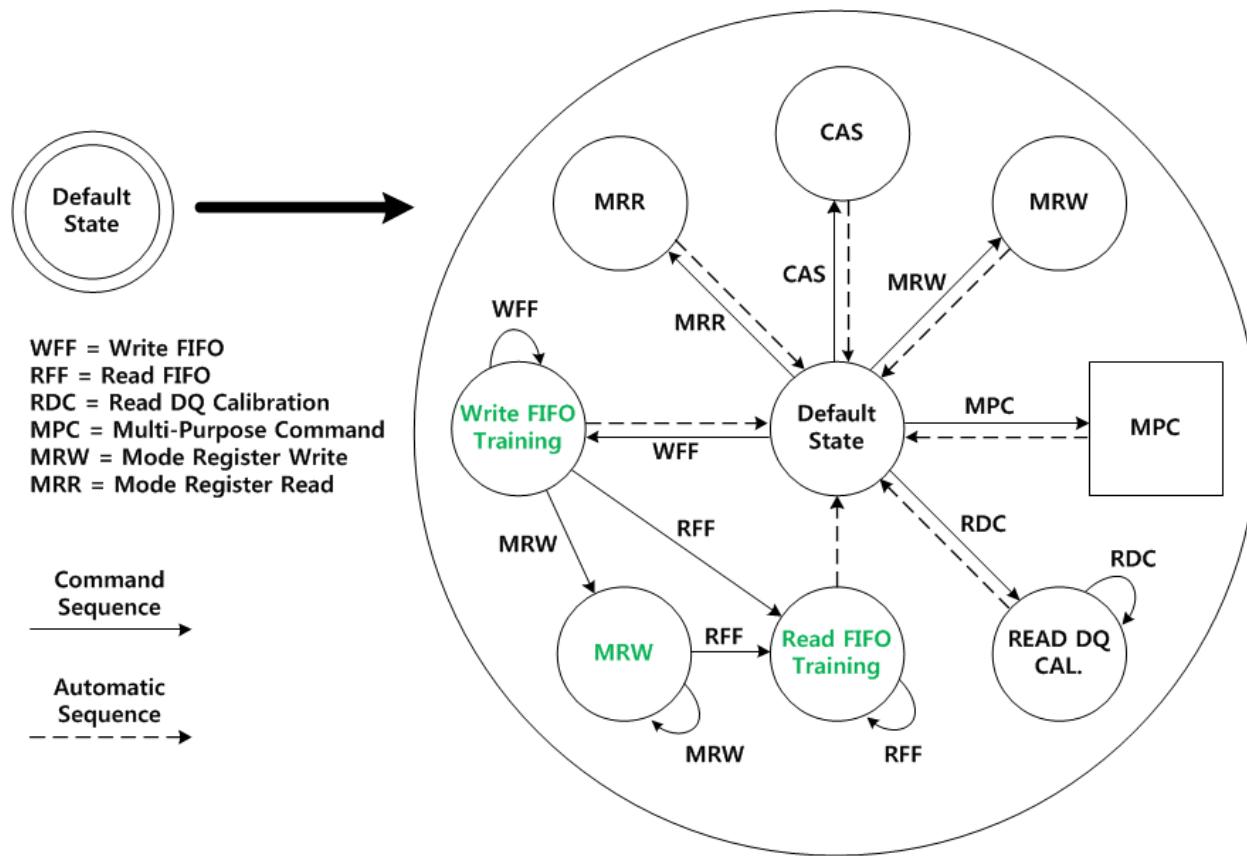


Figure 53 — Sub-State Diagram-1 related with MRR, MRW, CAS, WFF, RFF, RDC and MPC Command

5 Simplified LPDDR5 State Diagram (Cont'd)

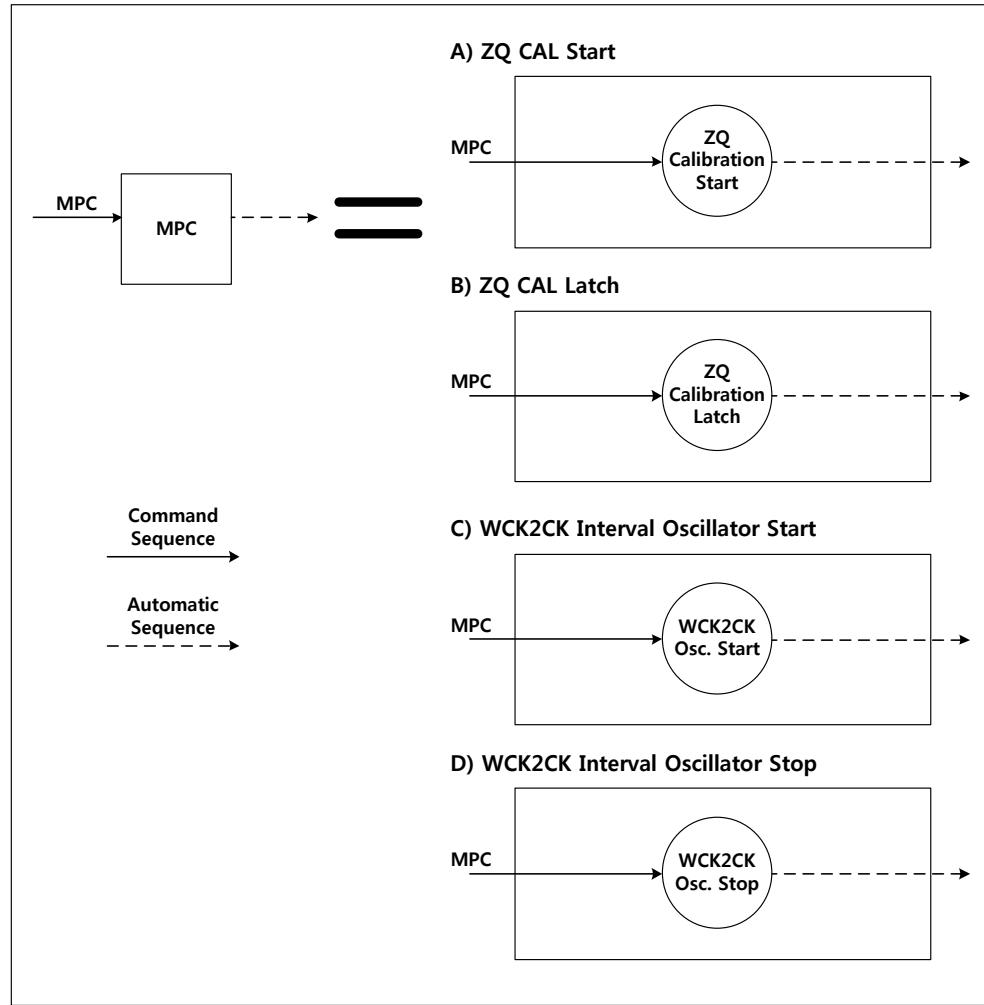


Figure 54 — Sub-State Diagram-2: related with MPC State

5 Simplified LPDDR5 State Diagram (Cont'd)

NOTE 1 From the Self-Refresh state the device can enter Power-Down, MRR, MRW, MPC and Deep Sleep Mode states. See 7.5.3, on Self-Refresh, for more information.

NOTE 2 In IDLE state, all banks are pre-charged.

NOTE 3 In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See 7.6.2, on Mode Register Write (MRW), for more information.

NOTE 4 In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See 7.6.10, on Multi-Purpose Command (MPC), for more information.

NOTE 5 This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

NOTE 6 States that have an "automatic return" and can be accessed from more than one prior state (e.g., MRW from either idle or Active states) will return to the state from when they were initiated (e.g., MRW from Idle will return to Idle).

NOTE 7 The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET state applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

NOTE 8 Bank Active state can enter "CAS and WCK2CK Sync WR", "CAS and WCK2CK Sync RD" State for WCK-to-CK Synchronization, Non-Target ODT setting or Burst Length setting if it is needed.

NOTE 9 Deep Sleep Mode state can enter Self-Refresh Power Down state toggling CS (VDD2H level). See 7.5.7 for more information on Deep Sleep Mode.

NOTE 10 CAS command is the stand alone command.

NOTE 11 "Bank Active" to "Per-Bank Refresh" transition only refers to different banks not the same bank.

NOTE 12 Only MRW commands for MR16 OP[1:0]: FSP-WR, OP[3:2]: FSP-OP, OP[6]: VRCG and MR14 OP[6:0]:VREF(DQ[7:0]) and MR15 OP[6:0]:VREF(DQ[15:8]) are allowed from WRITE FIFO command to READ FIFO command.

6 Mode Register Definition

6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM

Table 37 shows the mode registers for LPDDR5 SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode register Write command is used to write a mode register. LPDDR5 device provides additional MRR capability to some write-only Mode Registers containing important memory system configuration and status info. Mode Registers 1, 3, 11, 16, 17, 37, and 40 can be read by issuing a Mode Register Read (MRR) command.

Table 37 — Mode Register Assignment in LPDDR5 SDRAM

6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM (Cont'd)

Table 37 — Mode Register Assignment in LPDDR5 SDRAM (Cont'd)

MR #	MA[6:0]	Access	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]			
13	0D _H	W	Dual VDD2	CBT Mode	DMD	RFU	VRO	Thermal Offset					
14	0E _H	R/W	VDLC	V _{REF} (DQ[7:0])									
				V _{REF} (DQ[7:0])									
				V _{REF} (DQ[7:0])									
15	0F _H	R/W	RFU	V _{REF} (DQ[15:8])									
				V _{REF} (DQ[15:8])									
				V _{REF} (DQ[15:8])									
16	10 _H	R/W	CBT-PH	VRCG	CBT	FSP-OP		FSP-WR					
17	11 _H	R/W	x8 ODTD Upper	x8 ODTD Lower	ODTD-CA	RFU	ODTD-C K	SOC ODT					
					ODTD-CA		ODTD-C K	SOC ODT					
					ODTD-CA		ODTD-C K	SOC ODT					
18	12 _H	W	CKR	WCK2CK Leveling	RFU	WCK ON	WCK_F M	WCK ODT					
			CKR			WCK ON	WCK_F M	WCK ODT					
			CKR			WCK ON	WCK_F M	WCK ODT					
19	13 _H	W	RFU				DVFSQ		DVFSC				
							DVFSQ		DVFSC				
							DVFSQ		DVFSC				
20	14 _H	W	RDC DQ Mode	RDC DMI Mode	MRWDU	MRWDL	WCK Mode		RDQS				
			WCK Mode				RDQS		RDQS				
			WCK Mode				RDQS		RDQS				
21	15 _H	R/W	RFU	WXFE	RDCFE	WDCFE	RFU	WXFS	RDCFS	WDCFS			
22	16 _H	W	RECC		WECC		RFU						
23	17 _H	W	RFU PASR Segment Mask										
24	18 _H	N/A R/W	DFE Support	DFE Quantity for Upper Byte				RFU	DFE Quantity for Lower Byte				
				DFE Quantity for Upper Byte					DFE Quantity for Lower Byte				
				DFE Quantity for Upper Byte					DFE Quantity for Lower Byte				
25	19 _H	W	RFU	PARC	CA Inputs TERM	CK pair TERM	RFU						
26	1A _H	R/W	RFU		DCMU1	DCMU0	DCML1	DCML0	DCM Flip	DCM Start/ Stop			

6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM (Cont'd)

Table 37 — Mode Register Assignment in LPDDR5 SDRAM (Cont'd)

MR#	MA[6:0]	Access	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]							
27	1B _H	TBD	TRR														
28	1C _H	W	RFU		ZQ Mode	RFU	ZQ interval		ZQ Stop	ZQ Reset							
29	1D _H	N/A	PPR Resource														
30	1E _H	W	DCA for Upper byte			DCA for Lower byte											
			DCA for Upper byte			DCA for Lower byte											
			DCA for Upper byte			DCA for Lower byte											
31	1F _H	W	Lower-Byte per-bit control Register for DQ Calibration														
32	20 _H	W	Upper-Byte per-bit control Register for DQ Calibration														
33	21 _H	W	DQ Calibration Pattern "A"														
34	22 _H	W	DQ Calibration Pattern "B"														
35	23 _H	R	WCK2DQI Oscillator Count - LSB														
36	24 _H	R	WCK2DQI Oscillator Count - MSB														
37	25 _H	R/W	WCK2DQI interval timer run time setting														
38	26 _H	R	WCK2DQO Oscillator Count - LSB														
39	27 _H	R	WCK2DQO Oscillator Count - MSB														
40	28 _H	R/W	WCK2DQO interval timer run time setting														
41	29 _H	R/W	NT DQ ODT		PPRE	RFU											
			NT DQ ODT														
			NT DQ ODT														
42	2A _H	W	PPR KEY Protection														
43	2B _H	R	DBE_flag	SBE_count													
44	2C _H	R	Data ECC Syndrome														
45	2D _H	R	Data ECC Syndrome	Error Byte Lane	DMI ECC Syndrome												
46	2E _H	N/A	DNU (Do Not Use)														
47	2F _H	R	Serial ID-1														
48	30 _H	R	Serial ID-2														
49	31 _H	R	Serial ID-3														
50	32 _H	R	Serial ID-4														
51	33 _H	R	Serial ID-5														
52	34 _H	R	Serial ID-6														
53	35 _H	R	Serial ID-7														
54	36 _H	R	Serial ID-8														
55: 63	37 _{H:} 3F _H	N/A	DNU (Do Not Use)														

Applied when FSP=0
Applied when FSP=1
Applied when FSP=2

NOTE 1 RFU bits shall be set to "0" during writes.

NOTE 2 RFU bits shall be read as "0" during reads.

NOTE 3 All mode registers that are specified as RFU or write-only shall return undefined data when read.

NOTE 4 All mode registers that are specified as RFU should not be written.

NOTE 5 Writes to read-only registers shall have no impact on the functionality of the device.

6.2 Mode Register Definition

6.2.1 Mode Register definition

Table 38 — MR0 Register Information (MA [7:0] = 00_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	RFU	RFU	Latency Mode	RFU

Table 39 — MR0 definition

Function	Register Type	Operand	Data	Notes
Latency Mode	Read only	OP[1]	0 _B : Device supports X16 mode latency 1 _B : Device supports byte mode latency	1
NOTE 1 Byte mode devices only support byte mode latency.				

6.2.1 Mode Register definition (Cont'd)

Table 40 — MR1 Register Information (MA[5:0] = 01_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WL				CK Mode	RFU	RFU	RFU

Table 41 — MR1 definition

Function	Register Type	Operand	Data				Notes	
CK mode		OP[3]	0 _B : Differential (default) 1 _B : Single Ended				1,2,3	
WL (Write Latency)		OP[7:4]	WL (x16/ch, DVFSC disable)					
			OP[7:4]	WCK:CK	Set A	Set B		
			0000 _B	2:1	4	4		
			0001 _B		4	6		
			0010 _B		6	8		
			0011 _B		8	10		
			0100 _B		8	14		
			0101 _B		10	16		
			0000 _B (default)	4:1	2	2		
			0001 _B		2	3		
			0010 _B		3	4		
			0011 _B		4	5		
			0100 _B		4	7		
			0101 _B		5	8		
			0110 _B		6	9		
			0111 _B		6	11		
			1000 _B		7	12		
			1001 _B		8	14		
			1010 _B		9	15		
			1011 _B		9	16		
			All others are RFU					
			WL (x16/ch, DVFSC enable)					
			OP[7:4]	WCK:CK	Set A	Set B		
			0000 _B	2:1	TBD	TBD		
			0001 _B		TBD	TBD		
			0010 _B		TBD	TBD		
			0000 _B (default)	4:1	TBD	TBD		
			0001 _B		TBD	TBD		
			0010 _B		TBD	TBD		
			All others are RFU					

6.2.1 Mode Register definition (Cont'd)

Table 41 — MR1 definition (cont'd)

Function	Register Type	Operand	Data				Notes	
CK mode		OP[3]	0_B : Differential (default) 1_B : Single Ended				1,2,3	
			WL (x8/ch, DVFS disable)					
			OP[7:4]	WCK:CK	Set A	Set B		
			0000 _B	2:1	4	4		
			0001 _B		4	6		
			0010 _B	2:1	6	8		
			0011 _B		8	10		
			0100 _B	2:1	8	14		
			0101 _B		10	16		
			0000 _B (default)	4:1	2	2		
			0001 _B		2	3		
			0010 _B		3	4		
			0011 _B		4	5		
			0100 _B		4	7		
			0101 _B		5	8		
			0110 _B		6	9		
			0111 _B		6	11		
			1000 _B		7	12		
			1001 _B		8	14		
			1010 _B		9	15		
			1011 _B		9	16		
WL (Write Latency)		OP[7:4]	All others are RFU				2,3	
			WL (x8/ch, DVFS enable)					
			OP[7:4]	WCK:CK	Set A	Set B		
			0000 _B	2:1	TBD	TBD		
			0001 _B		TBD	TBD		
			0010 _B		TBD	TBD		
			0000 _B (default)	4:1	TBD	TBD		
			0001 _B		TBD	TBD		
			0010 _B		TBD	TBD		
			All others are RFU					

6.2.1 Mode Register definition (Cont'd)

Table 42 — MR2 Register Information (MA[7:0] = 02_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
nWR				RL and nRTP			

Table 43 — MR2 Definition

Function	Register Type	Operand	Data				Notes
RL (Read latency) and nRTP (Read to Precharge delay)	Write-only	OP[3:0]	RL and nRTP (x16/ch, DVFSC disable)				
			OP[3:0]	WCK:CK Ratio	RL	nRTP	
			0000 _B	2:1	6	4	
			0001 _B	2:1	8	4	
			0010 _B	2:1	10	4	
			0011 _B	2:1	12	4	
			0100 _B	2:1	16	6	
			0101 _B	2:1	18	6	
			0000 _B Default	4:1	3	2	
			0001 _B	4:1	4	2	
			0010 _B	4:1	5	2	
			0011 _B	4:1	6	2	
			0100 _B	4:1	8	3	
			0101 _B	4:1	9	3	
			0110 _B	4:1	10	4	
			0111 _B	4:1	12	4	
			1000 _B	4:1	13	5	
			1001 _B	4:1	14	5	
			1010 _B	4:1	15	6	
			1011 _B	4:1	17	6	
			All others are RFU				
			RL and nRTP (x16/ch, DVFSC enable)				
			OP[3:0]	WCK:CK Ratio	RL	nRTP	
			0000 _B	2:1	TBD	TBD	
			0001 _B	2:1	TBD	TBD	
			0010 _B	2:1	TBD	TBD	
			0011 _B	2:1	TBD	TBD	
			0100 _B	2:1	TBD	TBD	
			0101 _B	2:1	TBD	TBD	
			0000 _B	4:1	TBD	TBD	
			0001 _B	4:1	TBD	TBD	
			0010 _B	4:1	TBD	TBD	
			0011 _B	4:1	TBD	TBD	
			0100 _B	4:1	TBD	TBD	
			0101 _B	4:1	TBD	TBD	
			All others are RFU				

1,2

6.2.1 Mode Register definition (Cont'd)

Table 43 — MR2 Definition (cont'd)

Function	Register Type	Operand	Data			Notes		
nWR (Write recovery)	Write-only	OP[7:4]	nWR (x16/ch, DVFSC disable)			1,2,3		
			OP[7:4]	WCK:CK Ratio	nWR			
			0000 _B	2:1	TBD			
			0001 _B	2:1	TBD			
			0010 _B	2:1	TBD			
			0011 _B	2:1	TBD			
			0100 _B	2:1	TBD			
			0101 _B	2:1	TBD			
			0000 _B Default	4:1	TBD			
			0001 _B	4:1	TBD			
			0010 _B	4:1	TBD			
			0011 _B	4:1	TBD			
			0100 _B	4:1	TBD			
			0101 _B	4:1	TBD			
			0110 _B	4:1	TBD			
			0111 _B	4:1	TBD			
			1000 _B	4:1	TBD	All others are RFU		
			1001 _B	4:1	TBD			
			1010 _B	4:1	TBD			
			1011 _B	4:1	TBD			
			nWR (x16/ch, DVFSC enable)					
			OP[7:4]	WCK:CK Ratio	nWR			
			0000 _B	2:1	TBD			
			0001 _B	2:1	TBD			
			0010 _B	2:1	TBD			
			0011 _B	2:1	TBD			
			0100 _B	2:1	TBD			
			0101 _B	2:1	TBD			
			0000 _B	4:1	TBD			
			0001 _B	4:1	TBD			
			0010 _B	4:1	TBD			
			0011 _B	4:1	TBD			
			0100 _B	4:1	TBD			
			0101 _B	4:1	TBD			
			All others are RFU			NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address. NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation. NOTE 3 The programmed value of nWR is the number of clock cycles the LPDDR5-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled.		

6.2.1 Mode Register definition (Cont'd)

Table 44 — MR3 Register Information (MA[7:0] = 03_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	WLS	BK/BG ORG			PDDS	

Table 45 — MR3 Definition

Function	Register Type	Operand	Data	Notes
PDDS (Pull-Down Drive Strength)	Write-only	OP[2:0]	000 _B : RFU 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 (default) 111 _B : Reserved	1,2,3
BK/BG ORG (Bank/Bank Group Organization)		OP[4:3]	00 _B : BG Mode 01 _B : 8B Mode 10 _B : 16B Mode 11 _B : Reserved	2,3,5,6
WLS (Write Latency Set)		OP[5]	0 _B : Write Latency Set "A" (default) 1 _B : Write Latency Set "B"	2,3
DBI-RD (DBI-Read select)		OP[6]	0 _B : Disabled (default) 1 _B : Read DBI-DC Enabled	2,3
DBI-WR (DBI-Write select)		OP[7]	0 _B : Disabled (default) 1 _B : Write DBI-DC Enabled	2,3,4

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 Masked Write must use DBI DC only. For more details concerning masked writes with DBI enabled, refer to 7.4.10 for information on data bus inversion.

NOTE 5 16B Mode with DVFS enabled can support up to 1600Mbps (\leq 1600Mbps). Please refer to operating frequency table in 2.2.5.

NOTE 6 The supported operation data rate for each Bank/Bank Group Organization is as follows.

- BG Mode for more than 3200Mbps (>3200Mbps).
- 8B Mode for all data rate range.
- 16B Mode for equal or less than 3200Mbps (\leq 3200Mbps).

6.2.1 Mode Register definition (Cont'd)

Table 46 — MR4 Register Information (MA[7:0] = 04_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU	ZQUF				Refresh Rate	

Table 47 — MR4 Definition

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read-only	OP[4:0]	00000 _B : SDRAM Low temperature operating limit exceeded 00001 _B : 8x refresh 00010 _B : 6x refresh 00011 _B : 4x refresh 00100 _B : 3.3x refresh 00101 _B : 2.5x refresh 00110 _B : 2.0x refresh 00111 _B : 1.7x refresh 01000 _B : 1.3x refresh 01001 _B : 1x refresh 01010 _B : 0.7x refresh 01011 _B : 0.5x refresh 01100 _B : 0.25x refresh, no de-rating 01101 _B : 0.25x refresh, with de-rating 01110 _B : 0.125x refresh, no de-rating 01111 _B : 0.125x refresh, with de-rating 11111 _B : SDRAM High temperature operating limit exceeded All others are reserved.	1,2,3,4,6,7
ZQUF (ZQ Update Flag)		OP[5]	0 _B : No change in calibration code since previous ZQ Latch command 1 _B : Calibration code has changed since previous ZQ Latch command	8
ZQ Master		OP[6]	0 _B : Not a master die 1 _B : Master die for ZQ Calibration purposes	9,10
TUF (Temperature Update Flag)		OP[7]	0 _B : No change in OP[4:0] since last MR4 read 1 _B : Change in OP[4:0] since last MR4 read (default)	5,6,7

NOTE 1 The refresh rate for each MR4-OP[4:0] setting applies to tREFI, tREFIpb, and tREFW. OP[4:0]= 01001_B corresponds to a device temperature of 85 °C. Other values require either a longer (1.3x, 8x) refresh interval at lower temperatures, or a shorter (0.7x, 0.125x) refresh interval at higher temperatures. If OP[4:0] is from 01010_B to 11111_B, the device temperature is greater than 85°C.

NOTE 2 At higher temperatures (>85 °C), AC timing derating may be required. If derating is required the LPDDR5-SDRAM will set OP[4:0]= 01101_B or 01111_B. See derating timing requirements in 9.2.

NOTE 3 DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.

NOTE 4 The device may not operate properly when OP[4:0]=00000_B or 11111_B.

NOTE 5 When OP[7]=1, the refresh rate reported in OP[4:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.

NOTE 6 OP[4:0] bits are indicated the latest Refresh Rate whenever OP[7]=1_B.

NOTE 7 See 7.6.9, on the Temperature Sensor, for information on the recommended frequency of reading MR4.

NOTE 8 After Power up initialization and reset sequence have been completed ZQUF MR4 OP[5] indicate 0_B.

NOTE 9 In command-based calibration mode, ZQCal Start commands only need to be issued to the ZQ Master die or dice to maintain accurate calibration. ZQCal Start commands received by non-ZQ Master die will be ignored. All die which share ZQ resources with a ZQ Master die that receives a valid ZQCal Start command will be calibrated. ZQCal Latch commands may be issued to each of these die after tZQCAL4, tZQCAL8 or tZQCAL16 has been met.

NOTE 10 LPDDR5 packages with more than one ZQ pin may include more than one ZQ Master die.

6.2.1 Mode Register definition (Cont'd)

Table 48 — MR5 Register Information (MA[7:0] = 05_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR5 Manufacturer ID							

Table 49 — MR5 Definition

Function	Register Type	Operand	Data				Notes
LPDDR5 Manufacturer ID	Read-only	OP[7:0]	See JEP166, LPDDR5 Manufacturer ID Codes				

Table 50 — MR6 Register Information (MA[7:0] = 06_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Table 51 — MR6 Definition

Function	Register Type	Operand	Data				Notes
LPDDR5 Revision ID-1	Read-only	OP[7:0]	00000000 _B : A-version 00000001 _B : B-version				1

NOTE 1 MR6 is vendor specific.

Table 52 — MR7 Register Information (MA[7:0] = 07_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Table 53 — MR7 Definition

Function	Register Type	Operand	Data				Notes
LPDDR5 Revision ID-2	Read-only	OP[7:0]	00000000 _B : A-version 00000001 _B : B-version				1

NOTE 1 MR7 is vendor specific.

6.2.1 Mode Register definition (Cont'd)

Table 54 — MR8 Register Information (MA[7:0] = 08_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width	Density						Type

Table 55 — MR8 Definition

Function	Register Type	Operand	Data	Notes
Type		OP[1:0]	00 _B : S32 (32n pre-fetch/8Banks), S16 SDRAM (16n pre-fetch/4Banks 4Bank Groups), S16 SDRAM (16n pre-fetch /16 Banks) All Others: Reserved	
Density	Read-only	OP[5:2]	0000 _B : 2Gb 0001 _B : 3Gb 0010 _B : 4Gb 0011 _B : 6Gb 0100 _B : 8Gb 0101 _B : 12Gb 0110 _B : 16Gb 0111 _B : 24Gb 1000 _B : 32Gb All Others: Reserved	
IO Width		OP[7:6]	00 _B : x16 01 _B : x8 All Others: Reserved	

Table 56 — MR9 Register Information (MA[7:0] = 09_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

Table 57 — MR9 Definition

Function	Register Type	Operand	Data	Notes
Vendor Specific Test Register	Write-only	OP[7:0]	Vendor Specific	1

NOTE 1 Only 00_H should be written to this register.

6.2.1 Mode Register definition (Cont'd)

Table 58 — MR10 Register Information (MA [7:0] = 0A_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RDQS PST		RDQS PRE		WCK PST		RFU	RPST Mode

Table 59 — MR10 Definition

Function	Register Type	Operand	Data	Notes
RDQS Post-amble mode	Write-only	OP[0]	0 _B : Toggle Mode (default) 1 _B : Static Mode	1,2,3
WCK PST (WCK Post-amble Length)		OP[3:2]	00 _B : 2.5*tWCK (default) 01 _B : 4.5*tWCK 10 _B : 6.5*tWCK 11 _B : Reserved	1,2,3,4,5
RDQS PRE (RD Pre-amble Length)		OP[5:4]	00 _B : Static:4*tWCK,Toggle:0 (Default) 01 _B : Static:2*tWCK,Toggle:2*tWCK 10 _B : Static:0,Toggle:4*tWCK 11 _B : Static:=RDQS_PRE, Toggle:4*tWCK	1,2,3,6,7
RDQS PST (RD Post-amble Length)		OP[7:6]	00 _B : 0.5*tWCK (Default) 01 _B : 2.5*tWCK 10 _B : 4.5*tWCK 11 _B : Reserved	1,2,3,4

NOTE 1 All units are tWCK.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 tWCKPST length should be larger than tRPST length.

NOTE 5 WCK PST OP[3:2] applies to both read and write operation timing as same setting.

NOTE 6 OP[5:4]=11_B can be supported over 3200Mbps operation and tRDQS_PRE is Min 2*tWCK and Max 4*tWCK.

NOTE 7 OP[5:4]=00_B/01_B/10_B can be supported over all frequency range.

6.2.1 Mode Register definition (Cont'd)

Table 60 — MR11 Register Information (MA[7:0] = 0B_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA ODT			RFU		DQ ODT	

Table 61 — MR11 Definition

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000 _B : Disable (Default) 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 111 _B : RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	000 _B : Disable (Default) 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 111 _B : RFU	1,2,3

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

6.2.1 Mode Register definition (Cont'd)

Table 62 — MR12 Register Information (MA[5:0] = 0C_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VBS	$V_{REF}(CA)$						

Table 63 — MR12 Definition

Function	Register Type	Operand	Data	Notes
$V_{REF}(CA)$ ($V_{REF}(CA)$ Setting)	Read/ Write	OP[6:0]	0000000 _B : -- Thru -- 1111111 _B : See table below	1,2,3,4, 5,7
VBS ($V_{REF}(CA)$ Byte Select)	Write	OP[7]	0 _B : Write the $V_{REF}(CA)$ values to OP[6:0] for x16 device, and Byte mode device which is assigned lower byte: DQ[7:0]. 1 _B : Write the $V_{REF}(CA)$ values to OP[6:0] for Byte mode device which is assigned upper byte: DQ[15:8].	6,7

NOTE 1 This register controls the VREF(CA) levels for Frequency-Set-Point[2:0].

NOTE 2 A read (MRR) to this register places the contents of OP[6:0] on DQ[6:0]. DQ[7] will read 0B. See 7.6.1 for more information on MRR Operation.

NOTE 3 A write to MR12 OP[6:0] sets the internal VREF(CA) level for FSP[0] when MR16 OP[1:0]=00B, sets FSP[1] when MR16 OP[1:0]=01B or sets FSP[2] when MR16 OP[1:0]=10B. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See 4.2.2 for more information on VREF(CA) training.

NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 6 Even if when the MRW command issues to the x16 device, writing "0" to OP[7] which is not a sticky bit is required.

NOTE 7 Byte Mode device output each individual MR12 OP[6:0] from DQ[7:0] for lower byte device and from DQ[15:8] for upper byte device by MRR command. OP[7] controls only the MRW operation.

6.2.1 Mode Register definition (Cont'd)

Table 64 — MR12 V_{REF}(CA) Settings

Function	Operand	V _{REF} Values (% of VDDQ)							Notes
V _{REF} Settings for MR12	OP [6:0]	0000000 _B :	10.0 ^b	0100000 _B :	26.0	1000000 _B :	42.0	1100000 _B :	58.0
		0000001 _B :	10.5 ^b	0100001 _B :	26.5	1000001 _B :	42.5	1100001 _B :	58.5
		0000010 _B :	11.0 ^b	0100010 _B :	27.0	1000010 _B :	43.0	1100010 _B :	59.0
		0000011 _B :	11.5 ^b	0100011 _B :	27.5	1000011 _B :	43.5	1100011 _B :	59.5
		0000100 _B :	12.0 ^b	0100100 _B :	28.0	1000100 _B :	44.0	1100100 _B :	60.0
		0000101 _B :	12.5 ^b	0100101 _B :	28.5	1000101 _B :	44.5	1100101 _B :	60.5
		0000110 _B :	13.0 ^b	0100110 _B :	29.0	1000110 _B :	45.0	1100110 _B :	61.0
		0000111 _B :	13.5 ^b	0100111 _B :	29.5	1000111 _B :	45.5	1100111 _B :	61.5
		0001000 _B :	14.0 ^b	0101000 _B :	30.0	1001000 _B :	46.0	1101000 _B :	62.0
		0001001 _B :	14.5 ^b	0101001 _B :	30.5	1001001 _B :	46.5	1101001 _B :	62.5
		0001010 _B :	15.0	0101010 _B :	31.0	1001010 _B :	47.0	1101010 _B :	63.0
		0001011 _B :	15.5	0101011 _B :	31.5	1001011 _B :	47.5	1101011 _B :	63.5
		0001100 _B :	16.0	0101100 _B :	32.0	1001100 _B :	48.0	1101100 _B :	64.0
		0001101 _B :	16.5	0101101 _B :	32.5	1001101 _B :	48.5	1101101 _B :	64.5
		0001110 _B :	17.0	0101110 _B :	33.0	1001110 _B :	49.0	1101110 _B :	65.0
		0001111 _B :	17.5	0101111 _B :	33.5	1001111 _B :	49.5	1101111 _B :	65.5
		0010000 _B :	18.0	0110000 _B :	34.0	1010000 _B : (default)	50.0	1110000 _B :	66.0
		0010001 _B :	18.5	0110001 _B :	34.5	1010001 _B :	50.5	1110001 _B :	66.5
		0010010 _B :	19.0	0110010 _B :	35.0	1010010 _B :	51.0	1110010 _B :	67.0
		0010011 _B :	19.5	0110011 _B :	35.5	1010011 _B :	51.5	1110011 _B :	67.5
		0010100 _B :	20.0	0110100 _B :	36.0	1010100 _B :	52.0	1110100 _B :	68.0
		0010101 _B :	20.5	0110101 _B :	36.5	1010101 _B :	52.5	1110101 _B :	68.5
		0010110 _B :	21.0	0110110 _B :	37.0	1010110 _B :	53.0	1110110 _B :	69.0
		0010111 _B :	21.5	0110111 _B :	37.5	1010111 _B :	53.5	1110111 _B :	69.5
		0011000 _B :	22.0	0111000 _B :	38.0	1011000 _B :	54.0	1111000 _B :	70.0
		0011001 _B :	22.5	0111001 _B :	38.5	1011001 _B :	54.5	1111001 _B :	70.5
		0011010 _B :	23.0	0111010 _B :	39.0	1011010 _B :	55.0	1111010 _B :	71.0
		0011011 _B :	23.5	0111011 _B :	39.5	1011011 _B :	55.5	1111011 _B :	71.5
		0011100 _B :	24.0	0111100 _B :	40.0	1011100 _B :	56.0	1111100 _B :	72.0
		0011101 _B :	24.5	0111101 _B :	40.5	1011101 _B :	56.5	1111101 _B :	72.5
		0011110 _B :	25.0	0111110 _B :	41.0	1011110 _B :	57.0	1111110 _B :	73.0
		0011111 _B :	25.5	0111111 _B :	41.5	1011111 _B :	57.5	1111111 _B :	73.5

NOTE 1 These values may be used for MR12 OP[6:0] to set the VREF(CA) levels in the LPDDR5-SDRAM.

NOTE 2 The MR12 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for CA and CK are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

NOTE 3 Absolute CA VREF low level (%code * VDDQ) must be higher than or equal to 75mV for normal operation. Vref error is not included this calculation.

NOTE 4 Absolute CA Vref high level (%code * VDDQ) must be lower than or equal to 350mV. Vref error is not included this calculation.

NOTE 5 Vref codes from 0000000_B to 0001001_B are able to be used only for testing purpose not for normal operation. Vref accuracy are not guaranteed from 0000000_B to 0001001_B.

1,2,3,4

6.2.1 Mode Register definition (Cont'd)

Table 65 — MR13 Register Information (MA[5:0] = 0D_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Dual VDD2	CBT Mode	DMD		RFU	VRO		Thermal Offset

Table 66 — MR13 Definition

Function	Register Type	Operand	Data	Notes
Thermal Offset	Write-only	OP[1:0]	00 _B : No offset, 0~5°C gradient (default) 01 _B : 5°C offset, 5~10°C gradient 10 _B : 10°C offset, 10~15°C gradient 11 _B : Reserved	
VRO (VREF Output)		OP[2]	0 _B : Normal operation (default) 1 _B : Output the VREF(CA) and VREF(DQ) values on DQ bits	1
DMD (Data Mask Disable)		OP[5]	0 _B : Data Mask Operation Enabled (default) 1 _B : Data Mask Operation Disabled	5
CBT Mode		OP[6]	0 _B : CBT Training Mode 1 (default) 1 _B : CBT Training Mode 2	
Dual VDD2		OP[7]	0 _B : Dual VDD2 rail (1.05V & 0.9V) used (default) 1 _B : Single 1.05V VDD2 rail used	2,3,4

NOTE 1 When set, the LPDDR5-SDRAM will output the VREF(CA) and VREF(DQ) voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR16 OP[3:2], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels. The DQ pins used for VREF output are vendor specific.

NOTE 2 LPDDR5 SDRAM may be powered up / initialized/ reset using either a single or dual VDD2 configuration regardless of the OP[7] setting. OP[7] shall be set based on the VDD2 configuration during initialization before normal operation. See 4.1 for additional information.

NOTE 3 In the single VDD2 configuration (1.05V), the same voltage shall be supplied to all VDD2L and VDD2H balls.

NOTE 4 When enabled (OP[7]=1_B), MR19 OP[1:0] setting is ignored and DRAM operates in High Speed mode.

NOTE 5 When enabled (OP[5]=0_B) data masking is enabled for the device. When disabled (OP[5]=1_B), masked write command is illegal. See 7.4.10, LPDDR5 Data Mask (DM) and Data Bus Inversion (DBI) Function.

6.2.1 Mode Register definition (Cont'd)

Table 67 — MR14 Register Information (MA[7:0] = 0E_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VDLC	$V_{REF}(DQ[7:0])$						

Table 68 — MR14 definition

Function	Register Type	Operand	Data	Notes
$V_{REF}(DQ[7:0])$ ($V_{REF}(DQ[7:0])$ Setting)	Read/ Write	OP[6:0]	0000000 _B : -- Thru -- 1111111 _B : See table below	1,2,3,4,5
VDLC (V_{REF} DQ Lower byte copy)		OP[7]	X16 device only 0 _B : $V_{REF}(DQ[15:8])$ follow MR15 OP[6:0] code (default) 1 _B : $V_{REF}(DQ[15:8])$ follow MR14 OP[6:0] code Byte Mode device ignores OP[7]	6,7

NOTE 1 This register controls the $V_{REF}(DQ[7:0])$ levels for Frequency-Set-Point[2:0].

NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See 7.6.1 for more information on MRR Operation.

NOTE 3 A write to OP[6:0] sets the internal $V_{REF}(DQ[7:0])$ level for FSP[0] when MR16 OP[1:0]=00_B, sets FSP[1] when MR16 OP[1:0]=01_B or sets FSP[2] when MR16 OP[1:0]=10_B. The time required for $V_{REF}(DQ[7:0])$ to reach the set level depends on the step size from the current level to the new level. See 4.1.1 for more information on $V_{REF}(DQ)$ training.

NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 6 When OP[7] is 1B, MR14 MRR will return $V_{REF}(DQ[15:8])$ and MR15 MRR value is undefined. To verify the V_{REF} code, please refer to Table 69 for MR14 OP[6:0].

NOTE 7 Byte mode device doesn't support VDLC function. SOC need to set MR14 and MR15 to individual devices.

6.2.1 Mode Register definition (Cont'd)

Table 69 — MR14 $V_{REF}(DQ[7:0])$ Settings

Function	Operand	V_{REF} Values (% of V_{DDQ})							Notes
V_{REF} Settings for MR14	OP [6:0]	0000000 _B :	10.0 ⁻⁵	0100000 _B :	26.0	1000000 _B :	42.0	1100000 _B :	58.0
		0000001 _B :	10.5 ⁻⁵	0100001 _B :	26.5	1000001 _B :	42.5	1100001 _B :	58.5
		0000010 _B :	11.0 ⁻⁵	0100010 _B :	27.0	1000010 _B :	43.0	1100010 _B :	59.0
		0000011 _B :	11.5 ⁻⁵	0100011 _B :	27.5	1000011 _B :	43.5	1100011 _B :	59.5
		0000100 _B :	12.0 ⁻⁵	0100100 _B :	28.0	1000100 _B :	44.0	1100100 _B :	60.0
		0000101 _B :	12.5 ⁻⁵	0100101 _B :	28.5	1000101 _B :	44.5	1100101 _B :	60.5
		0000110 _B :	13.0 ⁻⁵	0100110 _B :	29.0	1000110 _B :	45.0	1100110 _B :	61.0
		0000111 _B :	13.5 ⁻⁵	0100111 _B :	29.5	1000111 _B :	45.5	1100111 _B :	61.5
		0001000 _B :	14.0 ⁻⁵	0101000 _B :	30.0	1001000 _B :	46.0	1101000 _B :	62.0
		0001001 _B :	14.5 ⁻⁵	0101001 _B :	30.5	1001001 _B :	46.5	1101001 _B :	62.5
		0001010 _B :	15.0	0101010 _B :	31.0	1001010 _B :	47.0	1101010 _B :	63.0
		0001011 _B :	15.5	0101011 _B :	31.5	1001011 _B :	47.5	1101011 _B :	63.5
		0001100 _B :	16.0	0101100 _B :	32.0	1001100 _B :	48.0	1101100 _B :	64.0
		0001101 _B :	16.5	0101101 _B :	32.5	1001101 _B :	48.5	1101101 _B :	64.5
		0001110 _B :	17.0	0101110 _B :	33.0	1001110 _B :	49.0	1101110 _B :	65.0
		0001111 _B :	17.5	0101111 _B :	33.5	1001111 _B :	49.5	1101111 _B :	65.5
		0010000 _B :	18.0	0110000 _B :	34.0	1010000 _B : (default)	50.0	1110000 _B :	66.0
		0010001 _B :	18.5	0110001 _B :	34.5	1010001 _B :	50.5	1110001 _B :	66.5
		0010010 _B :	19.0	0110010 _B :	35.0	1010010 _B :	51.0	1110010 _B :	67.0
		0010011 _B :	19.5	0110011 _B :	35.5	1010011 _B :	51.5	1110011 _B :	67.5
		0010100 _B :	20.0	0110100 _B :	36.0	1010100 _B :	52.0	1110100 _B :	68.0
		0010101 _B :	20.5	0110101 _B :	36.5	1010101 _B :	52.5	1110101 _B :	68.5
		0010110 _B :	21.0	0110110 _B :	37.0	1010110 _B :	53.0	1110110 _B :	69.0
		0010111 _B :	21.5	0110111 _B :	37.5	1010111 _B :	53.5	1110111 _B :	69.5
		0011000 _B :	22.0	0111000 _B :	38.0	1011000 _B :	54.0	1111000 _B :	70.0
		0011001 _B :	22.5	0111001 _B :	38.5	1011001 _B :	54.5	1111001 _B :	70.5
		0011010 _B :	23.0	0111010 _B :	39.0	1011010 _B :	55.0	1111010 _B :	71.0
		0011011 _B :	23.5	0111011 _B :	39.5	1011011 _B :	55.5	1111011 _B :	71.5
		0011100 _B :	24.0	0111100 _B :	40.0	1011100 _B :	56.0	1111100 _B :	72.0
		0011101 _B :	24.5	0111101 _B :	40.5	1011101 _B :	56.5	1111101 _B :	72.5
		0011110 _B :	25.0	0111110 _B :	41.0	1011110 _B :	57.0	1111110 _B :	73.0
		0011111 _B :	25.5	0111111 _B :	41.5	1011111 _B :	57.5	1111111 _B :	73.5

NOTE 1 These values may be used for MR14 OP[6:0] to set the $V_{REF}(DQ[7:0])$ levels in the LPDDR5-SDRAM.

NOTE 2 The MR14 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different termination values.

NOTE 3 Absolute DQ[7:0] Vref low level (%code * VDDQ) must be higher than or equal to 75mV for normal operation. Vref error is not included this calculation.

NOTE 4 Absolute DQ[7:0] Vref high level (%code * VDDQ) must be lower than or equal to 350mV when WCK is less than or equal to 1600MHz. Absolute DQ[7:0] Vref high level (%code * VDDQ) must be lower than or equal to 225mV when WCK is higher than 1600MHz. V_{REF} error is not included this calculation.

1,2,3,4

6.2.1 Mode Register definition (Cont'd)

Table 70 — MR15 Register Information (MA[7:0] = 0F_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	$V_{REF}(DQ[15:8])$						

Table 71 — MR15 definition

Function	Register Type	Operand	Data	Notes
$V_{REF}(DQ[15:8])$ ($V_{REF}(DQ[15:8])$ Setting)	Read/ Write	OP[6:0]	0000000 _B : -- Thru -- 1111111 _B : See table below	1,2,3, 4,5,6

- NOTE 1 This register controls the $V_{REF}(DQ[15:8])$ levels for Frequency-Set-Point[2:0].
- NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[15:8]. Any RFU bits and unused DQ's shall be set to '0'. See 7.6.1 for more information on MRR Operation.
- NOTE 3 A write to OP[6:0] sets the internal $V_{REF}(DQ[15:8])$ level for FSP[0] when MR16 OP[1:0]=00_B, sets FSP[1] when MR16 OP[1:0]=01_B or sets FSP[2] when MR16 OP[1:0]=10_B. The time required for $V_{REF}(DQ[15:8])$ to reach the set level depends on the step size from the current level to the new level. See 4.1.1 for more information on $V_{REF}(DQ)$ training.
- NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
- NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- NOTE 6 MR15 MRR value is undefined when MR14 OP[7] is 1B. When MR14 OP[7] is 1_B, $V_{REF}(DQ[15:8])$ can be read from MR14.

6.2.1 Mode Register definition (Cont'd)

Table 72 — MR15 VREF(DQ[15:8]) Settings

Function	Operand	V _{REF} Values (% of V _{DDQ})								Notes
V _{REF} Settings for MR15	OP [6:0]	0000000 _B :	10.0 ⁻⁵	0100000 _B :	26.0	1000000 _B :	42.0	1100000 _B :	58.0	1,2,3,4
		0000001 _B :	10.5 ⁻⁵	0100001 _B :	26.5	1000001 _B :	42.5	1100001 _B :	58.5	
		0000010 _B :	11.0 ⁻⁵	0100010 _B :	27.0	1000010 _B :	43.0	1100010 _B :	59.0	
		0000011 _B :	11.5 ⁻⁵	0100011 _B :	27.5	1000011 _B :	43.5	1100011 _B :	59.5	
		0000100 _B :	12.0 ⁻⁵	0100100 _B :	28.0	1000100 _B :	44.0	1100100 _B :	60.0	
		0000101 _B :	12.5 ⁻⁵	0100101 _B :	28.5	1000101 _B :	44.5	1100101 _B :	60.5	
		0000110 _B :	13.0 ⁻⁵	0100110 _B :	29.0	1000110 _B :	45.0	1100110 _B :	61.0	
		0000111 _B :	13.5 ⁻⁵	0100111 _B :	29.5	1000111 _B :	45.5	1100111 _B :	61.5	
		0001000 _B :	14.0 ⁻⁵	0101000 _B :	30.0	1001000 _B :	46.0	1101000 _B :	62.0	
		0001001 _B :	14.5 ⁻⁵	0101001 _B :	30.5	1001001 _B :	46.5	1101001 _B :	62.5	
		0001010 _B :	15.0	0101010 _B :	31.0	1001010 _B :	47.0	1101010 _B :	63.0	
		0001011 _B :	15.5	0101011 _B :	31.5	1001011 _B :	47.5	1101011 _B :	63.5	
		0001100 _B :	16.0	0101100 _B :	32.0	1001100 _B :	48.0	1101100 _B :	64.0	
		0001101 _B :	16.5	0101101 _B :	32.5	1001101 _B :	48.5	1101101 _B :	64.5	
		0001110 _B :	17.0	0101110 _B :	33.0	1001110 _B :	49.0	1101110 _B :	65.0	
		0001111 _B :	17.5	0101111 _B :	33.5	1001111 _B :	49.5	1101111 _B :	65.5	
		0010000 _B :	18.0	0110000 _B :	34.0	1010000 _B : (default)	50.0	1110000 _B :	66.0	
		0010001 _B :	18.5	0110001 _B :	34.5	1010001 _B :	50.5	1110001 _B :	66.5	
		0010010 _B :	19.0	0110010 _B :	35.0	1010010 _B :	51.0	1110010 _B :	67.0	
		0010011 _B :	19.5	0110011 _B :	35.5	1010011 _B :	51.5	1110011 _B :	67.5	
		0010100 _B :	20.0	0110100 _B :	36.0	1010100 _B :	52.0	1110100 _B :	68.0	
		0010101 _B :	20.5	0110101 _B :	36.5	1010101 _B :	52.5	1110101 _B :	68.5	
		0010110 _B :	21.0	0110110 _B :	37.0	1010110 _B :	53.0	1110110 _B :	69.0	
		0010111 _B :	21.5	0110111 _B :	37.5	1010111 _B :	53.5	1110111 _B :	69.5	
		0011000 _B :	22.0	0111000 _B :	38.0	1011000 _B :	54.0	1111000 _B :	70.0	
		0011001 _B :	22.5	0111001 _B :	38.5	1011001 _B :	54.5	1111001 _B :	70.5	
		0011010 _B :	23.0	0111010 _B :	39.0	1011010 _B :	55.0	1111010 _B :	71.0	
		0011011 _B :	23.5	0111011 _B :	39.5	1011011 _B :	55.5	1111011 _B :	71.5	
		0011100 _B :	24.0	0111100 _B :	40.0	1011100 _B :	56.0	1111100 _B :	72.0	
		0011101 _B :	24.5	0111101 _B :	40.5	1011101 _B :	56.5	1111101 _B :	72.5	
		0011110 _B :	25.0	0111110 _B :	41.0	1011110 _B :	57.0	1111110 _B :	73.0	
		0011111 _B :	25.5	0111111 _B :	41.5	1011111 _B :	57.5	1111111 _B :	73.5	

NOTE 1 These values may be used for MR15 OP[6:0] to set the V_{REF}(DQ[15:8]) levels in the LPDDR5 SDRAM.

NOTE 2 The MR15 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different termination values.

NOTE 3 Absolute DQ[15:8] V_{REF} low level (%code * VDDQ) must be higher than or equal to 75mV for normal operation. V_{REF} error is not included in this calculation.

NOTE 4 Absolute DQ[15:8] V_{REF} high level (%code * VDDQ) must be lower than or equal to 350mV when WCK is less than or equal to 1600MHz. Absolute DQ[15:8] V_{REF} high level (%code * VDDQ) must be lower than or equal to 225mV when WCK is higher than 1600MHz. V_{REF} error is not included in this calculation.

NOTE 5 V_{REF} codes from 0000000_B to 0001001_B are able to be used only for testing purpose not for normal operation. V_{REF} accuracy are not guaranteed from 0000000_B to 0001001_B.

6.2.1 Mode Register definition (Cont'd)

Table 73 — MR16 Register Information (MA[5:0] = 10_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CBT-Phase	VRCG	CBT		FSP-OP		FSP-WR	

Table 74 — MR16 definition

Function	Register Type	Operand	Data	Notes
FSP-WR (Frequency Set Point Write Enable)	Write/ Read	OP[1:0]	00 _B : Frequency-Set-Point [0] (default) 01 _B : Frequency-Set-Point [1] 10 _B : Frequency-Set-Point [2] 11 _B : Reserved	1
FSP-OP (Frequency Set Point Operation Mode)		OP[3:2]	00 _B : Frequency-Set-Point [0] (default) 01 _B : Frequency-Set-Point [1] 10 _B : Frequency-Set-Point [2] 11 _B : Reserved	2
CBT (Command Bus Training)		OP[5:4]	00 _B : Normal Operation (default) 01 _B : Command Bus Training Mode Enabled FSP0 10 _B : Command Bus Training Mode Enabled FSP1 11 _B : Command Bus Training Mode Enabled FSP2	3
VRCG (VREF Current Generator)		OP[6]	0 _B : Normal Operation (default) 1 _B : VREF Fast Response (high current) mode	4
CBT-Phase		OP[7]	0 _B : DQ outputs CA pattern latched by CK rising edge (default) 1 _B : DQ outputs CA pattern latched by CK falling edge	
NOTE 1 FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V _{REF} (CA) Setting, V _{REF} (DQ) Setting. For more information, refer to 7.6.3, Frequency Set Point.				
NOTE 2 FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V _{REF} (CA) Setting, V _{REF} (DQ) Setting. For more information, refer to 7.6.3, Frequency Set Point.				
NOTE 3 A write to set OP[5:4]= 01 _B , 10 _B or 11 _B causes the LPDDR5-SDRAM to enter the Command Bus Training mode. When OP[5:4]= 01 _B , 10 _B or 11 _B , commands are ignored and the contents of CA[6:0] are mapped to the DQ bus. See the Command Bus Training (4.2.2) for more information.				
NOTE 4 When OP[6]=1 _B , the VREF circuit uses a high-current mode to improve VREF settling time.				

6.2.1 Mode Register definition (Cont'd)

Table 75 — MR17 Register Information (MA[5:0] = 11_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
x8ODTD Upper	x8ODTD Lower	ODTD-CA	RFU	ODTD-CK		SOC ODT	

Table 76 — MR17 definition

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000 _B : Disable (default) 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 111 _B : RFU	1,2,3,5
ODTD-CK (CK ODT termination)		OP[3]	0 _B : ODT-CK Enable 1 _B : ODT-CK Disable(default)	2,3,4
ODTD-CA (CA ODT termination)		OP[5]	0 _B : ODT-CA Enable 1 _B : ODT-CA Disable(default)	2,3,4
X8 ODTD Lower (CA/CLK ODT termination disable, Lower Byte select)		OP[6]	x8 per ch. only, Lower Byte selected Device 0 _B : ODT-CA/CLK follows MR17 OP[5], OP[3] & MR11 OP[6:4] (default) 1 _B : ODT-CA/CLK Disabled	
X8 ODTD Upper		OP[7]	x8 per ch. only, Upper Byte selected Device 0 _B : ODT-CA/CLK follows MR17 OP[5], OP[3] & MR11 OP[6:4] (default) 1 _B : ODT-CA/CLK Disabled	

NOTE 1 All values are "typical".

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 To ensure proper operation in a multi-rank configuration, when CA, CK ODT is enabled via MR11 OP[6:4] and also via MR17, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down and Idle Power-down.

NOTE 5 DRAM Pull-up driver strength is controlled by OP[2:0] SOC ODT setting when DQ termination is disabled.

6.2.1 Mode Register definition (Cont'd)

Table 77 — MR18 Register Information (MA[7:0] = 12_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CKR	WCK2CK Leveling	RFU	WCK ON	WCK_FM		WCK ODT	

Table 78 — MR18 Definition

Function	Register Type	Operand	Data	Notes
WCK ODT		OP[2:0]	000 _B : ODT disable (default) 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 110 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 111 _B : RFU	1,2,4
WCK FM (WCK Frequency Mode)	Write-only	OP[3]	0 _B : Low frequency mode (default) 1 _B : High frequency mode	1,2,5
WCK ON (WCK always ON mode)		OP[4]	0 _B : WCK Always On Mode disabled (Default) 1 _B : WCK Always On Mode enabled	1,2
WCK2CK Leveling		OP[6]	0 _B : WCK2CK Leveling Mode Disable (default) 1 _B : WCK2CK Leveling Mode Enable	
CKR (WCK to CK frequency ratio)		OP[7]	0 _B : 4:1 ratio 1 _B : 2:1 ratio (default)	1,2,3

NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the SDRAM, and may be changed without affecting SDRAM operation.

NOTE 3 CKR 2:1 can support up to 3200Mbps.

NOTE 4 The SDRAM will continue to terminate WCK in all states, if termination is enabled by MR18 OP[2:0].

NOTE 5 tWCK2DQ AC parameters can be changed by MR18 OP[3]. Refer to tWCK2DQ AC parameter table. WCK single-ended mode (MR20 OP[3:2]) can be allowed during Low frequency mode only.

6.2.1 Mode Register definition (Cont'd)

Table 79 — MR19 Register Information (MA[7:0] = 13_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DVFSQ		DVFSC	

Table 80 — MR19 Definition

Function	Register Type	Operand	Data	Notes
DVFSC (VDD2 Dynamic Voltage and Frequency Scaling Core)	Write-only	OP[1:0]	00 _B : High Speed mode (only VDD2H: 1.05V rail) (default) 01 _B : Low speed mode (use VDD2L: 0.9V rail) All others: reserved	1,2
DVFSQ (VDDQ Dynamic Voltage and Frequency Scaling VDDQ)		OP[3:2]	00 _B : VDDQ = 0.5V (default) 01 _B : VDDQ = 0.3V All others: reserved	1,2,3

NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 3 When DVFSQ OP[3:2] is 01_B, DRAM will turn off all ODT DQ, CS, CA, CK and WCK.

6.2.1 Mode Register definition (Cont'd)

Table 81 — MR20 Register Information (MA[7:0] = 14_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RDC DQ mode	RDC DMI mode	MRWDL	MRWDU		WCK mode		RDQS

Table 82 — MR20 definition

Function	Register Type	Operand	Data	Notes
RDQS (Read DQS)	Write-only	OP[1:0]	00 _B : RDQS_t and RDQS_c disabled 01 _B : RDQS_t enabled and RDQS_c disabled (default) 10 _B : RDQS_t and RDQS_c enabled 11 _B : RDQS_t disabled and RDQS_c enabled	1,2,3, 6,7,9
WCK mode		OP[3:2]	00 _B : differential (default) 01 _B : single-ended from WCK_t 10 _B : single-ended from WCK_c 11 _B : reserved	1,2,4, 5,8
MRWDL (Mode Register Write Disable Lower byte)		OP[4]	0 _B : Lower Byte MRW is enabled (default) 1 _B : Lower Byte MRW is disabled	10
MRWDU (Mode Register Write Disable Upper byte)		OP[5]	0 _B : Upper Byte MRW is enabled (default) 1 _B : Upper Byte MRW is disabled	10
RDC DMI mode		OP[6]	In Read DQ Calibration, DMI output pattern is controlled as: 0 _B : DMI pattern will be decided by MR33/34 (default) 1 _B : DMI pattern will be low-fixed	
RDC DQ mode		OP[7]	In Read DQ Calibration, DQ output pattern is controlled by MR33/34 (pattern) and MR31/32 (per-bit control), where, MR31/32 function is defined as: 0 _B : MR31/32 decides whether "invert" or not. (default) 1 _B : MR31/32 decides whether "low-fix" or not.	

NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 3 WCK clocking generates RDQS_t and RDQS_c.

NOTE 4 When MR20 OP[3:2]= 01_B, WCK_t is used as WCK timing, and WCK_c should be maintained at a valid logic level.

NOTE 5 When MR20 OP[3:2]= 10_B, WCK_c is used as WCK timing, and WCK_t should be maintained at a valid logic level

NOTE 6 When MR20 OP[1:0]= 01_B, RDQS_t is used as RDQS timing, and RDQS_c should be Hi-Z state.

NOTE 7 When MR20 OP[1:0]= 11_B, RDQS_c is used as RDQS timing, and RDQS_t should be Hi-Z state. NOTE 8 When MR20 OP[3:2]= 01_B, WCK_t polarity is the same as WCK_t in MR20 OP[3:2]=00_B, and when MR20 OP[3:2]= 10_B, WCK_c polarity is the same as WCK_c in MR20 OP[3:2]=00_B.

NOTE 9 When MR20 OP[1:0]= 01_B, RDQS_t polarity is the same as RDQS_t in MR20 OP[1:0]=10_B, and when MR20 OP[1:0]= 11_B, RDQS_c polarity is the same as RDQS_c in MR20 OP[1:0]=10_B.

NOTE 10 This MR setting is not valid to a standard X16 die.

6.2.1 Mode Register definition (Cont'd)

Table 83 — MR21 Register Information (MA[7:0] = 15_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	WXFE	RDCFE	WDCFE	RFU	WXFS	RDCFS	WDCFS

Table 84 — MR21 Definition

Function	Register Type	Operand	Data	Notes
WDCFS (WRITE Data Copy Function Support)	Read-only	OP[0]	0 _B : LPDDR5 WRITE data copy function not supported 1 _B : LPDDR5 WRITE data copy function supported	4
RDCFS (READ Data Copy Function Support)		OP[1]	0 _B : LPDDR5 READ data copy function not supported 1 _B : LPDDR5 READ data copy function supported	4
WXFS (Write X Function Support)		OP[2]	0 _B : LPDDR5 Write-X function not supported 1 _B : LPDDR5 Write-X function supported	4
WDCFE (WRITE Data Copy Function Enable)	Write-only	OP[4]	0 _B : LPDDR5 WRITE data copy function disable (default) 1 _B : LPDDR5 WRITE data copy function enable	1
RDCFE (READ Data Copy Function Enable)		OP[5]	0 _B : LPDDR5 READ data copy function disable (default) 1 _B : LPDDR5 READ data copy function enable	2
WXFE (Write X Function Enable)		OP[6]	0 _B : LPDDR5 write-X function disable (default) 1 _B : LPDDR5 write-X function enable	3

NOTE 1 MR21 OP[4] is "don't care" in case of MR21 OP[0]=0_B (LPDDR5 WRITE data copy function not supported).

NOTE 2 MR21 OP[5] is "don't care" in case of MR21 OP[1]=0_B (LPDDR5 READ data copy function not supported).

NOTE 3 MR21 OP[6] is "don't care" in case of MR21 OP[2]=0_B (LPDDR5 write-X function not supported).

NOTE 4 Data Copy function and Write X function are optional. Refer to the vendor's data sheet.

6.2.1 Mode Register definition (Cont'd)

Table 85 — MR22 Register Information (MA[7:0] = 16_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RECC	WECC					RFU	

Table 86 — MR22 Definition

Function	Register Type	Operand	Data	Notes
WECC (Write link ECC Control)	Write-only	OP[5:4]	00 _B : Write link ECC disable (default) 01 _B : Write link ECC enable 10 _B : Reserved 11 _B : Reserved	1,2
RECC (Read link ECC Control)		OP[7:6]	00 _B : Read link ECC disable (default) 01 _B : Read link ECC enable 10 _B : Reserved 11 _B : Reserved	1,2

NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 2 Refer to 7.7.7 for LPDDR5 link ECC descriptions.

Table 87 — MR23 Register Information (MA[5:0] = 17H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Table 88 — MR23 Definition

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write Only	[7:0]	0 _B : Segment Refresh Enable (default) 1 _B : Segment Refresh Disable	1,2

Table 89 — Row Address of Masked Segment for x16 Mode

Segment	OP[n]	Segment Mask	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R12:R10	R13:R11	R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	R16:R14	R16:R14
0	0	xxxxxx1					000 _B				
1	1	xxxxx1x					001 _B				
2	2	xxxx1xx					010 _B				
3	3	xxx1xxx					011 _B				
4	4	xx1xxxx					100 _B				
5	5	xx1xxxxx					101 _B				
6	6	x1xxxxx	110 _B	Not Allowed	110 _B						
7	7	1xxxxxx	111 _B		111 _B		111 _B		111 _B		111 _B

NOTE 1 This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.

NOTE 2 For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00_B).

Table 90 — Row Address of Masked Segment for x8 Mode

Segment	OP[n]	Segment Mask	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	R16:R14	R16:R14	R17:R15	R17:R15
0	0	xxxxxx1					000 _B				
1	1	xxxxx1x					001 _B				
2	2	xxxx1xx					010 _B				
3	3	xxx1xxx					011 _B				
4	4	xx1xxxx					100 _B				
5	5	xx1xxxxx					101 _B				
6	6	x1xxxxx	110 _B	Not Allowed	110 _B						
7	7	1xxxxxx	111 _B		111 _B		111 _B		111 _B		111 _B

NOTE 1 This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.

NOTE 2 For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00_B).

6.2.1 Mode Register definition (Cont'd)

Table 91 — MR24 Register Information (MA[5:0] = 18H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DFES	DFE Quantity for Upper Byte (DFEQU)				RFU	DFE Quantity for Lower Byte (DFEQL)	

Table 92 — MR24 Definition

Function	Register Type	Operand	Data	Notes
DFE Quantity for Lower Byte (DFEQL)	Write Only	OP[2:0]	000 _B : DFE disabled (default) 001 _B : Minimum negative feedback quantity ⋮ 011 _B : Maximum negative feedback quantity All Others: Reserved	1,2,3
DFE Quantity for Upper Byte (DFEQU)		OP[6:4]	000 _B : DFE disabled (default) 001 _B : Minimum negative feedback quantity ⋮ 011 _B : Maximum negative feedback quantity All Others: Reserved	1,2,3
DFE support (DFES)	Read Only	OP[7]	0 _B : DFE is not supported 1 _B : DFE is supported	

NOTE 1 DFE quantity is vendor specific. Please refer to each vendor specification.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

6.2.1 Mode Register definition (Cont'd)

Table 93 — MR25 Register Information (MA[7:0] = 19_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	PARC	CA Inputs TERM	CK Pair TERM				RFU

Table 94 — MR25 Definition

Function	Register Type	Operand	Data	Notes
CK Pair TERM (Other Shared dies' CK ODT Info)	Write-only	OP[4]	0 _B : All ranks sharing CK Pair are un-terminated (default) 1 _B : One of ranks sharing CK Pair are terminated	1,2
CA Inputs TERM (Other Shared dies' CA ODT Info)		OP[5]	0 _B : All ranks sharing CA Inputs are un-terminated (default) 1 _B : One of ranks sharing CA Inputs are terminated	1,2
PARC (Partial Array Refresh Control)		OP[6]	0 _B : PAAR disable (default) 1 _B : PAAR enable	3,4

NOTE 1 MR25 OP[5]/[4] is set to notify CA/CK ODT status of other shared dies.

NOTE 2 When CK and CA ODT status is different from each other (ex. CK termination, CA un-termination) and MR25 OP[5] is disabled, the un-terminated CA input buffer uses the fixed level reference voltage (TBD).

NOTE 3 MR23 PASR Segment Mask is applied to PAAR (Partial Array Auto Refresh) operation if PAAR enabled.

NOTE 4 Refer to 7.5.4 for LPDDR5 PASR descriptions.

Table 95 — MR26 Register Information (MA[7:0] = 1A_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DCMU1	DCMU0	DCML1	DCML0	DCM Flip	DCM Start/Stop

Table 96 — MR26 definition

Function	Register Type	Operand	Data	Notes
Duty cycle result for upper byte when DCM Flip=1 (DCMU1)	Read	OP[5]	0 _B : High duty cycle < 50% for upper byte 1 _B : High duty cycle > 50% for upper byte	
Duty cycle result for upper byte when DCM Flip=0 (DCMU0)		OP[4]	0 _B : High duty cycle < 50% for upper byte 1 _B : High duty cycle > 50% for upper byte	
Duty cycle result for lower byte when DCM Flip=1 (DCML1)		OP[3]	0 _B : High duty cycle < 50% for lower byte 1 _B : High duty cycle > 50% for lower byte	
Duty cycle result for lower byte when DCM Flip=0 (DCML0)		OP[2]	0 _B : High duty cycle < 50% for lower byte 1 _B : High duty cycle > 50% for lower byte	
Flip inputs to cancel offset(DCM_Flip)	Write	OP[1]	0 _B : No flip (default) 1 _B : Flip	
DCM_Start/Stop		OP[0]	0 _B : Stop (default) 1 _B : Start	

6.2.1 Mode Register definition (Cont'd)

Table 97 — MR27 Register Information (MA[7:0] = 1B_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TRR Mode	TRR Mode BAn			Unlimited		MAC Value	

Table 98 — MR27 Definition

Function	Register Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	000 _B : Unlimited when bit OP3=1 (Note 1, 4) 001 _B : TBD 010 _B : TBD 011 _B : TBD 100 _B : TBD 101 _B : TBD 110 _B : TBD 111 _B : TBD	
Unlimited MAC		OP[3]	0 _B : OP[2:0] define MAC value 1 _B : Unlimited MAC value (Note 1, 2, 4)	
TRR Mode BAn	Write-only	OP[6:4]	000 _B : Bank 0 001 _B : Bank 1 010 _B : Bank 2 011 _B : Bank 3 100 _B : Bank 4 101 _B : Bank 5 110 _B : Bank 6 111 _B : Bank 7	3
TRR Mode		OP[7]	0 _B : Disabled (default) 1 _B : Enabled	

NOTE 1 There is no restriction to number of activates.

NOTE 2 M27 OP [2:0] is set to zero.

NOTE 3 TRR mode uses 8Bank mode configuration and address mapping same as refresh operation.

NOTE 4 LPDDR5 devices which set MR27 OP[3]=1B (unlimited MAC) may not support TRR. Memory controller TRR support is not required for these devices.

6.2.1 Mode Register definition (Cont'd)

Table 99 — MR28 Register Information (MA[7:0] = 1C_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	ZQ Mode	RFU		ZQ Interval	ZQ Stop	ZQ Reset	

Table 100 — MR28 Definition

Function	Register Type	Operand	Data	Notes
ZQ Reset	Write-only	OP[0]	0 _B : Normal Operation (Default) 1 _B : ZQ Reset	1,2
ZQ Stop		OP[1]	0 _B : Normal Operation (Default) 1 _B : Background ZQ Calibration is halted after tZQSTOP	3,4
ZQ Interval		OP[3:2]	00 _B : Background Cal Interval ≤32ms 01 _B : Background Cal Interval ≤64ms (default) 10 _B : Background Cal Interval ≤128ms 11 _B : Background Cal Interval ≤256ms	5
ZQ Mode		OP[5]	0 _B : Background ZQ Calibration (Default) 1 _B : Command-Based ZQ Calibration	5

NOTE 1 See Table 22, ZQCal Timing Parameters for calibration latency and timing.

NOTE 2 Asserting ZQ Reset will set the calibration values to their default setting.

NOTE 3 When ZQ Stop is enabled, the ZQ resource is available for use by other devices. See 4.2.1.2, ZQ Stop Functionality.

NOTE 4 In Command-Based Calibration mode ZQCal Start commands are ignored when MR28 OP[1]=1_B.

NOTE 5 ZQ Interval and ZQ Mode MR settings are only applicable to ZQ Master die. These settings will be ignored by ZQ Slave die

6.2.1 Mode Register definition (Cont'd)

Table 101 — MR29 Register Information (MA[7:0] = 1DH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Resource Bank 7	PPR Resource Bank 6	PPR Resource Bank 5	PPR Resource Bank 4	PPR Resource Bank 3	PPR Resource Bank 2	PPR Resource Bank 1	PPR Resource Bank 0

Table 102 — MR29 Definition

Function	Register Type	Operand	Data	Notes
PPR Resource Bank 7	Read-only	OP[7]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 6		OP[6]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 5		OP[5]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 4		OP[4]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 3		OP[3]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 2		OP[2]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 1		OP[1]	0B: PPR Resource is not available 1B: PPR Resource is available	1
PPR Resource Bank 0		OP[0]	0B: PPR Resource is not available 1B: PPR Resource is available	1

NOTE 1 PPR Resources describe as follows:

PPR Resource	OP0 [Group 0]				OP1 [Group 1]				OP2 [Group 2]				OP3 [Group 3]			
4BK/4BG	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
16bank	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
8bank	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

6.2.1 Mode Register definition (Cont'd)

Table 103 — MR30 Register Information (MA[5:0] = 1E_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DCA for Upper Byte (DCAU)				DCA for Lower Byte (DCAL)			

Table 104 — MR30 Definition

Function	Register Type	Operand	Data	Notes
DCA for Lower Byte (DCAL)		OP[3:0]	0000 _B : 0 Steps (default no adjustment) 0001 _B : -1 Steps 0010 _B : -2 Steps 0011 _B : -3 Steps 0100 _B : -4 Steps 0101 _B : -5 Steps 0110 _B : -6 Steps 0111 _B : -7 Step 1000 _B : RFU 1001 _B : +1 Step 1010 _B : +2 Steps 1011 _B : +3 Steps 1100 _B : +4 Steps 1101 _B : +5 Steps 1110 _B : +6 Steps 1111 _B : +7 Steps	1,2,3,4,5
DCA for Upper Byte (DCAU)	Write-only	OP[7:4]	0000 _B : 0 Steps (default no adjustment) 0001 _B : -1 Steps 0010 _B : -2 Steps 0011 _B : -3 Steps 0100 _B : -4 Steps 0101 _B : -5 Steps 0110 _B : -6 Steps 0111 _B : -7 Step 1000 _B : RFU 1001 _B : +1 Step 1010 _B : +2 Steps 1011 _B : +3 Steps 1100 _B : +4 Steps 1101 _B : +5 Steps 1110 _B : +6 Steps 1111 _B : +7 Steps	1,2,3,4,5

NOTE 1 0001_B to 0111_B of bit sets will decrease the internal WCK duty cycle.

NOTE 2 1001_B to 1111_B of bit sets will increase the internal WCK duty cycle.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the SDRAM, and may be changed without affecting SDRAM operation.

NOTE 5. With byte mode device, OP[3:0] applies lower byte device and OP[7:4] applies upper byte device. Unused operands (OP[7:4] for lower byte device and OP[3:0] for upper byte device) should be set 0_B or 1_B by which are ignored SDRAM though.

6.2.1 Mode Register definition (Cont'd)

Table 105 — MR31 Register Information (MA[7:0] = 1F_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-byte per-bit control Register for DQ Calibration							

Table 106 — MR31 Definition

Function	Register Type	Operand	Data	Notes
Lower-byte per-bit control for DQ Calibration	Write-only	OP[7:0]	<p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane:</p> <p>In DQ inversion mode (MR20[7] = 0), 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR33 and MR34</p> <p>In DQ output fix0 mode (MR20[7] = 1), 0_B: Do not apply low-fix 1_B: Data pattern is low-fixed</p> <p>Default value for OP[7:0]=55_H</p>	1,2,3,4

NOTE 1 This register will invert or apply low-fix for the DQ Calibration pattern found in MR33 and MR34 for any single DQ, or any combination of DQ's.

Example: In case of DQ inversion mode, If MR31 OP[7:0]=00010101_B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.

In case of DQ output fix0 mode, If MR31 OP[7:0]=00010101_B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be low-fixed, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be low-fixed.

NOTE 2 DMI[0] is not inverted. DMI pattern is decided by MR33/34, where MR20[6] defines whether DMI output low-fix or not.

NOTE 3 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[7:6].

NOTE 4 In case of byte mode, MR31 is valid only for lower byte selected device.

Table 107 — MR31 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR31	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

6.2.1 Mode Register definition (Cont'd)

Table 108 — MR32 Register Information (MA[7:0] = 20_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper-byte per-bit control Register for DQ Calibration							

Table 109 — MR32 definition

Function	Register Type	Operand	Data	Notes
Upper-byte per-bit control for DQ Calibration	Write-only	OP[7:0]	<p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane:</p> <p>In DQ inversion mode (MR20[7] = 0), 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR33 and MR34</p> <p>In DQ output fix0 mode (MR20[7] = 1), 0_B: Do not apply low-fix 1_B: Data pattern is low-fixed</p> <p>Default value for OP[7:0] = 55_H</p>	1,2,3,4

NOTE 1 This register will invert or apply low-fix for the DQ Calibration pattern found in MR33 and MR34 for any single DQ, or any combination of DQ's.

Example: In case of DQ inversion mode, If MR32 OP[7:0]=00010101_B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.

In case of DQ output fix0 mode, If MR31 OP[7:0]=00010101_B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be low-fixed, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be low-fixed.

NOTE 2 DMI[1] is not inverted. DMI pattern is decided by MR33/34, where MR20[6] defines whether DMI output low-fix or not.

NOTE 3 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[7:6].

NOTE 4 In case of byte mode, MR32 is valid only for upper byte selected device.

Table 110 — MR32 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR32	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

6.2.1 Mode Register definition (Cont'd)

Table 111 — MR33 Register Information (MA[7:0] = 21_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "A"							

Table 112 — MR33 Definition

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR33 + MR34	Write-only	OP[7:0]	X _B : DQ Calibration Pattern A "5A _H " (default)	1,2,3,4

- NOTE 1 Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in this register followed by the contents of MR34. The pattern contained in MR33 is transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a tDC. The pattern is transmitted serially on each data lane, is organized as "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR33 is 27_H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 11100100_B.
A default pattern "5A_H" is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. The contents of MR31 and MR32 will invert the data pattern for a given DQ. See Table 106, for more information.
- NOTE 2 MR31 and MR32 may be used to invert the MR33/MR34 data patterns on the DQ pins. See Table 106 and Table 109 for more information. Data is never inverted on the DMI[1:0] pins.
- NOTE 3 The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6:5].
- NOTE 4 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6:5].

Table 113 — MR34 Register Information (MA[7:0] = 22_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B"							

Table 114 — MR34 Definition

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR33 + MR34	Write-only	OP[7:0]	X _B : DQ Calibration Pattern B "3C _H " (Default)	1,2,3,4

- NOTE 1 Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in MR33 and followed by the contents of this register. The pattern contained in MR34 is concatenated to the end of MR33 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a DRC. The pattern is transmitted serially on each data lane, organized "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR33 is 27_H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 111100100_B.
A default pattern "3C_H" is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. See MR33 for more information.
- NOTE 2 MR31 and MR32 may be used to invert the MR33/MR34 data patterns on the DQ pins. See MR31 and MR32 for more information. Data is never inverted on the DMI[1:0] pins.
- NOTE 3 The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6:5].
- NOTE 4 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

6.2.1 Mode Register definition (Cont'd)

Table 115 — MR35 Register Information (MA[7:0] = 23_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQI Oscillator Count - LSB							

Table 116 — MR35 Definition

Function	Register Type	Operand	Data	Notes
WCK2DQI Oscillator (DQ input Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM WCK2DQI Oscillator Count	1,2,3,4

NOTE 1 MR35 reports the LSB bits of the DRAM WCK2DQI Oscillator count. The DRAM WCK2DQI Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.

NOTE 2 Both MR35 and MR36 must be read (MRR) and combined to get the value of the WCK2DQI Oscillator count.

NOTE 3 A new MPC [Start WCK2DQI Oscillator] could be issued to reset the contents of MR35/MR36.

NOTE 4 WCKDQI & WCKDQO cannot be operated simultaneously.

Table 117 — MR36 Register Information (MA[7:0] = 24_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQI Oscillator Count - MSB							

Table 118 — MR36 Definition

Function	Register Type	Operand	Data	Notes
WCK2DQI Oscillator (DQ input Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 MSB DRAM WCK2DQI Oscillator Count	1,2,3,4

NOTE 1 MR36 reports the MSB bits of the DRAM WCK2DQI Oscillator count. The DRAM WCK2DQI Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.

NOTE 2 Both MR35 and MR36 must be read (MRR) and combined to get the value of the WCK2DQI Oscillator count.

NOTE 3 A new MPC [Start WCK2DQI Oscillator] could be issued to reset the contents of MR35/MR36.

NOTE 4 WCKDQI & WCKDQO cannot be operated simultaneously.

6.2.1 Mode Register definition (Cont'd)

Table 119 — MR37 Register Information (MA[7:0] = 25_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQI interval timer run time setting							

Table 120 — MR37 Definition

Function	Register Type	Operand	Data	Notes
WCK2DQI interval timer run time	Write-only	OP[7:0]	<p>00000000_B: WCK2DQI interval timer stop via MPC Command (Default)</p> <p>00000001_B: WCK2DQI timer stops automatically at 16th clocks after timer start</p> <p>00000010_B: WCK2DQI timer stops automatically at 32nd clocks after timer start</p> <p>00000011_B: WCK2DQI timer stops automatically at 48th clocks after timer start</p> <p>00000100_B: WCK2DQI timer stops automatically at 64th clocks after timer start</p> <p>----- Thru -----</p> <p>00111111_B: WCK2DQI timer stops automatically at (63X16)th clocks after timer start</p> <p>01XXXXXX_B: WCK2DQI timer stops automatically at 2048th clocks after timer start</p> <p>10XXXXXX_B: WCK2DQI timer stops automatically at 4096th clocks after timer start</p> <p>11XXXXXX_B: WCK2DQI timer stops automatically at 8192nd clocks after timer start</p>	1,2

NOTE 1 MPC command with OP[6:0]=TBDB (Stop WCK2DQI Interval Oscillator) stops WCK2DQI interval timer in case of MR37 OP[7:0] = 00000000_B.

NOTE 2 MPC command with OP[6:0]=TBD (Stop WCK2DQI Interval Oscillator) is illegal with non-zero values in MR37 OP[7:0].

6.2.1 Mode Register definition (Cont'd)

Table 121 — MR38 Register Information (MA[7:0] = 26_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQO Oscillator Count - LSB							

Table 122 — MR38 Definition

Function	Register Type	Operand	Data	Notes
WCK2DQO Oscillator (DQ output Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM WCK2DQO Oscillator Count	1,2,3

NOTE 1 MR38 reports the LSB bits of the DRAM WCK2DQO Oscillator count. The DRAM WCK2DQO Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.

NOTE 2 Both MR38 and MR39 must be read (MRR) and combined to get the value of the WCK2DQO Oscillator count.

NOTE 3 A new MPC [Start WCK2DQO Oscillator] can be issued at any time before sending MPC [Stop WCK2DQO Oscillator]. A new MPC [Start WCK2DQO Oscillator] resets the contents of MR38/MR39.

Table 123 — MR39 Register Information (MA[7:0] = 27_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQO Oscillator Count - MSB							

Table 124 — MR39 Definition

Function	Register Type	Operand	Data	Notes
WCK2DQO Oscillator (DQ output Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 MSB DRAM WCK2DQO Oscillator Count	1,2,3

NOTE 1 MR39 reports the MSB bits of the DRAM WCK2DQO Oscillator count. The DRAM WCK2DQO Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.

NOTE 2 Both MR38 and MR39 must be read (MRR) and combined to get the value of the WCK2DQO Oscillator count.

NOTE 3 A new MPC [Start WCK2DQO Oscillator] can be issued at any time before sending MPC [Stop WCK2DQO Oscillator]. A new MPC [Start WCK2DQO Oscillator] resets the contents of MR38/MR39.

6.2.1 Mode Register definition (Cont'd)

Table 125 — MR40 Register Information (MA[7:0] = 28_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQO interval timer run time setting							

Table 126 — MR40 Definition

Function	Register Type	Operand	Data	Notes
WCK2DQO interval timer run time	Write-only	OP[7:0]	00000000 _B : WCK2DQO interval timer stop via MPC Command (Default) 00000001 _B : WCK2DQO timer stops automatically at 16th clocks after timer start 00000010 _B : WCK2DQO timer stops automatically at 32nd clocks after timer start 00000011 _B : WCK2DQO timer stops automatically at 48th clocks after timer start 00000100 _B : WCK2DQO timer stops automatically at 64th clocks after timer start ----- Thru ----- 00111111 _B : WCK2DQO timer stops automatically at (63X16)th clocks after timer start 01XXXXXX _B : WCK2DQO timer stops automatically at 2048th clocks after timer start 10XXXXXX _B : WCK2DQO timer stops automatically at 4096th clocks after timer start 11XXXXXX _B : WCK2DQO timer stops automatically at 8192nd clocks after timer start	1, 2

NOTE 1 MPC command with OP[7:0]=10000100_B (Stop WCK2DQO Interval Oscillator) stops WCK2DQO interval timer in case of MR40 OP[7:0] = 00000000_B.

NOTE 2 MPC command with OP[7:0]=10000100_B (Stop WCK2DQO Interval Oscillator) is illegal with non-zero values in MR40 OP[7:0].

6.2.1 Mode Register definition (Cont'd)

Table 127 — MR41 Register Information (MA[7:0] = 29_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
NT DQ ODT		PPRE		RFU			

Function	Register Type	Operand	Data	Notes
NT DQ ODT (Non-Target DQ Bus Receiver On-Die-Termination)	Write-only	OP[7:5]	000 _B : Disable 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 (default) 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 111 _B : RFU	1,2,3
			OP[4] 0 _B : PPR Disable (default) 1 _B : PPR Enable	

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 128 — MR42 Register Information (MA[7:0] = 2A_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Key Protection							

Table 129 — MR42 definition

Function	Register Type	Operand	Data	Notes
PPR Key Protection	Write-only	OP[7:0]	PPR Key Protection code	1,2

NOTE 1 PPR protection code is vendor specific. Please refer vendor data sheet.

NOTE 2 PPR entry and exit sequence details are described in 7.7.4, Post Package Repair.

6.2.1 Mode Register definition (Cont'd)

Table 130 — MR43 Register Information ($MA[7:0] = 2B_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBE_flag	SBE_count						

Table 131 — MR43 definition

Function	Register Type	Operand	Data	Notes
DBE_flag	Read-only	OP[7]	0 _B : No double-bit errors have occurred on the DRAM interface 1 _B : One or more double-bit errors have occurred on the DRAM interface	1,2,4,6
SBE_count		OP[6:0]	The number of times a single-bit error or errors have occurred on the DRAM interface	1,2,3,4,5

- NOTE 1 These bits are cleared on power-up, DRAM reset, any Power-Down Exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4]=00b (Link ECC disabled). Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be tMRR + tMRW (rather than simply tMRR as required on most registers).
- NOTE 2 The DRAM should disable detection & recording of ECC errors during Write-FIFO commands, as these are used for training purposes and some errors are expected during training.
- NOTE 3 In a x16 DRAM device, up to 4 single-bit errors could potentially be detected in a single BL16 burst (byte 0 data SBE, byte 0 DMI SBE, byte 1 data SBE, and byte 1 DMI SBE). Any combination of these 4 simultaneous errors is considered a single SBE occurrence, and would only increment the SBE_count by 1. A BL32 burst can have up to 2 such SBE occurrences, and could increment the SBE_count by up to 2. In a x8 DRAM device, any simultaneous combination of data SBE and DMI SBE is considered a single SBE occurrence, and would only increment the SBE_count by 1 (up to 2 in a BL32 burst).
- NOTE 4 In x16 mode, errors from either interface byte are stored in a single register per DRAM (SBE_count would be the number of SBE occurrences on BOTH bytes & DBE_flag would indicate a DBE on EITHER byte). In x8 mode, errors are stored for a single interface byte and MRR returns both copies of this register, each on its corresponding byte lane.
- NOTE 5 SBE_count should be a saturating counter.
- NOTE 6 Once set, the DBE_flag bit remains set until explicitly cleared by one of the conditions described in note 1 above.

6.2.1 Mode Register definition (Cont'd)

Table 132 — MR44 Register Information (MA[7:0] = 2C_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Data ECC Syndrome [7:0]							
S[7]	S[6]	S[5]	S[4]	S[3]	S[2]	S[1]	S[0]

Table 133 — MR44 definition

Function	Register Type	Operand	Data	Notes
Data ECC Syndrome [7:0]	Read-only	OP[7:0]	Bits 7:0 of the data ECC syndrome from the most recent single-bit error	1,2,3,4,5

- NOTE 1 These bits are cleared on power-up, DRAM reset, any Power-Down Exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4]=00_B (Link ECC disabled). Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be tMRR + tMRW (rather than simply tMRR as required on most registers).
- NOTE 2 The DRAM should disable detection & recording of ECC errors during Write-FIFO commands, as these are used for training purposes and some errors are expected during training.
- NOTE 3 In x16 mode, error syndromes from either interface byte are stored in a single register per DRAM. In x8 mode, error syndromes are stored for a single interface byte and MRR returns both copies of this register, each on its corresponding byte lane.
- NOTE 4 In x16 mode, it is possible for errors to occur on both bytes simultaneously. In this rare case, only the syndrome from DQ[7:0] should be stored.
- NOTE 5 Regardless of detecting a data ECC error or a DMI ECC error, both syndromes should be stored at either error occurrence.

6.2.1 Mode Register definition (Cont'd)

Table 134 — MR45 Register Information (MA[7:0] = 2D_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Data ECC Syndrome [8]	Error Byte Lane	DMI ECC Syndrome					
S[8]	Error Byte Lane	DS[5]	DS[4]	DS[3]	DS[2]	DS[1]	DS[0]

Table 135 — MR45 definition

Function	Register Type	Operand	Data	Notes
Data ECC Syndrome[8] (S[8])	Read-only	OP[7]	Bit 8 of the data ECC syndrome from the most recent single-bit error	1,2,3,4,5
Error Byte Lane		OP[6]	0 _B : ECC error occurred on DQ[7:0] or DMI0 1 _B : ECC error occurred on DQ[15:8] or DMI1	1,2,3,4,5,6
DMI ECC Syndrome (DS[5:0])		OP[5:0]	The DMI ECC syndrome from the most recent single-bit error	1,2,3,4,5
<p>NOTE 1 These bits are cleared on power-up, DRAM reset, any Power-Down Exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4]=00b (Link ECC disabled). Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be tMRR + tMRW (rather than simply tMRR as required on most registers).</p> <p>NOTE 2 The DRAM should disable detection & recording of ECC errors during Write-FIFO commands, as these are used for training purposes and some errors are expected during training.</p> <p>NOTE 3 In x16 mode, error syndromes from either interface byte are stored in a single register per DRAM. In x8 mode, error syndromes are stored for a single interface byte and MRR returns both copies of this register, each on its corresponding byte lane.</p> <p>NOTE 4 In x16 mode, it is possible for errors to occur on both bytes simultaneously. In this rare case, only the error syndromes from byte 0 (DQ[7:0] & DMI0) should be stored, regardless of the error types on the two bytes.</p> <p>NOTE 5 Regardless of detecting a data ECC error or a DMI ECC error, both syndromes should be stored at either error occurrence.</p> <p>NOTE 6 In x8 mode, this bit is unused and shall always read back as 0.</p>				

Table 136 — MR46 Register Information (MA[5:0] = 2E_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				FIFO RDQS Training	RDQS Toggle	Enhanced RDQS	

Table 137 — MR46 definition

Function	Register Type	Operand	Data	Notes
Enhanced RDQS (Enhanced RDQS training mode)	Write-only	OP[0]	0 _B : Disabled (default) 1 _B : Enhanced RDQS training mode Enabled	
RDQS Toggle (RDQS toggle mode)		OP[1]	0 _B : Disabled (default) 1 _B : RDQS toggle mode Enabled	
FIFO RDQS Training (WCK-RDQS_t/Parity Training)		OP[2]	0 _B : Disabled (default) 1 _B : WCK-RDQS_t/Parity Training Enabled	1
<p>NOTE 1 When MR46 OP[3] = 1_B, Write FIFO command will allow data to be written through the RDQS_t pin. The data written via the RDQS_t pin can then be read back via the DMI by a Read FIFO command.</p>				

6.2.1 Mode Register definition (Cont'd)

Table 138 — MR47 Register Information (MA[7:0] = 2F_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-1							

Table 139 — MR47 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-1	Read Only	OP[7:0]	Serial ID-1	1

NOTE 1 MR47 is vendor specific.

Table 140 — MR48 Register Information (MA[7:0] = 30_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-2							

Table 141 — MR48 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-2	Read Only	OP[7:0]	Serial ID-2	1

NOTE 1 MR48 is vendor specific.

Table 142 — MR49 Register Information (MA[7:0] = 31_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-3							

Table 143 — MR49 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-3	Read Only	OP[7:0]	Serial ID-3	1

NOTE 1 MR49 is vendor specific.

Table 144 — MR50 Register Information (MA[7:0] = 32_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-4							

Table 145 — MR50 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-4	Read Only	OP[7:0]	Serial ID-4	1

NOTE 1 MR50 is vendor specific.

Table 146 — MR51 Register Information (MA[7:0] = 33_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-5							

Table 147 — MR51 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-5	Read Only	OP[7:0]	Serial ID-5	1

NOTE 1 MR51 is vendor specific.

6.2.1 Mode Register definition (Cont'd)

Table 148 — MR52 Register Information (MA[7:0] = 34_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-6							

Table 149 — MR52 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-6	Read Only	OP[7:0]	Serial ID-6	1

NOTE 1 MR52 is vendor specific.

Table 150 — MR53 Register Information (MA[7:0] = 35_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-7							

Table 151 — MR53 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-7	Read Only	OP[7:0]	Serial ID-7	1

NOTE 1 MR53 is vendor specific.

Table 152 — MR54 Register Information (MA[7:0] = 36H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-8							

Table 153 — MR54 Definition

Function	Register Type	Operand	Data	Notes
LPDDR5 Serial ID-8	Read Only	OP[7:0]	Serial ID-8	1

NOTE 1 MR54 is vendor specific.

7 **Operating**

7.1 Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR5 device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

7.1.1 Command Truth Table

Table 154 — Command Truth Table

7.1.1 Command Truth Table (Cont'd)

Table 154 — Command Truth Table (cont'd)

SDRAM COMMAND	BK ORG (BG, 16B, 8B)	SDR CMD PIN	DDR COMMAND PINS								CK_t edge	Notes
			CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6		
READ32 (RD32)	BG/16B	H	H	L	H	C0	C3	C4	C5	 R1	1, 2, 3, 6, 7, 10, 11	
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	 F1		
	16B		BA0	BA1	BA2	BA3		V	B3			
CAS	Any	H	L	L	H	H	WS_WR	WS_RD	WS_FS	 R1	1, 2, 7, 13	
		X	DC0	DC1	DC2	DC3	WRX	 F1				
MULTI PURPOSE COMMAND (MPC)	Any	H	L	L	L	L	H	H	OP7	 R1	1, 2	
		X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	 F1		
SELF REFRESH ENTRY (SRE)	Any	H	L	L	L	H	L	H	H	 R1	1, 2, 9	
		X	V	V	V	V	V	DSM	PD	 F1		
SELF REFRESH EXIT (SRX)	Any	H	L	L	L	H	L	H	L	 R1	1, 2	
		X	V	V	V	V	V	V	V	 F1		
MODE REGISTER WRITE-1 (MRW-1)	Any	H	L	L	L	H	H	L	H	 R1	1, 2	
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	 F1		
MODE REGISTER WRITE-2 (MRW-2)	Any	H	L	L	L	H	L	L	OP7	 R1	1, 2	
		X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	 F1		
MODE REGISTER READ (MRR)	Any	H	L	L	L	H	H	L	L	 R1	1, 2	
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	 F1		
WRITE FIFO (WFF)	Any	H	L	L	L	L	L	H	H	 R1	1, 2	
		X	L	L	L	L	L	L	L	 F1		
READ FIFO (RFF)	Any	H	L	L	L	L	L	H	L	 R1	1, 2	
		X	L	L	L	L	L	L	L	 F1		
READ DQ CALIBRATION (RDC)	Any	H	L	L	L	L	H	L	H	 R1	1, 2	
		X	L	L	L	L	L	L	L	 F1		

NOTE 1 LPDDR5 commands are one clock cycles long and defined by the states of CS at the rising edge (R1) of clock and CA[6:0] at the rising edge (R1) and the falling edge (F1) of clock. Note that some operations such as ACTIVATE, MODE REGISTER WRITE or WCK2CK SYNC (WS_RD, WS_WR, WS_FS) require two commands to initiate.

NOTE 2 "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CK_t, CK_c and CA[6:0] can be floated.

NOTE 3 Bank Group Address BG[1:0] and Bank Address BA[1:0] determine which bank is to be operated upon.

NOTE 4 An ACTIVATE-1 command must be followed by an ACTIVATE-2 command. Only CAS, WRITE, MASK WRITE, READ, PRECHARGE (to a different bank) commands can be issued between ACTIVATE-1 and ACTIVATE-2 commands. The maximum timing gap between ACTIVATE-1 and ACTIVATE-2 commands are 8 clock cycles. An ACTIVATE-1 command must be issued first before issuing an ACTIVATE-2 command. Once an ACTIVATE-1 command is issued, an ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.

NOTE 5 AB "HIGH" during PRECHARGE or REFRESH command indicates that command must be applied to all banks and bank address is a don't care.

NOTE 6 AP "HIGH" during WRITE, MASK WRITE or READ commands indicates that an auto-precharge will occur to the bank associated with the WRITE, MASK WRITE or READ command.

7.1.1 Command Truth Table (Cont'd)

Table 154 — Command Truth Table (cont'd)

NOTE 7 CAS command is only required for WRITE, MASK WRITE or READ operation if optional low power features (DC0-3 and/or WRX) of these commands are required or if Burst Start Address (B3) is non-zero to READ or if WCK2CK SYNC (WS_RD, WS_WR) or FAST SYNC (WS_FS) is applied to a target device. CAS operands (DC0-3, WRX and B3) are valid to immediately following WRITE or READ only. In case of CAS-FAST_SYNC(WS_FS="H" AND WS_WR="L" AND WS_RD="L") or CAS-SYNC_OFF (WS_FS="H" AND WS_WR="H" AND WS_RD="H"), other CAS operands (DC0-3, WRX, B3) shall be "LOW". Valid DC0-3 or WRX operand(s) may be issued together with WCK2CK SYNC (WS_WR="H", WS_RD="L", WS_FS="L"). Valid B3 operand may be issued together with WCK2CK SYNC (WS_RD="H", WS_WR="L", WS_FS="L"). Refer to

Table 155.

NOTE 8 WRITE32 (WRITE with BL32) command is valid in a BG/16B mode only. WRITE command is WR in an 8B mode and WR16 in a BG/16B mode.

NOTE 9 PD "HIGH" during SELF REFRESH ENTRY command indicates that both Self Refresh Entry and Power Down Entry will occur together. DSM "HIGH" during SELF REFRESH ENTRY command indicates that both Self Refresh Entry and Deep Sleep Mode Entry will occur together. Both PD "HIGH" and DSM "HIGH" are illegal.

NOTE 10 READ command includes Read Burst Start Address (B3, B4) associated with Burst Length setting, B3 for BL16 in a BG/16B mode, or B3, C0 for BL32 in a BG/16B mode, or B3, B4 for BL32 in an 8B mode. Refer to 2.2.6 for the Burst Sequence Tables.

NOTE 11 READ32 (READ with BL32) command is valid in a BG/16B mode only. READ command is RD in an 8B mode and RD16 in a BG/16B mode.

NOTE 12 CS shall be compliant to Power Down Entry/Exit timing requirements. Refer to 7.5.6 for more information on Power Down Function and Timing Description.

NOTE 13 Refer to 7.7.2, LPDDR5 low power function description and Data Copy function (DC0-DC3), and 7.7.3, Write X function (WRX).

Table 155 — Allowable CAS command operand(s) combination

Operation Mode	CAS Command Operand(s)					
	WS_WR	WS_RD	WS_FS	DC0-3	WRX	B3
WCK2CK SYNC (WR)	H	L	L	LLLL	L	L
WCK2CK SYNC (WR) + Write Data Copy	H	L	L	VVVV	L	L
WCK2CK SYNC (WR) + Write X	H	L	L	LLLL	H	L
WCK2CK SYNC (RD)	L	H	L	LLLL	L	V
WCK2CK FAST SYNC	L	L	H	LLLL	L	L
WCK2CK SYNC OFF	H	H	H	LLLL	L	L
Write Data Copy	L	L	L	VVVV	L	L
Write X	L	L	L	LLLL	H	L
Non-Zero Burst Start Address for RD	L	L	L	LLLL	L	H
Illegal	Other Operands Combination					

NOTE 1 "V" means "H" or "L" (a defined logic level).

7.2 WCK Operation

7.2.1 WCK2CK Synchronization operation

7.2.1.1 WCK2CK Synchronization

An LPDDR5 SDRAM utilizes two types of clock with different frequencies. The frequency of WCK is four times or twice higher than the command clock, requiring an LPDDR5 SDRAM to have clock divider in the WCK clock tree. By dividing the WCK, the operation speed of DRAM internal circuits in WCK domain is reduced to half. However, the WCK divider initial state is unpredictable and results in two different states in an LPDDR5 SDRAM: aligned with CK state and miss-aligned with CK state. **Figure 55** illustrates these two cases.

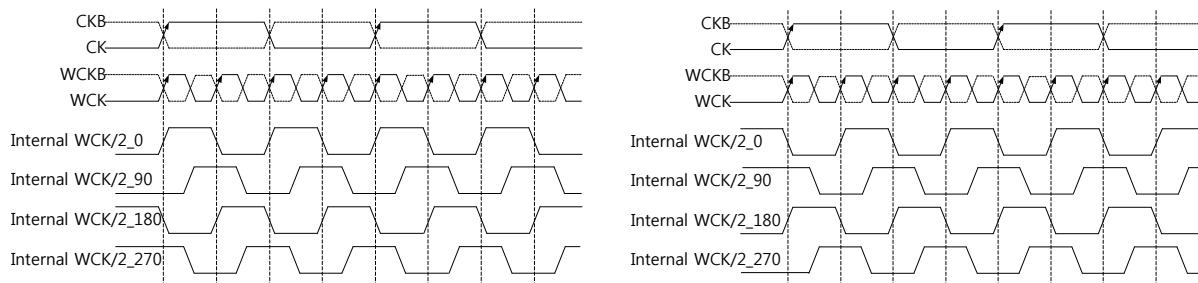


Figure 55 — Aligned WCK/2_0 to CK (Left) & Miss-Aligned WCK/2_0 to CK (Right)

The latency control unit inside the SDRAM performs clock domain change of WRITE or READ commands from CK domain to WCK domain. For error-free latency control, the latency control circuit must know whether the SDRAM is in aligned with CK state or miss-aligned with CK state. An LPDDR5 SDRAM is able to reset or detect its state by a process called WCK2CK Synchronization. When a SDRAM controller issues CAS command with the bit of WCK2CK Synchronization, the controller provides the SDRAM with half frequency WCK pulse to relax ISI and the timing margin. This operation is defined as WCK2CK Synchronization. At the timing when the SDRAM performs WCK2CK Sync operation, the SDRAM controller must provide the SDRAM with half frequency WCK pulse to relax WCK2CK Sync timing margin.

7.2.1.2 CAS Command with WCK2CK Synchronization Bits

The LPDDR5 WCK2CK Synchronization process is initiated by a CAS command with the related bit enabled. The CAS command with WCK2CK Synchronization should be issued before the write or READ command. Table 156 shows the CAS command with WCK2CK Synchronization bit (WS_WR, WS_RD, WS_FAST). CAS command with “1” at WCK2CK Synchronization flag bit informs DRAM WCK2CK Synchronization is required.

Table 156 — CAS command with WCK2CK Synchronization bits

Command	SDR Command Pin	DDR Command Pins								
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CK_t edge
CAS	H	L	L	H	H	WS_WR	WS_RD	WS_FS	R1	
	X	DC0	DC1	DC2	DC3	WRX	V	B3	F1	

7.2.1.2 CAS Command with WCK2CK Synchronization Bits (Cont'd)

Figure 56 shows the LPDDR5 WCK2CK Sync operation by CAS command with WCK2CK Sync operand enabled (WS_WR or WS_RD or WS_FAST = 1). DRAM controller must start to drive WCK as WCK_t/WCK_c=L/H after tWCKENL. The WCK2CK Sync operation occurs after tWCKENL+tWCKPRE_static followed by half-rate WCK during 1tCK. Before the WCK2CK Sync, WCK must toggle once to reduce the channel ISI in WCK. WCK2CK Training must be performed prior to WCK2CK Synchronization. The DRAM requires the proper WCK toggle pattern prior to insure WCK2CK sync properly. After the WCK2CK Sync is completed, the WCK must continue to toggle until the end of the read or write bursts are completed.

CAS(WS_WR=1) should be followed by WRITE command immediately. CAS(WS_RD=1) should also be followed by READ command immediately. CAS(WS_FAST=1) is only used as a standalone command and can be simultaneously issued to multi-ranks. Refer to 8.1.2, CAS command timing constraints. After Synchronization, the DRAM controller must keep WCK toggling until DQ bursts of READ or WRITE are completed or CAS(WCK Buffer off) command is issued. For Example, After PDX(Power Down Exit), CAS command with WCK2CK Sync operand enabled (WS_WR or WS_RD or WS_FAST=1) must be issued before the WRITE command or READ command. Because during Power Down, WCK2CK sync state is lost.

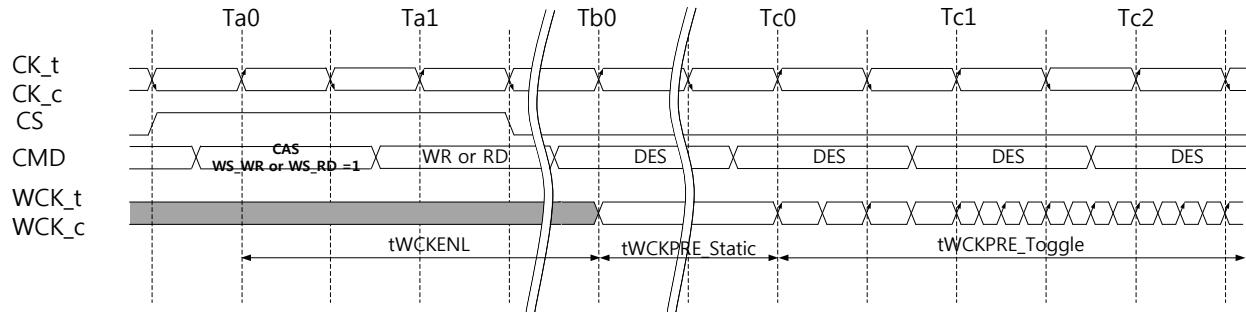


Figure 56 — LPDDR5 WCK2CK Sync operation by CAS command with WCK2CK Sync operand enabled

7.2.1.3 WCK2CK Sync operation followed by a WRITE command

When there is no on-going DQ burst, the DRAM controller turns off WCK drivers to enter Hi-Z state to remove current through WCK ODT (on-die termination) and an LPDDR5 SDRAM also turns off its WCK buffers. Turning off DRAM controller WCK driver or DRAM WCK buffer puts the LPDDR5 DRAM WCK divider into an unknown state, requiring a new WCK2CK Sync sequence before starting DQ operation (or WCK operation for READ/ WRITE/ Training). Therefore, the DRAM controller must track the WCK2CK Sync state of each DRAM, and issue CAS WCK2CK Sync command according to the WCK2CK Sync state before requesting DQ operation (or WCK operation) for READ/ WRITE/ Training operation.

A WCK2CK Sync immediately followed by WRITE operation is shown in Figure 57. The CAS WCK2CK Sync command will have WS_WR=1 when it is followed by WRITE command. No command is allowed between CAS(WS_WR=1) command and WRITE command, and CAS(WS_WR=1) command should be immediately followed by WRITE command. tWCKENL_WR is the delay required by an LPDDR5 DRAM to prepare for WCK2CK Sync operation after the CAS command with WS_WR=1.

7.2.1.3 WCK2CK Sync operation followed by a WRITE command (Cont'd)

At Td0 in Figure 57, tWCKENL_WR+tWCKPRE_Static+tWCKPRE_Toggle_WR from the WCK2CK Sync is satisfied and the memory controller starts the WRITE DQ burst. The WRITE DQ burst is completed and after tWCKPST, the memory controller may stop WCK toggle and put the WCK drivers into hi-Z state and WCK buffers can be also turned off for power saving.

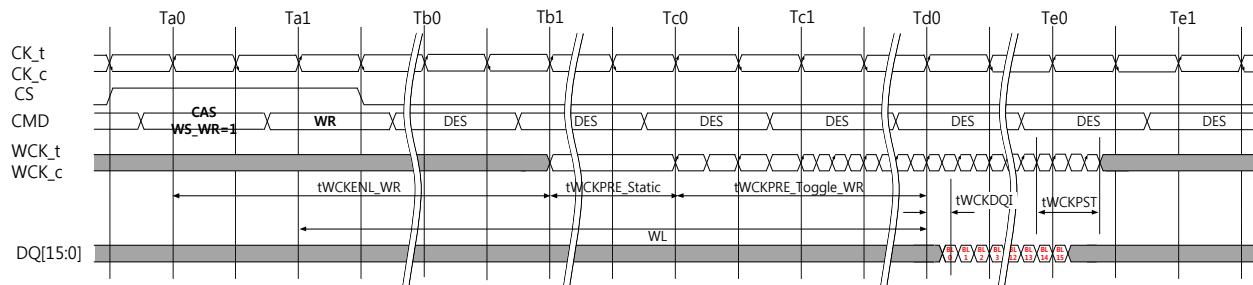


Figure 57 — WCK2CK Sync operation followed by a WRITE command

Table 157 — WCK2CK Sync AC Parameters for WRITE operation

WCK:CK Ratio	Data Rate [Mbps]		CK Frequency [Mbps]		WL(SetA) [nCK]	WL(SetB) [nCK]	tWCKENL_WR(SetA) [nCK]	tWCKENL_WR(SetB) [nCK]	tWCKPRE_Static [nCK]	tWCKPRE_toggle_WR [nCK]	tWCKPRE_total_WR [nCK]
	Lower Limit(>)	Upper Limit(<=)	Lower Limit(>)	Upper Limit(<=)							
2:1	40	533	10	133	4	4	1	1	1	3	4
	533	1067	133	267	4	6	0	2	2	3	5
	1067	1600	267	400	6	8	1	3	2	4	6
	1600	2133	400	533	8	10	2	4	3	4	7
	2133	2750	533	688	8	14	1	7	4	4	8
	2750	3200	688	800	10	16	3	9	4	4	8
4:1	40	533	5	67	2	2	0	0	1	2	3
	533	1067	67	133	2	3	0	1	1	2	3
	1067	1600	133	200	3	4	1	2	1	2	3
	1600	2133	200	267	4	5	1	2	2	2	4
	2133	2750	267	344	4	7	1	4	2	2	4
	2750	3200	344	400	5	8	2	5	2	2	4
	3200	3733	400	467	6	9	2	5	3	2	5
	3733	4267	467	533	6	11	2	7	3	2	5
	4267	4800	533	600	7	12	3	8	3	2	5
	4800	5500	600	688	8	14	3	9	4	2	6
	5500	6000	688	750	9	15	4	10	4	2	6
	6000	6400	750	800	9	16	4	11	4	2	6

NOTE 1 tWCKENL_WR = WL + 1 - tWCKPRE_total_WR

NOTE 2 tWCKPRE_total_WR = tWCKPRE_toggle_WR + tWCKPRE_Static

7.2.1.4 WCK2CK Sync operation followed by a READ command

Figure 58 illustrates the WCK2CK Sync operation followed by a READ command. The CAS WCK2CK Sync command must have WS_RD=1 when it is followed by READ command. No command is allowed between CAS(WS_RD=1) command and READ command, and CAS(WS_RD=1) command should be immediately followed by READ command. tWCKENL_RD is the optimal delay which guarantee WCK2CK sync operation and minimize WCK toggling power.

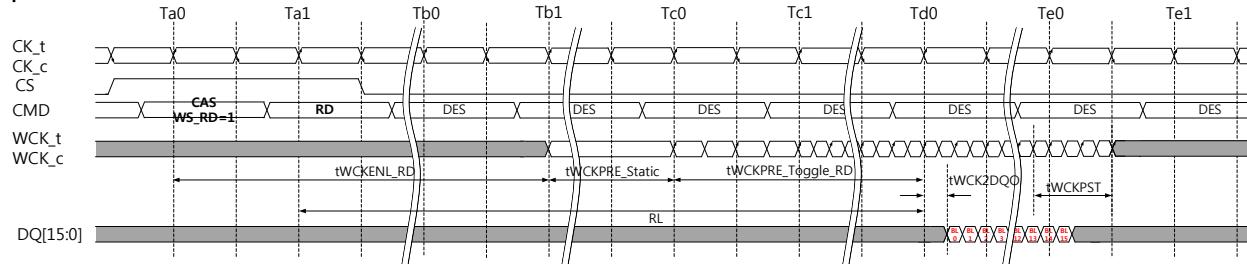


Figure 58 — WCK2CK Sync operation followed by a READ command

7.2.1.4 WCK2CK Sync operation followed by a READ command (Cont'd)

Table 158 — WCK2CK Sync AC Parameters for Read operation
DVFS disabled (MR19 OP[1:0] = 00_B), Read Link ECC off (MR22 OP[7:6]=00_B)

WCK:CK ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync READ AC Parameters [nCK]									
	Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	Set 0	Set 1	Set 2	Set 0	Set 1	Set 2	tWCKPRE_static	tWCKPRE_toggle_RD	tWCKPRE_total_RD	
2:1	40	533	10	133	6	6	6	0	0	0	1	6	7	
	533	1067	133	267	8	8	8	0	0	0	2	7	9	
	1067	1600	267	400	10	10	12	1	1	3	2	8	10	
	1600	2133	400	533	12	14	14	2	4	4	3	8	11	
	2133	2750	533	688	16	16	18	3	3	5	4	10	14	
	2750	3200	688	800	18	20	20	5	7	7	4	10	14	
4:1	40	533	5	67	3	3	3	0	0	0	1	3	4	
	533	1067	67	133	4	4	4	0	0	0	1	4	5	
	1067	1600	133	200	5	5	6	1	1	2	1	4	5	
	1600	2133	200	267	6	7	7	1	2	2	2	4	6	
	2133	2750	267	344	8	8	9	2	2	3	2	5	7	
	2750	3200	344	400	9	10	10	3	4	4	2	5	7	
	3200	3733	400	467	10	11	12	3	4	5	3	5	8	
	3733	4267	467	533	12	13	14	4	5	6	3	6	9	
	4267	4800	533	600	13	14	15	5	6	7	3	6	9	
	4800	5500	600	688	15	16	17	6	7	8	4	6	10	
	5500	6000	688	750	16	17	19	6	7	9	4	7	11	
	6000	6400	750	800	17	18	20	7	8	10	4	7	11	

NOTE 1 tWCKENL_RD = RL + 1 - tWCKPRE_total_RD

NOTE 2 tWCKPRE_total_RD = tWCKPRE_toggle_RD + tWCKPRE_Static

NOTE 3 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL value.

NOTE 4 Some operating features can affect Read Latency:

Feature	Description
1	Byte Mode
2	Read DBI and/or Read Data Copy

NOTE 5 RL Set 0 applies when no features are enabled.

RL Set 1 applies when one feature is enabled (1 or 2).

RL Set 2 applies when two features are enabled.

7.2.1.4 WCK2CK Sync operation followed by a READ command (Cont'd)

Table 159 — WCK2CK Sync AC Parameters for Read operation
DVFSC enabled (MR19 OP[1:0] = 01_B), Read Link ECC disable (MR22 OP[7:6]=00_B)

WCK:CK ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync READ AC Parameters [nCK]								
	Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	READ Latency			tWCKENL_RD			tWCKPRE_static	tWCKPRE_toggle_RD	tWCKPRE_total_RD
					Set 0	Set 1	Set 2	Set 0	Set 1	Set 2			
2:1	40	533	10	133	6	6	6	0	0	0	1	6	7
	533	1067	133	267	8	10	10	0	2	2	2	7	9
	1067	1600	267	400	12	12	14	3	3	5	2	8	10
4:1	40	533	5	67	3	3	3	0	0	0	1	3	4
	533	1067	67	133	4	5	5	0	1	1	1	4	5
	1067	1600	133	200	6	6	7	2	2	3	1	4	5

NOTE 1 tWCKENL_RD = RL + 1 - tWCKPRE_total_RD

NOTE 2 tWCKPRE_total_RD = tWCKPRE_toggle_RD + tWCKPRE_Static

NOTE 3 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL value.

NOTE 4 Some operating features can affect Read Latency:

Feature	Description
1	Byte Mode
2	Read DBI and/or Read Data Copy

NOTE 5 RL Set 0 applies when no features are enabled.

RL Set 1 applies when one feature is enabled (1 or 2).

RL Set 2 applies when two features are enabled.

Table 160 — WCK2CK Sync AC Parameters for Read operation
DVFSC disabled (MR19 OP[1:0] = 00_B), Read Link ECC enable (MR22 OP[7:6]=01_B)

WCK:CK ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync READ AC Parameters [nCK]								
	Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	READ Latency		tWCKENL_RD		tWCKPRE_static	tWCKPRE_toggle_RD	tWCKPRE_total_RD		
					Set 0	Set 1	Set 0	Set 1					
4:1	3200	3733	400	467	12	13	5	6	3	5	8		
	3733	4267	467	533	13	14	5	6	3	6	9		
	4267	4800	533	600	15	16	7	8	3	6	9		
	4800	5500	600	688	17	18	8	9	4	6	10		
	5500	6000	688	750	18	20	8	10	4	7	11		
	6000	6400	750	800	19	21	9	11	4	7	11		

NOTE 1 tWCKENL_RD = RL + 1 - tWCKPRE_total_RD

NOTE 2 tWCKPRE_total_RD = tWCKPRE_toggle_RD + tWCKPRE_Static

NOTE 3 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.

NOTE 4 RL Set 1 applies when the device is byte-mode.

7.2.1.5 WCK2CK Sync operation with CAS(WS_FAST=1)

The WCK2CK Sync operation is performed with minimum latency, tWCKENL_FAST, when a CAS command with WS_FAST=1 is issued to an LPDDR5 SDRAM. By this way, the LPDDR5 SDRAM controller can put LPDDR5 SDRAM into WCK2CK Synchronized state as early as possible. CAS(WS_FS=1) is used as a standalone command unlike CAS(WS_RD/WR) and can be issued to not only one rank but also multi-ranks simultaneously. tWCKPRE_toggle_FS can be varied by the command timing gap between CAS(WS_FS=1) and following READ or WRITE commands, whereas tWCKPRE_toggle_WR and tWCKPRE_toggle_RD are exact fixed number in nCK unit.

After CAS (WS_FSAT=1) command is issued, not only READ/ WRITE commands but also other commands like Active and Refresh can be issued. Refer to 8.1.2, CAS command timing constraints.

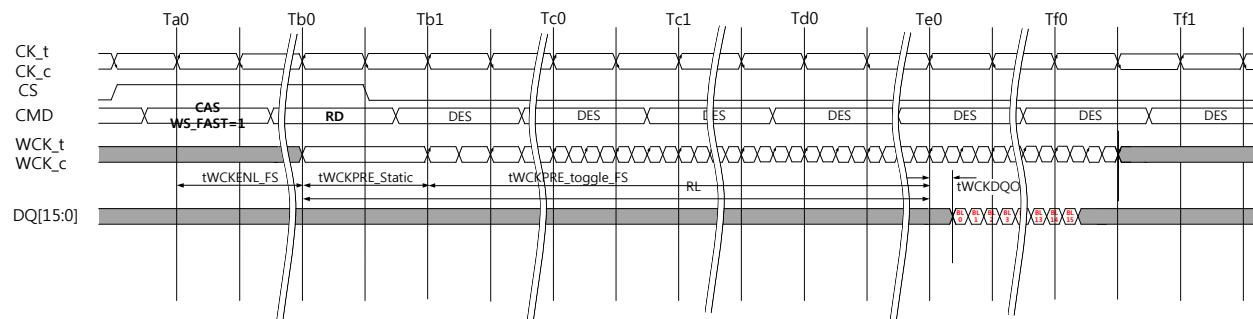


Figure 59 — Minimum latency WCK2CK Sync operation for CAS(WS_FAST=1)

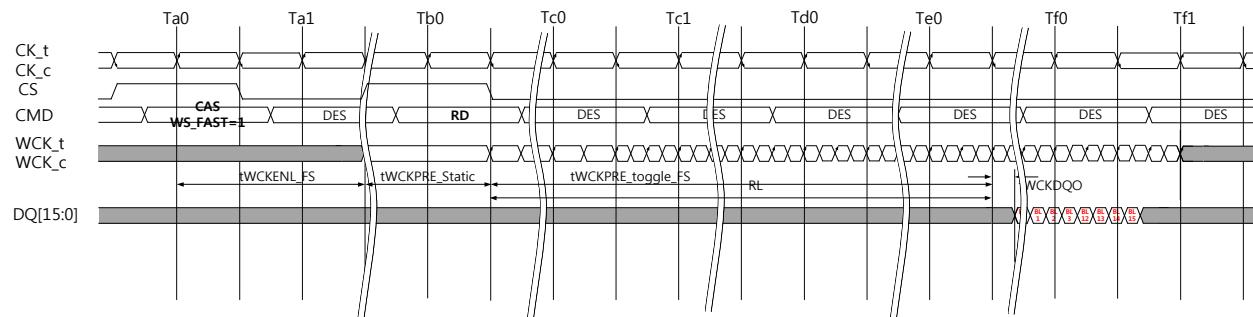


Figure 60 — WCK2CK sync operation for Read Operation with CAS(WS_FAST=1) with command gap

7.2.1.5 WCK2CK Sync operation with CAS(WS_FAST=1) (Cont'd)

Table 161 — WCK2CK Sync AC Parameters for CAS(WS_FAST)

WCK:CK Ratio	Data Rate [Mbps]		CK Frequency [MHz]		MR2 OP[3:0] setting	tWCKENL_FS [nCK]	tWCKPRE_Static [nCK]
	Lower Limit(>)	Upper Limit(≤)	Lower Limit(>)	Upper Limit(≤)			
2:1	40	533	10	133	0000 _B	0	1
	533	1067	133	267	0001 _B	0	2
	1067	1600	267	400	0010 _B	1	2
	1600	2133	400	533	0011 _B	1	3
	2133	2750	533	688	0100 _B	1	4
	2750	3200	688	800	0101 _B	2	4
4:1	40	533	5	67	0000 _B	0	1
	533	1067	67	133	0001 _B	0	1
	1067	1600	133	200	0010 _B	1	1
	1600	2133	200	267	0011 _B	1	2
	2133	2750	267	344	0100 _B	1	2
	2750	3200	344	400	0101 _B	1	2
	3200	3733	400	467	0110 _B	1	3
	3733	4267	467	533	0111 _B	1	3
	4267	4800	533	600	1000 _B	2	3
	4800	5500	600	688	1001 _B	2	4
	5500	6000	688	750	1010 _B	2	4
	6000	6400	750	800	1011 _B	2	4

7.2.1.6 Rank to rank WCK2CK Sync operation

There are two different methods to control WCK2CK Sync state of two rank LPDDR5 SDRAM. The first method is to start WCK2CK Sync process of rank 1 after completing DQ data burst of rank 0 as shown in Figure 61. In this case, tWCKPST of rank 0 and tWCKPRE of rank 1 should be guaranteed for right RDQS post-amble of read operation of rank 0 and for right WCK2CK Synchronization operation of rank 1, respectively.

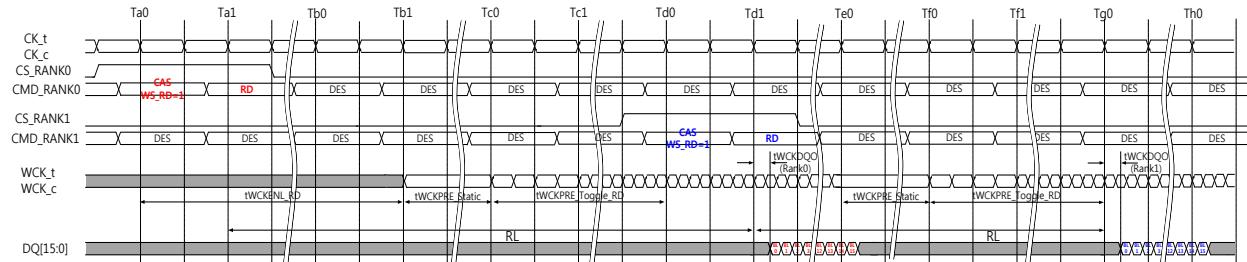


Figure 61 — Minimum gap rank to rank read operation with WCK2CK Sync after completing DQ burst in one rank

The second method is to start WCK2CK Sync process of both ranks simultaneously as shown in Figure 62. When both ranks are not in WCK2CK synchronized state and DQ bursts between two ranks are closed, a simultaneous CAS command with WS_FAST=1 is the recommended way, considering efficient DQ bus utilization.

If the following DQ bursts of one rank are far from the preceding ones of the other rank, extra power consumption due to WCK toggle should be considered. After synchronizing both ranks, if rank 0 is not used, CAS (WCK buffer off) command can be issued to rank 0 to save power.

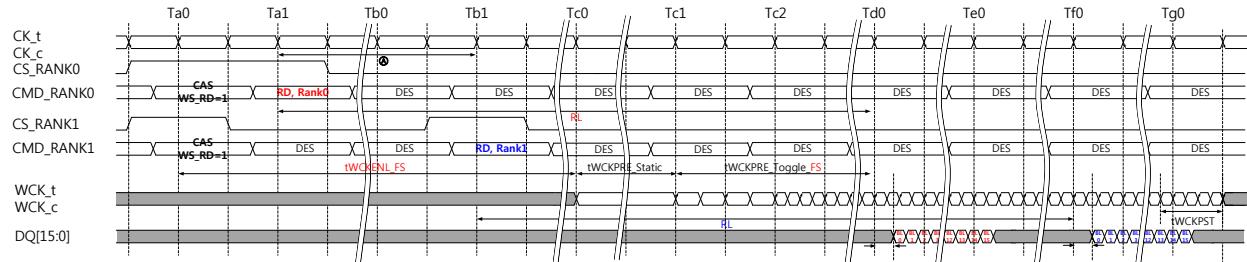


Figure 62 — Simultaneous WCK2CK Sync process for multi-ranks (especially two ranks)

7.2.2 WCK2CK SYNC Off Timing Definition

The next commands which require WCK2CK SYNC can be issued up to the maximum timing defined as the following tables. Duplicated CAS(WS_WR/RD) command issuing is inhibited during this period. Once the maximum timing is exceeded, CAS(WS_FS or WS_WR/RD) command is required to issue before issuing the commands which require WCK2CK SYNC.

Table 162 — WCK2CK SYNC Off Timing Definition (16B Mode) for WR16/32, RD16/32 and MWR

Current Command	Next Command	Bank Relationship	Command Timing Constraints w/o a new WCK2CK SYNC Start		Note
			Min	Max	
WRITE (WR16, WR32)	WRITE (WR16, WR32)	Any Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Same Bank	4*BL/n (WR16) 2.5*BL/n (WR32)	WL + BL/n_max + RD(tWCKPST/tCK)	1,2,3
		Different Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	READ (RD16, RD32)	Any Banks	WL + BL/n + RU(tWTR/tCK)	-	1,2
MASK WRITE	WRITE (WR16, WR32)	Any Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Same Bank	4*BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	1,2,3
		Different Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	READ (RD16, RD32)	Any Banks	WL + BL/n + RU(tWTR/tCK)	-	1,2
READ (RD16, RD32)	WRITE (WR16, WR32)	Any Banks	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Any Banks	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n_max + RD(tWCKPST/tCK)	2
	READ (RD16, RD32)	Any Banks	BL/n	RL + BL/n_max + RD(tWCKPST/tCK)	2

NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).

NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.

NOTE 3 If Min timing is equal or larger than Max timing depending WL, a new WCK2CK SYNC start (CAS-WS_FS/WS_WR) is required before issuing a next command.

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 163 — WCK2CK SYNC Off Timing Definition (BG Mode) for WR16/32, RD16/32 and MWR

Current Command	Next Command	Bank Relationship	Command Timing Constraints w/o a new WCK2CK SYNC Start		Note
			Min	Max	
WRITE (WR16, WR32)	WRITE (WR16, WR32)	Any Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Same Bank in Same BG	4*BL/n_max (WR16) 2.5*BL/n_max (WR32)	WL + BL/n_max + RD(tWCKPST/tCK)	1,2,3
		Different Banks in Same BG	BL/n_max	WL + BL/n_max + RD(tWCKPST/tCK)	1,2
		Different Banks in Different BG	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	READ (RD16, RD32)	Same or Different Banks in Same BG	WL + BL/n_max + RU(tWTR_L/tCK)	-	1,2
		Different Banks in Different BG	WL + BL/n_min + RU(tWTR_S/tCK)	-	1,2
MASK WRITE	WRITE (WR16, WR32)	Any Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Same Banks in Same BG	4*BL/n_max	WL + BL/n_max + RD(tWCKPST/tCK)	1,2,3
		Different Banks in Same BG	BL/n_max	WL + BL/n_max + RD(tWCKPST/tCK)	2
		Different Banks in Different BG	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	READ (RD16, RD32)	Same or Different Banks in Same BG	WL + BL/n_max + RU(tWTR_L/tCK)	-	1,2
		Different Banks in Different BG	WL + BL/n_min + RU(tWTR_S/tCK)	-	1,2
READ (RD16, RD32)	WRITE (WR16, WR32)	Same or Different Banks in Same BG	RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n_max + RD(tWCKPST/tCK)	2
	Different Banks in Different BG	RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL	2		
	MASK WRITE	Same or Different Banks in Same BG	RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n_max + RD(tWCKPST/tCK)	2
		Different Banks in Different BG	RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL		2
	READ (RD16, RD32)	Any Banks	BL/n	RL + BL/n_max + RD(tWCKPST/tCK)	2

NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).

NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.

NOTE 3 If Min timing is equal or larger than Max timing depending WL, a new WCK2CK SYNC start (CAS-WS_FS/WS_WR) is required before issuing a next command.

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 164 — WCK2CK SYNC Off Timing Definition (8B Mode) for WR16/32, RD16/32 and MWR

Current Command	Next Command	Bank Relationship	Command Timing Constraints w/o a new WCK2CK SYNC start		Note
			Min	Max	
WRITE	WRITE	Any Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Same Bank	4*BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	1,2,3
		Different Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	READ	Any Banks	WL + BL/n + RU(tWTR/tCK)	-	1,2
MASK WRITE	WRITE	Any Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Same Bank	4*BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	1,2,3
		Different Banks	BL/n	WL + BL/n_max + RD(tWCKPST/tCK)	2
	READ	Any Banks	WL + BL/n + RU(tWTR/tCK)	-	1,2
READ	WRITE	Any Banks	RL + BL/n + RU(tWCKDQO(max) /tCK) - WL	RL + BL/n_max + RD(tWCKPST/tCK)	2
	MASK WRITE	Any Banks	RL + BL/n + RU(tWCKDQO(max) /tCK) - WL	RL + BL/n_max + RD(tWCKPST/tCK)	2
	READ	Any Banks	BL/n	RL + BL/n_max + RD(tWCKPST/tCK)	2

NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).

NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.

NOTE 3 If Min timing is equal or larger than Max timing depending WL, a new WCK2CK SYNC start (CAS-WS_FS/WS_WR) is required before issuing a next command.

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 165 — WCK2CK SYNC Off Timing Definition for MRR

Current Command	Next Command	Command Timing Constraints w/o a new WCK2CK SYNC start		Note
		Min	Max	
MRR	MRR	tMRR	$RL + BL/n_{max} + RD(tWCKPST/tCK)$	2,4
	READ (RD16, RD32 with or w/o AP)	$RL + BL/n_{max} + RD(tWCKPST/tCK) + 2$	-	1,2,4
	WRITE (WR16, WR32, MWR with or w/o AP)	$RL + BL/n_{max} + RU(tWCKDQO(max)/tCK) - WL + 2$	$RL + BL/n_{max} + RD(tWCKPST/tCK)$	2,3,4
READ (RD16, RD32 with or w/o AP)	MRR	$RL + BL/n_{max} + RD(tWCKPST/tCK) + 2$	-	1,2
WRITE (WR16, WR32, MWR with or w/o AP)	MRR	$WL + BL/n_{max} + RU(tWTR/tCK)$	-	1,2

NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_RD).

NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.

NOTE 3 In case of DQ ODT enabled, MRR-WRITE (min) should be "RL + BL/n_max + RU(tWCKDQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) +2".

NOTE 4 Actual BL/n_max value is as follows;

CKR=2:1, 16B mode=4nCK, 8B mode=8nCK,

CKR=4:1, 16B mode=2nCK, BG mode=4nCK, 8B mode=4nCK

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 166 — WCK2CK SYNC Off Timing Definition for Training Commands

Current Command	Next Command	Command Timing Constraints w/o a new WCK2CK SYNC start		Note
		Min	Max	
WRITE FIFO (WFF)	WRITE FIFO (WFF)	2nCK (CKR=4:1) 4nCK (CKR=2:1)	WL + BL/n_max + RD(tWCKPST/tCK)	2,3
	READ FIFO (RFF)	WL + BL/n_max + RU(tWTR/tCK)	-	1,2,3
	WRITE (WR16, WR32, MWR with or w/o AP)	Not Allowed		2
	READ (RD16, RD32 with or w/o AP), MRR	Not Allowed		2
	READ DQ Calibration (RDC)	Not Allowed		2
READ FIFO (RFF)	WRITE FIFO (WFF)	tRTW	RL + BL/n_max + RD(tWCKPST/tCK)	2,3
	READ FIFO (RFF)	2nCK (CKR=4:1) 4nCK (CKR=2:1)	RL + BL/n_max + RD(tWCKPST/tCK)	2,3
	WRITE (WR16, WR32, MWR with or w/o AP)	tRTRRD	-	1,2
	READ (RD16, RD32 with or w/o AP), MRR	tRTRRD	-	1,2
	READ DQ Calibration (RDC)	tRTRRD	-	1,2
READ DQ Calibration (RDC)	WRITE FIFO (WFF)	tRTRRD	-	1,2
	READ FIFO (RFF)	Not Allowed		2
	WRITE (WR16, WR32, MWR with or w/o AP)	tRTRRD	-	1,2
	READ (RD16, RD32 with or w/o AP), MRR	tRTRRD	-	1,2
	READ DQ Calibration (RDC)	2nCK (CKR=4:1) 4nCK (CKR=2:1)	RL + BL/n_max + RD(tWCKPST/tCK)	2,3
WRITE (WR16, WR32, MWR with or w/o AP)	WRITE FIFO (WFF)	tWRWTR	-	1,2
	READ FIFO (RFF)	Not Allowed		2
	READ DQ Calibration (RDC)	WL + BL/n_max + RU(tWTR/tCK)	-	1,2
READ (RD16, RD32 with or w/o AP), MRR	WRITE FIFO (WFF)	tRTRRD	-	1,2
	READ FIFO (RFF)	Not Allowed		2
	READ DQ Calibration (RDC)	tRTRRD	-	1,2

NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).

NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.

NOTE 3 Actual BL/n_max value is as follows;

CKR=2:1, 16B mode=4nCK, 8B mode=8nCK,

CKR=4:1, 16B mode=2nCK, BG mode=4nCK, 8B mode=4nCK

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

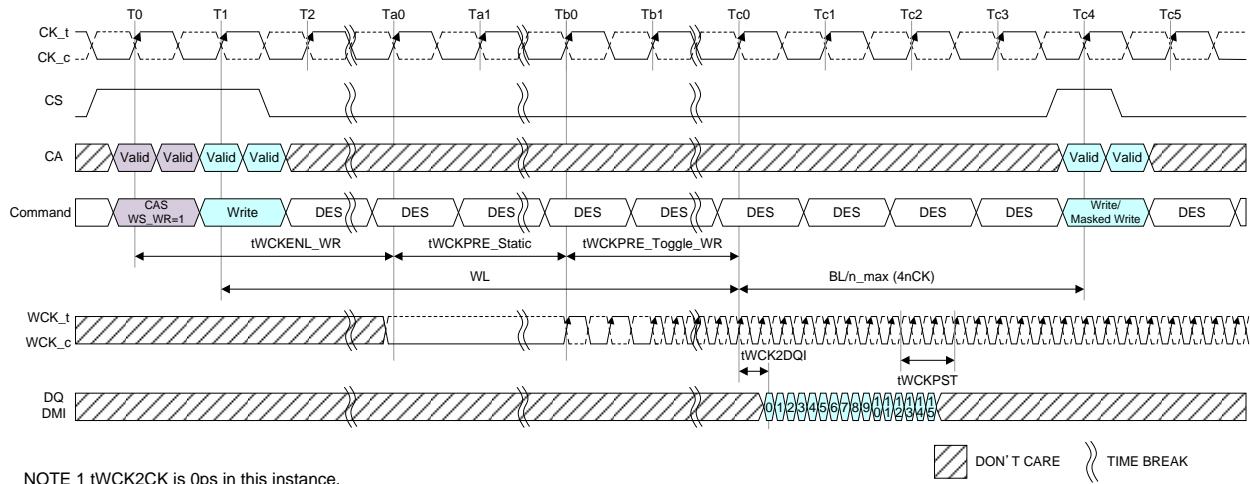


Figure 63 — Write sync off timing BG Mode, CKR (WCK vs. CK) = 4:1, BL=16

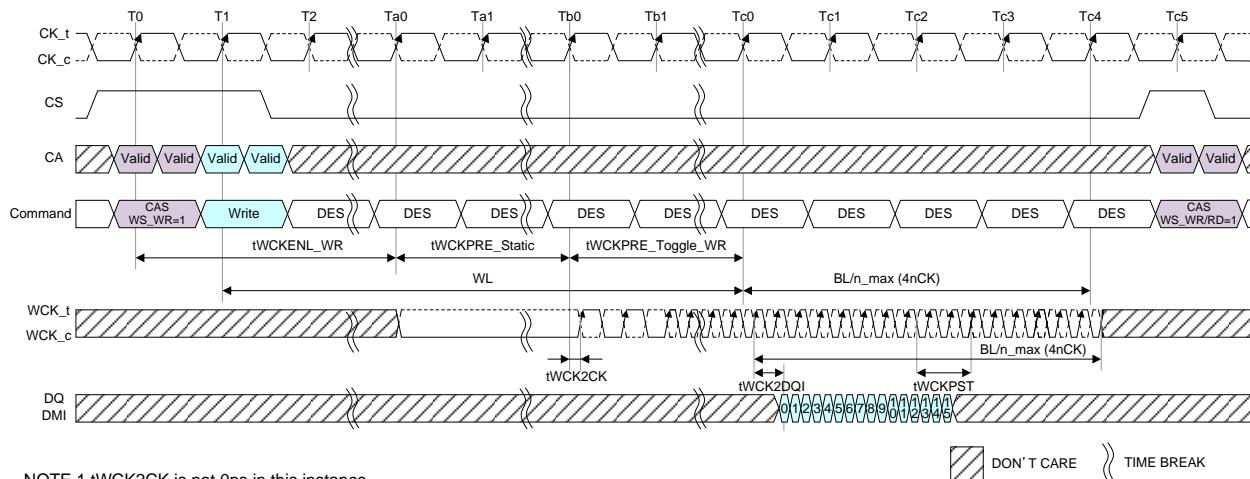


Figure 64 — Write sync off timing (WCK2CK Sync is expired), BG Mode, CKR (WCK vs. CK) = 4:1, BL=16

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

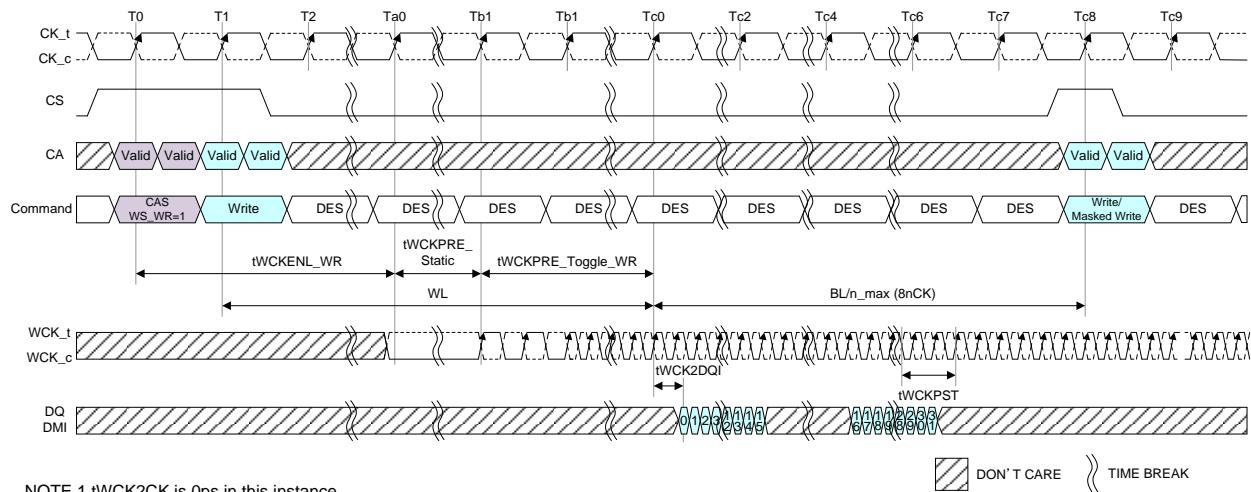


Figure 65 — Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32

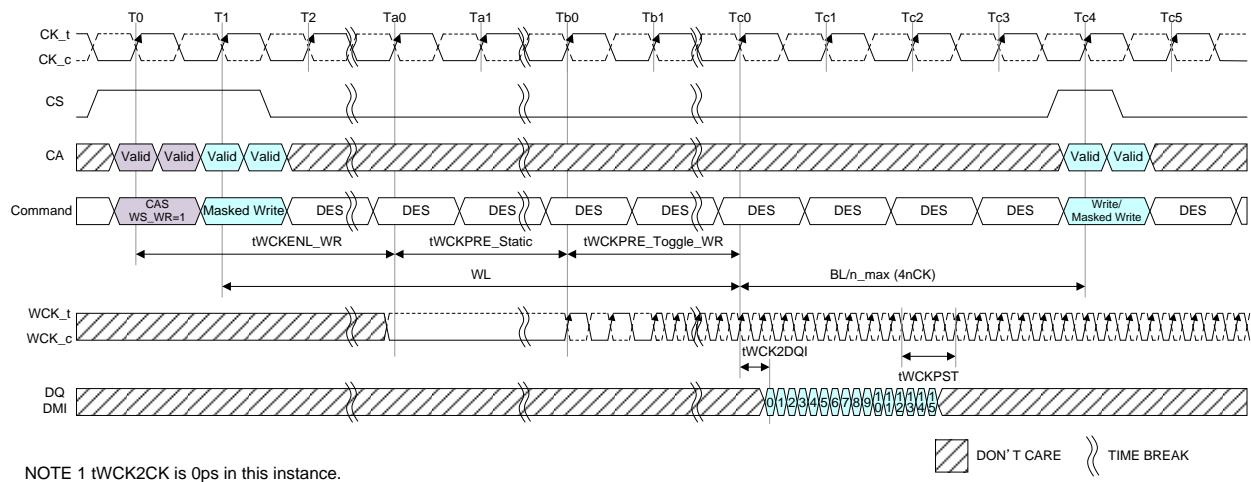


Figure 66 — Masked Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

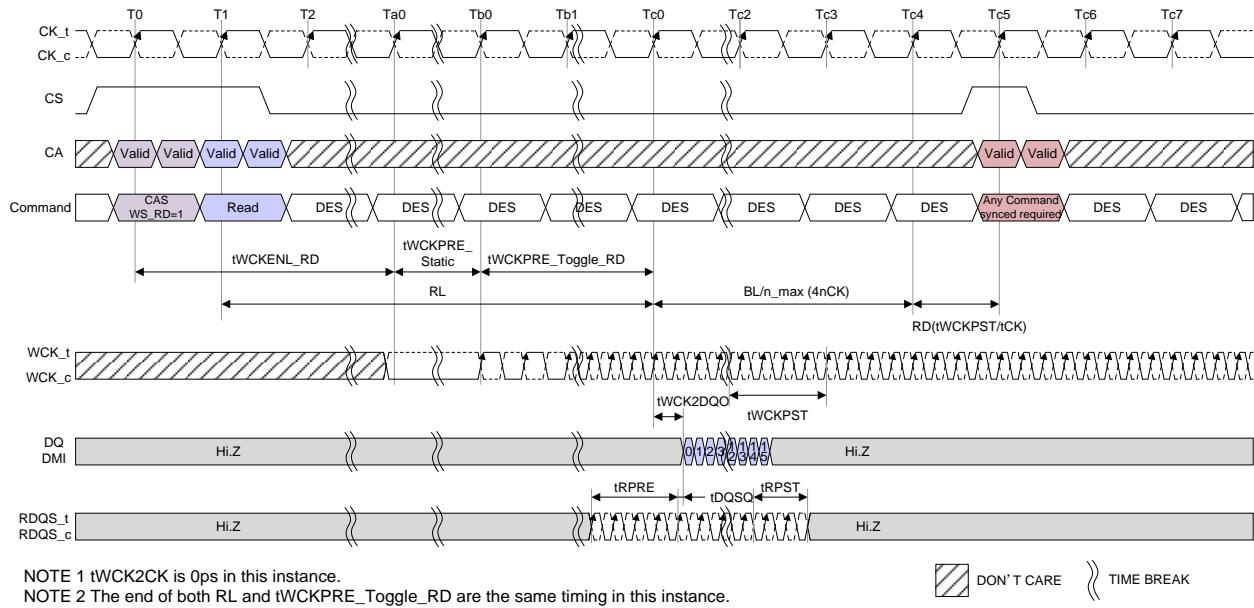


Figure 67 — Read sync off timing BG Mode: CKR (WCK vs. CK) = 4:1, BL=16, tRPST=2.5nWCK

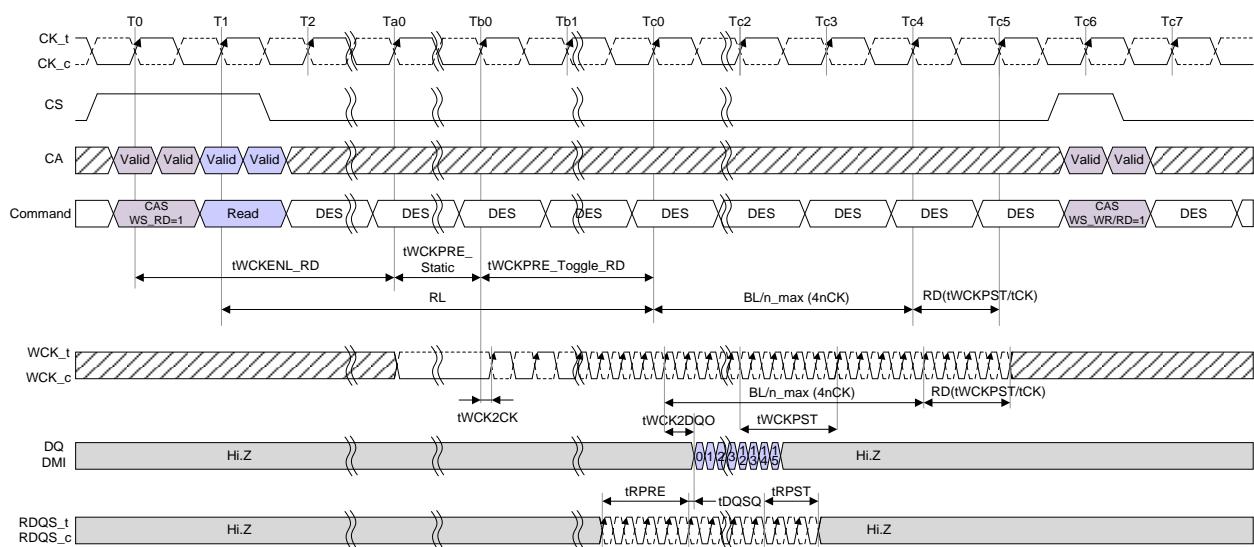


Figure 68 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR = 4:1, BL=16, tRPST=2.5nWCK

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

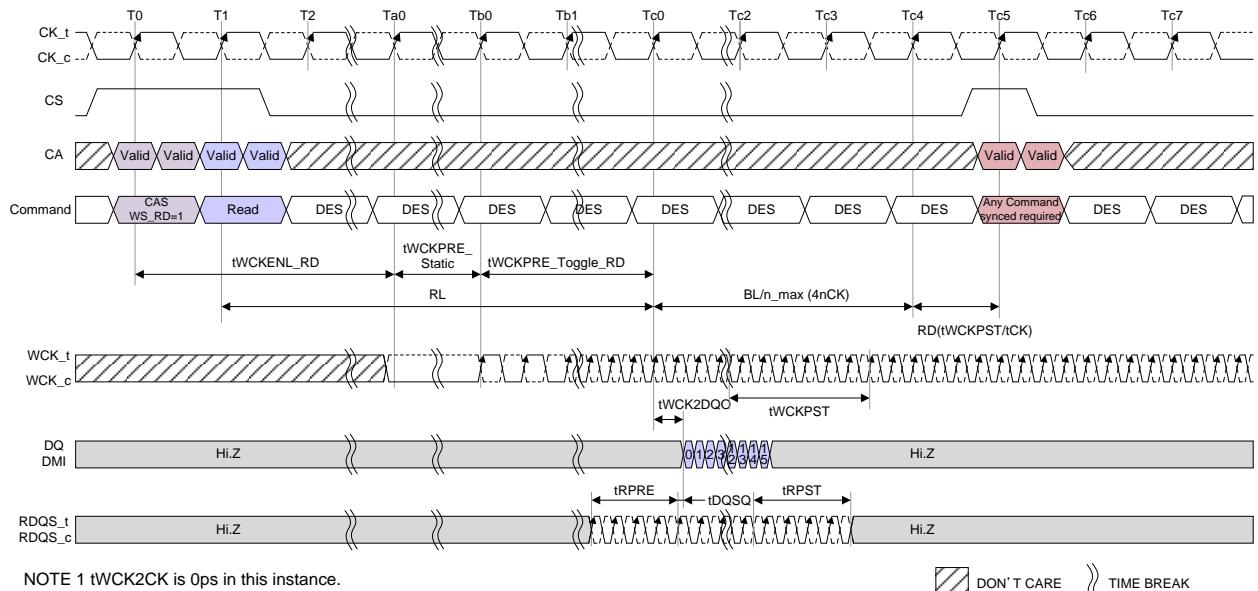


Figure 69 — Read sync off timing BG Mode: CKR (WCK vs. CK) = 4:1, BL=16, tRPST=4.5nWCK

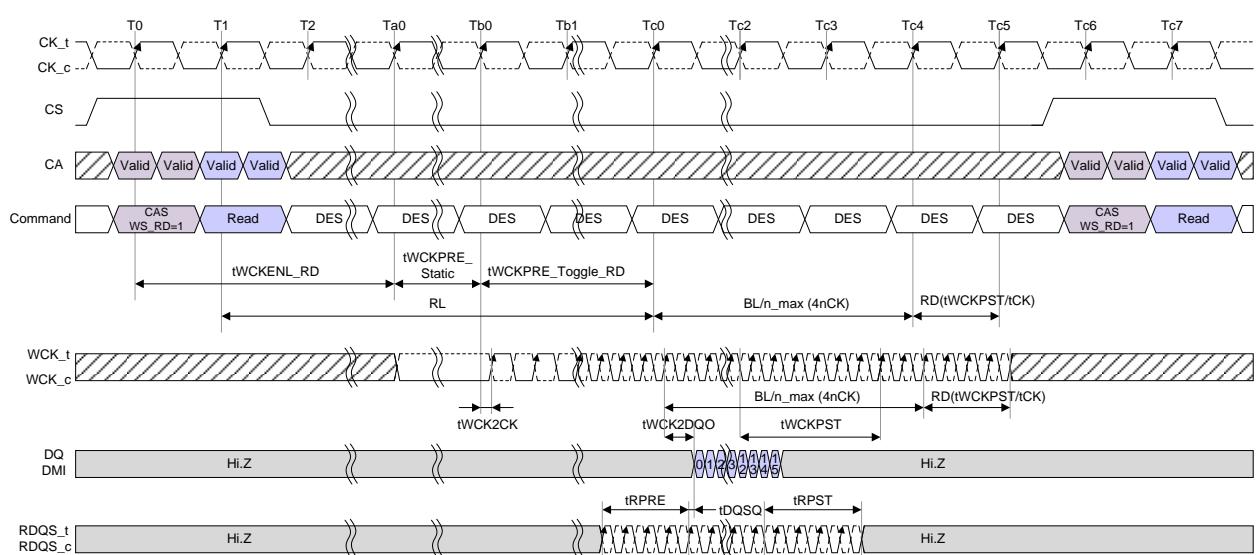


Figure 70 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR = 4:1, BL=16, tRPST=4.5nWCK

7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

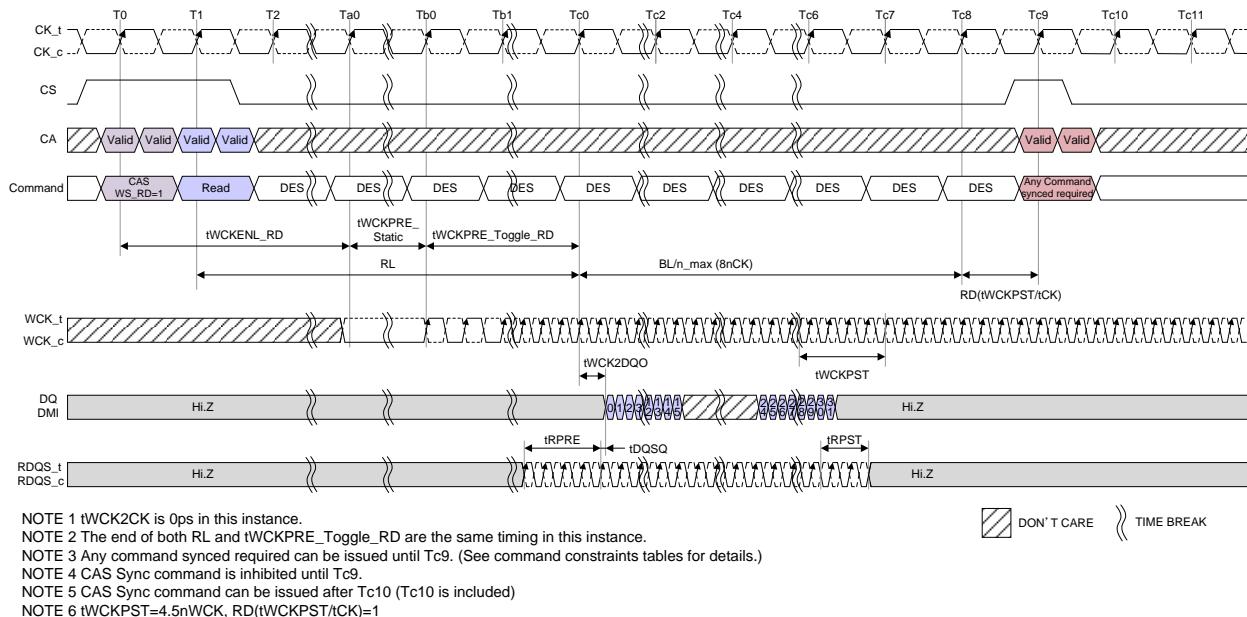


Figure 71 — Read sync off timing BG Mode: CKR (WCK vs. CK) = 4:1, BL=32, tRPST=2.5nWCK

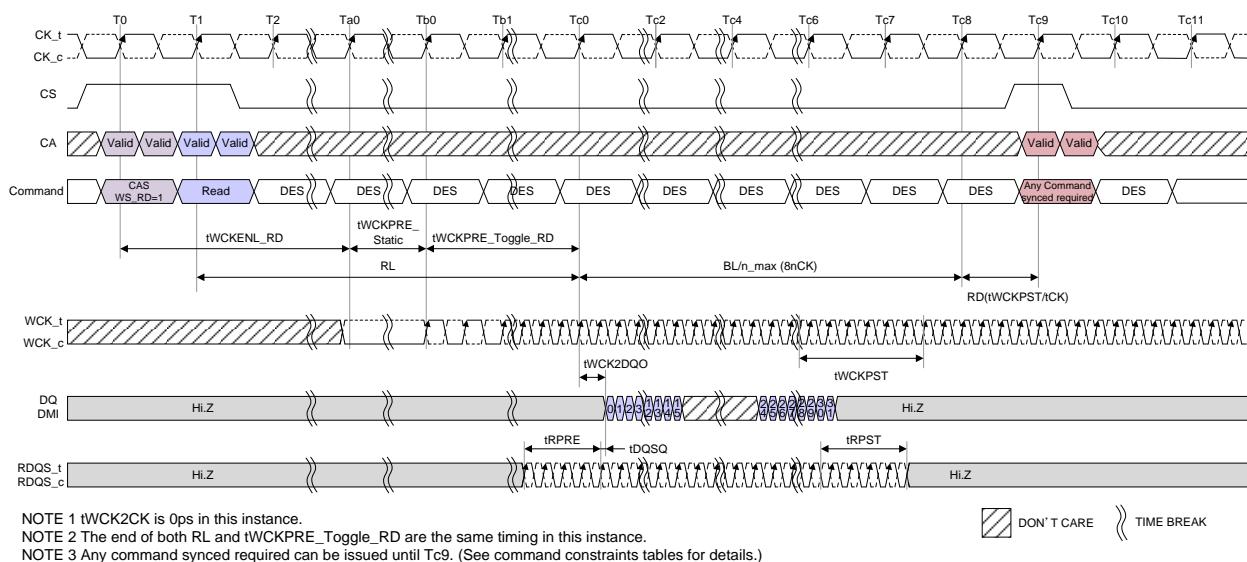


Figure 72 — Read sync off timing BG Mode: CKR (WCK vs. CK) = 4:1, BL=32, tRPST=4.5nWCK

7.2.3 Write Clock Free Running mode

An LPDDR5 SDRAM supports WCK free running mode as an MRS option. WCK free running mode is enabled by setting MR18 OP[4] = 1. When WCK free running mode is enabled, the WCK buffer in an LPDDR5 SDRAM is turned on with WCK2CK synchronization and keeps being turned on until DRAM receives power down, self-refresh power-down or deep-sleep commands or reset. Therefore, the DRAM controller must keep WCK toggling at its full rate after WCK2CK synchronization regardless of DQ operation. As the WCK2CK synchronization information is lost with power down entry, the DRAM controller must perform a WCK2CK synchronization sequence after power down exit before DQ operation.

Figure 73 illustrates WCK free running mode with WCK2CK synchronization followed by a write command. In this timing diagram, DRAM is initially in power-down state at Ta0. Therefore, the WCK buffer in DRAM is off state, losing the WCK2CK synchronization information. Although, the MR18 OP[4]=1, the WCK buffer is not turned on until receiving a CAS command with WCK2CK-sync bit high. At Tb1, a CAS command with WS_WR=1 initiates WCK2CK synchronization process and turns on the WCK buffer in DRAM. Once enabled, the WCK buffer keeps being on regardless of following commands until receiving the power-down entry command at Tf1. At Tf1, the power-down entry command turns off WCK buffer to reduce DRAM power consumption. The timing diagram of WCK free running mode starting with WCK2CK synchronization followed by a read command is shown in Figure 74.

7.2.3 Write Clock Free Running mode (Cont'd)

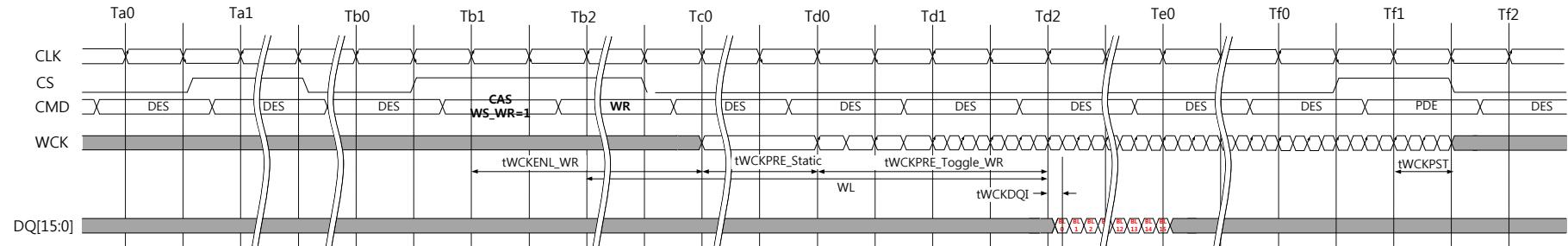


Figure 73 — WCK free running mode starting with WCK2CK-sync operation followed by a write command

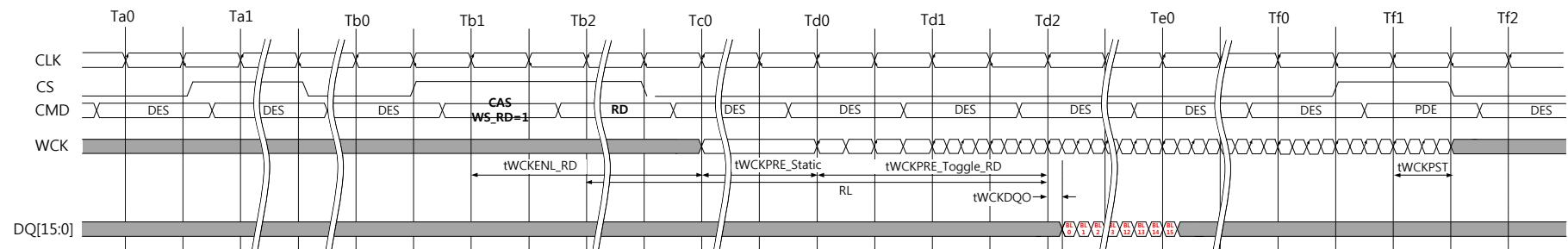


Figure 74 — Figure 2. WCK free running mode starting with WCK2CK-sync operation followed by a read command

7.2.3 Write Clock Free Running mode (Cont'd)

In WCK free running mode, DRAM controller can turn off WCK buffer in DRAM by sending a special WCK buffer off CAS command to save memory system power. This WCK buffer off command is shown in Table 167. An LPDDR5 SDRAM accepts WCK buffer off CAS command only when MR18 OP[4]=1 and ignores it when MR18 OP[4]=0. DRAM turns off WCK buffer asynchronously after receiving WCK buffer command. After WCK buffer off, a new WCK2CK synchronization sequence is required. WCK buffer off command is allowed only when there is no on-going write, read or other DQ operation in the DRAM. Figure 75 and Figure 76 illustrate CAS command based WCK buffer off following a write and read command, respectively. The required delay to issue WCK buffer off command after finishing DQ operation is tWCKOFF. The minimum value of tWCKOFF is RU(max(tWCKDQO)/tCK) + BL/n + 1. (n=8 in WCK:CK=4:1 mode and n=4 in WCK:CK=2:1 mode). For simple tWCKOFF expression, tWCKOFF formula uses the unified parameter tWCKDQO regardless of write or read operation, because the value of tWCKDQO is bigger than the value of tWCKDQI.

Table 167 — WCK buffer off CAS command (Allowed only when MR18 OP[4]=1)

Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CK
CAS	H	L	L	H	V	WS_WR=H	WS_RD=H	WS_FAST=H	R1
	X	V	V	V	V	V	V	V	F1

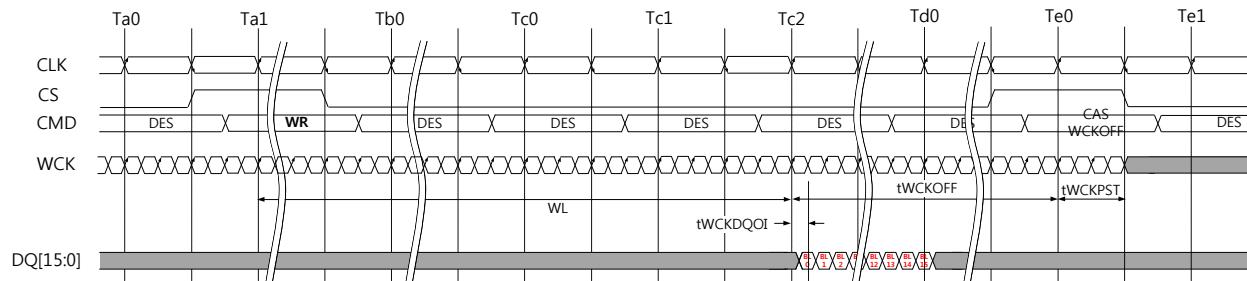


Figure 75 — CAS Command based WCK Buffer off following write command
 $\min(tWCKOFF) = RU(\max(tWCKDQO)/tCK) + BL/n + 1$, where n=8 in WCK:CK=4:1 mode
 and n=4 in WCK:CK=2:1 mode

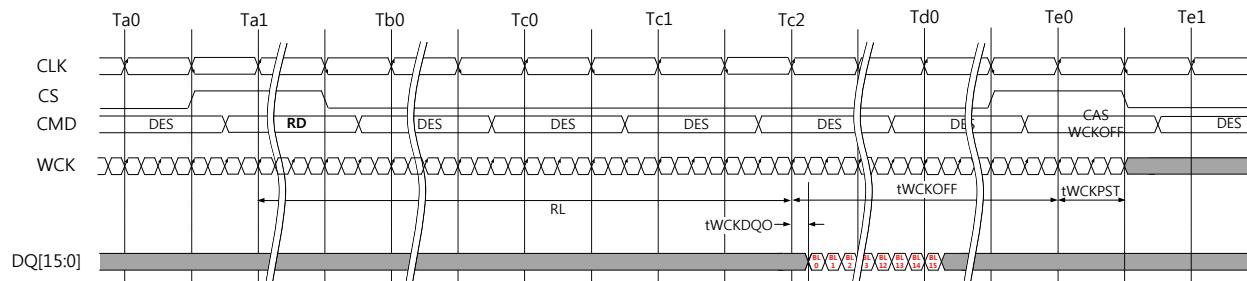
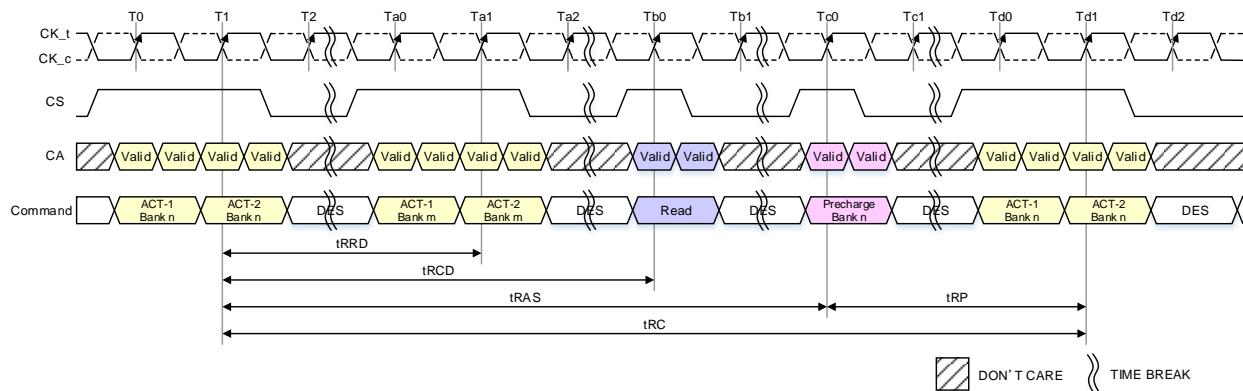


Figure 76 — CAS Command based WCK Buffer off following read command
 $\min(tWCKOFF) = RU(\max(tWCKDQO)/tCK) + BL/n + 1$, where n=8 in WCK:CK=4:1 mode
 and n=4 in WCK:CK=2:1 mode

7.3 Row operation

7.3.1 Active Command

The ACTIVATE command is composed of two commands, Activate-1 command and Activate-2. Activate-1 command is issued by holding CS HIGH, CA0 HIGH, CA1 HIGH, and CA2 HIGH at the rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. Activate-2 command shall be issued within 8 clock cycles (tAAD) after Activate-1 command was issued. Within tAAD period Only CAS, WRITE, MASKED WRITE, READ, MRR, PRECHARGE/Refresh (to a different bank) commands can be issued between ACTIVATE-1 and ACTIVATE-2 commands. It is an illegal operation if an Activate-2 command is not issued within tAAD of an Activate-1 command. During 8 bank mode, the bank addresses BA0, BA1, and BA2 are used to select desired bank. During BG mode, the bank/bank group addresses BA0, BA1, BG0, and BG1 are used to select desired bank. During 16 bank mode, the bank addresses BA0, BA1, BA2, and BA3 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command is required to be applied before any READ or WRITE/Masked Write operation can be executed. The SDRAM can accept a READ or WRITE/Masked Write command at tRCD after the ACTIVATE command is issued. After a bank has been activated, precharge command is issued to precharge bank or banks. The bank active and precharge times are defined as tRAS and tRP respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the SDRAM (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

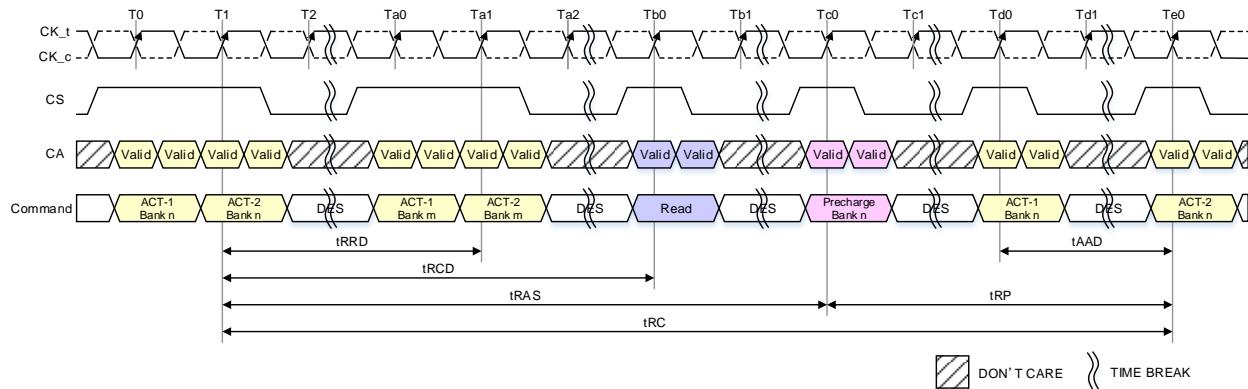


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 A PRECHARGE command uses tRPab timing for all bank PRECHARGE and tRPpb timing for single-bank PRECHARGE. In this figure, tRP is used to denote either all bank PRECHARGE or a single-bank PRECHARGE.

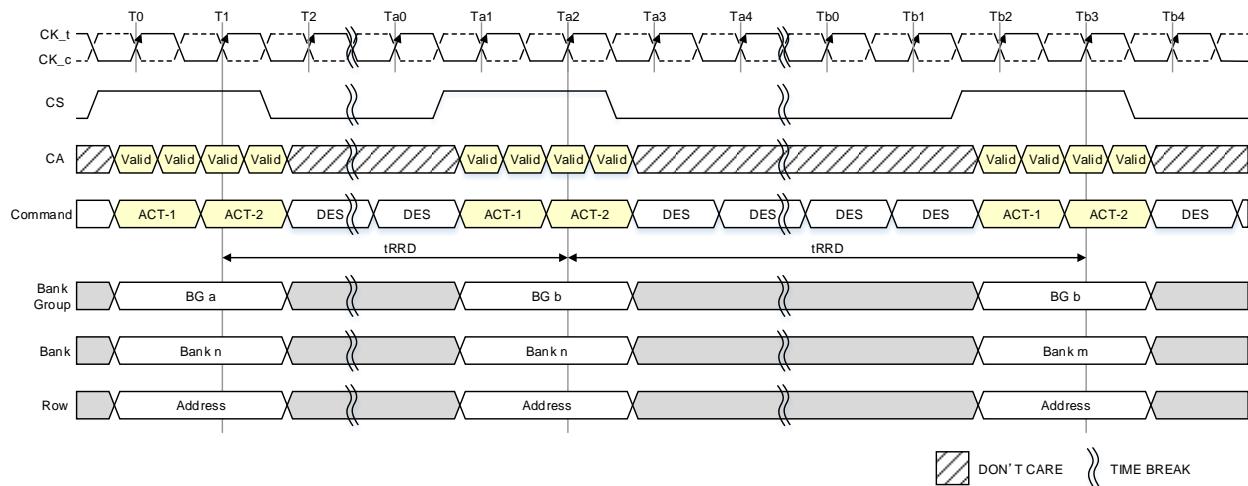
Figure 77 — Activate command for 8B/16B mode

7.3.1 Active Command (Cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
 NOTE 2 A PRECHARGE command uses tRPab timing for all bank PRECHARGE and tRPpb timing for single-bank PRECHARGE. In this figure, tRP is used to denote either all bank PRECHARGE or a single-bank PRECHARGE.

Figure 78 — Activate Command with Activate1 and Activate-2 spacing for 8B/16B mode



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
 NOTE 2 tIRR: ACTIVATE to ACTIVATE Command period: Applies to consecutive ACTIVATE Commands to different Bank Group.
 NOTE 3 tIRR: ACTIVATE to ACTIVATE Command period: Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group, too.

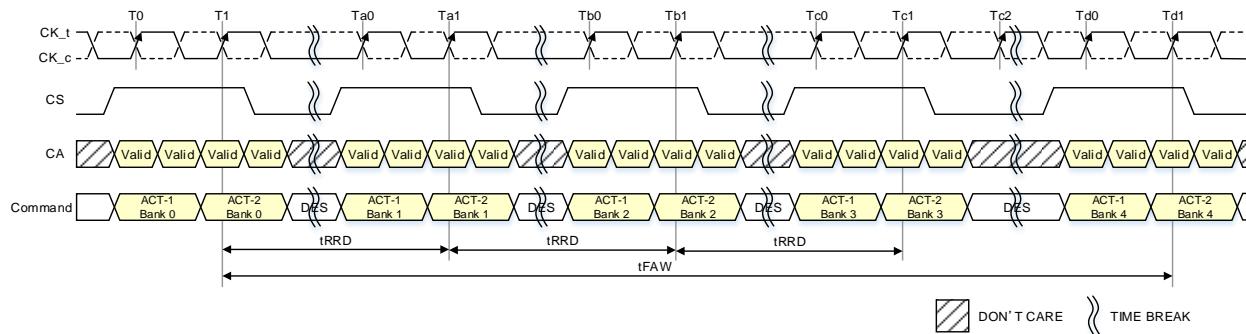
Figure 79 — Activate command for BG mode

7.3.1.1 8-Bank mode SDRAM Operation

Certain restrictions on operation of the 8-banks LPDDR5 SDRAM are required to be observed the number of sequential Bank Activation that can be issued.

8 bank SDRAM Sequential Bank Activation Restriction:

No more than 4 Banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceed the tFAW time.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 80 — 8 Banks tFAW Timing

7.3.1.2 BG mode SDRAM Operation

Certain restrictions on operation of the BG mode LPDDR5 SDRAM is required to be observed the number of sequential ACTIVATE commands that can be issued.

BG mode SDRAM Sequential Bank Activation Restriction:

No more than 4 Banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(tFAW / tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceed the tFAW time.

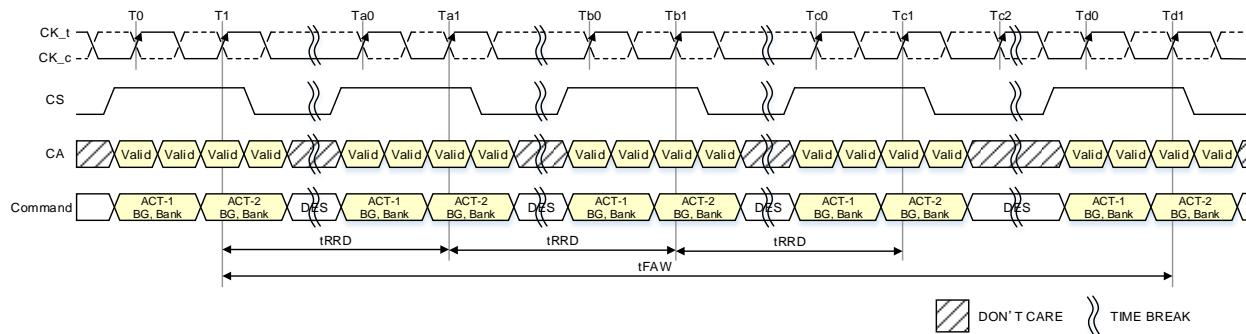


Figure 81 — BG mode tFAW timing

7.3.2 Pre-Charge Operation

7.3.2.1 Pre-Charge Operation

The Precharge command is used to Precharge or close a bank that has been activated. The Precharge command is initiated with CS, and CA[6:0] in the proper state as defined by the Command Truth Table, **Table 154**. The Precharge command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to Precharge. The Precharged bank(s) will be available for subsequent row access tRPab after an all-bank Precharge command is issued, or tRPpb after a single-bank Precharge command is issued.

To ensure that LPDDR5 devices can meet the instantaneous current demands, the row-Precharge time for an all-bank Precharge (tRPab) is longer than the per bank Precharge time (tRPpb).

Table 168 — Precharge Bank Selection 8 Bank mode

AB (CA[6], F1)	BA2 (CA[2], F1)	BA1 (CA[1], F1)	BA0 (CA[0], F1)	Precharged Bank(s)
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Valid	Valid	Valid	All Banks

7.3.2.1 Pre-Charge Operation (Cont'd)

Table 169 — Precharge Bank Selection 4 Bank / 4 Bank Group mode

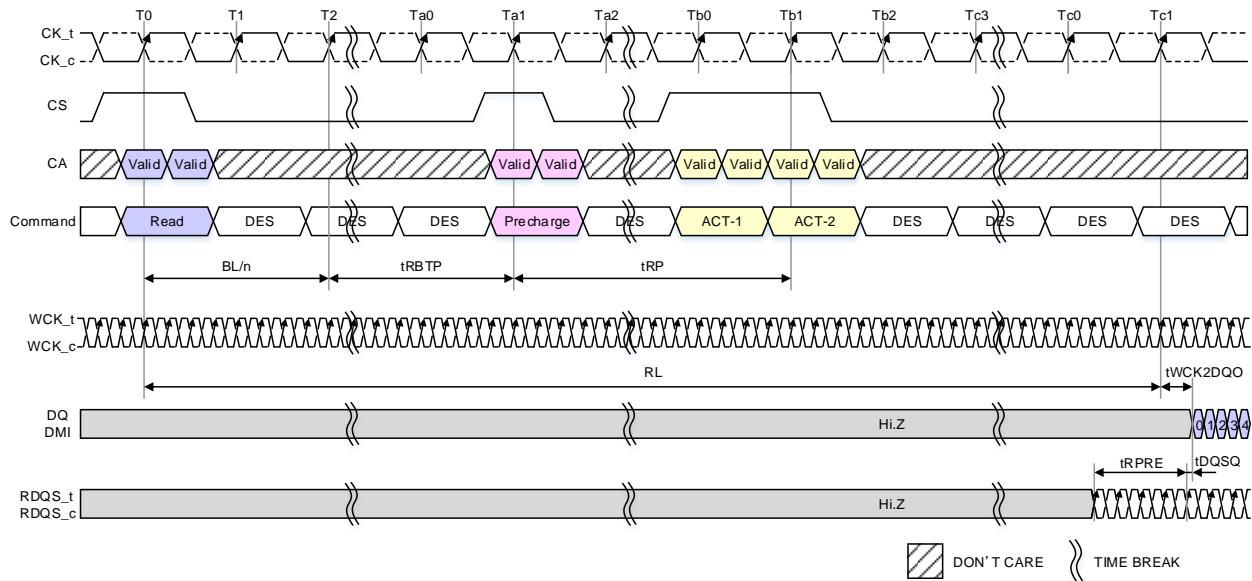
AB (CA[6], F1)	BG1 (CA[3], F1)	BG0 (CA[2], F1)	BA1 (CA[1], F1)	BA0 (CA[0], F1)	Precharged Bank(s)
0	0	0	0	0	Bank Group 0, Bank 0 only
0	0	0	0	1	Bank Group 0, Bank 1 only
0	0	0	1	0	Bank Group 0, Bank 2 only
0	0	0	1	1	Bank Group 0, Bank 3 only
0	0	1	0	0	Bank Group 1, Bank 0 only
0	0	1	0	1	Bank Group 1, Bank 1 only
0	0	1	1	0	Bank Group 1, Bank 2 only
0	0	1	1	1	Bank Group 1, Bank 3 only
0	1	0	0	0	Bank Group 2, Bank 0 only
0	1	0	0	1	Bank Group 2, Bank 1 only
0	1	0	1	0	Bank Group 2, Bank 2 only
0	1	0	1	1	Bank Group 2, Bank 3 only
0	1	1	0	0	Bank Group 3, Bank 0 only
0	1	1	0	1	Bank Group 3, Bank 1 only
0	1	1	1	0	Bank Group 3, Bank 2 only
0	1	1	1	1	Bank Group 3, Bank 3 only
1	Valid	Valid	Valid	Valid	All Banks

Table 170 — Precharge Bank Selection 16 Banks mode

AB (CA[6], F1)	BA3 (CA[3], F1)	BA2 (CA[2], F1)	BA1 (CA[1], F1)	BA0 (CA[0], F1)	Precharged Bank(s)
0	0	0	0	0	Bank 0 only
0	0	0	0	1	Bank 1 only
0	0	0	1	0	Bank 2 only
0	0	0	1	1	Bank 3 only
0	0	1	0	0	Bank 4 only
0	0	1	0	1	Bank 5 only
0	0	1	1	0	Bank 6 only
0	0	1	1	1	Bank 7 only
0	1	0	0	0	Bank 8 only
0	1	0	0	1	Bank 9 only
0	1	0	1	0	Bank 10 only
0	1	0	1	1	Bank 11 only
0	1	1	0	0	Bank 12 only
0	1	1	0	1	Bank 13 only
0	1	1	1	0	Bank 14 only
0	1	1	1	1	Bank 15 only
1	Valid	Valid	Valid	Valid	All Banks

7.3.2.1 Pre-Charge Operation (Cont'd)

The Precharge command can be issued after $BL/n + t_{RBTP}$ has been satisfied when bank organization is 16B mode. Refer to 8.1.1 for the command constraints tables for other modes (BG and 8B mode). However Precharge cannot be issued until after t_{RAS} is satisfied. A new bank Activate command can be issued to the same bank after the row Precharge time (t_{RP}) has elapsed. The minimum Read-to-Precharge time must also satisfy a minimum analog time from the rising clock edge the Read command. For LPDDR5 Read-to-Precharge timings see Figure 82.

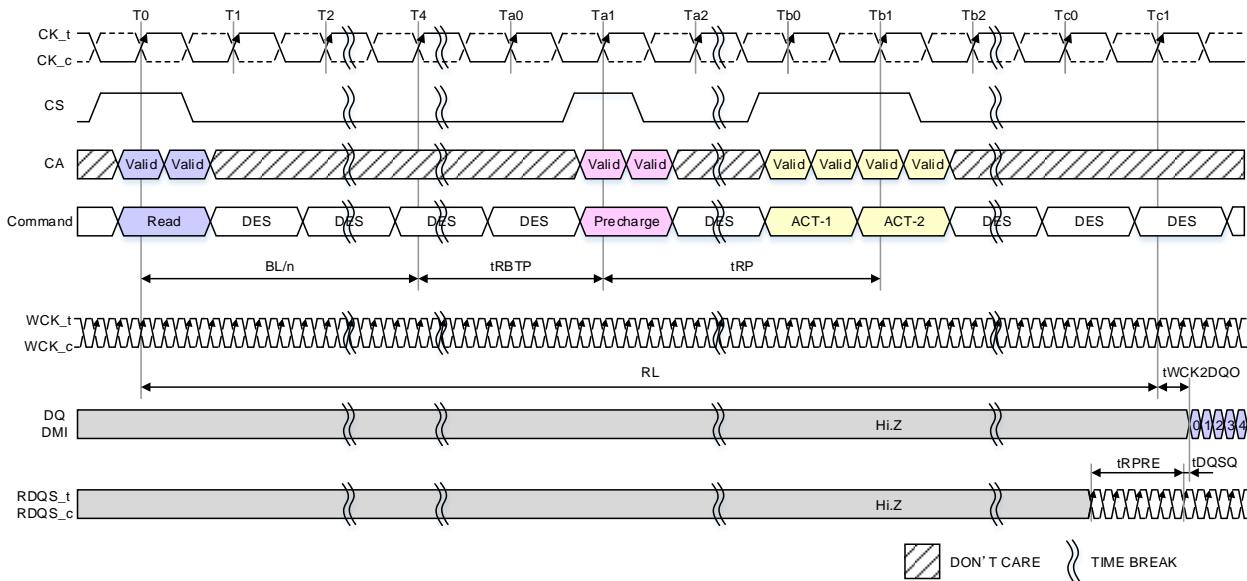


NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 82 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=16

7.3.2.1 Pre-Charge Operation (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 83 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=32

LPDDR5-SDRAM devices write data to the memory array in prefetch multiples. An internal Write operation can only begin after a prefetch group has been clocked, so tWR starts at the prefetch boundaries. The minimum Write-to-Precharge time for commands to the same bank is WL + BL/n + 1 + tWR clock cycles when bank organization is 16B mode. Refer to 8.1.1 for the command constraints table for other modes (BG and 8B mode).

7.3.2.1 Pre-Charge Operation (Cont'd)

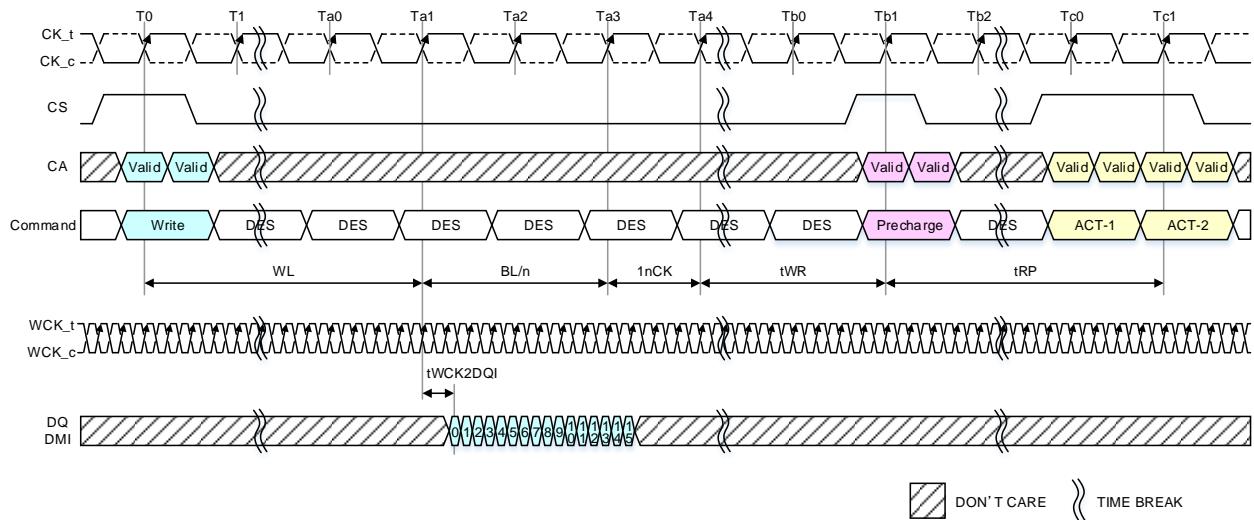


Figure 84 — Burst Write Followed by Precharge: 16B Mode, CKR = 4:1, BL=16

7.3.2.2 Auto-Precharge Operation

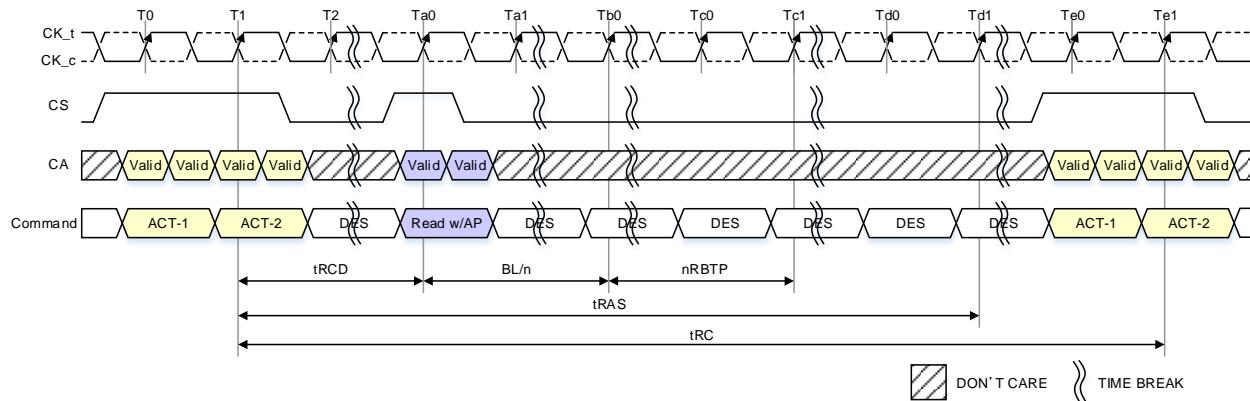
When a Read, Write, or Masked Write command is issued to the device, the AP bit (CA6) can be set to enable the activated bank to automatically begin Precharge at the earliest possible moment during the burst Read, Write or Masked Write cycle.

If AP is LOW when the Read, Write and Masked Write command is issued, then the normal Read, Write, or Masked Write burst operation is executed and the bank remains activated at the completion of the burst.

If AP is HIGH when the Read, Write, or Masked Write command is issued, the Auto-Precharge function is engaged. This feature enables the Precharge operation to be partially or completely hidden during burst Read cycles (dependent upon Read or Write latency), thus improving system performance for random data access. Read with Auto Precharge or Write/Mask Write with Auto Precharge commands may be issued after tRCD has been satisfied. The LPDDR5 SDRAM RAS Lockout feature will schedule the internal Precharge to assure that tRAS is satisfied.

tRC needs to be satisfied prior to issuing subsequent Activate commands to the same bank. Figure 85 shows example of RAS lock function.

7.3.2.2 Auto-Precharge Operation (Cont'd)

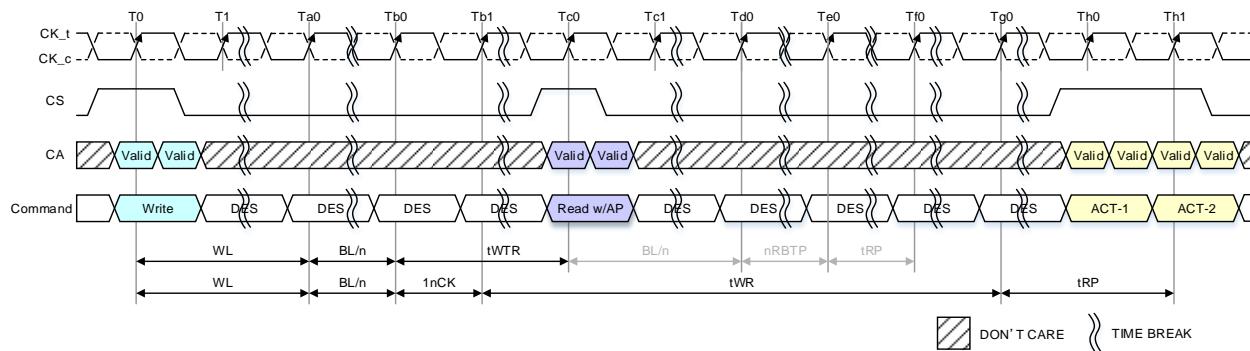


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 85 — Command Input Timing with RAS lock

7.3.2.2.1 Delay time from Write to Read with Auto Precharge

In the case of write command followed by Read with auto-Precharge, the controller must satisfy tWTR for the write command before initiating the SDRAM internal auto-Precharge. This means that ($tWTR + BL/n + nRBTP$) should be equal or longer than (tWR) when SDRAM bank organization is 16B. Refer to 8.1.1 for the command constraints table for other modes (BG and 8B mode). Refer to the following figure for details.



NOTE 1 tWTR starts at the rising edge of CK_t after WL + BL/n from Write command.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 86 — Delay time from Write to Read with Auto Precharge: 16B mode

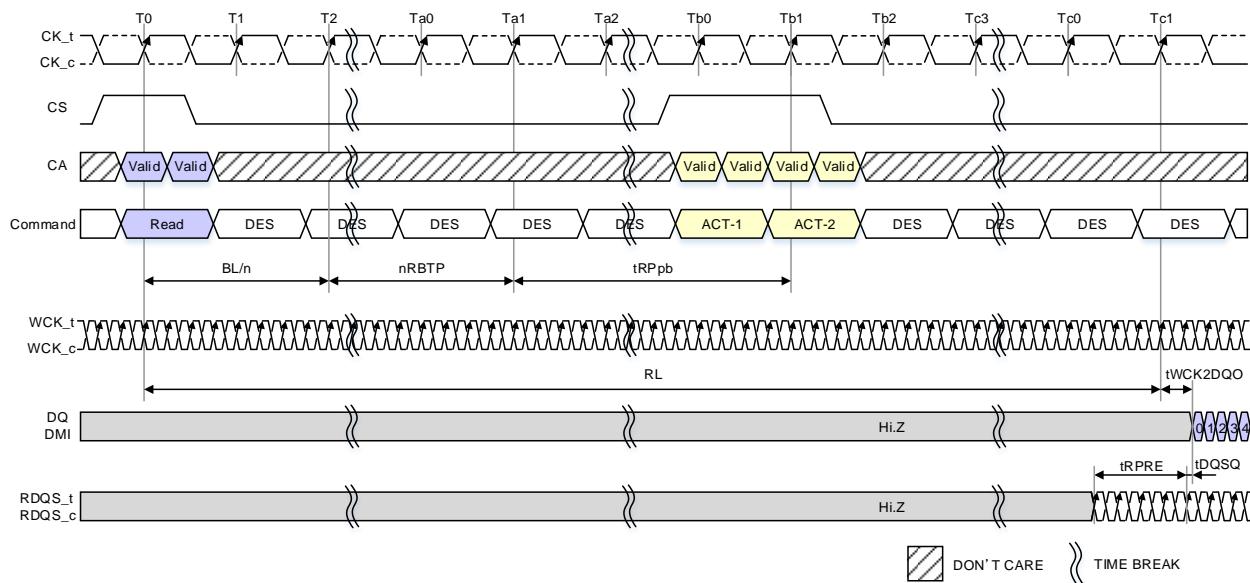
7.3.2.2.2 Burst Read with Auto-Precharge

If AP is HIGH when a Read command is issued, the Read with Auto-Precharge function is engaged. An internal Precharge procedure starts a following delay time after the Read command. The delay time depends on the bank organization.

Refer to 8.1.1 for the command constraints table for actual delay time from Read with Auto-Precharge.

For LPDDR5 Auto-Precharge calculations, see table 171. Following an Auto-Precharge operation, an Activate command can be issued to the same bank if the following two conditions are both satisfied:

- The RAS Precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge began, or
- The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

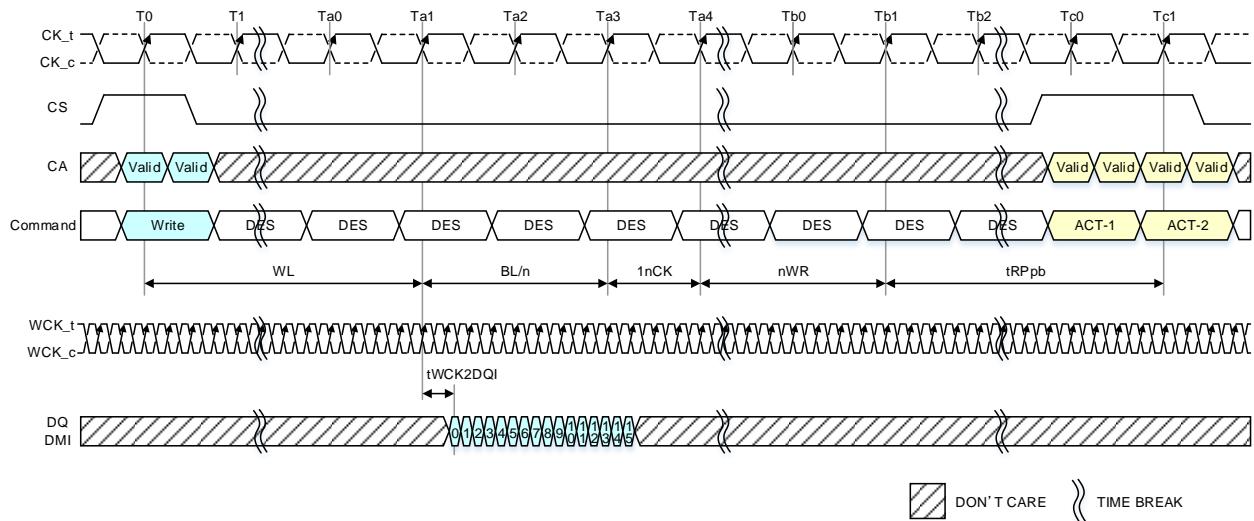
Figure 87 — Burst Read with Auto-Precharge: 16B mode

7.3.2.2.3 Burst Write with Auto-Precharge

If AP is HIGH when a Write command is issued, the Write with Auto-Precharge function is engaged. The device starts an Auto-Precharge on the rising edge nWR cycles after the completion of the Burst Write.

Following a Write with Auto-Precharge, an Activate command can be issued to the same bank if the following conditions are met:

- The RAS Precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge began, and
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 88 — Burst Write with Auto- Precharge: 16B mode

7.3.2.2.3 Burst Write with Auto-Precharge (Cont'd)

Table 171 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE) : DQ ODT is Disable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
READ BL=32 BG mode	PER BANK REFRESH (to same bank as Read)	illegal	-	
	ALL BANK REFRESH	illegal	-	
READ BL = 16 BG mode BL = 16 16Bank mode BL=32 8Bank mode	PER BANK REFRESH (to same bank as Read)	illegal	-	
	ALL BANK REFRESH	illegal	-	
WRITE BL=16 & 32	PER BANK REFRESH (to same bank as Write)	illegal	tCK	
	ALL BANK REFRESH	illegal	tCK	
MASK-WR BL = 16 BG mode BL = 16 16Bank mode BL=32 8Bank mode	PER BANK REFRESH (to same bank as MAK-WR)	illegal	tCK	
	ALL BANK REFRESH	illegal	tCK	

7.4 Read/Write Operation

7.4.1 Read and Write Access Operations

TBD

7.4.2 Read Preamble and Postamble

TBD

7.4.3 Burst Read Operation

An LPDDR5 SDRAM requires to be in auto-sync state WCK2CK synchronization state before the memory controller starting read DQ burst. For read operations, WCK must be driven at least tWCKPRE_Static+tWCKPRE_Toggle_RD before the read DQ burst. LPDDR5 will have a WCK post-amble of 0.5*tCK or TBD*tCK, after completing all read DQ burst.

7.4.3.1 Read Timing

A read command is initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table, **Table 154**. Read burst order is controlled by only one burst order bit, B3, at BL16 mode making the starting column burst address be a multiple of eight (ex. 0x0 or 0x8). The read latency (RL) is defined from the rising edge of the clock that starts a read command to the rising edge of the clock from which tWCKDQO is measured. The first valid data is available of RL * tCK + tWCK2CK + tWCKDQO after the clock rising edge of a read command. The DRAM controller WCK output is driven by DRAM controller tWCKPRE_Static+tWCKPRE_Toggle_RD before the first valid read data starts. The tWCKPRE_Static+tWCKPRE_Toggle_RD is dependent on operating frequency and the value is summarized in Table 158. The DQ-data is valid for tQW (DQ output window) and the controller must periodically train its internal capture clock to stay centered in the tQW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the controller on successive edges of WCK until the 16 or 32 bit data burst is complete. The WCK must remain active (toggling) for tWCKPST (WCK post-amble) after the completion of the burst read. After a burst READ operation, tRTP must be satisfied before a PRECHARGE command to the same bank can be issued. Pin timings are measured relative to the cross point of WCK_t and WCK_c.

7.4.3.1 Read Timing (Cont'd)

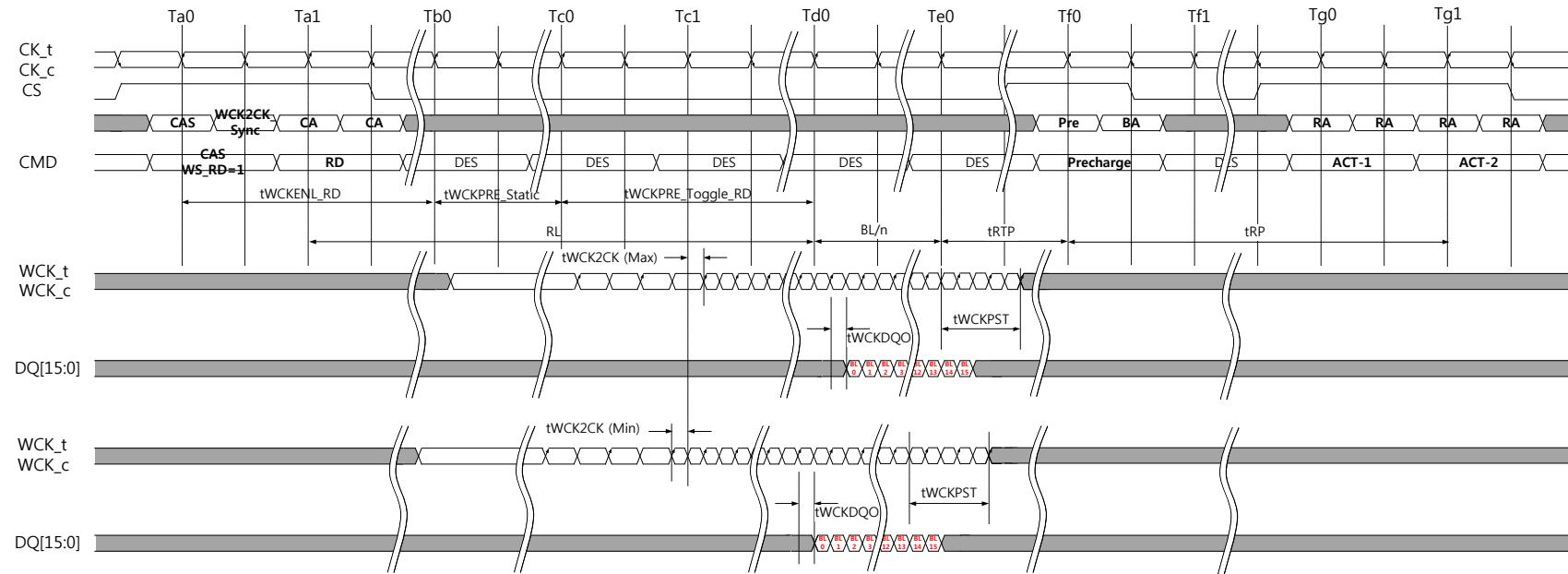


Figure 89 — Burst Read Operation

7.4.3.2 Read to Read Operation without additional WCK2CK-sync

Figure 90 shows timing diagram of back to back read operation with minimum tCCD. The CAS command with WCK2CK-sync is issued before the first read command, making the DRAM in auto-WCK2CK-sync state. Only one CAS command with WCK2CKsync before the first read command is required, because the WCK2CK-sync state continues until all the DQ burst completes.

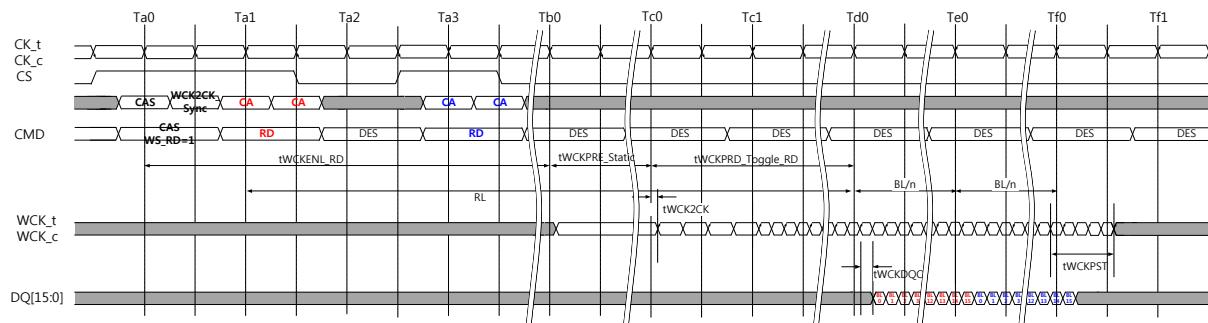


Figure 90 — Back to back read operation with tCCD(min) = 2tCK

When the command gap between two read commands is larger than $t_{CCD}(\min)$, a second read command can be issued without additional CAS command with WCK2CK-sync if the $t_{CCD} \leq RL + BL/8$. In **Figure 91**, if the second read command is given before Tf_0 , DRAM is still in WCK2CK-sync state, and additional CAS command with WCK2CK-sync is not required. To keep DRAM in WCK2CK-sync state, WCK is required to toggle at full-rate from Td_1 to Th_0+t_{WCKPST} . The second read command also extends the duration DRAM stays in WCK2CKsync by $RL+BL/8$. Therefore additional CAS command with WCK2CK-sync will not be required if another read command is given before Th_0 .

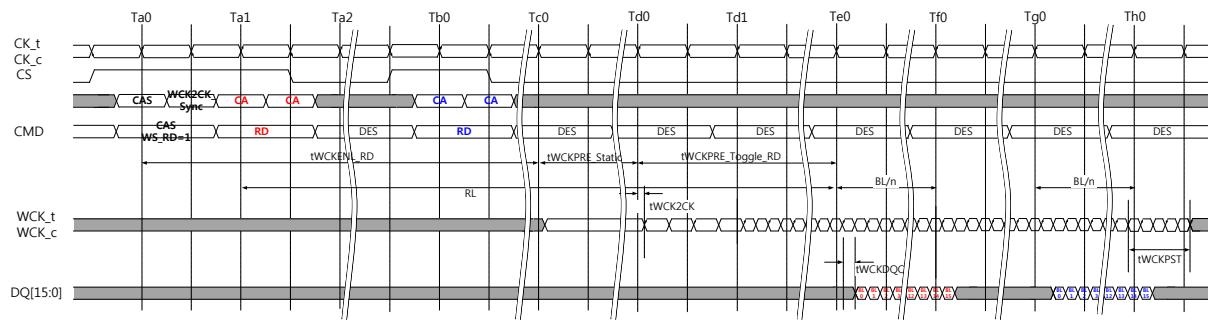


Figure 91 — Back to back read operation with $t_{CCD} \leq RL + BL/n$

7.4.3.3 Read to Read Operation with additional WCK2CK-sync

When command gap between two read commands is same or larger than $RL+BL/8+1$, a new WCK2CK-sync sequence is required. Figure 92 shows the case when the tCCD between two read commands are $RL+BL/8+1$. In this case a new CAS command with WCK2CK_Sync=1 at Td2 for next read command.

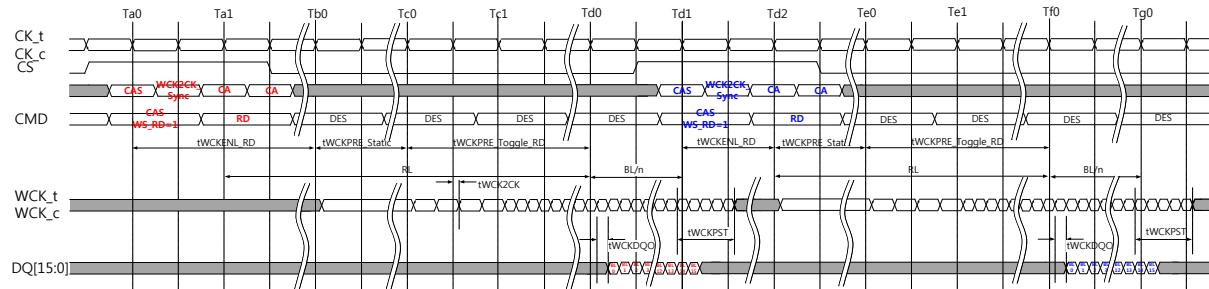


Figure 92 — Back to back read operation requiring a new WCK2CK-sync sequence

7.4.3.4 Read operation followed by write operation

If a write command following a read command is issued before $RL+BL/8$ from the previous command, WCK must keep toggle at its full-rate until the write DQ operation is completed and tWCKPST is satisfied. This case is shown in Figure 93.

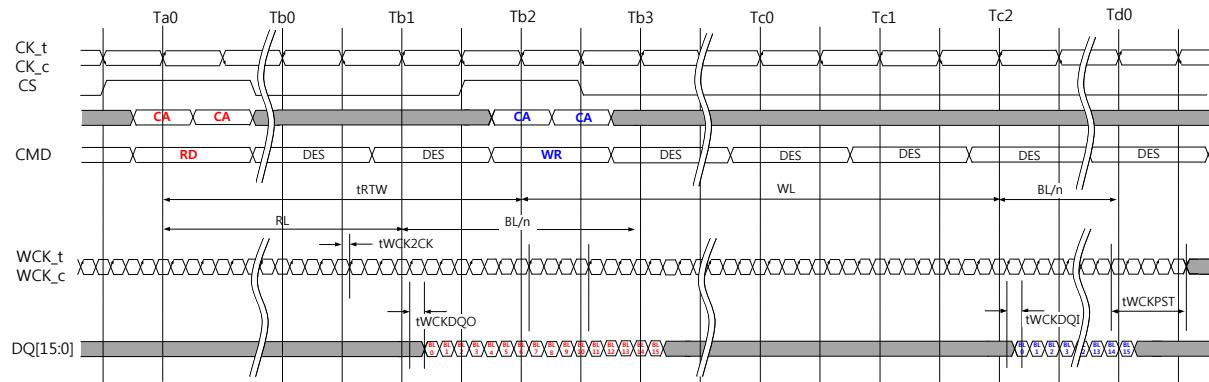


Figure 93 — Read operation followed by write operation without additional WCK2CK-sync sequence

However, an additional WCK2CK-sync sequence is required if the command gap is same or larger than $RL+BL/8$ because WCK2CK-sync state expires. In this case a CAS command with WCK2CK_Sync=1 must be given before the following write command as shown in Figure 94.

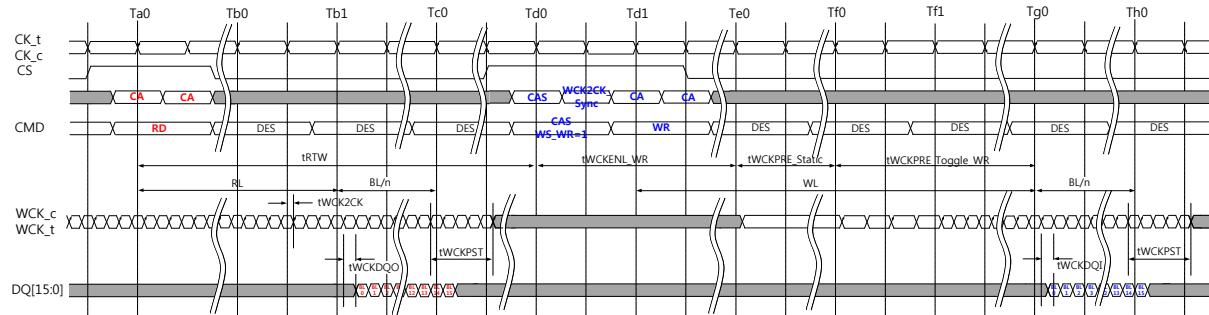


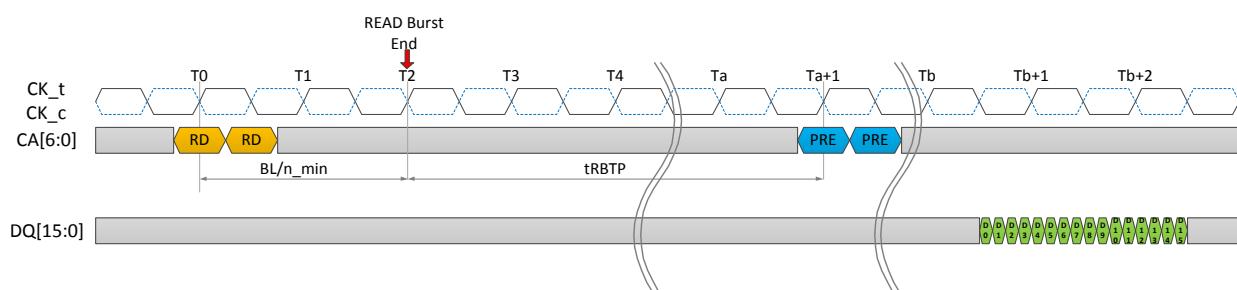
Figure 94 — Read operation followed by write operation with additional WCK2CK-sync sequence

7.4.4 READ Burst end to PRECHARGE Delay (tRBTP)

LPDDR5 device defines tRBTP as a delay from READ Burst end (BL/n_min from READ command) to a PRECHARGE command to specify the timing start point of tRBTP consistently over different Burst Length, WCK:CK ratio and Bank/BG mode setting.

Table 172 — Core Timing (tRBTP)

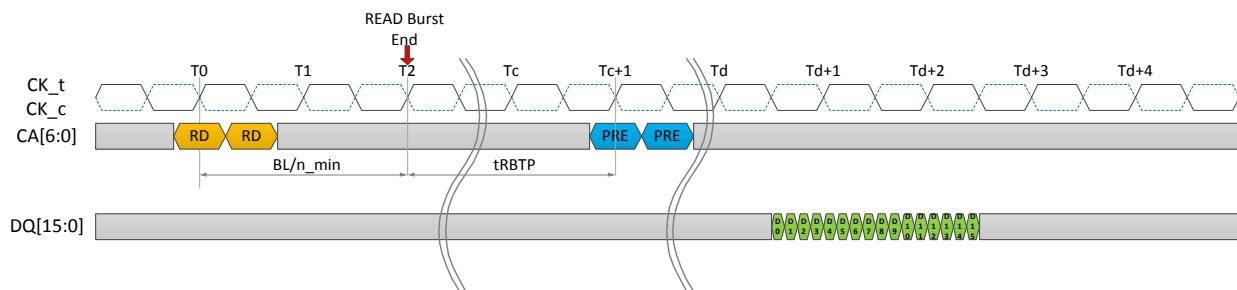
Parameter	Symbol	Min / Max	WCK:CK Ratio	WCK frequency (MHz)										Unit
				267	533	800	1067	1375	1600	1867	2134	2400	2750	
READ Burst end to PRECHARGE command delay	tRBTP	Min	2:1	Max(7.5ns, 4nCK) – 4nCK				N/A				ns		
			4:1	Max[7.5ns, 2nCK] – 2nCK										



NOTE 1 WCK:CK = 4:1, BL16, BG mode

NOTE 2 BL/n_min = 2*tCK (IO speed > 3200Mbps)

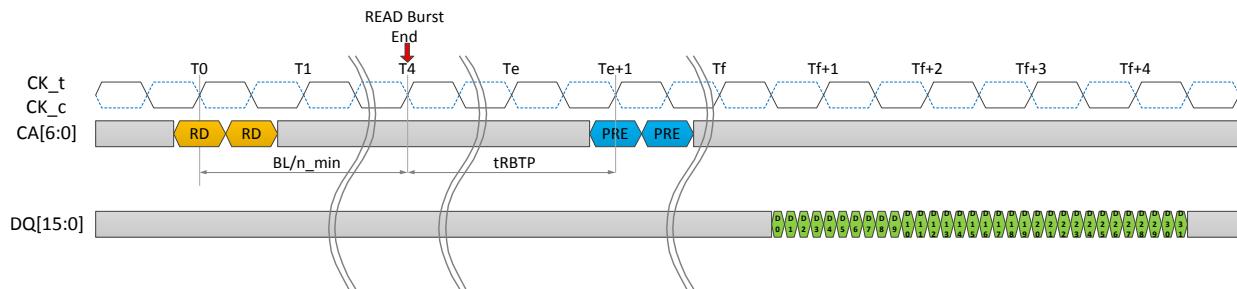
Figure 95 — Example of READ burst end to PRECHARGE command delay for same banks



NOTE 1 WCK:CK = 4:1, BL16, 16B mode

NOTE 2 BL/n_min = 2*tCK (IO speed ≤ 3200Mbps)

Figure 96 — Example of READ burst end to PRECHARGE command delay for same banks



NOTE 1 WCK:CK = 4:1, BL32, 8B mode

NOTE 2 BL/n_min = 4*tCK (IO speed > 3200Mbps)

Figure 97 — Example of READ burst end to PRECHARGE command delay for same banks

7.4.4 READ Burst end to PRECHARGE Delay (tRBTP) (Cont'd)

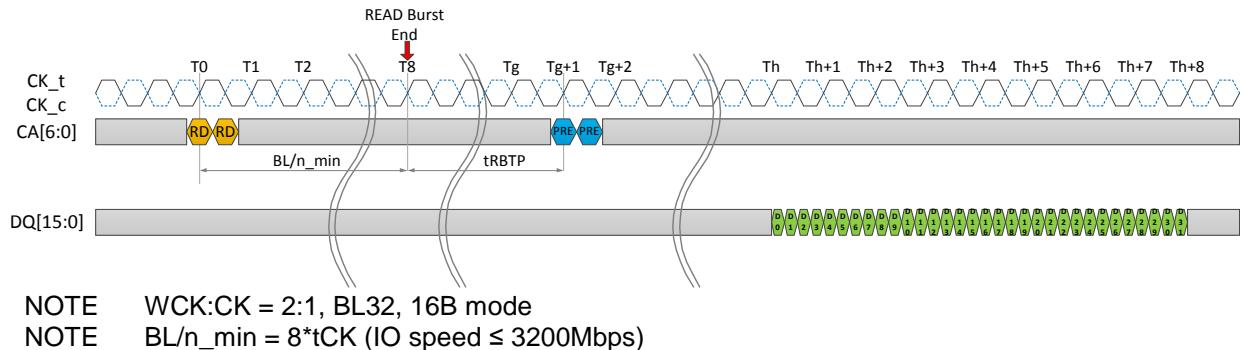


Figure 98 — Example of READ burst end to PRECHARGE command delay for same banks

7.4.5 RDQS Mode

For device operation at high clock frequencies, LPDDR5 may be set into RDQS mode in which a READ DATA STROBE (or a pair of READ DATA STROBE) will be sent on RDQS_c pin and RDQS_t pin along with the READ data. SoC will use a single-ended RDQS or a differential RDQS to latch the READ data.

7.4.5.1 RDQS Timing

Read timing with RDQS mode enabled is shown in **Figure 99**. Except the additional RDQS timing, all the timings are same as those of READ operation (7.4.3). RDQS-related parameters, tDQSQ, tRPRE and tRPST are defined in Table 173.

RDQS is assumed as a differential pair, RDQS_t and RDQS_c in **Figure 99**.

The read latency (RL) is defined from the rising edge of the clock that starts a read command to the rising edge of the clock from which tWCKDQO is measured. The first valid data is available for $RL * tCK + tWCK2CK + tWCKDQO$ after the clock rising edge of a read command.

The first latching edge of RDQS will start later than the first valid data with “tDQSQ” delay and tDQSQ is a known parameter in LPDDR4.

RDQS requires a pre-amble prior at the first latching edge (the rising edge of RDQS with the first valid data), and it requires a post-amble after the last latching edge. The pre-amble (tRPRE) and post-amble (tRPST) time lengths are defined as parameters can be set via mode register writes (MRW). tRPRE and tRPST are assumed 2tWCK in Figure 99, and the specific number is TBD.

7.4.5.1 RDQS Mode (Cont'd)

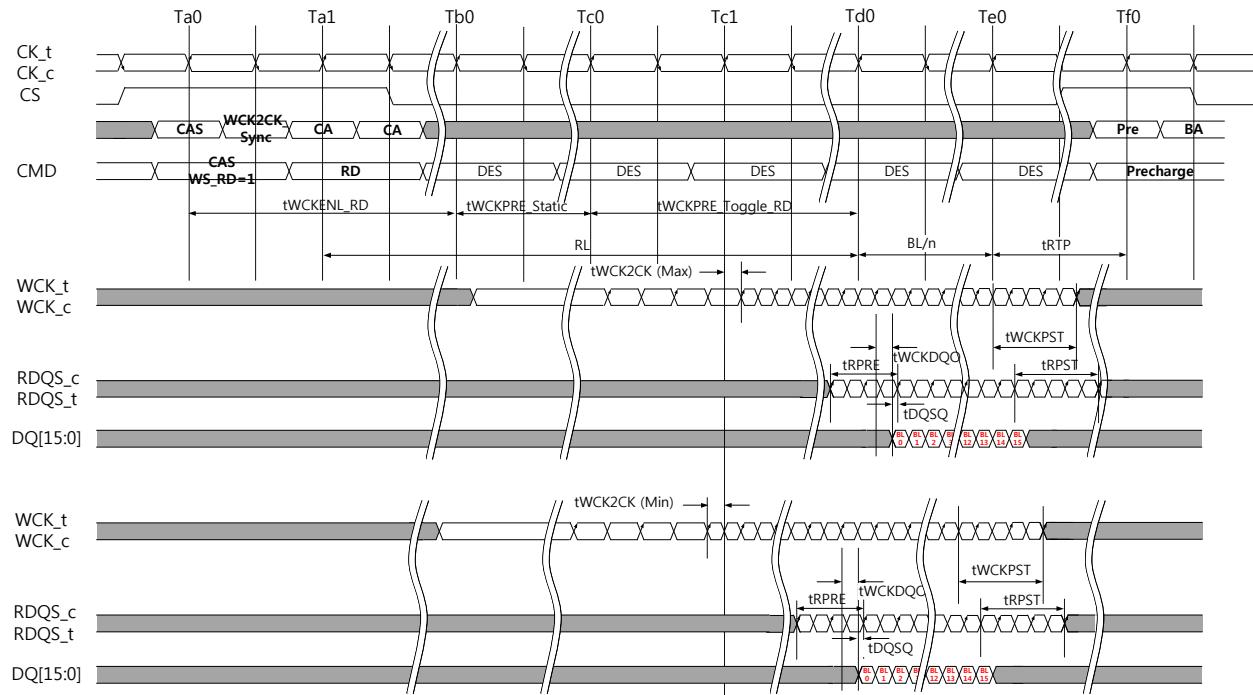


Figure 99 — Read timing with RDQS and related timing parameters

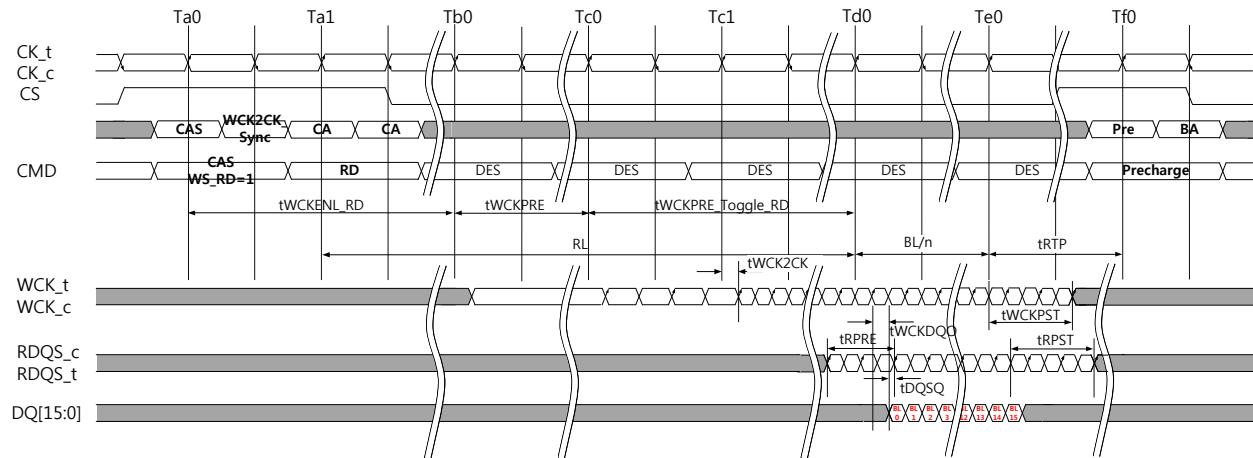
7.4.5.2 RDQS Related Functionalities

LPDDR5 supports both a single-ended RDQS and a differential RDQS to help SoC to optimize power and performance. RDQS configuration is selected via mode register writes (MRW).

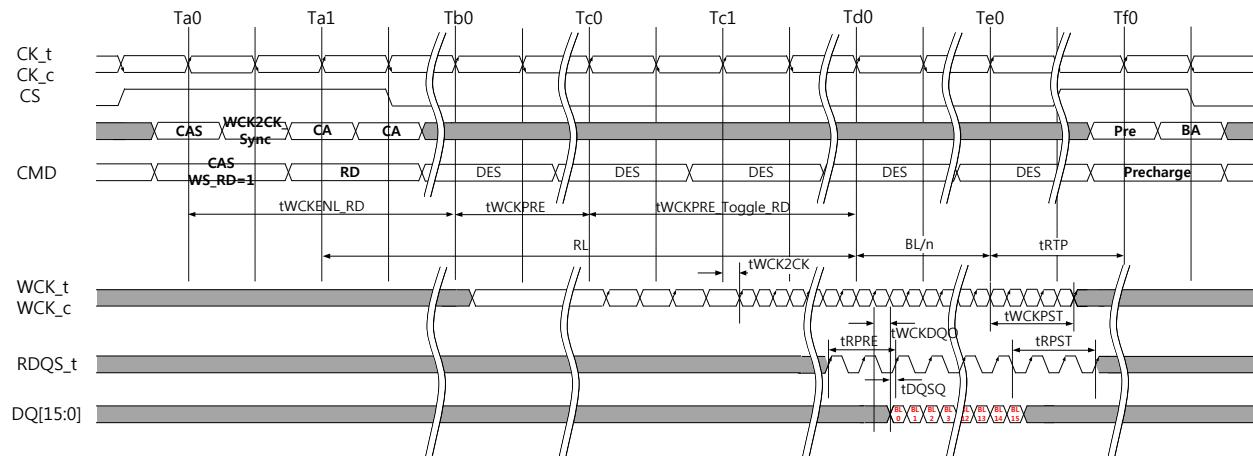
RDQS_t is used to send a read data strobe in a single-ended RDQS mode. RDQS_c and RDQS_t are used to send read data strobes in a differential RDQS mode.

The examples of RDQS settings are shown in **Figure 100**. There can be two cases as shown in Figure 100.

7.4.5.2 RDQS Related Functionalities (Cont'd)



CASE 1. Differential and Full-rate RDQS



CASE 2. Single-ended and Full-rate RDQS

Figure 100 — 4 All the possible types of RDQS

7.4.5.3 Mode Registers for RDQS

The length of RDQS pre-amble and post-amble can be determined by MR10 OP[4:7]. The specific number is TBD.

RDQS mode configuration can also be changed by MR20 OP[1:0]. When OP[1:0]=00 at MR20, RDQS mode will not be supported and SOC should latch the read data with its own internal clock. Single-ended RDQS mode and differential RDQS mode can be selected by setting OP[1:0] to 01, 10 and 11 each.

7.4.5.3 Mode Registers for RDQS (Cont'd)

Table 173 — RDQS Timing Parameters

Parameters	Symbol	Min/ Max	Value	Unit	Note
READ preamble	tRPRE	Min	TBD	tWCK	
READ postamble	tRPST	Min	TBD	tWCK	
RDQS_c low impedance time from CK_t, CK_c	tLZ(DQS)	Min	TBD	ps	
RDQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	Max	TBD	ps	
RDQS-DQ skew	tDQSQ	Max	TBD	ps	

7.4.5.4 RDQS Pattern Definition

LPDDR5 device requires MR20 OP[1:0] non zero to enable RDQS operation. The RDQS strobe provides a pre-amble pattern prior to the first latching edge (the rising edge of RDQS with data valid), and it also provides a post-amble pattern after the last latching edge. The pre-amble and post-amble length and type are set to MR10 via Mode Register Write commands. In Read to Read operations with BL/n, post-amble for 1st Read command and preamble for 2nd Read command will disappear to create consecutive RDQS latching edge for seamless burst operations. But in the case of Read to Read operations with command interval of BL/n + k*nCK, they will not completely disappear because it's not seamless burst operations. Timing diagrams and RDQS pattern definition tables in this material describe RDQS post-amble and pre-amble merging behavior in Read to Read operations with BL/n + k*nCK.

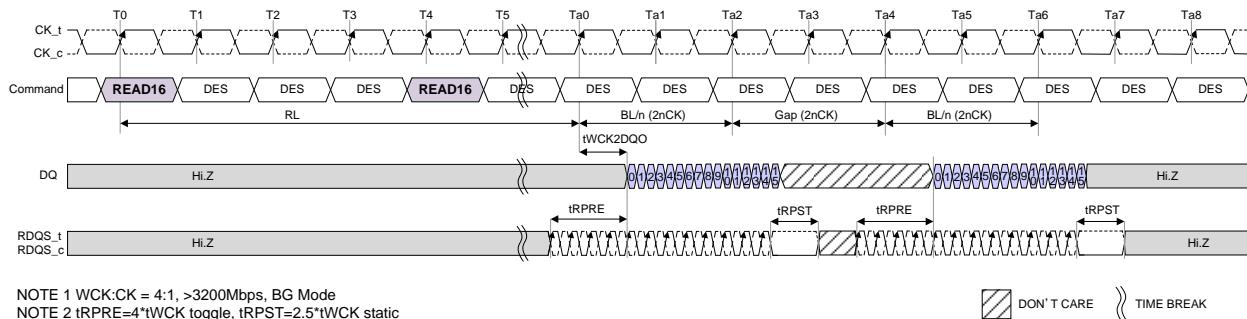


Figure 101 — READ16 to READ16 2nCK Gap Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK

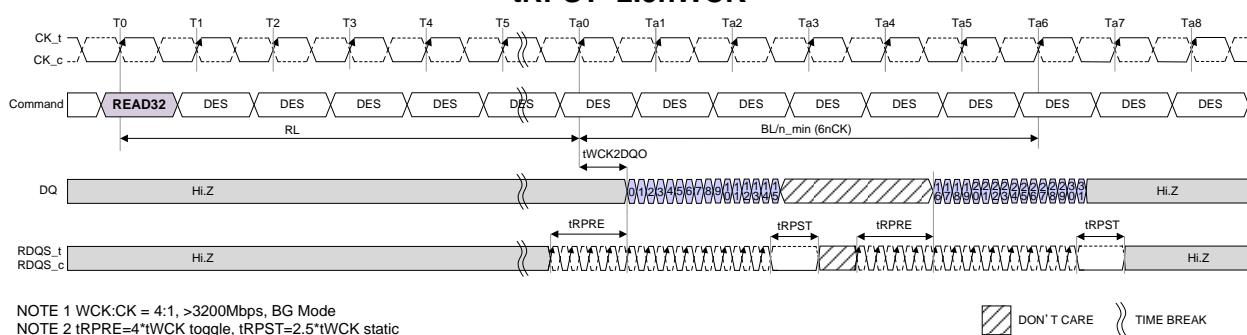


Figure 102 — BG Mode Read32 Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK

7.4.5.4 RDQS Pattern Definition (Cont'd)

Table 174 — RDQS Pattern Definition in case READ to READ command timing is BL/n + k*nCK (k=1, 2)

RDQS PST MR10 OP[0] & OP[7:6]	RDQS PRE MR10 OP[5:4]	1nCK(4nWCK) Gap WCK Cycle Number				2nCK(8nWCK) Gap WCK Cycle Number							
		1	2	3	4	1	2	3	4	5	6	7	8
		T	T	T	T	S	S	S	S	T	T	T	T
4.5*tWCK Static	tRDQS_PRE + 4*tWCK Toggle	T	T	T	T	S	S	S	S	T	T	T	T
	4*tWCK Toggle	T	T	T	T	S	S	S	S	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	S	S	T	T	S	S	S	S	S	S	T	T
	4*tWCK Static	S	S	S	S	S	S	S	S	S	S	S	S
2.5*tWCK Static	tRDQS_PRE + 4*tWCK Toggle	T	T	T	T	S	S	S	S	T	T	T	T
	4*tWCK Toggle	T	T	T	T	S	S	X	X	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	S	S	T	T	S	S	X	X	S	S	T	T
	4*tWCK Static	S	S	S	S	S	S	X	X	S	S	S	S
0.5*tWCK Static	tRDQS_PRE + 4*tWCK Toggle	T	T	T	T	X	X	S	S	T	T	T	T
	4*tWCK Toggle	T	T	T	T	X	X	X	X	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	S	S	T	T	X	X	X	X	S	S	T	T
	4*tWCK Static	S	S	S	S	X	X	X	X	S	S	S	S
4.5*tWCK Toggle	tRDQS_PRE + 4*tWCK Toggle	T	T	T	T	T	T	T	T	T	T	T	T
	4*tWCK Toggle	T	T	T	T	T	T	T	T	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	T	T	T	T	T	T	S	S	T	T
	4*tWCK Static	T	T	T	T	T	T	T	T	S	S	S	S
2.5*tWCK Toggle	tRDQS_PRE + 4*tWCK Toggle	T	T	T	T	T	T	S	S	T	T	T	T
	4*tWCK Toggle	T	T	T	T	T	T	X	X	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	T	T	T	T	X	X	S	S	T	T
	4*tWCK Static	T	T	S	S	T	T	X	X	S	S	S	S
0.5*tWCK Toggle	tRDQS_PRE + 4*tWCK Toggle	T	T	T	T	X	X	S	S	T	T	T	T
	4*tWCK Toggle	T	T	T	T	X	X	X	X	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	S	S	T	T	X	X	X	X	S	S	T	T
	4*tWCK Static	S	S	S	S	X	X	X	X	S	S	S	S

NOTE 1 RDQS pattern abbreviation: S(Static), T(Toggle), X(Don't Care).

NOTE 2 CKR(WCK:CK) is 4:1.

NOTE 3 MR10 OP[5:4]=11B (tRDQS_PRE + 4*tWCK Toggle) can be supported over 3200Mbps operation.

7.4.5.4 RDQS Pattern Definition (Cont'd)

Table 175 — RDQS Pattern Definition in case READ to READ command timing delay is $BL/n + k^*nCK$ ($k=1, 2, 3$)

RDQS PST MR10 OP[0] & OP[7:6]	RDQS PRE MR10 OP[5:4]	1nCK(2nWCK) Gap		2nCK(4nWCK) Gap				3nCK(6nWCK) Gap					
		WCK Cycle Number		WCK Cycle Number				WCK Cycle Number					
		1	2	1	2	3	4	1	2	3	4	5	6
4.5*tWCK Static	4*tWCK Toggle	T	T	T	T	T	T	S	S	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	S	S	T	T	S	S	S	S	T	T
	4*tWCK Static	S	S	S	S	S	S	S	S	S	S	S	S
2.5*tWCK Static	4*tWCK Toggle	T	T	T	T	T	T	S	S	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	S	S	T	T	S	S	S	S	T	T
	4*tWCK Static	S	S	S	S	S	S	S	S	S	S	S	S
0.5*tWCK Static	4*tWCK Toggle	T	T	T	T	T	T	X	X	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	S	S	T	T	X	X	S	S	T	T
	4*tWCK Static	S	S	S	S	S	S	X	X	S	S	S	S
4.5*tWCK Toggle	4*tWCK Toggle	T	T	T	T	T	T	T	T	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	T	T	T	T	T	T	T	T	T	T
	4*tWCK Static	T	T	T	T	T	T	T	T	T	T	S	S
2.5*tWCK Toggle	4*tWCK Toggle	T	T	T	T	T	T	T	T	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	T	T	T	T	T	T	S	S	T	T
	4*tWCK Static	T	T	T	T	S	S	T	T	S	S	S	S
0.5*tWCK Toggle	4*tWCK Toggle	T	T	T	T	T	T	X	X	T	T	T	T
	2*tWCK Static + 2*tWCK Toggle	T	T	S	S	T	T	X	X	S	S	T	T
	4*tWCK Static	S	S	S	S	S	S	X	X	S	S	S	S

NOTE 1 RDQS pattern abbreviation: S(Static), T(Toggle), X(Don't Care).

NOTE 2 CKR(WCK:CK) is 2:1.

7.4.6 Write Preamble and Postamble

TBD

7.4.7 Burst Write Operation

An LPDDR5 SDRAM requires being in WCK2CK synchronization state before the internal write operation starts. For WRITE operations, WCK must be driven at least $t_{WCKPRE_Static} + t_{WCKPRE_Toggle_WR}$ before the write DQ burst. LPDDR5 will have a WCK post-amble of $0.5 \cdot t_{CK}$ or TBD $\cdot t_{CK}$, after completing all write DQ burst.

7.4.7.1 Write Timing

A WRITE command is initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table (Table 154). LPDDR5 write command does not support burst ordering, so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the rising edge of the clock that starts a write command to the rising edge of the clock from which t_{WCKDQI} is measured. The first valid “latching” edge of WCK must be driven $WL \cdot t_{CK} + t_{WCK2CK}$ after the rising edge of clock that completes a write command. The LPDDR5-SDRAM uses an un-matched WCK-DQ path for lower power, so the WCK must arrive at the SDRAM ball prior to the DQ signal by the amount of t_{WCKDQI} . WCK is driven by DRAM controller $t_{WCKPRE_Static} + t_{WCKPRE_Toggle_WR}$ before the first valid rising strobe edge. The $t_{WCKPRE_Static} + t_{WCKPRE_Toggle_WR}$ dependent on operating frequency and the amount is summarized in Table 157. The WCK must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for t_{DIVW} (data input valid window) and the WCK must be periodically trained to stay centered in the t_{DIVW} window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of WCK until the 16 or 32 bit data burst is complete. The WCK must remain active (toggling) for t_{WCKPST} (WCK post-amble) after the completion of the burst WRITE. After a burst WRITE operation, t_{WR} must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of WCK_t and WCK_c .

7.4.7.1 Write Timing (Cont'd)

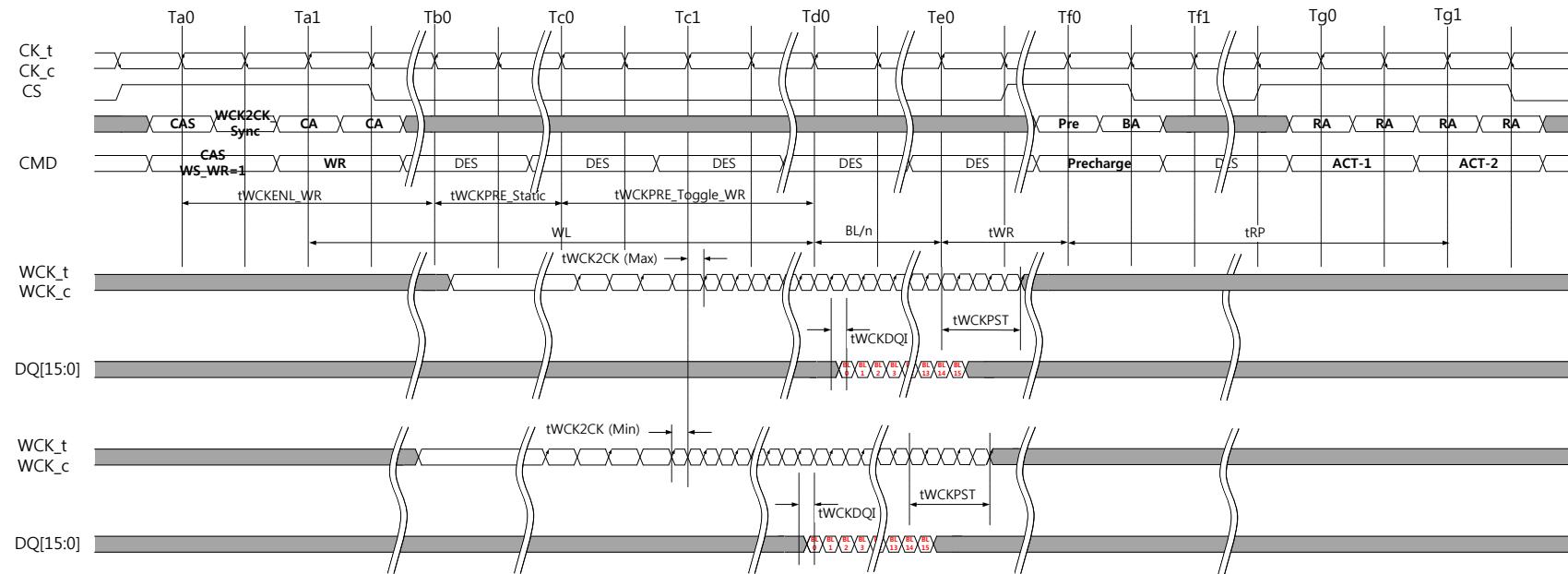


Figure 103 — Burst Write Operation

7.4.7.2 Write to Write Operation without additional WCK2CK-sync

Figure 104 shows timing diagram of back to back write operation with minimum tCCD. The CAS command with WCK2CK-sync is issued before the first write command, making the DRAM in WCK2CK-sync state. Only one CAS WCK2CK-sync command before the first write command is required, because the WCK2CK-sync state continues until all the DQ burst completes.

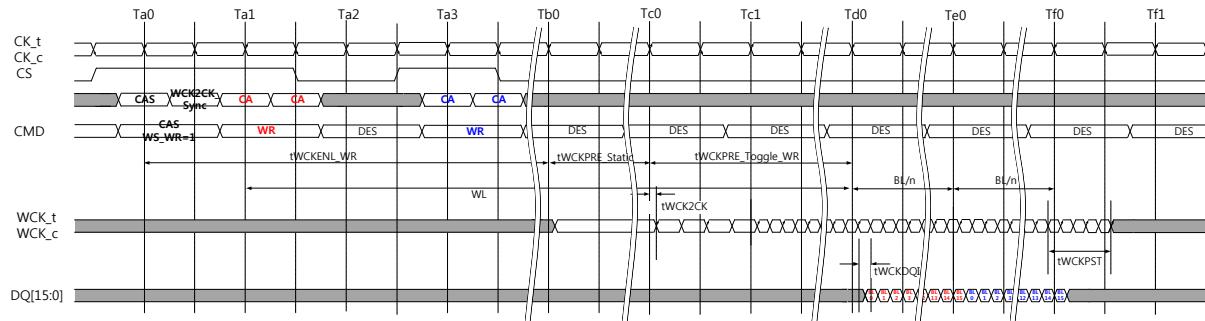


Figure 104 — Back to back write operation with tCCD(min) = 2tCK

When the command gap between two write commands is larger than tCCD(min), a second write command can be issued without additional WCK2CK-sync command if the $tCCD \leq WL + BL/n$ ($n=4$ at WCK:CLK=2:1, $n=8$ at WCK:CLK=4:1). In **Figure 105**, if the second write command is given before Tf0, DRAM is still in WCK2CK-sync state, and additional CAS command with WCK2CK-sync is not required. To keep DRAM in WCK2CK-sync state, WCK is required to toggle at full-rate from Td1 to Th0+tWCKPST. The second write command also extends the duration DRAM stays in WCK2CK-sync by $WL + BL/n$ ($n=4$ at WCK:CLK=2:1, $n=8$ at WCK:CLK=4:1). Therefore additional CAS command with WCK2CK-sync will not be required if another write command is given before Th0.

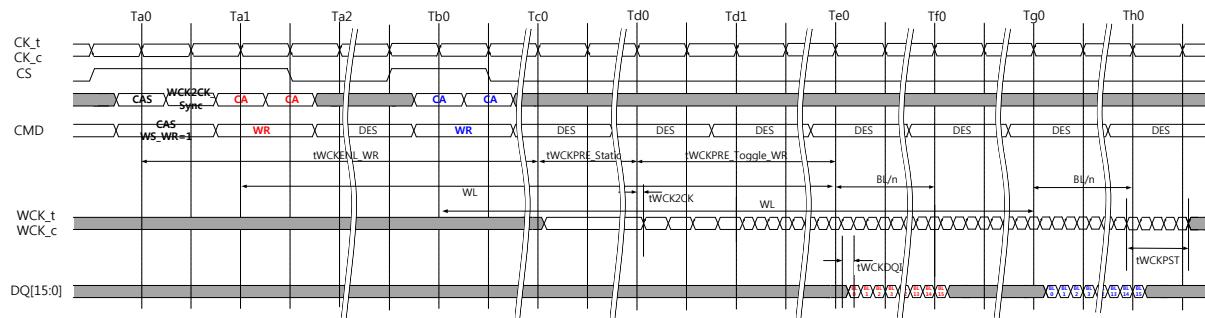


Figure 105 — Back to back write operation with tCCD ? WL + BL/n (n=4 at WCK:CLK=2:1, n=8 at WCK:CLK=4:1)

7.4.7.3 Write to Write Operation with additional WCK2CK-sync

When the command gap between two write commands is same or larger than $WL+BL/n + 1$ ($n=4$ at WCK:CLK=2:1, $n=8$ at WCK:CLK=4:1), a new WCK2CK synchronization sequence is required.

Figure 106 show the case when the tCCD between two write commands are $WL+BL/n + 1$ ($n=4$ at WCK:CLK=2:1, $n=8$ at WCK:CLK=4:1). In this case a new CAS command with WCK2CK_Sync=1 at Td1 for next write command.

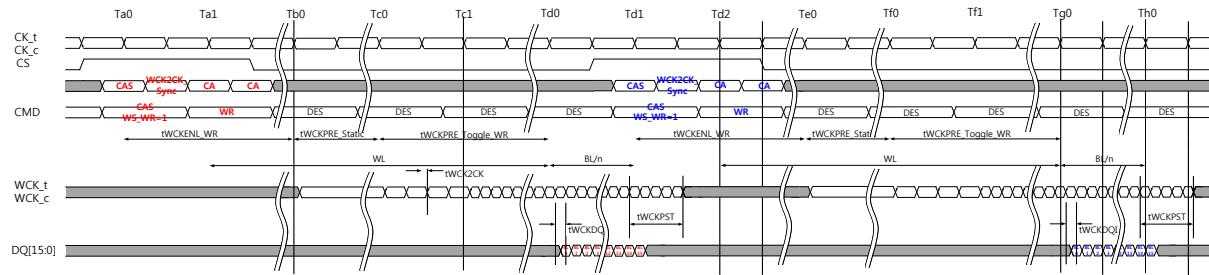


Figure 106 — Back to back write operation requiring a new WCK2CK-sync sequence

7.4.7.4 Write operation followed by read operation

When a read command follows a write command, the minimum gap between two commands is defined as $\min(tWTR)$. $tWTR$ is measured from the rising clock edge that satisfies $WL+BL/n$ ($n=4$ at WCK:CLK=2:1, $n=8$ at WCK:CLK=4:1), after a write command to the following read command. Therefore, an LPDDR5 DRAM always loses WCK2CK-sync information in write to read turn around, requiring a new WCK2CK synchronization sequence for the following write command. Figure 107 illustrates this case.

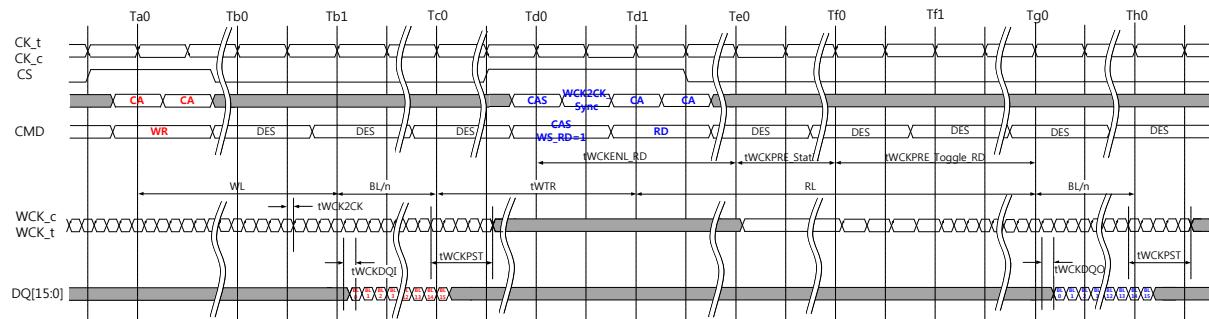


Figure 107 — Write operation followed by read operation

7.4.8 Read and Write Latency

7.4.8.1 Read and Read-to-Precharge Latencies

Latencies related to Read timing are measured from the rising edge of CK_t that begins the Read command. Latencies are specified separately for the DVFSC Disabled and DVFSC Enabled cases. For each MR2 OP[3:0] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

Table 176 — Read Latencies for Link ECC off case (DVFSC disabled)

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRBTP [nCK]
					Set 0	Set 1	Set 2	
40	533	2:1	10	133	6	6	6	0
	1067		133	267	8	8	8	0
	1600		267	400	10	10	12	0
	2133		400	533	12	14	14	0
	2750		533	688	16	16	18	2
	3200		688	800	18	20	20	2
40	533	4:1	5	67	3	3	3	0
	1067		67	133	4	4	4	0
	1600		133	200	5	5	6	0
	2133		200	267	6	7	7	0
	2750		267	344	8	8	9	1
	3200		344	400	9	10	10	1
	3733		400	467	10	11	12	2
	3733		467	533	12	13	14	2
	4267		533	600	13	14	15	3
	4800		600	688	15	16	17	4
	5500		688	750	16	17	19	4
	6000		750	800	17	18	20	4
	6400							

NOTE 1 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.

NOTE 2 The programmed value of nRBTP is the number of clock cycles the LPDDR5 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP(Auto Precharge). It is determined by RU(tRBTP/tCK).

NOTE 3 Some operating features can affect Read Latency:

Feature	Description
1	Byte Mode
2	Read DBI and/or Read Data Copy

RL Set 0 applies when no features are enabled.

RL Set 1 applies when one feature is enabled (1 or 2).

RL Set 2 applies when two features are enabled.

7.4.8.1 Read and Read-to-Precharge Latencies (Cont'd)

Table 177 — Read Latencies for Link ECC off case (DVFSC enabled)

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRBTP [nCK]
					Set 0	Set 1	Set 2	
40	533	2:1	10	133	6	6	6	0
533	1067		133	267	8	10	10	0
1067	1600		267	400	12	12	14	0
40	533	4:1	5	67	3	3	3	0
533	1067		67	133	4	5	5	0
1067	1600		133	200	6	6	7	0

NOTE 1 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.

NOTE 2 The programmed value of nRBTP is the number of clock cycles the LPDDR5 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP(Auto Precharge). It is determined by RU(tRBTP/tCK).

NOTE 3 Some operating features can affect Read Latency:

Feature	Description
1	Byte Mode
2	Read DBI and/or Read Data Copy

RL Set 0 applies when no features are enabled.

RL Set 1 applies when one feature is enabled (1 or 2).

RL Set 2 applies when two features are enabled.

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency		nRBTP [nCK]
					Set 0	Set 1	
3200	3733	4:1	400	467	12	13	2
3733	4267		467	533	13	14	2
4267	4800		533	600	15	16	3
4800	5500		600	688	17	18	4
5500	6000		688	750	18	20	4
6000	6400		750	800	19	21	4

NOTE 1 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.

NOTE 2 The programmed value of nRBTP is the number of clock cycles the LPDDR5 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP(Auto Precharge). It is determined by RU(tRBTP/tCK).

NOTE 3 RL Set 1 applies when the device is byte-mode.

7.4.8.2 Write Latency

Write latency is measured from the rising edge of CK_t that begins the Write command. Latencies are specified separately for the DVFSC Disabled and DVFSC Enabled cases. For each MR1 OP[7:4] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

7.4.8.2 Write Latency (Cont'd)

Table 178 — Write Latency: DVFSC Disabled

MR1 OP[7:4]	WCK:CK Ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WL		Unit
		Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	Set A	Set B	
0000	2:1	40	533	10	133	4	4	nCK
0001	2:1	533	1067	133	267	4	6	nCK
0010	2:1	1067	1600	267	400	6	8	nCK
0011	2:1	1600	2133	400	533	8	10	nCK
0100	2:1	2133	2750	533	688	8	14	nCK
0101	2:1	2750	3200	688	800	10	16	nCK
0000	4:1	40	533	5	67	2	2	nCK
0001	4:1	533	1067	67	133	2	3	nCK
0010	4:1	1067	1600	133	200	3	4	nCK
0011	4:1	1600	2133	200	267	4	5	nCK
0100	4:1	2133	2750	267	344	4	7	nCK
0101	4:1	2750	3200	344	400	5	8	nCK
0110	4:1	3200	3733	400	467	6	9	nCK
0111	4:1	3733	4267	467	533	6	11	nCK
1000	4:1	4267	4800	533	600	7	12	nCK
1001	4:1	4800	5500	600	688	8	14	nCK
1010	4:1	5500	6000	688	750	9	15	nCK
1011	4:1	6000	6400	750	800	9	16	nCK

NOTE 1 The Write Latency applies both x16 and x8 SDRAM.

NOTE 2 The Write latency applies regardless of the following function setting: (Disable/Enable)
Byte Mode, Write DBI, Write Data Copy and Link ECC.

NOTE 3 Write Latency Set "A" and Set "B" is determined by MR3 OP[5]. When MR3 OP[5]=0, then
Write Latency Set "A" should be used. When MR3 OP[5]=1, then Write Latency Set "B" should
be used.

Table 179 — Write Latency: DVFSC Enabled

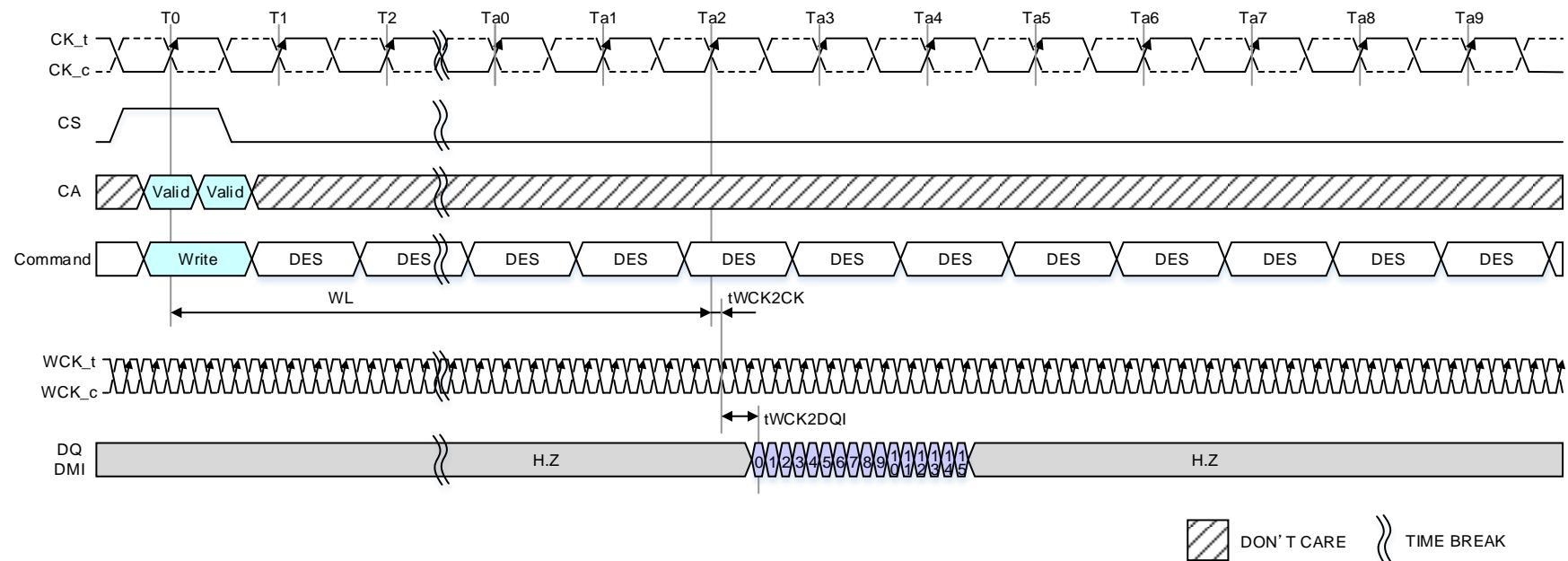
MR1 OP[7:4]	WCK:CK Ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WL		Unit
		Lower Limit (>)	Upper Limit (≤)	Lower Limit <th>Upper Limit (≤)</th> <th>Set A</th> <th>Set B</th> <th data-kind="ghost"></th>	Upper Limit (≤)	Set A	Set B	
0000	2:1	40	533	10	133	4	4	nCK
0001	2:1	533	1067	133	267	4	6	nCK
0010	2:1	1067	1600	267	400	6	8	nCK
0000	4:1	40	533	5	67	2	2	nCK
0001	4:1	533	1067	67	133	2	3	nCK
0010	4:1	1067	1600	133	200	3	4	nCK

NOTE 1 The Write Latency applies both x16 and x8 SDRAM.

NOTE 2 The Write latency applies regardless of the following function setting: (Disable/Enable)
Byte Mode, Write DBI, Write Data Copy and Link ECC.

NOTE 3 Write Latency Set "A" and Set "B" is determined by MR3 OP[5]. When MR3 OP[5]=0, then
Write Latency Set "A" should be used. When MR3 OP[5]=1, then Write Latency Set "B" should
be used.

7.4.8.2 Write Latency (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 108 — Write Latency Timing

7.4.8.3 Write Recovery time

Write Recovery time (nWR) is measured from the first rising edge of CK_t that occurs after the last latching edge of WCK. For each MR2 OP[7:4] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

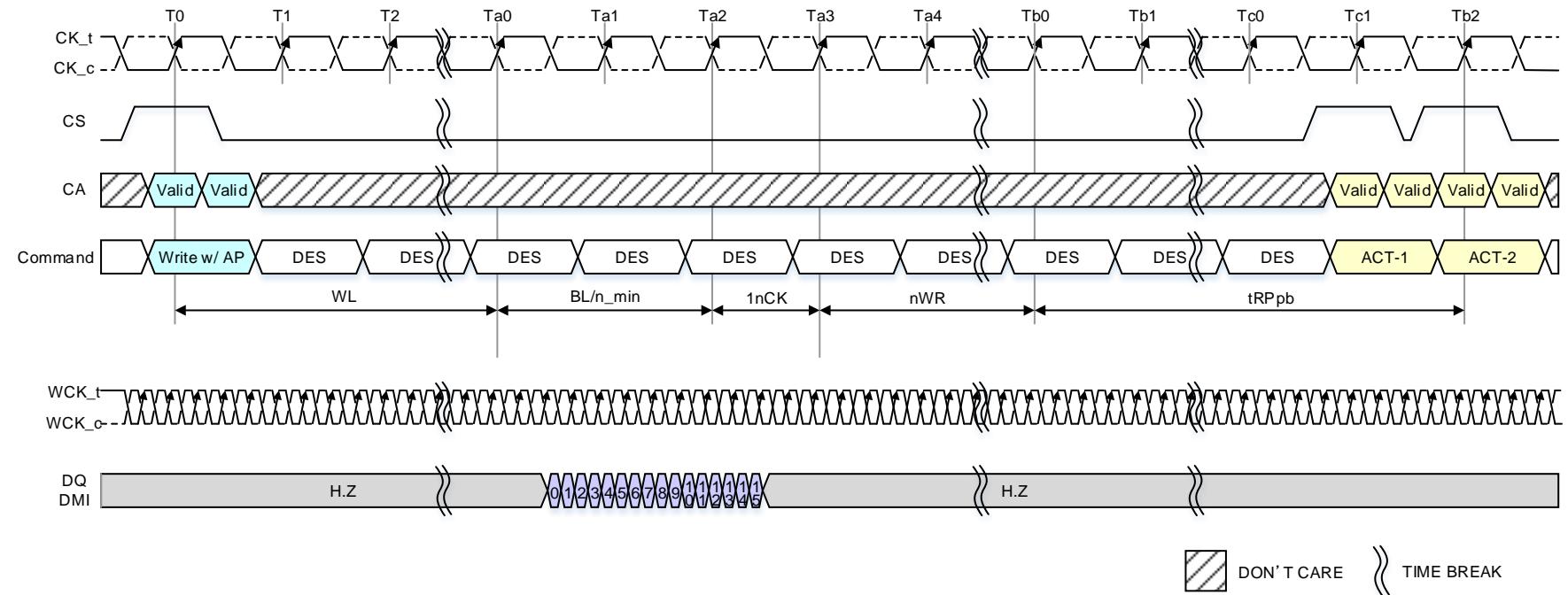
Table 180 — nWR Latency

MR2 OP[7:4]	WCK:CK Ratio	Data Rate Range [Mbps]		CK Frequency Range [MHz]		nWR						Unit
		Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	x16 w/o DVFS w/o Link ECC	x8 w/o DVFS w/o Link ECC	x16 w/o DVFS w Link ECC	x8 w/o DVFS w Link ECC	x16 w DVFS w/o Link ECC	x8 w DVFS w/o Link ECC	
0000	2:1	40	533	10	133	5	5	N/A	N/A	6	6	nCK
0001	2:1	533	1067	133	267	10	10	N/A	N/A	11	12	nCK
0010	2:1	1067	1600	267	400	14	15	N/A	N/A	17	18	nCK
0011	2:1	1600	2133	400	533	19	20	N/A	N/A	N/A	N/A	nCK
0100	2:1	2133	2750	533	688	24	25	N/A	N/A	N/A	N/A	nCK
0101	2:1	2750	3200	688	800	28	29	N/A	N/A	N/A	N/A	nCK
0000	4:1	40	533	5	67	3	3	N/A	N/A	3	3	nCK
0001	4:1	533	1067	67	133	5	5	N/A	N/A	6	6	nCK
0010	4:1	1067	1600	133	200	7	8	N/A	N/A	9	9	nCK
0011	4:1	1600	2133	200	267	10	10	N/A	N/A	N/A	N/A	nCK
0100	4:1	2133	2750	267	344	12	13	N/A	N/A	N/A	N/A	nCK
0101	4:1	2750	3200	344	400	14	15	N/A	N/A	N/A	N/A	nCK
0110	4:1	3200	3733	400	467	16	17	18	19	N/A	N/A	nCK
0111	4:1	3733	4267	467	533	19	20	21	22	N/A	N/A	nCK
1000	4:1	4267	4800	533	600	21	22	23	24	N/A	N/A	nCK
1001	4:1	4800	5500	600	688	24	25	27	28	N/A	N/A	nCK
1010	4:1	5500	6000	688	750	26	28	29	31	N/A	N/A	nCK
1011	4:1	6000	6400	750	800	28	29	31	32	N/A	N/A	nCK

NOTE 1 The LPDDR5 SDRAM should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each nWR value.

NOTE 2 The programmed value of nWR is the number of clock cycles the LPDDR5 SDRAM uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Precharge). It is determined by RU(tWR/tCK).

7.4.8.3 Write Recovery time (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 109 — Write Recovery Latency Timing

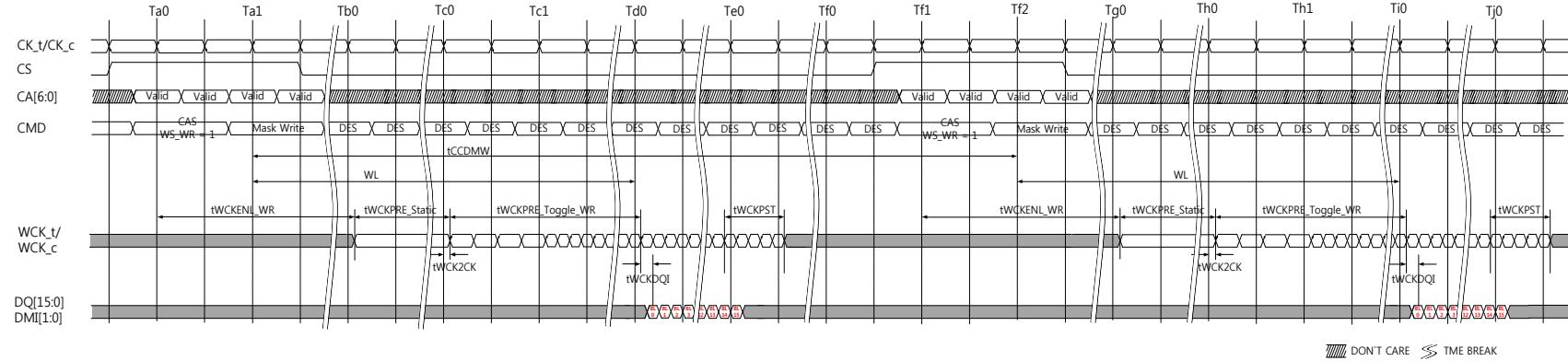
7.4.9 Masked Write

The LPDDR5 SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command. This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write command to the same banks in same bank-group cannot be issued until tCCDMW later, to allow the LPDDR5-SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See 7.4.10 for more information on the use of the DMI signal. Please refer to 8 for command timing constraints for each bank architecture timing. Table 181 is a description of tCCDMW following CKR and Bank mode.

Table 181 — tCCDMW

WCK:CK Ratio	Bank ORG	WCK frequency	tCCDMW
2:1	16B	$\leq 1600\text{Mhz}$	16^*tCK
	8B	$\leq 1600\text{Mhz}$	16^*tCK
4:1	16B	$\leq 1600\text{Mhz}$	8^*tCK
	BG Mode	$> 1600\text{Mhz}$	16^*tCK
	8B	Any freq.	16^*tCK

7.4.9 Masked Write (Cont'd)



NOTE 1 Masked Write command is only BL=16 in 4Bank/4BG or 16 Bank mode.

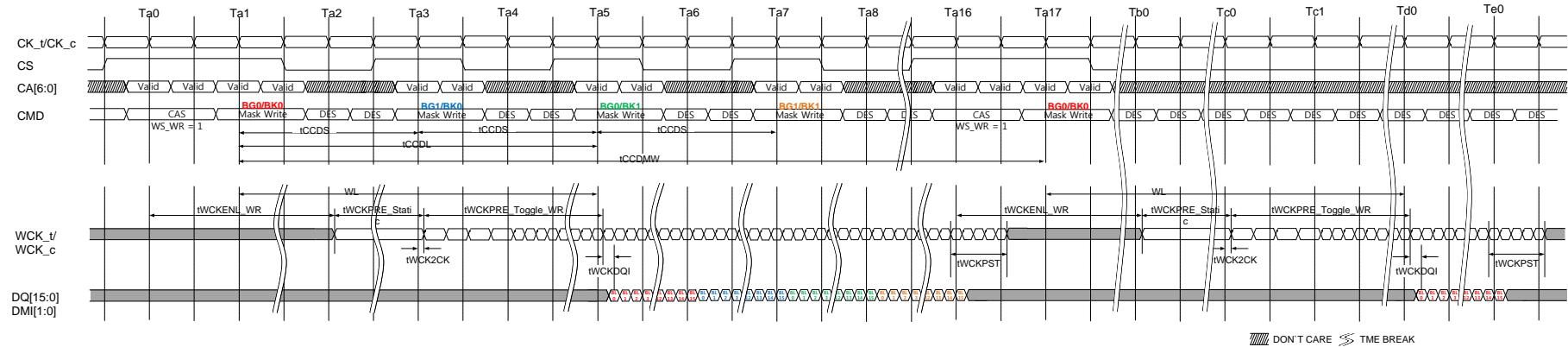
NOTE 2 In order to issue another Masked Write command to same bank without any other commands in between, new WCK2CK synchronization process may be required when $tCCDMW > WL + BL/n_{max}$ if DRAM is not in WCK free running mode.

NOTE 3 $tCCDMW = 16 \times tCK$ (4xtCCD_L) in 4Bank 4BG mode, and $8 \times tCK$ (4xtCCD) in 16 bank mode.

NOTE 4 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 110 — Masked Write Command – Same Bank Operation Timing without any other DQ operation commands in 4Bank/4BG or 16Bank mode

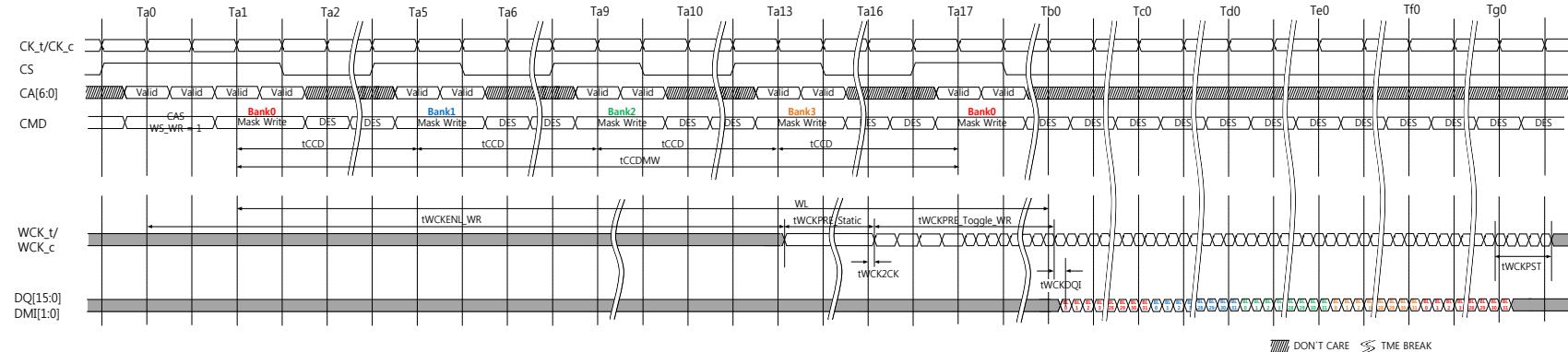
7.4.9 Masked Write (Cont'd)



- NOTE 1 Masked Write command is only BL=16 in 4Bank/4BG.
- NOTE 2 Masked Write command for different bank groups can be issued every after $t_{CCD_S}(2 \times t_{CK})$.
- NOTE 3 Masked Write command for different bank in same bank group can be issued every after $t_{CCD_L}(4 \times t_{CK})$.
- NOTE 4 Masked Write command for same bank in same bank group must be issued after $t_{CCDMW}(16 \times t_{CK})$.
- NOTE 5 DES commands are shown for ease of illustration; other commands may be valid at these times

Figure 111 — Masked Write Command – Different Bank Group Operation Timing in 4Bank/4BG mode

7.4.9 Masked Write (Cont'd)



NOTE 1 Masked Write command is only BL=32 in 8 bank mode.

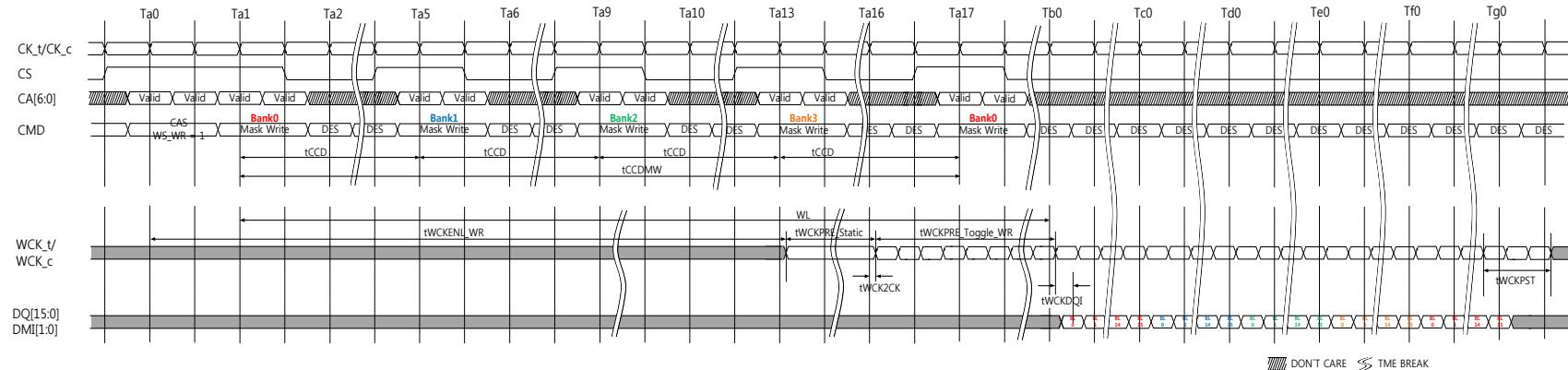
NOTE 2 Masked Write command for different bank can be issued every after tCCD(4 × tCK).

NOTE 3 Masked Write command for same bank must be issued after tCCDMW (16 × tCK).

NOTE 4 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 112 — Masked Write Command – Different Bank Operation Timing in 8-Bank Mode (BL32 only)

7.4.9 Masked Write (Cont'd)



- NOTE 1 Masked Write command is only BL=16 in 16 bank mode.
- NOTE 2 Masked Write command for different bank can be issued every after $t_{CCD}(4 \times t_{CK})$ (CKR=2:1).
- NOTE 3 Masked Write command for same bank must be issued after $t_{CCDMW} (16 \times t_{CK})$ (CKR=2:1).
- NOTE 4 DES commands are shown for ease of illustration; other commands may be valid at these time.

Figure 113 — Masked Write Command – 16 Bank Mode (WCK:CK = 2:1)

7.4.10 Data Mask (DM) and Data Bus Inversion (DBI-DC) Function

LPDDR5 SDRAM supports the function of Data Mask and Data Bus inversion. Its details are as follows:

- LPDDR5 device supports Data Mask (DM) function for Write operation.
- LPDDR5 device supports Data Bus Inversion (DBI-DC) function for Write and Read operation.
- LPDDR5 supports DM and DBI-DC function with a byte granularity.
- DBI-DC function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBI-DC function during Read can be enabled or disabled through MR3 OP[6].
- DM function during Masked Write can be enabled or disabled through MR13 OP[5].
- LPDDR5 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.
- DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

There are eight possible combinations for LPDDR5 device with DM and DBI-DC function. Table 182 describes the functional behavior for all combinations.

7.4.10.1 DMI Pin Behavior with Write Related Commands

Table 182 — DMI pin behavior by command and support function setting

Function				DMI Input Behavior		
Data Mask MR13 OP[5]	Write DBI MR3 OP[7]	Write Link ECC MR22 OP[4:5]	Write Data Copy MR21 OP[4]	Write CMD	Masked Write CMD	Write FIFO CMD
Disable	Disable	Disable	Disable	Receiver is turned off	Prohibited setting	Follows FIFO Definition
Disable	Disable	Disable	Enable	Receiver is turned off	Prohibited setting	Follows FIFO Definition
Disable	Disable	Enable	Disable	Receiver is turned off	Prohibited setting	Follows FIFO Definition
Disable	Disable	Enable	Enable	Receiver is turned off	Prohibited setting	Follows FIFO Definition
Disable	Enable	Disable	Disable	DBI data input	Prohibited setting	Follows FIFO Definition
Disable	Enable	Disable	Enable	Fixed low input when DC hit or DBI data input when DC miss	Prohibited setting	Follows FIFO Definition
Disable	Enable	Enable	Disable	DBI data input	Prohibited setting	Follows FIFO Definition
Disable	Enable	Enable	Enable	Fixed low input when DC hit or DBI data input when DC miss	Prohibited setting	Follows FIFO Definition
Enable	Disable	Disable	Disable	Fixed low input	DM data input	Follows FIFO Definition
Enable	Disable	Disable	Enable	Fixed low input	DM data input	Follows FIFO Definition
Enable	Disable	Enable	Disable	Fixed low input	DM data input	Follows FIFO Definition
Enable	Disable	Enable	Enable	Fixed low input	DM data input	Follows FIFO Definition
Enable	Enable	Disable	Disable	DBI data input	DM & DBI data input	Follows FIFO Definition
Enable	Enable	Disable	Enable	Fixed low input when DC hit or DBI data input when DC miss	DM & DBI data input	Follows FIFO Definition
Enable	Enable	Enable	Disable	DBI data input	DM & DBI data input	Follows FIFO Definition
Enable	Enable	Enable	Enable	Fixed low input when DC hit or DBI data input when DC miss	DM & DBI data input	Follows FIFO Definition

7.4.10.1 DMI Pin Behavior with Write Related Commands (Cont'd)

NOTE 1 Explanation of terminology in the cells.

- Receiver is turned off: The input level is shown in "don't" care in the timing diagram.
- Fixed low input: The input level is fixed to LOW.
- Follows FIFO Definition: DMI pin behavior follows WCK-DQ (FIFO) training definition. Data Mask, Write DBI and/or Write Link ECC functions are disabled regardless of MR setting. See 4.2.9 for more information on WCK-DQ.
- Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time.
- Valid data input: High or low input is required. These data are not required to have any meaning.
- DBI data input: DMI signal is treated as DBI signal and it indicates whether DRAM needs to invert the Write data received on DQs within a byte. The LPDDR5 device inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW. Total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively), the Write data received on the DQ inputs, should less than or equal to four during Write DBI is enabled.
- DM data input: The LPDDR5 DRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, DRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR5 DRAM does not perform mask operation and data received on DQ input is written to the array.
- DM&DBI data input: The LPDDR5 DRAM requires an explicit Masked Write command for all masked write operations. The LPDDR5 device masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR5 DRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.

NOTE 2 When both DM and Write Data copy is enabled, the low level is required to be to input to DMI when Write with Data Copy command is issued regardless Data Copy (DC) miss hit selection.

NOTE 3 Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.

7.4.10.2 DMI Pin Behavior with Read Related Commands

Table 183 — DMI pin behavior by command and support function setting

Function			DMI Output Behavior			
Read DBI MR3 OP[6]	Read Link ECC MR22 OP[7:6]	Read Data Copy MR21 OP[5]	Read	Read FIFO	Mode Register Read	Read DQ Calibration
Disable	Disable	Disable	Driver is turned off	Follows FIFO Definition	Driver is turned off	Driver is turned off
Disable	Disable	Enable	Follows Data Copy Definition	Follows FIFO Definition	Valid data output	Follows RDC Definition
Disable	Enable	Disable	Follows Link ECC Definition	Follows FIFO Definition	Valid data output	Follows RDC Definition
Disable	Enable	Enable	Prohibited setting	Prohibited setting	Prohibited setting	Prohibited setting
Enable	Disable	Disable	DBI data output	Follows FIFO Definition	Fixed low output	Follows RDC Definition
Enable	Disable	Enable	Follows Data Copy Definition	Follows FIFO Definition	Fixed low output	Follows RDC Definition
Enable	Enable	Disable	Prohibited setting	Prohibited setting	Prohibited setting	Prohibited setting
Enable	Enable	Enable	Prohibited setting	Prohibited setting	Prohibited setting	Prohibited setting

NOTE 1 Explanation of terminology in the cells.

- Follows FIFO Definition: DMI pin behavior follows WCK-DQ (FIFO) training definition. Read DBI, Read Link ECC and/or Read Data Copy functions are disabled regardless of MR setting. See WCK-DQ (0) for detail.
- Follows Data Copy Definition: DMI pin behavior follows Data Copy definition. See Data Copy (7.7.2) for detail.
- Follows Link ECC Definition: DMI pin behavior follows Link ECC definition. See Link ECC (7.7.7) for detail.
- Follows RDC Definition: DMI pin behavior follows RDC definition. Read DBI, Read Link ECC and/or Read Data Copy functions are disabled regardless of MR setting. See RDC (4.2.8) for detail.
- Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time.
- Valid data output: High or low data is outputted. And these output data are meaningless.
- Fixed low output: The output level is fixed to LOW
- DBI data output: The LPDDR5 DRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.

7.5 Refresh operation

7.5.1 Refresh command

The REFRESH command is initiated with CS HIGH, CA[2:0] LOW, CA[5:3] HIGH, CA6 LOW at the rising edge of the clock. Per-bank REFRESH is initiated with CA6 LOW at the falling edge of the clock. All-bank REFRESH is initiated with CA6 HIGH at the falling edge of the clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1, and CA2 at the falling edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and Bank address BA2 is transferred on CA2. Bank address BA3 is transferred on CA3 additionally “don’t care” for 4bank/4BG and 16bank mode, and then per-bank REFRESH is performed to 2 banks simultaneously.

Example for 4Bank/4BG mode or 16Bank mode - A per-bank REFRESH command (REFpb) to the 16 banks can be issued in any order. e.g., REFpb commands may be issued in the following order: (1,9)-(5,13)-(0,8)-(2,10)-(6,14)-(7,15)-(3,11)-(4,12). After the 16 banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g., REFpb commands are issued in the following order that is different from the previous order:

(7,15)-(3,11)-(2,10)-(4,12)-(6,14)-(0,8)-(1,9)-(5,13). One of the possible order can also be a sequential round robin: (0,8)-(1,9)-(2,10)-(3,11)-(4,12)-(5,13)-(6,14)-(7,15). It is illegal to send a per-bank REFRESH command to the same bank unless all 16 banks have been refreshed using the per-bank REFRESH command. The count of 8 REFpb commands starts with the first REFpb command after a synchronization event.

Example for 8Bank mode - A per-bank REFRESH command (REFpb) to the 8-Banks can be issued in any order. e.g., REFpb commands may be issued in the following order: 1-0-2-7-6-3-4-5. After the 8-Banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g., REFpb commands are issued in the following order that is different from the previous order: 7-3-4-2-6-0-1-5. One of the possible order can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all 8-Banks have been refreshed using the per-bank REFRESH command. The count of 8 REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET_n or at every exit from self-refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in self-refresh or a REFab command can be issued at any time without cycling through all banks using per-bank REFRESH command. After the bank count is synchronized to zero, the controller can issue per-bank REFRESH commands in any order as described in the previous paragraph.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the DRAM will perform refreshes to all banks as indicated by the row counter. If another refresh command (REFab or REFpb) is issued after the REFab command, then it uses an incremented value of the row counter. Table 184 for 4bank/4BG mode or 16Bank mode, Table 185 for 8bank mode show examples of both bank and refresh counter increment behavior.

7.5.1 Refresh command (Cont'd)

Table 184 — Bank and Refresh counter increment behavior on the 4Bank/4BG mode or 16Bank mode

#	SUB #	Command	BG1	BG0	BA1	BA0	Refresh Bank #	Bank Counter #	Ref Counter # (Row Address #)	
0	0	Reset, SRX or REFab						To 0		
1	1	REFpb	X	0	0	0	0/8	0 to 1	n	
2	2	REFpb	X	0	0	1	1/9	1 to 2		
3	3	REFpb	X	0	1	0	2/10	2 to 3		
4	4	REFpb	X	0	1	1	3/11	3 to 4		
5	5	REFpb	X	1	0	0	4/12	4 to 5		
6	6	REFpb	X	1	0	1	5/13	5 to 6		
7	7	REFpb	X	1	1	0	6/14	6 to 7		
8	8	REFpb	X	1	1	1	7/15	7 to 0		
9	1	REFpb	X	1	1	0	6/14	0 to 1		
10	2	REFpb	X	1	1	1	7/15	1 to 2		
•										
•										
•										
15	7	REFpb	X	0	0	0	0/8	6 to 7	n+1	
16	8	REFpb	X	1	0	0	4/12	7 to 0		
17	1	REFpb	X	0	0	0	0/8	0 to 1		
18	2	REFpb	X	0	0	1	1/9	1 to 2	n+2	
19	3	REFpb	X	0	1	0	2/10	2 to 3		
20	0	REFab	V	V	V	V	0~15	To 0		
21	1	REFpb	X	0	1	0	2/10	0 to 1	n+3	
22	2	REFpb	X	1	0	1	5/13	1 to 2		

7.5.1 Refresh command (Cont'd)

Table 185 — Bank and Refresh counter increment behavior on the 8bank mode

#	SUB #	Command	BA2	BA1	BA0	Refresh Bank #	Bank Counter #	Ref Counter # (Row Address #)
0	0	Reset, SRX or REFab						To 0
1	1	REFpb	0	0	0	0	0 to 1	n
2	2	REFpb	0	0	1	1	1 to 2	
3	3	REFpb	0	1	0	2	2 to 3	
4	4	REFpb	0	1	1	3	3 to 4	
5	5	REFpb	1	0	0	4	4 to 5	
6	6	REFpb	1	0	1	5	5 to 6	
7	7	REFpb	1	1	0	6	6 to 7	
8	8	REFpb	1	1	1	7	7 to 0	
9	1	REFpb	1	1	0	6	0 to 1	n+1
10	2	REFpb	1	1	1	7	1 to 2	
• • •								
15	7	REFpb	0	0	0	0	6 to 7	n+1
16	8	REFpb	1	0	0	4	7 to 0	
17	1	REFpb	0	0	0	0	0 to 1	n+2
18	2	REFpb	0	0	1	1	1 to 2	
19	3	REFpb	0	1	0	2	2 to 3	
20	0	REFab	V	V	V	0~7	To 0	n+2
21	1	REFpb	0	1	0	2	0 to 1	n+3
22	2	REFpb	1	0	1	5	1 to 2	
Snip								

A bank must be idle before it can be refreshed. The controller must track the bank(or bank pair in the case of BG mode and 16bank mode) being refreshed by the per-bank REFRESH command. The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command.
- tpbR2pbR has been satisfied after the prior REFpb command.
- tRP has been satisfied after the prior PRECHARGE command to that bank.
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank or bank pair is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks not being refreshed within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the non-refreshing banks can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank or bank pair will be in the idle state.

7.5.1 Refresh command (Cont'd)

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command.
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank or bank pair.
- tpbr2act must be satisfied before issuing an ACTIVATE command to a different non-refreshing bank.
- tpbR2pbR must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command.
- tRFCpb has been satisfied following the prior REFpb command.
- tRP has been satisfied following the prior PRECHARGE command.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command.
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Table 186 — REFRESH Command Scheduling Separation requirements for 4Bank /4BG mode or 16Bank mode

Symbol	Minimum Delay From	To	Note
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate command to same bank as REFpb	
tpbr2act	REFpb	Activate command to different bank than REFpb	
tRRD_S	Activate	REFpb to different bank group than prior Activate command	1
		Activate command to different bank group than prior Activate command	
tRRD_L	Activate	REFpb in same bank group	1
		Activate command to different bank than prior Activate command in same bank group	
tpbR2pbR	REFpb	REFpb	

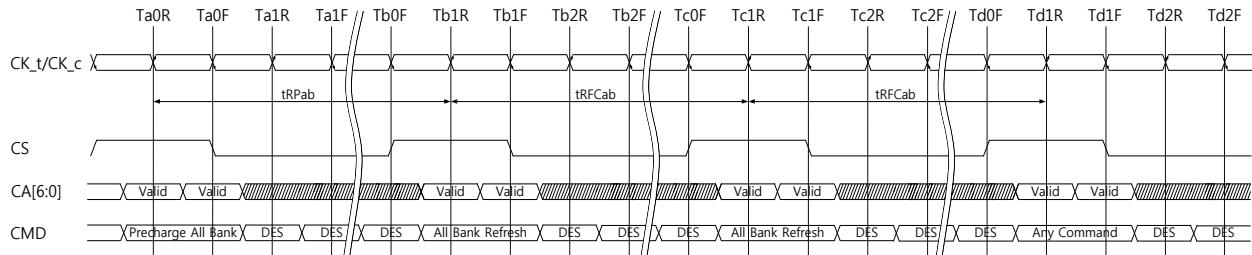
NOTE A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

7.5.1 Refresh command (Cont'd)

Table 187 — REFRESH Command Scheduling Separation requirements for 8Bank mode

Symbol	Minimum Delay From	To	Note
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate command to same bank as REFpb	
tpbr2act	REFpb	Activate command to different bank than REFpb	
tRRD	REFpb	Activate command to different bank than REFpb	
	Activate	REFpb	1
		Activate command to different bank than prior Activate command	
tpbR2pbR	REFpb	REFpb	

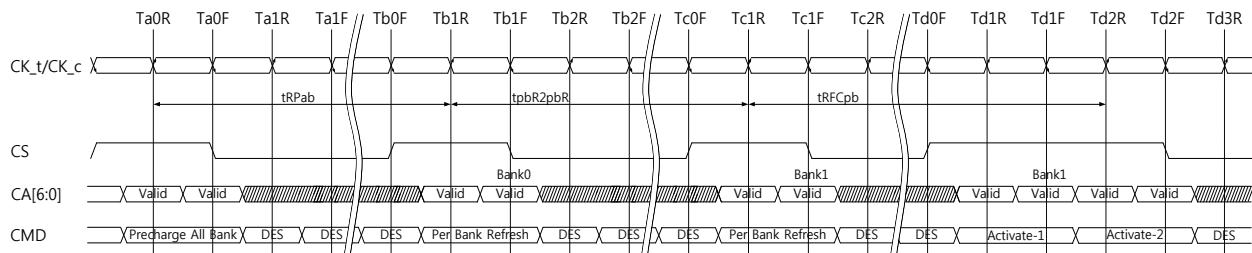
NOTE A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.



NOTES - 1. Only DES, NOP, PDE, MRR, MRW, MPC commands allowed after Refresh command registered until tRFCab(min) expires.

DON'T CARE TME BREAK

Figure 114 — All-Bank Refresh Operation



NOTES - 1. In the beginning of this example, the REFpb bank is pointing to bank 0.

2. Operations to banks other than the bank being refreshed are supported during the tRECpb period.

DON'T CARE TME BREAK

Figure 115 — Per-Bank Refresh Operation

7.5.1 Refresh command (Cont'd)

In general, a Refresh command needs to be issued to the LPDDR5 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR5 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in Table 188.

In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to $9 \times tREFI$. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to $9 \times tREFI$. At any given time, a maximum of 16 REF commands can be issued within $2 \times tREFI$. Self-Refresh Mode may be entered with a maximum of 8 Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed 8. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

7.5.1 Refresh command (Cont'd)

Table 188 — REFRESH Command Timing Constraints

MR4 OP[4:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab within max(2xtREFI x refresh rate multiplier,16xtRFC)	Per-bank Refresh
00000 _B	Low temp. Limit	N/A	N/A	N/A	N/A
00001 _B	8 x tREFI	1	2 x 8 x tREFI	2	1/8 of REFab
00010 _B	6 x tREFI	1	2 x 6 x tREFI	2	1/8 of REFab
00011 _B	4 x tREFI	2	3 x 4 x tREFI	4	1/8 of REFab
00100 _B	3.3 x tREFI	2	3 x 3.3 x tREFI	4	1/8 of REFab
00101 _B	2.5 x tREFI	3	4 x 2.5 x tREFI	6	1/8 of REFab
00110 _B	2.0 x tREFI	4	5 x 2.0 x tREFI	8	1/8 of REFab
00111 _B	1.7 x tREFI	5	6 x 1.7 x tREFI	10	1/8 of REFab
01000 _B	1.3 x tREFI	6	7 x 1.3 x tREFI	12	1/8 of REFab
01001 _B	1 x tREFI	8	9 x 1 x tREFI	16	1/8 of REFab
01010 _B	0.7 x tREFI	8	9 x 0.7 x tREFI	16	1/8 of REFab
01011 _B	0.5 x tREFI	8	9 x 0.5 x tREFI	16	1/8 of REFab
01100 _B	0.25 x tREFI, no de-rating	8	9 x 0.25 x tREFI	16	1/8 of REFab
01101 _B	0.25 x tREFI, with de-rating	8	9 x 0.25 x tREFI	16	1/8 of REFab
01110 _B	0.125 x tREFI, no de-rating	8	9 x 0.125 x tREFI	16	1/8 of REFab
01111 _B	0.125 x tREFI, with de-rating	8	9 x 0.125 x tREFI	16	1/8 of REFab
11111 _B	SDRAM High temperature operating limit exceeded	N/A	N/A	N/A	N/A

NOTE1 For any thermal transition phase where Refresh mode is transitioned, DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.

NOTE 2 LPDDR5 devices are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[4:0]. If shorter refresh period is applied, the corresponding requirements from table apply. For example, When MR4 OP[4:0]= 00001_B, controller can be in any refresh rate from 8 x tREFI to 0.25 x tREFI. When MR4 OP[4:0]= 00010_B, the only prohibited refresh rate is 8 * tREFI.

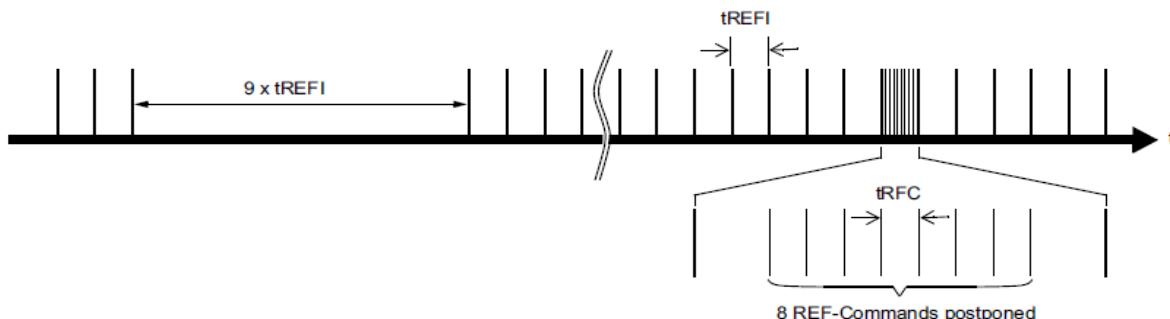


Figure 116 — Postponing Refresh Commands (Example)

7.5.1 Refresh command (Cont'd)

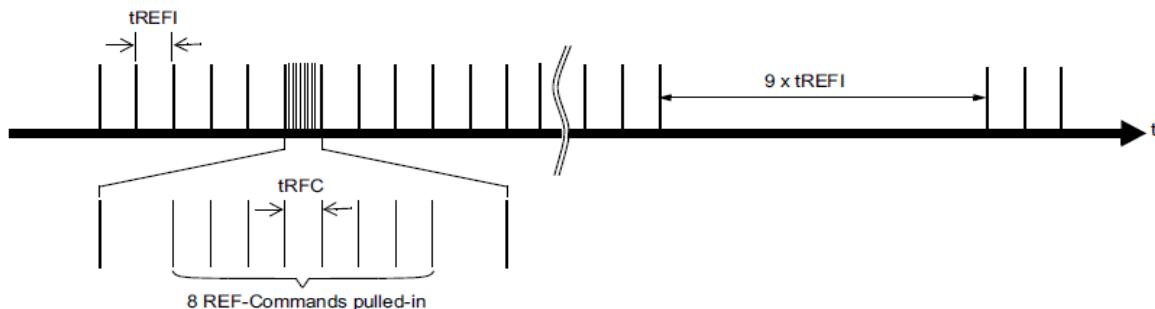


Figure 117 — Pulling-in Refresh Commands (Example)

7.5.2 Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self-Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR5 DRAM requires minimum of one extra Refresh command prior to Self-Refresh Entry command.

Table 189 — Refresh Requirement Parameters for BG mode or 16Bank mode

Refresh Requirements	Symbol	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb	Units	
Number of banks per channel		16										
Refresh Window (tREFW) (1x Refresh) ^{2,3}	tREFW	32										
Required Number of REFRESH Commands in a tREFW window	R	8192	8192	8192	8192	8192	8192	8192	8192	8192		
Average Refresh Interval (1x Refresh) ²	REFab	tREFI	3.906	3.906	3.906	3.906	3.906	3.906	3.906	3.906	μs	
	REFpb	tREFipb	488	488	488	488	488	488	488	488	ns	
Refresh Cycle Time (All Banks)	tRFCab	130	180	180	280	280	TBD	TBD	TBD	TBD	ns	
Refresh Cycle time (Per Bank)	tRFCpb	60	90	90	140	140	TBD	TBD	TBD	TBD	ns	
Per-bank Refresh to Per-bank Refresh different bank time	tpbR2pbR	60	90	90	90	90	TBD	TBD	TBD	TBD	ns	
REFpb to Activate command to different bank	tpbR2act	7.5	7.5	7.5	7.5	7.5	TBD	TBD	TBD	TBD	ns	

NOTE 1 Refresh for each channel is independent of the other channel in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

NOTE 2 1x refresh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[4:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.

NOTE 3 Refer to Table 47, MR4 OP[4:0], for detailed Refresh Rate and its multipliers.

7.5.2 Refresh Requirement (Cont'd)

Table 190 — Refresh Requirement Parameters for 8Bank mode

Refresh Requirements	Symbol	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb	Units
Number of banks						8					
Refresh Window (tREFW) (1x Refresh) ^{2,3}	tREFW					32					ms
Required Number of REFRESH Commands in a tREFW window	R	8192	8192	8192	8192	8192	8192	8192	8192	8192	
Average Refresh Interval (1x Refresh) ²	REFab	tREFI	3.906	3.906	3.906	3.906	3.906	3.906	3.906	3.906	μs
	REFpb	tREFIp _b	488	488	488	488	488	488	488	488	ns
Refresh Cycle Time (All Banks)	tRFCab	130	180	180	280	280	TBD	TBD	TBD	TBD	ns
Refresh Cycle time (Per Bank)	tRFCpb	60	90	90	140	140	TBD	TBD	TBD	TBD	ns
Per-bank Refresh to Per-bank Refresh different bank time	tpbR2pbR	60	90	90	90	90	TBD	TBD	TBD	TBD	ns
REFpb to Activate command to different bank	tpbR2act	10	10	10	10	10	TBD	TBD	TBD	TBD	ns

NOTE 1 Refresh for each channel is independent of the other channel in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

NOTE 2 1x refresh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[4:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.

NOTE 3 Refer to Table 47, MR4 OP[4:0], for detailed Refresh Rate and its multipliers.

7.5.3 Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR5 SDRAM; the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CS HIGH, CA[2:0] LOW, CA3 HIGH, CA4 LOW, CA5 HIGH and CA6 HIGH at the rising edge of the clock and CS don't care, CA[4:0] Valid (Valid that means it is Logic Level, High or Low), CA5 LOW and CA6 LOW at the falling edge of the clock. If Self Refresh command is issued with CA6 HIGH at the falling edge of the clock, Self-Refresh Command is initiated with Power Down status. Self-Refresh command is only allowed when read data burst is completed, in other words Read postamble is completed and SDRAM is idle state.

During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated and CA ODT state is maintained setting of its mode register, as well as NT ODT. SDRAM can accept the following commands; PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting.

LPDDR5 SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges.

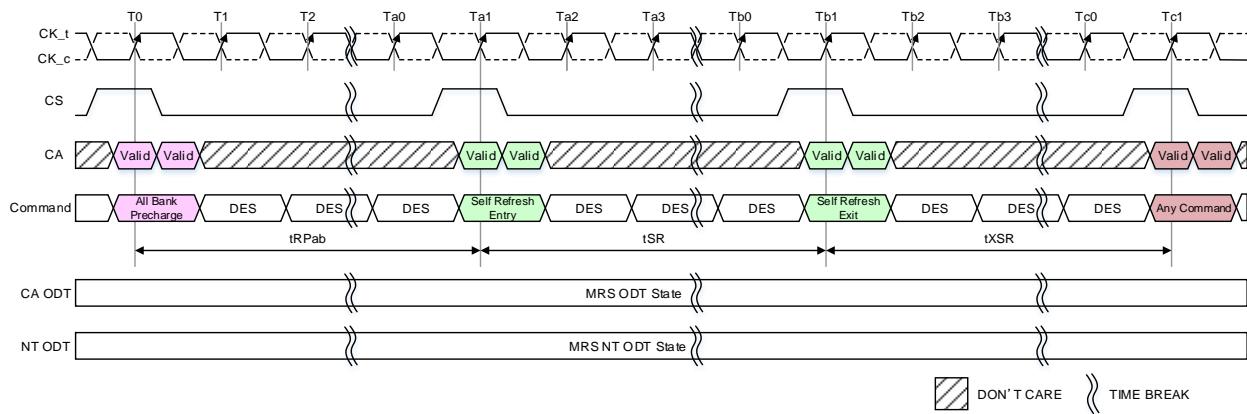
SDRAM will also manage Self Refresh power consumption when the operating temperature changes lower at low temperature and higher at high temperatures.

For proper Self Refresh operation, power supply pins (VDD1, VDD2H, VDD2L and VDDQ) is required to be at valid levels. However VDDQ may be turned off during Self-Refresh with Power Down after tESPD is satisfied (Refer to **Figure 119** about tESPD).

Prior to exiting Self-Refresh with Power Down, VDDQ is required to be within specified limits. The minimum time that the SDRAM is required to remained in Self Refresh mode is tSRmin. Once Self Refresh Exit is registered, only MRR, CAS, DES, MPC, MRW except PASR setting are allowed until tXSR is satisfied.

7.5.3 Self Refresh Operation (Cont'd)

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (1 all-bank or 16 per-bank for 4bank/4BG mode or 8 per-bank for 8bank mode) is issued before entry into a subsequent Self Refresh. This REFRESH command is not included in the count of regular refresh commands required by the tREFI interval, and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within 2 x tREFI.



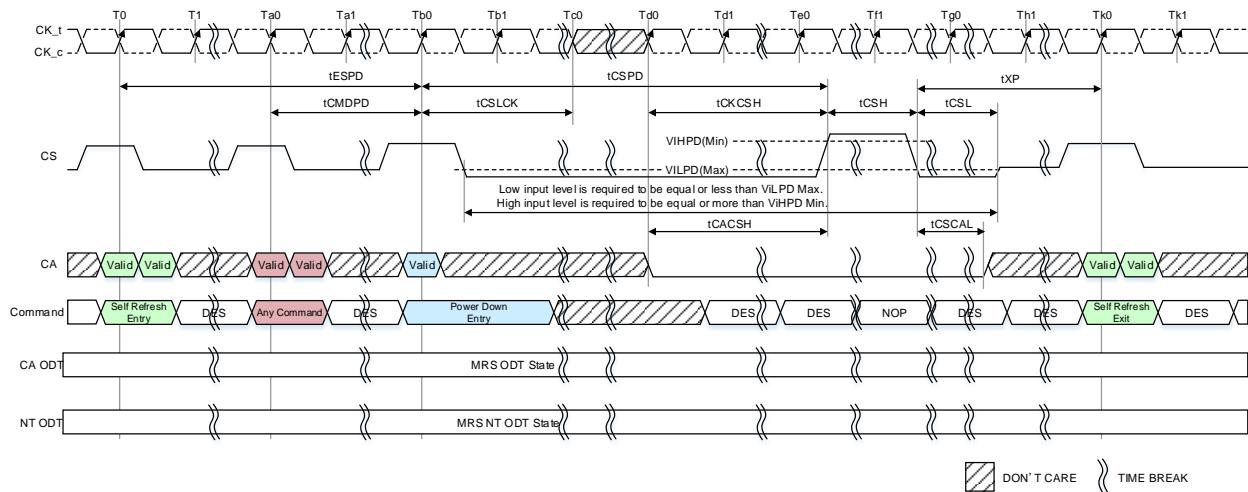
NOTE 1 PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting is allowed during Self Refresh.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 118 — Self Refresh Entry/Exit Timing

7.5.3.1 Power Down Entry and Exit during Self refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure 119. The power-down state is asynchronously exited when CS toggles HIGH (VIHPD). The AC parameters related to the Power Down are defined in the Power Down section, 7.5.5. The operation by command issued prior to PDE is required to be completed before changing clock frequency or stop clocking or turning off VDDQ.

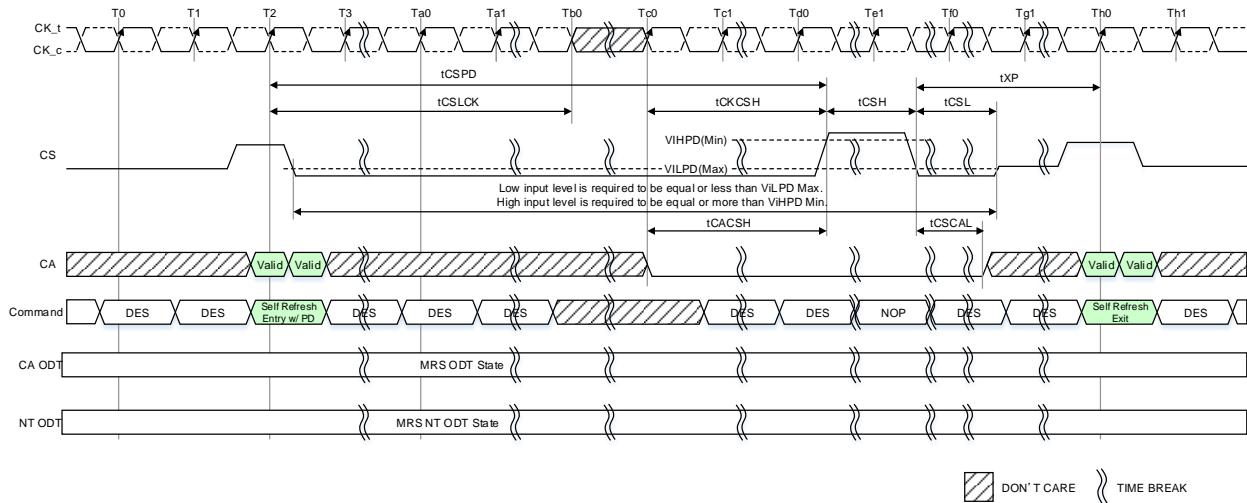


- NOTE 1 PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting is allowed during Self Refresh (No Power Down). The operation by command issued prior to Power Down Entry (PDE) is required to be completed before clock frequency or stop clocking or turning off VDDQ.
- NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon existing Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIHPD(Min).
- NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover point of VILPD(Max).
- NOTE 5 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

Figure 119 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit

7.5.3.1 Power Down Entry and Exit during Self refresh (Cont'd)

If Self Refresh command is issued with CA6 HIGH at the falling edge of the clock, Self-Refresh Command is initiated with Power Down status.

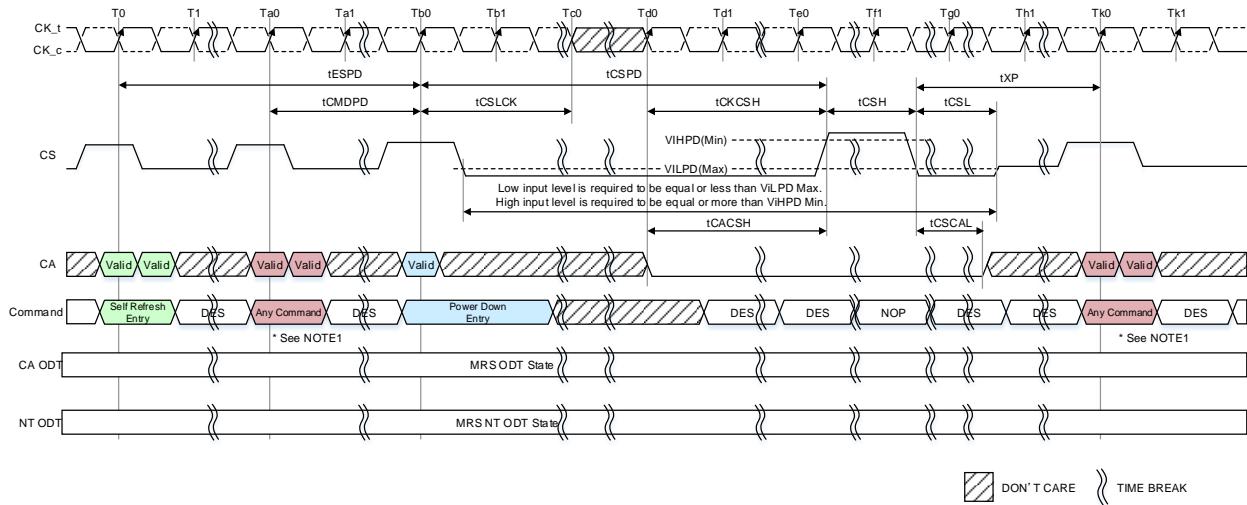


- NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

Figure 120 — Self Refresh Entry with PD="1" Timing

7.5.3.2 Command input Timing after Power Down Exit during Self Refresh

Command input timings after Power Down Exit during Self Refresh mode are shown in **Figure 121**.



NOTE 1 PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting is allowed during Self Refresh (No Power Down). The operation by command issued prior to Power Down Entry (PDE) is required to be completed before clock frequency or stop clocking or turning off VDDQ.

NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

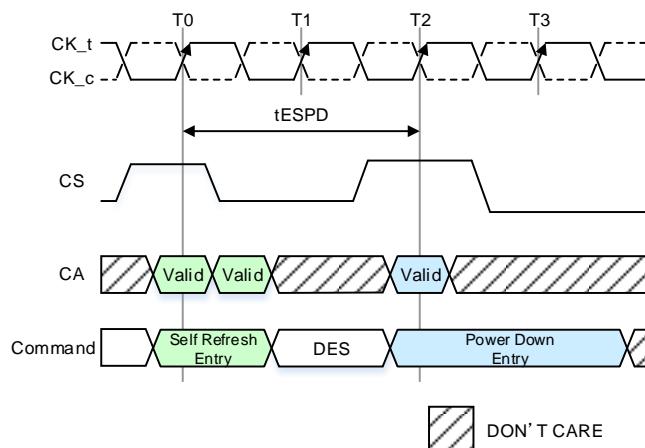
Figure 121 — Command input timing after Power Down Exit during Self Refresh

7.5.3.3 Self Refresh AC Timing Table

Table 191 — Self Refresh AC Timing

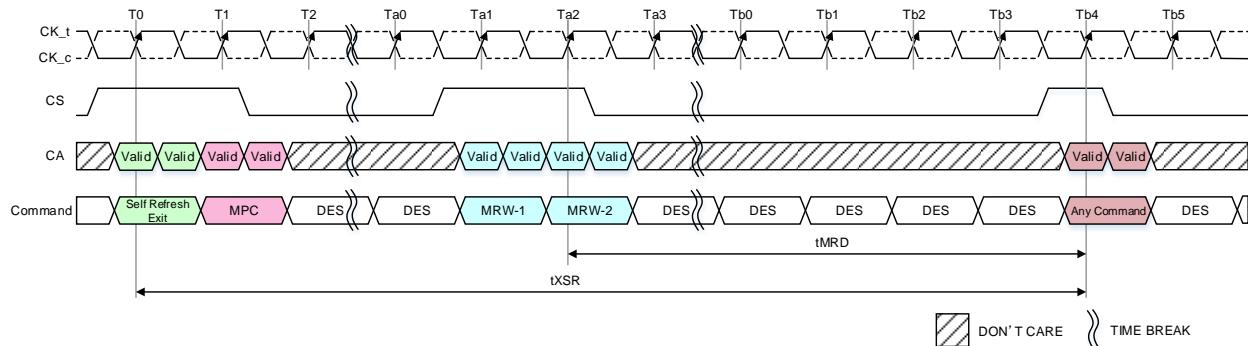
Parameters	Symbol	Min/ Max	Value	Unit	Note
Self Refresh Timing					
Delay from SRE command to PDE	tESPD	Min.	2	nCK	
Minimum Self Refresh Time (Entry to Exit)	tSR	Min.	Max(15ns, 2nCK)	ns	1
Exit Self Refresh to Valid commands	tXSR	Min.	tRFCab + Max(7.5ns, 2nCK)	ns	1

NOTE 1 Delay time has to satisfy both analog time(ns) and clock count(nCK). It means that tESPD will not expire until CK has toggled through at least 2 full cycles (2^*nCK) and 1.75ns has transpired. The case which 2nCK is applied to is shown below.



7.5.3.4 MRR, MRW, RFF, WFF, RDC, MPC Command during tXSR

Mode Register Read (MRR), Mode Register Write (MRW), Write FIFO (WFF), Read FIFO (RFF), Read DQ Calibration (RDC) and Multi Purpose Command (MPC) can be issued during tXSR period.



NOTE 1 MPC and MRW command are shown in this figure, any combination of MRR, MRW, WFF, RFF, RDC and MPC is allowed during tXSR period.

NOTE 2 Any command also includes MRR, MRW, WFF, RFF, RDC and all MPC command.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 122 — MRR, MRW, WFF, RFF, RDC and MPC Commands Issuing Timing during tXSR

Table 192 — Self Refresh Exit (SRX) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
Self Refresh Exit (SRX)	MODE REGISTER READ (MRR)	1	-	
	MODE REGISTER WRITE-1 (MRW-1)	1	-	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	WRITE FIFO (WFF)	1	-	
	READ FIFO (RFF)	1	-	
	READ DQ CALIBRATION (RDC)	1	-	
	MULTI PURPOSE COMMAND (MPC)	1	-	

7.5.4 Partial Array Self Refresh (PASR)

7.5.4.1 PASR Segment Masking

The LPDDR5 SDRAM adopts 8 bank base refresh schemes. A segment in each bank of the LPDDR5 SDRAM can be independently configured whether a Self Refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the segment masking status of each segment up to 8 segments. For segment masking bit assignments, see Table 88, Mode Register 23.

The mask bit to the segment controls a refresh operation of entire memory within the segment. When the segment is masked via MRW, a refresh operation to the entire segment is blocked and data retention by a segment is not guaranteed in Self Refresh mode. To enable a refresh operation to the segment, a coupled mask bit has to be programmed, “unmasked”.

Table 193 — Example of Segment Masking use in LPDDR5 SDRAM

	Segment Mask (MR23)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Segment 0	0								
Segment 1	0								
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0								
Segment 4	0								
Segment 5	0								
Segment 6	0								
Segment 7	1	M	M	M	M	M	M	M	M

NOTE 1 This table illustrates an example. When a refresh operation to segment 2 and segment 7 are masked.

7.5.5 Power Down

TBD

7.5.6 Power-Down Entry and Exit

Power-Down is entered by issuing Power-Down Entry Command. Power-Down Entry Command is issued by holding CS HIGH, CA[5:0] LOW and CA6 HIGH at the first rising edge of the clock. Power-Down Entry Command must not be issued while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- Mask Write
- VREF(CA) Range and Value setting via MRW
- VREF(DQ) Range and Value setting via MRW
- Command Bus Training mode Entering/Exiting via MRW
- VRCG High Current mode Entering/Exiting via MRW

And the LPDDR5 SDRAM cannot be placed in Power-Down state during “Start WCK2DQI Interval Oscillator” and “Start WCK2DQO Interval Oscillator” operation.

Power-Down Entry Command can be issued while any other operations such as row activation, Precharge, Auto Precharge or Refresh are in progress. The Power-Down IDD specification will not be applied until such operations are complete. Power-Down entry and exit are shown in **Figure 123**.

Entering Power-Down deactivates the input and output buffers, excluding CS and Reset_n. Clock input is required after Power-Down Entry Command is issued, this timing period is defined as tCSLCK. Power-Down Entry Command will result in deactivation of all input receivers except CS and Reset_n after tCSLCK has expired. In Power-Down mode, CS must be held LOW; all other input signals except Reset_n are “Don’t Care”. CS LOW must be maintained until tCSPDmin is satisfied.

VDDQ can be turned off during Power-Down. Prior to exiting Power-Down, VDDQ must be within its minimum/maximum operating range.

No refresh operations are performed in Power-Down mode except Self-Refresh Power-Down and Deep Sleep Mode. The maximum duration in Power-Down mode is only limited by the refresh requirements outlined in the Refresh command section.

The Power-Down state is asynchronously exited when CS toggles HIGH (VDD2H). Power-Down Entry command can be re-issued with tCSPDmin after CS goes HIGH. A valid, executable command can be applied with Power-Down exit latency tXP after CS goes HIGH.

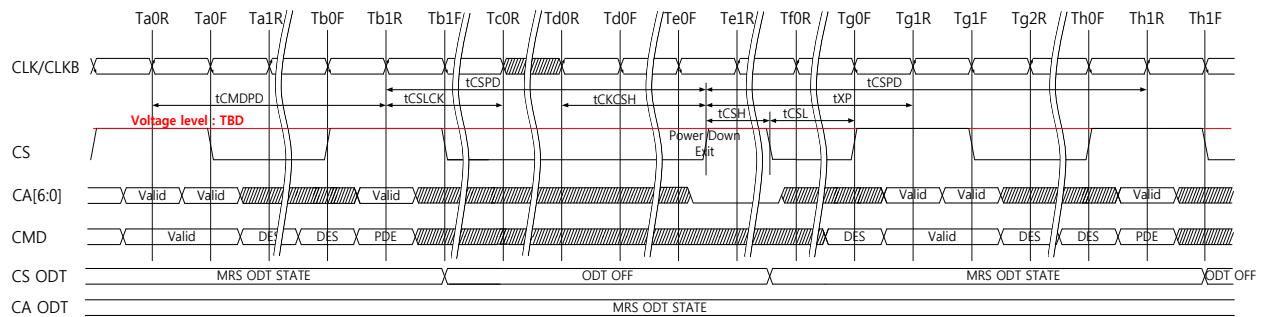
Clock frequency change or Clock Stop is inhibited during tCMDPD, tCSLCK, tCKCSH, tXP, tMRWP and tZQPD periods.

If Power-Down occurs when all banks are idle, this mode is referred to as idle Power-Down. If Power-Down occurs when there is a row active in any bank, this mode is referred to as active Power-Down. And if Power-Down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh Power-Down in which the internal refresh is continuing in the same way as Self Refresh mode.

7.5.6 Power-Down Entry and Exit (Cont'd)

When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also MR17 setting, the rank providing ODT will continue to terminate CA, CK bus in all DRAM states including Power-Down. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.

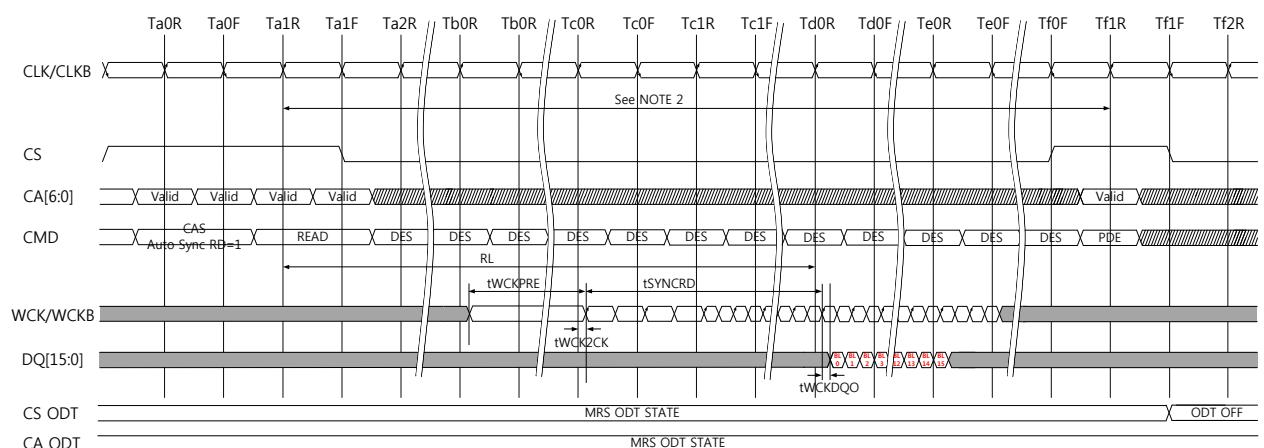
Power-Down AC timing parameters are defined in Table 194.



- NOTES - 1. Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSDH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
2. VIH level of CS is TBD.

■■■■■ DON'T CARE S TIME BREAK

Figure 123 — Basic Power-Down Entry and Exit Timing



- NOTES - 1. Power Down Entry Command is not allowed until the end of the burst operation.
2. Minimum Delay time from Read Command or Read with Auto Precharge Command to Power Down Entry Command is as follows.
: RL + RU{[tWCK2CK(max) + tWCKDQO(max)]/tCK} + BL/8 + 1 [Unit : tCK]

■■■■■ DON'T CARE S TIME BREAK

Figure 124 — Read and Read with Auto Precharge to Power-Down Entry

7.5.6 Power-Down Entry and Exit (Cont'd)

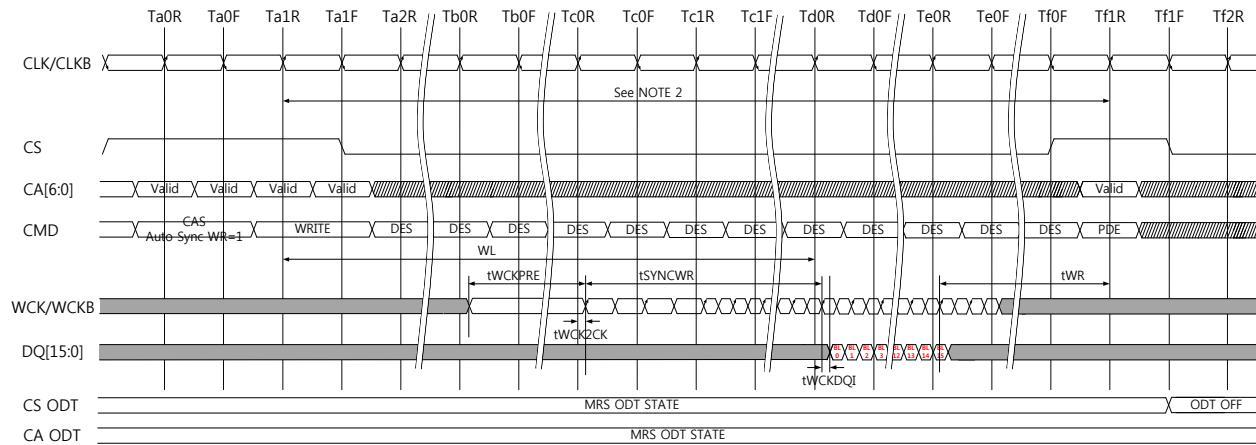


Figure 125 — Write and Mask Write to Power-Down Entry

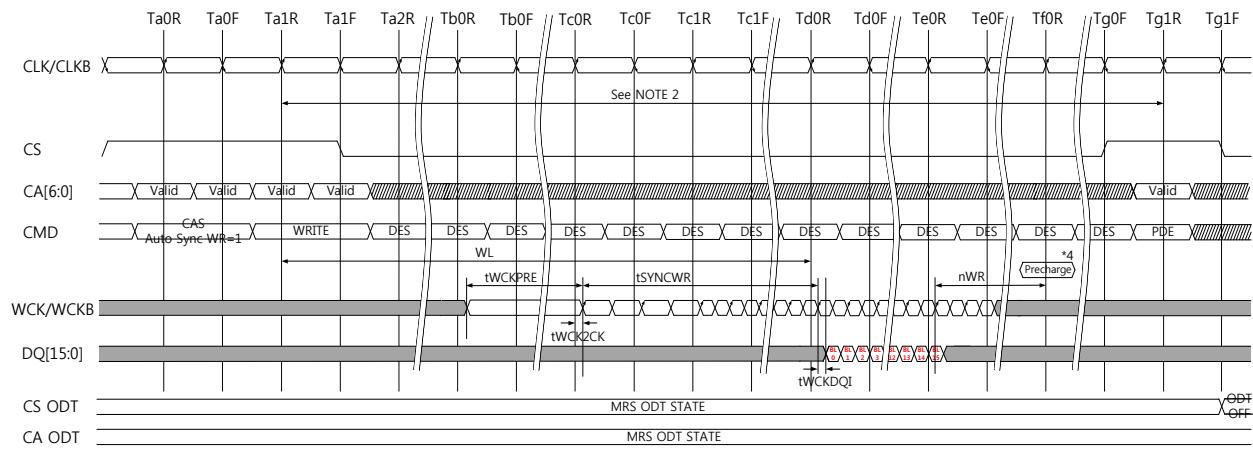
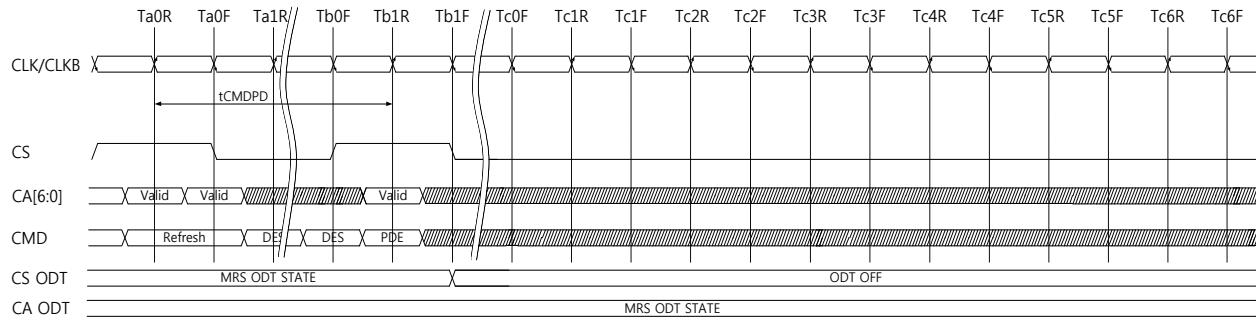


Figure 126 — Write with Auto Precharge and Mask Write with Auto Precharge to Power-Down Entry

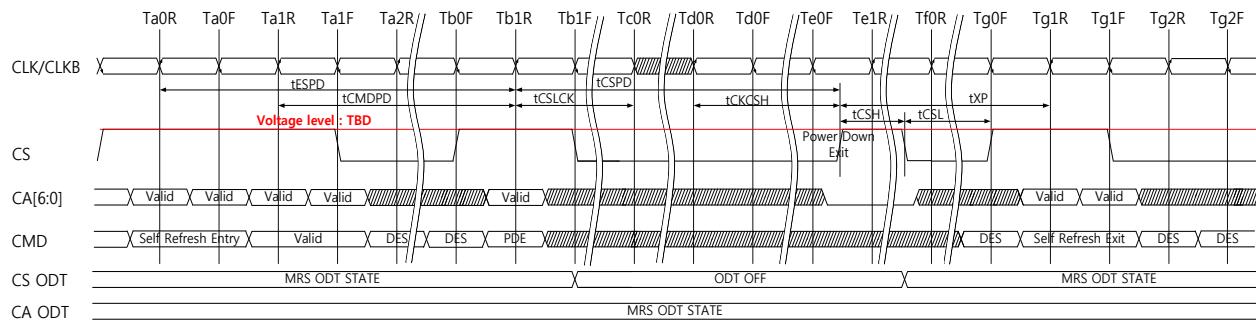
7.5.6 Power-Down Entry and Exit (Cont'd)



NOTES - 1. tCMDPD must be satisfied.

DON'T CARE TIME BREAK

Figure 127 — Refresh Entry to Power-Down Entry



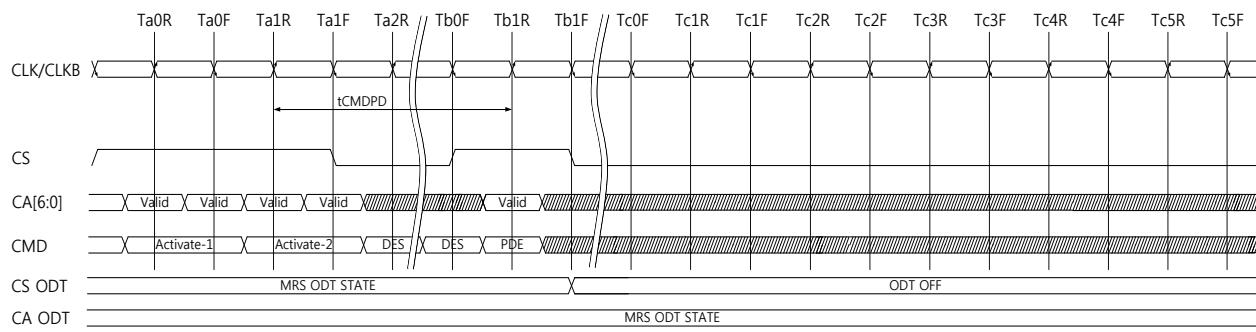
NOTES - 1. MRR, CAS, DES, SRX, MPC, MRW except PASR setting is allowed during Self Refresh(No Power Down).

2. Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

3. VIH level of CS is TBD.

DON'T CARE TIME BREAK

Figure 128 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit



NOTES - 1. tCMDPD must be satisfied.

DON'T CARE TIME BREAK

Figure 129 — Activate Command to Power-Down Entry

7.5.6 Power-Down Entry and Exit (Cont'd)

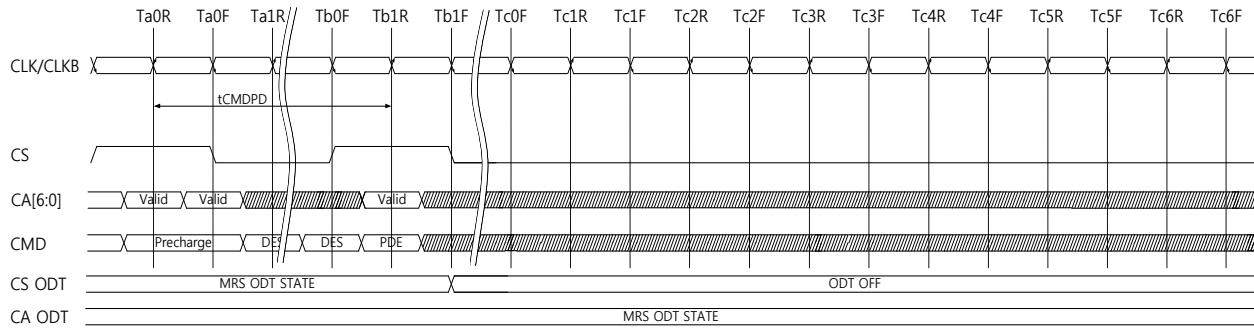


Figure 130 — Precharge Command to Power-Down Entry

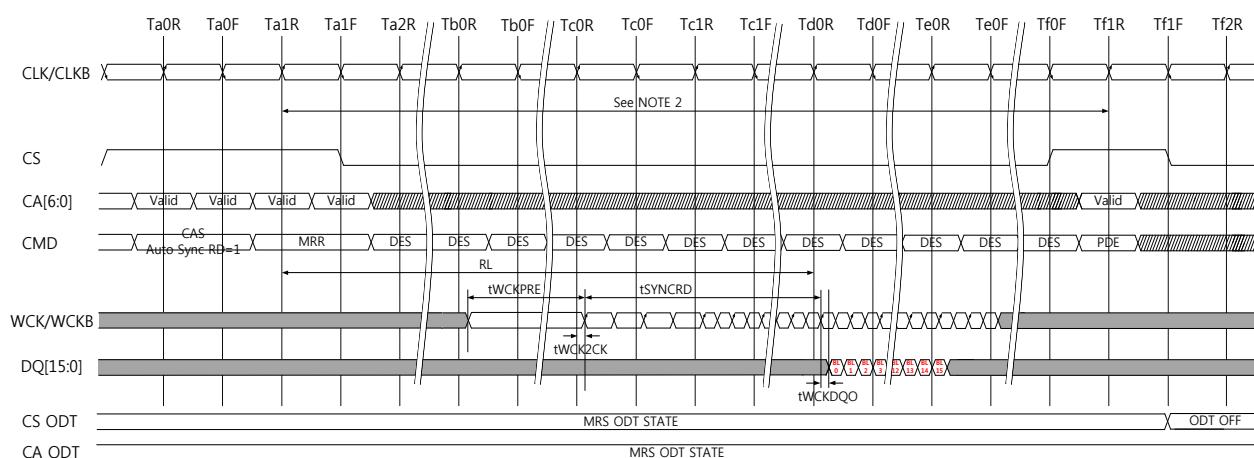


Figure 131 — Mode Register Read to Power-Down Entry

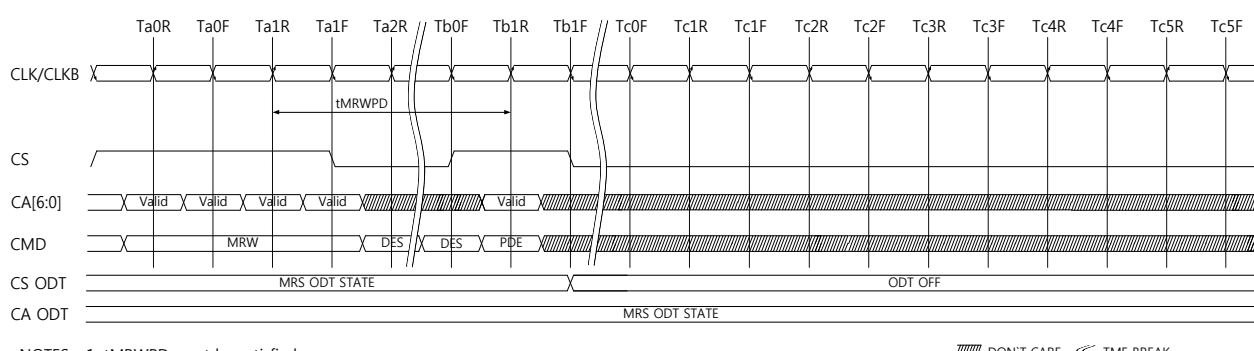
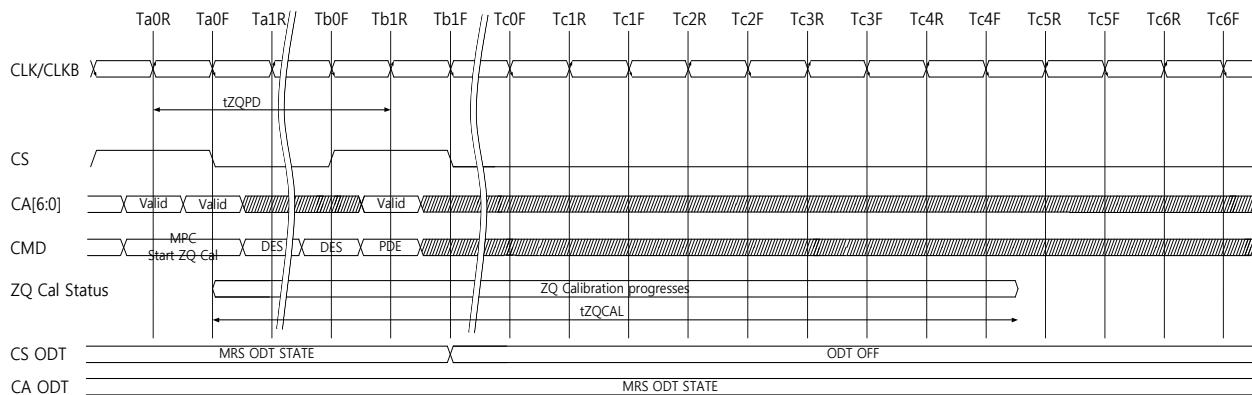


Figure 132 — Mode Register Write to Power-Down Entry

7.5.6 Power-Down Entry and Exit (Cont'd)



NOTES - 1. ZQ Calibration continues if Power Down Entry Command is issued after tZQPD is satisfied.

X DON'T CARE S TIME BREAK

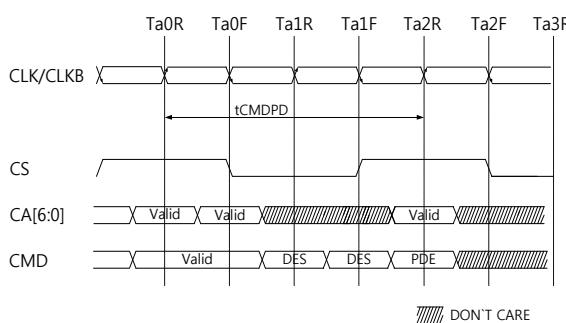
Figure 133 — Multi Purpose Command for Start ZQ Calibration to Power-Down Entry

Table 194 — Mode Register Read/Write AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Power-Down Timing					
Minimum interval between PDE and PDX	tCSPD	Min.	Max(7.5ns, 3nCK)	ns	1
Delay from valid command to PDE	tCMDPD	Min.	Max(1.75ns, 2nCK)	ns	1
Valid Clock Requirement after PDE	tCSLCK	Min.	Max(5ns, 3nCK)	ns	1
Valid Clock Requirement before PDX	tCKCSH	Min.	Max(1.75ns, 2nCK)	ns	1
Exit Power-Down to next valid command delay	tXP	Min.	Max(7.5ns, 3nCK)	ns	1
Minimum CS High Pulse width @ PDX	tCSH	Min.	3	ns	
Minimum CS Low Duration time @ PDX	tCSL	Min.	4	ns	
Delay from MRW command to PDE	tMRWPD	Min.	Max(14ns, 6nCK)	ns	1
Delay from ZQ Calibration Start Command to PDE	tZQPD	Min.	Max(1.75ns, 2nCK)	ns	1

NOTES - 1. Delay time has to satisfy both analog time(ns) and clock count(nCK).

For example, tCMDPD will not expire until CK has toggled through at least 2 full cycles(2*tCK) and 1.75ns has transpired. The case which 2nCK is applied to is shown below.



7.5.7 Sleep Mode

Deep Sleep Mode is an additional Self-Refresh mode with longer Entry/Exit times allowing the DRAM to manage internal circuits for low current consumption (specified by IDD_{tbd}). Deep Sleep Mode is entered by Self Refresh Entry Command defined by having CS HIGH, CA[2:0] LOW, CA3 HIGH, CA4 LOW, CA5 HIGH and CA6 HIGH at the rising edge of the clock and CS don't care, CA[4:0] Valid (Valid that means it is Logic Level, High or Low), CA5 HIGH and CA6 LOW at the falling edge of the clock. Deep Sleep Mode is only allowed when read data burst is completed and SDRAM is idle state or Self Refresh state. Deep Sleep Mode state diagram is shown in Figure 134.

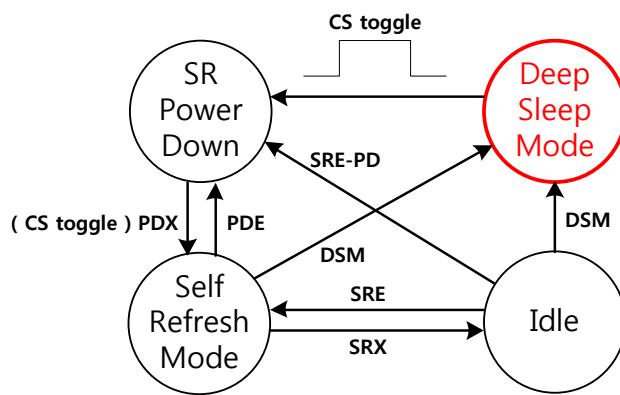


Figure 134 — Deep Sleep Mode state diagram

Once the SDRAM is entered in Deep Sleep Mode, it is recommended that Deep Sleep Mode is maintained for a relatively long time to reduce Self Refresh current more efficiently. It is functionally possible that SDRAM is exited quickly after Deep Sleep Mode issued. But, the short Deep Sleep Mode duration time is of little avail to reduce IDD6 Current. tPDN_DSM is the minimum recommendatory time for Deep Sleep Mode duration.

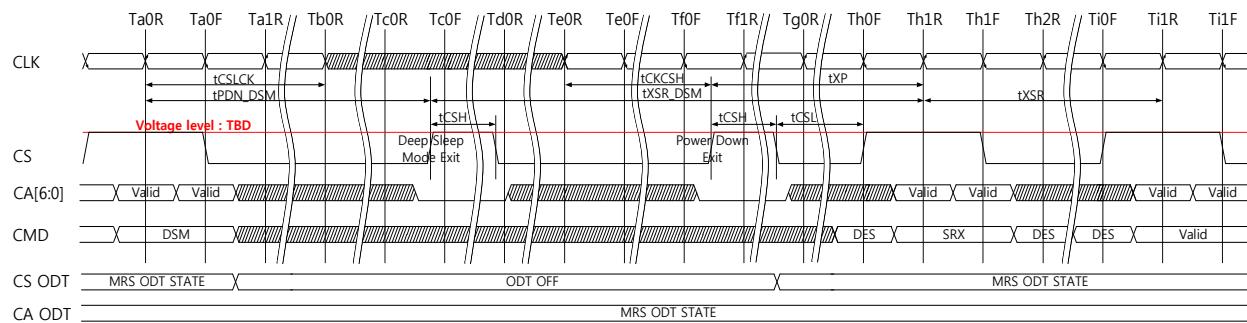
In Deep Sleep Mode, SDRAM is almost turned off except for Self refresh operation parts. Deep Sleep Mode state is asynchronously exited to Self-Refresh Power Down mode when CS toggles HIGH (VDD2H). The SDRAM must be satisfied tXSR_DSM to be fully re-powered up and then the SDRAM is ready for normal operations.

When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also MR17 setting, the rank providing ODT will continue to terminate CA, CK bus in all DRAM states including Power-Down and Deep Sleep Mode. CS ODT state goes OFF ignoring MRS ODT state after Deep Sleep Mode is issued.

LPDDR5 SDRAM can operate in Deep Sleep Mode in both the standard or elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes lower at low temperature and higher at high temperature.

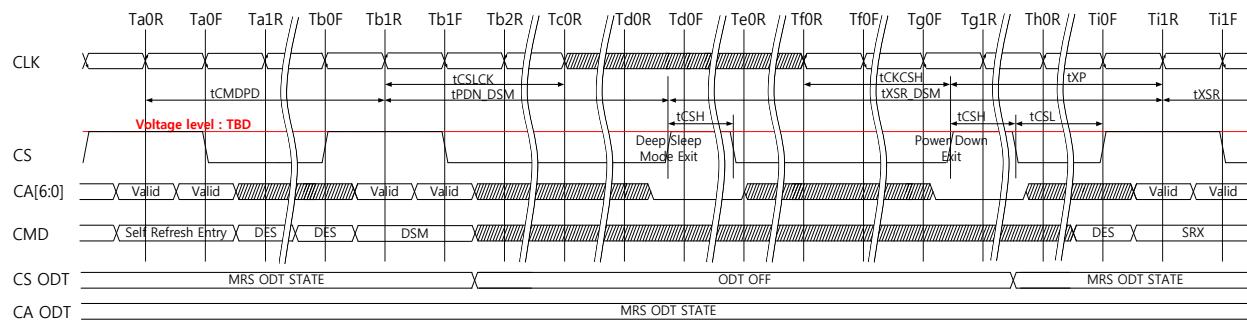
Deep Sleep Mode entry and exit are shown in **Figure 135** and the related AC timing parameters are defined in Table 195.

7.5.7 Sleep Mode (Cont'd)



NOTES - 1. Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
2. VIH level of CS is TBD.

Figure 135 — Deep Sleep Mode Entry in IDLE state and Exit Timing



NOTES - 1. Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
2. VIH level of CS is TBD.

Figure 136 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing

Table 195 — Deep Sleep Mode AC Timing Table

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Deep Sleep Mode Timing					
Minimum interval between Deep Sleep Mode Entry and Exit	tPDN	Min	Max(TBDns, TBDnCK)	ns	
Minimum Deep Sleep Mode duration time for DRAM compliance with IDDtdb power specification	tPDN_DSM	Min.	4	ms	
Delay from Deep Sleep Mode Exit to SRX	tXSR_DSM	Min.	200	μs	

7.6 Other Operation

7.6.1 Mode Register Read

The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR5-SDRAM registers. The MRR command is initiated with CS and CA[6:0] in the proper state as defined by the Command Truth Table, **Table 154**. The mode register address operands (MA[6:0]) allow the user to select one of 128 registers. The mode register contents are available on the first 8 UI's data bits of DQ[7:0] after RL + tWCK2DQO following the MRR command. Subsequent data bits contain valid but undefined content. WCK is toggled for the duration of the Mode Register READ burst. MRR has a command burst length 16 regardless of bank group, 16bank or 8bank mode.

In byte mode, the lower byte device follows the DQ output mapping in Table 196 because only DQ[7:0] is used to show the output from mode register. The upper byte device follows the DQ output mapping in Table 197 (MRR data).

MRR operation must not be interrupted.

Table 196 — DQ Output Mapping for lower byte

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15						
DQ0	OP0										V											
DQ1	OP1										V											
DQ2	OP2										V											
DQ3	OP3										V											
DQ4	OP4										V											
DQ5	OP5										V											
DQ6	OP6										V											
DQ7	OP7										V											
DQ[15:8]	V																					
DMI[1:0]	V																					

NOTE 1 MRR data is extended to first 8 UI's for DRAM controller to sample data easily.

NOTE 2 The read preamble and post amble of MRR are the same as normal read operation.

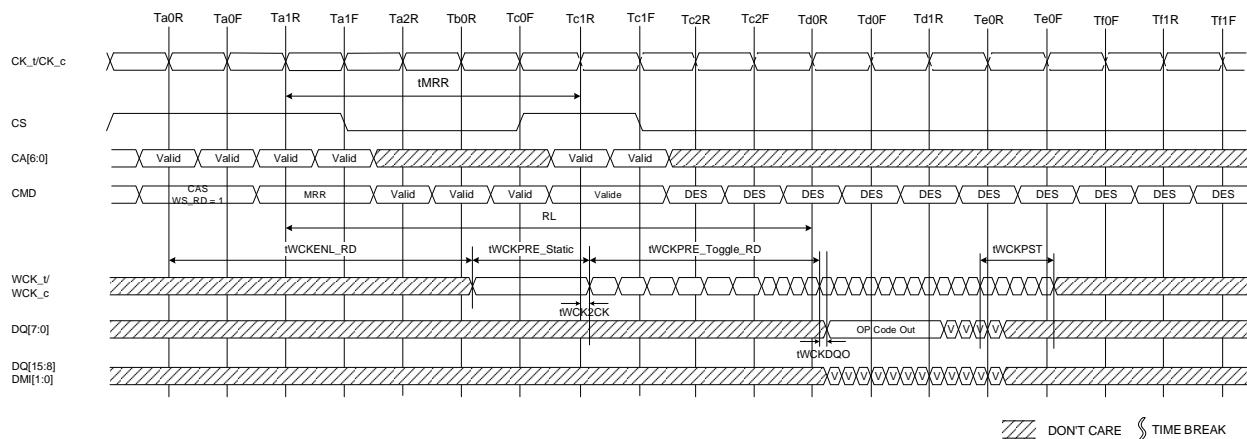
7.6.1 Mode Register Read (Cont'd)

Table 197 — DQ Output Mapping for upper byte

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ[7:0]	V															
DQ8	OP0															
DQ9	OP1															
DQ10	OP2															
DQ11	OP3															
DQ12	OP4															
DQ13	OP5															
DQ14	OP6															
DQ15	OP7															
DMI[1:0]	V															

NOTE 1 MRR data is extended to first 8 UI's for DRAM controller to sample data easily.

NOTE 2 The read preamble and post amble of MRR are the same as normal read operation.



NOTE 1 Only BL=16 is supported.

NOTE 2 Only DES is allowed during tMRR period.

NOTE 3 There are some exception about issuing commands after tMRR. Refer to MRR/MRW Timing Constraints Table for details.

NOTE 4 DBI is disable mode.

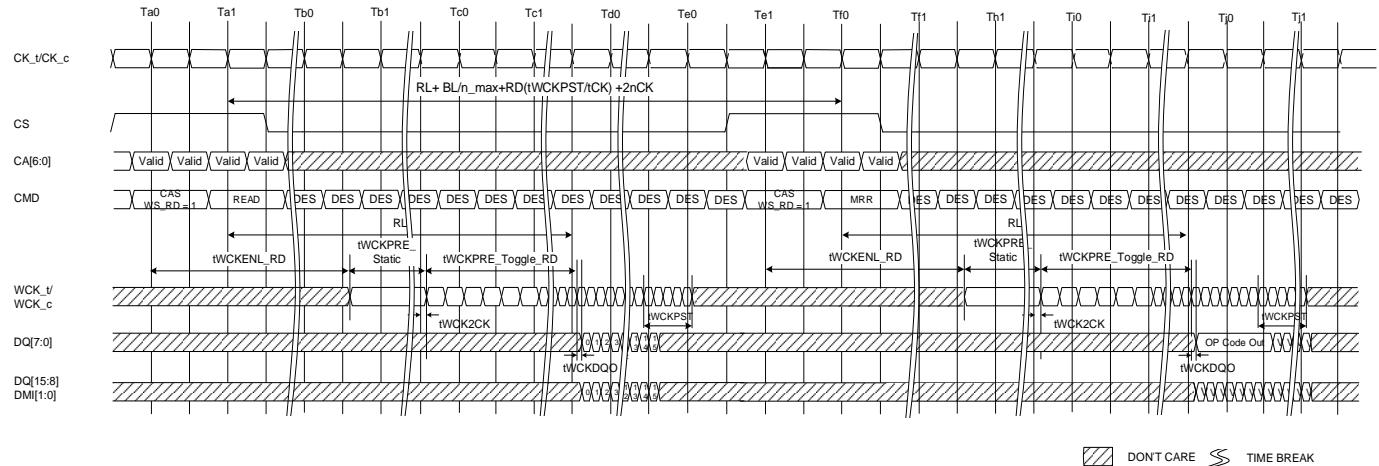
NOTE 5 DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

NOTE 6 DQ: VSS termination, WCK: VSS Termination.

Figure 137 — Mode Register Read Operation

7.6.1.1 MRR after Read and Write Command

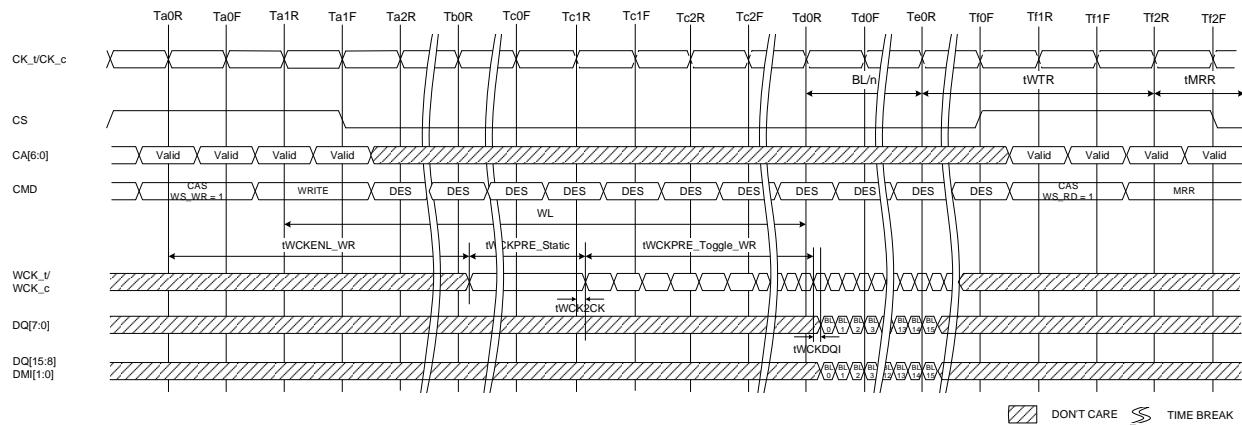
After a prior Read Command, the MRR command must not be issued earlier than $RL + BL/n_{max} + RD(tWCKPST/tCK) + 2nCK$ clock cycles, in a similar way $WL + BL/n_{max} + RU(tWTR/tCK)$ clock cycles after a prior Write, Write with AP, Masked Write, Masked Write with AP and Write FIFO command in order to avoid the collision of Read and Write burst data on SDRAM's internal Data bus. The timing variable “ BL/n_{max} ” is defined in the effective burst length table.



- NOTE 1 The minimum number of clock cycles from the burst READ command to the MRR command is $RL + BL/n_{max} + RD(tWCKPST/tCK) + 2nCK$. The timing variable “ BL/n_{max} ” is defined in the effective burst length table.
 NOTE 2 Read BL = 16, MRR BL = 16, DQ : VSSQ termination, WCK : VSS Termination.
 NOTE 3 DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

Figure 138 — READ to MRR Timing

7.6.1.1 MRR after Read and Write Command (Cont'd)

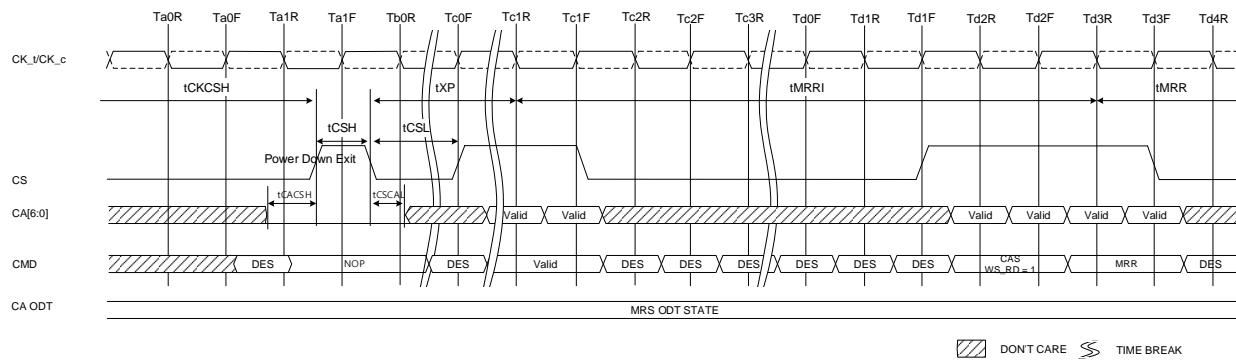


- NOTE 1 The minimum number of clock cycles from the burst write command to the MRR command is WL+BL/n_max+RU(tWTR/tCk). The timing variable "BL/n_max" is defined in the effective burst length table.
- NOTE 2 Write BL = 16, MRR BL =16, DQ: VSS termination, WCK: VSS Termination.
- NOTE 3 Only DES is allowed during tMRR period.
- NOTE 4 DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.
- NOTE 5 tWTR starts at the rising edge of CK after the last latching edge of WCK.

Figure 139 — WRITE to MRR Timing

7.6.1.2 MRR after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode.



NOTE 1 Only DES is allowed during tMRR period.

NOTE 2 DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

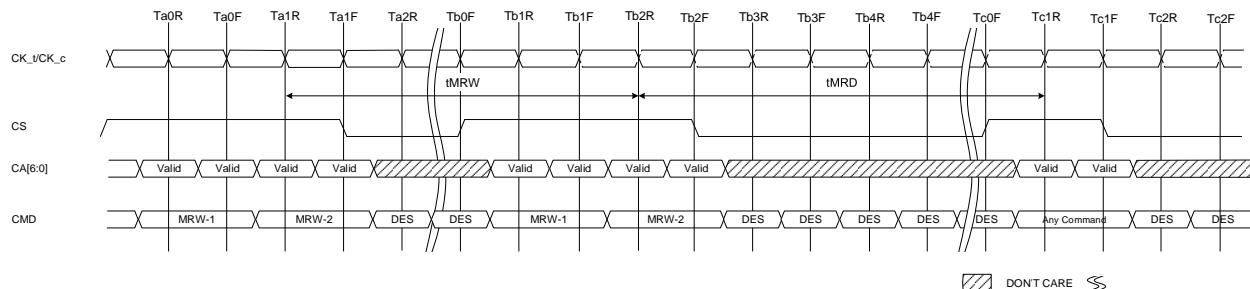
Figure 140 — MRR Following Power-Down

Table 198 — Mode Register Read/Write AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min.	tRCD + 2nCK	ns	
MODE REGISTER READ command period	tMRR	Min.	4 @ CK:WCK=1:4 8 @ CK:WCK=1:2	nCK	
MODE REGISTER WRITE command period	tMRW	Min.	Max (10ns, 5nCK)	ns	
Mode register set command delay	tMRD	Min.	Max (14ns, 5nCK)	ns	

7.6.2 Mode Register Write

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CS and CA[6:0] to valid levels as defined by Command Truth Table, **Table 154**. The mode register address and the data written to the mode registers is contained in CA[6:0]. The Mode Register Write command is composed of two commands, MRW-1 command and MRW-2 command. But, MRW-1 command must be followed by MRW-2 command consecutively. The MRW command period is defined by tMRW. The Mode Register Write command to read-only registers have no impact on the functionality of the device.



NOTE 1 Only DES command is allowed during tMRW and tMRD periods.

Figure 141 — Mode Register Write Timing

Table 199 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State		Next State
		SDRAM	SDRAM	
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)		All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)		All Banks Idle
Bank(s) Active	MRR	Mode Register Reading		Bank(s) Active
	MRW	Mode Register Writing		Bank(s) Active

7.6.2.1 Mode Register Write Disable control for Byte Mode device

Byte mode device may share their CK_c/CK_t, CS and CA's between upper byte and lower byte of device. Setting MR20 OP[5:4] will allow disabling upper and lower bytes independently for an MRW to the following mode registers. MRxx OP[n+1,n] (MRW Byte Mode Disable) control specific mode register write operation.

MRW Byte Mode Disable control following mode register OP code.

- MR13 OP[1:0] Thermal Offset
- MR25 OP[5:4] CA BUS TERM, CK BUS TERM
- MR41 OP[4] PPREG
- MR41 OP[7:5] NT DO ODT

7.6.3 Frequency Set Point

Frequency Set Points (FSP) allow the LPDDR5 SDRAM CA Bus to be switched between three differing operating frequencies, with changes in voltage swings and termination values, without ever being in an untrained state which could result in a loss of communication to the SDRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These tripled registers form three sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for a selected Frequency Set-Point without affecting the LPDDR5-SDRAM's current operation. Once all necessary parameters have been written to the selected Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have three physical registers controlled by FSP-WR and FSP-OP include:

Table 200 — Mode Register Function with three physical registers

MR#	Operand	Function	Note
MR1	OP[3]	CK mode	
	OP[7:4]	WL (Write Latency)	
MR2	OP[3:0]	RL (Read latency) and nRBTP(READ burst end to PRECHARGE delay)	
	OP[7:4]	nWR(Write-Recovery for Auto-Precharge commands)	
MR3	OP[2:0]	PDDS (Pull-Down Drive Strength)	
	OP[4:3]	BK/BG ORG (Bank/Bank Group Organization)	
	OP[5]	WLS (Write Latency Set)	
	OP[6]	DBI-RD (DBI-Read select)	
	OP[7]	DBI-WR (DBI-Write select)	
MR10	OP[0]	RDQS Post-amble mode	
	OP[3:2]	WCK PST (WCK Post-amble Length)	
	OP[5:4]	RDQS PRE (RD Pre-amble Length)	
	OP[7:6]	RDQS PST (RD Post-amble Length)	
MR11	OP[2:0]	DQ ODT (DQ Bus Receiver On-Die-Termination)	
	OP[6:4]	CA ODT (CA Bus Receiver On-Die-Termination)	
MR12	OP[6:0]	V _{REF} (CA) (V _{REF} (CA) Setting)	
MR14	OP[6:0]	V _{REF} (DQ[7:0]) (V _{REF} (DQ[7:0]) Setting)	
MR15	OP[6:0]	V _{REF} (DQ[15:8]) (V _{REF} (DQ[15:8]) Setting)	
MR17	OP[2:0]	SoC ODT (Controller ODT Value for VOH calibration)	
	OP[3]	ODTD-CK (CK ODT termination)	
	OP[5]	ODTD-CA (CA ODT termination)	
MR18	OP[2:0]	WCK ODT	
	OP[3]	WCK FM (WCK Frequency Mode)	
	OP[4]	WCK ON (WCK always ON mode)	
	OP[7]	CKR (WCK to CK frequency ratio)	
MR19	OP[1:0]	DVFSC (VDD2 Dynamic Voltage and Frequency Scaling Core)	
	OP[3:2]	DVFSQ (VDDQ Dynamic Voltage and Frequency Scaling VDDQ)	
MR20	OP[1:0]	RDQS (Read DQS)	
	OP[3:2]	WCK mode	
MR24	OP[2:0]	DFE Quantity for Lower Byte (DFEQL)	
	OP[6:4]	DFE Quantity for Upper Byte (DFEQU)	
MR30	OP[3:0]	DCA for Lower Byte (DCAL)	
	OP[7:4]	DCA for Upper Byte (DCAU)	
MR41	OP[7:5]	NT DQ ODT (Non-Target DQ Bus Receiver On-Die-Termination)	

See 6.2.1, Mode Register Definition, for more details.

7.6.3 Frequency Set Point (Cont'd)

Table 201 shows how the three mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

Table 201 — Relation between MR Setting and DRAM Operation

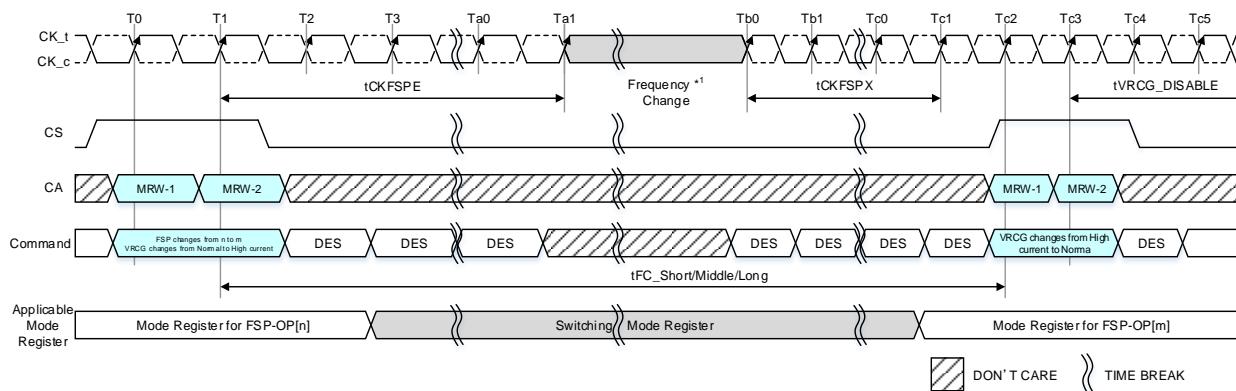
Function	MR# & Operand	Data	Operation	Note
FSP-WR	MR16 OP[1:0]	00 _B (Default)	Data write to Mode Register N for FSP-OP[0] by MRW Command. Data read from Mode Register N for FSP-OP[0] by MRR Command.	1
		01 _B	Data write to Mode Register N for FSP-OP[1] by MRW Command. Data read from Mode Register N for FSP-OP[1] by MRR Command.	
		10 _B	Data write to Mode Register N for FSP-OP[2] by MRW Command. Data read from Mode Register N for FSP-OP[2] by MRR Command.	
FSP-OP	MR16 OP[3:2]	00 _B (Default)	SDRAM operates with Mode Register N for FSP-OP[0] setting.	2
		01 _B	SDRAM operates with Mode Register N for FSP-OP[1] setting.	
		10 _B	SDRAM operates with Mode Register N for FSP-OP[2] setting.	

NOTE 1 FSP-WR stands for Frequency Set Point Write/Read.

NOTE 2 FSP-OP stands for Frequency Set Point Operating Point.

7.6.3.1 Frequency set point update Timing

The Frequency set point update timing is shown in Figure 142. When changing the frequency set point via MR16 OP[3:2], the VRCG setting: MR16 OP[6] is required to be changed into VREF Fast Response (high current) mode at the same time. After Frequency change time(tFC) is satisfied. VRCG can be changed into Normal Operation mode via MR16 OP[6].



NOTE 1 The Clock frequency change should be made during the 'frequency change' timing (Ta1 to Tb0). For more information, refer to 7.6.6, Input Clock Stop and Frequency Change.

Figure 142 — Frequency Set Point Switching Timing

7.6.3.2 Frequency set point update Timing for DVFSC and DVFSQ

TBD

Table 202 — Frequency Set Point AC Timing Table

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			5 3	1 0	1 6	2 1	2 7	3 2	3 7	4 2	4 8	5 5	6 0	6 4		
Frequency Set Point parameters																
Frequency Set Point Switching Time	tFC_Short	Min	200+0.5tCK										ns	1,2		
	tFC_Middle	Min	200+0.5tCK										ns	1,2		
	tFC_Long	Min	250+0.5tCK										ns	1,2		
Valid Clock Requirement after Entering FSP Change	tCKFSPE	Min	max(7.5ns, 4nCK)										-			
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	Min	max(7.5ns, 4nCK)										-			

NOTE 1 Frequency Set Point Switching Time depends on value of $V_{REF}(CA)$ setting: MR12 OP[6:0] of FSP-OP 0, 1 and 2. The details are shown in Table 203. Additionally change of Frequency Set Point may affect $V_{REF}(DQ)$ setting. Settling time of $V_{REF}(DQ)$ level is same as $V_{REF}(CA)$ level.

NOTE 2 tCK for this timing is the tCK value of the operating frequency when the MRW is issued.

Table 203 — tFC value mapping

Application	Step Size	
	From FSP -OP0	To FSP-OP1
tFC_Short	Base	A single step size increment/decrement
tFC_Middle	Base	Two and less than 33 step size increment/decrement
tFC_Long	Base	More than 32 step size increment/decrement

NOTE 1 Changing from FSP-OPx to FSP-OPy is also supported.

Table 204 provides an example of tFC value mapping when FSP-OP moves from OP0 to OP1.

Table 204 — tFC value mapping example

Case	From/To	FSP-OP: MR16 OP[3:2]	$V_{REF}(CA)$ Setting: MR12: OP[6:0]	Application	Note
1	From	00	0001100	tFC_Short	1
	To	01	0001101		
2	From	00	0001100	tFC_Middle	2
	To	01	0011110		
3	From	00	0001000	tFC_Long	3
	To	01	0101000		

NOTE 1 A single step size increment/decrement for $V_{REF}(CA)$ Setting Value.

NOTE 2 Two and less than 33 step size increment/decrement for $V_{REF}(CA)$ Setting Value.

NOTE 3 More than 32 step size increment/decrement for $V_{REF}(CA)$ Setting Value.

7.6.3.2 Frequency set point update Timing for DVFS and DVFSQ (Cont'd)

The LPDDR5-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR5 SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point, **Figure 143**. See the section Command Bus Training (4.2.2) for more details on this training mode.

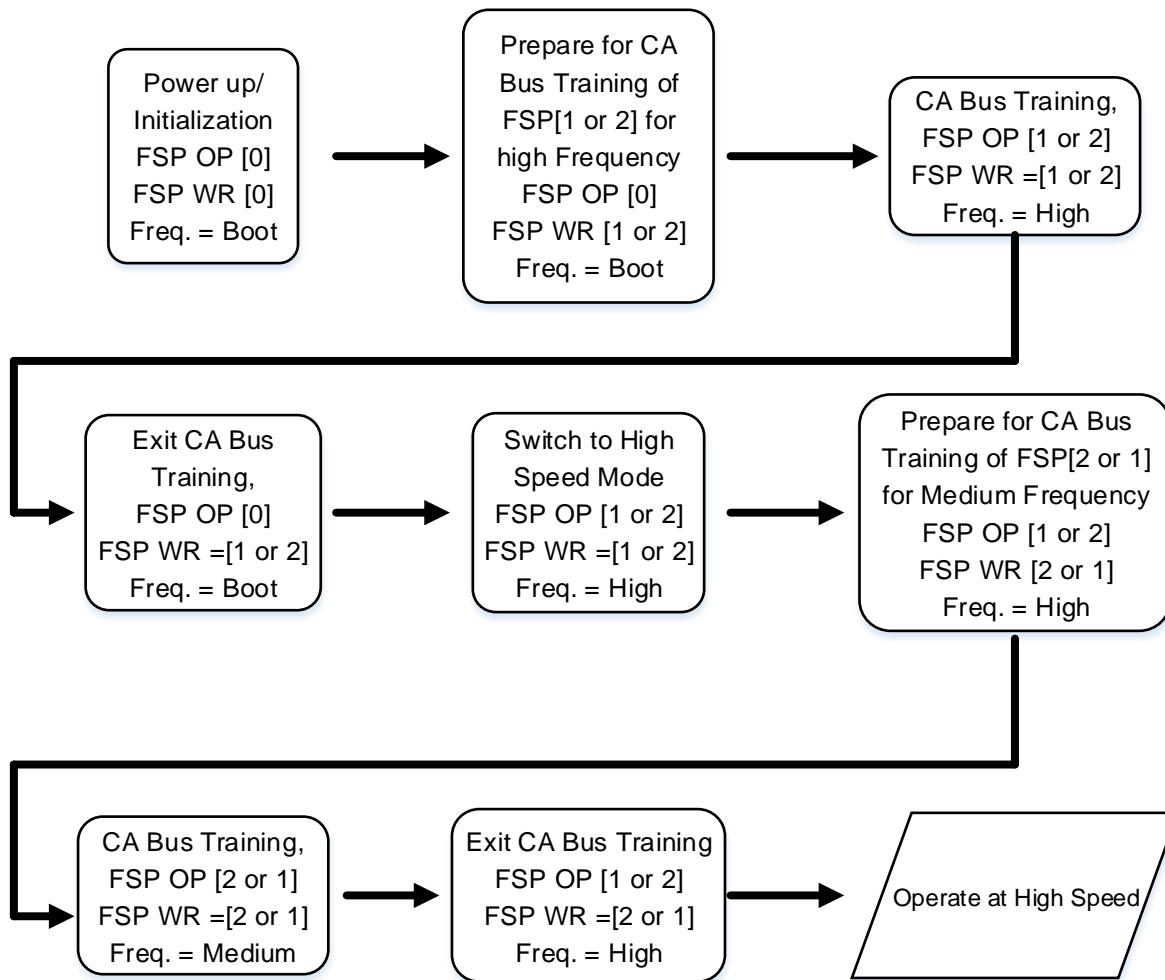


Figure 143 — Training Three Frequency Set-Points

7.6.3.2 Frequency set point update Timing for DVFSC and DVFSQ (Cont'd)

Once all Frequency Set-Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (Figure 144).

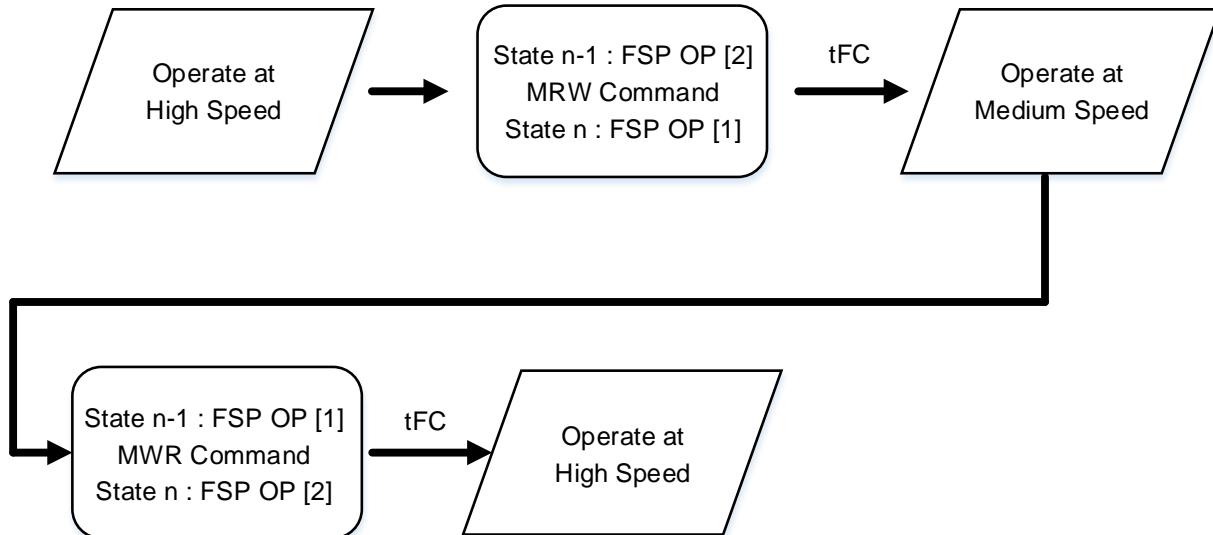


Figure 144 — Switching Between Two Trained Frequency Set-Points (Example)

Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the $V_{REF}(CA)$ calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure 145).

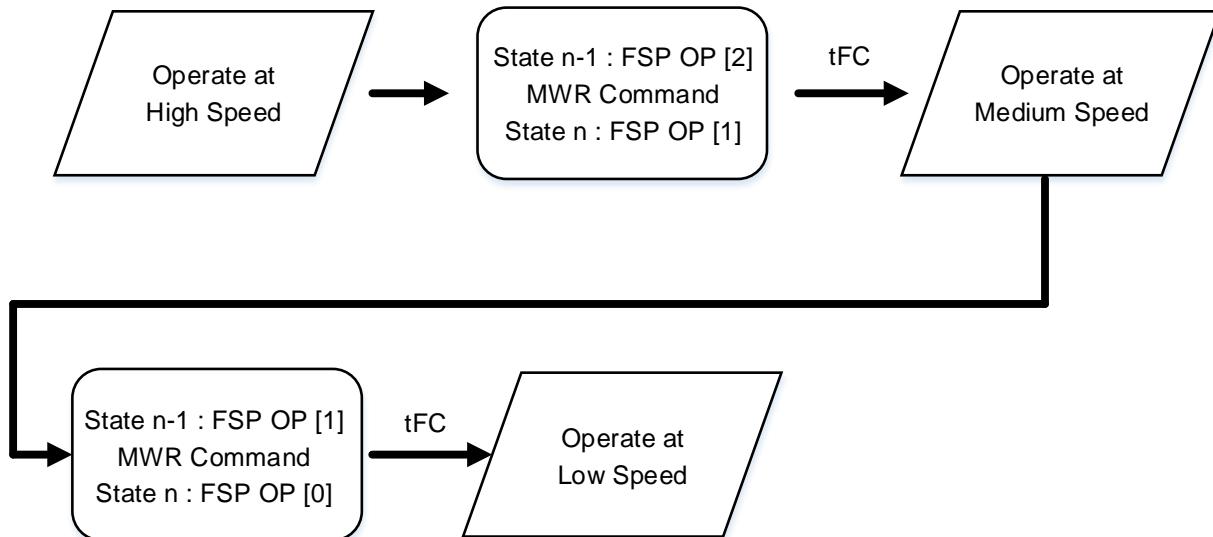


Figure 145 — Switching to a Third Trained Frequency Set-Point (Example)

7.6.4 On-Die Termination (ODT)

7.6.4.1 On-Die Termination for Command/Address Bus

Command/Address ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for CK_t, CK_c, and CA[6:0] signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting. A simple functional representation of the Command/Address ODT feature is shown in Figure 146.

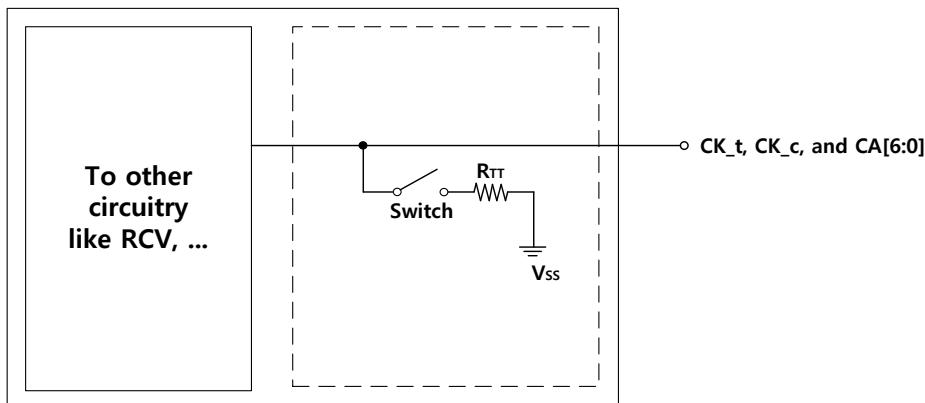


Figure 146 — Functional Representation of Command/Address bus ODT

7.6.4.1.1 ODT Mode Register and ODT State Table for Command/Address Bus

Command/Address ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_c, CA[6:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA bus is ODT disabled.

CA/CK ODT of the device is designed to enable one rank (termination for one rank and un-termination for other ranks) or multi ranks (balanced termination for all ranks) to terminate the entire command bus in the multi rank system. For this reason, the rank providing CA, CK ODT via MR11 OP[6:4] and also MR17 setting will continue to terminate CA, CK bus in all DRAM states including Power-Down and Deep Sleep Mode.

For the individual ODT control, LPDDR5 SDRAM uses the MR17 setting. MR17 OP[3] is set to disable the CK ODT and MR17 OP[5] is set to disable the CA ODT. MR17 OP[7:6] is set to disable CK/CA ODT of the lower or upper byte of selected device and is only used for the Byte Mode device (X8).

In the multi-rank/channel system, the device usually shares the CA/CK bus and the un-terminated die needs to know ODT status of other shared dies when the termination status of CA/CK bus is different from each other. LPDDR5 SDRAM uses the MR25 setting to decide a buffer type for power optimization. MR25 OP[4] is set to notify CK ODT status of other shared dies, MR25 OP[5] is set to notify CA ODT status of other shared dies.

Example: when CK and CA ODT status is different from each other(ex. CK termination, CA un-termination) and MR25 OP[5] is disabled, the un-terminated CA input buffer use the fixed level reference voltage (TBD).

7.6.4.1.1 ODT Mode Register and ODT State Table for Command/Address Bus (Cont'd)

The ODT state of the Command/Address bus is shown in Table 205.

Table 205 — Command/Address Bus ODT State
LPDDR5 X16 Mode Device (MR8 OP[7:6] = 00B case)

MR17	X8ODTD Upper	X8ODTD Lower	CA	CK	CA	CK_t/CK_c
	OP[6]	OP[5]	OP[4]	OP[3]		
LPDDR5	X	X	0	0	T	T
	X	X	0	1	T	
	X	X	1	0		T
	X	X	1	1		

NOTE 1 X16 mode device ignores MR17 OP[6:5] setting.

NOTE 2 MR11 OP[6:4] must be 001_B, 010_B, 011_B, 100_B, 101_B, or 110_B to turn on CA/CK ODT.

NOTE 3 T means “terminated” condition. Blank is “un-terminated”.

LPDDR5 Byte Mode Device (MR8 OP[7:6] = 01B case)

MR17	X8ODTD Upper	X8ODTD Lower	CA	CK	CA		CK_t/CK_c	
	OP[6]	OP[5]	OP[4]	OP[3]	0Byte	1Byte	0Byte	1Byte
LPDDR5	0	0	0	0	T	T	T	T
	0	0	0	1	T	T		
	0	0	1	0			T	T
	0	0	1	1				
	0	1	0	0		T		T
	0	1	0	1		T		
	0	1	1	0				T
	0	1	1	1				
	1	0	0	0	T		T	
	1	0	0	1	T			
	1	0	1	0			T	
	1	0	1	1				

NOTE 1 MR11 OP[6:4] must be 001_B, 010_B, 011_B, 100_B, 101_B, or 110_B to turn on CA/CK ODT.

NOTE 2 T means “terminated” condition. Blank is “un-terminated”.

NOTE 3 Two T(T for 0_B and 1_B) means balanced (identical) CA/CK ODT setting in x8 system.

7.6.4.1.2 ODT Mode Register and ODT Characteristics for Command/Address Bus

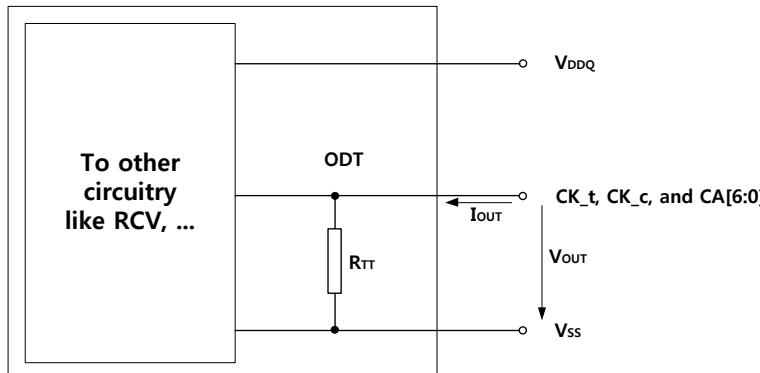


Figure 147 — On Die Termination for Command/Address Bus

Table 206 — ODT DC Electrical Characteristics, assuming $RZQ = 240\Omega \pm 1\%$ over the entire operating temperature range after a proper ZQ calibration

MR11 OP[6:4]	RTT	Vout	Min	Nom	Max	Unit	Note
001	240Ω	$VOLdc = 0.2*VDDQ$	0.8	1.0	1.1	RZQ	1,2,3
		$VOMdc = 0.5*VDDQ$	0.9	1.0	1.1	RZQ	1,2,3
		$VOHdc = 0.75*VDDQ$	0.9	1.0	1.3	RZQ	1,2,3
010	120Ω	$VOLdc = 0.2*VDDQ$	0.8	1.0	1.1	RZQ/2	1,2,3
		$VOMdc = 0.5*VDDQ$	0.9	1.0	1.1	RZQ/2	1,2,3
		$VOHdc = 0.75*VDDQ$	0.9	1.0	1.3	RZQ/2	1,2,3
011	80Ω	$VOLdc = 0.2*VDDQ$	0.8	1.0	1.1	RZQ/3	1,2,3
		$VOMdc = 0.5*VDDQ$	0.9	1.0	1.1	RZQ/3	1,2,3
		$VOHdc = 0.75*VDDQ$	0.9	1.0	1.3	RZQ/3	1,2,3
100	60Ω	$VOLdc = 0.2*VDDQ$	0.8	1.0	1.1	RZQ/4	1,2,3
		$VOMdc = 0.5*VDDQ$	0.9	1.0	1.1	RZQ/4	1,2,3
		$VOHdc = 0.75*VDDQ$	0.9	1.0	1.3	RZQ/4	1,2,3
101	48Ω	$VOLdc = 0.2*VDDQ$	0.8	1.0	1.1	RZQ/5	1,2,3
		$VOMdc = 0.5*VDDQ$	0.9	1.0	1.1	RZQ/5	1,2,3
		$VOHdc = 0.75*VDDQ$	0.9	1.0	1.3	RZQ/5	1,2,3
110	40Ω	$VOLdc = 0.2*VDDQ$	0.8	1.0	1.1	RZQ/6	1,2,3
		$VOMdc = 0.5*VDDQ$	0.9	1.0	1.1	RZQ/6	1,2,3
		$VOHdc = 0.75*VDDQ$	0.9	1.0	1.3	RZQ/6	1,2,3
Mismatch CA-CA within CLK group		$0.5*VDDQ$	-		2	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see TBD.

NOTE 2 Pull-Dn ODT resistors are recommended to be calibrated at $0.5*VDDQ$. Other calibration schemes may be used to achieve the linearity spec shown, e.g., calibration at $0.2*VDDQ$ and $0.75*VDDQ$.

NOTE 3 Measurement definition for RTT : TBD.

NOTE 4 CA to CA mismatch within clock group (CA) variation for a given component including CK_t and CK_c (characterized).

$$CA - CA(\text{Mismatch}) = \frac{RTT(\text{max}) - RTT(\text{min})}{RTT(\text{avg})}$$

7.6.4.1.3 ODT update time for Command/Address Bus

ODT update time for Command/Address Bus after Mode Register set are shown in Figure 148.

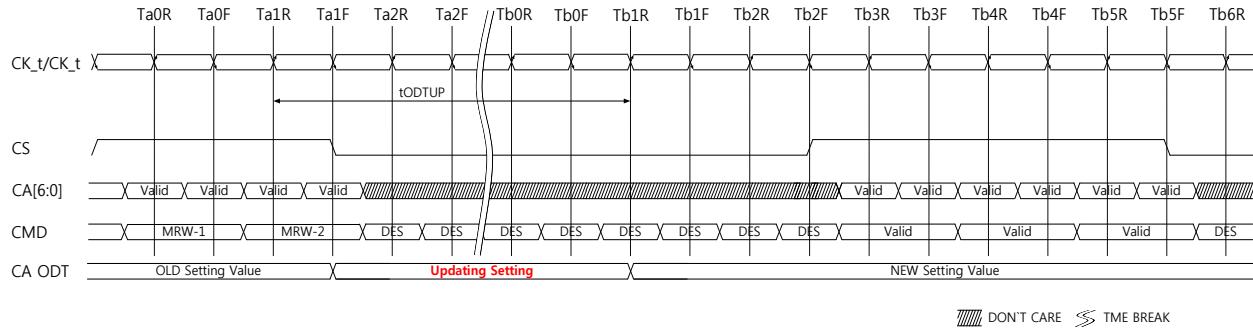


Figure 148 — ODT for Command/Address setting update timing

Table 207 — ODT Command/Address bus AC timing parameter

Speed		ALL Operation Frequency		Unit
Parameter	Symbol	MIN	MAX	
ODT C/A Value Update Time	tODTUP	-	250	ns

7.6.4.2 On-Die Termination for Data Bus

Data Bus ODT(On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DMI, RDQS_t/c signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during Write or Mask Write operation.

The Data Bus ODT feature is off and cannot be supported in Power-Down and Self-Refresh and Deep Sleep Mode states. A simple functional representation of the DRAM ODT feature is shown in **Figure 149**.

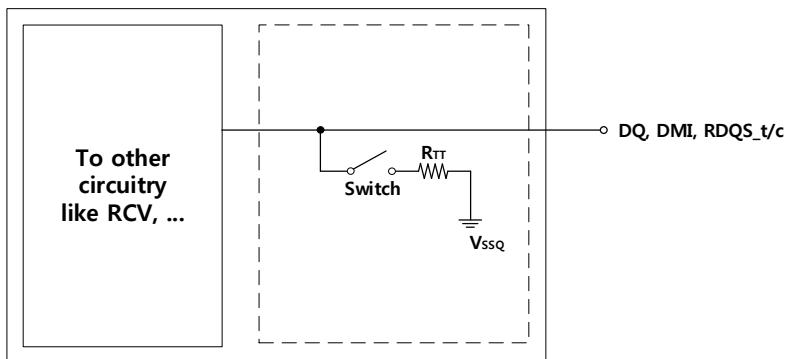


Figure 149 — Functional Representation of Data bus ODT

7.6.4.2.1 ODT Mode Register for Data Bus

The Data Bus ODT mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of RTT is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP[2:0] = 0.

7.6.4.2.2 Asynchronous ODT for Data Bus

Although ODT Mode is enabled in MR11 OP[2:0], DRAM ODT is basically Hi-Z. DRAM ODT state is automatically turned ON asynchronously based on the Write or Mask Write command that DRAM samples. After the write burst is complete, DRAM ODT state is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled.

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODTOff,min, tODTOff,max

ODTLon is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODTon reference. ODTlon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTlon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTlon latency is satisfied from the Write or Mask Write (the rising edge of the clock).

7.6.4.2.2 Asynchronous ODT for Data Bus (Cont'd)

ODTLooff is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODToff reference. ODTLooff latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLooff latency. Minimum RTT turn-off time ($t_{ODToff,min}$) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn-off time ($t_{ODToff,max}$) is the point in time when the on-die termination has reached high impedance. $t_{ODToff,min}$ and $t_{ODToff,max}$ are measured once ODTLooff latency is satisfied from the Write or Mask Write command (the rising edge of the clock).

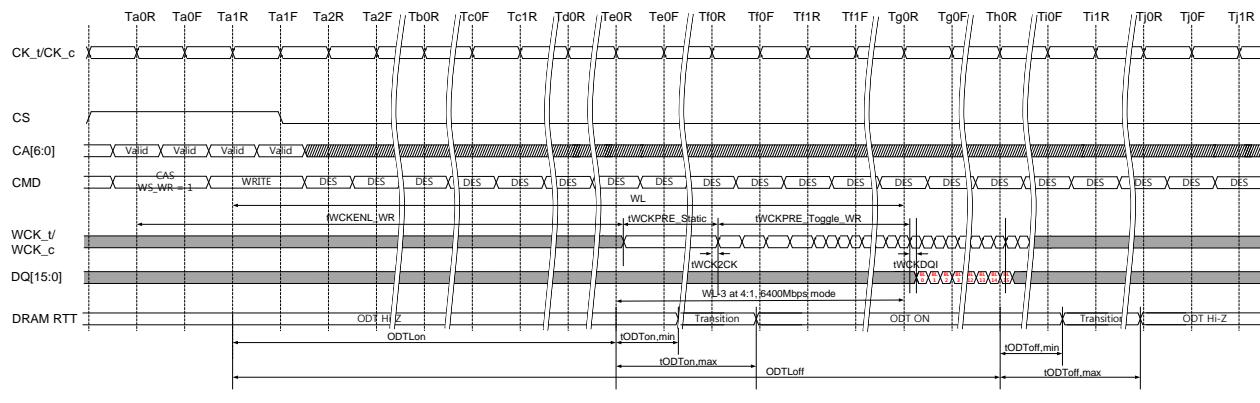
Table 208 — ODTLon and ODTLooff Latency Values

Data Rate (Mbps)	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLon Units=nCK	ODTLooff (WL + BL/n_min + RU(tWCK2DQI(max)/tCK)) Units=nCK						
					ALL mode	16BANK mode		8BANK mode		4BANK/4BG mode	
						BL16	BL32	BL32	BL16	BL32	BL32
533	2:1	10	133	WL - 1	WL + 5	WL + 9	WL + 9	-	-	-	-
1067	2:1	133	267	WL - 2	WL + 5	WL + 9	WL + 9	-	-	-	-
1600	2:1	267	400	WL - 2	WL + 5	WL + 9	WL + 9	-	-	-	-
2133	2:1	400	533	WL - 3	WL + 5	WL + 9	WL + 9	-	-	-	-
2750	2:1	533	688	WL - 3	WL + 5	WL + 9	WL + 9	-	-	-	-
3200	2:1	688	800	WL - 4	WL + 5	WL + 9	WL + 9	-	-	-	-
<hr/>											
533	4:1	5	67	WL - 1	WL + 3	WL + 5	WL + 5	-	-	-	-
1067	4:1	67	133	WL - 1	WL + 3	WL + 5	WL + 5	-	-	-	-
1600	4:1	133	200	WL - 1	WL + 3	WL + 5	WL + 5	-	-	-	-
2133	4:1	200	267	WL - 2	WL + 3	WL + 5	WL + 5	-	-	-	-
2750	4:1	267	344	WL - 2	WL + 3	WL + 5	WL + 5	-	-	-	-
3200	4:1	344	400	WL - 2	WL + 3	WL + 5	WL + 5	-	-	-	-
3733	4:1	400	467	WL - 2	-	-	WL + 5	WL + 3	WL + 7		
4267	4:1	467	533	WL - 3	-	-	WL + 5	WL + 3	WL + 7		
4800	4:1	533	600	WL - 3	-	-	WL + 5	WL + 3	WL + 7		
5500	4:1	600	688	WL - 3	-	-	WL + 5	WL + 3	WL + 7		
6000	4:1	688	750	WL - 3	-	-	WL + 5	WL + 3	WL + 7		
6400	4:1	750	800	WL - 3	-	-	WL + 5	WL + 3	WL + 7		

7.6.4.2.2 Asynchronous ODT for Data Bus (Cont'd)

Table 209 — Asynchronous ODT Turn On and Turn Off Timing

Parameter	ALL Operation Frequency	Unit
tODTon,min	1.5	ns
tODTon,max	3.5	ns
tODTOff,min	1.5	ns
tODTOff,max	3.5	ns



NOTE 1 BL=16@4Bank/4BG mode, DQ: VSSQ termination.

NOTE 2 DES commands are show for ease of illustration; other commands may be valid at these times.

Figure 150 — Asynchronous ODTon/ODToff Timing

7.6.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus

On-Die Termination effective resistance RTT is defined by MR11 OP[2:0]. ODT is applied to the DQ, DMI, RDQS_t/c pins. A functional representation of the on-die termination is shown in Figure 151.

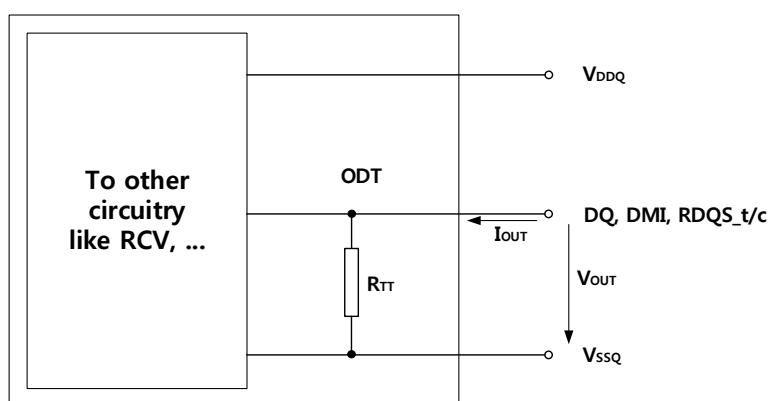


Figure 151 — On Die Termination for Data Bus

7.6.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus (Cont'd)

Table 210 — ODT DC Electrical Characteristics, assuming RZQ = 240Ω±1% over the entire operating temperature range after a proper ZQ calibration

MR11 OP[2:0]	RTT	Vout	Min	Nom	Max	Unit	Note
001	240Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ	1,2,3
010	120Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/2	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/2	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/2	1,2,3
011	80Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/3	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/3	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/3	1,2,3
100	60Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/4	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/4	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/4	1,2,3
101	48Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/5	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/5	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/5	1,2,3
110	40Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/6	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/6	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/6	1,2,3
Mismatch DQ-DQ within byte		0.5*VDDQ	-		2	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see 15.9.

NOTE 2 Pull-Dn ODT resistors are recommended to be calibrated at 0.5*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown, e.g., calibration at 0.2* VDDQ and 0.75*VDDQ.

NOTE 3 Measurement definition for RTT: TBD

NOTE 4 DQ to DQ mismatch within byte variation for a given component (characterized).

$$\text{DQ} - \text{DQ(Mismatch)} = \frac{\text{RTT(max)} - \text{RTT(min)}}{\text{RTT(avg)}}$$

7.6.4.3 On-Die Termination for WCK_t and WCK_c

WCK ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for WCK_t and WCK_c signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for DRAM devices via Mode Register setting. A simple functional representation of the DRAM ODT feature is shown in Figure 152.

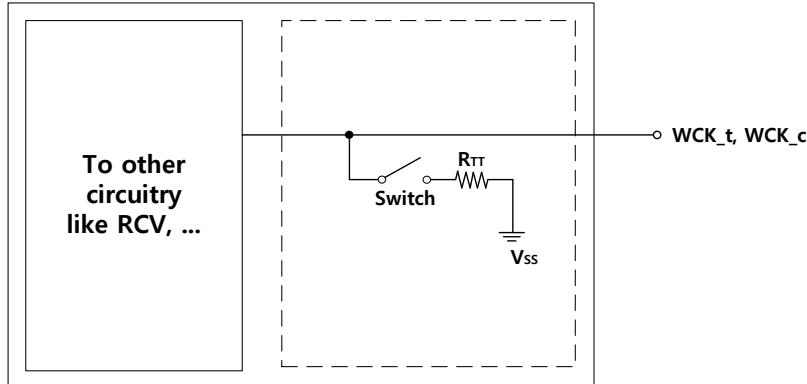


Figure 152 — Functional Representation of WCK ODT

7.6.4.3.1 ODT Mode Register for WCK_t/c

The WCK ODT termination values are set and enabled via MR18. The WCK ODT resistance values are set by MR18 OP[2:0]. The default state for the WCK is ODT disabled.

The WCK ODT of the device always maintains the present ODT status except that the device is in the Power-Down or Self-Refresh Power-Down or Deep Sleep Mode.

7.6.4.3.2 ODT during WCK2CK training

If the WCK ODT is enabled in MR18 OP[2:0], in WCK2CK training mode, DRAM always provides the termination on WCK_t/WCK_c signals with pre-defined ODT value by MR18 OP[2:0]. DQ termination is always off in WCK2CK training mode.

7.6.5 Non-target ODT

LPDDR5 supports the Non-target DRAM ODT function for DQ, DMI, and RDQS pins to improve signal integrity in 2-rank configuration. The Non-target DRAM ODT function is enabled by MR11 OP[3]=1_B and its ODT value is set by MR41 OP[7:5]. The Non-target DRAM ODT is activated at all states except TBD mode. A simple DRAM ODT configuration at Read and Write case is shown in **Figure 153**. Users should notice that NT-ODT function in stand-by state with DQ driven by high level because of leakage current from SoC to DRAM termination. Also, loopback test function for debug and testing purpose between DRAM and SOC can be supported by enabling MR41 OP[5:7] Non-target ODT setting.

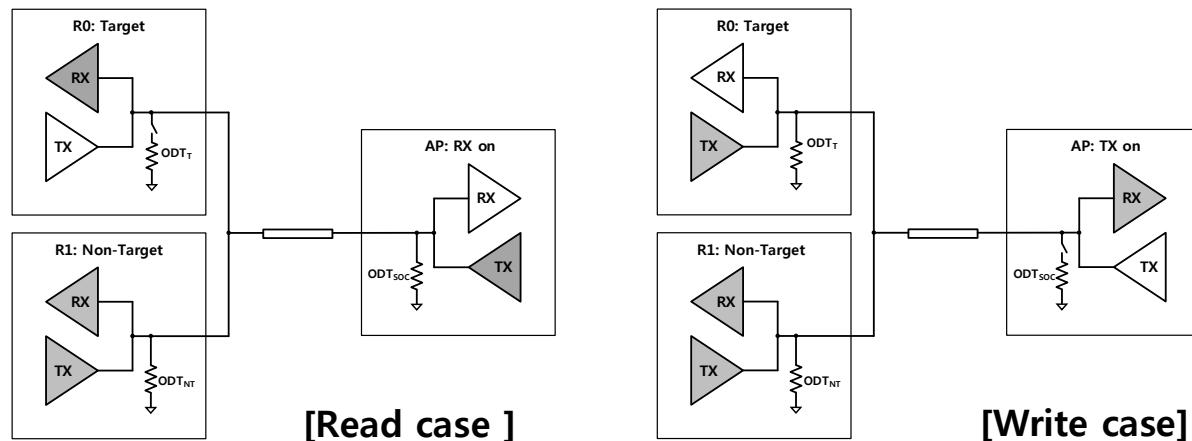


Figure 153 — DRAM ODT configuration of Non-target DRAM ODT mode

Table 211 — Non-target and Target ODT status depending on DRAM state

Current DRAM State	Non-Target DRAM	Target DRAM
Power Down	Enable (MR41 OP[7:5])	Enable (MR41 OP[7:5])
Self-Refresh Power Down	Enable (MR41 OP[7:5])	Enable (MR41 OP[7:5])
Deep Sleep Mode	TBD	
Pre-charge/Active Standby	Enable (MR41 OP[7:5])	Enable (MR41 OP[7:5])
Write/Write FIFO	Enable (MR41 OP[7:5])	Enable (MR11 OP[2:0])
Read/Read FIFO/Read DQ Calibration/MRR	Enable (MR41 OP[7:5])	PDDDS/PUDS

7.6.5.1 Non-target DRAM ODT control

In Non-Target ODT (NT-ODT) mode, Target DRAM ODT and Non-Target DRAM ODT can be set by MR41 and any combination is possible if VIH specification of DQ is satisfied for Write operation. In Read operation, since DRAM calibrates Pull-Up strength to satisfy VOH specification according as SoC ODT of MR17 OP[2:0], SoC ODT of MR17 OP[2:0] should be the same as equivalent resistance of NT-ODT (MR41 OP[7:5]) and ODT of SoC Rx. Notice that the ODT value of non-target rank should be always one fixed level irrespective of read/write operation and NT-ODT should be disabled in case of VRO enabled by MR13 OP[2]. Refer to the table below for more information.

Table 212 — Normal Mode vs. NT-ODT Mode for Write Operation

Mode MR11 OP[3]	Target Rank ODT	Non-Target Rank ODT	Equivalent ODT of 2-Rank DRAM
OP[3]=0 (Normal Mode)	MR11 OP[2:0] (ODT _T)	Disable	ODT _T
OP[3]=1 (NT-ODT Mode)	MR11 OP[2:0] (ODT _T)	MR41 OP[7:5] (ODT _{NT})	ODT _T ODT _{NT}

Table 213 — Normal Mode vs. NT-ODT Mode for Read Operation

Mode MR11 OP[3]	Non-Target Rank ODT	SoC Rx ODT	Equivalent ODT for RD operation	MR17 OP[2:0] (SoC ODT for DRAM Pull-Up Cal.)
OP[3]=0 (Normal Mode)	Disable	ODT _{SOC}	ODT _{SOC}	ODT _{SOC}
OP[3]=1 (NT-ODT Mode)	MR41 OP[7:5] (ODT _{NT})	ODT _{SOC}	ODT _{NT} ODT _{SOC}	ODT _{NT} ODT _{SOC} ¹

NOTE 1 Since SoC ODT of MR17 can only support RZQ/n (n=1,2,3,4,5,6), (ODT_{NT}||ODT_{SOC}) should be one of RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, and RZQ/6.

7.6.5.1 Non-target DRAM ODT control (Cont'd)

Table 214 shows all combinations that equivalent ODT is RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, or RZQ/6.

Table 214 — Combination of Target ODT, Non-target ODT and SoC ODT

ODT_{NT}	ODT_T	ODT_{SoC}	Write ($ODT_{eq}=ODT_{NT} \parallel ODT_T$)	Read (SoC ODT MR17 OP[2:0])
RZQ/1	RZQ/1	RZQ/0	RZQ/2	RZQ/1
	RZQ/2	RZQ/1	RZQ/3	RZQ/2
	RZQ/3	RZQ/2	RZQ/4	RZQ/3
	RZQ/4	RZQ/3	RZQ/5	RZQ/4
	RZQ/5	RZQ/4	RZQ/6	RZQ/5
	-	RZQ/5	-	RZQ/6
RZQ/2	RZQ/1	RZQ/0	RZQ/3	RZQ/2
	RZQ/2	RZQ/1	RZQ/4	RZQ/3
	RZQ/3	RZQ/2	RZQ/5	RZQ/4
	RZQ/4	RZQ/3	RZQ/6	RZQ/5
	-	RZQ/4	-	RZQ/6
RZQ/3	RZQ/1	RZQ/0	RZQ/4	RZQ/3
	RZQ/2	RZQ/1	RZQ/5	RZQ/4
	RZQ/3	RZQ/2	RZQ/6	RZQ/5
	-	RZQ/3	-	RZQ/6
RZQ/4	RZQ/1	RZQ/0	RZQ/5	RZQ/4
	RZQ/2	RZQ/1	RZQ/6	RZQ/5
	-	RZQ/2	-	RZQ/6
RZQ/5	RZQ/1	RZQ/0	RZQ/6	RZQ/5
	-	RZQ/1	-	RZQ/6
RZQ/6	RZQ/0	RZQ/0	RZQ/6	RZQ/6

7.6.5.1 Non-target DRAM ODT control (Cont'd)

Table 215 — DQ ODT setting example for Write Operation in NT-ODT Mode

Link ECC	DBI-WR MR3 OP[7]	DMD MR13 OP[5]	RDQS MR20 OP[1:0]	DQ	DMI	RDQS_t	RDQS_c
Dis-abled	0 _B	0 _B	00 _B	NT-ODT	NT-ODT	Disable	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	Disable	NT-ODT
		1 _B	00 _B	NT-ODT	Disable	Disable	Disable
			01 _B	NT-ODT	Disable	NT-ODT	Disable
			10 _B	NT-ODT	Disable	NT-ODT	NT-ODT
			11 _B	NT-ODT	Disable	Disable	NT-ODT
	1 _B	0 _B	00 _B	NT-ODT	NT-ODT	Disable	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	Disable	NT-ODT
		1 _B	00 _B	NT-ODT	NT-ODT	Disable	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	Disable	NT-ODT
En-abled	0 _B	0 _B	00 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
		1 _B	00 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
	1 _B	0 _B	00 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
		1 _B	00 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			01 _B	NT-ODT	NT-ODT	NT-ODT	Disable
			10 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT
			11 _B	NT-ODT	NT-ODT	NT-ODT	NT-ODT

7.6.5.2 Asynchronous NT-ODT

The NT-ODT is enabled by MR11 OP[3] and a target ODT of DRAM is controlled by Write, Mask Write or Read command. In stand-by mode except TBD, the ODT of each DRAM is turned on with NT-ODT value (MR41 OP[2:0]). When Write, Mask Write or Read command is issued to the target DRAM, According to timing parameters like ODTLon(_RD), tODT_(RD)on, ODTLoff(_RD) or tODT_(RD)off, the ODT of the target DRAM is controlled.

Following timing parameters apply when DRAM NT-ODT mode is enabled.

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODTOff,min, tODTOff,max
- ODTLon_RD, tODT_RDon,min, tODT_RDon,max
- ODTLoff_RD, tODT_RDOff,min, tODT_RDOff,ma

ODTLon is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODTon reference. ODTLon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from the Write or Mask Write command.

ODTloff is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODTOff reference. ODTloff latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTloff latency. Minimum RTT turn-off time (tODTOff,min) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODTOff,max) is the point in time when the on-die termination has reached high impedance. tODTOff,min and tODTOff,max are measured once ODTloff latency is satisfied from the Write or Mask Write command.

ODTloff_RD is a synchronous parameter and it is the latency from the Read command(the rising edge of the clock) to tODT_RDOff reference. ODTloff_RD latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTloff_RD latency. Minimum RTT turn-off time (tODT_RDOff,min) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODT_RDOff,max) is the point in time when the on-die termination has reached high impedance. tODT_RDOff,min and tODT_RDOff,max are measured once ODTloff latency is satisfied from the Read command.

ODTLon_RD is a synchronous parameter and it is the latency from the Read command (the rising edge of the clock) to tODT_RDon reference. ODTLon_RD latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon_RD latency. Minimum RTT turn-on time (tODT_RDon,min) is the point in time when the device termination circuit leaves high impedance state and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODT_RDon,max) is the point in time when the ODT resistance is fully on. tODT_RDon,min and tODT_RDon,max are measured once ODTLon_RD latency is satisfied from the Read command.

7.6.5.2 Asynchronous NT-ODT (Cont'd)

Table 216 — ODTLon and ODTLoff Latency Values for Write

Data Rate	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLon Units=nCK	ODTLoff (WL + BL/n_min + RU(tWCK2DQI(max)/tCK)) Units=nCK				
					ALL mode		16BANK mode		8BANK mode
				BL32	BL16	BL32	BL32	BL16	BL32
533	2:1	10	133	WL - 1	WL + 5	WL + 9	WL + 9	-	-
1067	2:1	133	267	WL - 2	WL + 5	WL + 9	WL + 9	-	-
1600	2:1	267	400	WL - 2	WL + 5	WL + 9	WL + 9	-	-
2133	2:1	400	533	WL - 3	WL + 5	WL + 9	WL + 9	-	-
2750	2:1	533	688	WL - 3	WL + 5	WL + 9	WL + 9	-	-
3200	2:1	688	800	WL - 4	WL + 5	WL + 9	WL + 9	-	-
<hr/>									
533	4:1	5	67	WL - 1	WL + 3	WL + 5	WL + 5	-	-
1067	4:1	67	133	WL - 1	WL + 3	WL + 5	WL + 5	-	-
1600	4:1	133	200	WL - 1	WL + 3	WL + 5	WL + 5	-	-
2133	4:1	200	267	WL - 2	WL + 3	WL + 5	WL + 5	-	-
2750	4:1	267	344	WL - 2	WL + 3	WL + 5	WL + 5	-	-
3200	4:1	344	400	WL - 2	WL + 3	WL + 5	WL + 5	-	-
3733	4:1	400	467	WL - 2	-	-	WL + 5	WL + 3	WL + 7
4267	4:1	467	533	WL - 3	-	-	WL + 5	WL + 3	WL + 7
4800	4:1	533	600	WL - 3	-	-	WL + 5	WL + 3	WL + 7
5500	4:1	600	688	WL - 3	-	-	WL + 5	WL + 3	WL + 7
6000	4:1	688	750	WL - 3	-	-	WL + 5	WL + 3	WL + 7
6400	4:1	750	800	WL - 3	-	-	WL + 5	WL + 3	WL + 7

NOTE 1 ODTLoff is not related to WCK post-amble because the ODT of WCK is always turned on or off.

Table 217 — Asynchronous NT-ODT Turn On and Turn off Timing for Write

Parameter	ALL Operation Frequency	Unit
tODTon,min	1.5	ns
tODTon,max	3.5	ns
tODToff,min	1.5	ns
tODToff,max	3.5	ns

7.6.5.2 Asynchronous NT-ODT (Cont'd)

Table 218 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS disabled

Data Rate	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTloff_RD Units=nCK	ODTLon_RD (RL + BL/n_min + RU(tWCK2DQO(max)/tCK)) Units=nCK					
					ALL mode	16BANK mode		8BANK mode	4BANK/4BG mode	
						BL16	BL32	BL32	BL16	BL32
533	2:1	10	133	RL - 1	RL + 5	RL + 9	RL + 9	-	-	
1067	2:1	133	267	RL - 2	RL + 5	RL + 9	RL + 9	-	-	
1600	2:1	267	400	RL - 2	RL + 5	RL + 9	RL + 9	-	-	
2133	2:1	400	533	RL - 3	RL + 6	RL + 10	RL + 10	-	-	
2750	2:1	533	688	RL - 3	RL + 6	RL + 10	RL + 10	-	-	
3200	2:1	688	800	RL - 4	RL + 6	RL + 10	RL + 10	-	-	
533	4:1	5	67	RL - 1	RL + 3	RL + 5	RL + 5	-	-	
1067	4:1	67	133	RL - 1	RL + 3	RL + 5	RL + 5	-	-	
1600	4:1	133	200	RL - 1	RL + 3	RL + 5	RL + 5	-	-	
2133	4:1	200	267	RL - 2	RL + 3	RL + 5	RL + 5	-	-	
2750	4:1	267	344	RL - 2	RL + 3	RL + 5	RL + 5	-	-	
3200	4:1	344	400	RL - 2	RL + 3	RL + 5	RL + 5	-	-	
3733	4:1	400	467	RL - 2	-	-	RL + 5	RL + 3	RL + 7	
4267	4:1	467	533	RL - 3	-	-	RL + 6	RL + 4	RL + 8	
4800	4:1	533	600	RL - 3	-	-	RL + 6	RL + 4	RL + 8	
5500	4:1	600	688	RL - 3	-	-	RL + 6	RL + 4	RL + 8	
6000	4:1	688	750	RL - 3	-	-	RL + 6	RL + 4	RL + 8	
6400	4:1	750	800	RL - 3	-	-	RL + 6	RL + 4	RL + 8	

7.6.5.2 Asynchronous NT-ODT (Cont'd)

Table 219 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS enabled & MR10 OP[5:4]=00_B, 01_B, 10_B

Data Rate	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLoff_RD Units=nCK	ODTLon_RD (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2) Units=nCK at CKR=2:1					
					ODTLon_RD (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK at CKR=4:1					
					ALL mode	16BANK mode		8BANK mode	4BANK/4BG mode	
						BL16	BL32	BL32	BL16	BL32
533	2:1	10	133	RL - 3	RL + 7	RL + 11	RL + 11	-	-	-
1067	2:1	133	267	RL - 4	RL + 7	RL + 11	RL + 11	-	-	-
1600	2:1	267	400	RL - 4	RL + 7	RL + 11	RL + 11	-	-	-
2133	2:1	400	533	RL - 5	RL + 8	RL + 12	RL + 12	-	-	-
2750	2:1	533	688	RL - 5	RL + 8	RL + 12	RL + 12	-	-	-
3200	2:1	688	800	RL - 6	RL + 8	RL + 12	RL + 12	-	-	-
<hr/>										
533	4:1	5	67	RL - 2	RL + 4	RL + 6	RL + 6	-	-	-
1067	4:1	67	133	RL - 2	RL + 4	RL + 6	RL + 6	-	-	-
1600	4:1	133	200	RL - 2	RL + 4	RL + 6	RL + 6	-	-	-
2133	4:1	200	267	RL - 3	RL + 4	RL + 6	RL + 6	-	-	-
2750	4:1	267	344	RL - 3	RL + 4	RL + 6	RL + 6	-	-	-
3200	4:1	344	400	RL - 3	RL + 4	RL + 6	RL + 6	-	-	-
3733	4:1	400	467	RL - 3	-	-	RL + 6	RL + 4	RL + 8	
4267	4:1	467	533	RL - 4	-	-	RL + 7	RL + 5	RL + 9	
4800	4:1	533	600	RL - 4	-	-	RL + 7	RL + 5	RL + 9	
5500	4:1	600	688	RL - 4	-	-	RL + 7	RL + 5	RL + 9	
6000	4:1	688	750	RL - 4	-	-	RL + 7	RL + 5	RL + 9	
6400	4:1	750	800	RL - 4	-	-	RL + 7	RL + 5	RL + 9	

7.6.5.2 Asynchronous NT-ODT (Cont'd)

Table 220 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS enabled & MR10 OP[5:4]=11_B

Data Rate	WCK:CK Ratio	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLoff_RD Units=nCK	ODTLon_RD (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK, at CKR=4:1					
					ALL mode	16BANK mode		8BANK mode	4BANK/4BG mode	
						BL16	BL32	BL32	BL16	BL32
3733	4:1	400	467	RL - 4	-	-	RL + 6	RL + 4	RL + 8	
4267	4:1	467	533	RL - 5	-	-	RL + 7	RL + 5	RL + 9	
4800	4:1	533	600	RL - 5	-	-	RL + 7	RL + 5	RL + 9	
5500	4:1	600	688	RL - 5	-	-	RL + 7	RL + 5	RL + 9	
6000	4:1	688	750	RL - 5	-	-	RL + 7	RL + 5	RL + 9	
6400	4:1	750	800	RL - 5	-	-	RL + 7	RL + 5	RL + 9	

Table 221 — Asynchronous NT-ODT Turn On and Turn Off Timing

Parameter	ALL Operation Frequency	Unit
tODT_RDon,min	1.5	ns
tODT_RDon,max	3.5	ns
tODT_RDOff,min	1.5	ns
tODT_RDOff,max	3.5	ns

7.6.5.3 Timing diagram of Write case

In Non-target DRAM ODT enabled mode, ODT timings (ODTLon) are referenced to WL after the write command and the ODT value in target rank can be updated within tODTon,max as shown in Figure 154. After write operation, target ODT value should be recovered to pre-defined Non-target DRAM ODT value within the tODTOff,max.

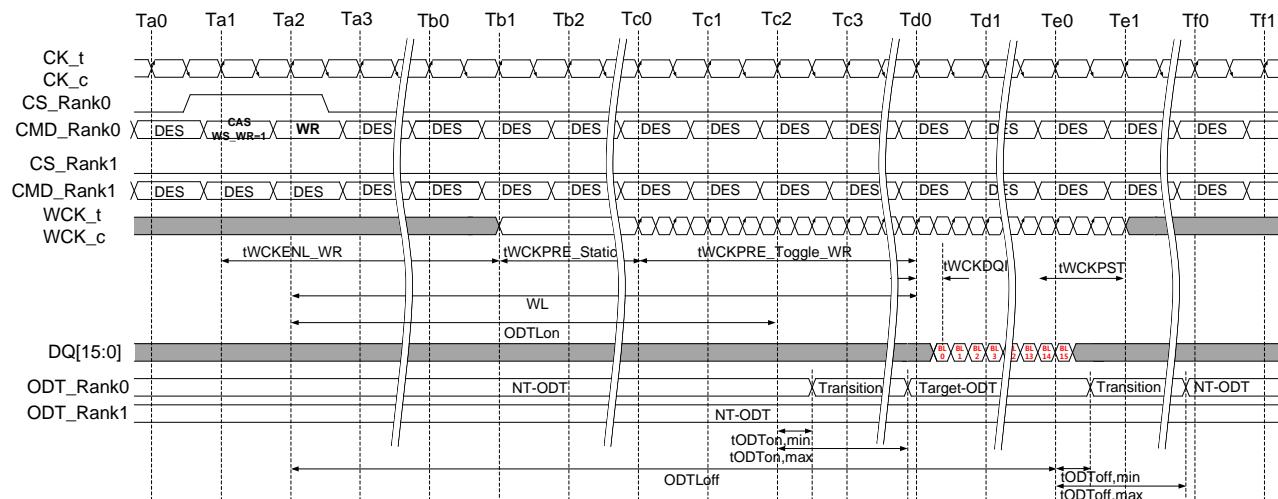


Figure 154 — ODT Control on Non-target DRAM for Write

7.6.5.4 Timing diagram of Read case

In Non-target DRAM ODT enabled mode, ODT timings (ODT_{loff}_RD) are referenced to RL after the read command and the ODT value in target rank is disabled within tODT_{RDoff,max} as shown in Figure 155. After read operation, disabled ODT should be recovered to pre-defined Non-target DRAM ODT value within the tODT_{RDon,max}.

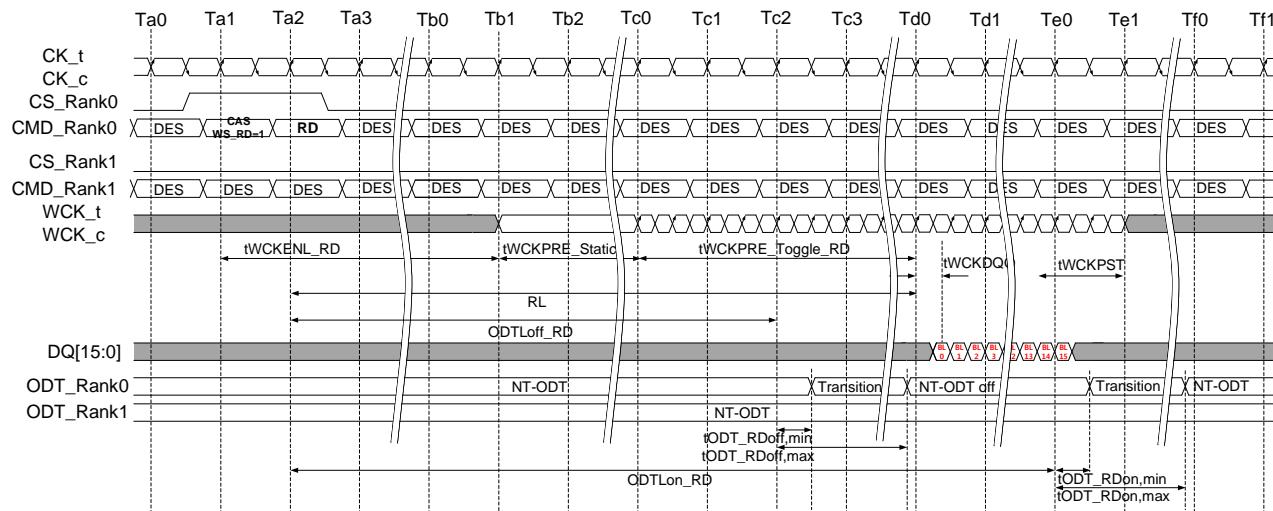


Figure 155 — ODT Control on Non-target DRAM for Read

7.6.6 Input Clock Stop and Frequency Change

LPDDR5 SDRAM supports input clock frequency change under the following conditions:

- tCK(abs)min is met for each clock cycle.
- Refresh requirements apply during clock frequency change.
- All banks are required to be idle state or during tRFC.
- The certain timing conditions such as tRCD, tWR, tWRA, tMRW, tMRR have been met prior to changing the frequency.
- CS shall be held LOW during clock frequency change.
- The LPDDR5 SDRAM is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of TBD.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR5 SDRAM supports clock stop under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop.
- CS shall be held LOW during clock stop.
- Refresh requirements apply during clock stop.
- All banks are required to be idle state or during tRFC.
- The certain timing conditions such as tRCD, tWR, tRP, tMRW, tMRR, tZQLAT, etc. have been met prior to stopping the clock.
- Read with auto precharge and write with auto precharge commands need extra TBD clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations.

7.6.6 Input Clock Stop and Frequency Change (Cont'd)

- REFab, REFab, SRE, SRX and ZQcal Start commands are required to have TBD additional clocks prior to stopping the clock.
- The LPDDR5 SDRAM is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of TBD.

7.6.7 V_{REF} Current Generator (VRCG)

LPDDR5 SDRAM VREF current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal V_{REF}(DQ) and V_{REF}(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR16 OP[6] = 1. Only Deselect commands may be issued until tVRCG_ENABLE is satisfied. tVRCG_ENABLE timing is shown in Figure 156.

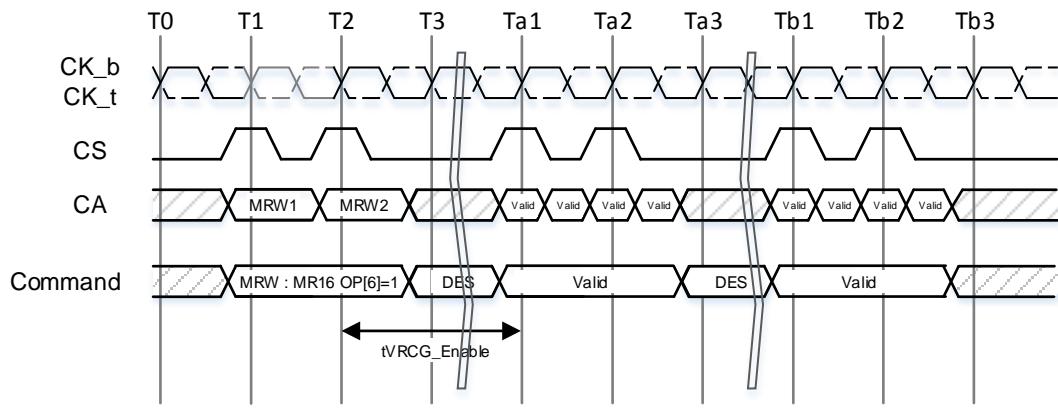


Figure 156 — VRCG Enable Timing

VRCG high current mode is disabled by setting MR16 OP[6] = 0. Only Deselect commands may be issued until tVRCG_DISABLE is satisfied. tVRCG_DISABLE timing is shown in Figure 157.

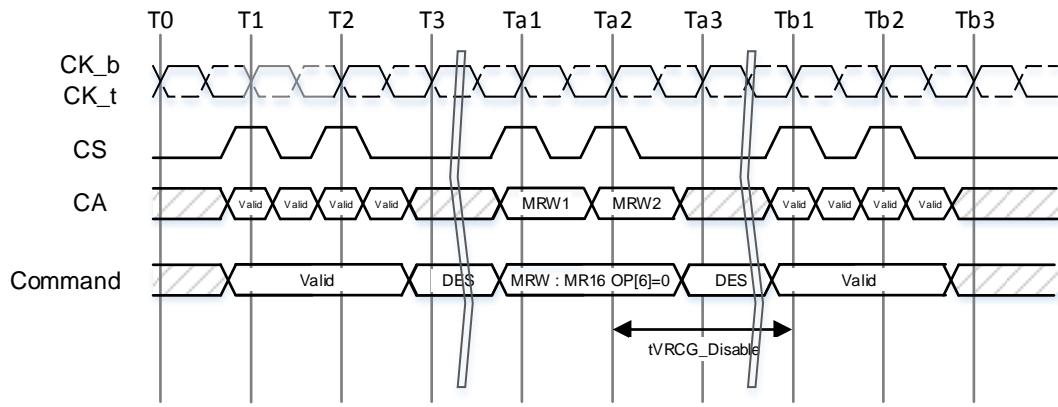


Figure 157 — VRCG Disable Timing

Note that LPDDR5 SDRAM devices support V_{REF}(CA) and V_{REF}(DQ) range and value changes without enabling VRCG high current mode.

Table 222 — VRCG Enable / Disable Timing

Parameter	Symbol	Min	Max	Unit	Note
V _{REF} High Current Mode Enable Time	tVRCG_ENABLE		150	ns	
V _{REF} High Current Mode Disable Time	tVRCG_DISABLE		100	ns	

7.6.8 Thermal Offset

Because of their tight thermal coupling with the LPDDR5 device, hot spots on an SOC can induce thermal gradients across the LPDDR5 device. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR13 OP[1:0]. This temperature offset may modify refresh behavior. It will take a max of 200us to have the change reflected in MR4 OP[4:0]. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR5 memory controller.

7.6.9 Temperature Sensor

LPDDR5 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR5 devices shall monitor device temperature and update MR4 according to tTSI. Device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in self refresh state.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[4:0] equals 'b01001. LPDDR5 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

7.6.9 Temperature Sensor (Cont'd)

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2^{\circ}\text{C}$$

Table 223 — Temperature Sensor

Parameter	Symbol	Max/ Min	Value	Unit	Note
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms: $(10^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^{\circ}\text{C}$.

In this case, ReadInterval shall be no greater than 167 ms.

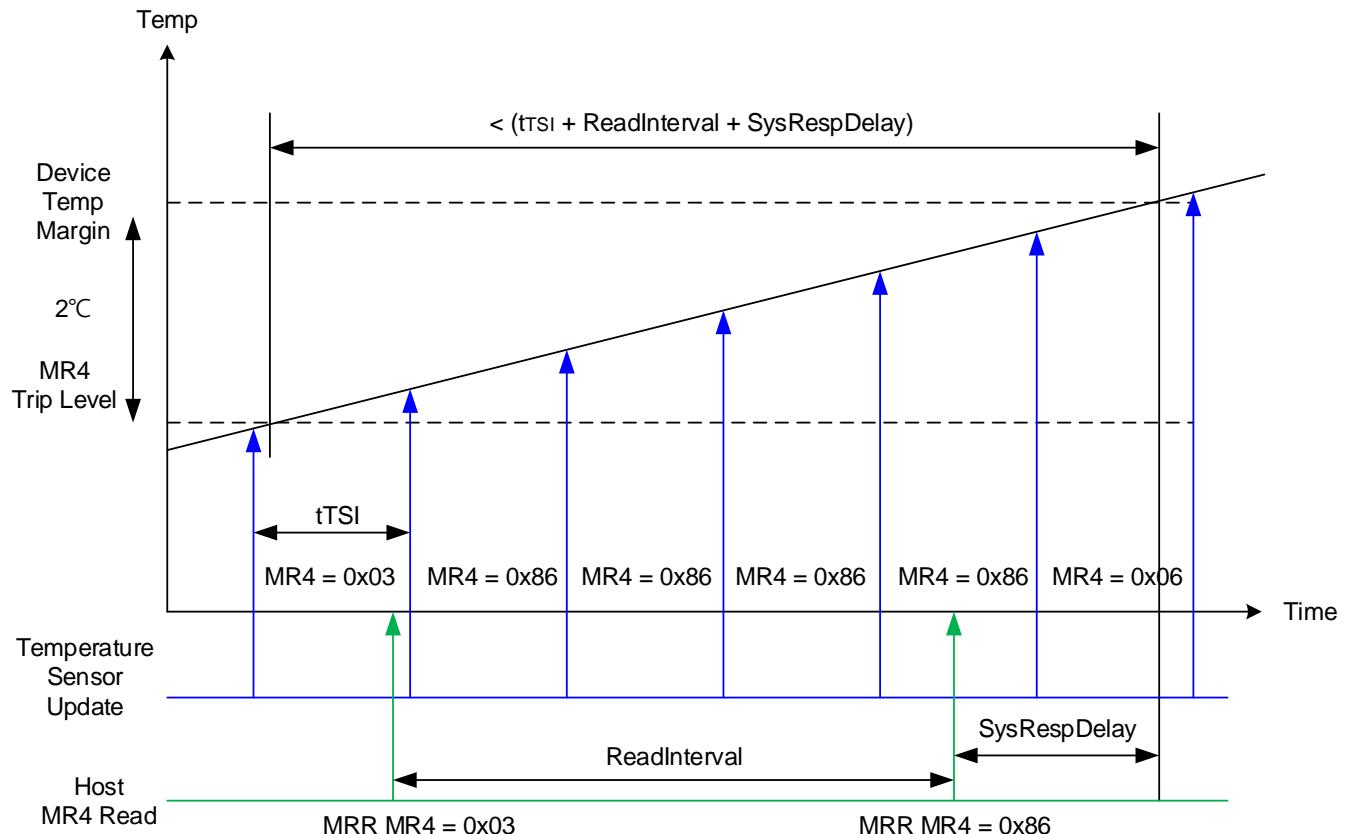


Figure 158 — Temp Sensor Timing

7.6.10 Multi-Purpose Command (MPC)

LPDDR5 SDRAM uses the MPC command to issue commands about ZQ calibration and WCK2DQx Interval Oscillator. The MPC command is initiated with CS, and CA[6:0] asserted to the proper state at the crossing points of CK_t and CK_c, as defined by the Command Truth Table, **Table 154**. The MPC command has eight operands (OP[7:0]) that are decoded to execute specific commands in the SDRAM. OP[7] is a special bit that is decoded on the first crossing point of CK_t and CK_c of the MPC command.

The MPC command supports the following functions:

- Start WCK2DQI Interval Oscillator
- Stop WCK2DQI Interval Oscillator
- Start WCK2DQO Interval Oscillator
- Stop WCK2DQO Interval Oscillator
- ZQ CAL Start
- ZQ CAL Latch

Table 224 — MPC Command Definition

SDRAM COMMAND	DDR COMMAND PINS								CK_t edge	Notes
	CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6		
MULTI PURPOSE COMMAND (MPC)	H	L	L	L	L	H	H	OP7	↑ R1	
	X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	↓ F1	

Table 225 — MPC Command Definition for OP[7:0]

Function	Operand	Data	Notes
Commands	OP[7:0]	10000001 _B : Start WCK2DQI Interval Oscillator 10000010 _B : Stop WCK2DQI Interval Oscillator 10000011 _B : Start WCK2DQO Interval Oscillator 10000100 _B : Stop WCK2DQO Interval Oscillator 10000101 _B : ZQ CAL Start 10000110 _B : ZQ CAL Latch All Others: Reserved	

7.6.11 tWCK2DQ Interval Oscillator

As voltage and temperature change on the SDRAM die, the WCK clock tree delay will shift and may require re-training. The LPDDR5-SDRAM includes an internal CK based WCK2DQx Interval Oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The CK based WCK2DQx Interval Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error in WCK clock tree. In order to provide low power interval oscillator to user, the WCK2DQx Interval Oscillator counts the number of CK cycles, not the number of WCK cycles.

The WCK2DQx Interval Oscillator is started by issuing a MPC [Start WCK2DQI Osc] or MPC [Start WCK2DQO Osc] command with OP[7:0] set as described in the MPC Operation section, which will start an internal ring oscillator. A counter is implemented to count the number of times a signal propagates through a replica of the WCK clock tree, the established time interval.

7.6.11 tWCK2DQ Interval Oscillator (Cont'd)

The WCK2DQx Interval Oscillator may be stopped by issuing a MPC [Stop WCK2DQI Osc] or MPC [Stop WCK2DQO Osc] command with OP[7:0] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR37/MR40 for more information). If MR37 or MR40 is set to automatically stop the WCK2DQx Interval Oscillator, then the MPC [Stop WCK2DQI Osc] or MPC [Stop WCK2DQO Osc] command should not be used (illegal). When the WCK2DQx Interval Oscillator is stopped by either method, the result of the oscillator counter for WCK2DQI is automatically stored in MR35 and MR36, and the data for WCK2DQO is also stored in MR38 and MR39.

A new MPC [Start WCK2DQI Osc] or MPC [Start WCK2DQO Osc] command with OP[6:0] can be issued, and the new MPC [Start WCK2DQI Osc] or MPC [Start WCK2DQO Osc] command will reset the stored result in MR35/36 or MR38/39, respectively. If power down command is issued while WCK2DQ Interval Oscillator is operating, DRAM will stop operating oscillator. In this case, results stored in MR35/36 or MR38/39 are invalid and shall be ignored.

WCK2DQI Interval Oscillator and WCK2DQO Interval Oscillator cannot be operated Simultaneously. After completing WCK2DQI(or WCK2DQO) Interval Oscillator operation, WCK2DQO (or WCK2DQI) Interval Oscillator Start MPC can be issued.

The controller may adjust the accuracy of the result by running the WCK2DQx Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{WCK2DQx Interval Oscillator Granularity Error} = \frac{2 * (\text{WCK2DQx Delay})}{\text{Run Time}}$$

Where:

Run Time = Total time between start and stop commands

WCK2DQ delay = the value of the WCK clock tree delay (tWCK2DQ min/max)

Additional matching error must be included, which is the difference between WCK training circuit and the actual WCK clock tree across voltage and temperature. Therefore, the total accuracy of the WCK2DQx Interval Oscillator counter is given by:

$$\text{WCK2DQx Interval Oscillator Accuracy} = 1 - \text{Granularity Error} - \text{Matching Error}$$

Example: If the total time between start and stop commands is 200ns, and the maximum WCK clock tree delay is 1600ps (tWCK2DQO max), then the WCK Oscillator Granularity Error is:

$$\text{WCK2DQx Interval Oscillator Granularity Error} = \frac{2 * (1.6\text{ns})}{200\text{ns}} = 1.6\%$$

This equates to a granularity timing error of 25.6ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{WCK2DQx Interval Oscillator Accuracy} = 1 - \frac{25.6\text{ps} + 5.5\text{ps}}{1600\text{ps}} = 98.06\%$$

7.6.11 tWCK2DQ Interval Oscillator (Cont'd)

Example: Running the WCK Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum WCK clock tree delay is 1600ps (tWCK2DQO max), then the WCK Oscillator Granularity Error is:

$$\text{WCK2DQx Oscillator Granularity Error} = \frac{2 * (1.6\text{ns})}{500\text{ns}} = 0.64\%$$

This equates to a granularity timing error of 10ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{WCK2DQx Oscillator Accuracy} = 1 - \frac{10\text{ps} + 5.5\text{ps}}{1600\text{ps}} = 99.0\%$$

The result of the WCK2DQx Interval Oscillator is defined as the number of CK cycles which reflects WCK Clock Tree Delays that are counted during the run time determined by the controller. The result for WCK2DQI is stored in MR35-OP[7:0] and MR36-OP[7:0], and that for WCK2DQO is also stored in MR38-OP[7:0] and MR39-OP[7:0]. MR35 and MR38 contain the least significant bits (LSB) of the result for WCK2DQI and WCK2DQO, respectively. MR36 and MR39 contain the most significant bits (MSB) of the result for WCK2DQI and WCK2DQO, respectively.

MR35 and MR36 are overwritten by the SDRAM when a MPC-1 [Stop WCK2DQI Osc] command is received. Similarly, for a WCK2DQI stop command, MR38 and MR39 is also overwritten when SDRAM receives MPC-1 [Stop WCK2DQO Osc] command.

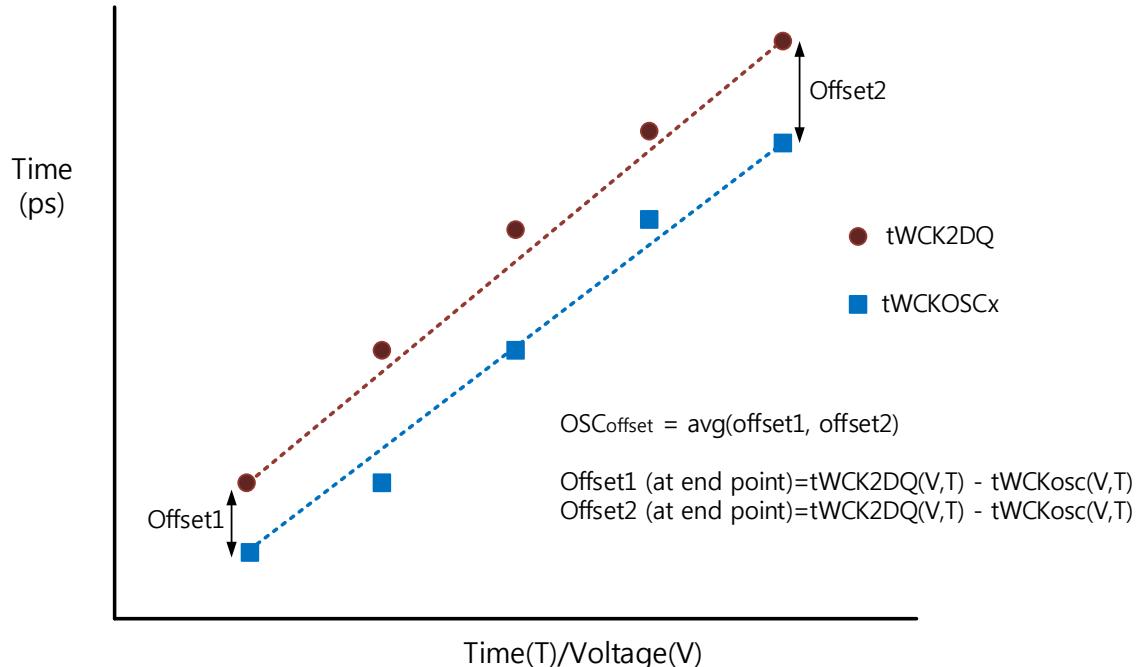
The SDRAM counter will count to its maximum value ($=2^{16}$) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest “run time” for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest WCK2DQI Run Time Interval} = 2^{16} * \text{tWCK2DQ(min)} = 2^{16} * 0.3\text{ns} = 19.66\text{us}$$

$$\text{Longest WCK2DQO Run Time Interval} = 2^{16} * \text{tWCK2DQ(min)} = 2^{16} * 0.65\text{ns} = 42.6\text{us}$$

7.6.11.1 Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the WCK training circuit (interval oscillator) and the actual WCK clock tree across voltage and temperature.



- $\text{OSC}_{\text{Match}}: \text{OSC}_{\text{Match}} = [\text{tWCK2DQ}_{(V,T)} - \text{tWCKosc}_{(V,T)} - \text{OSCOffset}]$
- $\text{tWCK}_{\text{osc}} : \text{tWCKosc}(V, T) = \frac{\text{Run Time}}{2 * \text{Count}}$

Figure 159 — Interval oscillator offset

Table 226 — WCK Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Units	Notes
Write WCK Oscillator Matching Error: voltage variation	WOSC _{Match_volt}	TBD	TBD	ps	1,2,3
Write WCK Oscillator Error: Temperature variation	WOSC _{Match_temp}	TBD	TBD	ps	1,2,3
Write WCK Oscillator Offset	WOSC _{offset}	TBD	TBD	ps	2
Read WCK Oscillator Matching Error: voltage variation	ROSC _{Match_volt}	TBD	TBD	ps	1,2,3
Read WCK Oscillator Error: Temperature variation	ROSC _{Match_temp}	TBD	TBD	ps	1,2,3
Read WCK Oscillator Offset	ROSC _{offset}	TBD	TBD	ps	2

NOTE 1 The WOSCmatch or ROSCmatch is the matching error per between the actual WCK and WCK interval oscillator over voltage and temp.

NOTE 2 This parameter will be characterized or guaranteed by design.

NOTE 3 The input stimulus for tWCK2DQ will be consistent over voltage and temp conditions.

NOTE 4 tWCK2DQ(V,T) delay will be the average of WCK to DQ delay over the runtime period.

7.7 Specific features, Reliability & Power-optimization

7.7.1 Dynamic Voltage and Frequency Scaling (DVFS)

LPDDR5 Dynamic Voltage and Frequency Scaling (DVFS) consists of two modes intended to reduce the LPDRAM energy consumption. The two modes are DVFSC (DVFS Core) and DVFSQ (DVFS VDDQ).

7.7.1.1 DVFSC Mode

In DVFSC mode, when enabled by MR19 OP[1:0]=01B, the LPDRAM may operate internal circuitry from either the VDD2H rail or the VDD2L rail. When the memory controller commands a FSP change, the LPDRAM may internally switch some internal circuits from one rail to the other. This switching will complete within tFC, when normal operation at the new frequency set point may commence. DVFSC mode changes are only allowed as part of FSP-OP switching. Changes to DVFSC mode by direct programming of MR19 OP[1:0] for the current operating point are illegal.

Some LPDRAM operations will take longer to complete when DVFSC is enabled. Latencies and AC timing parameters are specified in separate tables depending on the current DVFSC state of the LPDRAM.

Application usage of DVFSC mode is optional. Systems which will not implement DVFSC must supply the specified VDD2H voltage level to both the VDD2H and VDD2L rails of the LPDRAM, and must set MR13 OP[7]=1 and MR19 OP[1:0]=00_B at all times.

Figure 160 and Figure 161 illustrate DVFSC high-to-low and low-to-high timing respectively. In these diagrams commands other than the FSP switch are shown as examples only – other commands are also valid except read or write commands. For more information on FSP switching refer to 7.6.3, Frequency Set Points.

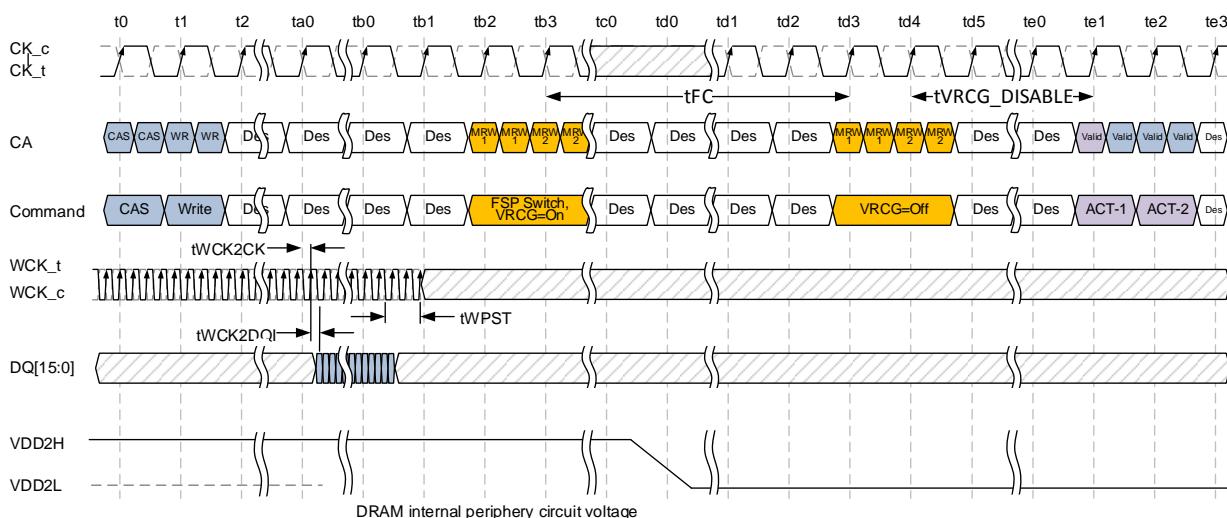


Figure 160 — DVFSC High (VDD2H) to Low (VDD2L) Transition

7.7.1.1 DVFSC Mode (Cont'd)

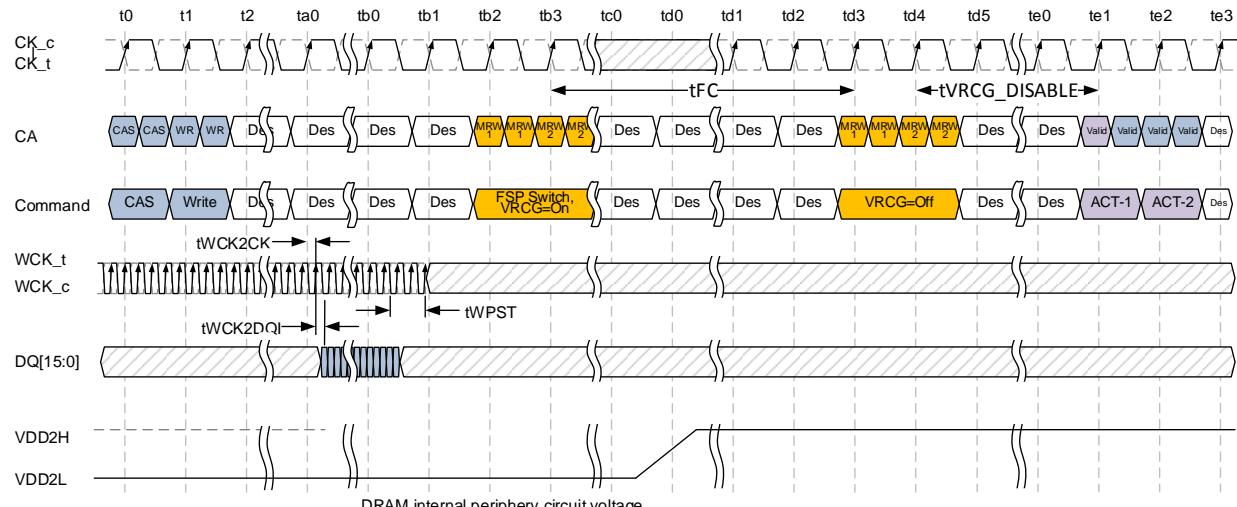


Figure 161 — DVFSC Low (VDD2L) to High (VDD2H) Transition

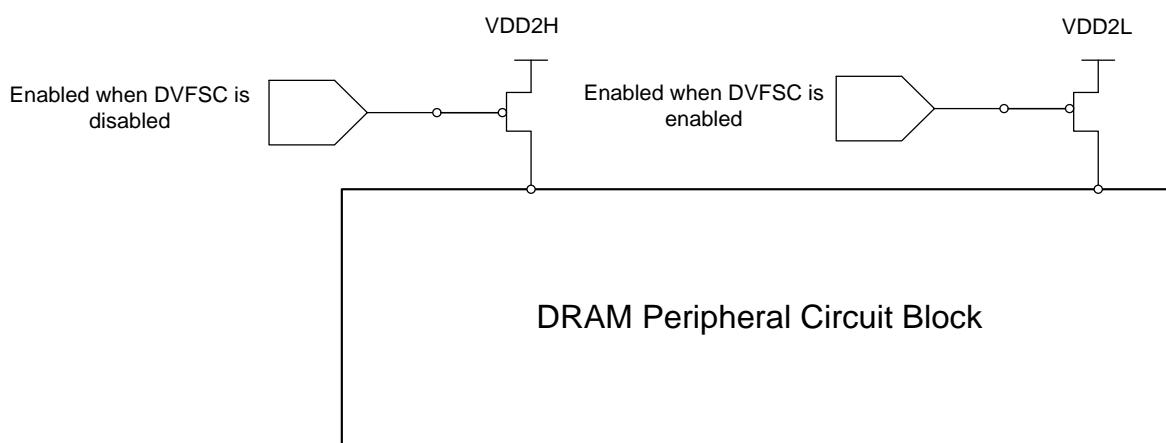


Figure 162 — Example DVFSC Block Diagram

7.7.1.2 DVFSQ Mode

LPDDR5 devices can allow the VDDQ to be ramped during operation including Read/Write transactions. Exact speeds and levels are to be determined by the system builder according to the limits specified in this standard, their own system limitations, and at their own risk. Some guidelines are:

If operation of the LPDRAM will be halted during the VDDQ voltage ramp:

1. The device must be placed in power-down mode or CS held low until the voltage ramp is complete.
2. Re-calibration is recommended before high-speed operation at VDDQ=0.5 V nominal after ramping the VDDQ level.
3. FSP change to appropriate new settings should occur before operation at the new level.

If operation of the LPDRAM during the VDDQ voltage ramp is intended:

1. The LPDRAM should be operated at settings and speeds suitable for the lowest VDDQ level.
2. Operation with ODT disabled is highly recommended, and generally required for VDDQ levels below 0.5 V nominal.
3. The VDDQ voltage ramp should always be equal or slower than the specified limits.
4. Recommended to set VRCG enabled to ensure internal Vref tracking of the changing VDDQ level.
5. Re-calibration is recommended before high-speed operation at VDDQ=0.5 V nominal after ramping the VDDQ level.
6. FSP change to appropriate new settings should occur before higher-speed operation at the new level.

7.7.1.2.1 DVFSQ High-to-Low Transition

An example DVFSQ high-to-low transition sequence is:

1. Operating at high speed with VDDQ=0.5 V nominal.
 2. FSP switch from high frequency to a low frequency suitable for non-ODT operation, enable VRCG.
 3. Wait tFC (stall traffic).
 4. Issue MRW MR16 - set VRCG = 0.
 5. Wait tVRCG_DISABLE (stall traffic).
 6. Issue MRW MR28 - set ZQ Stop=1 to disable background calibration.
 7. Wait tZQSTOP.
 8. Enter DVFSQ (reduce VDDQ below 0.5 V nominal).
 9. Continue operation with reduced VDDQ.

Background ZQ Calibration mode is assumed. Refer to 4.2.1 for details and options related to ZQ requirements.

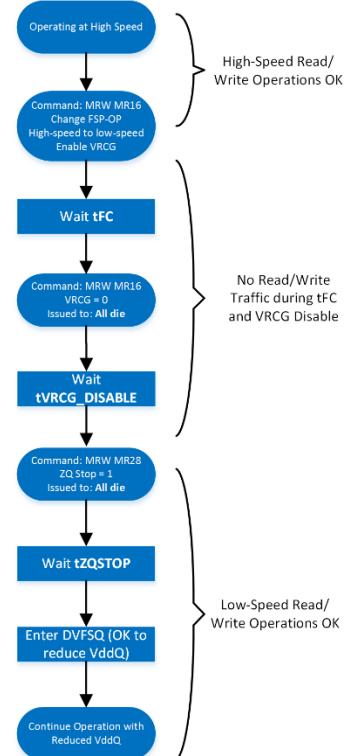


Figure 163 — DVFSQ High (VDDQ) to Low Transition Flow Chart

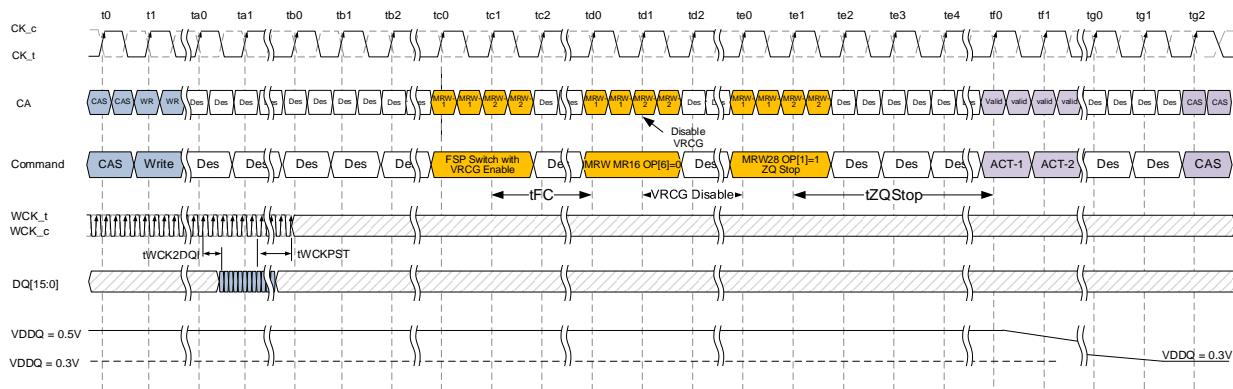


Figure 164 — DVFSQ High (VDDQ) to Low Transition Timing

7.7.1.2.2 DVFSQ Low-to-High Transition without VRCG during VDDQ ramp

An example DVFSQ low-to-high transition sequence is:

1. Operating at low speed with $VDDQ < 0.5$ V nominal.
 2. Ramp $VDDQ$ up to 0.5 V nominal.
 3. Issue MRW MR28 - set ZQ Stop=0 to enable background calibration.
 4. Wait $tZQCALx$.
 5. FSP switch from low frequency to high frequency and VRCG enabled.
 6. Wait tFC (stall traffic).
 7. Issue MRW 16 to disable VRCG.
 8. Wait $tVRCG_DISABLE$ (stall traffic).
 9. Begin high-speed operation with $VDDQ = 0.5$ V nominal.

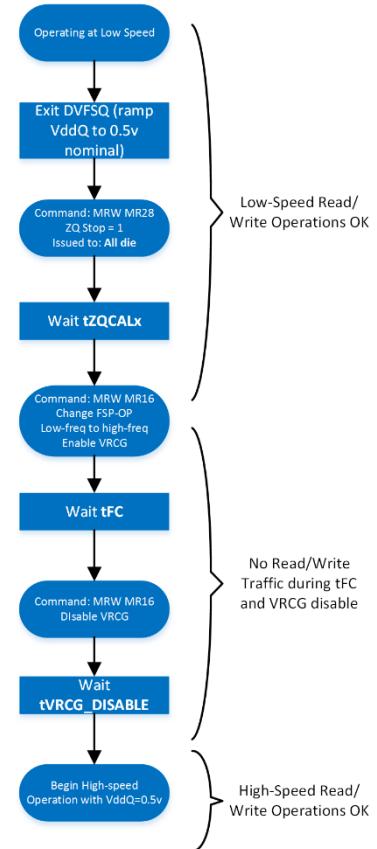


Figure 165 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart without VRCG

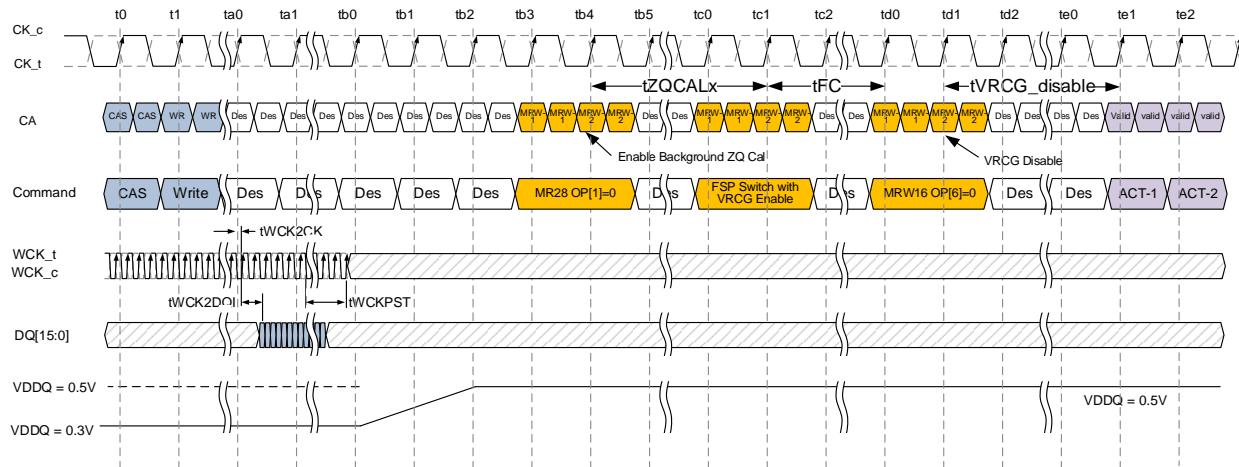


Figure 166 — DVFSQ Low (VDDQ) to High Transition Timing without VRCG during VDDQ ramp

7.7.1.2.3 DVFSQ Low-to-High Transition with VRCG

Enabling VRCG before a VDDQ level transition allows the VREF circuits to accurately track during higher VDDQ slew rates, as shown in Table 227. An example DVFSQ low-to-high transition sequence including use of VRCG mode is:

1. Operating at low speed with VDDQ<0.5 V nominal.
2. Enable VRCG.
3. Wait tVRG_enable (stall traffic).
4. Ramp VddQ up to 0.5v nominal.
5. Issue MRW MR28 - set ZQ Stop=0 to enable background calibration.
6. Wait tZQCALx.
7. FSP switch from low frequency to high frequency.
8. Wait tFC (stall traffic).
9. Disable VRCG.
10. Wait tVRG_disable (continue stall traffic).
11. Begin high-speed operation with VDDQ=0.5 V nominal.

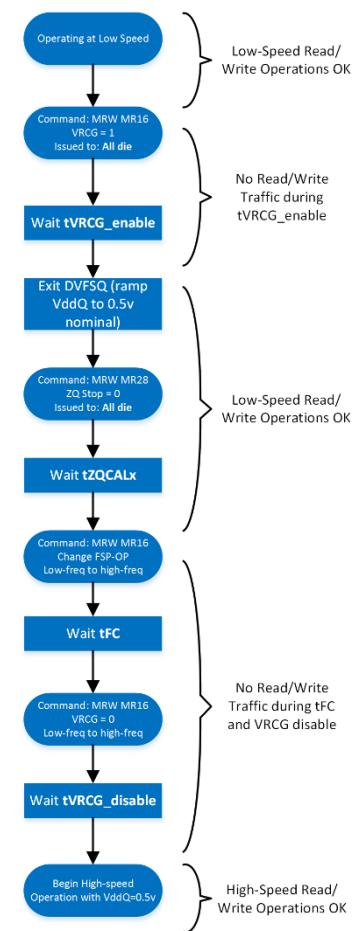


Figure 167 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart with VRCG

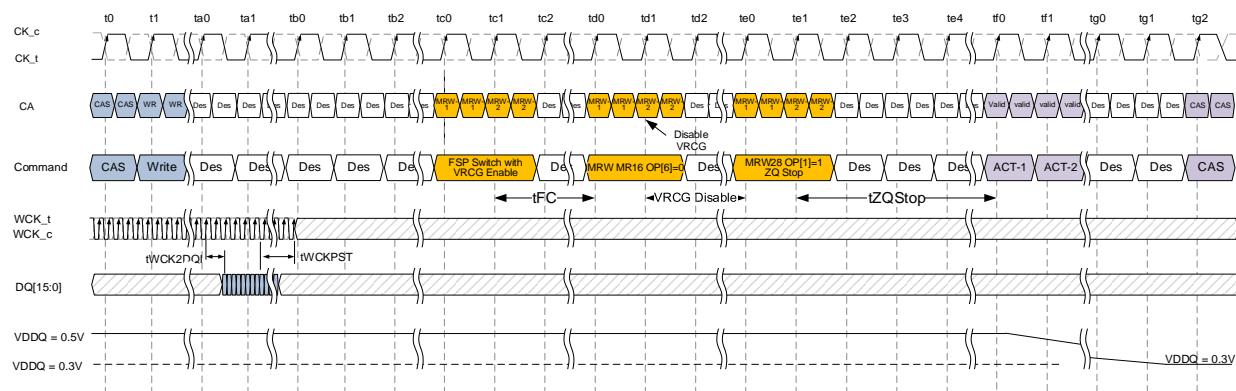


Figure 168 — DVFSQ Low (VDDQ) to High Transition with VRCG

7.7.1.2.3 DVFSQ Low-to-High Transition with VRCG (Cont'd)

Table 227 — VDDQ Ramp Rates

Parameter	Symbol	Max/Min	Value	Units
VDDQ Slew Rate, VRCG Enabled	VDQSR1	Max	20	mV/μs
VDDQ Slew Rate, VRCG Disabled	VDQSR2	Max	4.8	mV/μs

7.7.2 Data Copy Low Power Function

LPDDR5 device can support a data copy low power function to reduce LPDDR5 IO and core power (IDD4W, IDD4R) consumption by utilizing data pattern repeatability per 8Byte data copy granularity. If LPDDR5 device support the data copy function (MR21 OP[0]= 1_B (WDCFS, WRITE Data Copy Function Supported) and/or MR21 OP[1]= 1B (RDCFS, READ Data Copy Function Supported)), users may enable the data copy function by MR21 programming (MR21 OP[4]=1_B (WDCFE, WRITE Data Copy Function Enable) and/or MR21 OP[5]=1_B (RDCFE, READ Data Copy Function Enable)). The LPDDR5 Data Copy Low Power function is added on normal Write, Mask Write and/or Read operations with the same AC timing conditions.

7.7.2.1 Write Data Copy Function

LPDDR5 Write data copy function is applied to each 8 Byte data granularity per DQ byte, if LPDDR5 device supports the WRITE data copy function (MR21 OP[0]= 1_B (WDCFS, WRITE Data Copy Function Supported)) and the WRITE data copy function is enabled by MR21 programming (MR21 OP[4]=1_B (WDCFE, WRITE Data Copy Function Enable)). Whenever any data pattern is repeated over 8Byte data, only the reference data (Reference Data 0-7 in Figure 169) is transferred through one DQ link (DQ0 for a lower DQ byte, DQ8 for an upper DQ byte) per DQ byte from a host to a LPDDR5 device. LPDDR5 device recovers the original 8Byte data by copying the reference data to other 7 DQ data during LPDDR5 device's internal Write operation. Figure 169 illustrates data copy granularity and reference data configuration per X16 channel (BL32).

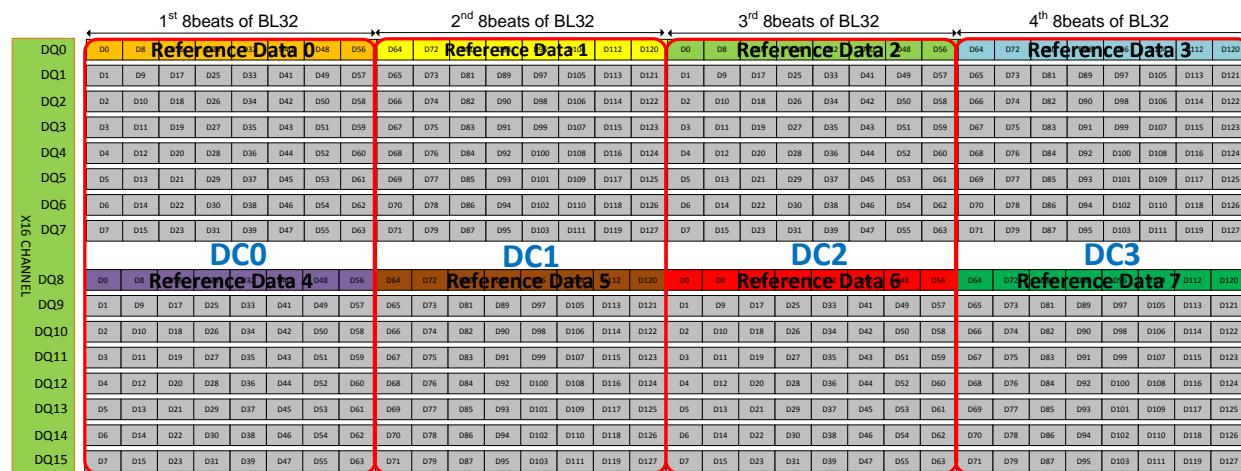


Figure 169 — Data copy granularity and reference data configuration in BL32

Each reference data can be any data pattern (i.e., 256 data patterns) and there is no dependence between reference data. Refer to Table 228 about reference data S[7:0] bit mapping details.

7.7.2.1 Write Data Copy Function (Cont'd)

Table 228 — Reference data S[7:0] bit mapping

DQ Byte	Burst Cycle Number (Beat of Burst)							
	1	2	3	4	5	6	7	8
Reference Data S[7:0] through DQ0	S0	S1	S2	S3	S4	S5	S6	S7
Original 64bit Data								
DQ0	D0	D8	D16	D24	D32	D40	D48	D56
DQ1	D1	D9	D17	D25	D33	D41	D49	D57
DQ2	D2	D10	D18	D26	D34	D42	D50	D58
DQ3	D3	D11	D19	D27	D35	D43	D51	D59
DQ4	D4	D12	D20	D28	D36	D44	D52	D60
DQ5	D5	D13	D21	D29	D37	D45	D53	D61
DQ6	D6	D14	D22	D30	D38	D46	D54	D62
DQ7	D7	D15	D23	D31	D39	D47	D55	D63

NOTE 1 Data Copy hit occurs when the following bitwise condition is met:
 $(D0=D1=D2=D3=D4=D5=D6=D7) \text{ AND } (D8=D9=D10=D11=D12=D13=D14=D15) \text{ AND }$
 $(D16=D17=D18=D19=D20=D21=D22=D23) \text{ AND }$
 $(D24=D25=D26=D27=D28=D29=D30=D31) \text{ AND }$
 $(D32=D33=D34=D35=D36=D37=D38=D39) \text{ AND }$
 $(D40=D41=D42=D43=D44=D45=D46=D47) \text{ AND }$
 $(D48=D49=D50=D51=D52=D53=D54=D55) \text{ AND }$
 $(D56=D57=D58=D59=D60=D61=D62=D63)$

NOTE 2 S0 is copied to D0, D1, D2, D3, D4, D5, D6 and D7

NOTE 3 S1 is copied to D8, D9, D10, D11, D12, D13, D14 and D15

NOTE 4 S2 is copied to D16, D17, D18, D19, D20, D21, D22 and D23

NOTE 5 S3 is copied to D24, D25, D26, D27, D28, D29, D30 and D31

NOTE 6 S4 is copied to D32, D33, D34, D35, D36, D37, D38 and D39

NOTE 7 S5 is copied to D40, D41, D42, D43, D44, D45, D46 and D47

NOTE 8 S6 is copied to D48, D49, D50, D51, D52, D53, D54 and D55

NOTE 9 S7 is copied to D56, D57, D58, D59, D60, D61, D62 and D63

CAS command delivers Write data copy hit or miss information to LPDDR5 devices with 4bit operands (DC0 – DC3, refer to LPDDR5 Command Truth Table, **Table 154**.

Table 229 — Write data copy hit or miss operands (DC0 – DC3) of CAS command

Write Data Copy Operand of CAS Command	Description	Notes
DC0	0B: Write data copy miss (normal Write) 1B: Write data copy hit (reference byte through DQ0 and DQ8)	1
DC1	0B: Write data copy miss (normal Write) 1B: Write data copy hit (reference byte through DQ0 and DQ8)	2
DC2	0B: Write data copy miss (normal Write) 1B: Write data copy hit (reference byte through DQ0 and DQ8)	3,5
DC3	0B: Write data copy miss (normal Write) 1B: Write data copy hit (reference byte through DQ0 and DQ8)	4,5

NOTE 1 DC0 is applied to the first 8 beats of BL16 or BL32.

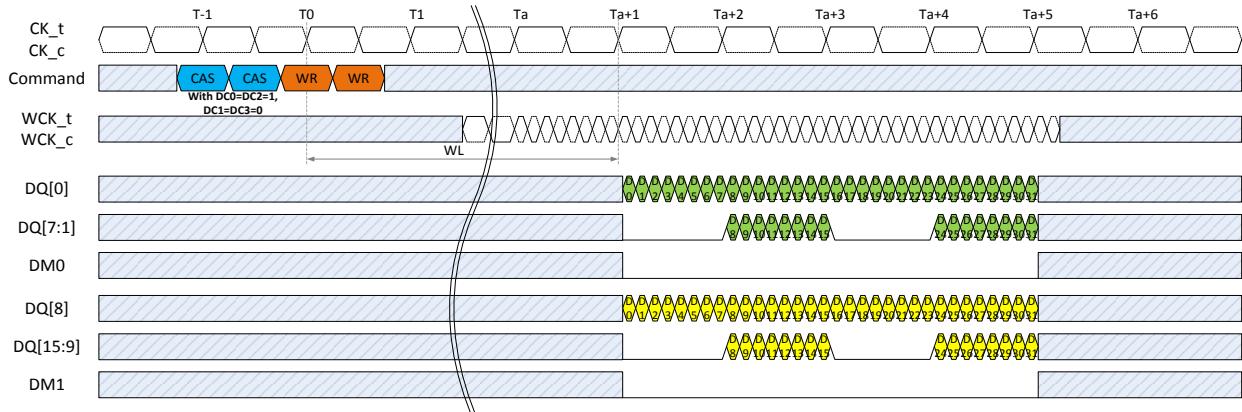
NOTE 2 DC1 is applied to the second 8 beats of BL16 or BL32.

NOTE 3 DC2 is applied to the third 8 beats of BL32.

NOTE 4 DC3 is applied to the fourth 8 beats of BL32.

NOTE 5 DC2 and DC3 are "don't care" in case of BL16.

7.7.2.1 Write Data Copy Function (Cont'd)



NOTE 1 WCK:CK = 4:1, BL32, ODT on

NOTE 2 CAS command with $DC0=DC2=1_B$, $DC1=DC3=0_B$

Figure 170 — Example of Write Data Copy Function Timing Diagram

7.7.2.2 Read Data Copy Function

LPDDR5 Read data copy function is applied to each 8 Byte data granularity per DQ byte, if LPDDR5 device supports the READ data copy function (MR21 OP[1]= 1B (RDCFS, READ Data Copy Function Supported)) and the READ data copy function is enabled by MR21 programming (MR21 OP[5]=1B (RDCFE, READ Data Copy Function Enable)). LPDDR5 device may include an internal data comparator logic to determine any data pattern repeatability per 8Byte read data during Read operations. If any data pattern repeatability over 8Byte read data is found, LPDDR5 device returns a reference data S[7:0] through one DQ link (DQ0 for a lower DQ byte, DQ8 for an upper DQ byte) per DQ byte and a Read data copy hit or miss flag bit through a DM pin (DM0 for a lower DQ byte, DM1 for an upper DQ byte) to a host system. Read reference data S[7:0] bit mapping is same as Write data copy operation. (Refer to Table 230). LPDDR5 device shall drive other DQs (DQ[7:1] in a lower DQ byte, DQ[15:9] in an upper DQ byte) in 8 Byte data granularity to LOW in case of the Read data copy hit.

Table 230 — Read data copy function

DM Burst Data	Description	Notes
1 st beat of DM burst data (DM-0)	0B: Read data copy miss (normal Read) 1B: Read data copy hit (reference byte through DQ0 (or DQ8))	1
9 th beat of DM burst data (DM-8)	0B: Read data copy miss (normal Read) 1B: Read data copy hit (reference byte through DQ0 (or DQ8))	2
17 th beat of DM burst data (DM-16)	0B: Read data copy miss (normal Read) 1B: Read data copy hit (reference byte through DQ0 (or DQ8))	3
25 th beat of DM burst data (DM-24)	0B: Read data copy miss (normal Read) 1B: Read data copy hit (reference byte through DQ0 (or DQ8))	4

NOTE 1 DM-0 is a read data copy hit or miss flag bit applied to the first 8 beats of BL16 or BL32.

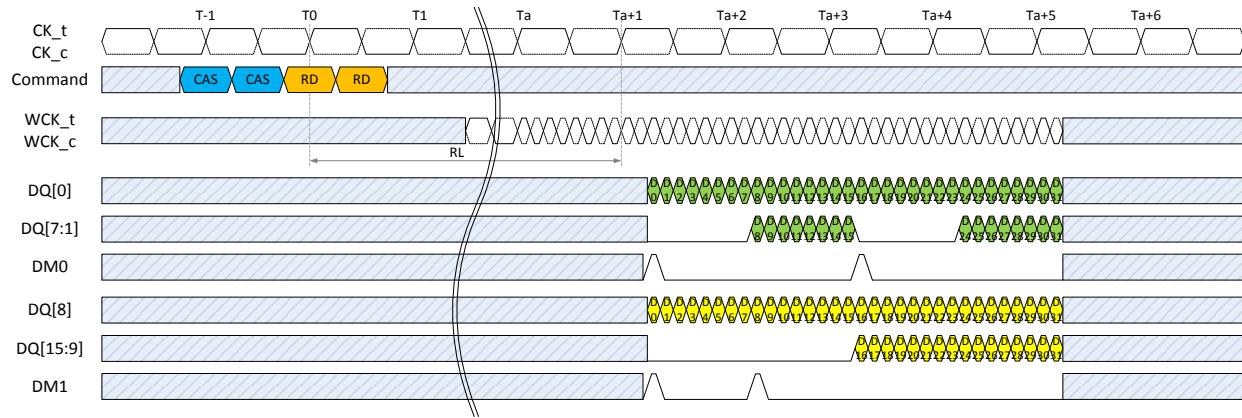
NOTE 2 DM-8 is a read data copy hit or miss flag bit applied to the second 8 beats of BL16 or BL32.

NOTE 3 DM-16 is a read data copy hit or miss flag bit applied to the third 8 beats of BL32 only.

NOTE 4 DM-24 is a read data copy hit or miss flag bit applied to the fourth 8 beats of BL32 only.

7.7.2.2 Read Data Copy Function (Cont'd)

Figure 171 shows an example of Read Data Copy function timing diagram in case of mixed read data copy hit and miss.



NOTE 1 WCK:CK = 4:1, BL32, ODT on

NOTE 2 DM0 for a lower byte: DM0-0= 1_B, DM0-8= 0_B, DM0-16= 1_B, DM0-24= 0_B

NOTE 3 DM1 for an upper byte: DM1-0= 1_B, DM1-8= 1_B, DM1-16= 0_B, DM1-24= 0_B

Figure 171 — Example of Read Data Copy Function Timing Diagram

7.7.2.3 Read Data Copy Function with Read DBI Enable

LPDDR5 device supports a Data Bus Inversion function in Read operations. The Read data copy hit/miss flag bits can share a DM pin signal with Read DBI bits in case of both functions enabled. If LPDDR5 device supports the READ data copy function (MR21 OP[1]= 1_B (RDCFS, READ Data Copy Function Supported)) and the READ data copy function is enabled by MR21 programming (MR21 OP[5]=1_B (RDCFE, READ Data Copy Function Enable)) and the Read DBI function is enabled by MR3 programming (MR3 OP[6]=1_B, DBI-RD, Read-DBI_DC Enable), LPDDR5 device drives other DQs (DQ[7:1] in a lower DQ byte, DQ[15:9] in an upper DQ byte) to specific data pattern at 1st and 9th beat of data burst (BL16) or at 1st, 9th, 17th and 25th beat of data burst data (BL32). When the number of “1” data bits within other DQs at 1st and 9th beat of data burst (BL16) or at 1st, 9th, 17th and 25th beat of data burst data (BL32), is greater than four, the corresponding DM bit is the Read data copy flag bit. Otherwise, the corresponding DM bit is the Read DBI bit.

7.7.3 Write X operation

An LPDDR5 memory system may reduce power in write operation of repeated data pattern utilizing Write X function. Write X function is an optional feature in LPDDR5 device, and the LPDDR5 controller is able to detect its supportability by mode register read of MR21 OP[2]. If the MRR result of MR21 OP[2]=1, the controller can enable Write X function by setting MR21 OP[6] = 1 by MRW command. A write X command consists of a CAS command and following write command with column address. The CAS command with DC0=0, DC1=0, DC2=0, DC3=0 and WRX=H with following write command initiates write X command with zero data write at corresponding column address.

7.7.3 Write X operation (Cont'd)

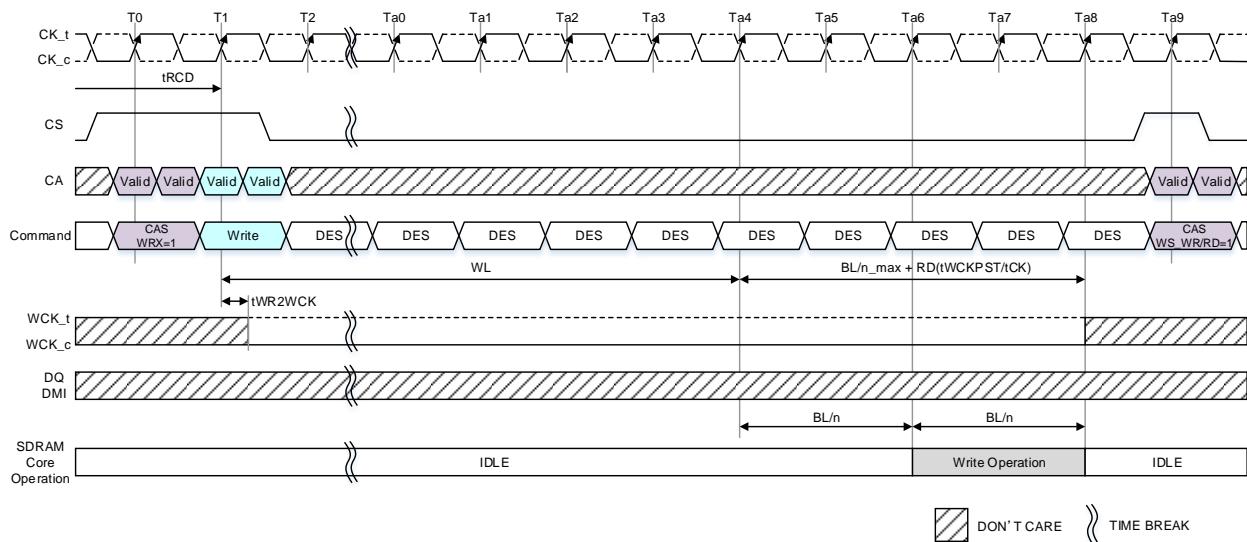
Table 231 — CAS command with write X (zero) enable bits.

Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CK
CAS	H	L	L	H	H	V	V	V	R1
	X	DC0=0	DC1=0	DC2=0	DC3=0	WRX	V	V	F1

The write X enable bits in Table 231 are non-sticky bits. After CAS command with write X enabled is issued, followed write commands perform write X operation.

The Write X function can be operated to an activated bank without WCK2CK sync and data input to SDRAM's DQ pins. In this case the input of WCK_t/c is required to be valid and compliment level after tWR2WCK from Write command. For example, WCK_t to High and WCK_c to low and vice versa. Additionally, the toggling input to WCK_t/c is possible too, and the toggling input does not transfer to SDRAM internal WCK clock tree at non WCK2CK sync state, hence the power consumption is smaller than Write operation during WCK2CK sync state.

Figure 172 shows write X operation without WCK clock. Although write X operation does not require WCK or DQ operation, DRAM internal write operation occurs at same timing as normal write operation. Therefore, all core timing parameters of write command in 7.4.7.1 also apply to the write X command.



NOTE 1 CAS Sync command is inhibited until Ta8.

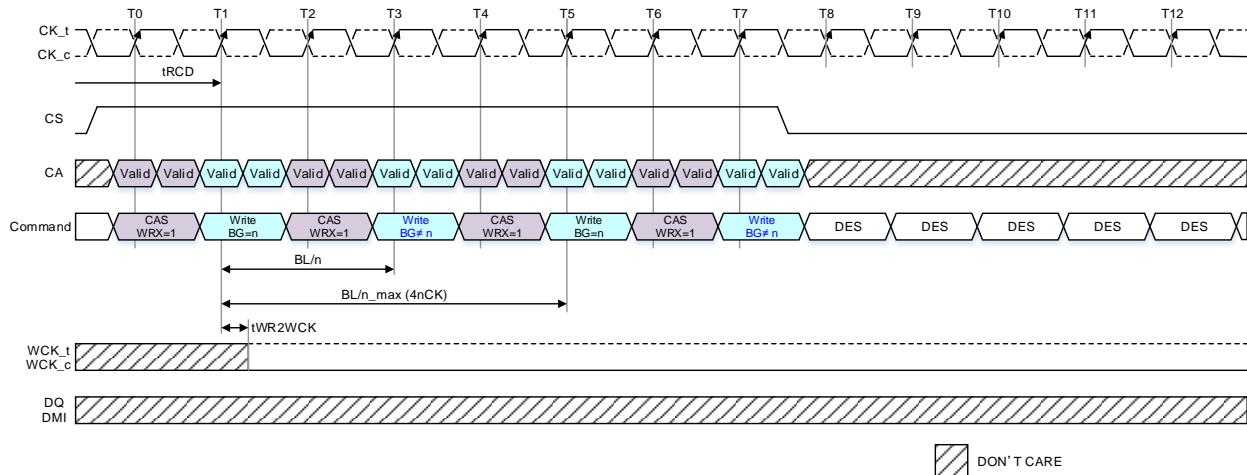
NOTE 2 CAS Sync command can be issued after Ta9 (Ta9 is included).

NOTE 3 tWCKPST=2.5nWCK, RD(tWCKPST/tCK)=0.

NOTE 4. The CAS Sync command input timing is applied the same timing as Write command w/o Write X, see 7.2.2, WCK2CK SYNC Off Timing Definition.

Figure 172 — Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16

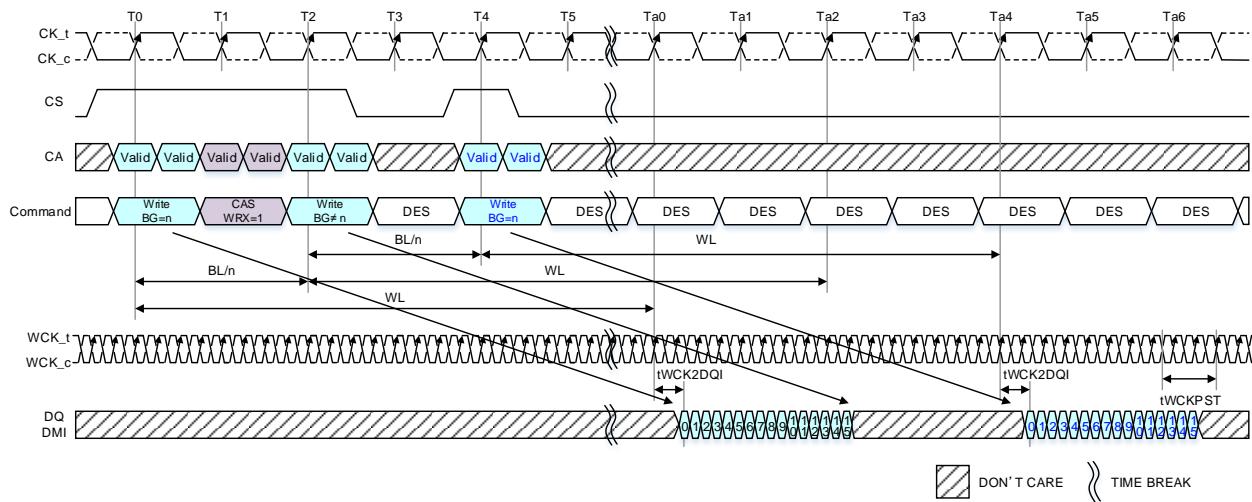
7.7.3 Write X operation (Cont'd)



NOTE 1 Write w/ write X timing follows Write w/o Write X timing.

Figure 173 — Consecutive Write and Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16

Write X operation also can be performed during WCK2CK sync process. An LPDDR5 SDRAM controller is allowed issue Write X command in WCK2CK sync'd state. However, DRAM is not able to turn off WCK buffer in this case, reducing the power saving amount of write X. Like normal write command, write X command extends WCK2CK sync state, as shown in Figure 174.



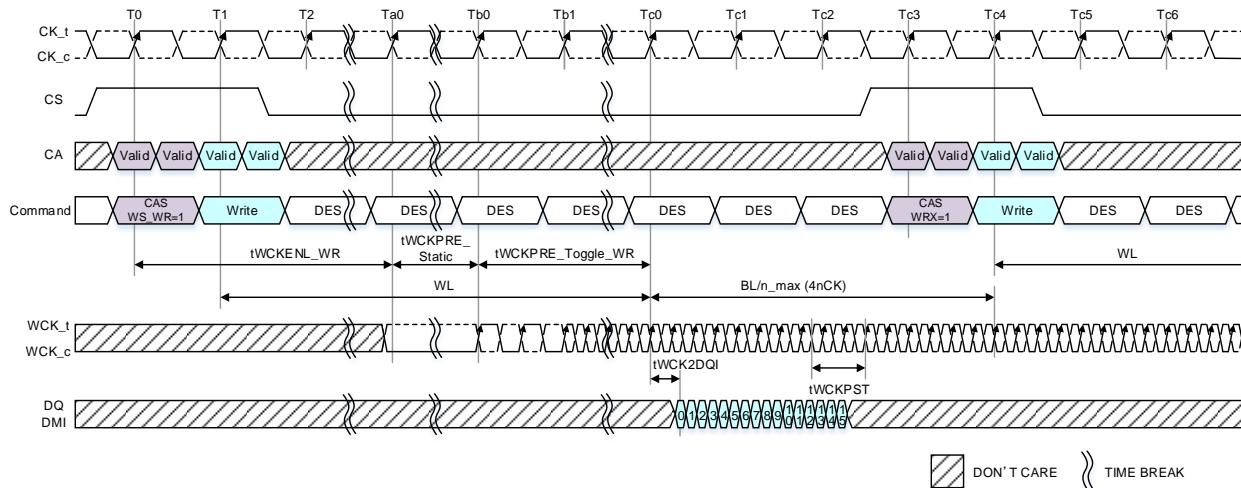
NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 Write w/ Write X timing follows Write w/o Write X timing.

Figure 174 — Consecutive Write and Write X timing at Sync: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16

7.7.3 Write X operation (Cont'd)

The WCK2CK SYNC Off Timing Definition applied Write X command. Figure 175 shows a case where WCK2CK synchronization is continued by the Write X command, and Figure 176 show a case where it does not continue.



NOTE 1 tWCK2CK is 0ps in this instance.

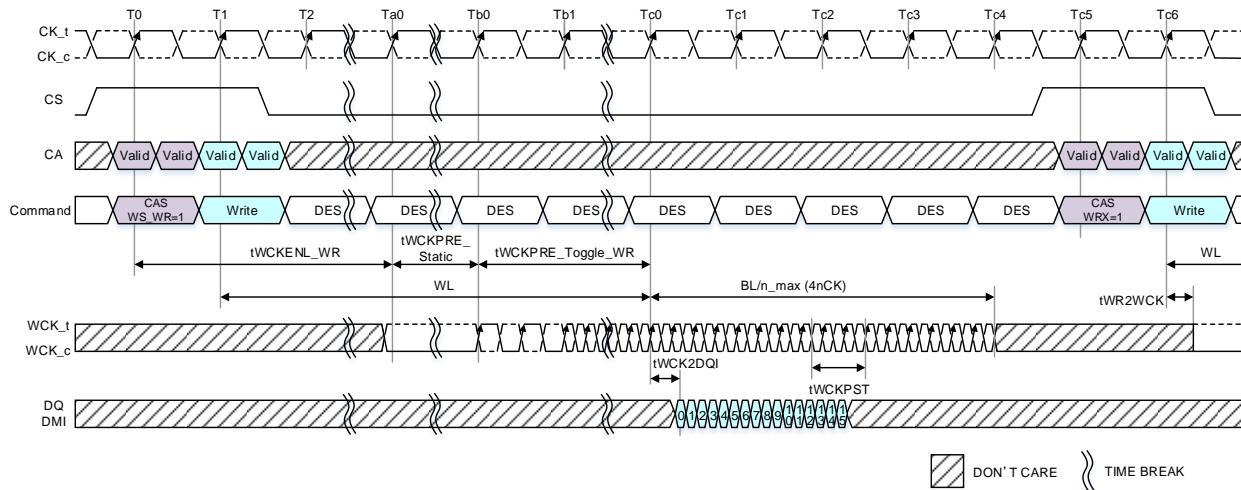
NOTE 2 The end of both WL and tWCKPRE_Toggle_WR are the same timing in this instance.

NOTE 3 Write w/ write X command can be issued until Tc4.

NOTE 4 tWCKPST=2.5nWCK, RD(tWCKPST/tCK)=0.

Figure 175 — Write w/ write X issuing timing at Sync state.

The issuing CAS_WRX command timing is respected the constraint of CAS Sync command after WCK2CK sync is expired in order to the command scheduling becomes easy. For example, issuing CAS_WRX command is inhibited on Tc4 in Figure 176.



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both WL and tWCKPRE_Toggle_WR are the same timing in this instance.

NOTE 3 WCK2CK sync is expired on Tc4.

NOTE 4 CAS_WRX command is inhibited on Tc4.

NOTE 5 CAS WRX command can be issued after Tc5 (Tc5 is included).

NOTE 6 tWCKPST=2.5nWCK, RD(tWCKPST/tCK)=0.

Figure 176 — CAS_WRX Command timing after WCK2CK sync state is expired

7.7.3 Write X operation (Cont'd)

Table 232 — AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Notes
Valid WCK Requirement after Write w/ Write X	tWR2WCK	Min	1.25	ns	-

7.7.4 Post Package Repair (PPR)

The repair process is irrevocable so great care should be exercised when using. At Post Package Repair, the fail row address to fix is required to designate using 8B mode addressing. With PPR, LPDDR5 SDRAM can correct 1 Row per bank. When PPR is executed in the BG or 16B mode, refer to the address mapping in Bank Architecture section. The controller should prevent unintended PPR mode entry and repair.

The availability of PPR for each bank [7:0] is readable via MR29 OP[7:0] respectively.

Table 233 — MR29 OP[7:0] Register Information

Function	Register Type	Operand	Data	Notes
PPR Resource Bank 0	Read-only	MR29 OP[0]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 1		MR29 OP[1]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 2		MR29 OP[2]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 3		MR29 OP[3]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 4		MR29 OP[4]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 5		MR29 OP[5]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 6		MR29 OP[6]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	
PPR Resource Bank 7		MR29 OP[7]	0 _B : PPR Resource is not available 1 _B : PPR Resource is available	

The "bank address" is specified by CA[0:2] during the Activate command and is valid for a single PPR sequence. Valid combination for 8B mode includes CA[0:2]=000_B, 001_B, 010_B, 011_B, 100_B, 101_B, 110_B and 111_B. And CA[3] is required to be V (valid).

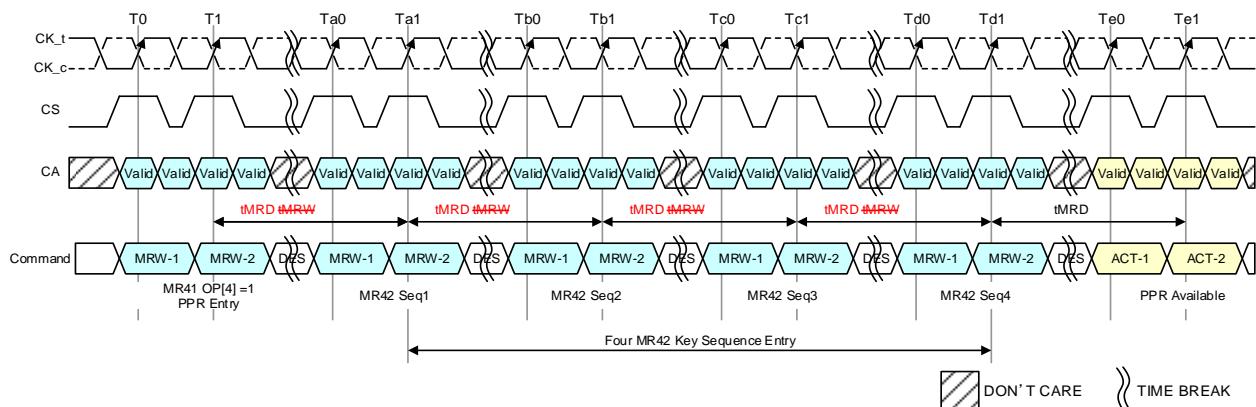
The BG/Bank address mapping on PPR is shown in Table 234.

Table 234 — Combination of PPR Resource for CA Input

CA Input at ACT command				8B Mode	BG Mode		16B Mode
CA0	CA1	CA2	CA3	Bank	BG	Bank	Bank
0	0	0	V	0	0,2	0	0,8
1	0	0	V	1	0,2	1	1,9
0	1	0	V	2	0,2	2	2,10
1	1	0	V	3	0,2	3	3,11
0	0	1	V	4	1,3	0	4,12
1	0	1	V	5	1,3	1	5,13
0	1	1	V	6	1,3	2	6,14
1	1	1	V	7	1,3	3	7,15

7.7.4.1 Guard Key Protection

Entry into PPR is protected through a sequential MRS guard key to prevent unintentional PPR programming. The PPR guard key requires a sequence of four MRW commands to be issued immediately after entering PPR, as shown in **Figure 177**. The guard key sequence is entered in the specified order as stated below, and shown in Table 235. Any interruptions of the guard key sequence by other MRW/MRR commands or non-MR commands such as ACT, WR, RD, REFab and REFpb are not allowed. Since interruption of the guard key entry is not allowed, if the guard key is not entered in the required order or is interrupted by other commands, PPR mode will not execute and the setting value of MR41 OP[4] will return to 0 automatically. The offending command which terminated PPR entry may or may not execute correctly. However, the offending command will not cause the SDRAM to lock up. Additionally, when PPR entry sequence is interrupted all subsequent commands such as ACT command will be conducted as normal SDRAM commands. If a PPR operation was prematurely terminated, MR41 OP[4] is required to be set to "1" prior to performing another PPR operation. The SDRAM does not provide an error indication if an incorrect PPR guard key sequence is entered.



NOTE 1 Only DES commands are allowed during tMRD If another command is entered in this period, PPR mode will not execute and the setting value of MR41 OP[4] will return to 0 automatically.

Figure 177 — Guard Key Timing Diagram

Table 235 — Guard Key Encoding for MR42

Command	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR42 Seq1	1	1	0	0	1	1	1	1
MR42 Seq2	0	1	1	1	0	0	1	1
MR42 Seq3	1	0	1	1	1	0	1	1
MR42 Seq4	0	0	1	1	1	0	1	1

7.7.4.2 PPR Fail Row Address Repair

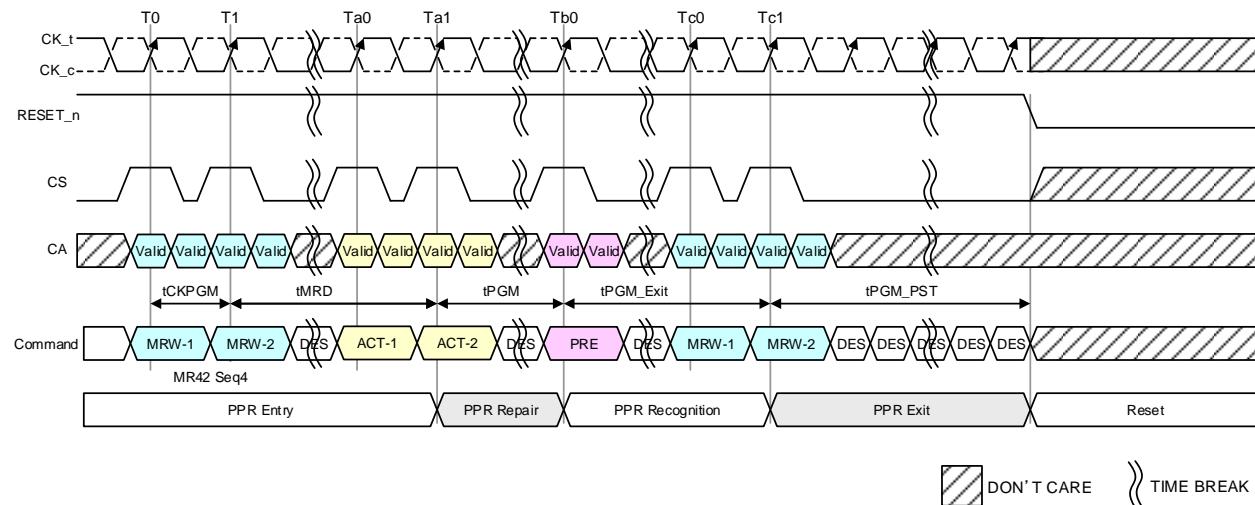
Once PPR mode is entered by setting MR41 OP[4]=1 (enable) and issuing the guard key sequence, the ACT command is used to transmit the bank and row address of the row to be repaired in SDRAM. The specific steps of PPR are as follows.

The following is procedure of PPR.

1. Before entering PPR mode, All banks are required to be Precharged and idle state.
2. Enable PPR using MR41 OP[4]=1 and wait tMRD.
3. Issue the guard key as four consecutive MR42 OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command should be spaced by tMRD.
4. Issue an ACT command with the Bank Group, Bank and Row fail address.
5. Wait tPGM to allow the SDRAM to repair target Row Address internally then issue PRE.
6. Wait tPGM_Exit after PRE which allows the SDRAM to recognize repaired Row address RAn.
7. Exit PPR by setting MR41 OP[4]=0 and wait tPGMPST.
8. Assert Reset_n, and then to do the reset and initialization procedure.
9. In more than one fail address repair case, Repeat Steps 2 to 8

After entering PPR mode, do not deviate from the above-mentioned procedure. It is prohibited to insert any other command except DES and NOP between step 3 and step 8. The PPR procedure is required to be performed at a clock frequency of 800MHz or less; the frequency for PPR mode is defined as tCKPGM.

Once PPR mode is exited, the controller can verify that the target row was repaired by writing data into the target row and reading it back after reset and initialization procedure.



- NOTE 1 With one PPR command, only one row can be repaired at one time per die.
 NOTE 2 RESET is required at the end of every PPR procedure.
 NOTE 3 During PPR, memory contents are not refreshed and may be lost.
 NOTE 4 Assert Reset_n: Refer to 4.1, Reset, Power-up, Initialization and Power-off Procedure, for details.

Figure 178 — PPR Timing

7.7.4.2 PPR Fail Row Address Repair (Cont'd)

Table 236 — PPR Timing Parameters

Parameter	Symbol	min	max	Unit	Notes
PPR Programming Clock	tCKPGM	1.25	200	ns	
PPR Programming Time	tPGM	2000	-	ms	
PPR Exit Time	tPGM Exit	15	-	ns	
New Address Setting time	tPGMPST	500	-	μs	

7.7.5 Target Row Refresh

LPDDR5 SDRAM has a requirement that a given row can be accessed a limited number of times within a refresh period ($tREFW * 2$) without adjacent rows being refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. For TRR mode, all bank information and control are based on 8B Mode regardless of which Bank Architecture is selected via MR. The row receiving excessive activity is the Target Row (TRn), the adjacent rows to be refreshed are the victim rows. When the MAC limit is reached for TRn, either the LPDDR5 SDRAM must receive $(R * 2)$ Refresh Commands before another row activate is issued, or the LPDDR5 SDRAM should be placed into Targeted Row Refresh (TRR) mode. TRR Mode will re-refresh the rows adjacent to the TRn that encountered tMAC limit.

If LPDDR5 SDRAM supports Unlimited MAC value: MR27 OP[2:0]=000 and MR27 OP[3]=1, Target Row Refresh operation is not required. In this case the LPDDR5 SDRAM may allow setting MR27 OP[7]=1: TRR mode enable, but LPDDR5 SDRAM's behavior is vendor specific. For example, a certain LPDDR5 SDRAM may ignore MRW command for entering/exiting TRR mode or a certain SDRAM may support commands related TRR mode. See vendor device datasheets for details about TRR mode definition at supporting Unlimited MAC value case.

There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the activates from the two target rows on a victim row in a bank should not exceed MAC value.

MR27 fields required to support the new TRR settings. Setting MR27 OP[7]=1 enables TRR Mode and setting MR27 OP[7]=0 disables TRR Mode. MR27 OP[6:4] defines which bank (BAn) the target row is located in (See Table 98, MR27, for details).

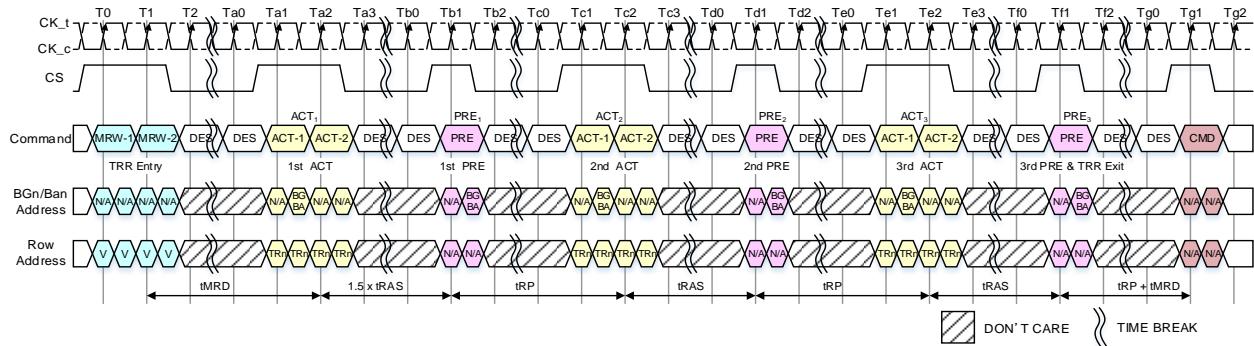
The TRR mode and other LPDDR5 SDRAM calibration modes must be disabled during initialization. The TRR mode is entered from a DRAM Idle State. Once TRR mode has been entered, no other Mode Register commands except MR27 OP[7]=0 (setting MR27 OP[7]=0 interrupt and reissue the TRR mode) are allowed until TRR mode is completed.

When enabled; TRR Mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BAn precharge has completed plus tMRD. Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR27 OP[7]=0; if the TRR is exited via another MRS command, the value written to MR27 OP[6:4] are don't cares.

7.7.5.1 TRR Mode Operation

- 1) Figure 179 depicts TRR mode. The following steps must be performed when TRR mode is enabled. Three activate and precharge command sequences are issued to complete TRR operation. (Shown as ACT1 / PRE1, ACT2 / PRE2 and ACT3 / PRE3 in the drawing). A Precharge All (PREA) commands issued while LPDDR5 SDRAM is in TRR mode will also perform precharge to BAn and counts towards a PREn command.
- 2) Prior to issuing the MRW command to enter TRR mode, the SDRAM should be in the idle state. A MRW command must be issued with MR27 OP[7]=1 and MR27 OP[6:4] defining the bank in which the targeted row is located. All other MR27 bits should remain unchanged.
- 3) No activity is to occur in the DRAM until tMRD has been satisfied. Once tMRD has been satisfied, the only commands to BAn allowed are ACT and PRE until the TRR mode has been completed.
- 4) The first ACT to the BAn with the TRn address can now be applied, no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until $[(1.5 * tRAS) + tRP]$ is satisfied.
- 5) After the first ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued $(1.5 * tRAS)$ later; and then followed tRP later by the second ACT to the BAn with the TRn address. Once the 2nd activate to the BAn is issued, nonBAn banks are allowed to have activity.
- 6) After the second ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued tRAS later and then followed tRP later by the third ACT to the BAn with the TRn address.
- 7) After the third ACT to the BAn with the TRn address is issued, a PRE to BAn would be issued tRAS later; and once the third PRE has been issued, nonBAn banks are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP + tMRD is satisfied.
- 8) TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any-time the TRR mode is interrupted and not completed, the interrupted TRR Mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, an MR27 change is required with setting MR27 OP[7]=0, MR27 OP[6:4] are don't care, followed by three PRE to BAn, tRP time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.
- 9) Refresh command to the LPDDR5 SDRAM or entering Self Refresh mode is not allowed while the DRAM is in TRR mode.

7.7.5.1 TRR Mode Operation (Cont'd)



NOTE 1 TRn is targeted row.

NOTE 2 Bank BAn represents the bank in which the targeted row is located.

NOTE 3 TRR mode self-clears after tMRD + tRP measured from 3rd BAn precharge PRE3 at clock edge Tf1.

NOTE 4 TRR mode or any other activity can be re-engaged after tRP + tMRD from 3rd BAn precharge PRE3. PRE_ALL also counts if issued instead of PREn. TRR mode is cleared by DRAM after PRE3 to the BAn bank.

NOTE 5 Activate commands to BAn during TRR mode do not provide refreshing support, i.e., the Refresh counter is unaffected.

NOTE 6 The DRAM must restore the degraded row(s) caused by excessive activation of the targeted row (TRn) necessary to meet refresh requirements.

NOTE 7 A new TRR mode must wait tMRD+tRP time after the third precharge.

NOTE 8 BAn may not be used with any other command.

NOTE 9 ACT and PRE are the only allowed commands to BAn during TRR Mode.

NOTE 10 Refresh commands are not allowed during TRR mode.

NOTE 11 All DRAM timings are to be met by DRAM during TRR mode such as tFAW. Issuing of ACT1, ACT2 and ACT3 counts towards tFAW budget.

Figure 179 — Target Row Refresh Mode

7.7.6 Decision Feedback Equalization (DFE)

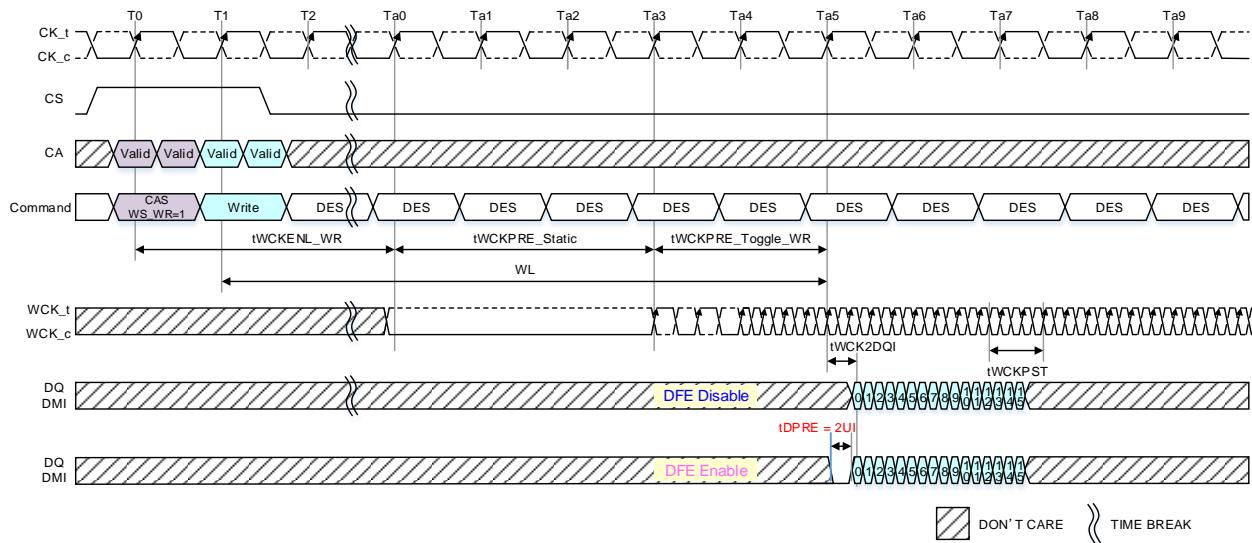
LPDDR5 support very high data rate. To compensate channel characteristics, equalization technique helps Rx margin. DFE can be enabled when WCK is higher than 800MHz.

LPDDR5 provide Decision Feedback Equalization (DFE) capability for DQ Rx. LPDDR5 DFE is enabled by MR24 OP[2:0] for lower byte and MR24 OP[6:4] for upper byte. LPDDR5 supports only 1 tap negative feedback. DFE quantity can be controlled by MR24 OP[2:0] for lower byte and MR24 OP[6:4] for upper byte with seven steps. LPDDR5 can support different feedback quantity for each byte.

DFE is optional feature.

Before write data burst operation, LPDDR5 with DFE enabled requires 2UI DQ pre-drive to 0. This pre-drive set precondition of DFE circuits. In case of back to back write, there is no need to add pre-drive.

7.7.6 Decision Feedback Equalization (DFE) (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both WL and tWCKPRE_Toggle_WR are the same timing in this instance

NOTE 3 Data Rate: 3733Mbps, tWCKPRE _Static: 3nCK, tWCKPRE toggle_WR: 2nCK

Figure 180 — DFE pre-drive requirement

7.7.7 Link ECC

Supporting Link ECC is an optional feature. In addition, DRAMs which support Link ECC need not do so at WCK frequencies less than or equal to 1600MHz. If supported by the DRAM, Link ECC may then be enabled or disabled by the controller as required by the system configuration, operating speed, or other requirements.

During each Write burst when Link ECC is enabled, ECC will be generated and checked across the 128 Data bits within a specified portion of the burst. ECC will be separately generated and checked across the 16 DMI bits within the same specified portion of the burst. In the case of the data ECC, the DBI encoded data must be used, as Masked Writes can modify the data in a way which changes the ECC.

This ECC (6 bits on DMI + 9 bits on the data) would be received by the DRAM on the RDQS_t pin along with Write Data on the DQ pins and DBI/DM on the DMI pin as illustrated in Figure 181.

7.7.7 Link ECC (Cont'd)

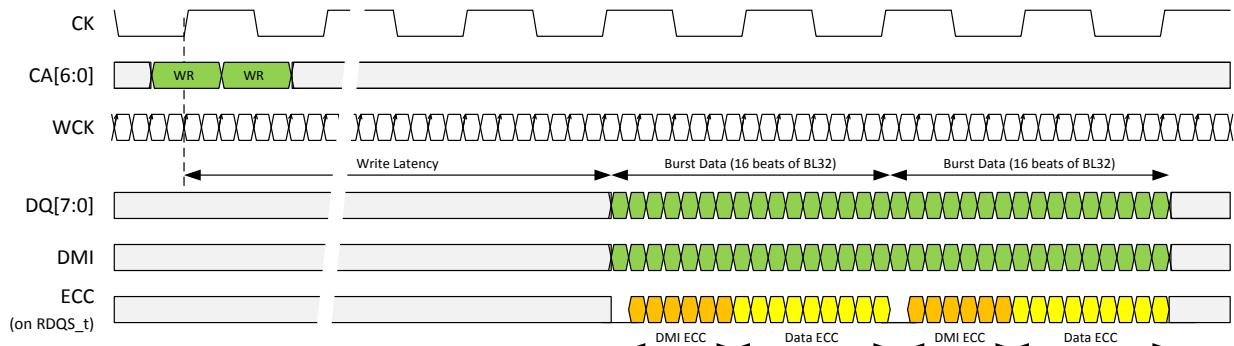


Figure 181 — Write command showing link ECC transfer

During each Read burst when Link ECC is enabled, ECC will be generated across the 128 Data bits in a specified portion of the burst. Since Link ECC and Read DBI are mutually exclusive, there is no need to calculate ECC across the DBI bits in the Read case.

This ECC (9 bits on the data only) would be transmitted from the DRAM on the DMI pin along with Read Data on the DQ pins as illustrated in the Read Command diagram below. Link ECC and the Read Data Copy function are mutually exclusive, since both drive information on DMI, and would conflict if both functions were enabled simultaneously.

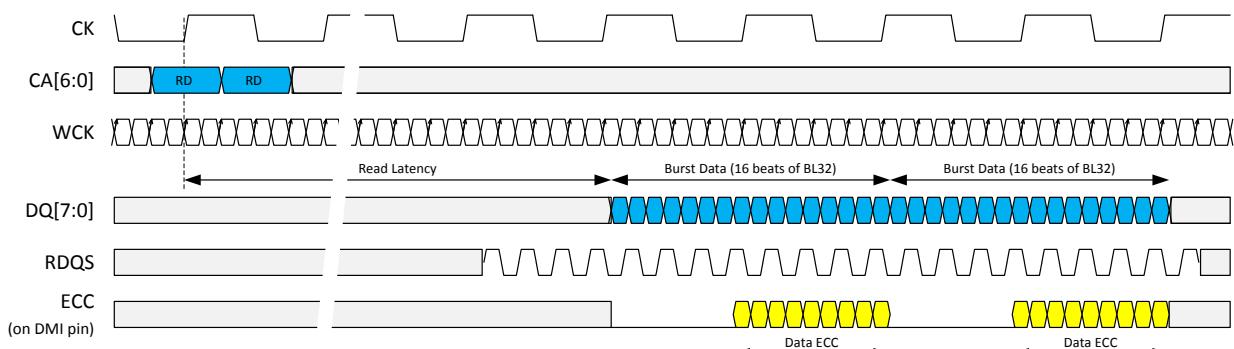


Figure 182 — Read command showing Link ECC transfer

A BL16 burst consists of 16 consecutive data beats; a BL32 burst consists of 32 consecutive beats. The ECC is calculated on 16-beat quantities of Data or DMI, so a BL32 burst has 2 separate sets of ECCs per burst per byte, one on the first 16 beats and another on the next 16 beats. A BL16 burst has only 1 set per burst per byte. A set of ECCs refers to all 15 ECC bits on a Write or the 9 ECC bits on a Read.

Link ECC is also calculated on each byte of the interface independently. So BL16 on a full 16-bit DRAM channel includes 2 sets of ECCs, and BL32 on a full DRAM channel includes a total of 4 sets.

7.7.7 Link ECC (Cont'd)

The ECC check matrix for the LPDDR5 Data ECC is defined below.

Table 237 — ECC Check Matrix for Data

Beat	0							1							2							3							4							5						
DQ Pin	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7		
S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1		
S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1			
S2	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1				
S3	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1					
S4	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0				
S5	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1					
S6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1	1					
S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1	1					
S8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
Beat	6							7							8							9							10							11						
DQ Pin	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7		
S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1		
S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	1			
S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1				
S3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1				
S4	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
S5	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0			
S6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
S8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
Beat	12							13							14							15							Check Bit													
DQ Pin	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	C0	C1	C2	C3	C4	C5	C6	C7	C8									
S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0			
S3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0			
S4	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0			
S5	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
S6	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0			
S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0			
S8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			

Although shown in 3 sections, this should be considered a single matrix of 9 rows by 137 columns. Each column represents one of the data bits or check bits, which are inputs to the ECC logic. Columns are labeled at the top with a beat number and a DQ bit number (or a check bit number). Each row is labelled at the left with an ECC output bit name (S0-S8).

Each data bit's location within the burst is defined within the table itself (by beat number and DQ bit number). On the upper byte of a 16-bit channel, the DQ bit numbers would be those shown above plus 8. In the 2nd half of a BL32 burst, the beat numbers would be those shown plus 16. All of the check bits appear on the pin which is currently set to Parity. This would be RDQS_t on a Write and DMI on a Read. C0-C8 appear on beats 7-15 of the burst in numerical order (23-31 in the 2nd half of a BL32 burst). That is, C0 is on beat 7, C1 on beat 8 and so on with C8 on beat 15.

During a Write Data Copy command (Write or Masked Write with MR21 OP[4]=1B, and DC[3:0] non-zero in the prior CAS command), only DQ[0] & DQ[8] are driven on the interface during data copy hits. DQ[7:1] & DQ[15:9] should be considered zero during these data copy hits for both the encoding and decoding of ECC. DC0=1 means hit on the 1st 8 beats of a burst, DC1=1 means hit on the 2nd 8 beats, DC2=1 means hit on the 3rd 8 beats of a BL32 burst, and DC3=1 means hit on the 4th 8 beats of a BL32 burst.

7.7.7 Link ECC (Cont'd)

On beats 0-6 of a Read burst, the Parity pin shall be held at a logic zero level. On a BL32 Read burst, the Parity pin shall also be held at a logic zero level during beats 16-22. In certain modes, a BL32 burst is separated between beats 0-15 and beats 16-31 of the burst. The beat numbers mentioned apply to the burst associated with a single DRAM command, regardless of whether such separation of the burst occurs.

On beat 0 of a Write burst, the Parity pin shall be held at a logic zero level. On a BL32 write burst, the Parity pin shall also be held at a logic zero level on beat 16. In certain modes, a BL32 burst is separated between beats 0-15 and beats 16-31 of the burst. The beat numbers mentioned apply to the burst associated with a single DRAM command, regardless of whether such separation of the burst occurs.

The DMI bits are covered by a separate ECC. The check matrix for this code is defined below.

Table 238 — ECC Check Matrix for DMI

Bit	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	C0	C1	C2	C3	C4	C5
S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	0	0	0
S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	0	0	0
S2	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0
S3	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	0	0
S4	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
S5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The bits labeled M0-M15 appear on the DMI pin on beats 0-15 in numerical order (16-31 in the 2nd half of a BL32 burst). The check bits from this ECC appear on the RDQS_t pin on a write. There is no DMI ECC on a Read. C0-C5 appear on beats 1-6 of the burst in numerical order (17-22 in the 2nd half of a BL32 burst).

Usage of the ECC check matrix for ENCODING:

During encoding, C0-C7 should be 0 for the purpose of calculating S0-S7 but the computed S0-S7 values must be used when calculating S8. The ECC output bits (S0-S8) are then utilized as C0-C8 for the interface and driven on the Parity signal at their previously defined bit locations within the burst.

The DMI ECC check matrix is used in the same fashion.

Usage of the ECC check matrix for DECODING:

During decoding, the ECC inputs to the matrix (C0-C8) are driven with the values which come from the Parity signal of the interface at their previously defined bit locations within the burst. The ECC output bits (S0-S8) are then used as the ECC syndrome for error detection & correction.

The DMI ECC check matrix is used in the same fashion.

Error Detection:

After decoding the data ECC, the resulting ECC syndrome [S8:S0] will be zero in the case of no ECC errors. When the syndrome is non-zero, S8 high indicates a single-bit error (SBE), while S8 low indicates a double-bit error (DBE).

After decoding the DMI ECC, the resulting ECC syndrome [S5:S0] will be zero in the case of no ECC errors. When the syndrome is non-zero, S5 high indicates a SBE, while S5 low indicates a DBE.

7.7.7 Link ECC (Cont'd)

Error Correction:

When a single-bit data error is detected, [S2:S0] point directly to the DQ bit in error, and [S7:S3] can be decoded to generate a pointer to the beat in which the error falls, thus pinpointing the bit which is in error. Note that [S7:S3] do not form a direct pointer to the beat number until this decoding is performed. When less than 2 ones appear in [S7:S3], the error is in C0-C8.

When a single-bit DMI error is detected, [S4:S2] can be decoded to generate the 2 MSBs of a pointer to the beat in which the error falls. Concatenating these 2 bits with [S1:S0] (which need no decoding), produces a 4-bit pointer to the beat number where the DMI error occurred. When less than 2 ones appear in [S4:S2], the error is in C0-C5.

Error reporting:

A counter of Single-Bit-Errors and a Double-Bit-Error flag will be maintained on the DRAM, both of which can be read through mode register MR43. The DRAM will also store both syndromes from the most recent single-bit ECC error in MR44 & MR45. Note that both the data syndrome and the DMI syndrome are stored at this time regardless of which one indicates an error. Refer to these mode register definitions for additional detail (Table 131, Table 133, and Table 135).

Errors on Write FIFO commands will be ignored: When an ECC error occurs on a Write-FIFO command, the DRAM will not correct the data or DMI bits, it will not increment the SBE_count or set the DBE_flag in MR43, and it will not save the ECC syndromes in MR44 & MR45.

The controller would want to ignore ECC errors in a similar fashion on Read-FIFO and Read DQ Calibration commands. These 2 commands (along with Write-FIFO) are used for interface training, and errors are expected to occur during this training.

ECC & DBI – Order of operations:

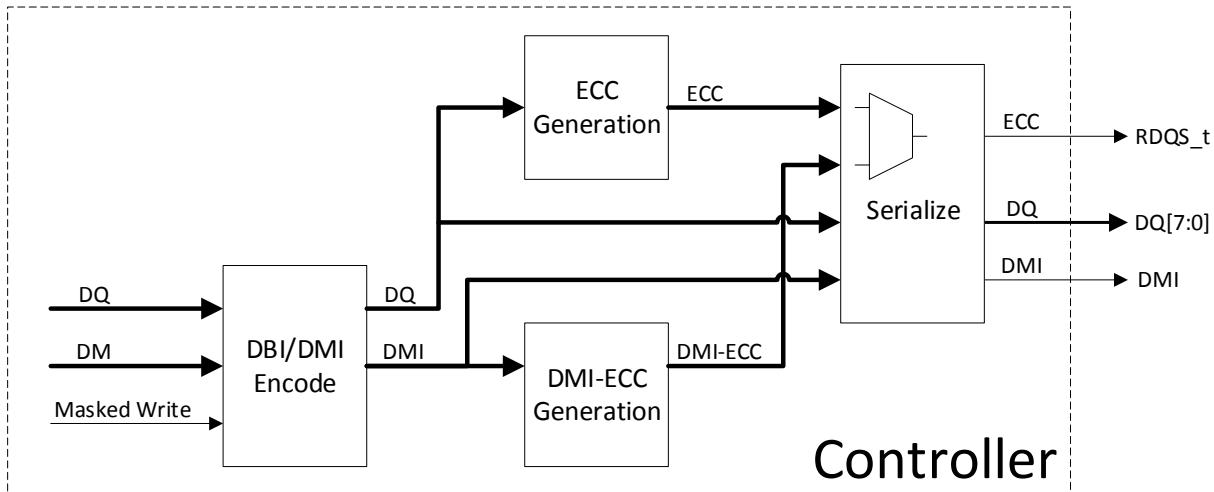
When transmitting Write data, the Controller can first perform DBI/DMI encoding of the data (if DBI is enabled). DBI encoding will follow the same rules as on LPDDR4. It can then perform ECC generation on the resulting Data and DMI bits (if ECC is enabled). It is important to perform ECC generation after the DBI encoding, as Masked writes can alter the data during DBI encoding. The modified data is used for calculating the data ECC in all cases. The 6-bit DMI ECC and 9-bit data ECC are both transmitted on the RDQS_t pin and sent at the bit-times previously defined.

Figure 183 illustrates the data flow.

When receiving Write data, the DRAM will first perform checking & correction on the DMI ECC. In parallel, it will perform ECC checking and correction on the data itself. Once the DMI is verified, it will proceed to perform DBI decoding of the data. DBI decoding follows the same rules as on LPDDR4. The Data ECC can be checked prior to DBI decoding due to the unique characteristics of the ECC code (the nature of the code is such that inverting an entire beat of the data would not change the ECC).

Figure 183 illustrates this data flow.

7.7.7 Link ECC (Cont'd)



Write operation

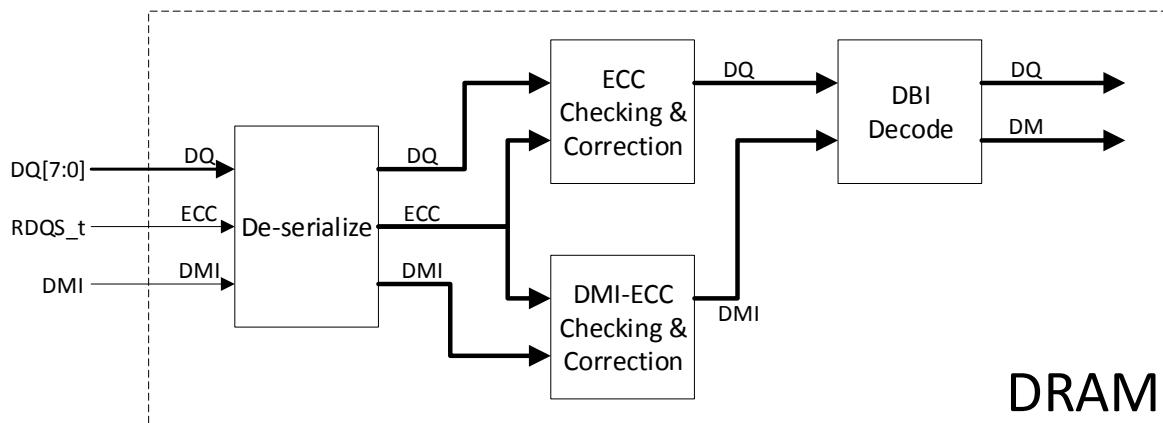
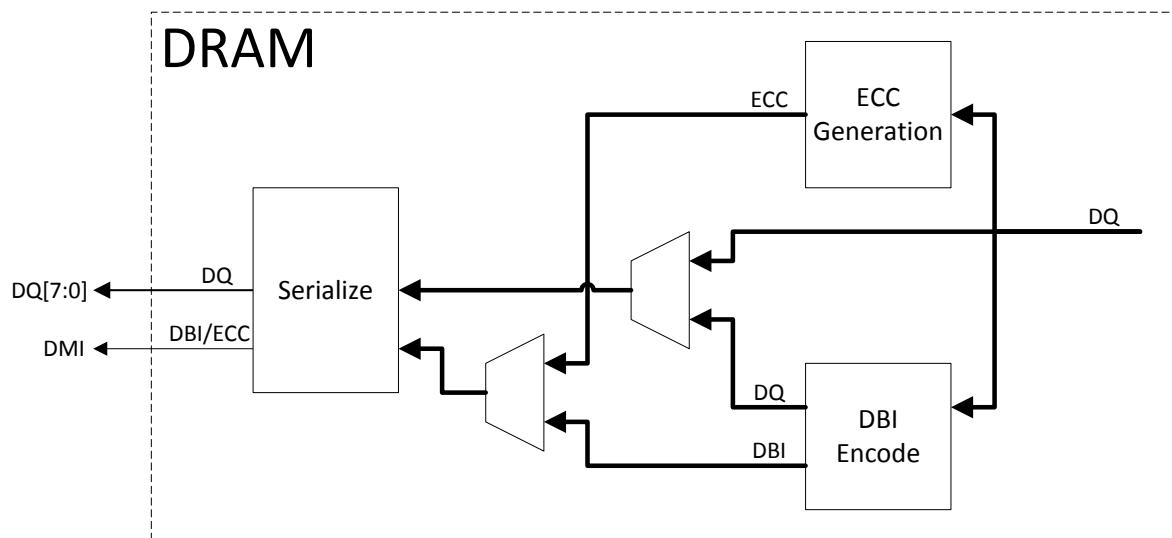


Figure 183 — Data flow on a memory Write operation

7.7.7 Link ECC (Cont'd)

When transmitting Read data, the DRAM will either perform DBI encoding (if DBI is enabled), or ECC generation on the data (if ECC is enabled). Which operation is performed will depend on the features enabled. Since Read DBI and Link ECC are mutually exclusive, it never needs to perform both functions, and it never needs to compute or transmit ECC on the DBI bits. The DBI encoding follows the same rules as on LPDDR4. See the Read operation diagram below which illustrates the data flow.

When receiving Read data, the Controller would want to perform either DBI decoding (if DBI is enabled), or ECC checking & correction (if ECC is enabled), depending on the features enabled. DBI decoding follows the same rules as on LPDDR4. The Read operation diagram illustrates this data flow.



Read operation

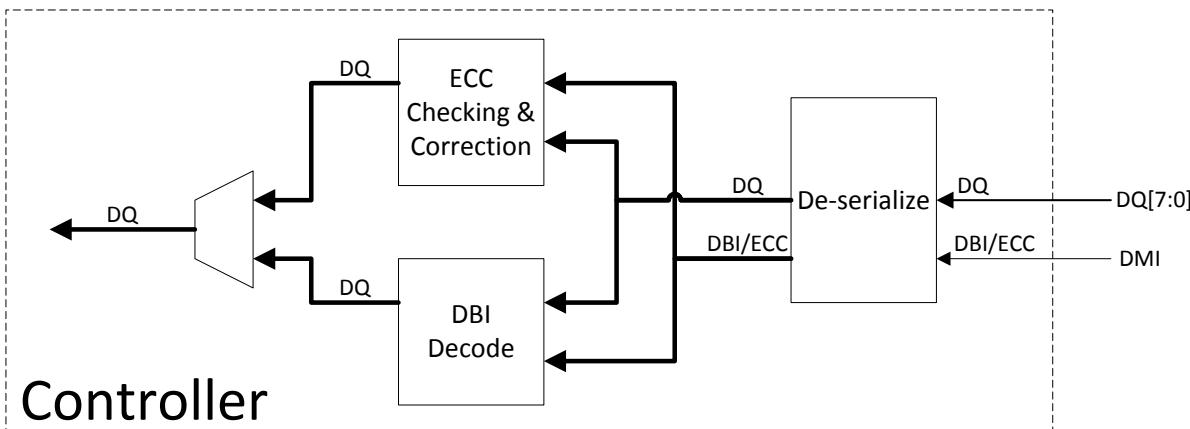


Figure 184 — Data flow on a memory Read operation

7.7.7 Link ECC (Cont'd)

Link Error Reporting Overview:

The DRAM keeps a count of single-bit interface error occurrences detected and corrected by the link ECC. A SBE occurrence is a 16b burst in which one or more SBEs are detected. It also sets a single flag if one or more double-bit interface errors have been detected by ECC. Since ECC checking always happens at the receiving end of the link, the DRAM is only detecting ECC errors on Write or Masked Write commands; errors on Read commands must be detected by the controller.

The controller can check to see if the DRAM has detected any errors by periodically reading MR43. The action of reading this register clears the SBE_count and DBE_flag. If any errors have been detected, the controller can optionally proceed to obtain the syndromes from the **most recent** single-bit ECC error by reading MR44 & MR45. This action would similarly clear the syndromes as each of these mode registers is read. The syndromes would primarily be used for debugging interface problems during system development; they have limited usefulness in a production system (except during failure analysis of field returns).

7.7.8 Single-ended mode for Clock, Write Clock and RDQS

LPDDR5 SDRAM supports the function of single-ended mode for Clock, Write Clock and Strobe independently to reduce power consumption during low frequency operation. The data rate is required to be equal or less than 1600Mbps and ODT and NT ODT states for CK, CA, WCK, RDQS, DQ and DMI are required to be unterminated during Single-ended mode for Clock, Write Clock and/or RDQS.

Entering and exiting single-ended mode for Clock, Write Clock and RDQS is controlled by the following MR setting.

- MR1 OP[3]: CK mode
- MR20 OP[1:0]: RDQS (Read DQS)
- MR20 OP[3:2] : WCK mode

Single-ended mode for RDQS affects to the following commands.

- Read
- Mode Register Read
- Read DQ Training
- Read FIFO
- RDQS toggle mode
- Enhanced RDQS training mode
- Duty Cycle Adjuster

The allowable combinations for CK_t/c, WCK_t/c and RDQS_t/c are shown in Table 239. The remaining combinations are inhibited.

Table 239 — Allowable combination among CK_t/c, WCK_t/c and RDQS_t/c

CK_t	CK_c	WCK_t	WCK_c	RDQS_t	RDQS_c
Enable	Enable	Enable	Enable	Enable	Enable
Enable	Disable	Enable	Enable	Enable	Enable
		Enable	Disable	Enable	Disable
		Disable	Enable	Disable	Enable
		Enable	Disable	Disable	Disable

7.7.8.1 Restriction of Single-ended mode

The following restriction applies under Single-ended mode.

Table 240 — Restriction of Single-ended mode for MR1 and MR20

Mode Register	Opcode	Description	Restriction
MR1	OP[3]=1 _B	Single-ended CK is enabled	CK_t is used as CK timing and CK_c is set to a valid logic state
MR20	OP[3:2]=01 _B	Single-ended WCK_t is enabled	WCK_t is used as WCK timing and WCK_c is set to a valid logic state
			WCK_t polarity is the same as when WCK_t is configured as differential OP[3:2]=00 _B
MR20	OP[3:2]=10 _B	Single-ended WCK_c is enabled	WCK_c is used as WCK timing and WCK_t is set to a valid logic state
			WCK_c polarity is the same as when WCK_c is configured as differential OP[3:2]=00 _B
MR20	OP[1:0]=01 _B	Single-ended RDQS_t is enabled	WCK_t is used as RDQS timing and RDQS_c is set to a valid logic state
			RDQS_t polarity is the same as when RDQS_c is configured as differential OP[1:0]=10 _B
MR20	OP[1:0]=10 _B	Single-ended RDQS_c is enabled	RDQS_c is used as RDQS timing and RDQS_t is set to a valid logic state
			WCK_c polarity is the same as when RDQS_c is configured as differential OP[1:0]=10 _B

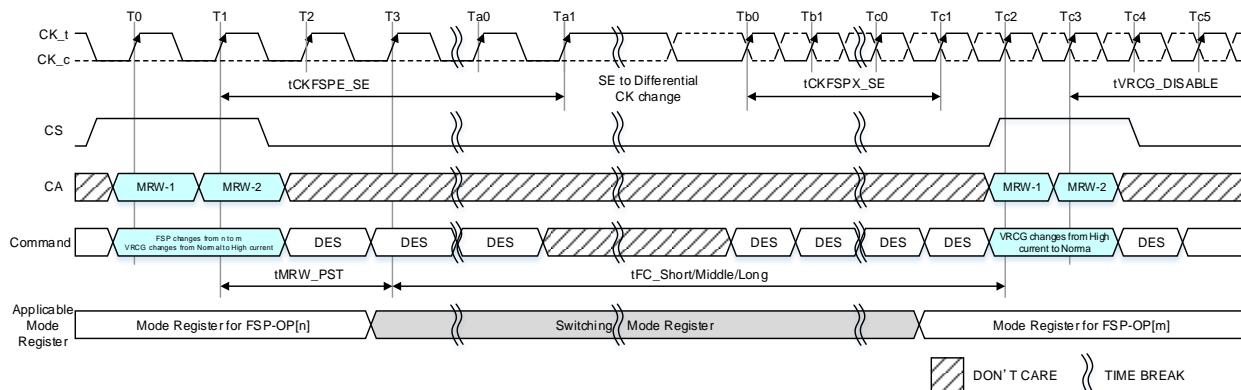
7.7.8.2 Switching sequence between Single-ended and Differential

The mode switching for WCK and RDQS can be made by both an MR setting by MRW command and Frequency Set Point (FSP) procedure.

Switching the CK mode from differential to single ended and vice versa is done only via FSP procedure. The frequency set point update timing for Differential from/to Single-ended mode switching is shown in Figure 185 and Figure 186.

When changing the frequency set point MR16 OP[3:2], the VRCG setting: MR16 OP[6] is required to be changed into V_{REF} Fast Response (high current) mode at the same time. After frequency change time (t_{FC}) is satisfied, VRCG can be changed into normal operation mode via MR16 OP[6].

When CK mode switches via FSP procedure, additional timing period is needed after MRW command.

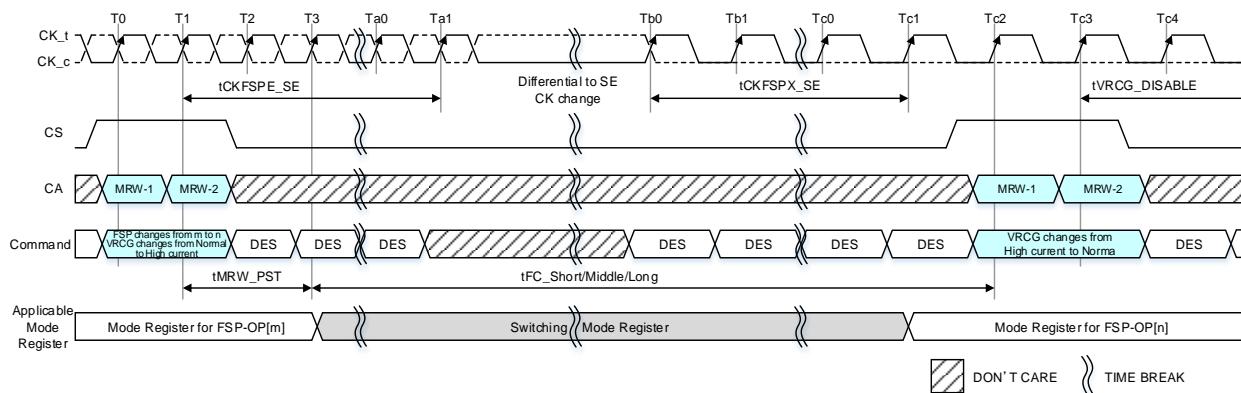


NOTE 1 The Clock frequency change definition should follow the frequency change operation. For more information, refer to 7.6.6, Input Clock Stop and Frequency Change.

NOTE 2 CK_c input level before Ta1 is an example. A stable high clock input is also allowed.

NOTE 3 Mode Register Setting FSP-OP=n: MR1 OP3=1_B: Single-Ended CK, Mode Register Setting FSP-OP=m: MR1 OP3=0_B: Differential CK.

Figure 185 — SE to Differential CK and Write DQS -FSP Switching Timing



NOTE 1 The Clock frequency change definition should follow the frequency change operation. For more information, refer to 7.6.6, Input Clock Stop and Frequency Change.

NOTE 2 Clock input level after Tb0 is an example. A stable high clock input is also allowed.

NOTE 3 Mode Register Setting FSP-OP=m: MR1 OP3=0_B: Differential CK Mode Register Setting FSP-OP=m: MR1 OP3=1_B: Single-Ended CK.

Figure 186 — Differential to SE CK and Write DQS -FSP Switching Timing

7.7.8.3 VRCG Enable timing

The VRCG Enable timing is postponed 2 clocks after MRW command to remove the effect of $V_{REF}(CA)$ variation by VRCG mode change when MR1 OP[3]: Single ended Clock has been set 1_B (Enable) at least one physical register is shown in Figure 187 and Figure 188.

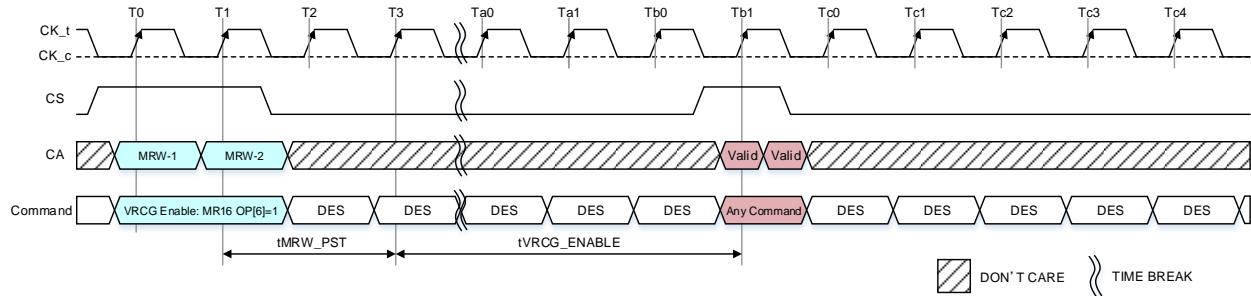


Figure 187 — VRCG status change to high current mode: Single-ended Clock Case

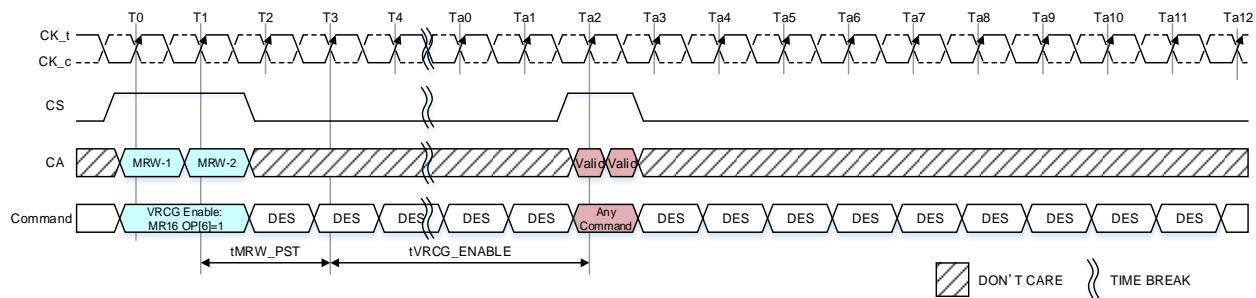


Figure 188 — VRCG status change to high current mode: Differential Clock Case

7.7.8.4 AC parameters for Single Ended (SE)

The AC timing is shown in Table 241 is applied under conditions of Single ended mode.

Table 241 — SE from/to Differential FSP and additional period for MRW AC timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
			Equal or less than 1600Mbps		
Frequency Set Point Parameters for Switching Single-ended from/to Differential Clock					
Valid Clock Requirement after entering FSP when changing between SE/Differential modes	tCKFSPE_SE	Min	Max(15ns, 8nCK)	-	
Valid Clock Requirement before first valid command after an FSP change between SE/Differential modes	tCKFSPX_SE	Min	Max(15ns, 8nCK)	-	
Additional period for after MRW command					
Post Clock for MRW	tMRW_PST	Min	2	nCK	

Table 242 — Delta CK and DQS Specification

Item	Min/ Max	Equal or less than 1600Mbps	Unit	Note
Vref for single ended CK	-	VDDQ/2	-	
Vref for single ended WCK	-	VDDQ/2	-	
tClVW1	Min	0.52	UI	UI = 0.5tCK
tClVW2	Min	0.35	UI	UI = 0.5tCK
tDlVW1	Min	0.52	UI	UI = 0.5tWCK,
tDlVW2	Min	0.35	UI	UI = 0.5tWCK,
tQSH	Min	tWCH-0.10	tWCK(avg)	
tQLS	Min	tWCL-0.10	tWCK(avg)	
tWCK2CK	Min	Max(-0.25*tWCK -100ps, TBDps)	ps	@WCK=800MHz, 2:1 mode CK/WCK asymmetrical
	Max	Max(0.25*tWCK +100ps, TBDps)	ps	

7.7.8.5 Command bus training procedure

TBD

8 Command Constraint and AC timing

8.1 Effective Burst Length (BL/n) Definition

Table 243 — Effective Burst Length (BL/n) Definition

WCK:CK Ratio	Bank ORG	Bank to Bank Constraints	WCK frequency	Burst Length (BL)	BL/n	BL/n_min	BL/n_max
2:1	16B Mode	Any Bank to Bank	$\leq 1600\text{MHz}$	BL16	$4*tCK (\text{BL}/4)$	$4*tCK (\text{BL}/4)$	$4*tCK (\text{BL}/4)$
				BL32	$8*tCK (\text{BL}/4)$	$8*tCK (\text{BL}/4)$	$8*tCK (\text{BL}/4)$
	8B Mode	Any Bank to Bank	$\leq 1600\text{MHz}$	BL32	$8*tCK (\text{BL}/4)$	$8*tCK (\text{BL}/4)$	$8*tCK (\text{BL}/4)$
		MRR, WFF, RFF, RDC ⁸⁾	$\leq 1600\text{MHz}$	BL16	$8*tCK (\text{BL}/2)$	$8*tCK (\text{BL}/2)$	$8*tCK (\text{BL}/2)$
4:1	16B Mode	Any Bank to Bank	$\leq 1600\text{MHz}$	BL16	$2*tCK (\text{BL}/8)$	$2*tCK (\text{BL}/8)$	$2*tCK (\text{BL}/8)$
				BL32	$4*tCK (\text{BL}/8)$	$4*tCK (\text{BL}/8)$	$4*tCK (\text{BL}/8)$
	BG Mode	Same BG	$> 1600\text{MHz}$	BL16	$4*tCK (2*\text{BL}/8)$	$2*tCK (\text{BL}/8)$	$4*tCK (2*\text{BL}/8)$
		Different BG			$2*tCK (\text{BL}/8)$		
		Same BG	$> 1600\text{MHz}$	BL32	$8*tCK (2*\text{BL}/8)$	$6*tCK (1.5*\text{BL}/8)$	$8*tCK (2*\text{BL}/8)$
		Different BG			$2*tCK (0.5*\text{BL}/8)$		
	8B Mode	Any Bank to Bank	Any freq	BL32	$4*tCK (\text{BL}/8)$	$4*tCK (\text{BL}/8)$	$4*tCK (\text{BL}/8)$
		MRR, WFF, RFF, RDC ⁸⁾	Any freq	BL16	$4*tCK (\text{BL}/4)$	$4*tCK (\text{BL}/4)$	$4*tCK (\text{BL}/4)$

NOTE 1 BL/n is minimum column to column cycle time, tCCD(min).

NOTE 2 BL/n_min is minimum burst data transfer time in DQ bus.

NOTE 3 BL/n_max is required column array cycle time to allow next column array cycle.

NOTE 4 BL/n, BL/n_min and BL/n_max are parameters in a CK domain.

NOTE 5 BL/n, BL/n_min and BL/n_max are same in an 8B or 16B mode.

NOTE 6 In case of same BG in a BG mode, BL/n = BL/n_max > BL/n_min.

NOTE 7 In case of different BG in a BG mode, BL/n=BL/n_min < BL/n_max for BL16, BL/n < BL/n_min < BL/n_max for BL32.

NOTE 8 For MRR, WFF, RFF and RDC commands in an 8B mode, normal Write/Read operation timings (BL32) are applied to WCK2CK SYNC Off and ODT/Non-target ODT.

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

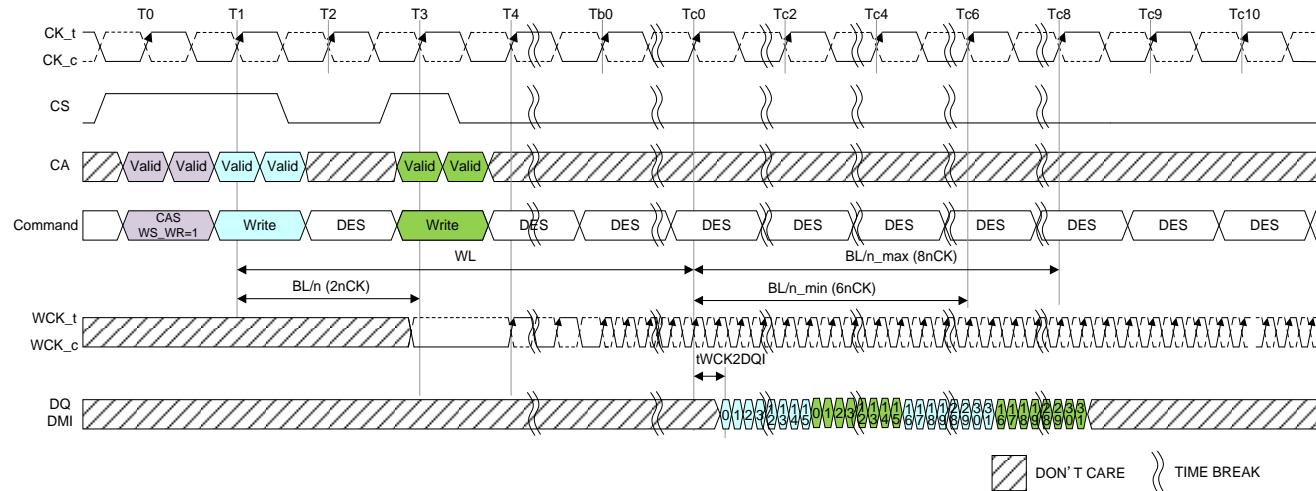


Figure 189 — Write Timing Diagram (BG mode, CKR=4:1, BL32) Example for BL/n, BL/n_min and BL/n_max

Table 244 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is disabled)

Current CMD \ Next CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (BL16 or BL32)	Illegal	BL/n	RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL	BL/n_min + RU(tRBTP/tCK) ¹⁾
WRITE (BL16)	Illegal	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	4*BL/n_max	WL + BL/n_min + 1 + RU(tWR/tCK)
WRITE (BL32)				2.5*BL/n_max	
MASK WRITE (BL16)	Illegal	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	4*BL/n_max	WL + BL/n_min + 1 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK)	Illegal	Illegal	Illegal	2

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

Table 245 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT is disabled)

Current CMD \ Next CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD_L/tCK)	1	1	1	1
READ (BL16 or BL32)	1	BL/n	RL + BL/n_max + RU(tWCKDQO(max) /tCK) - WL	RL + BL/n_max + RU(tWCKDQO(max) /tCK) - WL	1
WRITE (BL16)	1	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	BL/n_max	1
WRITE (BL32)	1	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	BL/n_max	1
MASK WRITE (BL16)	1	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	BL/n_max	1
PRECHARGE	1	1	1	1	2

Table 246 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is disabled)

Current CMD \ Next CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD_S/tCK)	1	1	1	1
READ (BL16 or BL32)	1	BL/n	RL + BL/n_min + RU(tWCKDQO(max) /tCK) - WL	RL + BL/n_min + RU(tWCKDQO(max) /tCK) - WL	1
WRITE (BL16)	1	WL + BL/n_min + RU(tWTR_S/tCK)	BL/n	BL/n	1
WRITE (BL32)	1	WL + BL/n_min + RU(tWTR_S/tCK)	BL/n	BL/n	1
MASK WRITE (BL16)	1	WL + BL/n_min + RU(tWTR_S/tCK)	BL/n	BL/n	1
PRECHARGE	1	1	1	1	2

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

Table 247 — Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is disabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (BL32)	Illegal	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	BL/n + RU(tRBTP/tCK) ¹⁾
WRITE (BL32)	Illegal	WL + BL/n + RU(tWTR/tCK)	BL/n	4*BL/n	WL + BL/n + 1 + RU(tWR/tCK)
MASK WRITE (BL32)	Illegal	WL + BL/n + RU(tWTR/tCK)	BL/n	4*BL/n	WL + BL/n + 1 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK)	Illegal	Illegal	Illegal	2

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP)

Table 248 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is disabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	1	1	1	1
READ (BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	1
WRITE (BL32)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1
MASK WRITE (BL32)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1
PRECHARGE	1	1	1	1	2

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

Table 249 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is disabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (BL16 or BL32)	Illegal	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	BL/n + RU(tRBTP/tCK) ¹⁾
WRITE (BL16)	Illegal	WL + BL/n + RU(tWTR/tCK)	BL/n	4*BL/n	WL + BL/n + 1 + RU(tWR/tCK)
WRITE (BL32)				2.5*BL/n	
MASK WRITE (BL16)	Illegal	WL + BL/n + RU(tWTR/tCK)	BL/n	4*BL/n	WL + BL/n + 1 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK)	Illegal	Illegal	Illegal	2

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP)

Table 250 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is disabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	1	1	1	1
READ (BL16 or BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	RL + BL/n + RU(tWCKDQO(max)/tCK) - WL	1
WRITE (BL16)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1
WRITE (BL32)					
MASK WRITE (BL16)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1
PRECHARGE	1	1	1	1	2

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

Table 251 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is enabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL16 or BL32)	Illegal	BL/n	$RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	$RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	$BL/n_min + RU(tRBTP/tCK)^1$

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP)

Table 252 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT is enabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL16 or BL32)	1	BL/n	$RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	$RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	1

Table 253 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is enabled)

Next CMD \ Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL16 or BL32)	1	BL/n	$RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	$RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	1

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

Table 254 — Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is enabled)

Next CMD Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL32)	Illegal	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	BL/n + RU(tRBTP/tCK) ¹⁾

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP)

Table 255 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is enabled)

Next CMD Current CMD	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	1

8.1 Effective Burst Length (BL/n) Definition (Cont'd)

Table 256 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is enabled)

Next CMD Current CMD \	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL16 or BL32)	Illegal	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	BL/n + RU(tRBTP/tCK) ¹⁾

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP)

Table 257 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is enabled)

Next CMD Current CMD \	ACTIVE	READ	WRITE	MASK WRITE	PRECHARGE
READ (BL16 or BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	1

8.1.1 Auto Precharge Command Timing Constraints

Table 258 — Auto Precharge Command Timing Constraints for Same Banks in Same Bank Group

Next CMD \\ Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE or PRECHARGE ALL
READ with AP (BL16 or BL32)	$BL/n_{min} + nRBTP^1) + RU(tRPpb/tCK)$	illegal	illegal	illegal	$BL/n_{min} + nRBTP^1)$
WRITE with AP (BL16 or BL32)	$WL + BL/n_{min} + 1 + nWR + RU(tRPpb/tCK)$	illegal	illegal	illegal	$WL + BL/n_{min} + 1 + nWR$
MASK WRITE with AP (BL16)	$WL + BL/n_{min} + 1 + nWR + RU(tRPpb/tCK)$	illegal	illegal	illegal	$WL + BL/n_{min} + 1 + nWR$

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP).

Table 259 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT Disabled)

Next CMD \\ Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL16 or BL32)	1	BL/n	$RL + BL/n_{max} + RU(tWCKDQO(max)/tCK) - WL$	$RL + BL/n_{max} + RU(tWCKDQO(max)/tCK) - WL$	1
WRITE with AP (BL16)	1	$WL + BL/n_{max} + RU(tWTR_L/tCK)$	BL/n	BL/n_max	1
WRITE with AP (BL32)					
MASK WRITE with AP (BL16)	1	$WL + BL/n_{max} + RU(tWTR_L/tCK)$	BL/n	BL/n_max	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in Same Bank Group (Table 258) is applied.

Table 260 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT Disabled)

Next CMD \\ Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL16 or BL32)	1	BL/n	$RL + BL/n_{min} + RU(tWCKDQO(max)/tCK) - WL$	$RL + BL/n_{min} + RU(tWCKDQO(max)/tCK) - WL$	1
WRITE with AP (BL16)	1	$WL + BL/n_{min} + RU(tWTR_S/tCK)$	BL/n	BL/n	1
WRITE with AP (BL32)					
MASK WRITE with AP (BL16)	1	$WL + BL/n_{min} + RU(tWTR_S/tCK)$	BL/n	BL/n	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in Same Bank Group (Table 258) is applied.

8.1.1 Auto Precharge Command Timing Constraints (Cont'd)

Table 261 — Command Timing Constraints for Same Banks in 8B Mode

Next CMD \\ Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE or PRECHARGE ALL
READ with AP (BL32)	BL/n + nRBTP ¹⁾ + RU(tRPpb/tCK)	illegal	illegal	illegal	BL/n + nRBTP ¹⁾
WRITE with AP (BL32)	WL + BL/n + 1 + nWR + RU(tRPpb/tCK)	illegal	illegal	illegal	WL + BL/n + 1 + nWR
MASK WRITE with AP (BL32)	WL + BL/n + 1 + nWR + RU(tRPpb/tCK)	illegal	illegal	illegal	WL + BL/n + 1 + nWR

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP).

Table 262 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT Disabled)

Next CMD \\ Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max) /tCK) - WL	RL + BL/n + RU(tWCKDQO(max) /tCK) - WL	1
WRITE with AP (BL32)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1
MASK WRITE with AP (BL32)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1

NOTE In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in 8B Mode (Table 261) is applied.

Table 263 — Command Timing Constraints for Same Banks in 16B Mode

Next CMD \\ Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE or PRECHARGE ALL
READ with AP (BL16 or BL32)	BL/n + nRBTP ¹⁾ + RU(tRPpb/tCK)	illegal	illegal	illegal	BL/n + nRBTP ¹⁾
WRITE with AP (BL16 or BL32)	WL + BL/n + 1 + nWR + RU(tRPpb/tCK)	illegal	illegal	illegal	WL + BL/n + 1 + nWR
MASK WRITE with AP (BL16)	WL + BL/n + 1 + nWR + RU(tRPpb/tCK)	illegal	illegal	illegal	WL + BL/n + 1 + nWR

NOTE 1 Refer to 7.4.4, READ burst end to PRECHARGE delay (tRBTP).

8.1.1 Auto Precharge Command Timing Constraints (Cont'd)

Table 264 – Command Timing Constraints for Different Banks in 16B Mode (DQ ODT Disabled)

Next CMD Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL16 or BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max) /tCK) - WL	RL + BL/n + RU(tWCKDQO(max) /tCK) - WL	1
WRITE with AP (BL16 or BL32)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1
MASK WRITE with AP (BL16)	1	WL + BL/n + RU(tWTR/tCK)	BL/n	BL/n	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in 16B Mode (Table 263) is applied.

Table 265 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT Enabled)

Next CMD Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL16 or BL32)	1	BL/n	RL + BL/n_max + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1	RL + BL/n_max + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in Same Bank Group (Table 258) is applied.

Table 266 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT Enabled)

Next CMD Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL16 or BL32)	1	BL/n	RL + BL/n_min + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1	RL + BL/n_min + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in Same Bank Group (Table 258) is applied.

8.1.1 Auto Precharge Command Timing Constraints (Cont'd)

Table 267 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT Enabled)

Next CMD Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	RL + BL/n + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in 8B Mode (Table 261) is applied.

Table 268 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT Enabled)

Next CMD Current CMD	ACTIVE	READ with or without AP	WRITE with or without AP	MASK WRITE with or without AP	PRECHARGE ¹⁾
READ with AP (BL16 or BL32)	1	BL/n	RL + BL/n + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	RL + BL/n + RU(tWCKDQO(max) /tCK) + RD(tRPST/tCK) – ODTLon – RD(tODTon(min)/tCK) + 1	1

NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in 16B Mode (Table 263) is applied.

8.1.2 CAS Command Timing Constraints

Table 269 — CAS (WS_FS) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (WS_FS=1, WS_WR=0, WS_RD=0)	POWER DOWN ENTRY (PDE)	RU(tCMDPD/tCK)	-	
	ACTIVATE-1 (ACT-1)	1	-	
	ACTIVATE-2 (ACT-2)	1	-	2
	PRECHARGE (PRE) (Per Bank, All Banks)	1	-	
	REFRESH (REF) (Per Bank, All Banks)	1	-	
	MASK WRITE (MWR)	1	8	
	WRITE (WR/WR16/WR32)	1	8	
	READ (RD/RD16/RD32)	1	8	
	CAS (WS_WR)	illegal	illegal	1
	CAS (WS_RD)	illegal	illegal	1
	CAS (WS_FS)	illegal	illegal	1
	CAS (WS_OFF)	6	-	4
	CAS (DC0-3)	2	-	
	CAS (WRX)	2	-	
	CAS (B3)	2	-	
	MULTI PURPOSE COMMAND (MPC)	1	-	
	SELF REFRESH ENTRY (SRE)	1	-	
	SELF REFRESH EXIT (SRX)	1	-	
	DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)	RU(tCMDPD/tCK)	-	
	MODE REGISTER WRITE-1 (MRW-1)	1	-	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	1	8	
	WRITE FIFO (WFF)	1	8	
	READ FIFO (RFF)	1	8	
	READ DQ CALIBRATION (RDC)	1	8	

NOTE 1 Duplicated WCK2CK SYNC initiation is illegal.

NOTE 2 It is illegal unless an ACT-1 command is issued before the current command (CAS-WS_FS).

NOTE 3 When CAS-FAST_SYNC (WS_FS=1, WS_WR=0, WS_RD=0) is issued, other CAS operands (DC0-3, WRX, B3) shall be "0".

NOTE 4 Max(tWCKENL_FS + tWCKPRE_Static) = 6nCK.

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 270 — CAS (WS_WR) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (WS_WR=1, WS_FS=0, WS_RD=0)	POWER DOWN ENTRY (PDE)	illegal	illegal	
	ACTIVATE-1 (ACT-1)	illegal	illegal	
	ACTIVATE-2 (ACT-2)	illegal	illegal	
	PRECHARGE (PRE) (Per Bank, All Banks)	illegal	illegal	
	REFRESH (REF) (Per Bank, All Banks)	illegal	illegal	
	MASK WRITE (MWR)	1	1	2
	WRITE (WR/WR16/WR32)	1	1	2
	READ (RD/RD16/RD32)	illegal	illegal	
	CAS (WS_WR)	illegal	illegal	
	CAS (WS_RD)	illegal	illegal	
	CAS (WS_FS)	illegal	illegal	
	CAS (WS_OFF)	illegal	illegal	
	CAS (DC0-3)	illegal	illegal	
	CAS (WRX)	illegal	illegal	
	CAS (B3)	illegal	illegal	
	MULTI PURPOSE COMMAND (MPC)	illegal	illegal	
	SELF REFRESH ENTRY (SRE)	illegal	illegal	
	SELF REFRESH EXIT (SRX)	illegal	illegal	
	DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)	illegal	illegal	
	MODE REGISTER WRITE-1 (MRW-1)	illegal	illegal	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	illegal	illegal	
	WRITE FIFO (WFF)	1	1	
	READ FIFO (RFF)	illegal	illegal	
	READ DQ CALIBRATION (RDC)	illegal	illegal	

NOTE 1 A CAS(WS_WR) command shall be followed by a MWR/WR/WR16/WR32/WFF command immediately without any command in between.

NOTE 2 When CAS(WS_WR=1, WS_RD=0, WS_FS=0) is issued, CAS operands (DC0-3 or WRX) can be applied together. Other CAS operand (B3) shall be "0".

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 271 — CAS (WS_RD) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (WS_RD=1, WS_WR=0, WS_FS=0)	POWER DOWN ENTRY (PDE)	illegal	illegal	
	ACTIVATE-1 (ACT-1)	illegal	illegal	
	ACTIVATE-2 (ACT-2)	illegal	illegal	
	PRECHARGE (PRE) (Per Bank, All Banks)	illegal	illegal	
	REFRESH (REF) (Per Bank, All Banks)	illegal	illegal	
	MASK WRITE (MWR)	illegal	illegal	
	WRITE (WR/WR16/WR32)	illegal	illegal	
	READ (RD/RD16/RD32)	1	1	2
	CAS (WS_WR)	illegal	illegal	
	CAS (WS_RD)	illegal	illegal	
	CAS (WS_FS)	illegal	illegal	
	CAS (WS_OFF)	illegal	illegal	
	CAS (DC0-3)	illegal	illegal	
	CAS (WRX)	illegal	illegal	
	CAS (B3)	illegal	illegal	
	MULTI PURPOSE COMMAND (MPC)	illegal	illegal	
	SELF REFRESH ENTRY (SRE)	illegal	illegal	
	SELF REFRESH EXIT (SRX)	illegal	illegal	
	DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)	illegal	illegal	
	MODE REGISTER WRITE-1 (MRW-1)	illegal	illegal	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	1	1	
	WRITE FIFO (WFF)	illegal	illegal	
	READ FIFO (RFF)	1	1	
	READ DQ CALIBRATION (RDC)	1	1	

NOTE 1 A CAS(WS_RD) command shall be followed by a MRR/RD/RD16/RD32/RFF/RDC command immediately without any command in between.

NOTE 2 When CAS(WS_RD=1, WS_WR=0, WS_FS=0) is issued, CAS operands (B3) can be applied together. Other CAS operands (DC0-3, WRX) shall be "0".

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 272 — CAS (WS_OFF) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (WS_OFF: WS_FS=1, WS_WR=1, WS_RD=1)	POWER DOWN ENTRY (PDE)	RU(tCMDPD/tCK)	-	
	ACTIVATE-1 (ACT-1)	1	-	
	ACTIVATE-2 (ACT-2)	1	-	1
	PRECHARGE (PRE) (Per Bank, All Banks)	1	-	
	REFRESH (REF) (Per Bank, All Banks)	1	-	
	MASK WRITE (MWR)	illegal	illegal	
	WRITE (WR/WR16/WR32)	illegal	illegal	
	READ (RD/RD16/RD32)	illegal	illegal	
	CAS (WS_WR)	3	-	
	CAS (WS_RD)	3	-	
	CAS (WS_FS)	3	-	
	CAS (WS_OFF)	illegal	-	
	CAS (DC0-3)	3	-	2
	CAS (WRX)	3	-	2
	CAS (B3)	3	-	2
	MULTI PURPOSE COMMAND (MPC)	1	-	
	SELF REFRESH ENTRY (SRE)	1	-	
	SELF REFRESH EXIT (SRX)	1	-	
	DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)	RU(tCMDPD/tCK)	-	
	MODE REGISTER WRITE-1 (MRW-1)	1	-	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	illegal	illegal	
	WRITE FIFO (WFF)	illegal	illegal	
	READ FIFO (RFF)	illegal	illegal	
	READ DQ CALIBRATION (RDC)	illegal	illegal	

NOTE 1 It is illegal unless an ACT-1 command is issued before the current command (CAS-WS_FS).

NOTE 2 New WCK2CK SYNC should be initiated together. If not, it is illegal.

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 273 — CAS (DC0-3), CAS (WRX) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (DC0-3) or CAS (WRX)	POWER DOWN ENTRY (PDE)	illegal	illegal	
	ACTIVATE-1 (ACT-1)	illegal	illegal	
	ACTIVATE-2 (ACT-2)	illegal	illegal	
	PRECHARGE (PRE) (Per Bank, All Banks)	illegal	illegal	
	REFRESH (REF) (Per Bank, All Banks)	illegal	illegal	
	MASK WRITE (MWR)	illegal	illegal	
	WRITE (WR/WR16/WR32)	1	1	1, 2
	READ (RD/RD16/RD32)	illegal	illegal	
	CAS (WS_WR)	illegal	illegal	3
	CAS (WS_RD)	illegal	illegal	3
	CAS (WS_FS)	illegal	illegal	3
	CAS (WS_OFF)	illegal	illegal	
	CAS (DC0-3)	illegal	illegal	
	CAS (WRX)	illegal	illegal	
	CAS (B3)	illegal	illegal	
	MULTI PURPOSE COMMAND (MPC)	illegal	illegal	
	SELF REFRESH ENTRY (SRE)	illegal	illegal	
	SELF REFRESH EXIT (SRX)	illegal	illegal	
	DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)	illegal	illegal	
	MODE REGISTER WRITE-1 (MRW-1)	illegal	illegal	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	illegal	illegal	
	WRITE FIFO (WFF)	illegal	illegal	
	READ FIFO (RFF)	illegal	illegal	
	READ DQ CALIBRATION (RDC)	illegal	illegal	

NOTE 1 Data Copy and WRITE X functions are mutually exclusive.

NOTE 2 CAS(DC0-3) or CAS(WRX) command should be followed by a WRITE command (WR/WR16/WR32) immediately without any command in between.

NOTE 3 WCK2CK SYNC should be initiated before issuing CAS(DC0-3) or CAS(WRX). Duplicated CAS-WCK2CK SYNC initiation is illegal.

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 274 — CAS (B3) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (B3=1)	POWER DOWN ENTRY (PDE)	illegal	illegal	
	ACTIVATE-1 (ACT-1)	illegal	illegal	
	ACTIVATE-2 (ACT-2)	illegal	illegal	
	PRECHARGE (PRE) (Per Bank, All Banks)	illegal	illegal	
	REFRESH (REF) (Per Bank, All Banks)	illegal	illegal	
	MASK WRITE (MWR)	illegal	illegal	
	WRITE (WR/WR16/WR32)	illegal	illegal	
	READ (RD/RD16/RD32)	1	1	2
	CAS (WS_WR)	illegal	illegal	
	CAS (WS_RD)	illegal	illegal	
	CAS (WS_FS)	illegal	illegal	
	CAS (WS_OFF)	illegal	illegal	
	CAS (DC0-3)	illegal	illegal	
	CAS (WRX)	illegal	illegal	
	CAS (B3)	illegal	illegal	
	MULTI PURPOSE COMMAND (MPC)	illegal	illegal	
	SELF REFRESH ENTRY (SRE)	illegal	illegal	
	SELF REFRESH EXIT (SRX)	illegal	illegal	
	DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)	illegal	illegal	
	MODE REGISTER WRITE-1 (MRW-1)	illegal	illegal	
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	illegal	illegal	1
	WRITE FIFO (WFF)	illegal	illegal	
	READ FIFO (RFF)	illegal	illegal	1
	READ DQ CALIBRATION (RDC)	illegal	illegal	1

NOTE 1 Burst Start Address (B3) is not valid in MRR, RFF and RDC operations.

NOTE 2 CAS(B3) command should be followed by a READ command (RD/RD16/RD32) immediately without any command in between.

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 275 — CAS(WS_FS), CAS(WS_WR), CAS(WS_RD), CAS(WS_OFF) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
POWER DOWN ENTRY (PDE)	CAS(WS_FS) or CAS(WS_WR) or CAS(WS_RD) or CAS(WS_OFF)	illegal	illegal	
ACTIVATE-1 (ACT-1)		1	-	
ACTIVATE-2 (ACT-2)		1	-	
PRECHARGE (PRE) (Per Bank, All Banks)		1	-	
REFRESH (REF) (Per Bank, All Banks)		1	-	
MASK WRITE (MWR)		WL + BL/n_max + RD(tWCKPST/tCK) + 1	-	2
WRITE (WR/WR16/WR32)		WL + BL/n_max + RD(tWCKPST/tCK) + 1	-	2
READ (RD/RD16/RD32)		RL + BL/n_max + RD(tWCKPST/tCK) + 1	-	2
CAS (WS_WR)		illegal	illegal	3
CAS (WS_RD)		illegal	illegal	3
CAS (WS_FS)		illegal	illegal	3
CAS (WS_OFF)		2	-	1
CAS (DC0-3)		illegal	illegal	3, 4
CAS (WRX)		illegal	illegal	3, 4
CAS (B3)		illegal	illegal	3, 4
MULTI PURPOSE COMMAND (MPC)		1	-	
SELF REFRESH ENTRY (SRE)		1	-	
SELF REFRESH EXIT (SRX)		RU(tXSR/tCK)	-	
DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)		illegal	illegal	
MODE REGISTER WRITE-1 (MRW-1)		illegal	illegal	
MODE REGISTER WRITE-2 (MRW-2)		RU(tMRD/tCK)	-	
MODE REGISTER READ (MRR)		RL + BL/n_max + RD(tWCKPST/tCK) + 1	-	2
WRITE FIFO (WFF)		WL + BL/n_max + RD(tWTR/tCK) - 1	-	2, 5, 8, 10
READ FIFO (RFF)		tRTRRD-1 or tRTW-1	-	2, 6, 9, 10
READ DQ CALIBRATION (RDC)		tRTRRD - 1	-	2, 7, 9, 10

NOTE 1 Duplicated WCK2CK SYNC OFF is illegal.

NOTE 2 WCK2CK SYNC automatic off timing delay from a current command (RD, WR, MWR, MRR, WFF, RFF, RDC) is "WL (or RL) + BL/n_max + RD(tWCKPST/tCK)".

NOTE 3 Duplicated WCK2CK SYNC initiation is illegal.

NOTE 4 WCK2CK SYNC should be initiated together or before issuing CAS(DC0-3) or CAS(WRX) or CAS(B3) command.

NOTE 5 Write (WR, WR16/32, MWR), Read (RD, RD16/32), MRR and RDC are not allowed. The min timing is applied to "CAS-WS_FS/WS_RD + RFF" only.

NOTE 6 "tRTRRD-1" timing (min) is applied to "CAS(WS_FS/WS_RD) + RD/MRR/RDC" or "CAS(WS_FS/WS_WR) + WR/MWR". "tRTW-1" timing(min) is applied in case of "CAS(WS_FS/WS_WR) + WFF".

NOTE 7 "CAS(WS_FS/WS_RD) + RFF" is not allowed.

NOTE 8 For CAS(WS_OFF), the min timing should be "WL + BL/n_max + RD(tWCKPST/tCK) + 1".

NOTE 9 For CAS(WS_OFF), the min timing should be "RL + BL/n_max + RD(tWCKPST/tCK) + 1".

NOTE 10 Refer to 8.1.3 for information on timing constraints for training commands.

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 276 — CAS(DC0-3), CAS(WRX) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
POWER DOWN ENTRY (PDE)	CAS(DC0-3) or CAS(WRX)	illegal	illegal	
ACTIVATE-1 (ACT-1)		1	-	
ACTIVATE-2 (ACT-2)		1	-	
PRECHARGE (PRE) (Per Bank, All Banks)		1	-	
REFRESH (REF) (Per Bank, All Banks)		1	-	
MASK WRITE (MWR)		BL/n -1	-	1
WRITE (WR/WR16/WR32)		BL/n - 1	-	1
READ (RD/RD16/RD32)		RL + BL/n_max + RU(tWCK2DQO(max) /tCK) - WL -1	-	1, 3
CAS (WS_WR)		illegal	illegal	
CAS (WS_RD)		illegal	illegal	
CAS (WS_FS)		2	TBD	
CAS (WS_OFF)		2	-	2
CAS (DC0-3)		illegal	illegal	
CAS (WRX)		illegal	illegal	
CAS (B3)		illegal	illegal	
MULTI PURPOSE COMMAND (MPC)		1	-	
SELF REFRESH ENTRY (SRE)		illegal	illegal	
SELF REFRESH EXIT (SRX)		RU(tXSR/tCK)	-	
DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)		illegal	illegal	
MODE REGISTER WRITE-1 (MRW-1)		illegal	illegal	
MODE REGISTER WRITE-2 (MRW-2)		RU(tMRD/tCK)	-	
MODE REGISTER READ (MRR)		RL + BL/n_max + RU(tWCK2DQO(max) /tCK) - WL + 1	-	1
WRITE FIFO (WFF)		illegal	illegal	1
READ FIFO (RFF)		tRTRRD - 1	-	1
READ DQ CALIBRATION (RDC)		tRTRRD - 1	-	1
NOTE 1 Refer to LPDDR5 command timing constraints.				
NOTE 2 New WCK2CK SYNC should be initiated together with CAS(DC0-3) or CAS(WRX). If not, it is illegal.				
NOTE 3 In case of DQ ODT enabled, READ-CAS(DC0-3/WRX) min timing should be "RL + BL/n_max + RU(tWCK2DQO(max) /tCK) - ODTLon - RD(tODTon(min)/tCK)".				
NOTE 4 Data Copy and WRITE X functions are mutually exclusive.				

8.1.2 CAS Command Timing Constraints (Cont'd)

Table 277 — CAS (B3) Command Timing Constraints

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
POWER DOWN ENTRY (PDE)	CAS(B3)	illegal	illegal	
ACTIVATE-1 (ACT-1)		1	-	
ACTIVATE-2 (ACT-2)		1	-	
PRECHARGE (PRE) (Per Bank, All Banks)		1	-	
REFRESH (REF) (Per Bank, All Banks)		1	-	
MASK WRITE (MWR)		WL + BL/n_max + RU(tWTR/tCK) - 1	-	1, 3
WRITE (WR/WR16/WR32)		WL + BL/n_max + RU(tWTR/tCK) - 1	-	1, 3
READ (RD/RD16/RD32)		BL/n - 1	-	1
CAS (WS_WR)		illegal	illegal	
CAS (WS_RD)		illegal	illegal	
CAS (WS_FS)		2	TBD	
CAS (WS_OFF)		2	-	2
CAS (DC0-3)		illegal	illegal	
CAS (WRX)		illegal	illegal	
CAS (B3)		illegal	illegal	
MULTI PURPOSE COMMAND (MPC)		1	-	
SELF REFRESH ENTRY (SRE)		illegal	illegal	
SELF REFRESH EXIT (SRX)		RU(tXSR/tCK)	-	
DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)		illegal	illegal	
MODE REGISTER WRITE-1 (MRW-1)		illegal	illegal	
MODE REGISTER WRITE-2 (MRW-2)		RU(tMRD/tCK)	-	
MODE REGISTER READ (MRR)		tMRR – 1	-	1
WRITE FIFO (WFF)		illegal	illegal	1
READ FIFO (RFF)		tRTRRD - 1	-	1
READ DQ CALIBRATION (RDC)		tRTRRD - 1	-	1

NOTE 1 Refer to LPDDR5 command timing constraints.

NOTE 2 New WCK2CK SYNC should be initiated together with CAS(B3). If not, it is illegal.

NOTE 3 tWTR in 8B/16B modes, tWTR_S in case of different BG in a BG mode, tWTR_L in case of same BG in a BG mode.

8.1.3 Training related timing constraints

LPDDR5-SDRAMs can be entered Read or Write training state by issuing such as WRITE FIFO, READ FIFO and READ DQ Calibration. For those training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the rising CK edge of each training command with the same timing relationship as any normal Read or Write command. Also, WCK synchronization should be applied in a same manner as normal Read or Write operation. WRITE FIFO, READ FIFO and READ DQ Calibration have a command burst length 16 regardless of bankgroup, 16bank or 8bank mode.

Table 278 —Training-Related Timing Constraints

Previous Command	Next Command	Min Delay	Unit	Note
WR/WR32/MWR/WRX	WRITE FIFO	tWRWTR	nCK	1,5
	READ FIFO	Not Allowed	-	2
	READ DQ Calibration	WL+BL/n_max +RU(tWTR/tCK)	nCK	5
RD/RD32/MRR	WRITE FIFO	tRTRRD	nCK	3,5
	READ FIFO	Not Allowed	-	2
	READ DQ Calibration	tRTRRD	nCK	3,5
WRITE FIFO	WR/WR32/MWR/WRX	Not Allowed	-	2
	WRITE FIFO	2 @ CK:WCK=1:4 4 @ CK:WCK=1:2	nCK	
	RD/RD32/MRR	Not Allowed	-	2
	READ FIFO	WL+BL/n_max +RU(tWTR/tCK)	nCK	5
	READ DQ Calibration	Not Allowed	-	2
READ FIFO	WR/WR32/MWR/WRX	tRTRRD	nCK	3,5
	WRITE FIFO	tRTW	nCK	4,5
	RD/RD32/MRR	tRTRRD	nCK	3,5
	READ FIFO	2 @ CK:WCK=1:4 4 @ CK:WCK=1:2	nCK	
	READ DQ Calibration	tRTRRD	nCK	3,5
READ DQ Calibration	WR/WR32/MWR/WRX	tRTRRD	nCK	3,5
	WRITE FIFO	tRTRRD	nCK	3,5
	RD/RD32/MRR	tRTRRD	nCK	3,5
	READ FIFO	Not Allowed	-	2
	READ DQ Calibration	2 @ CK:WCK=1:4 4 @ CK:WCK=1:2	nCK	

NOTE 1 tWRWTR = WL + BL/n_max + MAX[RU7.5ns/tCK],4nCK]

NOTE 2 No commands are allowed between WRITE FIFO and READ FIFO except MRW commands related to training parameter and CAS command related with WCK2CK SYNC operation.

NOTE 3 tRTRRD = RL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK]

NOTE 4 tRTW is TBD and has different value based on ODT state.

NOTE 5 CAS command may be needed for WCK sync prior to "Next Command"

8.1.4 MRR/MRW Timing Constraints

Table 279 — MRR/MRW Timing Constraints: DQ ODT is Disable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note
MRR	MRR	tMRR		2
	RD/RDA	RL +BL/n_max + RD(tWCKPST/tCK) +2		2
	WR/WRA/MWR/M WRA	RL+ BL/n_max +RU(tWCKDQO(max)/tCK) -WL+2	nCK	1
	MRW	RL+ BL/n_max +RU(tWCKDQO(max)/tCK)+2	nCK	1
RD/RDA	MRR	RL +BL/n_max + RD(tWCKPST/tCK) +2	nCK	1
WR/WRA/MWR/M WRA		WL+BL/n_max +RU(tWTR/tCK)	nCK	1,2
MRW		tMRD		
Power Down Exit		tXP + tMRRI		
MRW	RD/RDA	tMRD		
	WR/WRA/MWR/M WRA	tMRD		
	MRW	tMRW		
RD/RD FIFO/RD DQ CAL	MRW	RL+RU(tWCKDQO(max)/tCK)+BL/n_max+MAX[RU(7.5ns/tCK),4nCK]	nCK	1,2
RD with Auto-Precharge		RL+ RU(tWCKDQO(max)/tCK)+BL/n_max +MAX[RU(7.5ns/tCK),4nCK] +nRBTP	nCK	1,2
WR/MWR/WR FIFO		WL+BL/n_max +MAX[RU(7.5ns/tCK),4nCK]	nCK	1,2
WR/MWR with Auto-Precharge		WL+BL/n_max +MAX[RU(7.5ns/tCK),4nCK]+nWR	nCK	1,2

NOTE 1 The timing variable "BL/n" and "BL/n_max" are defined by the previous command and shown in Table 243, effective burst length definition.

NOTE 2 CAS command may be needed for WCK sync prior to "To Command"

8.1.4 MRR/MRW Timing Constraints (Cont'd)

Table 280 — MRR/MRW Timing Constraints: DQ ODT is Enable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note
MRR	MRR	Same as ODT Disable Case		
	RD/RDA	Same as ODT Disable Case		
	WR/WRA/MWR/MWRA	RL +RU(tWCKDQO(max)/tCK) + BL/n_max-ODTLon - RD(tODTon(min)/tCK)+2	nCK	1
	MRW	Same as ODT Disable Case		
RD/RDA	MRR	Same as ODT Disable Case		
WR/WRA/MWR/MWRA				
MRW				
Power Down Exit				
MRW	RD/RDA	Same as ODT Disable Case		
	WR/WRA/MWR/MWRA			
	MRW			
RD/RD FIFO/RD DQ CAL	MRW	Same as ODT Disable Case		
RD with Auto-Precharge				
WR/MWR/WR FIFO				
WR/MWR with Auto-Precharge				

NOTE 1 The timing variable "BL/n_max" is defined by the previous command and shown in the effective burst length table.,

8.1.5 Rank to Rank Command Timing Constraints

Table 281 — Command Timing Constraints in case of Different Ranks, ODT ON, CAS-WS_FS Broadcast ON

Next CMD \\ Current CMD	READ or RFF or MRR or RDC	WRITE or MASK WRITE or WFF	CAS (WS_WR)	CAS (WS_RD)	CAS (WS_FS)
READ (BL16 or BL32)	$BL/n_{min} + 1^2) + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$	$RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	illegal	illegal	illegal
RFF or MRR or RDC (BL16)	$BL/n_{min} + 1^2) + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$	$RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1$	illegal	illegal	illegal
WRITE (BL16 or BL32)	$ODTLoft + RU(tODToff(max)/tCK) - RL$	$ODTLoft + RU(tODToff(max)/tCK) - ODTLon$	illegal	illegal	illegal
MASK WRITE (BL16)	$ODTLoft + RU(tODToff(max)/tCK) - RL$	$ODTLoft + RU(tODToff(max)/tCK) - ODTLon$	illegal	illegal	illegal
WFF (BL16)	$ODTLoft + RU(tODToff(max)/tCK) - RL$	$ODTLoft + RU(tODToff(max)/tCK) - ODTLon$	illegal	illegal	illegal

NOTE 1 Next command is issued to a different rank.

NOTE 2 $RU(tWCK2DQO_rank2rank(max)/tCK) = 1$. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies.

NOTE 3 $RD(tWCK2DQO(min)/tCK) = 0$.

NOTE 4 Rank to Rank command timing constraints in this table are for LPDDR5 users design and consideration only.

8.1.5 Rank to Rank Command Timing Constraints (Cont'd)

**Table 282 — Command Timing Constraints in case of Different Ranks, ODT OFF,
CAS-WS_FS Broadcast ON**

Next CMD \\ Current CMD	READ or RFF or MRR or RDC	WRITE or MASK WRITE or WFF	CAS (WS_WR)	CAS (WS_RD)	CAS (WS_FS)
READ (BL16 or BL32)	$BL/n_{min} + 1^2) + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$	$RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - WL$	illegal	illegal	illegal
RFF or MRR or RDC (BL16)	$BL/n_{min} + 1^2) + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$	$RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - WL$	illegal	illegal	illegal
WRITE (BL16 or BL32)	$WL + BL/n_{min} + 1^3 - RL$	$BL/n_{min} + 1^4)$	illegal	illegal	illegal
MASK WRITE (BL16)	$WL + BL/n_{min} + 1^3 - RL$	$BL/n_{min} + 1^4)$	illegal	illegal	illegal
WFF (BL16)	$WL + BL/n_{min} + 1^3 - RL$	$BL/n_{min} + 1^4)$	illegal	illegal	illegal

NOTE 1 Next command is issued to a different rank.

NOTE 2 $RU(tWCK2DQO_rank2rank(max)/tCK) = 1$. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies.

NOTE 3 $RU(tWCK2DQI(max)/tCK) = 1$.

NOTE 4 $RU(tWCK2DQI_rank2rank(max)/tCK) = 1$. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies. If LPDDR5 DFE feature is enabled, an additional timing delay may be required like $RU[(tWCK2DQI(max) + tDPRE)/tCK]$.

NOTE 5 Rank to Rank command timing constraints in in this table are for LPDDR5 users design and consideration only.

8.1.5 Rank to Rank Command Timing Constraints (Cont'd)

Table 283 — Command Timing Constraints in case of Different Ranks, ODT ON, CAS-WS_FS Broadcast OFF

Next CMD \\ Current CMD	READ or RFF or MRR or RDC	WRITE or MASK WRITE or WFF	CAS (WS_WR)	CAS (WS_RD)	CAS (WS_FS)
READ (BL16 or BL32)	illegal	illegal	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - min[(ODTLon + RD(tODTon(min)/tCK)), tWCKENL_WR]$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_FS$
RFF or MRR or RDC (BL16)	illegal	illegal	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - min[(ODTLon + RD(tODTon(min)/tCK)), tWCKENL_WR]$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_FS$
WRITE (BL16 or BL32)	illegal	illegal	$WL + BL/n_{max} + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] - tWCKENL_WR$	$WL + BL/n_{max} + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] - tWCKENL_RD$	$WL + BL/n_{max} + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] - tWCKENL_FS$
MASK WRITE or WFF (BL16)	illegal	illegal	$WL + BL/n_{max} + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] - tWCKENL_WR$	$WL + BL/n_{max} + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] - tWCKENL_RD$	$WL + BL/n_{max} + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] - tWCKENL_FS$

NOTE 1 Next command is issued to a different rank.

NOTE 2 Rank to Rank command timing constraints in in this table are for LPDDR5 users design and consideration only.

Table 284 — Command Timing Constraints in case of Different Ranks, ODT OFF, CAS-WS_FS Broadcast OFF

Next CMD \\ Current CMD	READ or RFF or MRR or RDC	WRITE or MASK WRITE or WFF	CAS (WS_WR)	CAS (WS_RD)	CAS (WS_FS)
READ (BL16 or BL32)	illegal	illegal	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_WR$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_FS$
RFF or MRR or RDC (BL16)	illegal	illegal	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_WR$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD$	$RL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_FS$
WRITE (BL16 or BL32)	illegal	illegal	$WL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_WR$	$WL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD$	$WL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_FS$
MASK WRITE or WFF (BL16)	illegal	illegal	$WL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_WR$	$WL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD$	$WL + BL/n_{max} + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_FS$

NOTE 1 Next command is issued to a different rank.

NOTE 2 Rank to Rank command timing constraints in in this table are for LPDDR5 users design and consideration only.

9 AC Timing

9.1 Core AC Timing Parameters by Speed Grade

The two basic Core AC timing tables and its derivation Core AC timing tables are included this subclause. The SDRAM status for one basic Core AC timing table is x16, DVFSC is disabled and Link ECC is disabled and the SDRAM status for other basic Core AC timing table is x16, DVFSC is enabled and Link ECC is disabled. Byte mode (x8) and/or Link ECC is enabled affects tWR and tWTR value, which is described to the derivation tables.

9.1.1 Timing table for x16, DVFSC Disabled & Link ECC Disabled

Table 285 — x16 Core Timing for BG mode: DVFSC Disabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0
Core Timing for BG mode														
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab with all-bank precharge tRAS + tRPpb with per-bank precharge								-	-	-	
RAS-to-CAS delay	tRCD	Min	max(18ns, 2nCK)								-	-	-	
Row precharge time (all banks)	tRPab	Min	max(21ns, 2nCK)								-	-	-	
Row precharge time (single bank)	tRPpb	Min	max(18ns, 2nCK)								-	-	-	
Row active time	tRAS	Min	max(42ns, 3nCK)								-	-	-	
		Max	min(9 * tREFI * Refresh Rate, 70.2) μ s								-	-	-	
WRITE recovery time	tWR	Min	max(34ns, 3nCK)								-	-	-	
Active bank-A to active bank-B	tRRD	Min	max(5ns, 2nCK)								-	-	-	
Four-bank ACTIVATE window	tFAW	Min	20								ns	-	-	
READ Burst end to PRECHARGE command delay	tRBTP	Min	max(7.5ns, 4nCK) – 4nCK(CKR=2:1) max(7.5ns, 2nCK) – 2nCK(CKR=4:1)								-	-	-	
WRITE-to-READ delay	tWTR_S	Min	max(6.25ns, 4nCK)								-	-	-	
	tWTR_L	Min	max(12ns, 4nCK)								-	-	-	
Precharge to Precharge Delay	tPPD	Min	2								nCK	-	-	

Table 286 — x16 Core Timing for 16B mode: DVFSC Disabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0
Core Timing for 16B mode														
WRITE-to-READ delay	tWTR	Min	max(12ns, 4nCK)								-	-	-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 287 — x16 Core Timing for 8B mode: DVFSC Disabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0
Core Timing for 8B mode														
Active bank-A to active bank-B	tRRD	Min	max(10ns, 2nCK)								-	-	-	
Four-bank ACTIVATE window	tFAW	Min	40								ns	-	-	
WRITE-to-READ delay	tWTR	Min	max(12ns, 4nCK)								-	-	-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

9.1.1.1 Timing Table for x8 (Byte Mode) SDRAM

Table 288 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for BG mode																
WRITE recovery time	tWR	Min													-	
	tWTR_S	Min													-	
	tWTR_L	Min													-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 289 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for 16B mode																
WRITE recovery time	tWR	Min													-	
	tWTR	Min													-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 290 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for 8B mode																
Active bank-A to active bank-B	tRRD	Min													-	
Four-bank ACTIVATE window	tFAW	Min													ns	
WRITE recovery time	tWR	Min													-	
WRITE-to-READ delay	tWTR	Min													-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

9.1.1.2 Timing Table for Link ECC is enabled

Table 291 — x16 Core Timing for BG mode: DVFSC Disabled & Link ECC Enabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for BG mode																
WRITE recovery time	tWR	Min	max(38ns, 3nCK)										-	-		
WRITE-to-READ delay	tWTR_S	Min	max(10.25ns, 4nCK)										-	-		
	tWTR_L	Min	max(16ns, 4nCK)										-	-		

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 292 — x16 Core Timing for 16B mode: DVFSC Disabled & Link ECC Enabled

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 293 — x16 Core Timing for 8B mode: DVFSC Disabled & Link ECC Enabled

9.1.1.3 Timing Table for x8 (Byte Mode) SDRAM and Link ECC is enabled

Table 294 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Link ECC Enabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for BG mode																
WRITE recovery time	tWR	Min													-	
	tWTR_S	Min													-	
	tWTR_L	Min													-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 295 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Link ECC Enabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for 16B mode																
WRITE recovery time	tWR	Min													-	
	tWTR	Min													-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

Table 296 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Link ECC Enabled

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0		
Core Timing for 8B mode																
Active bank-A to active bank-B	tRRD	Min													-	
Four-bank ACTIVATE window	tFAW	Min													ns	
WRITE recovery time	tWR	Min													-	
WRITE-to-READ delay	tWTR	Min													-	

NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 285.

9.1.2 Timing table for x16, DVFS Enabled & Link ECC Disabled

Table 297 — x16 Core Timing for 16B mode: DVFSC Enabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 0	
Core Timing for 16B mode														
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab with all-bank precharge				tRAS + tRPpb with per-bank precharge				-			
RAS-to-CAS delay	tRCD	Min	max(19ns, 2nCK)								-			
Row precharge time (all banks)	tRPab	Min	max(21ns, 2nCK)								-			
Row precharge time (single bank)	tRPpb	Min	max(18ns, 2nCK)								-			
Row active time	tRAS	Min	max(42ns, 3nCK)								-			
		Max	min(9 * tREFI * Refresh Rate, 70.2) µs								-			
WRITE recovery time	tWR	Min	max(41ns, 3nCK)								-			
Active bank-A to active bank-B	tRRD	Min	max(5ns, 2nCK)								-			
Four-bank ACTIVATE window	tFAW	Min	20								ns			
READ Burst end to PRECHARGE command delay	tRBTP	Min	max(8.5ns, 4nCK) – 4nCK (CKR=2:1)				max(8.5ns, 2nCK) – 2nCK (CKR=4:1)				-			
		Max									-			
WRITE-to-READ delay	tWTR	Min	max(19ns, 4nCK)								-			
Precharge to Precharge Delay	tPPD	Min	2								nCK			

Table 298 — x16 Core Timing for 8B mode: DVFS Enabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes	
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0	
Core Timing for 8B mode															
Active bank-A to active bank-B	tRRD	Min	max(10ns, 2nCK)								-				
Four-bank ACTIVATE window	tFAW	Min	40								ns				

NOTE 1 The rest of the Core AC timing is the same as 16B mode: Table 297.

9.1.2.1 Timing Table for x8 (Byte Mode) SDRAM

Table 299 — Byte Mode Core Timing for 16B mode: DVFS Enabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes
			6	1	2	2	3	4	4	5	6	6		
Core Timing for 16B mode														
WRITE recovery time	tWR	Min						max(43ns, 3nCK)				-		
WRITE-to-READ delay	tWTR	Min						max(21ns, 4nCK)				-		

NOTE 1 The rest of the Core AC timing is the same as 16B mode: Table 297.

Table 300 — Byte Mode Core Timing for 8B mode: DVFS Enabled & Link ECC Disabled

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes	
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 5	8 0	
Core Timing for 8B mode															
Active bank-A to active bank-B	tRRD	Min	max(10ns, 2nCK)								-				
Four-bank ACTIVATE window	tFAW	Min	40								ns				
WRITE recovery time	tWR	Min	max(43ns, 3nCK)								-				
WRITE-to-READ delay	tWTR	Min	max(21ns, 4nCK)								-				

9.2 Core AC Temperature derating for AC Timing

Table 301 — Temperature Derating AC Timing

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Notes
			6 7	1 3	2 0	2 6	3 4	4 0	4 6	5 3	6 0	6 8	7 0	
Temperature Derating														
DQ to WCK input offset	tWCK2DQI_HF	Max												ps
	WCK2DQI_LF	Max												ps
WCK to DQ output offset	tWCK2DQO_HF	Max												ps
	tWCK2DQO_LF	Max												ps
RAS-to-CAS delay	tRCD	Min												-
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min												-
RAS-to-CAS delay	tRCD	Min												-
Row precharge time (all banks)	tRPab	Min												-
Row precharge time (single bank)	tRPpb	Min												-
Active bank-A to active bank-B	tRRD	Min												-

NOTE 1 Timing derating applies for operation at TBD °C to TBD °C.

10 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 302 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Note
VDD1 Supply Voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2H Supply Voltage relative to VSS	VDD2H	-0.4	1.5	V	1
VDD2L Supply Voltage relative to VSS	VDD2L	-0.4	1.5	V	1
VDDQ Supply Voltage relative to VSS	VDDQ	-0.4	1.5	V	1
Voltage on Any Ball Except VDD1 relative to VSS	VIN, VOUT	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

NOTE 1 See "Power-Up, Initialization" in 4.1 for relationships between power supplies.

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A.

11 AC and DC Operating Condition

11.1 Recommended DC Operating Conditions

Table 303 — Recommended DC Operating Conditions

DRAM	Symbol	Freq:DC to TBD MHz Voltage Spec				Freq: TBD MHz to TBD MHz Z(f) Spec		Notes
		Min	Typ	Max	Unit	Zmax	Unit	
Core 1 Power	VDD1	1.7	1.8	1.95	V	TBD	mOhm	1,2,9
Core 2 Power/Input Buffer Power	VDD2H	1.01	1.05	1.12	V	TBD	mOhm	1,2,9
	VDD2L	0.87	0.9	0.97	V	TBD	mOhm	1,2,9
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V	TBD	mOhm
		Spec Range-2	0.27	0.3	0.37	V		
		Allowable Range	0.27	N/A	0.57	V	N/A	5,6,7,8

NOTE 1 VDD1 uses significantly less current than VDD2H and VDD2L.

NOTE 2 DC to TBD MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask defined by VdIVW. Refer to Figure 190, DC voltage range.

NOTE 3 SPEC Range 1 is intended for IO operation with both ODT enabled and disabled.

NOTE 4 SPEC Range 2 is intended for IO operation with ODT disabled.

NOTE 5 IO operation at VDDQ levels between outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.

NOTE 6 Allowable range is valid only when DVFSQ enabled.

NOTE 7 100mV tolerance (-30mV/+70mV) is applied to VDDQ allowable ranges. Refer to Figure 191 VDDQ tolerance definition in allowable range.

NOTE 8 Vendors may support 0.6V. VDDQ (typ) as an option. Because ZQ calibration is optimized at VDDQ=0.5V, the output drive strength. May not be guaranteed at VDDQ=0.6V. Refer to a vendor's data sheet.

NOTE 9 Z(f) is per BGA pin per voltage domain. Z(f) does not include the DRAM package and silicon die.

11.1 Recommended DC Operating Conditions (Cont'd)

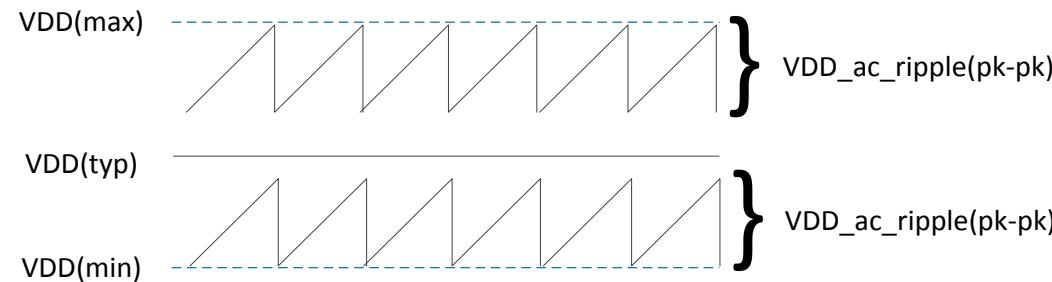


Figure 190 — DC Voltage Range

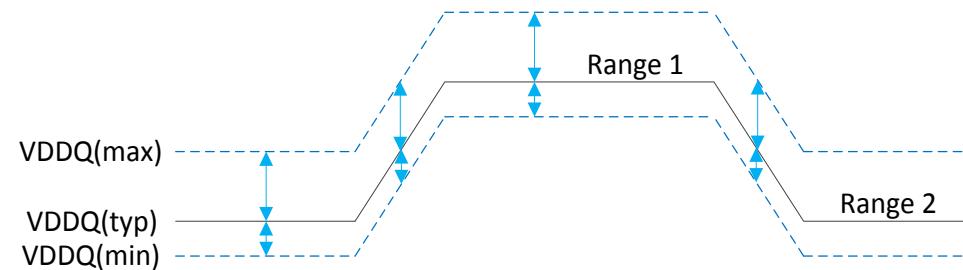


Figure 191 — VDDQ Tolerance Definition in Allowable Range

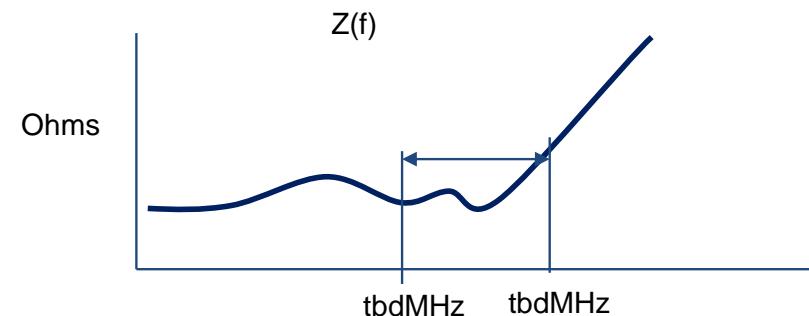


Figure 192 — Zprofile/ $Z(f)$ of the system at the DRAM package solder ball (without DRAM component)

11.2 Input Leakage Current

Table 304 — Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage Current	I_L	TBD	TBD	uA	1,2

NOTE 1 For CK_t, CK_c, WCK_t, WCK_c, CS, CA and RESET_n. Any input 0V ≤ VIN ≤ VDD2H (All other pins not under test = 0V).

NOTE 2 CA ODT is disabled for CK_t, CK_c, WCK_t, WCK_c and CA.

11.3 Input/Output Leakage Current

Table 305 — Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output Leakage Current	I_{OZ}	TBD	TBD	uA	1,2

NOTE 1 For DQ, RDQS_t, RDQS_c and DMI. Any I/O 0V ≤ VOUT ≤ VDDQ.

NOTE 2 I/Os status are disabled: High Impedance and ODT Off.

11.4 Operating Temperature Range

Table 306 — Operating Temperature Range

Parameter / Condition	Symbol	Min	Max	Unit	Notes
Standard	$T_{oper_standard}$	-25	85	°C	1,2,3
Elevated	$T_{oper_elevated}$	-25	105	°C	1,2,3

NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A.

NOTE 2 Some applications require operation of LPDDR5 in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For LPDDR5 devices, derating may be necessary to operate in this range.

NOTE 3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

11.4.1 Operating Temperature Range (Automotive spec addendum only)

Table 307 — Operating Temperature Range

Parameter / Condition	Symbol	Min	Max	Unit	Notes
Standard	$T_{oper_standard}$	-25	85	°C	1
Automotive Grade1	$T_{oper_auto_grade1}$	-40	125	°C	1,2,3,4
Automotive Grade 2	$T_{oper_auto_grade2}$	-40	105	°C	1,2,3,4
Automotive Grade 3	$T_{oper_auto_grade3}$	-40	85	°C	1,2,3,4

NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A.

NOTE 2 Automotive: Some applications require operation of LPDDR5 in the maximum temperature conditions over 85°C. For LPDDR5 devices, de-rating may be necessary to operate in this range (over 85°C).

NOTE 3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating, and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or automotive grades Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

NOTE 4 Automotive temperature condition is only allowed at the limited part which specifies the guarantee in the datasheet.

11.5 Electrostatic Discharge Sensitivity Characteristics

Table 308 — Electrostatic Discharge Sensitivity Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESD_{HBM}	1000		V	1
Charged-device model (CDM)	ESD_{CDM}	250		V	2

NOTE 1 Refer to ESDA/JEDEC Joint Standard JS-001-2017 for measurement procedures.

NOTE 2 Refer JESD22-A115C for measurement procedures.

12 AC and DC Input/Output Measurement levels

12.1 1.05V High speed LVC MOS

12.1.1 Standard specifications

All voltages are referenced to ground except where noted.

12.1.2 Input Level for Reset_n

LPDDR5 uses CMOS with VDD2H Reset_n signaling to ensure stable LPDDR5 reset operation.

Table 309 — Reset input level specification

Item	Symbol	Min/Max		Unit	Note
Reset_n ViH	ViH_RS	Min	0.8xVDD2H	V	
		Max	VDD2H+0.2	V	1
Reset_n ViL	ViL_RS	Min	-0.2	V	1
		Max	0.2xVDD2H	V	

NOTE 1 Refer LPDDR5 overshoot and undershoot, 12.1.4.

12.1.3 Input Level for CS

The definition applies to CS.

Table 310 — LPDDR5 Input Level for CS

Parameter	Symbol	Min	Max	Unit	Note
Input High Level	V _{IH}	TBD	TBD	V	1
Input Low Level	V _{IL}	TBD	TBD	V	1

NOTE 1 Refer LPDDR5 AC Over / Undershoot section, 12.1.4.

12.1.4 AC Overshoot / Undershoot

12.1.4.1 AC Overshoot / Undershoot

Table 311 — AC Overshoot / Undershoot

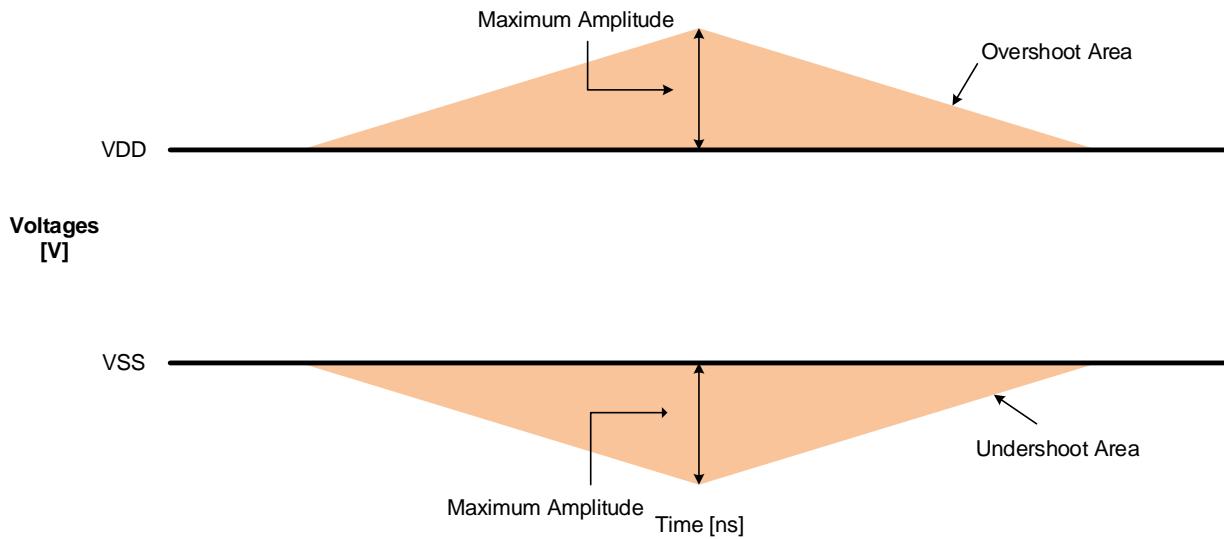
Parameter	Specification
Maximum Peak Amplitude allowed for overshoot area	0.35V
Maximum Peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD2H/VDDQ	0.8V·ns
Maximum undershoot area above VSS	0.8V·ns

12.1.4.2 AC Overshoot / Undershoot for LVSTL

Table 312 — LPDDR5 AC Overshoot / Undershoot for LVSTL

Parameter	Min/ Max	Data Rate				Units
		1600	3200	5500	6400	
Maximum Peak Amplitude allowed for overshoot area	Max	0.3	0.3	0.3	0.3	V
Maximum Peak Amplitude allowed for undershoot area	Max	0.3	0.3	0.3	0.3	V
Maximum overshoot area above VDD2H/VDDQ	Max	0.1	0.1	0.1	0.1	V·ns
Maximum undershoot area above VSS	Max	0.1	0.1	0.1	0.1	V·ns

12.1.4.2 AC Overshoot / Undershoot for LVSTL (Cont'd)



NOTE 1 VDD is VDD2H for CA[6:0] and CK_t/c, CS and RESET_n. VDD is VDDQ for DQ, DMI, RDQS_t, WCK_t/c

NOTE 2 Maximum peak amplitude values are referenced from actual VDD and VSS values.

NOTE 3 Maximum area values are referenced from maximum operating VDD and VSS values.

Figure 193 — Overshoot and Undershoot Definition

12.2 Differential Input Voltage

12.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

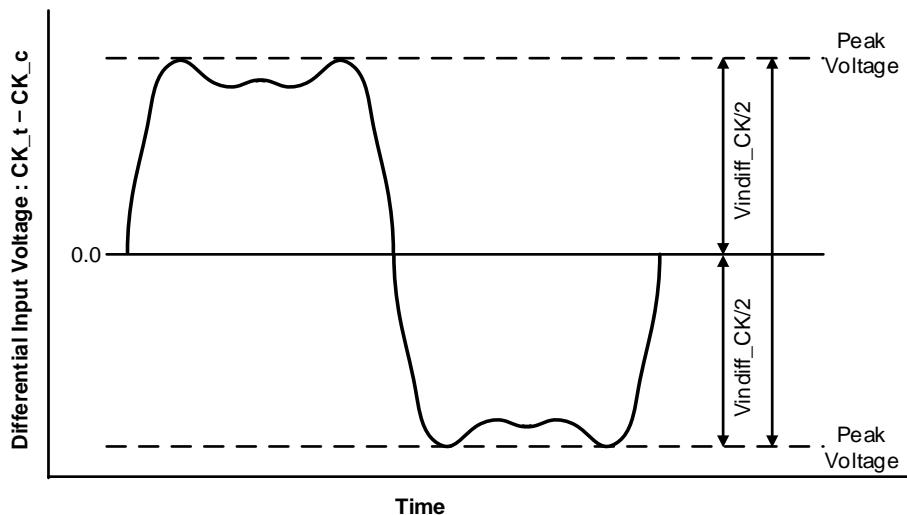


Figure 194 — CK Differential Input Voltage

12.2.1 Differential Input Voltage for CK (Cont'd)

Table 313 — CK Differential Input Voltage

Parameter	Symbol	Clock Rate						Unit	Note		
		266MHz		533MHz		800MHz					
		Min	Max	Min	Max	Min	Max				
CK Differential Input Voltage	Vindiff_CK	350	-	350	-	350	-	mV	1,2		

NOTE 1 Refer to Table 176 to match the clock rate to data rate.

NOTE 2 The peak voltage of Differential CK signals is calculated in a following equation.

$$\text{Vindiff_CK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VCK_t - VCK_c$$

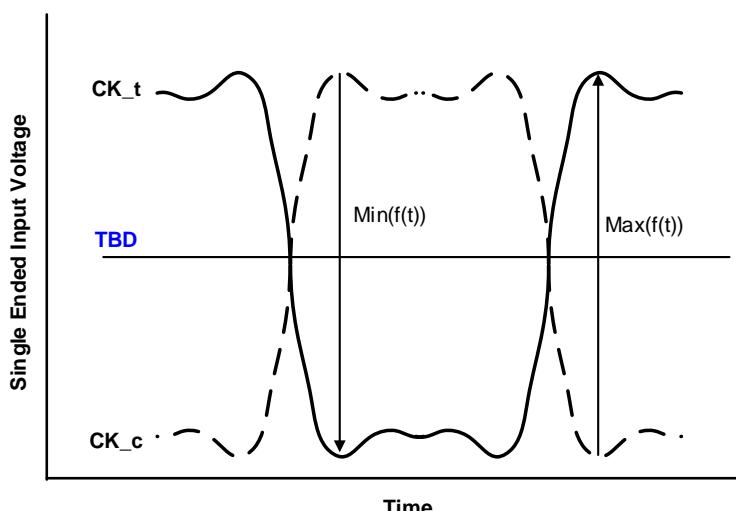
12.2.1.1 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals are calculated in a following equation.

$$\text{VIH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$\text{VIL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VCK_t - VCK_c$$

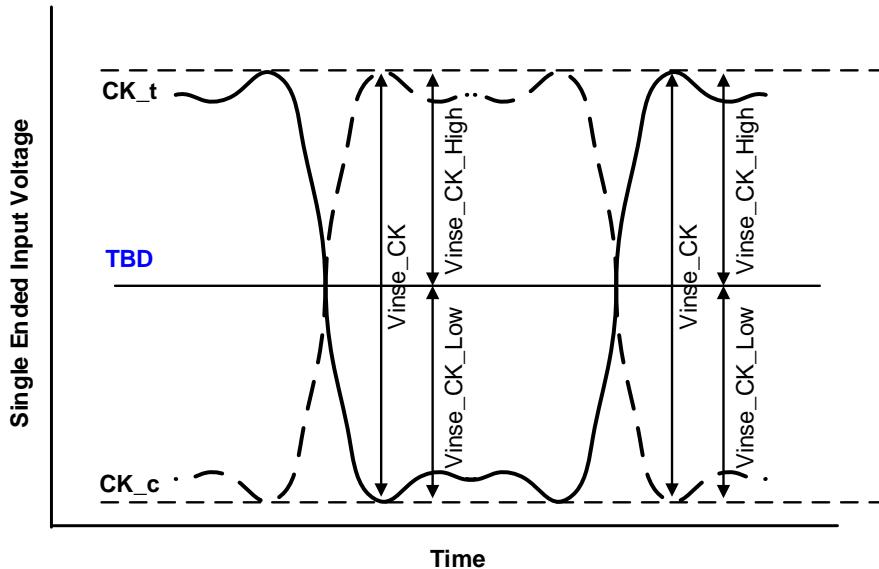


NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training.

Figure 195 — Definition of differential Clock Peak Voltage

12.2.1.2 Single ended Input Voltage for CK

The minimum input voltage need to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver.



NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training

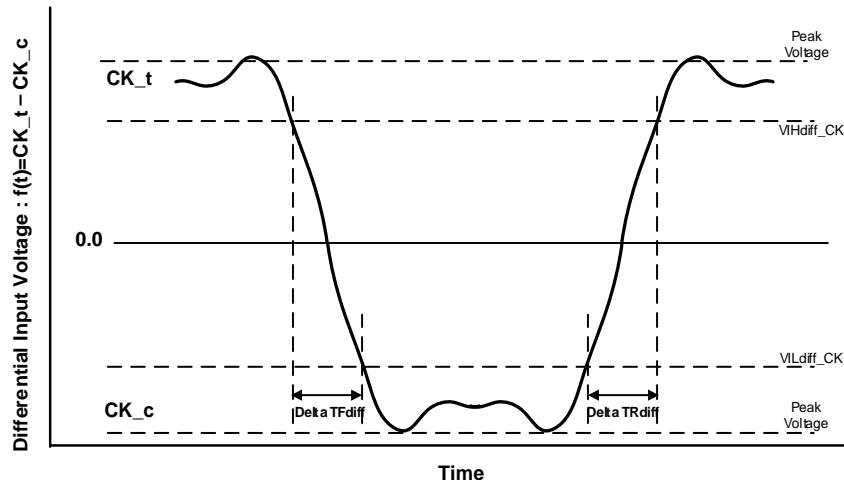
Figure 196 — Clock Single ended Input Voltage

Table 314 — Clock Single-Ended Input Voltage

Parameter	Symbol	Clock Rate						Unit	Note		
		266MHz		533MHz		800MHz					
		Min	Max	Min	Max	Min	Max				
Clock Single-ended input Voltage	Vinse_CK	175	-	175	-	175	-	mV			
Clock Single-ended input Voltage High from TBD	Vinse_CK_High	87.5	-	87.5	-	87.5	-	mV			
Clock Single-ended input Voltage Low from TBD	Vinse_CK_Low	87.5	-	87.5	-	87.5	-	mV			

12.2.1.3 Differential Input Slew Rate Definition for CK

Input slew rate for differential signals (CK_t , CK_c) are defined and measured as shown in Figure 197 and the following Tables.



- NOTE 1 Differential signal rising edge from VIL_{diff_CK} to VIH_{diff_CK} must be monotonic slope.
 NOTE 2 Differential signal falling edge from VIH_{diff_CK} to VIL_{diff_CK} must be monotonic slope.

Figure 197 — Differential Input Slew Rate Definition for CK_t , CK_c

Table 315 — Differential Input Slew Rate Definition for CK_t , CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge ($CK_t - CK_c$)	VIL_{diff_CK}	VIH_{diff_CK}	$ VIL_{diff_CK} - VIH_{diff_CK} /\Delta T_{Fdiff}$
Differential input slew rate for falling edge ($CK_t - CK_c$)	VIH_{diff_CK}	VIL_{diff_CK}	$ VIL_{diff_CK} - VIH_{diff_CK} /\Delta T_{Rdiff}$

Table 316 — Differential Input Level for CK_t , CK_c

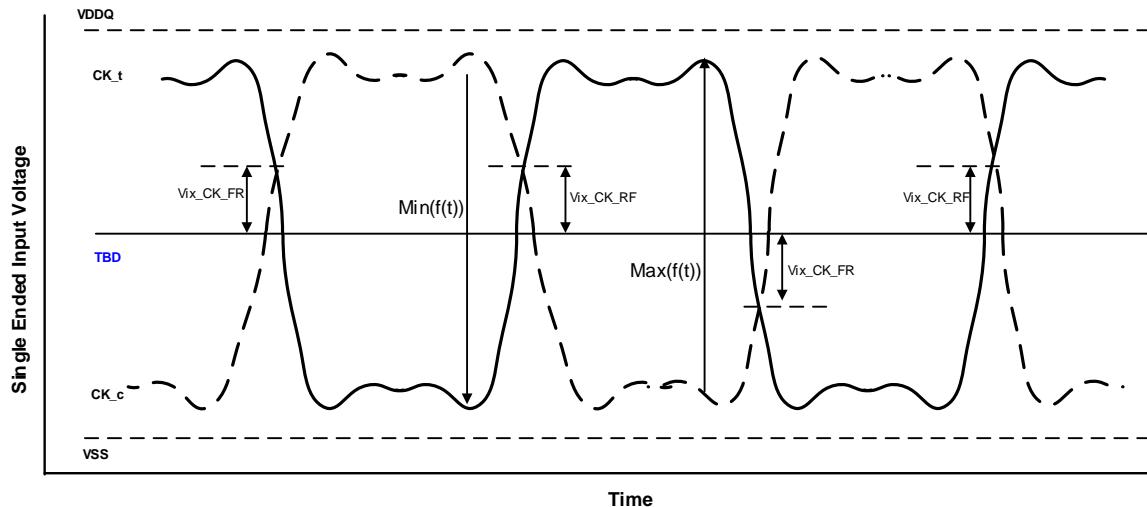
Parameter	Symbol	Clock Rate						Unit	Note		
		266MHz		533MHz		800MHz					
		Min	Max	Min	Max	Min	Max				
Differential Input High	VIH_{diff_CK}	145	-	145	-	145	-	mV			
Differential Input Low	VIL_{diff_CK}	-	-145	-	-145	-	-145	mV			

Table 317 — Differential Input Slew Rate for CK_t , CK_c

Parameter	Symbol	Clock Rate						Unit	Note		
		266MHz		533MHz		800MHz					
		Min	Max	Min	Max	Min	Max				
Differential Input Slew Rate for Clock	SRI_{diff_CK}	2	14	2	14	2	14	V/ns			

12.2.1.4 Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK_t , CK_c) must meet the requirements in Table 318. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is TBD.



NOTE 1 The base level of Vix_{CK_FR}/RF is TBD that is LPDDR5 SDRAM internal setting value by $Vref$ training.

Figure 198 — Differential Input Slew Rate Definition for CK_t , CK_c

Table 318 — Cross point voltage for differential input signals (Clock)

Parameter	Symbol	Clock Rate						Unit	Note		
		266MHz		533MHz		800MHz					
		Min	Max	Min	Max	Min	Max				
Clock Differential input crosspoint voltage ratio	Vix_{CK_ratio}	-	25	-	25	-	25	%	1,2		

NOTE 1 Vix_{CK_Ratio} is defined by this equation: $Vix_{CK_Ratio} = Vix_{CK_FR}/|Min(f(t))|$

NOTE 2 Vix_{CK_Ratio} is defined by this equation: $Vix_{CK_Ratio} = Vix_{CK_RF}/Max(f(t))$

12.2.2 Differential Input Voltage for WCK

The minimum input voltage need to satisfy both Vindiff_WCK and Vindiff_WCK /2 specification at input receiver and their measurement period is 1tWCK. Vindiff_WCK is the peak to peak voltage centered on 0 volts differential and Vindiff_WCK /2 is max and min peak voltage from 0V.

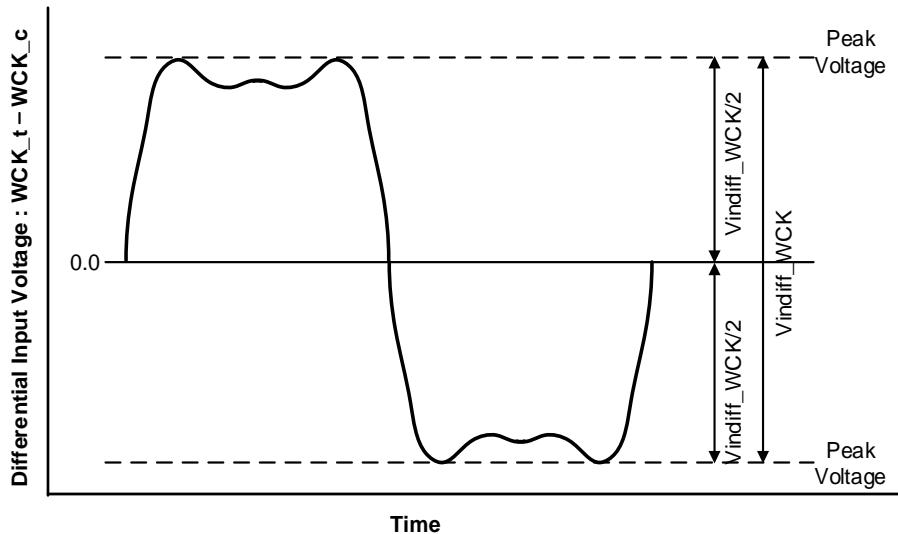


Figure 199 — WCK Differential Input Voltage

Table 319 — WCK differential input voltage

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		800		1066		1600		2133		2750		3200					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential Input Voltage	Vindiff_WCK	300	-	300	-	300	-	280	-	TBD	-	TBD	-	mV	1,2		

NOTE 1 Refer to Table 176 to match the WCK rate to data rate.

NOTE 2 The peak voltage of Differential WCK signals is calculated in a following equation.

$$\text{Vindiff_WCK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VWCK}_t - \text{VWCK}_c$$

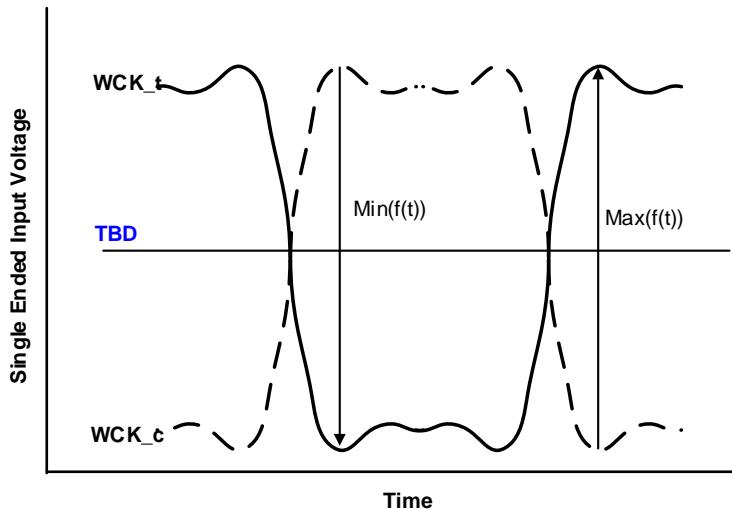
12.2.2.1 Peak Voltage Calculation Method

The peak voltage of Differential WCK signals are calculated in a following equation.

$$VIH.DIFF.Peak\ Voltage = \text{Max}(f(t))$$

$$VIL.DIFF.Peak\ Voltage = \text{Min}(f(t))$$

$$f(t) = VWCK_t - VWCK_c$$

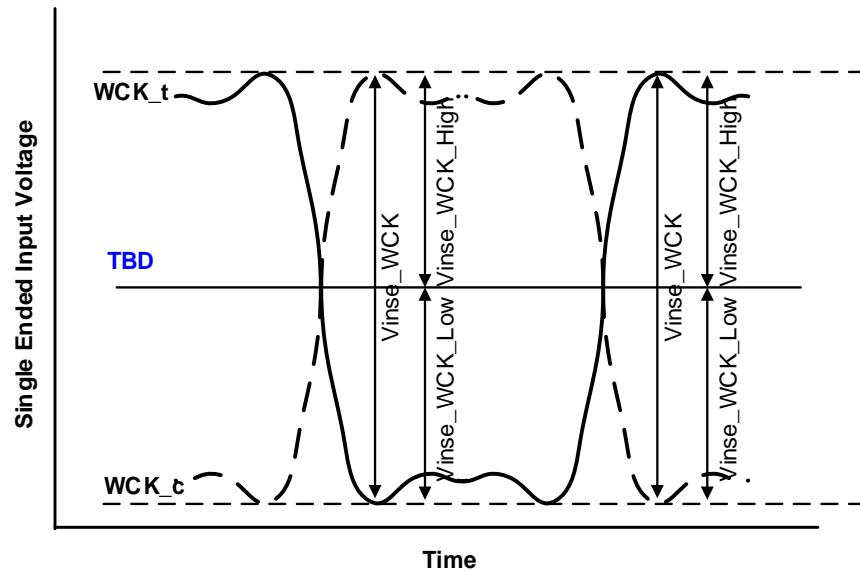


NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training.

Figure 200 — Definition of differential WCK Peak Voltage

12.2.2.2 Single ended Input Voltage for WCK

The minimum input voltage need to satisfy both Vinse_WCK, Vinse_WCK_High/Low specification at input receiver.



NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training

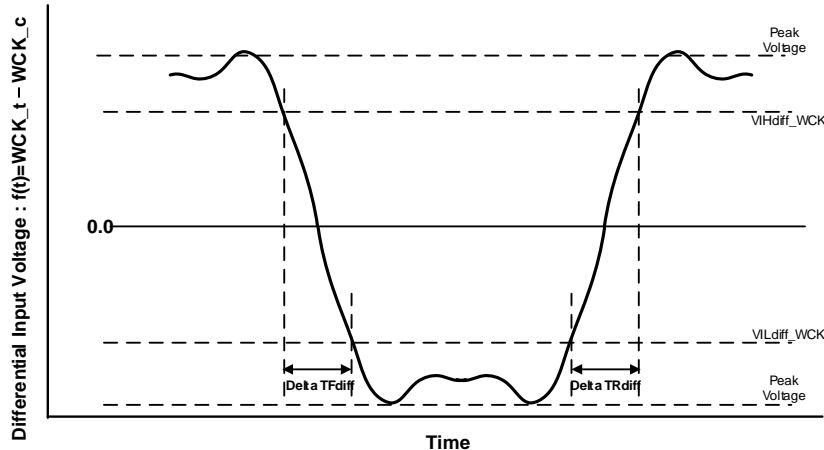
Figure 201 — WCK Single ended Input Voltage

Table 320 — WCK Single-Ended Input Voltage

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		800		1066		1600		2133		2750		3200					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Single-ended input Voltage	Vinse_WCK	150	-	150	-	150	-	140	-	TBD	-	TBD	-	mV			
WCK Single-ended input Voltage High from TBD	Vinse_WCK_High	75	-	75	-	75	-	70	-	TBD	-	TBD	-	mV			
WCK Single-ended input Voltage Low from TBD	Vinse_WCK_Low	75	-	75	-	75	-	70	-	TBD	-	TBD	-	mV			

12.2.2.3 Differential Input Slew Rate Definition for WCK

Input slew rate for differential signals (WCK_t, WCK_c) are defined and measured as shown in Figure 202 and the following Tables.



NOTE 1 Differential signal rising edge from VILdiff_WCK to VIHdiff_WCK must be monotonic slope.

NOTE 2 Differential signal falling edge from VIHdiff_WCK to VILdiff_WCK must be monotonic slope.

Figure 202 — Differential Input Slew Rate Definition for WCK_t, WCK_c

Table 321 — Differential Input Slew Rate Definition for WCK_t, WCK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (WCK_t - WCK_c)	VILdiff_WCK	VIHdiff_WCK	$ VILdiff_WCK - VIHdiff_WCK /\Delta TR_{diff}$
Differential input slew rate for falling edge (WCK_t - WCK_c)	VIHdiff_WCK	VILdiff_WCK	$ VILdiff_WCK - VIHdiff_WCK /\Delta TF_{diff}$

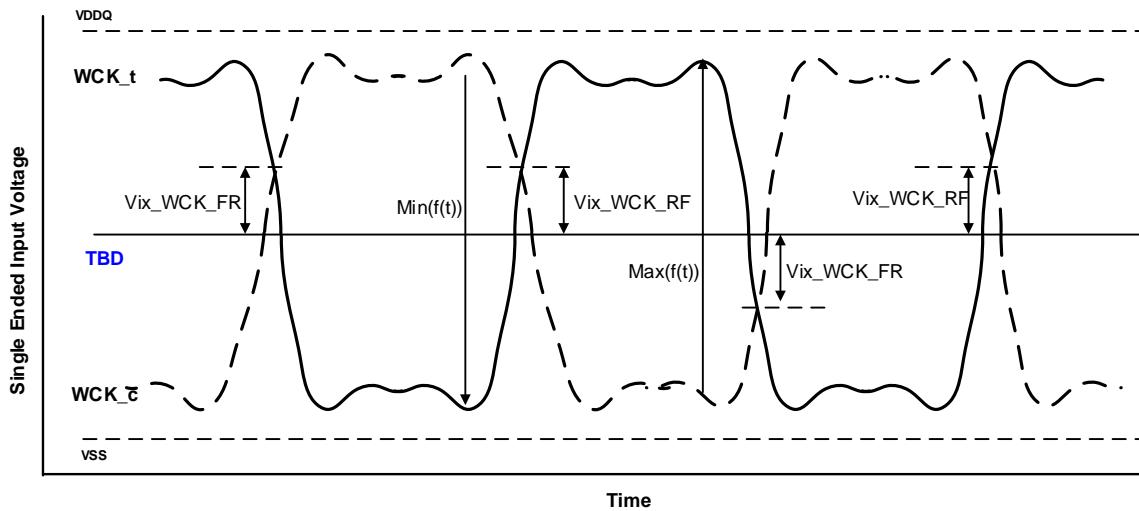
Table 322 — Differential Input Level for WCK t, WCK c

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		800		1066		1600		2133		2750		3200					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Differential Input High	VIHdiff_WCK	120	-	120	-	120	-	100	-	TBD	-	TBD	-	mV			
Differential Input Low	VILdiff_WCK	-	120	-	120	-	120	-	100	-	TBD	-	TBD	mV			

Table 323 — Differential Input Slew Rate for WCK t, WCK c

12.2.2.4 Differential Input Cross Point Voltage for WCK

The cross point voltage of differential input signals (WCK_t, WCK_c) must meet the requirements in Table 322. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is TBD.



NOTE 1 The base level of Vix_WCK_FR/RF is TBD that is LPDDR5 SDRAM internal setting value by Vref training.

Figure 203 — Vix Definition (WCK)

Table 324 — Cross point voltage for differential input signals (WCK)

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		800		1066		1600		2133		2750		3200					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential input crosspoint voltage ratio	Vix_WCK_ratio	-	20	-	20	-	20	-	20	-	20	-	20	%	1,2		

NOTE 1 Vix_WCK_Ratio is defined by this equation: $Vix_WCK_Ratio = Vix_WCK_FR / |Min(f(t))|$

NOTE 2 Vix_WCK_Ratio is defined by this equation: $Vix_WCK_Ratio = Vix_WCK_RF / Max(f(t))$

12.3 Output Slew Rate

12.3.1 Single Ended Output Slew Rate

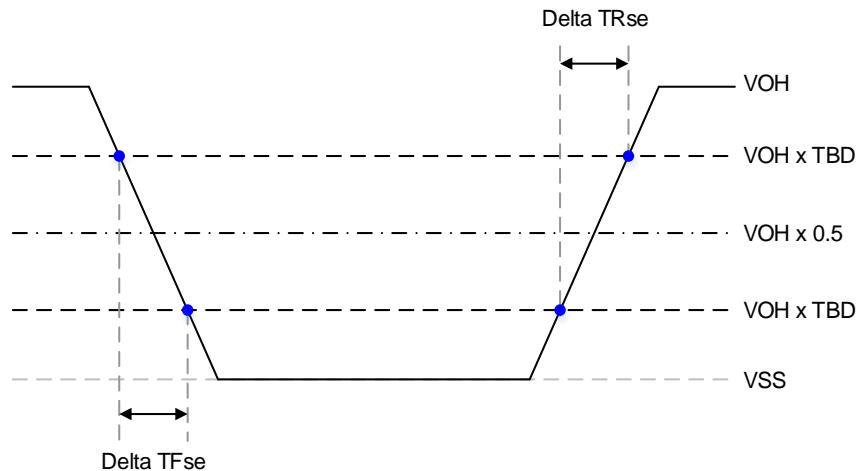


Figure 204 — Single Ended Output Slew Rate Definition

Table 325 — Output Slew Rate (single-ended)

Parameter	Symbol	Value		Units
		Min	Max	
Single-ended Output Slew Rate	SRQse*	TBD	TBD	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	TBD	TBD	-

* SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), and se: Single-ended Signals

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOH x TBD and VOH x TBR.

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

NOTE 5 The parameters about Single-ended applies to RDQS_t and RDQS_c when either RDQS_t or RDQS_c is disabled.

12.3.2 Differential Output Slew Rate

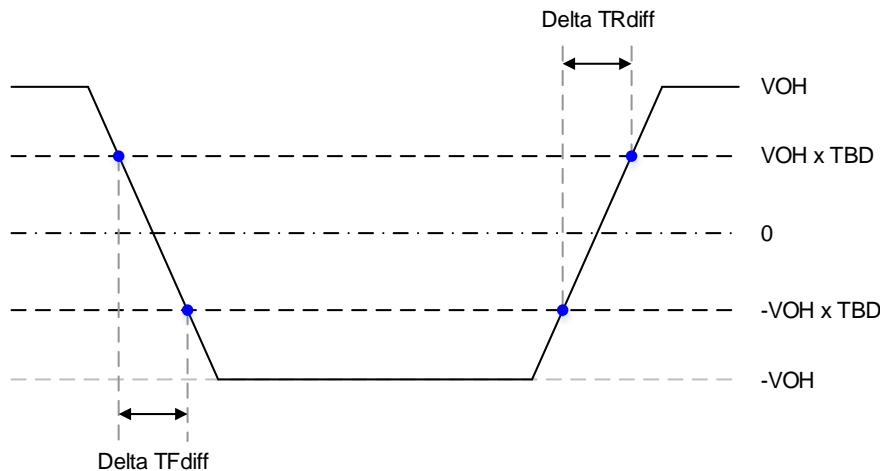


Figure 205 — Differential Output Slew Rate Definition

Table 326 — Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate	SRQdiff*	TBD	TBD	V/ns

* SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), and diff: Differential Signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between -VOH x TBD and VOH x TBD.

NOTE 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

12.4 Driver Output Timing Reference load

These "Timing Reference Loads" are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

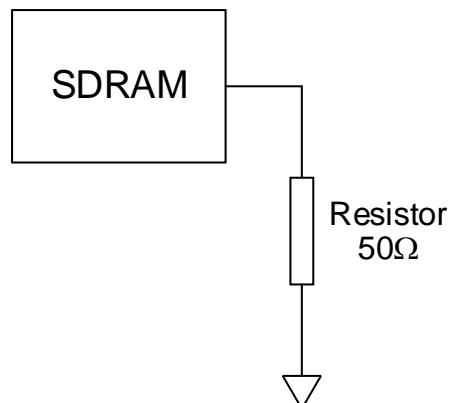


Figure 206 — Driver Output Reference Load for Timing and Slew Rate

12.5 Single Ended WCK

12.5.1 Single Ended WCK input definitions

The minimum input voltage need to satisfy both Vinse_WCK_SE_High and Vinse_WCK_SE_Low specification at input receiver and their measurement period is 1tWCK. Vinse_WCK_SE is the peak to peak voltage centered on VDDQ/2 and Vinse_WCK_SE_High and Vinse_WCK_SE_Low is max and min peak voltage from VDDQ/2.

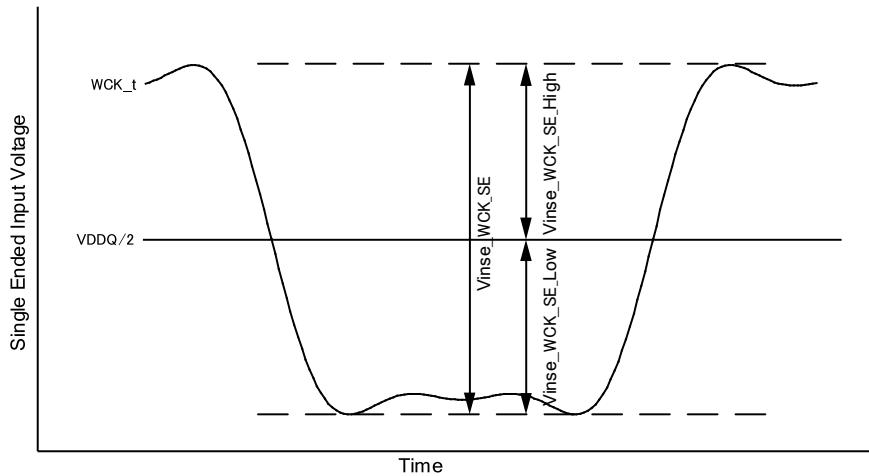


Figure 207 — Single Ended Mode WCK input Voltage

12.5.2 Single Ended Mode WCK Pulse Definitions

Single Ended Mode WCK pulse definitions are defined shown below.

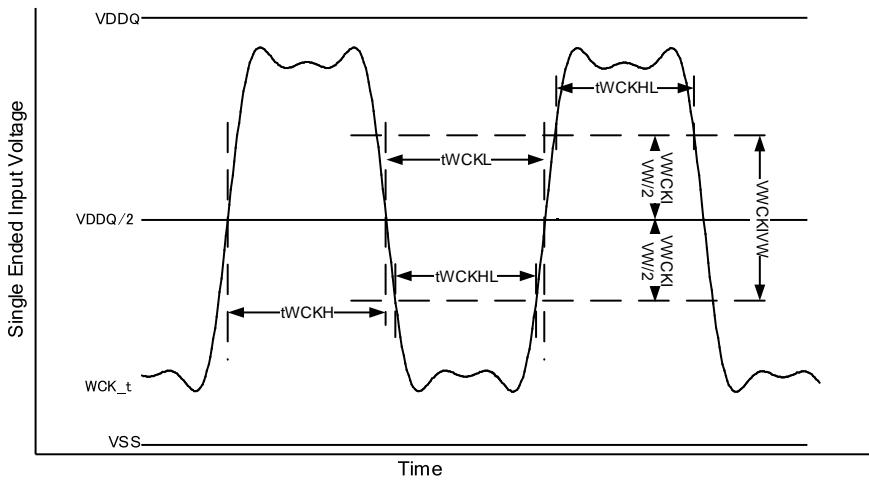


Figure 208 — Single Ended Mode WCK pulse

12.5.2 Single-Ended Mode WCK Pulse Definitions (Cont'd)

Table 327 — Single Ended WCK parameters

Parameter	Symbol	Min/Max	WCK Frequency	Unit	Note
			800MHz		
WCK Single ended input voltage	Vinse_WCK_SE	Min	220	mV	
WCK Single Ended Input Voltage High	Vinse_WCK_SE_High	Min	110	mV	
WCK Single Ended Input Voltage Low	Vinse_WCK_SE_low	Min	110	mV	
WCK single ended timing window	VWCKIVW	Min	180	mV	
Clock Single Ended WCK Pulse	tWCKHL	Min	0.23	tWCK (avg)	
WCK single ended Slew Rate	SRIWCKSE	Min	1	V/ns	1
		Max	7		

NOTE 1 Single ended slew rate is measured at VDDQ/2 - VWCKIVW/2 and VDDQ/2 + VWCKIVW/2

12.6 Single Ended CK

12.6.1 Single Ended CK input definitions

The minimum input voltage need to satisfy both Vinse_CK_SE_High and Vinse_CK_SE_Low specification at input receiver and their measurement period is 1tCK. Vinse_CK_SE is the peak to peak voltage centered on VDDQ/2 and Vinse_CK_SE_High and Vinse_CK_SE_Low is max and min peak voltage from VDDQ/2.

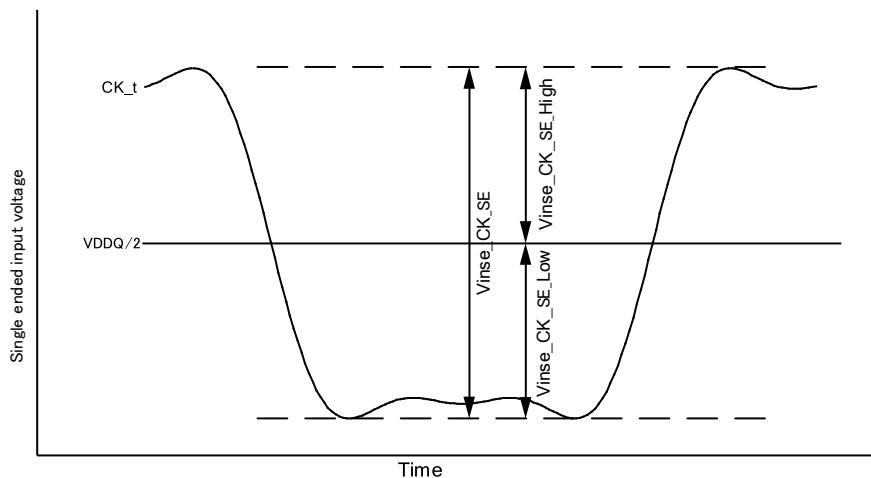


Figure 209 — Single Ended Mode CK input Voltage

12.6.2 Single Ended Mode CK Pulse Definitions

Single Ended Mode CK pulse definitions are defined as shown in Table 328.

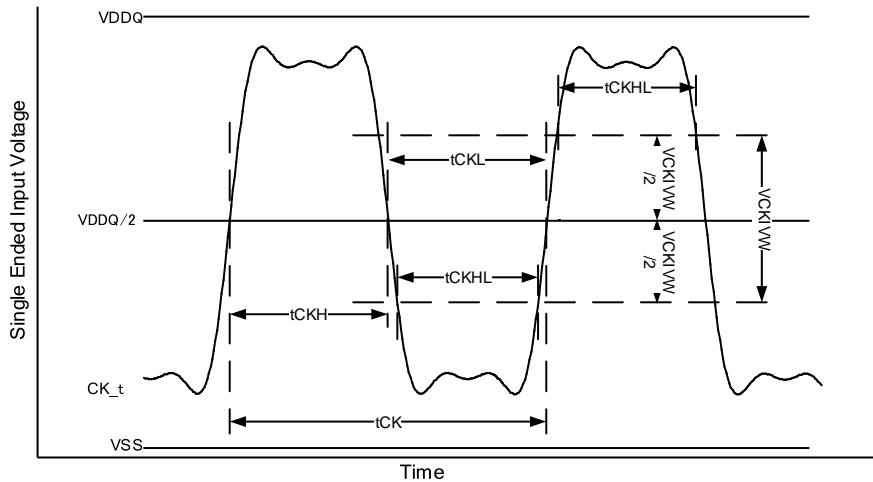


Figure 210 — Single Ended Mode CK pulse

Table 328 — Single Ended CK parameters

Parameter	Symbol	Min/Max	CK Frequency	Unit	Note
			400MHz		
CK Single ended input voltage	Vinse_CK_SE	Min	220	mV	
CK Single Ended Input Voltage High	Vinse_CK_SE_High	Min	110	mV	
CK Single Ended Input Voltage Low	Vinse_CK_SE_low	Min	110	mV	
CK single ended timing window	VCKIVW	min	190	mV	
Clock Single Ended CK Pulse	tCKHL	Min	0.26	tCK(avg)	
CK single ended Slew Rate	SRICKSE	Min	1	V/ns	1
		Max	7		

NOTE 1 Single ended slew rate is measured at $VDDQ/2 - VCKIVW/2$ and $VDDQ/2 + VCKIVW/2$.

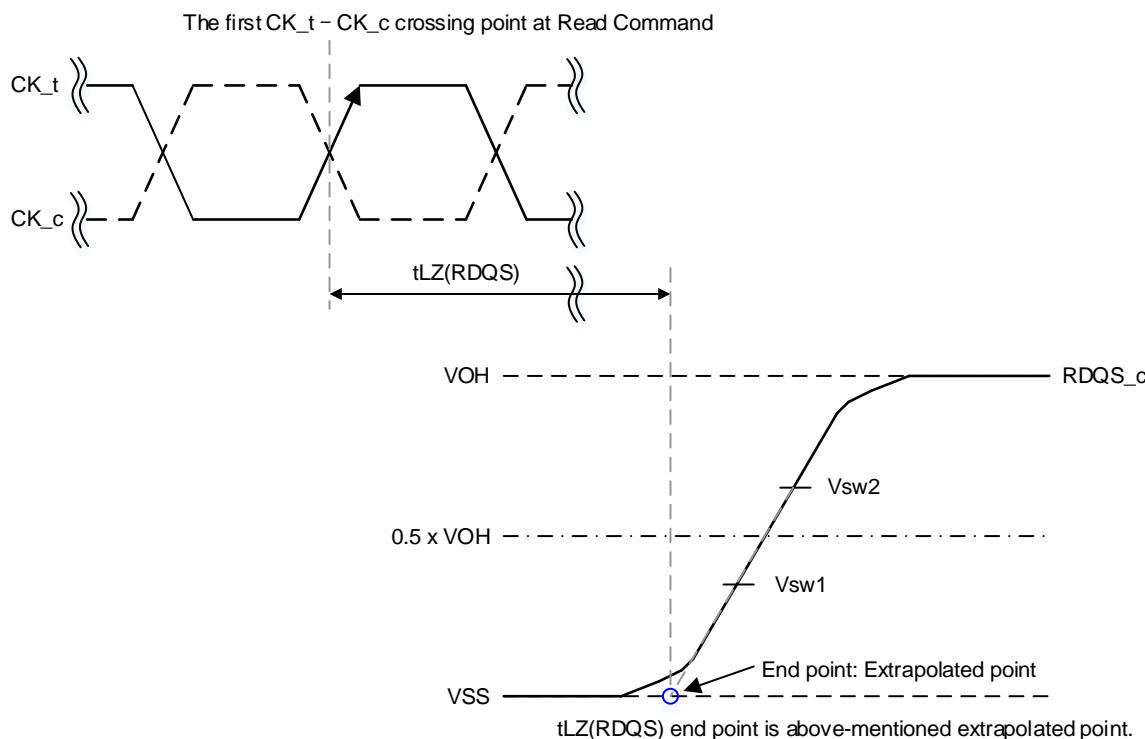
12.7 Read Timing tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

12.7.1 tLZ(RDQS) tLZ(DQ) tHZ(RDQS) tHZ(DQ)

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to voltage levels that indicate when the device output is no longer driving tHZ(RDQS) and tHZ(DQ), or begins driving tLZ(RDQS), tLZ(DQ).

This section includes a method to calculate the point when the device is no longer driving tHZ(RDQS) and tHZ(DQ), or begins driving tLZ(RDQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(RDQS), tLZ(DQ), tHZ(RDQS), and tHZ(DQ) are defined as single ended.

12.7.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment)



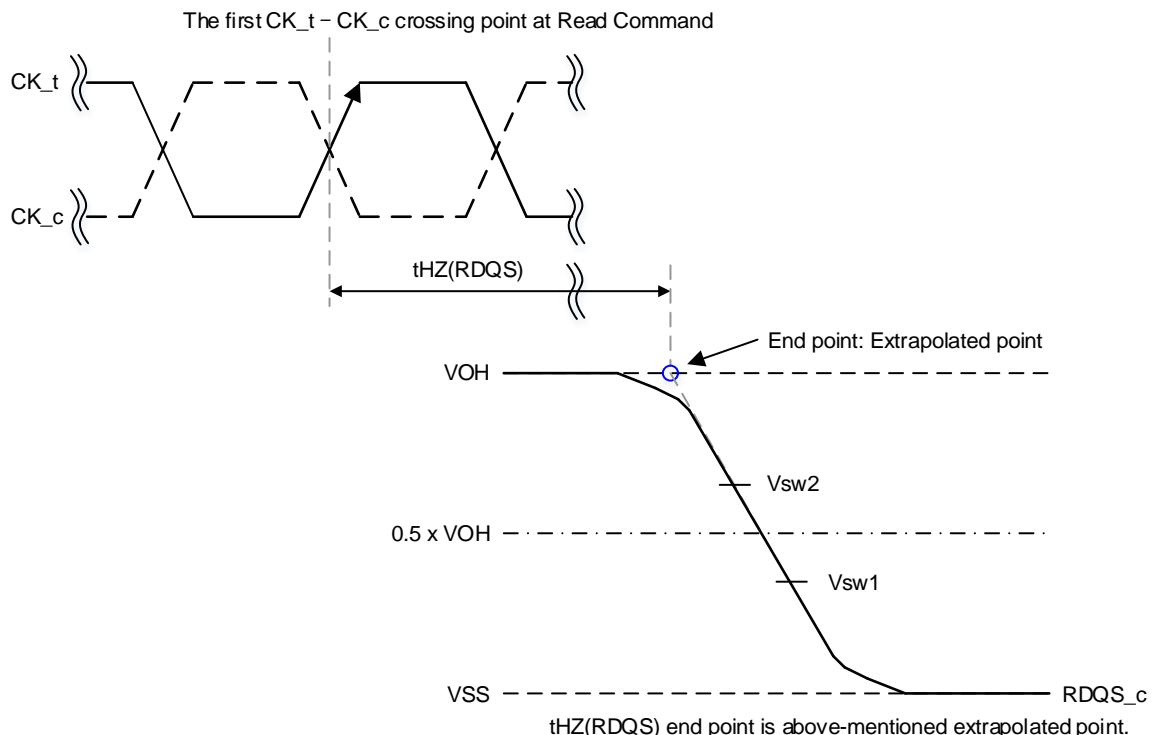
NOTE 1 Conditions for Calibration: $VDDQ = 0.5$ V, Pull Down Driver $Ron = 40\text{ohm}$, $VOH = VDDQ/2$

NOTE 2 Termination condition for $RDQS_t$ and $RDQS_c = 50\text{ohm}$ to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

Figure 211 — tLZ(RDQS) method for calculating transitions and end point

12.7.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment) (Cont'd)



NOTE 1 Conditions for Calibration: VDDQ = 0.5 V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

NOTE 2 Termination condition for RDQS_t and RDQS_c = 50ohm to VSS.

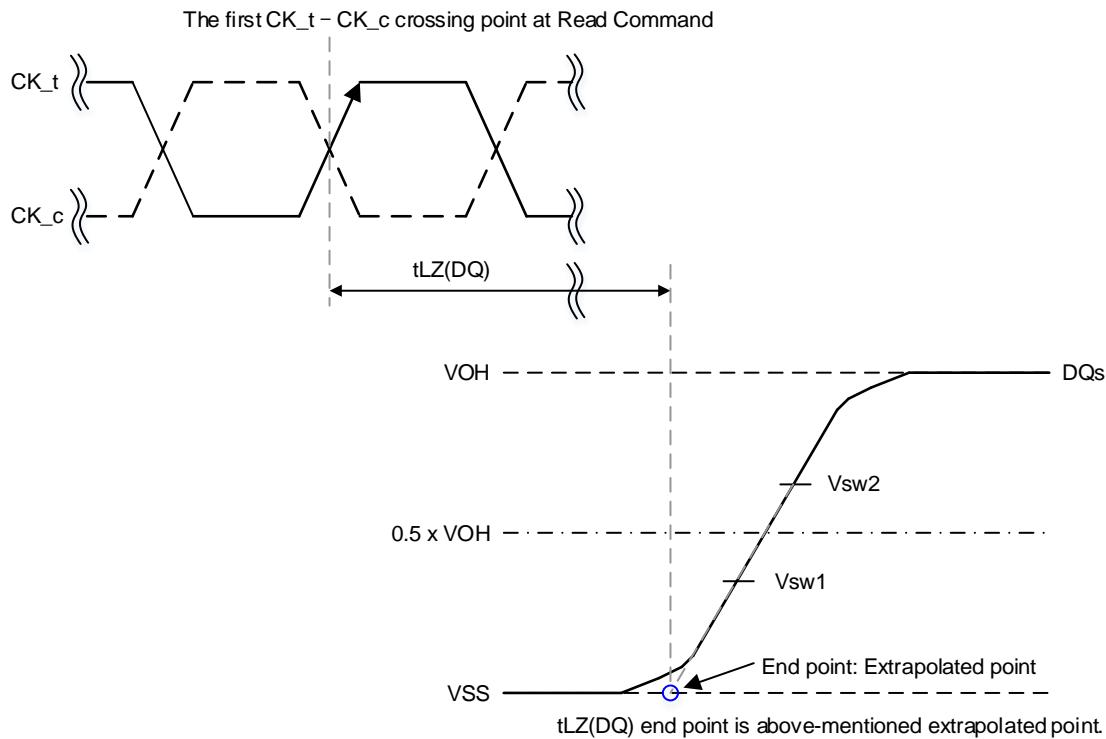
NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

Figure 212 — tHZ(RDQS) method for calculating transitions and end point

Table 329 — Reference Voltage for tLZ(RDQS), tHZ(RDQS) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Notes
RDQS_c low-impedance time from CK_t, CK_c	tLZ(RDQS)	0.4 x VOH	0.6 x VOH	
RDQS_c high impedance time from CK_t, CK_c	tHZ(RDQS)	0.4 x VOH	0.6 x VOH	

12.7.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)



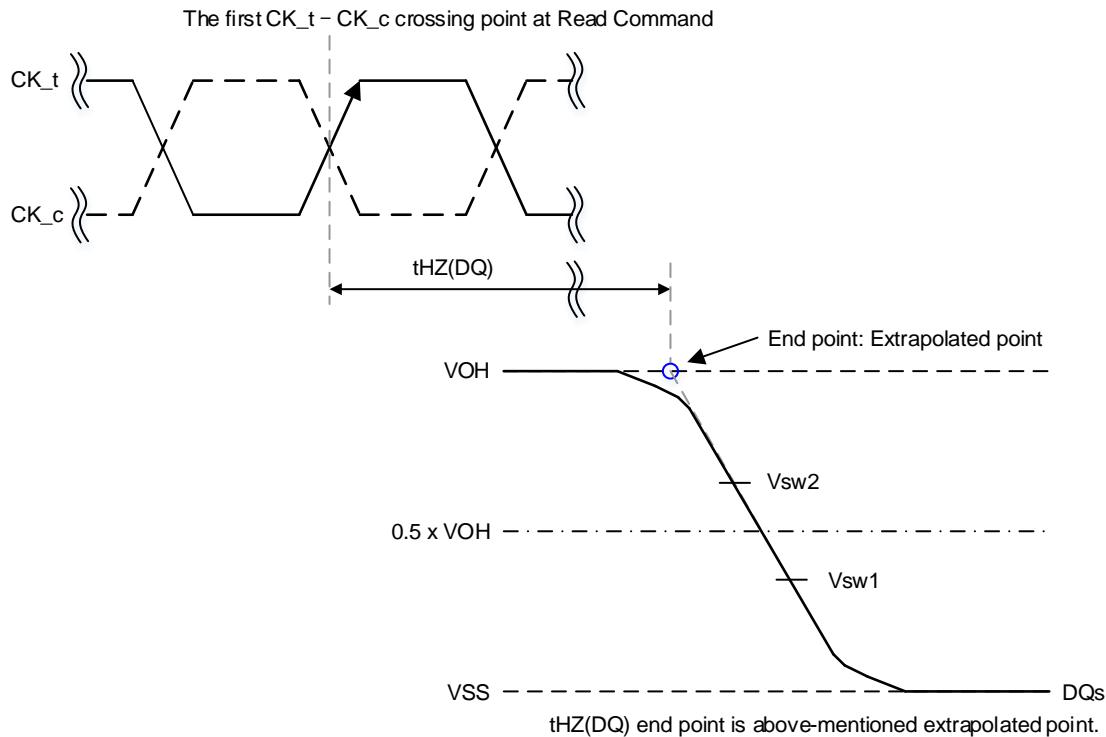
NOTE 1 Conditions for Calibration: $VDDQ = 0.5$ V, Pull Down Driver $Ron = 40\text{ohm}$, $VOH = VDDQ/2$

NOTE 2 Termination condition for DQs and DMI = 50ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

Figure 213 — tLZ(DQ) method for calculating transitions and end point

12.7.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) (Cont'd)



NOTE 1 Conditions for Calibration: $VDDQ = 0.5$ V, Pull Down Driver $Ron = 40\text{ohm}$, $VOH = VDDQ/2$

NOTE 2 Termination condition for DQs and DMI = 50ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

Figure 214 — tHZ(DQ) method for calculating transitions and end point

Table 330 — Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements

Measured Parameter	Measured Parameter Symbol	$V_{sw1}[\text{V}]$	$V_{sw2}[\text{V}]$	Notes
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	$0.4 \times VOH$	$0.6 \times VOH$	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	$0.4 \times VOH$	$0.6 \times VOH$	

12.7.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) (Cont'd)

Table 331 — Read AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Notes
			Up to 6400Mbps		
READ preamble	tRPRE	Min	TBD	tCK(avg)	
READ postamble	tRPST	Min	TBD	tCK(avg)	
RDQS_c low-impedance time from CK_t, CK_c	tLZ(RDQS)	Min	(RL x tCK) + tWCK2CK(Min) + tWCK2DQO(Min) -(tRPRE(Max) x tCK) - TBDps	ps	
RDQS_c high impedance time from CK_t, CK_c	tHZ(RDQS)	Max	(RL x tCK) + tWCK2CK(Max) + BL_n_min + (RPST(Max) x tCK) - TBDps	ps	
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	Min	(RL x tCK + tWCK2CK(Min) + tDQSQ(Min) - TBDps	ps	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	Max	(RL x tCK) + tWCK2CK(Max) + tWCK2DQO(Max) + BL_n_min - TBDps	ps	

13 Input / Output Capacitance

Table 332 — Input / Output Capacitance

Parameter	Symbol		LPDDR5 3200-533	LPDDR5 4266-3733	LPDDR5 5500-4800	LPDDR5 6400	Units	Notes
Input Capacitance, CK_t and CK_c	CCK	Min	0.5	0.5	0.5	0.5	pF	1,2
		Max	1.1	1.1	1.1	1.1	pF	1,2
Input Capacitance delta, CK_t and CK_c	CDCK	Min	0.0	0.0	0.0	0.0	pF	1,2,3
		Max	0.09	0.09	0.09	0.09	pF	1,2,3
Input Capacitance, WCK_t and WCK_c	CWCK	Min	0.5	0.5	0.5	0.5	pF	1,2
		Max	TBD	TBD	TBD	TBD	pF	1,2
Input Capacitance delta, WCK_t and WCK_c	CDWCK	Min	0.0	0.0	0.0	0.0	pF	1,2,4
		Max	0.09	0.09	0.09	0.09	pF	1,2,4
Input Capacitance, All other input-only pins	CI	Min	0.5	0.5	0.5	0.5	pF	1,2,5
		Max	1.1	1.1	1.1	1.1	pF	1,2,5
Input Capacitance delta, All other input-only pins	CDI	Min	-0.1	-0.1	-0.1	-0.1	pF	1,2,6
		Max	0.1	0.1	0.1	0.1	pF	1,2,6
Input/output Capacitance, DQ and DMI	CIO	Min	0.5	0.5	0.5	0.5	pF	1,2,7
		Max	TBD	TBD	TBD	TBD	pF	1,2,7
Input/output Capacitance delta, DQ and DMI	CDIO	Min	-0.1	-0.1	-0.1	-0.1	pF	1,2
		Max	0.1	0.1	0.1	0.1	pF	1,2
Output Capacitance, RDQS_t and RDQS_c	COO	Min	0.5	0.5	0.5	0.5	pF	1,2
		Max	TBD	TBD	TBD	TBD	pF	1,2
Output Capacitance delta, RDQS_t and RDQS_c	CDOO	Min	0.0	0.0	0.0	0.0	pF	1,2,8
		Max	0.1	0.1	0.1	0.1	pF	1,2,8
Input/output capacitance, ZQ pin	CZQ	Min	0.0	0.0	0.0	0.0	pF	1,2
		Max	5.0	5.0	5.0	5.0	pF	1,2

NOTE 1 This parameter applies to die device, including IO capacitance, RDL if needed (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA)) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.

NOTE 3 Absolute value of CCK_t . CCK_c.

NOTE 4 Absolute value of CWCK_t . CWCK_c.

NOTE 5 CI applies to CS, CA0~CA6.

NOTE 6 CDI = CI . 0.5 * (CCK_t + CCK_c)

NOTE 7 DMI loading matches DQ.

NOTE 8 Absolute value of CRDQS_t . CRDQS_c.

14 IDD Specification Parameters and Test Conditions

14.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(DC)} \text{ MAX}$
- HIGH: $V_{IN} \geq V_{IH(DC)} \text{ MIN}$
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See Tables 333 through 339

Table 333 — Definition of Switching for CA Input Signals

CK_t edge	R1	F1	R2	F2	R3	F3	R4	F4	R5	F5	R6	F6	R7	F7	R8	F8
CS	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
CA0	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	H	H	H	H	L	L	L	L	L	H
CA2	H	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
CA3	H	H	H	L	L	L	H	H	H	H	L	L	L	L	L	H
CA4	H	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
CA5	H	H	H	L	L	L	H	H	H	H	L	L	L	L	L	H
CA6	H	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H

NOTE 1 CS must always be driven LOW.

NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

NOTE 3 The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table 334 — CA Pattern for IDD4R @ BG mode

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	High	Read	H	L	L	L	L	L	L	1
F0	Low		L	H	H	L	L	L	L	
R1	High	DES	L	L	L	L	L	L	L	
F1	Low		L	L	L	L	L	L	L	
R2	High	Read	H	L	L	L	L	L	L	2
F2	Low		L	H	L	H	L	L	L	
R3	Low	CAS (B3)	L	L	H	H	L	L	L	
F3	Low		L	L	L	L	L	L	H	
R4	High	Read	H	L	L	H	H	H	H	3
F4	Low		L	H	H	L	H	H	L	
R5	High	CAS (B3)	L	L	H	H	L	L	L	
F5	Low		L	L	L	L	L	L	H	
R6	High	Read	H	L	L	H	H	H	H	4
F6	Low		L	H	L	H	H	H	L	
R7	Low	DES	L	L	L	L	L	L	L	
F7	Low		L	L	L	L	L	L	L	

NOTE 1 Pattern A is applied to DQs.

NOTE 2 Pattern B is applied to DQs.

NOTE 3 Pattern A' is applied to DQs.

NOTE 4 Pattern B' is applied to DQs.

NOTE 5 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is BG mode.

14.1 IDD Measurement Conditions (Cont'd)

Table 335 — CA Pattern for IDD4R @ 16B mode

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	High	Read	H	L	L	L	L	L	L	1
F0	Low		L	H	H	L	L	L	L	
R1	High	CAS (B3)	L	L	H	H	L	L	L	
F1	Low		L	L	L	L	L	L	H	
R2	High	Read	H	L	L	H	H	H	H	2
F2	Low		L	H	H	L	H	H	L	
R3	Low	DES	L	L	L	L	L	L	L	
F3	Low		L	L	L	L	L	L	L	

NOTE 1 Pattern A is applied to DQs.

NOTE 2 Pattern B is applied to DQs.

NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 16B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD.

Table 336 — CA Pattern for IDD4R @ 8B mode

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	High	Read	H	L	L	L	L	L	L	1
F0	Low		L	H	H	L	L	L	L	
R1	Low	DES	L	L	L	L	L	L	L	
F1	Low		L	L	L	L	L	L	L	
R2	Low	DES	L	L	L	L	L	L	L	2
F2	Low		L	L	L	L	L	L	L	
R3	High	CAS (B3)	L	L	H	H	L	L	L	
F3	Low		L	L	L	L	L	L	H	
R4	High	Read	H	L	L	H	H	H	H	3
F4	Low		L	H	H	L	H	H	L	
R5	Low	DES	L	L	L	L	L	L	L	
F5	Low		L	L	L	L	L	L	L	
R6	Low	DES	L	L	L	L	L	L	L	4
F6	Low		L	L	L	L	L	L	L	
R7	Low	DES	L	L	L	L	L	L	L	
F7	Low		L	L	L	L	L	L	L	

NOTE 1 Pattern A is applied to DQs.

NOTE 2 Pattern B is applied to DQs.

NOTE 3 Pattern CA' is applied to DQs.

NOTE 4 Pattern DB' is applied to DQs.

NOTE 5 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 8B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD.

14.1 IDD Measurement Conditions (Cont'd)

Table 337 — CA Pattern for IDD4W@ BG mode

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	High	WRITE	L	H	H	L	L	L	L	1
F0	Low		L	H	H	L	L	L	L	
R1	Low	DES	L	L	L	L	L	L	L	
F1	Low		L	L	L	L	L	L	L	
R2	High	WRITE	L	H	H	L	L	L	L	2
F2	Low		L	H	L	H	L	L	L	
R3	Low	DES	L	L	L	L	L	L	L	
F3	Low		L	L	L	L	L	L	L	
R4	High	WRITE	L	H	H	H	H	H	H	1
F4	Low		L	H	H	L	H	H	L	
R5	Low	DES	L	L	L	L	L	L	L	
F5	Low		L	L	L	L	L	L	L	
R6	High	WRITE	L	H	H	H	H	H	H	2
F6	Low		L	H	L	H	H	H	L	
R7	Low	DES	L	L	L	L	L	L	L	
F7	Low		L	L	L	L	L	L	L	

NOTE 1 Pattern A is applied to DQs.

NOTE 2 Pattern B is applied to DQs.

NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is BG mode.

Table 338 — CA Pattern for IDD4W @ 16B mode

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	High	WRITE	L	H	H	L	L	L	L	1
F0	Low		L	H	H	L	L	L	L	
R1	Low	DES	L	L	L	L	L	L	L	
F1	Low		L	L	L	L	L	L	L	
R2	High	WRITE	L	H	H	H	H	H	H	2
F2	Low		L	H	H	L	H	H	L	
R3	Low	DES	L	L	L	L	L	L	L	
F3	Low		L	L	L	L	L	L	L	

NOTE 1 Pattern A is applied to DQs.

NOTE 2 Pattern B is applied to DQs.

NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 16B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD.

14.1 IDD Measurement Conditions (Cont'd)

Table 339 — CA Pattern for IDD4W@ 8B mode

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	High	WRITE	L	H	H	L	L	L	L	1
F0	Low		L	H	H	L	L	L	L	
R1	Low	DES	L	L	L	L	L	L	L	
F1	Low		L	L	L	L	L	L	L	
R2	Low	DES	L	L	L	L	L	L	L	2
F2	Low		L	L	L	L	L	L	L	
R3	Low	DES	L	L	L	L	L	L	L	
F3	Low		L	L	L	L	L	L	L	
R4	High	WRITE	L	H	H	H	H	H	H	1
F4	Low		L	H	H	L	H	H	L	
R5	Low	DES	L	L	L	L	L	L	L	
F5	Low		L	L	L	L	L	L	L	
R6	Low	DES	L	L	L	L	L	L	L	2
F6	Low		L	L	L	L	L	L	L	
R7	Low	DES	L	L	L	L	L	L	L	
F7	Low		L	L	L	L	L	L	L	

NOTE 1 Pattern A is applied to DQs.

NOTE 2 Pattern B is applied to DQs.

NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 8B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD.

14.1 IDD Measurement Conditions (Cont'd)

Table 340 — Data Pattern for IDD4R @ DBI Off

Type	BL	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1's
Pattern A	BL0	1	1	1	1	1	1	1	1	0	8
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	0	0	0	6
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	1	1	1	1	1	1	1	1	0	8
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	0	0	0	6
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B	BL0	1	1	1	1	1	1	0	0	0	6
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	1	1	0	2
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	0	0	0	0
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	1	1	0	8
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	1	1	0	2
	BL9	0	0	0	0	1	1	1	1	0	4
	BL10	1	1	1	1	1	1	0	0	0	6
	BL11	1	1	1	1	0	0	0	0	0	4
	BL12	1	1	1	1	1	1	1	1	0	8
	BL13	1	1	1	1	0	0	0	0	0	4
	BL14	0	0	0	0	0	0	0	0	0	0
	BL15	0	0	0	0	1	1	1	1	0	4

14.1 IDD Measurement Conditions (Cont'd)

Table 340 — Data Pattern for IDD4R @ DBI Off (Cont'd)

Type	BL	DQs – IDD4R DBI OFF									# of 1's
		DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
Pattern A'	BL0	1	1	1	1	1	1	1	1	0	8
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	0	0	0	6
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	1	1	1	1	1	1	1	1	0	8
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	0	0	0	6
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B'	BL0	0	0	0	0	0	0	1	1	0	2
	BL1	0	0	0	0	1	1	1	1	0	4
	BL2	1	1	1	1	1	1	0	0	0	6
	BL3	1	1	1	1	0	0	0	0	0	4
	BL4	1	1	1	1	1	1	1	1	0	8
	BL5	1	1	1	1	0	0	0	0	0	4
	BL6	0	0	0	0	0	0	0	0	0	0
	BL7	0	0	0	0	1	1	1	1	0	4
	BL8	1	1	1	1	1	1	0	0	0	6
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	1	1	0	2
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	0	0	0	0
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	1	1	0	8
	BL15	1	1	1	1	0	0	0	0	0	4
# of 1's		32	32	32	32	32	32	32	32	0	

NOTE 1 Pattern A' is defined by B3 ordering change based on pattern A.

NOTE 2 Pattern B' is defined by B3 ordering change based on pattern B.

14.1 IDD Measurement Conditions (Cont'd)

Table 341 — Data Pattern for IDD4W @ DBI Off

14.1 IDD Measurement Conditions (Cont'd)

Table 342 — Data Pattern for IDD4R @ DBI On

Type	BL	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1's
Pattern A	BL0	0	0	0	0	0	0	0	0	1	1
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	1	1	1	3
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	0	0	1	1
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	1	1	1	3
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B	BL0	0	0	0	0	0	0	1	1	1	3
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	1	1	0	2
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	0	0	0	0
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	0	0	1	1
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	1	1	0	2
	BL9	0	0	0	0	1	1	1	1	0	4
	BL10	0	0	0	0	0	0	1	1	1	3
	BL11	1	1	1	1	0	0	0	0	0	4
	BL12	0	0	0	0	0	0	0	0	1	1
	BL13	1	1	1	1	0	0	0	0	0	4
	BL14	0	0	0	0	0	0	0	0	0	0
	BL15	0	0	0	0	1	1	1	1	0	4

14.1 IDD Measurement Conditions (Cont'd)

Table 342 — Data Pattern for IDD4R @ DBI Off (Cont'd)

Type	BL	DQs – IDD4R DBI ON									# of 1's
		DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
Pattern A'	BL0	0	0	0	0	0	0	0	0	1	1
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	1	1	1	3
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	0	0	1	1
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	1	1	1	3
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B'	BL0	0	0	0	0	0	0	1	1	0	2
	BL1	0	0	0	0	1	1	1	1	0	4
	BL2	0	0	0	0	0	0	1	1	1	3
	BL3	1	1	1	1	0	0	0	0	0	4
	BL4	0	0	0	0	0	0	0	0	1	1
	BL5	1	1	1	1	0	0	0	0	0	4
	BL6	0	0	0	0	0	0	0	0	0	0
	BL7	0	0	0	0	1	1	1	1	0	4
	BL8	0	0	0	0	0	0	1	1	1	3
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	1	1	0	2
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	0	0	0	0
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	0	0	1	1
	BL15	1	1	1	1	0	0	0	0	0	4
# of 1's		16	16	16	16	16	16	32	32	16	

NOTE 1 Pattern A' is defined by B3 ordering change based on pattern A.

NOTE 2 Pattern B' is defined by B3 ordering change based on pattern B.

14.1 IDD Measurement Conditions (Cont'd)

Table 343 — Data Pattern for IDD4W @ DBI On

Type	BL	DQs – IDD4W DBI ON										# of 1's
		DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI		
Pattern A	BL0	0	0	0	0	0	0	0	0	1	1	
	BL1	1	1	1	1	0	0	0	0	0	4	
	BL2	0	0	0	0	0	0	0	0	0	0	
	BL3	0	0	0	0	1	1	1	1	0	4	
	BL4	0	0	0	0	0	0	1	1	0	2	
	BL5	0	0	0	0	1	1	1	1	0	4	
	BL6	0	0	0	0	0	0	1	1	1	3	
	BL7	1	1	1	1	0	0	0	0	0	4	
	BL8	0	0	0	0	0	0	0	0	1	1	
	BL9	1	1	1	1	0	0	0	0	0	4	
	BL10	0	0	0	0	0	0	0	0	0	0	
	BL11	0	0	0	0	1	1	1	1	0	4	
	BL12	0	0	0	0	0	0	1	1	0	2	
	BL13	0	0	0	0	1	1	1	1	0	4	
	BL14	0	0	0	0	0	0	1	1	1	3	
	BL15	1	1	1	1	0	0	0	0	0	4	
Pattern B	BL0	0	0	0	0	0	0	1	1	1	3	
	BL1	1	1	1	1	0	0	0	0	0	4	
	BL2	0	0	0	0	0	0	1	1	0	2	
	BL3	0	0	0	0	1	1	1	1	0	4	
	BL4	0	0	0	0	0	0	0	0	0	0	
	BL5	0	0	0	0	1	1	1	1	0	4	
	BL6	0	0	0	0	0	0	0	0	1	1	
	BL7	1	1	1	1	0	0	0	0	0	4	
	BL8	0	0	0	0	0	0	1	1	0	2	
	BL9	0	0	0	0	1	1	1	1	0	4	
	BL10	0	0	0	0	0	0	1	1	1	3	
	BL11	1	1	1	1	0	0	0	0	0	4	
	BL12	0	0	0	0	0	0	0	0	1	1	
	BL13	1	1	1	1	0	0	0	0	0	4	
	BL14	0	0	0	0	0	0	0	0	0	0	
	BL15	0	0	0	0	1	1	1	1	0	4	
# of 1's		8	8	8	8	8	8	16	16	8		

14.2 IDD Specifications

Table 344 — LPDDR5 IDD Specification Parameters and Operating Conditions

Parameter / Condition	Symbol	Power Supply	Note
Operating one bank active-Precharge current: tCK = tCKmin; tRC = tRCmin; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	IDD0 ₁	VDD1	9
	IDD0 _{2H}	VDD2H	9
	IDD0 _{2L}	VDD2L	9
	IDD0 _Q	VDD2Q	3
Idle power-down standby current: tCK = tCKmin; Power-down entry command is issued CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	IDD2P ₁	VDD1	
	IDD2P _{2H}	VDD2H	
	IDD2P _{2L}	VDD2L	
	IDD2P _Q	VDD2Q	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	IDD2PS ₁	VDD1	
	IDD2PS _{2H}	VDD2H	
	IDD2PS _{2L}	VDD2L	
	IDD2PS _Q	VDD2Q	3
Idle non power-down standby current: tCK = tCKmin; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	IDD2N ₁	VDD1	
	IDD2N _{2H}	VDD2H	
	IDD2N _{2L}	VDD2L	
	IDD2N _Q	VDD2Q	3
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	IDD2NS ₁	VDD1	
	IDD2NS _{2H}	VDD2H	
	IDD2NS _{2L}	VDD2L	
	IDD2NS _Q	VDD2Q	3
Active power-down standby current: tCK = tCKmin; CS is LOW; One bank is active; Power-down entry command is issued CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	IDD3P ₁	VDD1	9
	IDD3P _{2H}	VDD2H	9
	IDD3P _{2L}	VDD2L	9
	IDD3P _Q	VDD2Q	3

14.2 IDD Specifications (Cont'd)

Table 344 — Data Pattern for IDD4R @ DBI Off (Cont'd)

Parameter / Condition	Symbol	Power Supply	Note
Active power-down standby current with clock stop: Power-down entry command is issued CK_t=LOW, CK_c=HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD3PS ₁	VDD1	9
	IDD3PS _{2H}	VDD2H	9
	IDD3PS _{2L}	VDD2L	8, 9
	IDD3PS _Q	VDD2Q	4
Active non-power-down standby current: tCK = tCKmin; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD3N ₁	VDD1	9
	IDD3N _{2H}	VDD2H	9
	IDD3N _{2L}	VDD2L	8, 9
	IDD3N _Q	VDD2Q	4
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD3NS ₁	VDD1	9
	IDD3NS _{2H}	VDD2H	9
	IDD3NS _{2L}	VDD2L	8, 9
	IDD3NS _Q	VDD2Q	4
Operating burst READ current @ BG Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; One bank in each bank group 1 and 2 is active; BL = 16 or 32 ; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R ₁	VDD1	
	IDD4R _{2H}	VDD2H	
	IDD4R _{2L}	VDD2L	8
	IDD4R _Q	VDD2Q	5
Operating burst READ current @ 8/16Bank Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R ₁	VDD1	
	IDD4R _{2H}	VDD2H	
	IDD4R _{2L}	VDD2L	8
	IDD4R _Q	VDD2Q	5
Operating burst WRITE current @ BG Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; One bank in each bank group 1 and 2 is active; BL = 16 or 32 ; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer RDQS_t is stable (if Link ECC is enabled) ODT disabled	IDD4W ₁	VDD1	
	IDD4W _{2H}	VDD2H	
	IDD4W _{2L}	VDD2L	8
	IDD4W _Q	VDD2Q	4

14.2 IDD Specifications (Cont'd)

Table 344 — Data Pattern for IDD4R @ DBI Off (Cont'd)

Parameter / Condition	Symbol	Power Supply	Note
Operating burst WRITE current @ 8/16Bank Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; One banks is active; BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode ; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer RDQS_t is stable (if Link ECC is enabled) ODT disabled	IDD4W ₁	VDD1	
	IDD4W _{2H}	VDD2H	
	IDD4W _{2L}	VDD2L	8
	IDD4W _Q	VDD2Q	4
All-bank REFRESH Burst current: tCK = tCKmin; CS is LOW between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD5 ₁	VDD1	
	IDD5 _{2H}	VDD2H	
	IDD5 _{2L}	VDD2L	8
	IDD5 _Q	VDD2Q	4
All-bank REFRESH Average current: tCK = tCKmin; CS is LOW between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD5AB ₁	VDD1	
	IDD5AB _{2H}	VDD2H	
	IDD5AB _{2L}	VDD2L	8
	IDD5AB _Q	VDD2Q	4
Per-bank REFRESH Average current: tCK = tCKmin; CS is LOW between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD5PB ₁	VDD1	
	IDD5PB _{2H}	VDD2H	
	IDD5PB _{2L}	VDD2L	8
	IDD5PB _Q	VDD2Q	4
Power down Self refresh current: CK_t=LOW, CK_c=HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ($\leq 85^{\circ}$ C) Maximum TBDx Self-Refresh Rate; ($> 85^{\circ}$ C) RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD6 ₁	VDD1	6,7
	IDD6 _{2H}	VDD2H	6,7
	IDD6 _{2L}	VDD2L	6,7,8
	IDD6 _Q	VDD2Q	4,6,7,8

14.2 IDD Specifications (Cont'd)

Table 344 — Data Pattern for IDD4R @ DBI Off (Cont'd)

Parameter / Condition	Symbol	Power Supply	Note
Deep sleep mode current: CK_t=LOW, CK_c=HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ($\leq 85^{\circ}$ C) Maximum TBDx Self-Refresh Rate; ($> 85^{\circ}$ C) RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	IDD6 _{DS1}	VDD1	6,7,8
	IDD6 _{DS2H}	VDD2H	6,7
	IDD6 _{DS2L}	VDD2L	6,7,8
	IDD6 _{DSQ}	VDD2Q	4,6,7

- NOTE 1 Published IDD values are the maximum of the distribution of the arithmetic mean.
- NOTE 2 ODT disabled. MR11 OP[6:4] = 000_B
- NOTE 3 IDD current specifications are tested after the device is properly initialized.
- NOTE 4 Measured currents are the summation of VDDQ and VDD2H / VDD2L.
- NOTE 5 Guaranteed by design with output load = 5pF and RON = 40 ohm.
- NOTE 6 The 1x Self-Refresh Rate is the rate at which the LPDDR5 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
- NOTE 7 This is the general definition that applies to full array Self Refresh.
- NOTE 8 When MR13 OP[7] is high, single VDD2 rail, VDD2L Current shall be added to VDD2H Current.
- NOTE 9 IDD values can be different according to the bank organization set by MR3 OP[4:3].
- NOTE 10 When DVFS is enabled, the minimum tCK shall be set by following DVFS operating frequency.

15 Electrical Characteristics and AC Timing

15.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR5 device.

15.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(\text{avg}) = \left(\sum_{j=1}^N tCKj \right) / N$$

where $N = 200$

Unit "tCK(avg)" represents the actual clock average tCK(avg) of the input clock under operation.
Unit "nCK" represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

15.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

15.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(\text{avg}) = \left(\sum_{j=1}^N tCHj \right) / (N \times tCK(\text{avg}))$$

where $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(\text{avg}) = \left(\sum_{j=1}^N tCLj \right) / (N \times tCK(\text{avg}))$$

where $N = 200$

15.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

15.1.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

$t_{JIT}(per) = \text{Min/max of } \{t_{CKi} - t_{CK}(\text{avg}) \text{ where } i = 1 \text{ to } 200\}$.

tJIT(per),act is the actual clock jitter for a given system.

tJIT(per),allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

15.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT}(cc) = \text{Max of } \{|t_{CK}(i+1) - t_{CK}(i)|\}$.

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

15.1.7 Clock Timing

Table 345 — Clock AC Timings for 5/10/67/133MHz

Parameter	Symbol	5MHz		10MHz		67MHz		133MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	200	200	100	200	14.93	200	7.5	200	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-11200	1120 0	-5600	560 0	-840	840	-430	430	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	2240 0	-	112 00	-	168 0	-	860	ps	

15.1.7 Clock Timing (Cont'd)

Table 346 — Clock AC Timings for 200/267/344/400MHz

Parameter	Symbol	200MHz		267MHz		344MHz		400MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	5	200	3.75	200	2.9	200	2.5	200	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	ns							
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-280	280	-210	210	-170	170	-140	140	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	560	-	420	-	340	-	280	ps	

Table 347 — Clock AC Timings for 467/533/600/688

Parameter	Symbol	467MHz		533MHz		600MHz		688MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	2.15	200	1.875	200	1.667	200	1.453	200	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	ns							
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-120	120	-110	110	-95	95	-85	85	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	240	-	220	-	190	-	170	ps	

Table 348 — Clock AC Timings for 750/800MHz

Parameter	Symbol	750MHz		800MHz		Units	Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	1.333	200	1.25	200	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-75	75	-70	70	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	150	-	140	ps	

15.2 Write Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input write clocks violating the min/max values may result in malfunction of the LPDDR5 device.

15.2.1 Definition for tWCK(avg) and nWCK

tWCK(avg) is calculated as the average write clock period across any consecutive 200 cycle window, where each write clock period is calculated from rising edge to rising edge.

$$tWCK(\text{avg}) = \left(\sum_{j=1}^N tWCKj \right) / N$$

where $N = 200$

Unit "tWCK(avg)" represents the actual write clock average tWCK(avg) of the input write clock under operation. Unit "nWCK" represents one write clock cycle of the input write clock, counting the actual write clock edges. tWCK(avg) may change by up to +/-1% within a 100 write clock cycle window, provided that all jitter and timing specs are met.

15.2.2 Definition for tWCK(abs)

tWCK(abs) is defined as the absolute write clock period, as measured from one rising edge to the next consecutive rising edge.

tWCK(abs) is not subject to production test.

15.2.3 Definition for tWCH(avg) and tWCL(avg)

tWCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tWCH(\text{avg}) = \left(\sum_{j=1}^N tWCHj \right) / (N \times tWCK(\text{avg}))$$

where $N = 200$

tWCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tWCL(\text{avg}) = \left(\sum_{j=1}^N tWCLj \right) / (N \times tWCK(\text{avg}))$$

where $N = 200$

15.2.4 Definition for tWCH(abs) and tWCL(abs)

tWCH(abs) is the absolute instantaneous write clock high pulse width, as measured from one rising edge to the following falling edge.

tWCL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge.

Both tWCH(abs) and tWCL(abs) are not subject to production test.

15.2.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tWCK from tWCK(avg).

tJIT(per) = Min/max of {tWCKi - tWCK(avg) where i = 1 to 200}.

tJIT(per),act is the actual write clock jitter for a given system.

tJIT(per),allowed is the specified allowed write clock period jitter.

tJIT(per) is not subject to production test.

15.2.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in write clock period between two consecutive write clock cycles.

tJIT(cc) = Max of |{tWCK(i + 1) - tWCK(i)}|.

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

15.2.7 Definition for tERR(2per)

tERR(2per) is defined as the cumulative error across 2 consecutive cycles from tWCK(avg).

tERR(2per) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tWCKj \right) - n \times tWCK(avg)$$

where N = 2

15.2.8 Definition for tERR(3per)

tERR(3per) is defined as the cumulative error across 3 consecutive cycles from tWCK(avg).

tERR(3per) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tWCKj \right) - n \times tWCK(avg)$$

where N = 3

15.2.9 Definition for tERR(4per)

tERR(4per) is defined as the cumulative error across 4 consecutive cycles from tWCK(avg).
tERR(4per) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tWCKj \right) - n \times tWCK(avg)$$

where $N = 4$

15.2.10 Write Clock Timing

Table 349 — Write Clock AC Timings for 266/533/800/1067MHz

15.2.10 Write Clock Timing (Cont'd)

Table 350 — Write Clock AC Timings for 1375/1600/1867/2134MHz

Table 351 — Write Clock AC Timings for 2400/2750/3000/3200MHz

15.3 tWCK2DQ AC parameters

TBD

15.4 DQ Tx Jitter Spec

The DRAM DQ to RDQS differential jitter is defined to support both SOC matched and unmatched DQ-RDQS input receiver (Rx) types over NUI of mismatch. All output timings are referenced to RDQS for source synchronous timing relationship. The appropriate RDQS preamble mode must be selected in order to support the unmatched SOC Rx. It is the responsibility of the SOC and system to insure the advanced RDQS preambles edges are robust for system operation.

The N-UI DQ to RDQS output timing is defined as t_{QH_NUI} and t_{DQSQ_NUI} where N defines the number of UI RDQS is shifted from the corresponding DQ as shown in the figures below.

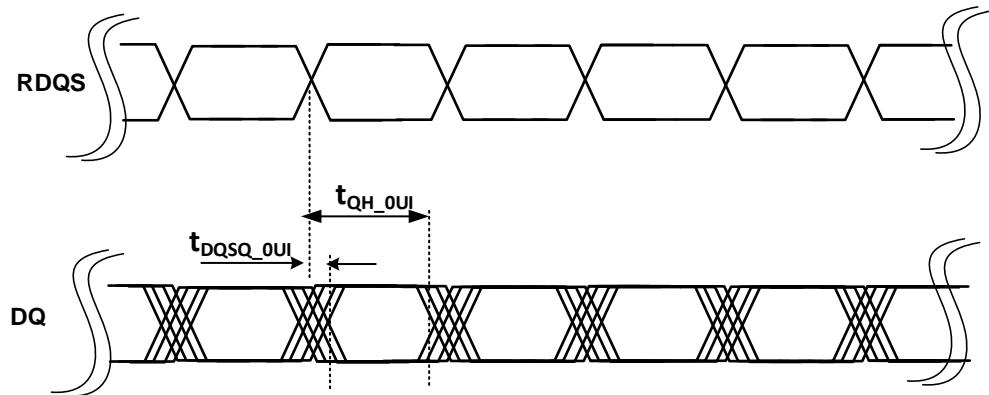


Figure 215 — DQ to RDQS 0UI read data timing example

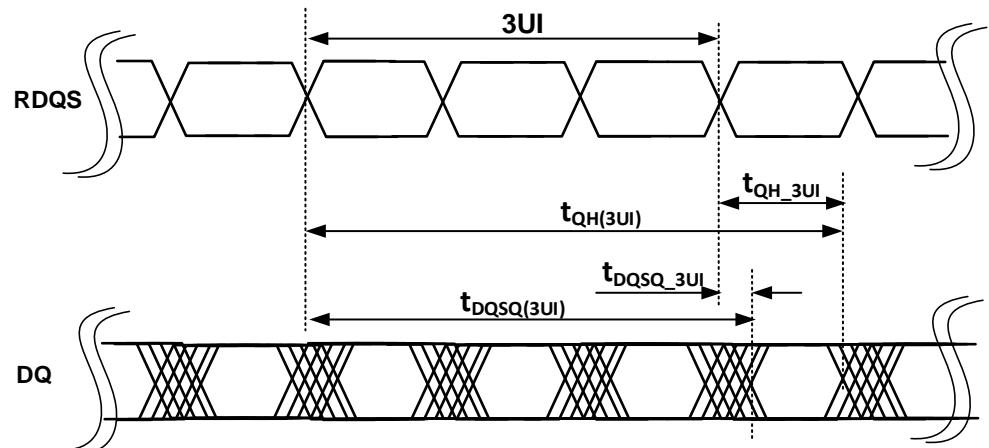


Figure 216 — DQ to RDQS 3UI read data timing example

The timing parameters t_{DQSQ_NUI} and t_{QH_NUI} are defined as follows:

$$t_{DQSQ_NUI} = t_{DQSQ(NUI)} - N \cdot UI$$

$$t_{QH_NUI} = t_{QH(NUI)} - N \cdot UI$$

N is the number of UI of RDQS to DQ mismatch UI is the average UI width.

15.4 DQ Tx Jitter Spec (Cont'd)

The figures below include examples of 0 and 3UI mismatch using the 4 tWCK RDQS read preamble of 2tWCK static + 2tWCK toggle.

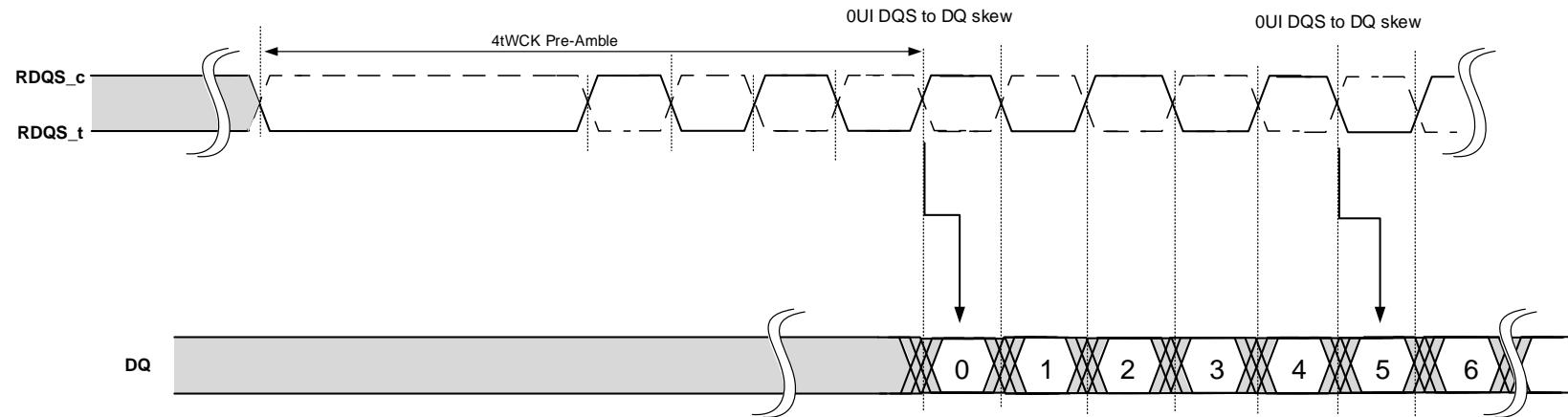


Figure 217 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 0 UI mismatch

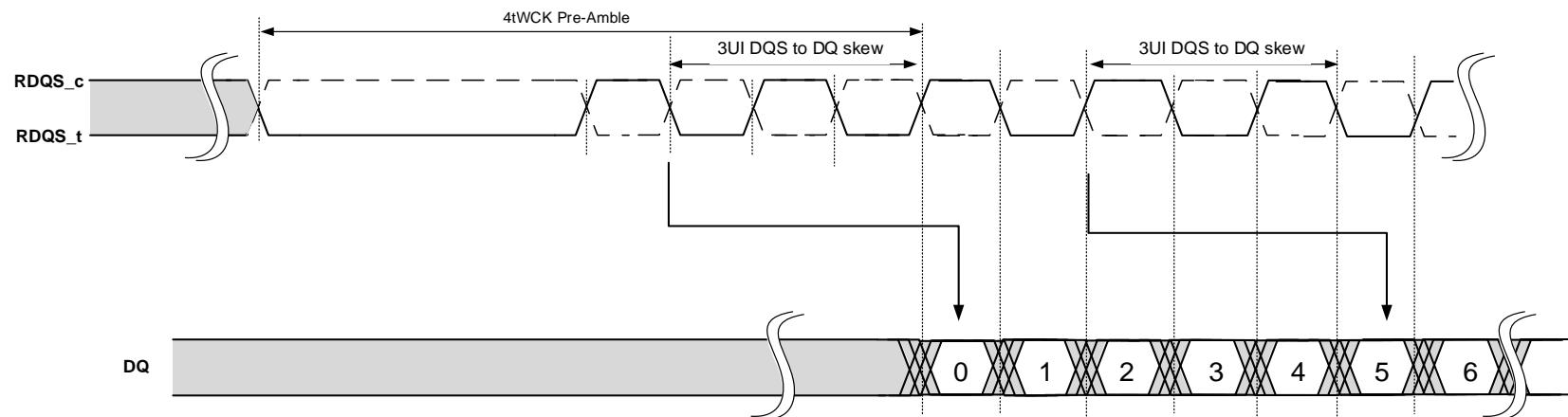


Figure 218 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 3UI mismatch

15.4 DQ Tx Jitter Spec (Cont'd)

Table 352 — DRAM DQ output timing

Symbol	Parameter	CK Freq- 67/133/200/267/344/400/467/533/600/688/750/800		Unit s	Note s
		Min	Max		
t_{DQSQ}	0UI RDQS_t, RDQS_c to DQ Skew per byte group	-	TBD	UI	1,2,3
t_{QH}	0UI RDQS_t, RDQS_c to DQ output hold time per byte group	TBD	-	UI	1,2,3
t_{DQSQ_1UI}	1UI RDQS_t, RDQS_c to DQ Skew per byte group	-	TBD	UI	1,2,3
t_{QH_1UI}	1UI RDQS_t, RDQS_c to DQ output hold time per byte group	TBD	-	UI	1,2,3
t_{DQSQ_2UI}	2UI RDQS_t, RDQS_c to DQ Skew per byte group	-	TBD	UI	1,2,3
t_{QH_2UI}	2UI RDQS_t, RDQS_c to DQ output hold time per byte group	TBD	-	UI	1,2,3
t_{DQSQ_3UI}	3UI RDQS_t, RDQS_c to DQ Skew per byte group	-	TBD	UI	1,2,3
t_{QH_3UI}	3UI RDQS_t, RDQS_c to DQ output hold time per byte group	TBD	-	UI	1,2,3

NOTE 1 These parameters are defined per pin over voltage and temperature.

NOTE 2 These parameters are a function of WCK input clock jitter(tbd).

NOTE 3 This parameter is calculated using the proper NUI mismatch. Equations below where N= Rx mismatch in UI, UI(avg)=avg UI:

a. $t_{DQSQ_NUI} = t_{DQSQ(NUI)} - N * UI(\text{avg})$

b. $t_{QH_NUI} = t_{QH(NUI)} - N * UI(\text{avg})$

15.5 CS Rx specification

LPDDR5 CS Rx is defined as two modes Asynchronous mode and Synchronous mode. Asynchronous mode Rx spec applies to during power down / deep sleep mode and exit from power down / deep sleep mode. Synchronous mode applies to other period than exit mode.

15.5.1 CS Rx mask and single pulse definition for Synchronous mode

LPDDR5 CS Rx mask for Synchronous mode is defined as hexagonal mask shape as shown in Figure 219. CS signals apply the same compliance mask and operate in single data rate mode. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.

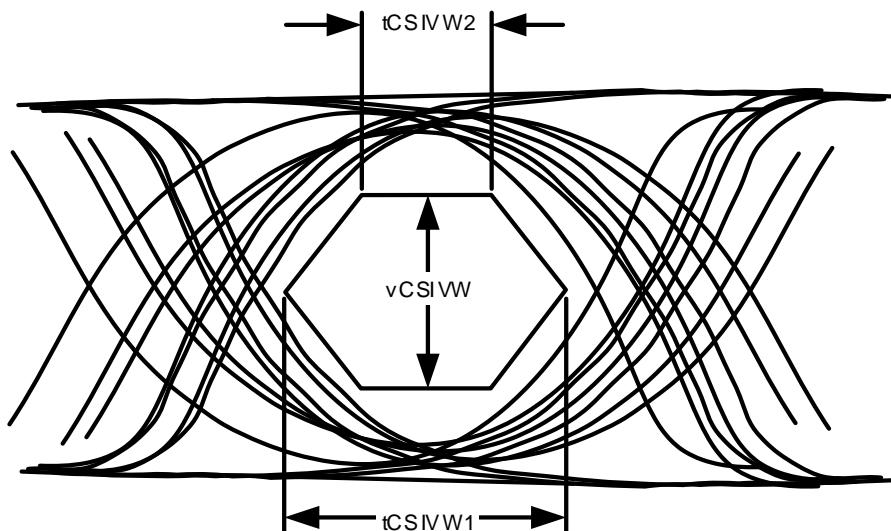
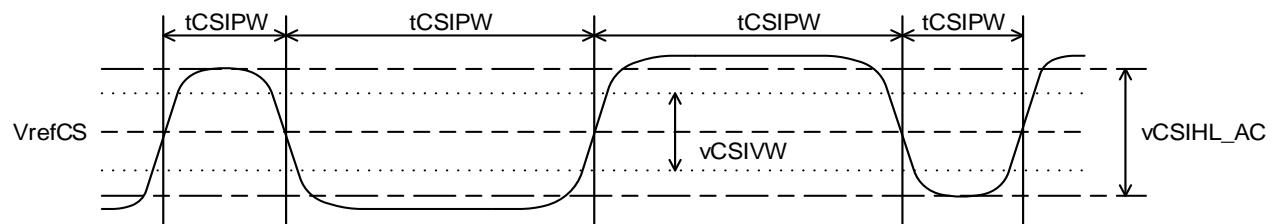


Figure 219 — Synchronous mode CS Rx Mask definition

LPDDR5 CS Rx single pulse definition as shown in Figure 220.



NOTE 1 Single pulse include any cycle of pulse.

Figure 220 — Synchronous mode CS Rx single pulse definition

15.5.1 CS Rx mask and single pulse definition for Synchronous mode (Cont'd)

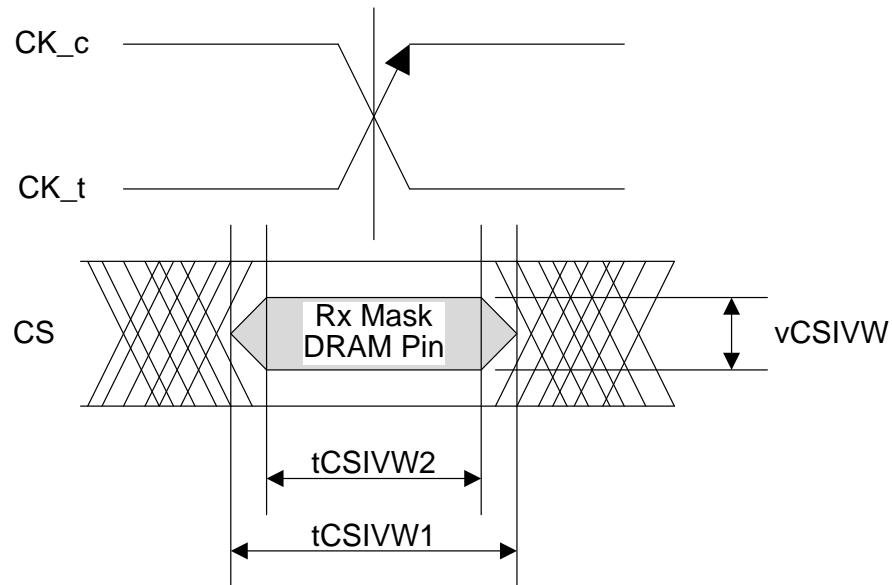


Figure 221 — Synchronous mode CS Timings at the DRAM Pin

Timing terms in Figure 221 are measured from CK_t/CK_c (differential mode) / CK (single end mode) to the center (midpoint) of the tCSIVW1 and tCSIVW2 window taken at midpoint and vCSIVW voltage levels.

15.5.2 CS Rx input level definition for Asynchronous mode

LPDDR5 CS Rx spec for power down mode is defined as shown in Figure 222. CS has to be lower than ViLPD to stay in power down mode or deep sleep mode. To exit from power down or deep sleep mode, CS has to satisfy ViHPD and power down / deep sleep timing specifications.

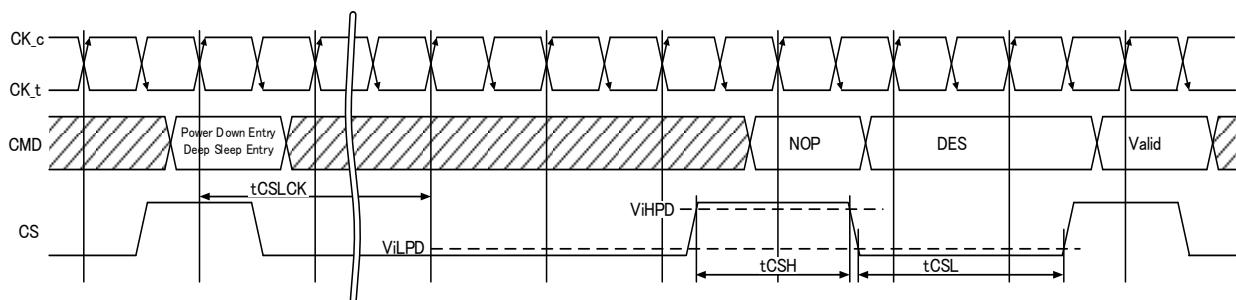


Figure 222 — Asynchronous mode ViHPD and ViLPD at Power Down Exit

15.5.3 Synchronous mode CS Rx mask / single pulse spec and Asynchronous mode CS input spec.

Table 353 — CS Rx Specification

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Note
			67	133	200	267	344	400	467	533	600	688	750	800		
Rx Mask																
CS Rx mask width at VrefCS	tCSIWV1	Min													UI	1
CS Rx mask width at vCSIWV	tCSIWV2	Min													UI	1
CS Rx mask height	vCSIWV	Min													mV	2
Rx Single pulse																
CS Rx pulse width	tCSIPW	Min													UI	
CS Rx pulse amplitude	vCSIHL_AC	Min													mV	3
CS reference voltage	Vref_CS														mV	
Power down																
CS VIL during Power down / Deep Sleep	ViLPD	Max													mV	4
CS VIH during Power down / Deep Sleep	ViHPD	Min													mV	5
		Max													V	5

NOTE 1 CS Rx mask voltage and timing parameters at the pin including temperature drift and voltage AC noise impact for frequencies > TBD MHz and max voltage of TBD mv pk-pk from DC-TBDMHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.

NOTE 2 CS single pulse signal amplitude into the receiver has to meet or exceed vCSIHL AC at any point over the total UI. No timing requirement above level. vCSIHL_AC is the peak to peak voltage centered around VrefCS such that vCSIHL_AC/2 min has to be met both above and below VrefCS.

NOTE 3 vCSIHL_AC does not have to be met when no transitions are occurring.

NOTE 4 The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.

NOTE 5 ViHPD is applied only for Power Down and Deep Sleep exit.

15.6 CA Rx specification

15.6.1 CA Rx mask and single pulse definition

LPDDR5 CA Rx mask is defined as hexagonal mask shape as shown in Figure 223. All CA signals apply the same compliance mask and operate in double data rate mode. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.

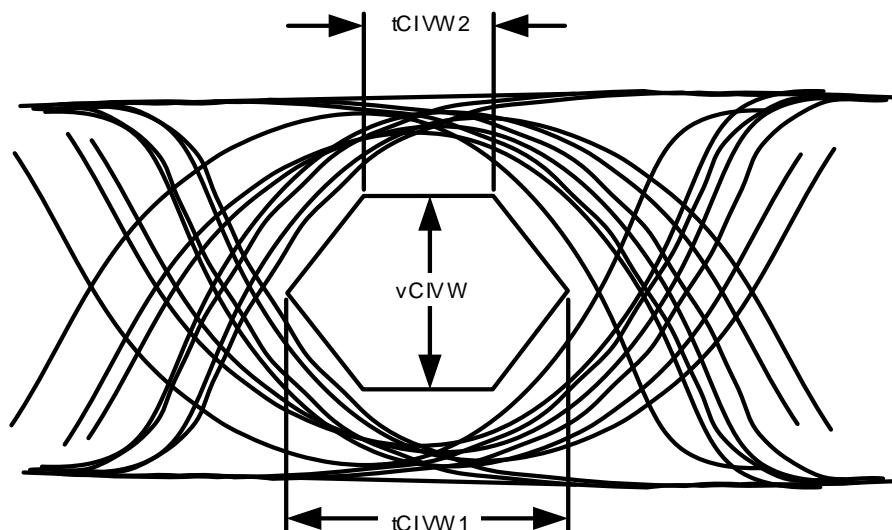
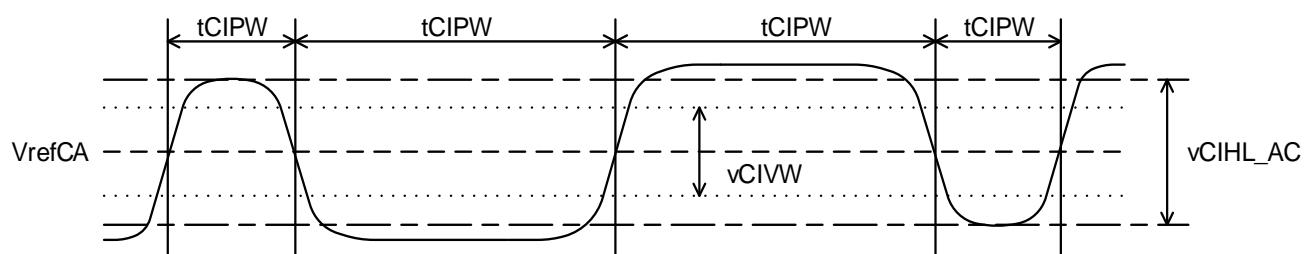


Figure 223 — CA Rx Mask definition

LPDDR5 CA Rx single pulse definition as shown in

Figure 224.



NOTE 1 Single pulse include any cycle of pulse.

NOTE 2 VrefCA is calculated value based on VDDQ and MR12.

Figure 224 — CA Rx single pulse definition

15.6.1 CA Rx mask and single pulse definition (Cont'd)

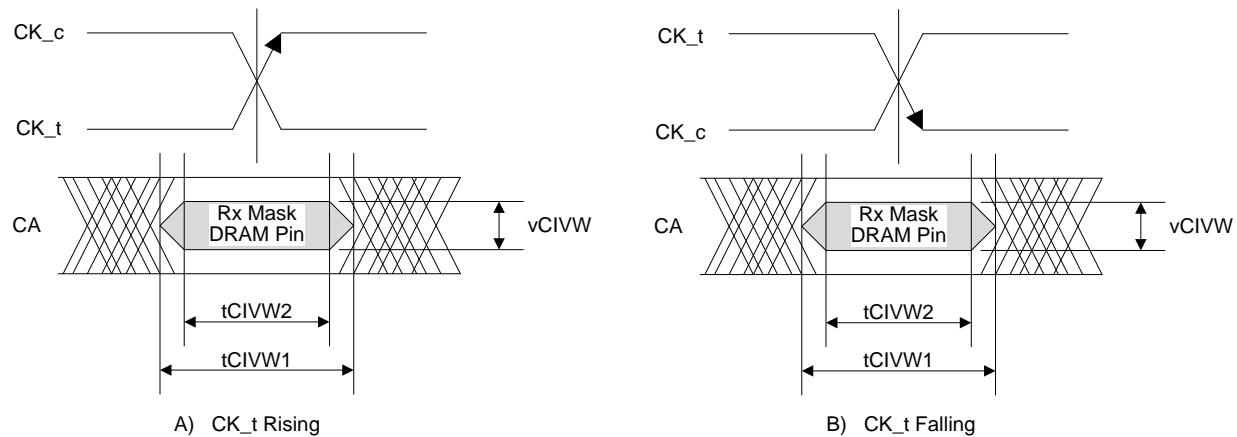


Figure 225 — CA timings at the DRAM Pins

Differential CK mode definition

All of the timing terms in Figure 225 are measured from CK_t/CK_c (differential mode) / CK (single ended mode) to the center (midpoint) of the tCIVW1 and tCIVW2 window taken at the midpoint and vCIVW voltage level. CA Rx mask window center is around CK_t/CK_c cross point (differential mode) / CK (single ended mode).

Single Ended CK mode definition.

15.6.2 CA Rx mask and single pulse specification

Table 354 — CA Rx Specification

Item	Symbol	Min/ Max	CK Frequency (MHz)										Unit	Note	
			67 ^A	133	200	266	344	400	467	533	600	688	750	800	
Rx Mask															
CA Rx mask width at TBD	tCIVW1	Min												UI	1,2
CA Rx mask width at vCIVW	tCIVW2	Min												UI	1,2
CA Rx mask height	vCIVW	Min												mV	3
Rx Single pulse															
CA Rx pulse width	tCIPW	Min												UI	4
CA Rx pulse amplitude	vCIHL_AC	Min												mV	5
CA Vref															
CA Vref	VrefCA	Max												mV	
		Min												mV	
CA mask offset															
CA to CA offset	tCA2CA	Max												ps	6
A) The Rx voltage and absolute timing requirements apply for all CA operating frequencies at or below 67 for all speed bins. For example tCIVW1 (ns) = 4.77ns at or below 67MHz CK frequencies.															

NOTE 1 CA Rx mask voltage and timing parameters at the pin including temperature drift and voltage AC noise impact for frequencies >TBD MHz and max voltage of TBD mv pk-pk from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise has to comply to the component Min-Max DC operating conditions.

NOTE 2 Rx mask voltage vCIVW1(max) has to be centered around VrefCA.

NOTE 3 CA single input pulse signal amplitude into the receiver has to meet or exceed vCIHL AC at any point over the total UI. No timing requirement above level. vCIHL AC is the peak to peak voltage centered around VrefCA such that vCIHL_AC/2 min has to be met both above and below VrefCA.

NOTE 4 CA only minimum input pulse width defined at the VrefCA.

NOTE 5 vCIHL_AC does not have to be met when no transitions are occurring.

NOTE 6 tCA2CA is defined fastest CA[x] mask center to slowest CA[y] mask center.

15.7 DQ, DMI, Parity and DBI Rx specification

15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition

LPDDR5 DQ, DMI, Parity and DBI Rx mask is defined as hexagonal mask as shown in Figure 226. The mask ($vDIVW$, $tDIVW1$, $tDIVW2$) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal.

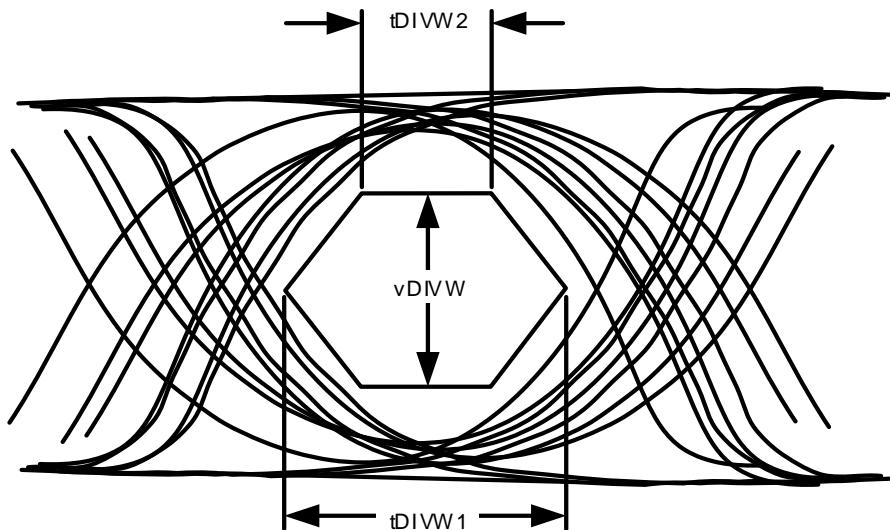
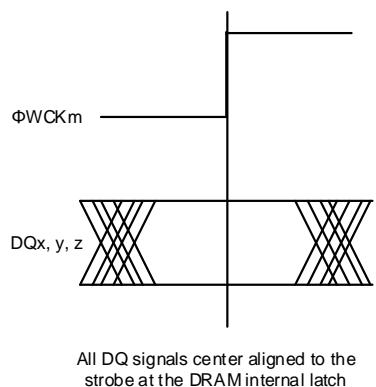


Figure 226 — DQ, DMI, Parity and DBI Rx Mask definition

15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition (Cont'd)

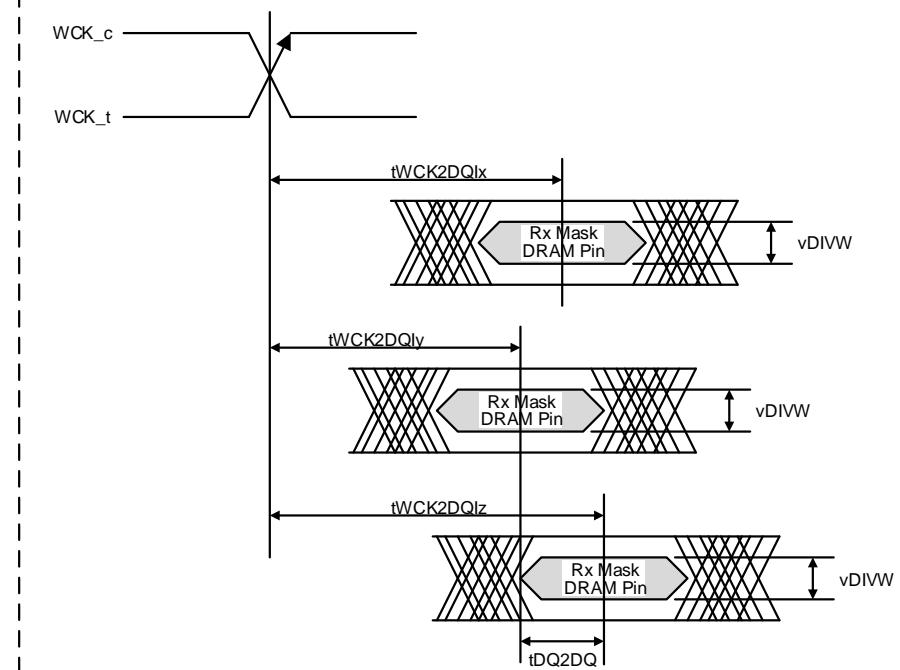
DQ, internal WCK data-in at DRAM Latch

Internal composite Data-Eye Center aligned to Internal WCK



DQ, WCK data-in at DRAM Pin

Non Minimum Data Eye / Maximum Rx Mask



NOTE 1 tWCK2DQI is measured at the center (midpoint) of the tDIVW window.

NOTE 2 DQz represents the max tWCK2DQI in this example

NOTE 3 DQy represents the min tWCK2DQI in this example

Figure 227 — DQ to WCK tWCK2DQI and tDQ2DQ Timings at the DRAM pins referenced from the internal latch

15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition (Cont'd)

LPDDR5 DQ, DMI, Parity and DBI Rx single pulse definition as shown in Figure 228.

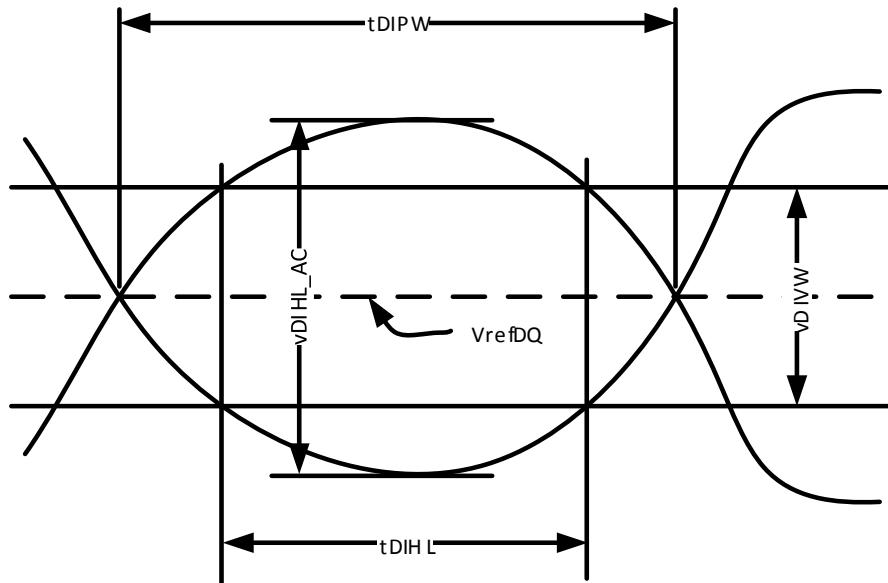


Figure 228 — DQ, DMI, Parity and DBI Rx single pulse definition

15.7.2 DQ, DMI, Parity and DBI Rx mask and single pulse specification

Table 355 — DQ, DMI, Parity and DBI Rx Specification

item	Symbol	Min/ Max	WCK Frequency (MHz)											Unit	Note
			266	533	800	1067	1375	1600	1867	2134	2400	2750	3000		
Rx Mask															
DQ Rx mask width at TBD	tDIVW1	Min												UI	1
DQ Rx mask width at vDIVW	tDIVW2	Min												UI	1
DQ Rx mask height	vDIVW	Min	140		120							100		mV	1,2
Rx Single pulse															
DQ Rx pulse width	tDIPW	Min												UI	4
DQ Rx pulse width above/below vDIVW	tDIHL	Min												UI	4
DQ Rx pulse amplitude	vDIHL_AC	Min										140		mV	3
DQ Vref															
DQ Vref	VrefDQ	Max		350								225		mV	
		Min										75		mV	

NOTE 1 Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >TBD MHz and max voltage of TBD mv pk-pk from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.

NOTE 2 Rx mask voltage vDIVW has to be centered around VrefDQ.

NOTE 3 DQ single input pulse amplitude into the receiver has to meet or exceed vDIHL_AC at any point over the total UI. No timing requirement above level. vDIHL AC is the peak to peak voltage centered around VrefDQ such that vDIHL_AC/2 min has to be met both above and below VrefDQ.

NOTE 4 DQ only minimum input pulse width defined at the VrefDQ.

15.8 Pull Up/Pull Down Driver Characteristics and Calibration

All output pins (DQ, DMI, RDQS_t and RDQS_c) driver characteristics and calibration are defined following.

Table 356 — Pull-down Driver Characteristics, with ZQ Calibration

$R_{ONPD,nom}$	Resistor	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.9	1	1.1	RZQ/6
48 Ohm	R_{ON48PD}	0.9	1	1.1	RZQ/5
60 Ohm	R_{ON60PD}	0.9	1	1.1	RZQ/4
80 Ohm	R_{ON80PD}	0.9	1	1.1	RZQ/3
120 Ohm	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 Ohm	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

NOTE 1 All value are after ZQ Calibration, see Table 358. Without ZQ Calibration R_{ONPD} values are $\pm 30\%$.

NOTE 2 R_{ONPD} limits are defined at same voltage and temperature as at the time ZQ calibration was done.

Table 357 — Pull-Up Characteristics, with ZQ Calibration

$VOH_{PU,nom}$	$VOH,nom(mV)$	Min	Nom	Max	Unit
$V_{DDQ}^*0.5$	250	0.9	1	1.1	VOH,nom

NOTE 1 All values are after ZQ Calibration. Without ZQ Calibration $VOH(nom)$ values are $\pm 30\%$.

NOTE 2 VOH,nom (mV) values are based on a nominal $VDDQ = 0.5V$, $VDD2H=1.05V$.

NOTE 3 VOH_{PU} limits are defined at same voltage and temperature as at the time ZQ calibration was done.

NOTE 4 VOH_{PU} limits are defined for load termination matching the SOC ODT setting (in MR17 OP[2:0]) selected at the time ZQ calibration was done. If the selected SOC ODT setting MR17 OP[2:0]=000_B, then the VOH_{PU} limits are not defined.

NOTE 5 VOH_{PU} limits are defined as DC levels when all DQ drivers are driving high.

NOTE 6 Assumption of SOC ODT is typical for $VOH_{PU,nom}$ definition.

Table 358 — Valid Calibration Points

$VOH_{PU,nom}$	ODT Value					
	240	120	80	60	48	40
$V_{DDQ}^*0.5$	VALID	VALID	VALID	VALID	VALID	VALID

NOTE 1 Once the output is calibrated for a given $VOH(nom)$ calibration point, the ODT value may be changed without recalibration.

Table 359 — Un-terminated Pull Up Characteristics

$R_{ONUNPU,nom}$	Resistor	Min	Nom	Max	Unit
40 Ohm	$R_{ON40UNPU}$	0.7	1	1.3	RZQ/6
48 Ohm	$R_{ON48UNPU}$	0.7	1	1.3	RZQ/5
60 Ohm	$R_{ON60UNPU}$	0.7	1	1.3	RZQ/4
80 Ohm	$R_{ON80UNPU}$	0.7	1	1.3	RZQ/3
120 Ohm	$R_{ON120UNPU}$	0.7	1	1.3	RZQ/2
240 Ohm	$R_{ON240UNPU}$	0.7	1	1.3	RZQ/1

NOTE R_{ONUNPU} is defined at $VOH = VDDQ/2$.

15.9 Output Driver and Termination Resistance Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 360 — Worst Case Output Driver and Termination Resistance

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	$0.5 \times VDDQ$	$R_{ONPD}(\text{nom}) \times (0.90 - (dR_{ON}dT(\text{max}) \times \Delta T) - (dR_{ON}(\text{max})dV2 \times \Delta V2) - (dR_{ON}(\text{max})dVQ \times \Delta VQ))$	$R_{ONPD}(\text{nom}) \times (1.10 + (dR_{ON}(\text{max})dT \times \Delta T) + (dR_{ON}(\text{max})dV2 \times \Delta V2) + (dR_{ON}(\text{max})dVQ \times \Delta VQ))$	ohm	1,2,3
R_{TT}	$0.5 \times VDDQ$	$R_{TT}(\text{nom}) \times (0.90 - (dR_{ON}(\text{max})dT \times \Delta T) - (dR_{ON}(\text{max})dV2 \times \Delta V2) - (dR_{ON}(\text{max})dVQ \times \Delta VQ))$	$R_{TT}(\text{nom}) \times (1.10 + (dR_{ON}(\text{max})dT \times \Delta T) + (dR_{ON}(\text{max})dV2 \times \Delta V2) + (dR_{ON}(\text{max})dVQ \times \Delta VQ))$	ohm	1,2,3
R_{ONUNPU}	$0.5 \times VDDQ$	$R_{ONUNPU}(\text{nom}) \times (0.70 - (dR_{ON}UNdT(\text{max}) \times \Delta T) - (dR_{ON}(\text{max}) UNdV2 \times \Delta V2) - (dR_{ON}(\text{max}) UNdVQ \times \Delta VQ))$	$R_{ONUNPU}(\text{nom}) \times (1.30 + (dR_{ON}(\text{max}) UNdT \times \Delta T) + (dR_{ON}(\text{max}) UNdV2 \times \Delta V2) + (dR_{ON}(\text{max}) UNdVQ \times \Delta VQ))$	ohm	2,3

NOTE 1 $\Delta T = T - T(@ \text{Calibration})$, $\Delta V2 = VDD2H - VDD2H(@ \text{Calibration})$, $\Delta VQ = VDDQ - VDDQ(@ \text{Calibration})$

NOTE 2 $dR_{OND}dT$, $dR_{OND}dV2$, $dR_{OND}dVQ$, $dR_{TT}dV2$, $dR_{TT}dVQ$, $dR_{ON}UNDT$, $dR_{ON}UNDV2$ and $dR_{ON}UNDVQ$, are not subject to production test but are verified by design and characterization.

NOTE 3 VDD1, VDD2H, VDD2HQ and VDDQ must be nominal during measurement.

Table 361 — Worst Case Output high voltage

Voltage	Min	Max	Unit	Notes
$VOHPU$	$VOHPU(\text{nom}) \times (0.90 - (dVOH(\text{max})dT \times \Delta T) - (dVOH(\text{max})dV2 \times \Delta V2) - (dVOH(\text{max})dVQ \times \Delta VQ))$	$VOHPU(\text{nom}) \times (1.10 + (dVOH(\text{max})dT \times \Delta T) + (dVOH(\text{max})dV2 \times \Delta V2) + (dVOH(\text{max})dVQ \times \Delta VQ))$	V	1,2,3,4

NOTE 1 $\Delta T = T - T(@ \text{Calibration})$, $\Delta V2 = VDD2H - VDD2H(@ \text{Calibration})$, $\Delta VQ = VDDQ - VDDQ(@ \text{Calibration})$

NOTE 2 $dVOHdT$, $dVOHdV2$ and $dVOHdVQ$ are not subject to production test but are verified by design and characterization.

NOTE 3 Refer to 15.8, Pull Up/Pull Down Driver Characteristics, for VOHPU.

NOTE 4 VDD1, VDD2H, VDD2HQ and VDDQ must be nominal during measurement.

15.9 Output Driver and Termination Resistance Temperature and Voltage Sensitivity (Cont'd)

Table 362 — Output Driver and Termination Resistance Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	%/ $^{\circ}$ C
$dR_{ON}dV2$	R_{ON} VDD2H Voltage Sensitivity	0.00	0.50	%/mV
$dR_{ON}dVQ$	R_{ON} VDDQ Voltage Sensitivity	0.00	0.20	%/mV
$dVOHdT$	VOH Temperature Sensitivity	0.00	0.75	%/ $^{\circ}$ C
$dVOHdV2$	VOH VDD2H Voltage Sensitivity	0.00	0.35	%/mV
$dVOHdVQ$	VOH VDDQ Voltage Sensitivity	0.00	0.35	%/mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	%/ $^{\circ}$ C
$dR_{TT}dV2$	R_{TT} VDD2H Voltage Sensitivity	0.00	0.50	%/mV
$dR_{TT}dVQ$	R_{TT} VDDQ Voltage Sensitivity	0.00	0.20	%/mV
$dRONUNDT$	Un-terminated RON Temperature Sensitivity	0.00	0.75	%/ $^{\circ}$ C
$dRONUNDV2$	Un-terminated RON VDD2H Voltage Sensitivity	0.00	0.75	%/mV
$dRONUNDVQ$	Un-terminated RON VDDQ Voltage Sensitivity	0.00	0.75	%/mV

16 Die configuration, Package ballout & Pin Definition

16.1 Package Configuration

16.1.1 Package Considerations for Byte-Mode Devices

Two Byte-Mode LPDDR5 SDRAMs can be logically combined into a Standard LPDDR5 SDRAM. Byte mode devices use the same bank architecture with one row address added and the page size reduced by half compared to a standard device of the same density. Two byte-mode die of the same density can be combined to make an equivalent x16 device of twice the given density. The inputs are ganged and the DQ busses from the two devices are assigned individually to the 16-bit channels.

Packages for Standard and Byte-Mode devices share the same ballmaps. This section describes internal wiring changes and system considerations when using packages containing Byte-Mode devices.

Three different die combinations are supported:

- 1) Standard - Packages configured with only Standard LPDDR5 die.
- 2) Byte-Mode - Packages configured with only Byte-Mode LPDDR5 die.
- 3) Mixed - Packages configured with both Standard and Byte-Mode LPDDR5 die. In this mixed configuration, some ranks contain only Standard die and other ranks contain only Byte-Mode die.

For mixed packages, standard devices shall be assigned to the lower numbered ranks and byte-mode devices shall be assigned to the higher numbered ranks.

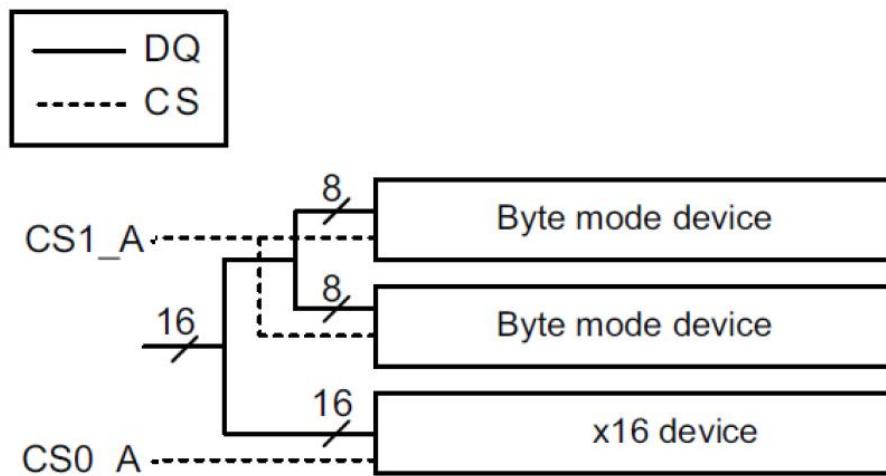


Figure 229 — Example of rank assignment for a single-channel dual-rank package

16.2 Pad Order

Table 363 — LPDDR5 Pad order

TOP	
Pad number	Pad Name
1	VDD2H
2	VSS
3	VDD1
4	VDD2H
5	VDD2L
6	VSS
7	VDD2H
8	VSS
9	DQ8
10	VDDQ
11	DQ9
12	VSS
13	DQ10
14	VDDQ
15	DQ11
16	VSS
17	RDQS1_t
18	RDQS1_c
19	VDDQ
20	VDD2H
21	WCK1_c
22	WCK1_t
23	VSS
24	VDD2L
25	VDDQ
26	DMI1
27	VSS
28	DQ12
29	VDDQ
30	DQ13
31	VSS
32	DQ14
33	VDDQ
34	DQ15
35	VSS

Pad number	Pad Name
36	VDD2H
37	RESET_n
38	VDD2L
39	VSS
40	CA6
41	CA5
42	VDD2H
43	CA4
44	CA3
45	VSS
46	CK_c
47	CK_t
48	VDD2H
49	CS
50	CA2
51	VSS
52	CA1
53	CA0
54	VDD2H
55	VDD2L
56	VSS
57	ZQ
58	VDDQ
59	VDD2H

Pad number	Pad Name
60	VSS
61	DQ7
62	VDDQ
63	DQ6
64	VSS
65	DQ5
66	VDDQ
67	DQ4
68	VSS
69	DMI0
70	VDDQ
71	VDD2L
72	VSS
73	WCK0_t
74	WCK0_c
75	VDD2H
76	VDDQ
77	RDQS0_c
78	RDQS0_t
79	VSS
80	DQ3
81	VDDQ
82	DQ2
83	VSS
84	DQ1
85	VDDQ
86	DQ0
87	VSS
88	VDD2H
89	VSS
90	VDD2L
91	VDD2H
92	VDD1
93	VSS
94	VDD2H
Bottom	

NOTE 1 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 2 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

16.3 Package Ballout

TBD

16.4 Package Die Layout

Ballmaps for LPDDR5 dual-channel packages shall follow the pad order based on the second die placement (Channel B) being rotated with respect to the first die (Channel A) placement.

Ballmaps for LPDDR5 quad-channel packages shall follow the pad order based on:

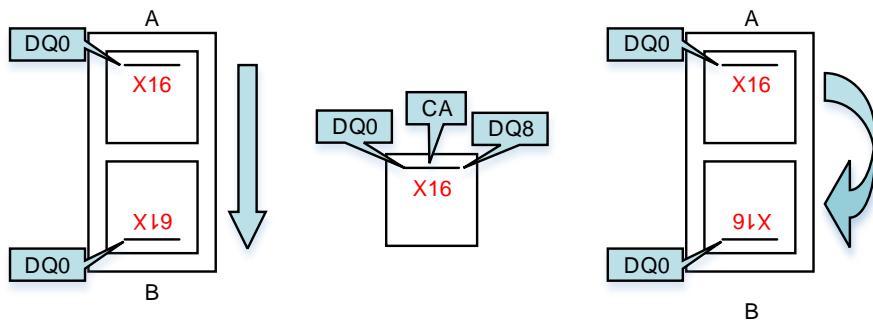
1. The Channel B die placement being rotated with respect to the Channel A die placement.
2. The Channel D die placement being rotated with respect to the Channel C die placement.

BELOW IS FOR REFERENCE ONLY:

LPDDR5 is based on a single channel (x16) die concept. In contrast, LPDDR4 is based on a dual channel die concept with the pad order of the second channel being mirrored with respect to the first channel.

Examples of dual channel mirror die (LPDDR4) and single channel die (LPDDR5) package layout are shown below. LPDDR5 pad ordering has not been balloted and is shown for illustrative purposes only.

Table 364 — Package configuration example



LPDDR4 Dual
Channel Mirror Die

- Ch. B is folded down from Ch. A.

LPDDR5 single
Channel die

- Pad order approach likely similar to LPDDR4

Example of placing 1 Ch.
die in 2 Ch. configuration

- Ch. B is rotated from Ch. A

16.5 Package Configuration

TBD

16.6 ZQ Wiring

LPDDR5 devices are designed to allow up to NZQ die within a single package to connect to a common ZQ resource. When multiple die share a ZQ resource, one die is designated as the master die. ZQ Calibration Command to Latch Time (tZQCAL4, tZQCAL8 and tZQCAL16) varies depending on the number of die sharing a ZQ resource. (See 4.2.1, ZQ Calibration, for more information.)

Single and dual-channel packages shall support a single ZQ ball which is wired to all die.

Quad-channel packages support 2 ZQ balls where all die from two channels are wired to each ZQ ball. Wiring details are specified in the package ballmap.

Logical mapping – channel, rank and byte (for byte mode) - for all master die is specified in the package ballmap.



Standard Improvement Form

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The referenced clause number has proven to be:

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