HAPS®-80 S104
Reference Manual

July 2017

SYNOPSYS®

solvnet.synopsys.com

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Revision History

Date	Revision	Comment
Jan 2016	0	Initial version.
July 2017	1	pg 14 Added JTAG connector to Connectors and Onboard Functions. pg 27 Added fastening daughter board information. pg 35 Added battery information. pg 36 Updated power supply to HAPS PSU-HC. pg 47 Corrected clock connector names. pg 49 Changed the number of systems that can be synchronized from four to any number. pg 60 Added a table for LED behavior during a firmware upgrade. pg 61 Added text about reset before powering down. pg 62 Added text about reference pins for DCI I/O standards text for HAPS-80 exception. pg 93 Added MGB Link pin tables. pg 107 Added PCB-Trace Delay.

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CHAPTER 1

General Information

HAPS-80 S104 conforms to the HapsTrak® standard which guarantees compatibility with previous and future generation HAPS products.

This document is the HAPS-80 S104 Reference Manual and describes the functions of the HAPS-80 S104 system.

For an up-to-date list of HAPS® daughter boards and accessories go to www.synopsys.com/haps.

ProtoCompiler is dedicated software for HAPS systems. Designed to minimize the effort and time required to bring-up and then deploy a Synopsys® HAPS Series system for IP validation and software development, for more information go to ynopsys.com/FPGA-based-prototyping. ProtoCompiler manuals and user guides can be found under SolvNet® > Documentation > ProtoCompiler.

Emissions

The HAPS®-80 S104 system is a hardware/software development platform that constitutes of an open system design (i.e., has no shielded enclosure) and it has not been tested for compliance with any standard for radio frequency. Since the operation of the product may cause interference with radio communications or with other electronic devices, Synopsys supplies the product to you with the following operational guidance: (a) operate the product only in a shielded laboratory environment, (b) take adequate measures to prevent, reduce or mitigate the effects of undesirable interference, and (c) do not operate the product for use in or with products or applications where the use or malfunction thereof may result in personal injury, death, or catastrophic loss. You assume the entire risk associated with your use of the product outside of these operational guidelines.

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Environmental Guidelines

The conditions recommended in this document apply to the inlet fans of HAPS units with fans or ambient conditions for units without fans.

	Range
Temperature	20 - 25°C (68 - 77°F)
Moisture	40 - 55% Relative Humidity

Ensure Sufficient Airflow

Make sure nothing is blocking the inlet fans or the outlets. For standard desktop use it is recommended to keep a minimum distance of 50 cm between the inlet fans/outlets and any blocking obstacles. When HAPS units are rack-mounted in a data center using a cooling system a smaller distance is acceptable.

Technical Support

Technical support is available on SolvNet® at solvnet.synopsys.com. First time users must register for access to both SolvNet and HAPS SupportNet.

HAPS SupportNet has the latest reference manuals, user guides, application notes, board files, firmware, and more. Login to SolvNet, click on the “Documentation” tab and then on “HAPS”.

IMPORTANT!

ESD

The HAPS®-80 S104 system, as all other electronic equipment, is sensitive to electrostatic discharge (ESD). Make sure to handle the device properly.

When handling the HAPS®-80 S104 system:

•Transport the HAPS®-80 S104 in an ESD case when moving outside an ESD protected environment

•Wear an antistatic wrist strap

•Work area should be ESD secured

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Hot Plugging is Prohibited

Do not hot plug daughter boards and cables. Always power down the HAPS®-80 S104 system when adding or removing daughter boards and cables. There is a risk of damaging both the system and daughter board if this instruction is not followed.

HapsTrak 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.

When connecting daughter boards and HT3 cable connectors, they should be held parallel to the HAPS-80 connector throughout the mating process.

For important information about installing daughter boards, see Fastening Daughter Boards, on page 27.

Handling

When moving the system always carry by baseplate and not by frame.

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Overview

Synopsys® High-Performance ASIC Prototyping System HAPS-80 with Symmetrical System Architecture (SSA) offers the best system performance, reliability, and design automation in the industry. HAPS-80 S104 is a Xilinx Virtex UltraScale based system in the HAPS series of ASIC prototyping platforms. The system is designed for maximum performance, with respect to signal integrity, speed and other critical issues. Signals to connectors are length matched, thus minimizing skew and allowing very high speed signaling. A single HAPS-80 S104 system can accommodate up to approximately 104 million ASIC gates. For larger capacity designs the HAPS-80 S104 can be expanded by connecting additional systems and daughter boards using the HapsTrak standard.

Figure 1: The HAPS-80 S104

Features

- 4 Xilinx Virtex UltraScale XCVU440 FLGA2892 FPGAs
- 16 GTH transceiver quads in 8 HapsTrak MGB connectors
- 32 GTH transceiver channels over SATA (MGB Links) for user design
- transceiver channels transceiver channels In-system DTD memory buffer with 8 GB memory.
- Cloud system configurations
- HapsTrak 3 connector technology
- Selectable I/O voltage for HapsTrak 3 daughter board slots

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- Support for high-speed interconnections and multiplexing between user FPGAs
- UMRBus® support with data transfers up to 100 MB/s
- Network connection over Ethernet
- Real-time monitoring of voltage and temperature
- UMRBus communication and configuration over:
  - PCIe
  - USB
  - Ethernet
- Standalone configuration through Flash memory medium

High level Construction

HAPS-80 is a modular design, both in the way it can be used in combination with other products from the HAPS family, but also in the way it has been designed internally. To facilitate scaling up and down in design size, the three members of the HAPS-80 family, S104, S52 and S26 have all been designed using the same FPGA module. This ensures identical design behavior and performance across the different HAPS-80 systems.

Access to the HapsTrak 3 connectors is from the top, whereas access to the power connector, MGB, clocks, configuration connectors is from the four sides.

It is important that the system be carried by holding the base plate. The top-side frame, if mounted, provides an additional structure for daughter boards, securing equipment and allows systems to be placed on top of each other and can be removed if needed. Note the weight limit specified in section System Dimensions, on page 63.

FPGA module and Virtex UltraScale

HAPS-80 S104 contains four FPGA modules each hosting one Virtex UltraScale XCVU440 device.

Delivering high bandwidth and low latency, Virtex UltraScale is highly suitable for prototyping and enables rapid development and emulation.

For more information go to xilinx.com.

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Connectors and Onboard Functions

HapsTrak 3

The HAPS-80 S104 System has a total of 96 HapsTrak 3 connectors, 8 MGB connectors and 32 MGB Links for debug use or user design. These are all directly connected to the FPGA and available for user designs.

HapsTrak 3 connector standard, with extended functionality and pinout as well as proven high performance both for single ended and differential signaling, makes efficient use of the Virtex UltraScale FPGA bank structure. For more information see HapsTrak 3 Signals, on page 29.

MGB

Each MGB connector supports 8 GTH transceiver channels. Virtex UltraScale FPGA provides GTH transceivers capable of up to 16.375 Gb/s. For more information see General Purpose I/Os, on page 30.

Connectors for System Setup

CDE Out, CDE In, network, USB and SD card interfaces, are used for set up of the board and configuration of the FPGAs. For more information see Configuration, on page 56.

JTAG

JTAG connector may be used to access Xilinx JTAG chain for User FPGAs. For more information go to the document “UG908 - Vivado Design Suite User Guide: Programming and Debugging” at xilinx.com.

Status LEDs

The status LEDs indicate if temperatures and voltages are within limits, and whether the FPGAs are configured, see LED Behavior, on page 59.

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Layout

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Figure 2: Block Diagram

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I/O Signals and Connections

Each FPGA on the HAPS-80 system connects to 24 HapsTrak 3 connectors, 2 MGB connectors, 8 MGB Links and GPIO. Although HapsTrak 3 connectors can be used for any type of application required I/O, the following is the recommended best practice:

- Use HapsTrak 3 connectors 1-12 for daughter board and for communication through interconnect cables to other HAPS systems.
- Use HapsTrak 3 connectors 13-24 for inter-system connections with buses.

Figure 3: I/O Signals and Connections

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VCCO Regions

The HapsTrak 3 connectors support VCCO voltages 1.0 V, 1.2V, 1.35V, 1.5V and 1.8V; except connectors 16, 17, 18 and 19 that have a fixed VCCO 1.8V.

Connector J12 HR is connected to a high-range I/O bank, and has the following extra properties:

- It supports 1.2V, 1.35V, 1.5V, 1.8V, 2.5V and 3.3V
- It does not support HSTDM (High Speed Time Domain Multiplexing).
- VRP is not connected

The GPIO signals are all 3.3V signals.

Note: For more information about HSTDM see the ProtoCompiler User Guide.

I/O Signals

Each HapsTrak 3 connector on the HAPS-80 system has 52 pins used for I/O signaling. See HapsTrak 3 Signals, on page 29.

FPGA Inter-connections

The HAPS-80 systems have built-in inter-FPGA connections explained on pg 24. FPGA inter-connections can also be done through flexible interconnect cables available in different lengths. The cables have auto-detection by means of an ID-PROM, VCCO Feedback, VCCO and DCI termination. For more information refer to HAPS Interconnect Cables HT3 Reference Manual at solvnet.synopsys.com.

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System IP and General Purpose I/Os

Figure 4: System IP

A GPIO header is available as an additional user input/output similar to previous generations of HAPS systems. The GPIO header, the MGB GPIO pins and the user LEDs are attached to the CDE Controller, a support device on the FPGA module. This save signals and the CDE controller also takes care of the voltage level adjustment to 3.3 V for the GPIO signals.

In order to use these signals, a System IP block will be instantiated in the FPGA. The Controller FPGA takes care of the voltage level adjustment of the GPIO signals. The GPIO connector carries 10 general purpose signals.

The System IP is a module that the ProtoCompiler automatically inserts for each HAPS-80 FPGA. It consolidates various operations including multiplexing, serialization and deserialization, local resets, GCLK0 de-skewing, UMR chaining, and PCB trace assignment for GPIO, buttons, and LEDs. For more information refer to the ProtoCompiler User Guide.

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Limitations

GPIO signals are limited to approximately 400 kHz.

LEDs

LEDs on the FPGA modules and on the front panel indicate status of the system. See Configuration, on page 56 for a detailed listing.

User LEDs FPGA

MGB Link Panel

User Panel

Power On/Off Button

Figure 5: LED locations on HAPS-80 systems

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Clocks

Local clocks on FPGAs are available through a number of HapsTrak 3 connector and the built-in FPGA inter-connect pins. Signals are differential, totaling 284 GC (Global Clock) pairs, 108 GC_QBC (Global Clock, Quad-Byte Clock) pairs and 432 DBC (Dedicated-Byte Clock) pairs.

HAPS-80 has 13 global clocks distributed to all user FPGAs with low intra-FPGA skew. The clocks can be sourced from internal generators, derived directly from the FPGAs, or derived from external sources.

For more information see Clocks, on page 37.

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CHAPTER 2

Concept

HapsTrak

HAPS is a system solution consisting of software and hardware that aims to provide the most productive and efficient way of doing FPGA prototyping.

Important features that makes HAPS a powerful FPGA prototyping system are:

- Access to FPGA I/O signals through the proven HapsTrak 3 and MGB connectors
- Highly flexible ways of creating interconnect structures through built-in interconnects, cables and interconnect cards
- Daughter boards and interface cards connect to the HapsTrak 3 or MGB connectors and provide access to, for example, DDR memory, FLASH and PCIe connections
- Convenient and scalable ways to connect multiple HAPS systems in cloud configurations

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HapsTrak 3

HapsTrak is a mechanical and electrical standard for attaching daughter boards and interconnects to a HAPS prototyping system. It specifies mechanical dimensions, connector types and locations, as well as pinout, electrical signal properties and power rules. To be HAPS compliant, all systems, motherboards and daughter boards must follow these standards.

The HapsTrak 3 (HT3) is a 160-pin connector containing 58 signal pins, most of which can be used for single ended or differential signaling. HAPS-80 uses 52 of the 58 signal pins and since HapsTrak 3 cables make use of VRN and VRP, 50 signals are available in the created bus.
See HapsTrak 3 Signals, on page 29.

All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

HapsTrak MGB

The HAPS MGB (Multi-GigaBit) family is a collection of interface cards, built around the HapsTrak MGB bus and supported by HAPS systems.

64 GTH transceiver channels in the FPGAs are available in 8 HapsTrak MGB connectors: 8 high-speed SerDes channels in each. Each connector also has 10 low-speed GPIO signals.

For more information about the available cards, go to synopsys.com or refer to the MGB Interface Cards Reference Manual at solvnet.synopsys.com.

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MGB Links

Each FPGA module has a panel with eight SATA connectors. Each connector has one XCVU440 GTH transceiver from two GTH quads with a dedicated reference clock oscillator at 150 MHz. The GTH transceivers can be used for data transfer to external devices or to another FPGA in the same or different HAPS-80 system. Some example applications are:

•SATA protocol data connection

•User proprietary protocol direct data connection

When using a SATA cable to connect between two connectors, select the correct cable type; straight or cross-over. A crossover SATA cable is required for direct connection between SATA connectors of two HAPS-80 FPGAs. By definition, the recommended maximum transceiver link speed when using a SATA III cable is no more than 6 Gbps per transceiver.

See MGB Link PCB-Trace Names, on page 103.

FPGA Interconnects

Built-in Interconnects

High-Speed SerDes Channels

New to the HAPS-80 series are 24 GTH high-speed SerDes channels built-in interconnects per FPGA. Some of these channels are reserved for internal use, such as built-in debug, and are not available for user designs, see Inter-FPGA Connections, on page 92.

Note: GTH high-speed SerDes channels available for user designs are subject to change in the future.

Fixed Inter-FPGA Connections

HAPS-80 S104 has fixed inter-FPGA connections between FPGAs A and D, and between FPGAs B and C. The fixed buses contain 141 signals including clocks.

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Figure 1: Built-in FPGA-FPGA Interconnects

Interconnect Boards and Cables

On HAPS systems the majority of I/O signals are available on HapsTrak connectors. The connectors can be used either to add external logic or for connectivity between FPGAs.

For more information see the *Interconnect Boards and Cables HT3 Reference Manual* on HAPS SupportNet.

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Daughter Boards

Each daughter board mates with one or several connectors on the HAPS system. Daughter boards can be moved around freely, allowing reconfiguration of the prototype system as parts of the design moves from one FPGA to another. See Expansion and I/Os, on page 28 for connectors with limitations.

A daughter board for HAPS-DX7, HAPS-70 and HAPS-80 series systems has SEAM or SEAM-RA terminal type HapsTrak 3 connectors and typically contains peripheral or interconnect circuitry. Daughter boards can span one or several connectors and have different lengths specified in Figure 2 as types A, B and C.

For making custom daughter boards refer to ‘HapsTrak 3 Standard’ found at solvnet.synopsys.com. Go to synopsys.com/haps to find the current list of standard daughter boards.

Figure 2: Daughter Board Types

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Fastening Daughter Boards

Use the included screws to fixate a daughter board to the HAPS system when possible. If different screws are required for your design, or they were not included with your daughter board, use only polyamide nylon screws. The length of the screw must not extend further than a maximum of 6 mm below the daughter board to insure that the integrity of the HAPS system is not compromised. See illustration below.

Multi-system setups

HAPS systems have been designed to support prototyping needs ranging from desktop-mode single FPGA up to large network connected setups consisting of 10 or more HAPS systems. Furthermore, systems from different generations can function together. This creates a flexible and powerful environment where subcomponents of a large design can be verified independently using smaller HAPS setups, while still allowing a full scale design verification in the larger HAPS setup.

Building Concept

On a high level, multi-system setups can be built together in three different ways:

- For systems with top side frames, up to three 4-FPGA systems can be placed in a vertical stack
- Using 4-post rack equipment. For more information, contact Synopsys support
- Using application specific custom made equipment

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CHAPTER 3

Expansion and I/Os

The connectors on HAPS-80 are used for expansion of a HAPS system with daughter boards, either supplied by Synopsys or custom-made. A list of standard daughter and interconnect boards can be found at www.synopsys.com/haps. The I/O connectors comply with the HapsTrak 3 Standard which can be downloaded from HAPS SupportNet on SolvNet.

I/O Connectors

Each FPGA on the HAPS-80 system is connected to 24 HapsTrak 3 connectors. Each one is a 160-pin connector containing 58 signal pins, most of which can be used for single ended or differential signaling. HAPS-80 systems use 52 of the 58 signal pins and since HapsTrak 3 cables make use of VRN and VRP, 50 signals are available in the created bus.

All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

Connectors on an FPGA Module share the 3.3V rail. The maximum allowed total power consumption on this rail is 50 A per FPGA Module.

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HapsTrak 3 Signals

HAPS-80 connects pins A[0-12], B[0-11], C[0-11], D[0-12] as well as VRN and VRP in each HT3 connector. Connectors can be individually set to a VCCO voltage from 1.0V to 1.8V according to Xilinx IOStandards.

J12 connects to an HR I/O Bank and can be set from 1.2V to 3.3V.

Connectors J16, J17, J18 and J19 of each FPGA are limited, this means:

- Pins D[11-12] are not connected
- Pins D[0-1] are not clock capable
- Fixed to 1.8V

8	GND	3.3	GND	3.3	GND	3.3	GND	3.3	1
16	A0	GND	B0	GND	C0	GND	D0	GND	9
24	GND	A2	GND	B2	GND	C2	GND	D2	17
32	A1	GND	B1	GND	C1	GND	D1	GND	25
40	GND	A3	GND	B3	GND	C3	GND	D3	33
48	A4	GND	B4	GND	C4	GND	D4	GND	41
56	GND	A6	GND	B6	GND	C6	GND	D6	49
64	A5	GND	B5	GND	C5	GND	D5	GND	57
72	GND	A7	GND	B7	GND	C7	GND	D7	65
80	A8	GND	B8	GND	C8	GND	D8	GND	73
88	GND	A10	GND	B10	GND	C10	GND	D10	81
96	A9	GND	B9	GND	C9	GND	D9	GND	89
104	GND	A11	GND	B11	GND	C11	GND	D11	97
112	A12	GND	B12	GND	C12	GND	D12	GND	105
120	GND	VRP	GND	C0P	GND	C1P	GND	Rsb	113
128	A13	GND	B13	GND	C13	GND	D13	GND	121
136	GND	VRN	GND	C0N	GND	C1N	GND	Rsb	129
144	IdC	IdA1	Uin0	GND	Uout0	GND	Rsb	GND	137
152	IdA0	IdD	GND	Uin1	GND	Uout1	GND	Reset_n	145
160	Vn	V	Vn	V	Vn	V	Vn	V	153

Legend

GND	Ground
VRP	Reference pins for DCI I/O-Standards
VRN	
C0N	Global clocks
C0P	
C1N	
C1P	
Uin0	LPC UMRBus signals
Uin1	
Uout0	
Uout1	
3.3	3.3V
V	VCCO
Vn	VCCO negotiation
xx	I/O
xx	A12 and D12 are pin paired (connected by a cable)
Reset_n	Reset
Idx	Identification clock, data and address
xx	NC
Rsb	Reserved for side band signal expansion

Figure 1: HapsTrak 3 Pins

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SLR Regions

Respect SLR (Super Logic Region) locations for interconnects and minimize routing between SLRs inside the FPGA. Respecting SLR locations generally renders logic with less clock skew within local region user logic. Certain restrictions exist in regard to clock resource use between SLRs.

Avoid crossing SLR boarders with a daughter board that has multiple HapsTrak 3 connectors and sources synchronous signals to the FPGA.

For more information see Xilinx User Guide UG572 and 'Architecture Clocking Resources User Guide' at xilinx.com.

HT3	Bank	CLOCK REGION	SLR	CLOCK REGION	Bank	HT3
FIXED INTERCONNECT	53	X0Y14	SLR2	X7Y14	73	J1
	52	X0Y13		X7Y13	72	J2
	51	X0Y12		X7Y12	71	J3
J13	50	X0Y11		X7Y11	70	J4
J14	49	X0Y10		X7Y10		
J15	48	X0Y9	SLR1	X7Y9	68	J5
J16	47	X0Y8		X7Y8	67	J6
J17	46	X0Y7		X7Y7	66	J7
J18	45	X0Y6		X7Y6	65	SYSTEM
J19	44	X0Y5		X7Y5	84, 94 (HR)	J12
J20	43	X0Y4	SLR0	X7Y4	63	J8
J21	42	X0Y3		X7Y3	62	J9
J22	41	X0Y2		X7Y2	61	J10
J23	40	X0Y1		X7Y1	60	J11
J24	39	X0Y0		X7Y0		

General Purpose I/Os

Each FPGA controls two dual-colored LEDs (L1 and L2), two buttons (B1 and B2) and 30 GPIO signals. 20 GPIOs are in the MGB connectors described in HapsTrak MGB Connectors, and 10 are located in a 2mm 14-pin header located on the MGB Link panel for each FPGA.

Note: LED L1 is the same as the LED GPIO on the top of the system.

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The signal level is 3.3V LVCMOS, and the header also provides power and GND pins to power simple I/O circuitry. GPIO signals are limited to approximately 400 kHz.

GPIO signals are not directly connected to the user FPGA, and must be controlled through the System IP block inserted by ProtoCompiler, as described in General Purpose I/Os, on page 30.

HapsTrak MGB Connectors

HAPS-80 S104 has two MGB connectors per FPGA giving a total of 8 MGB connectors. As each MGB connector contains 8 GTH high-speed SerDes channels, the system provides in total 64 of these channels. Each connector also has 10 low-speed GPIO signals. The HapsTrak MGB connectors are located in back of specially designed shelves in the sides of the HAPS-80 system. Grooves in the brackets provide the needed support for the MGB Interface Cards.

The HAPS MGB family is a collection of multi-gigabit SerDes based interface cards, built around the HapsTrak MGB bus and supported by HAPS-80 systems. For more information about the available cards, go to synopsys.com or refer to the MGB Interface Cards Reference Manual at solvnet.synopsys.com.

Figure 2: Built-in Shelves for MGB Interface Cards.

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Mounting an MGB Interface Card

To mount a MGB interface card in a HAPS-80 system:

1. Remove the appropriate cage from the HAPS-80 chassis by removing the screws at the top and bottom and sliding the cage out of the compartment.

2. Insert an MGB riser card, into one set of slots at the back of the cage. Make sure that the MGB interface connectors on the edge on the riser card are facing up and that the MGB card mating connectors are facing out. Each cage can hold two MGB cards.

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3. Slide the cage back into the chassis and secure the cage to the chassis with the four screws previously removed.

4. Reach into the cage and push the riser card up into its MGB mating connector located on the underside of the FPGA module. The riser card will “click” when properly seated.

5. Slide the interface card into a slot and push firmly to seat the card connector into its mating connector on the riser card.

6. Insert the MGB container locking pin through its mounting holes in the top and bottom tabs on the cage as shown to secure the card or cards in place.

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HapsTrak MGB Signals

Figure 3: HAPS MGB Connector Pins

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CHAPTER 4

Power

Power Overview

The HAPS-80 system is powered by connecting a +12 V source to two power terminals. All required voltages are generated from this source. Each HAPS-80 has its own power supply unit the HAPS PSU-HC.

Note: In rare heavy use cases, the HAPS-80 system may consume more power than the included power supply can deliver. If the HAPS-80 system is not operating properly under this type of condition, please contact support through SolvNet for assistance and advice.

Battery

Battery type: SR44 1.55V (195mAh) Silver Oxide coin cell

The UltraScale device makes it possible to encrypt bit streams in order to protect a design. The battery is used for buffering the encryption key while main power is off. The battery also functions as a backup for the real time clock.

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HAPS PSU-HC

The HAPS PSU-HC (PSU Host Control) allows you to conveniently power up to four HAPS-80 series units. The four output power connectors J1 through J4 are arranged in two groups (group 1 and group 2) each equipped with overcurrent protection. For large setups, HAPS PSU-HC units can be daisy chained to power on and off the HAPS systems from one location.

Refer to the HAPS PSU-HC Reference Manual on HAPS® SupportNet for operating instructions, important limitations, and conditions as well as proper cable hookup.

Power LEDs

The Power LED on the HAPS-80 system user panel and the Power button LED show green, indicating that +12 V is supplied and the on-board generated voltages, including the VCCO voltages, are within tolerance. If any voltage is incorrect, the Power LED will show red (the Power button LED will remain off).

The Power button LED will show amber when used with HAPS PSU-HC Control cable. See the HAPS PSU-HC Reference Manual for the PSU LED behavior during stand-by and error modes.

Correct Voltage

Incorrect Voltage

Power button LED

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CHAPTER 5

Clocks

Local Clocks

Local clocks on FPGAs are available through a number of HapsTrak 3 connector and the built-in FPGA inter-connect pins. Signals are differential, totaling 284 GC (Global Clock) pairs, 108 GC_QBC (Global Clock, Quad-Byte Clock) pairs and 432 DBC (Dedicated-Byte Clock) pairs.

Global Clocks

HAPS®-80 S104 has 13 global clocks distributed to all user FPGAs with low intra-FPGA skew. The clocks can be sourced from internal generators, derived directly from the FPGAs, or derived from external sources. All global clock nets use LVDS differential signaling for best performance.

- Clock GCLK0 is fixed at 100 MHz for system functions and is synchronized between multiple systems, to guarantee consistent data transfers between them. GCLK0 is reserved for system functions and should not be used directly by the customer design.
- GCLK1-GCLK12 are flexible and identical to those used in the HAPS-70 series this allows for convenient synchronization across HAPS-70 and HAPS-80 setups.

The HAPS-80 S104 system has two PLLs per FPGA that can be programmed to generate frequencies between 0.16 - 350 MHz, 367 - 473.33 MHz and 550 - 710 MHz. Outputs are synchronized on rising edge if greater than 5MHz. One output from each PLL is available in a pair of SMB connectors.

HAPS-80 clock availability:

- GCLK0 and Reset available in all HT3 connectors.

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- GCLK1-12 available in HT3 connectors 1-12 (one GCLK per connector).
- Clock start/stop functionality for GCLK12 can be controlled through CLKSTOPN pin from FPGA.
- Supervisor generated clocks for clock control through software (only supported by Synopsys tools).
- Clock Panel SMB connectors for external clocks.
- Easy clock synchronization between systems using CLK RIGHT/CLK LEFT connectors.

Clock Pins on Virtex UltraScale Devices

Each I/O bank in the Virtex UltraScale device provides three type of clock inputs with different properties; GC, GC_QBC and DBC.

In HAPS-80 systems, all pins in an I/O bank are available in the respective HT3 connector, including 4 pairs of clock capable pins that allow for clock input from daughter boards. Connectors 16, 17, 18 and 19, are an exception, with one clock capable pair less is available in each, see SLR Regions, on page 30.

For more information on GC, GC_QBC and DBC go to xilinx.com.

Global Clock Nets

HAPS-80 contains 13 global clock nets that are distributed to all FPGAs and selected HT3 connectors. All clocks are distributed as LVDS signals, and are length matched to assure the lowest possible skew between user FPGAs. In order to retain the best possible clock quality and the lowest skew, the user FPGAs should use an IBUFDS or IBUFGDS set to LVDS with DIFF_TERM enabled (provided by ProtoCompiler).

The global clock networks on HAPS-80 systems can be divided in four sections:

- Clock Generation
- Clock Interfaces
- Clock Distribution

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- Clock Stopping

Clock Generation

There are three global clocks on the HAPS-80 system:

- Fixed 100MHz Oscillator
- PLLs
- FPGAs

Figure 1: Clocks - Schematic View

Fixed 100 MHz Oscillator

The system contains a local 100 MHz oscillator available as GCLK0 in all FPGAs and on the C0 pin pair in all HT3 connectors. When several systems are chained, GCLK0 will be automatically synchronized using CDE IN and CDE OUT connectors.

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The system contains a local 100 MHz oscillator available as GCLK0 in its FPGA and on the C0 pin pair in all HT3 connectors. When several systems are chained, GCLK0 will be automatically synchronized using CDE IN and CDE OUT connectors.

PLLs

Each FPGA has two PLLs. Each PLL has three outputs feeding the clock distribution network and one output feeding two coaxes in the clock panel. The signal level is 2.5 V LVCMOS in SMB coaxes. These outputs can be used to source clocks for daughter boards or external equipment.

FPGAs

FPGA A and B can source global clock nets according to the table and illustration. This is useful to synchronize a system-level global clock with a peripheral clock from a daughter board. The FPGA connected to the daughter board would input the clock and redistribute it to the other FPGAs through a global clock net. FPGA C and D have the corresponding FPGA I/O connected to interconnects. The green boxes in Table signify signals used for FPGA interconnects and do not drive any clocks.

FPGA	Output Pin			
	CLKSRC1	CLKSRC2	CLKSRC3	CLKSRC4
A	CLK_SRC[1] (drives GCLK1/7)	CLK_SRC[2] (drives GCLK2/8)	CLK_SRC[3] (drives GCLK3/9)	CLK_SRC[4] (drives GCLK4/10)
B	CLK_SRC[5] (drives GCLK5/11)	CLK_SRC[6] (drives GCLK6/12)	BC[0]	BD[0]
C	CD[0]	CD[1]	CD[2]	BC[0]
D	CD[0]	CD[1]	CD[2]	BD[0]

Table 1: FPGA Possible Clock Connections

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Figure 2: Illustration over FPGA Possible Clock Connections

Clock Interfaces

CLK LEFT and CLK RIGHT

CLK LEFT and CLK RIGHT are compatible with all existing clock cables and modules. Up to 12 clocks can be synchronized between 2-3 systems over these connectors.

CLK LEFT and CLK RIGHT can be used simultaneously and separately. One can be used to input clocks from a clock module, and the other to synchronize global clocks on this system with a second HAPS system.

External Clock I/Os

External clocks and legacy HAPS systems can be connected to HAPS-80 using the coax connectors in the clock panel. Signal levels are 2.5 V LVCMOS. Inputs are 50-Ohm terminated to 1.25 V. Outputs should be parallel terminated at the destination.

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GLK ExtIN	1-6	Sources for Global Clock nets
PLL1	IN	Reference input for PLL1
	OUT1	PLL1 outputs OUT1 and OUT2 have the same frequency.
	OUT2	
PLL2	IN	Reference input for PLL2
	OUT1	PLL2 outputs OUT1 and OUT 2 have the same frequency.
	OUT2	

Table 2: External Clock Interfaces

Figure 3: Clock Panel

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Clock Distribution Network

For each GCLK1-12, the clock distribution network selects one of the possible clock sources for distribution to all FPGAs, and also selects the output clocks that are passed to the clock connectors. It is designed to provide low-skew clocks to all FPGAs regardless of which clock source is selected and provide a means for passing low-skew clocks between systems.

Each global clock net is sourced by a distribution buffer that feeds all user FPGAs. (The buffers driving GCLK1 and GCLK4 also source the PLL feedback nets and the SYNC_OUT signals). The input to the buffer can be selected to come from one of the CLK connectors or a local clock.

The local clock is chosen from a PLL or an FPGA output through a crosspoint switch (labeled 4x4 in Figure 4 and Figure 5). As can be seen in the figures, GCLKn and GCLK(n+6) share the same crosspoint switch and the same clock sources. PLL1_OUT1 can feed GCLK1, GCLK7 or both, but not with different frequencies. The clock output connectors are also fed from the same crosspoint switch. As a result, GCLK1 can be sourced from any of PLL1_OUT1, GCLK_ExtIN[1], or CLK_SRC[1]. Likewise, CLK_LEFT_CLK_OUT1 can be independently sourced from any one of the same sources.

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Figure 4: Clock Distribution Network - PLL1

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Figure 5: Clock Distribution Network - PLL2

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Clock Stopping

Each FPGA has an output, CLKSTOPN, that can be driven low to stop GCLK12. Hardware stop-points can be created by adding assertions in the user design that pull the CLKSTOPN signal low and stops the user design or parts of it when a failure occurs. The design state can then be examined by accessing debug circuitry through the UMRBus or debug interfaces.

Clock gating is performed with an AND gate placed in front of the local distribution buffer for GCLK12, see gray box in Figure 6. The parts of the design that shouldn't be stopped can be clocked by GCLK6 if it is set to have the same source as GCLK12.

Figure 6: Clock Stopping with CLKSTOPN

The illustration above is a simplified figure. Although each FPGA can drive the CLKSTOPN, these signals are not physically connected and cannot be used as a global signal.

Notes:

- The FPGAs cannot use PLLs to deskew GCLK12.
- Only local FPGAs on the same HAPS-80 system are stopped. Clocks that are chained through the CLK connectors are unaffected.
- Beware of runt pulses if clocks are re-enabled after examining design state. To get predictable timing for CLKSTOPN, select the same clock source for GCLK6 and GCLK12, then use GCLK6 to control CLKSTOPN.
- Apply proper timing constraints to the CLKSTOPN outputs to allow for round-trip latency of 7.5 ns from the CLKSTOPN pin back to the FPGA clock input.

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Clock Synchronization

Direct Synchronization

Figure 7: Direct Clock Synchronization

Clocks can be synchronized across two systems using a CDE_CABLE80 connected from CLK RIGHT on the first system to CLK LEFT on the second.

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- First system: Select the same source for both GCLKn and CLK_RIGHT_CLK_OUTn.
- Second system: Select CLK_LEFT_CLK_INn to source GCLKn.

The clock GCLKn on the first system then drives GCLKn on the second.

The signal routes between the cross-point switch and the clock buffer on the first system are length matched to equal the delay in the CDE_CABLE80, resulting with only a small skew in the clock signal to all FPGAs in both systems.

A third system can be added by sending the clock to CLK_LEFT_CLK_OUTn from the first system to the CLK_RIGHT connector of the third system. The clock will enter the third system as CLK_RIGHT_CLK_INn in the CLK RIGHT connector and can be distributed there as GCLKn+6. When using
ProtoCompiler, the system files will keep track of the clock indices.

This method will work with intermittent, gated or stoppable clocks. Note that a CDE_CA-BLE80 connects clock signals both ways.

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Indirect Synchronization

Figure 8: Indirect Clock Synchronization

Systems can be synchronized with a technique that uses the on-board PLLs for deskewing. Using a CDE_CABLE80 connect the CLK RIGHT of the first system to the CLK LEFT of the second system. GCLK1 will be fed to SYNC_OUT1 in both clock connectors. When a cable is connected to another system's clock connector, it will arrive as SYNC_IN1, and can be selected to source PLL1. The cable lengths are matched so that the PLL input select switch receives the clock simultaneously as it arrives at the FPGAs on the first system.

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Configure the PLL on the newly added system to output at the same frequency on PLL1_1 as the incoming frequency. Set the distribution circuitry to feed GCLK1 from this PLL output. The clock distribution circuitry is length matched so that the PLL will strive to minimize the skew between the SYNC_IN1 and the FPGA clocks, making the clock arrive at the FPGAs on both systems simultaneously.

The added system can provide the synchronized GCLK1 as SYNC_OUT1, so the procedure can be repeated to synchronize up any number of systems.

A similar chain can be built using PLL2 and GCLK4. Only these two SYNC signals are available on each system, so fewer clocks can be synchronized in this way compared to the simple direct technique previously described.

When using PLLs for synchronization, the clocks must be continuous and within the input range of the PLLs.

Distributing Clock Hierarchies

The indirect method can be used to distribute clock hierarchies across any number of systems. This is accomplished by generating a set of related frequencies from the PLL on the first system in the chain. The second system will receive and synchronize GCLK1 as SYNC_IN1, as described in Indirect Synchronization and can recreate the related frequencies on its remaining outputs.

To avoid clock phase issues, distribute the lowest frequency clock as GCLK1 and use related frequencies as simple multiples of this base clock.

Controlling Global Clock Networks

PLL clock frequencies and routing in the clock distribution network are controlled by confprosh commands, see System Configuration Software Handbook under Software on HAPS SupportNet.

HAPS External Clock Distribution Board (HAPS-ECDB)

The HAPS® External Clock Distribution Board (HAPS-ECDB) extends direct synchronization of clocks to connect or interface up to six HAPS systems together. The HAPS-ECDB automatically replicates input clocks to the output clocks to support up to twelve clocks across six HAPS systems capable of supporting up to 288M ASIC gates.

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The HAPS-ECDB extends the HAPS clock circuitry with increased flexibility for various design clocking variations. It accepts six clock inputs each from two CLK connectors designated as master clocks. Each of the twelve incoming clocks are buffered and distributed to five slave CLK connectors and back to the master connectors.

For more information see the External Clock Distribution Board Reference Manual on SupportNet.

Figure 9: HAPS-ECDB

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CHAPTER 6

Getting Started

Remember that the HAPS-80 S104 system, as all electronic equipment, is sensitive to static discharge. Make sure that you're properly grounded whenever handling the system directly.

Special Instructions for Adding Daughter Boards and Cables

Daughter Boards and cables must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged. See

Be aware that connectors 16, 17, 18 and 19 in an FPGA module of a HAPS-80 system have pins that are not connected, two less clock capable pins, and are limited to 1.8V VCCO, see pg 28.

Connector J12 is a high-range connector, where 2.5V and 3.3V are possible to select for VCCO. J12 does not support HSTDM. For more information about HSTDM consult the Proto-Compiler User Guide.

Always consult with the daughter board's reference manual. Most daughter boards are powered through the HapsTrak connector, but some may need external power.

Important! Do not hot plug daughter boards and cables. Always power down the HAPS-80 system when adding or removing daughter boards and cables. There is a risk of damaging both the system and daughter board if this instruction is not followed.

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Work Flow

This guide will describe two types of high-level use modes:

- Desktop mode: The HAPS system is connected to a neighboring PC host, either through a UMRBus pod or through a USB cable.
- Network mode: The HAPS system is connected to a network using Ethernet and access through the system is done by a remote network connected user.

Desktop mode

Follow these basic steps to get your design up and running on the HAPS-80 system.

1. Mount daughter boards, cables and UMRBus.

With the HAPS system powered off, connect the required daughter boards, cables and UMRBus through USB or UMRBus pod according to your design. If external clocks are needed, use CDE80 cables with CLK LEFT and CLK RIGHT connectors or coax cables with the clock panel SMB connectors.

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2. Power on HAPS system

Connect the power supply to both 12 V terminals on the back side and enable power. When power is applied to the system there is a boot sequence which may take a few seconds. During this phase the LEDs will change colors at the end of the boot sequence all LEDs should be green.

3. System configuration

Configure the system (for example, setting clocks and voltages) and FPGA design according to the System Configuration Software Handbook and follow the instructions under Configuration, on page 56.

4. Use design

See the HAPS ProtoCompiler documentation.

5. Power down HAPS-80 system

To power down the system, simply power off the 12 V power supply.

To restart press the Reconfig button for 3 to 5 seconds. Performing a restart will empty the configuration memory and reload the configuration project from the SD card if present.

More Information

- If external clocks are needed, use CABLE_CDE70 cables with CLK LEFT/CLK RIGHT connectors or coax cables with the clock panel SMB connectors. See Clock Synchronization, on page 47.
- The FPGAs can be configured during powerup from an SD card. See Configuration, on page 56.
- The individual LEDs on each module, marked FPGA DONE indicate if the corresponding FPGA is configured. After a successful configuration the LEDs will be green. Ready, Reset, Power and Alert LEDs on front panel will be green if the Startup project was loaded successfully.
- Pressing the Reset button triggers a reset in each individual FPGA.
- To clear system, press the Reconfig button momentarily.
  - System is cleared

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  - HapsTrak connectors are set to off
  - FPGAs are cleared
  - Clocks are disabled

Network mode

This use mode is similar to the desktop mode described above, but with the following differences:

- Instead of connecting to the system directly through the UMRbus (PCIe or USB connected), the connection is done over Ethernet
- Powering on and off the system is done by the remote user through Confpro commands or the Confpro GUI.

By default, HAPS-80 systems are configured to automatically receive an IP address by a DHCP server. This setting, as well as other network related information, can be viewed and modified through the Confpro GUI under the settings option.

For more information about network use refer to the System Configuration Software Handbook.

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CHAPTER 7

Configuration

HAPS-80 FPGA devices can be configured using:

- SD Card
- UMRBus® over USB
- UMRBus® over Ethernet
- HAPS UMRBus® Interface Kit (sold separately)

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SD Card

- Supported: SD and SDHC cards
- Maximum Capacity: 32 GB
- Format: FAT32
- Performance: 25 s.
  (~2.5 seconds per FPGA using 1:5 bitstream compression)

There are three ways to configure the HAPS-80 using the SD card; manually, Conf.Sel. wheel, or with the autostart feature. See HAPS System User Guide for more information.

Configure Select Wheel

The Conf.Sel. wheel on the front panel selects a project saved on the SD Card during startup or when the Reconfig button is pushed from 3 to 5 seconds.

Autostart

The autorun file on the SD card will be used to configure the HAPS-80 system at reboot or restart.To load a project during autostart, the select wheel should be placed in the ‘0’ position. Autostart should only be used when configuring a HAPS-80 as a standalone system.

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UMRBus®

USB

Connect a USB cable to the host PC and the HAPS-80 system. Configure the system according to the System Configuration Software Handbook.

Ethernet

The HAPS-80 systems can be accessed remotely through the network connector using System Configuration Software.

Connect a network cable and power on the system. The system will request an IP address from the DHCP server. The host name of the system is a combination of the HAPS series and the serial number, for example, HAPS80-X000923.

Configure the system according to the System Configuration Software Handbook.

HAPS UMRBus® Interface Kit

The HAPS UMRBus (Universal Multi-Resource Bus) Interface Kit is a complete and reliable set of components that allow bidirectional data exchange between software and hardware. For more information see the HAPS UMRBus Interface Kit Handbook at solvnet.synopsys.com.

Reconfigure & Reset

Reconfigure

To clear the system, press the Reconfig button momentarily.

To restart press the Reconfig button for 3 to 5 seconds and release. Performing a restart will empty the configuration memory and reload the configuration project from the SD card.

Reset

Pressing the Reset button triggers a reset in each individual FPGA. Reset is not considered synchronous between FPGAs. Each FPGA has its own single FPGA reset for the user to use. There is no global reset.

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Synchronous Reset

Global reset does not exist in HAPS-80 systems (RESETn in prior HAPS systems), only local reset that is part of the System IP and controlled externally from Confpro. If your design has a global reset go to ‘Assigning and Distributing HAPS-80 Reset’ in the ProtoCompiler User Guide or go to the ‘Synchronous Reset in Multiple FPGAs” Application Note on HAPS SupportNet.

LED Behavior

User LEDs FPGA

LED	Color	Behavior
SU DONE	Green	Supervisor is configured.
USER_FPGA DONE	Green	FPGA is configured.
GPIO	Green	User defined
	Red	User defined

Front Panel

LED	Color	Behavior
Ready	Off	HAPS-80 off
	Green	Supervisor ready
	Amber	Supervisor Power Good
	Blinking Amber/ Green	The system is locked.
	Red	+12 V
Reset	Off	HAPS-80 off
	Green	Reset is released to each FPGA
	Red	Reset active

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LED	Color	Behavior
Power	Off	UFPGA power off
	Green	UFPGA power good
	Red	UFPGA power failure
Alert	Blinking Green	System configuration in progress.
	Green	No alert
	Red	Supervisor temperature over limit
SD Card	Green	SD Card available
	Amber	SD Card read/write activity

Front Panel - During Firmware Update

LED	Color
Ready	Blinking-Green/ Amber
Reset	Green
Power	Blinking Green
Alert	Blinking Green

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CHAPTER 8

System

Design Considerations

Reset Before Power Down

On rare occasions, your HAPS-80 system might report a power error if the FPGAs are being cleared while running a power consuming design or designs using multiple MGB connections. A good design rule to avoid an error under these circumstances is to reset the design before clearing the FPGAs.

High-range I/O Bank

Connector J12 is connected to a high-range I/O bank. Do not use J12 for DDR or similar applications requiring LVDS IO standard. HapsTrak 3 Signals, on page 29.

Limited HapsTrak Connectors

Connectors J16-J19 do not have two pins, D[11-12], and have a fixed 1.8VCC0. See HapsTrak 3 Signals, on page 29.

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SLR

HT3/SLR alignment in Xilinx US440 is different from LX2000T, hence when placing daughter boards with multiple HapsTrak 3 connectors it is preferable (in some cases mandatory, for example, DDR) to place the daughter boards so that they don't cross SLR boundaries. See SLR Regions, on page 30.

Reference Pins for DCI I/O Standards

In the HapsTrak 3 Standard, pages 11 and 19, state that a 100 Ohm pullup from VRN to VCCO and a 100 Ohm pulldown from VRP to GND is necessary if a daughter board requires a DCI standard. This is true for HAPS-70 systems, but NOT for HAPS-80 systems. A switch connected to VRP is activated by the Supervisor and no further measures are needed.

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System Dimensions

LxWxH Dimensions with Sides

LxWxH Dimensions without Sides

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Side Dimensions

Top Dimensions

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System Weight

13.83 kg (30.5 lbs) - without sides

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CHAPTER 9

Pin Tables, PCB-Trace Names and Delays

HapsTrak 3 Connectors, on page 67

Inter-FPGA Connections, on page 92

MGB1 PCB-Trace Names, on page 101

MGB2 PCB-Trace Names, on page 102

MGB Link PCB-Trace Names, on page 103

Clock PCB-Trace Names, on page 104

Virtual I/O Pin PCB-Trace Names, on page 105

System IP/UMRBus PCB-Trace Names, on page 106

PCB-Trace Delays, on page 107

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HapsTrak 3 Connectors

Pin Table Key:

Pin	Description
HT3	HapsTrak 3 Connector
SLR	Super Logic Region
GC	Global Clock
DBC QBC	Byte lane clock (Dedicated-Byte Clock and Quad-Byte Clock) input pin pairs are clock inputs directly driving source synchronous clocks to the bit slices in the I/O banks.
VRP	DCI voltage reference resistor pin

J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12 - HR Bank
J13
J14
J15
J16 - Limited
J17 - Limited
J18 - Limited
J19 - Limited
J20
J21
J22
J23
J24

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J1

HT3		XCVU440 - FLGA2892 SLR 2			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	C17	GC	73	A1_A[0]	B1_A[0]	C1_A[0]	D1_A[0]
A1	N	B17	GC	73	A1_A[1]	B1_A[1]	C1_A[1]	D1_A[1]
A2	P	A23		73	A1_A[2]	B1_A[2]	C1_A[2]	D1_A[2]
A3	N	A22		73	A1_A[3]	B1_A[3]	C1_A[3]	D1_A[3]
A4	P	C22		73	A1_A[4]	B1_A[4]	C1_A[4]	D1_A[4]
A5	N	B22		73	A1_A[5]	B1_A[5]	C1_A[5]	D1_A[5]
A6	P	B24	DBC	73	A1_A[6]	B1_A[6]	C1_A[6]	D1_A[6]
A7	N	A24	DBC	73	A1_A[7]	B1_A[7]	C1_A[7]	D1_A[7]
A8	P	D23		73	A1_A[8]	B1_A[8]	C1_A[8]	D1_A[8]
A9	N	C23		73	A1_A[9]	B1_A[9]	C1_A[9]	D1_A[9]
A10	P	D24		73	A1_A[10]	B1_A[10]	C1_A[10]	D1_A[10]
A11	N	C24		73	A1_A[11]	B1_A[11]	C1_A[11]	D1_A[11]
A12	-	D21		73	A1_A[12]	B1_A[12]	C1_A[12]	D1_A[12]
A13		NC						
B0	P	C19	GC_QBC	73	A1_B[0]	B1_B[0]	C1_B[0]	D1_B[0]
B1	N	C18	GC_QBC	73	A1_B[1]	B1_B[1]	C1_B[1]	D1_B[1]
B2	P	A18		73	A1_B[2]	B1_B[2]	C1_B[2]	D1_B[2]
B3	N	A17		73	A1_B[3]	B1_B[3]	C1_B[3]	D1_B[3]
B4	P	A20		73	A1_B[4]	B1_B[4]	C1_B[4]	D1_B[4]
B5	N	A19		73	A1_B[5]	B1_B[5]	C1_B[5]	D1_B[5]
B6	P	B20		73	A1_B[6]	B1_B[6]	C1_B[6]	D1_B[6]
B7	N	B19		73	A1_B[7]	B1_B[7]	C1_B[7]	D1_B[7]
B8	P	D20		73	A1_B[8]	B1_B[8]	C1_B[8]	D1_B[8]
B9	N	D19		73	A1_B[9]	B1_B[9]	C1_B[9]	D1_B[9]
B10	P	C21	DBC	73	A1_B[10]	B1_B[10]	C1_B[10]	D1_B[10]
B11	N	B21	DBC	73	A1_B[11]	B1_B[11]	C1_B[11]	D1_B[11]
B12		NC						
B13		NC						
C0	P	D16	GC	73	A1_C[0]	B1_C[0]	C1_C[0]	D1_C[0]
C1	N	D15	GC	73	A1_C[1]	B1_C[1]	C1_C[1]	D1_C[1]
C2	P	B15		73	A1_C[2]	B1_C[2]	C1_C[2]	D1_C[2]
C3	N	A15		73	A1_C[3]	B1_C[3]	C1_C[3]	D1_C[3]
C4	P	B14		73	A1_C[4]	B1_C[4]	C1_C[4]	D1_C[4]
C5	N	A14		73	A1_C[5]	B1_C[5]	C1_C[5]	D1_C[5]
C6	P	D13		73	A1_C[6]	B1_C[6]	C1_C[6]	D1_C[6]
C7	N	C13		73	A1_C[7]	B1_C[7]	C1_C[7]	D1_C[7]
C8	P	D14		73	A1_C[8]	B1_C[8]	C1_C[8]	D1_C[8]
C9	N	C14		73	A1_C[9]	B1_C[9]	C1_C[9]	D1_C[9]
C10	P	B10		73	A1_C[10]	B1_C[10]	C1_C[10]	D1_C[10]
C11	N	A10		73	A1_C[11]	B1_C[11]	C1_C[11]	D1_C[11]
C12		NC						
C13		NC						
D0	P	C16	GC	73	A1_D[0]	B1_D[0]	C1_D[0]	D1_D[0]
D1	N	B16	GC	73	A1_D[1]	B1_D[1]	C1_D[1]	D1_D[1]
D2	P	B12		73	A1_D[2]	B1_D[2]	C1_D[2]	D1_D[2]
D3	N	A12		73	A1_D[3]	B1_D[3]	C1_D[3]	D1_D[3]
D4	P	C12	DBC	73	A1_D[4]	B1_D[4]	C1_D[4]	D1_D[4]
D5	N	C11	DBC	73	A1_D[5]	B1_D[5]	C1_D[5]	D1_D[5]
D6	P	D11		73	A1_D[6]	B1_D[6]	C1_D[6]	D1_D[6]
D7	N	D10		73	A1_D[7]	B1_D[7]	C1_D[7]	D1_D[7]
D8	P	E11		73	A1_D[8]	B1_D[8]	C1_D[8]	D1_D[8]
D9	N	E10		73	A1_D[9]	B1_D[9]	C1_D[9]	D1_D[9]
D10	P	E13	DBC	73	A1_D[10]	B1_D[10]	C1_D[10]	D1_D[10]
D11	N	E12	DBC	73	A1_D[11]	B1_D[11]	C1_D[11]	D1_D[11]
D12	-	A13		73	A1_D[12]	B1_D[12]	C1_D[12]	D1_D[12]
D13		NC						
VRP	-	B11	VRP	73	A1_VRP	B1_VRP	C1_VRP	D1_VRP
VRN	-	D18		73	A1_VRN	B1_VRN	C1_VRN	D1_VRN

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J2

HT3		XCVU440 - FLGA2892 SLR 2			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	L22	GC	72	A2_A[0]	B2_A[0]	C2_A[0]	D2_A[0]
A1	N	K22	GC	72	A2_A[1]	B2_A[1]	C2_A[1]	D2_A[1]
A2	P	E26		72	A2_A[2]	B2_A[2]	C2_A[2]	D2_A[2]
A3	N	E25		72	A2_A[3]	B2_A[3]	C2_A[3]	D2_A[3]
A4	P	G24		72	A2_A[4]	B2_A[4]	C2_A[4]	D2_A[4]
A5	N	F24		72	A2_A[5]	B2_A[5]	C2_A[5]	D2_A[5]
A6	P	F23	DBC	72	A2_A[6]	B2_A[6]	C2_A[6]	D2_A[6]
A7	N	E23	DBC	72	A2_A[7]	B2_A[7]	C2_A[7]	D2_A[7]
A8	P	F22		72	A2_A[8]	B2_A[8]	C2_A[8]	D2_A[8]
A9	N	E22		72	A2_A[9]	B2_A[9]	C2_A[9]	D2_A[9]
A10	P	H22		72	A2_A[10]	B2_A[10]	C2_A[10]	D2_A[10]
A11	N	G22		72	A2_A[11]	B2_A[11]	C2_A[11]	D2_A[11]
A12	-	G26		72	A2_A[12]	B2_A[12]	C2_A[12]	D2_A[12]
A13		NC						
B0	P	L23	GC_QBC	72	A2_B[0]	B2_B[0]	C2_B[0]	D2_B[0]
B1	N	K23	GC_QBC	72	A2_B[1]	B2_B[1]	C2_B[1]	D2_B[1]
B2	P	J23		72	A2_B[2]	B2_B[2]	C2_B[2]	D2_B[2]
B3	N	H23		72	A2_B[3]	B2_B[3]	C2_B[3]	D2_B[3]
B4	P	J24		72	A2_B[4]	B2_B[4]	C2_B[4]	D2_B[4]
B5	N	H24		72	A2_B[5]	B2_B[5]	C2_B[5]	D2_B[5]
B6	P	K25		72	A2_B[6]	B2_B[6]	C2_B[6]	D2_B[6]
B7	N	J25		72	A2_B[7]	B2_B[7]	C2_B[7]	D2_B[7]
B8	P	J26		72	A2_B[8]	B2_B[8]	C2_B[8]	D2_B[8]
B9	N	H26		72	A2_B[9]	B2_B[9]	C2_B[9]	D2_B[9]
B10	P	G25	DBC	72	A2_B[10]	B2_B[10]	C2_B[10]	D2_B[10]
B11	N	F25	DBC	72	A2_B[11]	B2_B[11]	C2_B[11]	D2_B[11]
B12		NC						
B13		NC						
C0	P	N22	GC	72	A2_C[0]	B2_C[0]	C2_C[0]	D2_C[0]
C1	N	M22	GC	72	A2_C[1]	B2_C[1]	C2_C[1]	D2_C[1]
C2	P	R21		72	A2_C[2]	B2_C[2]	C2_C[2]	D2_C[2]
C3	N	P21		72	A2_C[3]	B2_C[3]	C2_C[3]	D2_C[3]
C4	P	P23		72	A2_C[4]	B2_C[4]	C2_C[4]	D2_C[4]
C5	N	N23		72	A2_C[5]	B2_C[5]	C2_C[5]	D2_C[5]
C6	P	M25		72	A2_C[6]	B2_C[6]	C2_C[6]	D2_C[6]
C7	N	L25		72	A2_C[7]	B2_C[7]	C2_C[7]	D2_C[7]
C8	P	P25		72	A2_C[8]	B2_C[8]	C2_C[8]	D2_C[8]
C9	N	P24		72	A2_C[9]	B2_C[9]	C2_C[9]	D2_C[9]
C10	P	T23		72	A2_C[10]	B2_C[10]	C2_C[10]	D2_C[10]
C11	N	R23		72	A2_C[11]	B2_C[11]	C2_C[11]	D2_C[11]
C12		NC						
C13		NC						
D0	P	N24	GC	72	A2_D[0]	B2_D[0]	C2_D[0]	D2_D[0]
D1	N	M24	GC	72	A2_D[1]	B2_D[1]	C2_D[1]	D2_D[1]
D2	P	U22		72	A2_D[2]	B2_D[2]	C2_D[2]	D2_D[2]
D3	N	T22		72	A2_D[3]	B2_D[3]	C2_D[3]	D2_D[3]
D4	P	V21	DBC	72	A2_D[4]	B2_D[4]	C2_D[4]	D2_D[4]
D5	N	U21	DBC	72	A2_D[5]	B2_D[5]	C2_D[5]	D2_D[5]
D6	P	V23		72	A2_D[6]	B2_D[6]	C2_D[6]	D2_D[6]
D7	N	V22		72	A2_D[7]	B2_D[7]	C2_D[7]	D2_D[7]
D8	P	U24		72	A2_D[8]	B2_D[8]	C2_D[8]	D2_D[8]
D9	N	T24		72	A2_D[9]	B2_D[9]	C2_D[9]	D2_D[9]
D10	P	U25	DBC	72	A2_D[10]	B2_D[10]	C2_D[10]	D2_D[10]
D11	N	T25	DBC	72	A2_D[11]	B2_D[11]	C2_D[11]	D2_D[11]
D12	-	R22		72	A2_D[12]	B2_D[12]	C2_D[12]	D2_D[12]
D13		NC						
VRP	-	R25	VRP	72	A2_VRP	B2_VRP	C2_VRP	D2_VRP
VRN	-	L24		72	A2_VRN	B2_VRN	C2_VRN	D2_VRN

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J3

HT3		XCVU440 - FLGA2892 SLR 2			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	L18	GC	71	A3_A[0]	B3_A[0]	C3_A[0]	D3_A[0]
A1	N	K18	GC	71	A3_A[1]	B3_A[1]	C3_A[1]	D3_A[1]
A2	P	F18		71	A3_A[2]	B3_A[2]	C3_A[2]	D3_A[2]
A3	N	F17		71	A3_A[3]	B3_A[3]	C3_A[3]	D3_A[3]
A4	P	E18		71	A3_A[4]	B3_A[4]	C3_A[4]	D3_A[4]
A5	N	E17		71	A3_A[5]	B3_A[5]	C3_A[5]	D3_A[5]
A6	P	G20	DBC	71	A3_A[6]	B3_A[6]	C3_A[6]	D3_A[6]
A7	N	G19	DBC	71	A3_A[7]	B3_A[7]	C3_A[7]	D3_A[7]
A8	P	F20		71	A3_A[8]	B3_A[8]	C3_A[8]	D3_A[8]
A9	N	F19		71	A3_A[9]	B3_A[9]	C3_A[9]	D3_A[9]
A10	P	E21		71	A3_A[10]	B3_A[10]	C3_A[10]	D3_A[10]
A11	N	E20		71	A3_A[11]	B3_A[11]	C3_A[11]	D3_A[11]
A12	-	G21		71	A3_A[12]	B3_A[12]	C3_A[12]	D3_A[12]
A13		NC						
B0	P	L17	GC_QBC	71	A3_B[0]	B3_B[0]	C3_B[0]	D3_B[0]
B1	N	K17	GC_QBC	71	A3_B[1]	B3_B[1]	C3_B[1]	D3_B[1]
B2	P	J18		71	A3_B[2]	B3_B[2]	C3_B[2]	D3_B[2]
B3	N	H18		71	A3_B[3]	B3_B[3]	C3_B[3]	D3_B[3]
B4	P	J19		71	A3_B[4]	B3_B[4]	C3_B[4]	D3_B[4]
B5	N	H19		71	A3_B[5]	B3_B[5]	C3_B[5]	D3_B[5]
B6	P	K20		71	A3_B[6]	B3_B[6]	C3_B[6]	D3_B[6]
B7	N	J20		71	A3_B[7]	B3_B[7]	C3_B[7]	D3_B[7]
B8	P	J21		71	A3_B[8]	B3_B[8]	C3_B[8]	D3_B[8]
B9	N	H21		71	A3_B[9]	B3_B[9]	C3_B[9]	D3_B[9]
B10	P	H17	DBC	71	A3_B[10]	B3_B[10]	C3_B[10]	D3_B[10]
B11	N	G17	DBC	71	A3_B[11]	B3_B[11]	C3_B[11]	D3_B[11]
B12		NC						
B13		NC						
C0	P	M20	GC	71	A3_C[0]	B3_C[0]	C3_C[0]	D3_C[0]
C1	N	L20	GC	71	A3_C[1]	B3_C[1]	C3_C[1]	D3_C[1]
C2	P	N21		71	A3_C[2]	B3_C[2]	C3_C[2]	D3_C[2]
C3	N	M21		71	A3_C[3]	B3_C[3]	C3_C[3]	D3_C[3]
C4	P	P19		71	A3_C[4]	B3_C[4]	C3_C[4]	D3_C[4]
C5	N	N19		71	A3_C[5]	B3_C[5]	C3_C[5]	D3_C[5]
C6	P	P18		71	A3_C[6]	B3_C[6]	C3_C[6]	D3_C[6]
C7	N	N18		71	A3_C[7]	B3_C[7]	C3_C[7]	D3_C[7]
C8	P	N17		71	A3_C[8]	B3_C[8]	C3_C[8]	D3_C[8]
C9	N	M17		71	A3_C[9]	B3_C[9]	C3_C[9]	D3_C[9]
C10	P	T20		71	A3_C[10]	B3_C[10]	C3_C[10]	D3_C[10]
C11	N	R20		71	A3_C[11]	B3_C[11]	C3_C[11]	D3_C[11]
C12		NC						
C13		NC						
D0	P	M19	GC	71	A3_D[0]	B3_D[0]	C3_D[0]	D3_D[0]
D1	N	L19	GC	71	A3_D[1]	B3_D[1]	C3_D[1]	D3_D[1]
D2	P	T19		71	A3_D[2]	B3_D[2]	C3_D[2]	D3_D[2]
D3	N	T18		71	A3_D[3]	B3_D[3]	C3_D[3]	D3_D[3]
D4	P	R18	DBC	71	A3_D[4]	B3_D[4]	C3_D[4]	D3_D[4]
D5	N	R17	DBC	71	A3_D[5]	B3_D[5]	C3_D[5]	D3_D[5]
D6	P	U17		71	A3_D[6]	B3_D[6]	C3_D[6]	D3_D[6]
D7	N	T17		71	A3_D[7]	B3_D[7]	C3_D[7]	D3_D[7]
D8	P	U20		71	A3_D[8]	B3_D[8]	C3_D[8]	D3_D[8]
D9	N	U19		71	A3_D[9]	B3_D[9]	C3_D[9]	D3_D[9]
D10	P	V18	DBC	71	A3_D[10]	B3_D[10]	C3_D[10]	D3_D[10]
D11	N	V17	DBC	71	A3_D[11]	B3_D[11]	C3_D[11]	D3_D[11]
D12	-	P20		71	A3_D[12]	B3_D[12]	C3_D[12]	D3_D[12]
D13		NC						
VRP	-	V16	VRP	71	A3_VRP	B3_VRP	C3_VRP	D3_VRP
VRN	-	K21		71	A3_VRN	B3_VRN	C3_VRN	D3_VRN

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J4

HT3		XCVU440 - FLGA2892 SLR 2			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	L13	GC	70	A4_A[0]	B4_A[0]	C4_A[0]	D4_A[0]
A1	N	K13	GC	70	A4_A[1]	B4_A[1]	C4_A[1]	D4_A[1]
A2	P	H12		70	A4_A[2]	B4_A[2]	C4_A[2]	D4_A[2]
A3	N	G12		70	A4_A[3]	B4_A[3]	C4_A[3]	D4_A[3]
A4	P	F13		70	A4_A[4]	B4_A[4]	C4_A[4]	D4_A[4]
A5	N	F12		70	A4_A[5]	B4_A[5]	C4_A[5]	D4_A[5]
A6	P	G15	DBC	70	A4_A[6]	B4_A[6]	C4_A[6]	D4_A[6]
A7	N	G14	DBC	70	A4_A[7]	B4_A[7]	C4_A[7]	D4_A[7]
A8	P	F15		70	A4_A[8]	B4_A[8]	C4_A[8]	D4_A[8]
A9	N	F14		70	A4_A[9]	B4_A[9]	C4_A[9]	D4_A[9]
A10	P	E16		70	A4_A[10]	B4_A[10]	C4_A[10]	D4_A[10]
A11	N	E15		70	A4_A[11]	B4_A[11]	C4_A[11]	D4_A[11]
A12	-	G16		70	A4_A[12]	B4_A[12]	C4_A[12]	D4_A[12]
A13		NC						
B0	P	L15	GC_QBC	70	A4_B[0]	B4_B[0]	C4_B[0]	D4_B[0]
B1	N	L14	GC_QBC	70	A4_B[1]	B4_B[1]	C4_B[1]	D4_B[1]
B2	P	L12		70	A4_B[2]	B4_B[2]	C4_B[2]	D4_B[2]
B3	N	K12		70	A4_B[3]	B4_B[3]	C4_B[3]	D4_B[3]
B4	P	J14		70	A4_B[4]	B4_B[4]	C4_B[4]	D4_B[4]
B5	N	J13		70	A4_B[5]	B4_B[5]	C4_B[5]	D4_B[5]
B6	P	K15		70	A4_B[6]	B4_B[6]	C4_B[6]	D4_B[6]
B7	N	J15		70	A4_B[7]	B4_B[7]	C4_B[7]	D4_B[7]
B8	P	K16		70	A4_B[8]	B4_B[8]	C4_B[8]	D4_B[8]
B9	N	J16		70	A4_B[9]	B4_B[9]	C4_B[9]	D4_B[9]
B10	P	H14	DBC	70	A4_B[10]	B4_B[10]	C4_B[10]	D4_B[10]
B11	N	H13	DBC	70	A4_B[11]	B4_B[11]	C4_B[11]	D4_B[11]
B12		NC						
B13		NC						
C0	P	M16	GC	70	A4_C[0]	B4_C[0]	C4_C[0]	D4_C[0]
C1	N	M15	GC	70	A4_C[1]	B4_C[1]	C4_C[1]	D4_C[1]
C2	P	N12		70	A4_C[2]	B4_C[2]	C4_C[2]	D4_C[2]
C3	N	M12		70	A4_C[3]	B4_C[3]	C4_C[3]	D4_C[3]
C4	P	P13		70	A4_C[4]	B4_C[4]	C4_C[4]	D4_C[4]
C5	N	N13		70	A4_C[5]	B4_C[5]	C4_C[5]	D4_C[5]
C6	P	P15		70	A4_C[6]	B4_C[6]	C4_C[6]	D4_C[6]
C7	N	P14		70	A4_C[7]	B4_C[7]	C4_C[7]	D4_C[7]
C8	P	P16		70	A4_C[8]	B4_C[8]	C4_C[8]	D4_C[8]
C9	N	N16		70	A4_C[9]	B4_C[9]	C4_C[9]	D4_C[9]
C10	P	R16		70	A4_C[10]	B4_C[10]	C4_C[10]	D4_C[10]
C11	N	R15		70	A4_C[11]	B4_C[11]	C4_C[11]	D4_C[11]
C12		NC						
C13		NC						
D0	P	N14	GC	70	A4_D[0]	B4_D[0]	C4_D[0]	D4_D[0]
D1	N	M14	GC	70	A4_D[1]	B4_D[1]	C4_D[1]	D4_D[1]
D2	P	U15		70	A4_D[2]	B4_D[2]	C4_D[2]	D4_D[2]
D3	N	T15		70	A4_D[3]	B4_D[3]	C4_D[3]	D4_D[3]
D4	P	T13	DBC	70	A4_D[4]	B4_D[4]	C4_D[4]	D4_D[4]
D5	N	R13	DBC	70	A4_D[5]	B4_D[5]	C4_D[5]	D4_D[5]
D6	P	U14		70	A4_D[6]	B4_D[6]	C4_D[6]	D4_D[6]
D7	N	T14		70	A4_D[7]	B4_D[7]	C4_D[7]	D4_D[7]
D8	P	U12		70	A4_D[8]	B4_D[8]	C4_D[8]	D4_D[8]
D9	N	T12		70	A4_D[9]	B4_D[9]	C4_D[9]	D4_D[9]
D10	P	V13	DBC	70	A4_D[10]	B4_D[10]	C4_D[10]	D4_D[10]
D11	N	V12	DBC	70	A4_D[11]	B4_D[11]	C4_D[11]	D4_D[11]
D12	-	R12		70	A4_D[12]	B4_D[12]	C4_D[12]	D4_D[12]
D13		NC						
VRP	-	U16	VRP	70	A4_VRP	B4_VRP	C4_VRP	D4_VRP
VRN	-	H16		70	A4_VRN	B4_VRN	C4_VRN	D4_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BE42	GC	68	A5_A[0]	B5_A[0]	C5_A[0]	D5_A[0]
A1	N	BF42	GC	68	A5_A[1]	B5_A[1]	C5_A[1]	D5_A[1]
A2	P	BA40		68	A5_A[2]	B5_A[2]	C5_A[2]	D5_A[2]
A3	N	BB40		68	A5_A[3]	B5_A[3]	C5_A[3]	D5_A[3]
A4	P	BB41		68	A5_A[4]	B5_A[4]	C5_A[4]	D5_A[4]
A5	N	BC41		68	A5_A[5]	B5_A[5]	C5_A[5]	D5_A[5]
A6	P	BB42	DBC	68	A5_A[6]	B5_A[6]	C5_A[6]	D5_A[6]
A7	N	BC42	DBC	68	A5_A[7]	B5_A[7]	C5_A[7]	D5_A[7]
A8	P	BA42		68	A5_A[8]	B5_A[8]	C5_A[8]	D5_A[8]
A9	N	BA43		68	A5_A[9]	B5_A[9]	C5_A[9]	D5_A[9]
A10	P	AY41		68	A5_A[10]	B5_A[10]	C5_A[10]	D5_A[10]
A11	N	AY42		68	A5_A[11]	B5_A[11]	C5_A[11]	D5_A[11]
A12	-	BC39		68	A5_A[12]	B5_A[12]	C5_A[12]	D5_A[12]
A13		NC						
B0	P	BD41	GC_QBC	68	A5_B[0]	B5_B[0]	C5_B[0]	D5_B[0]
B1	N	BE41	GC_QBC	68	A5_B[1]	B5_B[1]	C5_B[1]	D5_B[1]
B2	P	BE40		68	A5_B[2]	B5_B[2]	C5_B[2]	D5_B[2]
B3	N	BF40		68	A5_B[3]	B5_B[3]	C5_B[3]	D5_B[3]
B4	P	BD39		68	A5_B[4]	B5_B[4]	C5_B[4]	D5_B[4]
B5	N	BD40		68	A5_B[5]	B5_B[5]	C5_B[5]	D5_B[5]
B6	P	BD43		68	A5_B[6]	B5_B[6]	C5_B[6]	D5_B[6]
B7	N	BE43		68	A5_B[7]	B5_B[7]	C5_B[7]	D5_B[7]
B8	P	BC43		68	A5_B[8]	B5_B[8]	C5_B[8]	D5_B[8]
B9	N	BD44		68	A5_B[9]	B5_B[9]	C5_B[9]	D5_B[9]
B10	P	BA39	DBC	68	A5_B[10]	B5_B[10]	C5_B[10]	D5_B[10]
B11	N	BB39	DBC	68	A5_B[11]	B5_B[11]	C5_B[11]	D5_B[11]
B12		NC						
B13		NC						
C0	P	BG41	GC	68	A5_C[0]	B5_C[0]	C5_C[0]	D5_C[0]
C1	N	BH41	GC	68	A5_C[1]	B5_C[1]	C5_C[1]	D5_C[1]
C2	P	BG39		68	A5_C[2]	B5_C[2]	C5_C[2]	D5_C[2]
C3	N	BG40		68	A5_C[3]	B5_C[3]	C5_C[3]	D5_C[3]
C4	P	BH39		68	A5_C[4]	B5_C[4]	C5_C[4]	D5_C[4]
C5	N	BJ39		68	A5_C[5]	B5_C[5]	C5_C[5]	D5_C[5]
C6	P	BJ40		68	A5_C[6]	B5_C[6]	C5_C[6]	D5_C[6]
C7	N	BK40		68	A5_C[7]	B5_C[7]	C5_C[7]	D5_C[7]
C8	P	BJ38		68	A5_C[8]	B5_C[8]	C5_C[8]	D5_C[8]
C9	N	BK38		68	A5_C[9]	B5_C[9]	C5_C[9]	D5_C[9]
C10	P	BF43		68	A5_C[10]	B5_C[10]	C5_C[10]	D5_C[10]
C11	N	BF44		68	A5_C[11]	B5_C[11]	C5_C[11]	D5_C[11]
C12		NC						
C13		NC						
D0	P	BG42	GC	68	A5_D[0]	B5_D[0]	C5_D[0]	D5_D[0]
D1	N	BH42	GC	68	A5_D[1]	B5_D[1]	C5_D[1]	D5_D[1]
D2	P	BG44		68	A5_D[2]	B5_D[2]	C5_D[2]	D5_D[2]
D3	N	BG45		68	A5_D[3]	B5_D[3]	C5_D[3]	D5_D[3]
D4	P	BH43	DBC	68	A5_D[4]	B5_D[4]	C5_D[4]	D5_D[4]
D5	N	BH44	DBC	68	A5_D[5]	B5_D[5]	C5_D[5]	D5_D[5]
D6	P	BJ43		68	A5_D[6]	B5_D[6]	C5_D[6]	D5_D[6]
D7	N	BJ44		68	A5_D[7]	B5_D[7]	C5_D[7]	D5_D[7]
D8	P	BJ45		68	A5_D[8]	B5_D[8]	C5_D[8]	D5_D[8]
D9	N	BK45		68	A5_D[9]	B5_D[9]	C5_D[9]	D5_D[9]
D10	P	BK41	DBC	68	A5_D[10]	B5_D[10]	C5_D[10]	D5_D[10]
D11	N	BK42	DBC	68	A5_D[11]	B5_D[11]	C5_D[11]	D5_D[11]
D12	-	BJ41		68	A5_D[12]	B5_D[12]	C5_D[12]	D5_D[12]
D13		NC						
VRP	-	BK43	VRP	68	A5_VRP	B5_VRP	C5_VRP	D5_VRP
VRN	-	BF39		68	A5_VRN	B5_VRN	C5_VRN	D5_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	AY38	GC	67	A6_A[0]	B6_A[0]	C6_A[0]	D6_A[0]
A1	N	BA38	GC	67	A6_A[1]	B6_A[1]	C6_A[1]	D6_A[1]
A2	P	AU36		67	A6_A[2]	B6_A[2]	C6_A[2]	D6_A[2]
A3	N	AV36		67	A6_A[3]	B6_A[3]	C6_A[3]	D6_A[3]
A4	P	AU37		67	A6_A[4]	B6_A[4]	C6_A[4]	D6_A[4]
A5	N	AV37		67	A6_A[5]	B6_A[5]	C6_A[5]	D6_A[5]
A6	P	AV38	DBC	67	A6_A[6]	B6_A[6]	C6_A[6]	D6_A[6]
A7	N	AV39	DBC	67	A6_A[7]	B6_A[7]	C6_A[7]	D6_A[7]
A8	P	AT39		67	A6_A[8]	B6_A[8]	C6_A[8]	D6_A[8]
A9	N	AU39		67	A6_A[9]	B6_A[9]	C6_A[9]	D6_A[9]
A10	P	AT40		67	A6_A[10]	B6_A[10]	C6_A[10]	D6_A[10]
A11	N	AU40		67	A6_A[11]	B6_A[11]	C6_A[11]	D6_A[11]
A12	-	AT38		67	A6_A[12]	B6_A[12]	C6_A[12]	D6_A[12]
A13		NC						
B0	P	AY37	GC_QBC	67	A6_B[0]	B6_B[0]	C6_B[0]	D6_B[0]
B1	N	BA37	GC_QBC	67	A6_B[1]	B6_B[1]	C6_B[1]	D6_B[1]
B2	P	AW36		67	A6_B[2]	B6_B[2]	C6_B[2]	D6_B[2]
B3	N	AY36		67	A6_B[3]	B6_B[3]	C6_B[3]	D6_B[3]
B4	P	AW35		67	A6_B[4]	B6_B[4]	C6_B[4]	D6_B[4]
B5	N	AY35		67	A6_B[5]	B6_B[5]	C6_B[5]	D6_B[5]
B6	P	BA35		67	A6_B[6]	B6_B[6]	C6_B[6]	D6_B[6]
B7	N	BB35		67	A6_B[7]	B6_B[7]	C6_B[7]	D6_B[7]
B8	P	AW38		67	A6_B[8]	B6_B[8]	C6_B[8]	D6_B[8]
B9	N	AW39		67	A6_B[9]	B6_B[9]	C6_B[9]	D6_B[9]
B10	P	AT35	DBC	67	A6_B[10]	B6_B[10]	C6_B[10]	D6_B[10]
B11	N	AU35	DBC	67	A6_B[11]	B6_B[11]	C6_B[11]	D6_B[11]
B12		NC						
B13		NC						
C0	P	BB37	GC	67	A6_C[0]	B6_C[0]	C6_C[0]	D6_C[0]
C1	N	BC37	GC	67	A6_C[1]	B6_C[1]	C6_C[1]	D6_C[1]
C2	P	BC38		67	A6_C[2]	B6_C[2]	C6_C[2]	D6_C[2]
C3	N	BD38		67	A6_C[3]	B6_C[3]	C6_C[3]	D6_C[3]
C4	P	BD35		67	A6_C[4]	B6_C[4]	C6_C[4]	D6_C[4]
C5	N	BD36		67	A6_C[5]	B6_C[5]	C6_C[5]	D6_C[5]
C6	P	BE36		67	A6_C[6]	B6_C[6]	C6_C[6]	D6_C[6]
C7	N	BE37		67	A6_C[7]	B6_C[7]	C6_C[7]	D6_C[7]
C8	P	BE35		67	A6_C[8]	B6_C[8]	C6_C[8]	D6_C[8]
C9	N	BF35		67	A6_C[9]	B6_C[9]	C6_C[9]	D6_C[9]
C10	P	BF37		67	A6_C[10]	B6_C[10]	C6_C[10]	D6_C[10]
C11	N	BF38		67	A6_C[11]	B6_C[11]	C6_C[11]	D6_C[11]
C12		NC						
C13		NC						
D0	P	BB36	GC	67	A6_D[0]	B6_D[0]	C6_D[0]	D6_D[0]
D1	N	BC36	GC	67	A6_D[1]	B6_D[1]	C6_D[1]	D6_D[1]
D2	P	BG36		67	A6_D[2]	B6_D[2]	C6_D[2]	D6_D[2]
D3	N	BG37		67	A6_D[3]	B6_D[3]	C6_D[3]	D6_D[3]
D4	P	BH37	DBC	67	A6_D[4]	B6_D[4]	C6_D[4]	D6_D[4]
D5	N	BH38	DBC	67	A6_D[5]	B6_D[5]	C6_D[5]	D6_D[5]
D6	P	BH36		67	A6_D[6]	B6_D[6]	C6_D[6]	D6_D[6]
D7	N	BJ36		67	A6_D[7]	B6_D[7]	C6_D[7]	D6_D[7]
D8	P	BK36		67	A6_D[8]	B6_D[8]	C6_D[8]	D6_D[8]
D9	N	BK37		67	A6_D[9]	B6_D[9]	C6_D[9]	D6_D[9]
D10	P	BJ35	DBC	67	A6_D[10]	B6_D[10]	C6_D[10]	D6_D[10]
D11	N	BK35	DBC	67	A6_D[11]	B6_D[11]	C6_D[11]	D6_D[11]
D12	-	BE38		67	A6_D[12]	B6_D[12]	C6_D[12]	D6_D[12]
D13		NC						
VRP	-	BG35	VRP	67	A6_VRP	B6_VRP	C6_VRP	D6_VRP
VRN	-	AW40		67	A6_VRN	B6_VRN	C6_VRN	D6_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	AY33	GC	66	A7_A[0]	B7_A[0]	C7_A[0]	D7_A[0]
A1	N	BA33	GC	66	A7_A[1]	B7_A[1]	C7_A[1]	D7_A[1]
A2	P	AV31		66	A7_A[2]	B7_A[2]	C7_A[2]	D7_A[2]
A3	N	AW31		66	A7_A[3]	B7_A[3]	C7_A[3]	D7_A[3]
A4	P	AU31		66	A7_A[4]	B7_A[4]	C7_A[4]	D7_A[4]
A5	N	AU32		66	A7_A[5]	B7_A[5]	C7_A[5]	D7_A[5]
A6	P	AV32	DBC	66	A7_A[6]	B7_A[6]	C7_A[6]	D7_A[6]
A7	N	AV33	DBC	66	A7_A[7]	B7_A[7]	C7_A[7]	D7_A[7]
A8	P	AU34		66	A7_A[8]	B7_A[8]	C7_A[8]	D7_A[8]
A9	N	AV34		66	A7_A[9]	B7_A[9]	C7_A[9]	D7_A[9]
A10	P	AT33		66	A7_A[10]	B7_A[10]	C7_A[10]	D7_A[10]
A11	N	AT34		66	A7_A[11]	B7_A[11]	C7_A[11]	D7_A[11]
A12	-	AW30		66	A7_A[12]	B7_A[12]	C7_A[12]	D7_A[12]
A13		NC						
B0	P	BA32	GC_QBC	66	A7_B[0]	B7_B[0]	C7_B[0]	D7_B[0]
B1	N	BB32	GC_QBC	66	A7_B[1]	B7_B[1]	C7_B[1]	D7_B[1]
B2	P	BB31		66	A7_B[2]	B7_B[2]	C7_B[2]	D7_B[2]
B3	N	BC31		66	A7_B[3]	B7_B[3]	C7_B[3]	D7_B[3]
B4	P	AY31		66	A7_B[4]	B7_B[4]	C7_B[4]	D7_B[4]
B5	N	AY32		66	A7_B[5]	B7_B[5]	C7_B[5]	D7_B[5]
B6	P	BA34		66	A7_B[6]	B7_B[6]	C7_B[6]	D7_B[6]
B7	N	BB34		66	A7_B[7]	B7_B[7]	C7_B[7]	D7_B[7]
B8	P	AW33		66	A7_B[8]	B7_B[8]	C7_B[8]	D7_B[8]
B9	N	AW34		66	A7_B[9]	B7_B[9]	C7_B[9]	D7_B[9]
B10	P	AT30	DBC	66	A7_B[10]	B7_B[10]	C7_B[10]	D7_B[10]
B11	N	AU30	DBC	66	A7_B[11]	B7_B[11]	C7_B[11]	D7_B[11]
B12		NC						
B13		NC						
C0	P	BC32	GC	66	A7_C[0]	B7_C[0]	C7_C[0]	D7_C[0]
C1	N	BC33	GC	66	A7_C[1]	B7_C[1]	C7_C[1]	D7_C[1]
C2	P	BC34		66	A7_C[2]	B7_C[2]	C7_C[2]	D7_C[2]
C3	N	BD34		66	A7_C[3]	B7_C[3]	C7_C[3]	D7_C[3]
C4	P	BF33		66	A7_C[4]	B7_C[4]	C7_C[4]	D7_C[4]
C5	N	BF34		66	A7_C[5]	B7_C[5]	C7_C[5]	D7_C[5]
C6	P	BE32		66	A7_C[6]	B7_C[6]	C7_C[6]	D7_C[6]
C7	N	BF32		66	A7_C[7]	B7_C[7]	C7_C[7]	D7_C[7]
C8	P	BD31		66	A7_C[8]	B7_C[8]	C7_C[8]	D7_C[8]
C9	N	BE31		66	A7_C[9]	B7_C[9]	C7_C[9]	D7_C[9]
C10	P	BG34		66	A7_C[10]	B7_C[10]	C7_C[10]	D7_C[10]
C11	N	BH34		66	A7_C[11]	B7_C[11]	C7_C[11]	D7_C[11]
C12		NC						
C13		NC						
D0	P	BD33	GC	66	A7_D[0]	B7_D[0]	C7_D[0]	D7_D[0]
D1	N	BE33	GC	66	A7_D[1]	B7_D[1]	C7_D[1]	D7_D[1]
D2	P	BJ33		66	A7_D[2]	B7_D[2]	C7_D[2]	D7_D[2]
D3	N	BJ34		66	A7_D[3]	B7_D[3]	C7_D[3]	D7_D[3]
D4	P	BH32	DBC	66	A7_D[4]	B7_D[4]	C7_D[4]	D7_D[4]
D5	N	BH33	DBC	66	A7_D[5]	B7_D[5]	C7_D[5]	D7_D[5]
D6	P	BH31		66	A7_D[6]	B7_D[6]	C7_D[6]	D7_D[6]
D7	N	BJ31		66	A7_D[7]	B7_D[7]	C7_D[7]	D7_D[7]
D8	P	BK32		66	A7_D[8]	B7_D[8]	C7_D[8]	D7_D[8]
D9	N	BK33		66	A7_D[9]	B7_D[9]	C7_D[9]	D7_D[9]
D10	P	BK30	DBC	66	A7_D[10]	B7_D[10]	C7_D[10]	D7_D[10]
D11	N	BK31	DBC	66	A7_D[11]	B7_D[11]	C7_D[11]	D7_D[11]
D12	-	BG31		66	A7_D[12]	B7_D[12]	C7_D[12]	D7_D[12]
D13		NC						
VRP	-	BG32	VRP	66	A7_VRP	B7_VRP	C7_VRP	D7_VRP
VRN	-	AY30		66	A7_VRN	B7_VRN	C7_VRN	D7_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BA14	GC	63	A8_A[0]	B8_A[0]	C8_A[0]	D8_A[0]
A1	N	BB14	GC	63	A8_A[1]	B8_A[1]	C8_A[1]	D8_A[1]
A2	P	AV14		63	A8_A[2]	B8_A[2]	C8_A[2]	D8_A[2]
A3	N	AW14		63	A8_A[3]	B8_A[3]	C8_A[3]	D8_A[3]
A4	P	AV13		63	A8_A[4]	B8_A[4]	C8_A[4]	D8_A[4]
A5	N	AW13		63	A8_A[5]	B8_A[5]	C8_A[5]	D8_A[5]
A6	P	AT12	DBC	63	A8_A[6]	B8_A[6]	C8_A[6]	D8_A[6]
A7	N	AU12	DBC	63	A8_A[7]	B8_A[7]	C8_A[7]	D8_A[7]
A8	P	AT14		63	A8_A[8]	B8_A[8]	C8_A[8]	D8_A[8]
A9	N	AU14		63	A8_A[9]	B8_A[9]	C8_A[9]	D8_A[9]
A10	P	AT15		63	A8_A[10]	B8_A[10]	C8_A[10]	D8_A[10]
A11	N	AU15		63	A8_A[11]	B8_A[11]	C8_A[11]	D8_A[11]
A12	-	AV12		63	A8_A[12]	B8_A[12]	C8_A[12]	D8_A[12]
A13		NC						
B0	P	BA15	GC_QBC	63	A8_B[0]	B8_B[0]	C8_B[0]	D8_B[0]
B1	N	BB15	GC_QBC	63	A8_B[1]	B8_B[1]	C8_B[1]	D8_B[1]
B2	P	AW15		63	A8_B[2]	B8_B[2]	C8_B[2]	D8_B[2]
B3	N	AY15		63	A8_B[3]	B8_B[3]	C8_B[3]	D8_B[3]
B4	P	AW16		63	A8_B[4]	B8_B[4]	C8_B[4]	D8_B[4]
B5	N	AY16		63	A8_B[5]	B8_B[5]	C8_B[5]	D8_B[5]
B6	P	AY13		63	A8_B[6]	B8_B[6]	C8_B[6]	D8_B[6]
B7	N	BA13		63	A8_B[7]	B8_B[7]	C8_B[7]	D8_B[7]
B8	P	AY12		63	A8_B[8]	B8_B[8]	C8_B[8]	D8_B[8]
B9	N	BA12		63	A8_B[9]	B8_B[9]	C8_B[9]	D8_B[9]
B10	P	AU16	DBC	63	A8_B[10]	B8_B[10]	C8_B[10]	D8_B[10]
B11	N	AV16	DBC	63	A8_B[11]	B8_B[11]	C8_B[11]	D8_B[11]
B12		NC						
B13		NC						
C0	P	BC14	GC	63	A8_C[0]	B8_C[0]	C8_C[0]	D8_C[0]
C1	N	BC13	GC	63	A8_C[1]	B8_C[1]	C8_C[1]	D8_C[1]
C2	P	BB12		63	A8_C[2]	B8_C[2]	C8_C[2]	D8_C[2]
C3	N	BC12		63	A8_C[3]	B8_C[3]	C8_C[3]	D8_C[3]
C4	P	BE13		63	A8_C[4]	B8_C[4]	C8_C[4]	D8_C[4]
C5	N	BE12		63	A8_C[5]	B8_C[5]	C8_C[5]	D8_C[5]
C6	P	BF13		63	A8_C[6]	B8_C[6]	C8_C[6]	D8_C[6]
C7	N	BF12		63	A8_C[7]	B8_C[7]	C8_C[7]	D8_C[7]
C8	P	BD15		63	A8_C[8]	B8_C[8]	C8_C[8]	D8_C[8]
C9	N	BE15		63	A8_C[9]	B8_C[9]	C8_C[9]	D8_C[9]
C10	P	BF15		63	A8_C[10]	B8_C[10]	C8_C[10]	D8_C[10]
C11	N	BG15		63	A8_C[11]	B8_C[11]	C8_C[11]	D8_C[11]
C12		NC						
C13		NC						
D0	P	BD14	GC	63	A8_D[0]	B8_D[0]	C8_D[0]	D8_D[0]
D1	N	BD13	GC	63	A8_D[1]	B8_D[1]	C8_D[1]	D8_D[1]
D2	P	BG14		63	A8_D[2]	B8_D[2]	C8_D[2]	D8_D[2]
D3	N	BH14		63	A8_D[3]	B8_D[3]	C8_D[3]	D8_D[3]
D4	P	BG12	DBC	63	A8_D[4]	B8_D[4]	C8_D[4]	D8_D[4]
D5	N	BH12	DBC	63	A8_D[5]	B8_D[5]	C8_D[5]	D8_D[5]
D6	P	BH13		63	A8_D[6]	B8_D[6]	C8_D[6]	D8_D[6]
D7	N	BJ13		63	A8_D[7]	B8_D[7]	C8_D[7]	D8_D[7]
D8	P	BJ15		63	A8_D[8]	B8_D[8]	C8_D[8]	D8_D[8]
D9	N	BJ14		63	A8_D[9]	B8_D[9]	C8_D[9]	D8_D[9]
D10	P	BH11	DBC	63	A8_D[10]	B8_D[10]	C8_D[10]	D8_D[10]
D11	N	BJ11	DBC	63	A8_D[11]	B8_D[11]	C8_D[11]	D8_D[11]
D12	-	BF14		63	A8_D[12]	B8_D[12]	C8_D[12]	D8_D[12]
D13		NC						
VRP	-	BJ10	VRP	63	A8_VRP	B8_VRP	C8_VRP	D8_VRP
VRN	-	BB16		63	A8_VRN	B8_VRN	C8_VRN	D8_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BC19	GC	62	A9_A[0]	B9_A[0]	C9_A[0]	D9_A[0]
A1	N	BC18	GC	62	A9_A[1]	B9_A[1]	C9_A[1]	D9_A[1]
A2	P	AV19		62	A9_A[2]	B9_A[2]	C9_A[2]	D9_A[2]
A3	N	AW19		62	A9_A[3]	B9_A[3]	C9_A[3]	D9_A[3]
A4	P	AV18		62	A9_A[4]	B9_A[4]	C9_A[4]	D9_A[4]
A5	N	AW18		62	A9_A[5]	B9_A[5]	C9_A[5]	D9_A[5]
A6	P	AT17	DBC	62	A9_A[6]	B9_A[6]	C9_A[6]	D9_A[6]
A7	N	AU17	DBC	62	A9_A[7]	B9_A[7]	C9_A[7]	D9_A[7]
A8	P	AT19		62	A9_A[8]	B9_A[8]	C9_A[8]	D9_A[8]
A9	N	AU19		62	A9_A[9]	B9_A[9]	C9_A[9]	D9_A[9]
A10	P	AT20		62	A9_A[10]	B9_A[10]	C9_A[10]	D9_A[10]
A11	N	AU20		62	A9_A[11]	B9_A[11]	C9_A[11]	D9_A[11]
A12	-	AV17		62	A9_A[12]	B9_A[12]	C9_A[12]	D9_A[12]
A13		NC						
B0	P	BA19	GC_QBC	62	A9_B[0]	B9_B[0]	C9_B[0]	D9_B[0]
B1	N	BB19	GC_QBC	62	A9_B[1]	B9_B[1]	C9_B[1]	D9_B[1]
B2	P	BA20		62	A9_B[2]	B9_B[2]	C9_B[2]	D9_B[2]
B3	N	BB20		62	A9_B[3]	B9_B[3]	C9_B[3]	D9_B[3]
B4	P	AY17		62	A9_B[4]	B9_B[4]	C9_B[4]	D9_B[4]
B5	N	BA17		62	A9_B[5]	B9_B[5]	C9_B[5]	D9_B[5]
B6	P	AY18		62	A9_B[6]	B9_B[6]	C9_B[6]	D9_B[6]
B7	N	BA18		62	A9_B[7]	B9_B[7]	C9_B[7]	D9_B[7]
B8	P	AW20		62	A9_B[8]	B9_B[8]	C9_B[8]	D9_B[8]
B9	N	AY20		62	A9_B[9]	B9_B[9]	C9_B[9]	D9_B[9]
B10	P	AU21	DBC	62	A9_B[10]	B9_B[10]	C9_B[10]	D9_B[10]
B11	N	AV21	DBC	62	A9_B[11]	B9_B[11]	C9_B[11]	D9_B[11]
B12		NC						
B13		NC						
C0	P	BD20	GC	62	A9_C[0]	B9_C[0]	C9_C[0]	D9_C[0]
C1	N	BD19	GC	62	A9_C[1]	B9_C[1]	C9_C[1]	D9_C[1]
C2	P	BC17		62	A9_C[2]	B9_C[2]	C9_C[2]	D9_C[2]
C3	N	BC16		62	A9_C[3]	B9_C[3]	C9_C[3]	D9_C[3]
C4	P	BD16		62	A9_C[4]	B9_C[4]	C9_C[4]	D9_C[4]
C5	N	BE16		62	A9_C[5]	B9_C[5]	C9_C[5]	D9_C[5]
C6	P	BE17		62	A9_C[6]	B9_C[6]	C9_C[6]	D9_C[6]
C7	N	BF17		62	A9_C[7]	B9_C[7]	C9_C[7]	D9_C[7]
C8	P	BF19		62	A9_C[8]	B9_C[8]	C9_C[8]	D9_C[8]
C9	N	BF18		62	A9_C[9]	B9_C[9]	C9_C[9]	D9_C[9]
C10	P	BG16		62	A9_C[10]	B9_C[10]	C9_C[10]	D9_C[10]
C11	N	BH16		62	A9_C[11]	B9_C[11]	C9_C[11]	D9_C[11]
C12		NC						
C13		NC						
D0	P	BD18	GC	62	A9_D[0]	B9_D[0]	C9_D[0]	D9_D[0]
D1	N	BE18	GC	62	A9_D[1]	B9_D[1]	C9_D[1]	D9_D[1]
D2	P	BG17		62	A9_D[2]	B9_D[2]	C9_D[2]	D9_D[2]
D3	N	BH17		62	A9_D[3]	B9_D[3]	C9_D[3]	D9_D[3]
D4	P	BH18	DBC	62	A9_D[4]	B9_D[4]	C9_D[4]	D9_D[4]
D5	N	BJ18	DBC	62	A9_D[5]	B9_D[5]	C9_D[5]	D9_D[5]
D6	P	BG19		62	A9_D[6]	B9_D[6]	C9_D[6]	D9_D[6]
D7	N	BH19		62	A9_D[7]	B9_D[7]	C9_D[7]	D9_D[7]
D8	P	BJ20		62	A9_D[8]	B9_D[8]	C9_D[8]	D9_D[8]
D9	N	BJ19		62	A9_D[9]	B9_D[9]	C9_D[9]	D9_D[9]
D10	P	BF20	DBC	62	A9_D[10]	B9_D[10]	C9_D[10]	D9_D[10]
D11	N	BG20	DBC	62	A9_D[11]	B9_D[11]	C9_D[11]	D9_D[11]
D12	-	BE20		62	A9_D[12]	B9_D[12]	C9_D[12]	D9_D[12]
D13		NC						
VRP	-	BJ16	VRP	62	A9_VRP	B9_VRP	C9_VRP	D9_VRP
VRN	-	BB17		62	A9_VRN	B9_VRN	C9_VRN	D9_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BA24	GC	61	A10_A[0]	B10_A[0]	C10_A[0]	D10_A[0]
A1	N	BB24	GC	61	A10_A[1]	B10_A[1]	C10_A[1]	D10_A[1]
A2	P	AT23		61	A10_A[2]	B10_A[2]	C10_A[2]	D10_A[2]
A3	N	AT22		61	A10_A[3]	B10_A[3]	C10_A[3]	D10_A[3]
A4	P	AU24		61	A10_A[4]	B10_A[4]	C10_A[4]	D10_A[4]
A5	N	AV24		61	A10_A[5]	B10_A[5]	C10_A[5]	D10_A[5]
A6	P	AT25	DBC	61	A10_A[6]	B10_A[6]	C10_A[6]	D10_A[6]
A7	N	AU25	DBC	61	A10_A[7]	B10_A[7]	C10_A[7]	D10_A[7]
A8	P	AW25		61	A10_A[8]	B10_A[8]	C10_A[8]	D10_A[8]
A9	N	AW24		61	A10_A[9]	B10_A[9]	C10_A[9]	D10_A[9]
A10	P	AV23		61	A10_A[10]	B10_A[10]	C10_A[10]	D10_A[10]
A11	N	AW23		61	A10_A[11]	B10_A[11]	C10_A[11]	D10_A[11]
A12	-	AW21		61	A10_A[12]	B10_A[12]	C10_A[12]	D10_A[12]
A13		NC						
B0	P	AY23	GC_QBC	61	A10_B[0]	B10_B[0]	C10_B[0]	D10_B[0]
B1	N	BA23	GC_QBC	61	A10_B[1]	B10_B[1]	C10_B[1]	D10_B[1]
B2	P	AY25		61	A10_B[2]	B10_B[2]	C10_B[2]	D10_B[2]
B3	N	BA25		61	A10_B[3]	B10_B[3]	C10_B[3]	D10_B[3]
B4	P	AY22		61	A10_B[4]	B10_B[4]	C10_B[4]	D10_B[4]
B5	N	AY21		61	A10_B[5]	B10_B[5]	C10_B[5]	D10_B[5]
B6	P	BA22		61	A10_B[6]	B10_B[6]	C10_B[6]	D10_B[6]
B7	N	BB22		61	A10_B[7]	B10_B[7]	C10_B[7]	D10_B[7]
B8	P	BB21		61	A10_B[8]	B10_B[8]	C10_B[8]	D10_B[8]
B9	N	BC21		61	A10_B[9]	B10_B[9]	C10_B[9]	D10_B[9]
B10	P	AU22	DBC	61	A10_B[10]	B10_B[10]	C10_B[10]	D10_B[10]
B11	N	AV22	DBC	61	A10_B[11]	B10_B[11]	C10_B[11]	D10_B[11]
B12		NC						
B13		NC						
C0	P	BC24	GC	61	A10_C[0]	B10_C[0]	C10_C[0]	D10_C[0]
C1	N	BD24	GC	61	A10_C[1]	B10_C[1]	C10_C[1]	D10_C[1]
C2	P	BD23		61	A10_C[2]	B10_C[2]	C10_C[2]	D10_C[2]
C3	N	BE23		61	A10_C[3]	B10_C[3]	C10_C[3]	D10_C[3]
C4	P	BF24		61	A10_C[4]	B10_C[4]	C10_C[4]	D10_C[4]
C5	N	BF23		61	A10_C[5]	B10_C[5]	C10_C[5]	D10_C[5]
C6	P	BE22		61	A10_C[6]	B10_C[6]	C10_C[6]	D10_C[6]
C7	N	BF22		61	A10_C[7]	B10_C[7]	C10_C[7]	D10_C[7]
C8	P	BD21		61	A10_C[8]	B10_C[8]	C10_C[8]	D10_C[8]
C9	N	BE21		61	A10_C[9]	B10_C[9]	C10_C[9]	D10_C[9]
C10	P	BF25		61	A10_C[10]	B10_C[10]	C10_C[10]	D10_C[10]
C11	N	BG25		61	A10_C[11]	B10_C[11]	C10_C[11]	D10_C[11]
C12		NC						
C13		NC						
D0	P	BC23	GC	61	A10_D[0]	B10_D[0]	C10_D[0]	D10_D[0]
D1	N	BC22	GC	61	A10_D[1]	B10_D[1]	C10_D[1]	D10_D[1]
D2	P	BG24		61	A10_D[2]	B10_D[2]	C10_D[2]	D10_D[2]
D3	N	BH24		61	A10_D[3]	B10_D[3]	C10_D[3]	D10_D[3]
D4	P	BJ25	DBC	61	A10_D[4]	B10_D[4]	C10_D[4]	D10_D[4]
D5	N	BJ24	DBC	61	A10_D[5]	B10_D[5]	C10_D[5]	D10_D[5]
D6	P	BG22		61	A10_D[6]	B10_D[6]	C10_D[6]	D10_D[6]
D7	N	BH22		61	A10_D[7]	B10_D[7]	C10_D[7]	D10_D[7]
D8	P	BH23		61	A10_D[8]	B10_D[8]	C10_D[8]	D10_D[8]
D9	N	BJ23		61	A10_D[9]	B10_D[9]	C10_D[9]	D10_D[9]
D10	P	BH21	DBC	61	A10_D[10]	B10_D[10]	C10_D[10]	D10_D[10]
D11	N	BJ21	DBC	61	A10_D[11]	B10_D[11]	C10_D[11]	D10_D[11]
D12	-	BE25		61	A10_D[12]	B10_D[12]	C10_D[12]	D10_D[12]
D13		NC						
VRP	-	BG21	VRP	61	A10_VRP	B10_VRP	C10_VRP	D10_VRP
VRN	-	BB25		61	A10_VRN	B10_VRN	C10_VRN	D10_VRN

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J11

HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BM15	GC	60	A11_A[0]	B11_A[0]	C11_A[0]	D11_A[0]
A1	N	BN14	GC	60	A11_A[1]	B11_A[1]	C11_A[1]	D11_A[1]
A2	P	BP11		60	A11_A[2]	B11_A[2]	C11_A[2]	D11_A[2]
A3	N	BP10		60	A11_A[3]	B11_A[3]	C11_A[3]	D11_A[3]
A4	P	BN9		60	A11_A[4]	B11_A[4]	C11_A[4]	D11_A[4]
A5	N	BP9		60	A11_A[5]	B11_A[5]	C11_A[5]	D11_A[5]
A6	P	BN8	DBC	60	A11_A[6]	B11_A[6]	C11_A[6]	D11_A[6]
A7	N	BP8	DBC	60	A11_A[7]	B11_A[7]	C11_A[7]	D11_A[7]
A8	P	BM11		60	A11_A[8]	B11_A[8]	C11_A[8]	D11_A[8]
A9	N	BM10		60	A11_A[9]	B11_A[9]	C11_A[9]	D11_A[9]
A10	P	BK10		60	A11_A[10]	B11_A[10]	C11_A[10]	D11_A[10]
A11	N	BL10		60	A11_A[11]	B11_A[11]	C11_A[11]	D11_A[11]
A12	-	BK11		60	A11_A[12]	B11_A[12]	C11_A[12]	D11_A[12]
A13		NC						
B0	P	BL14	GC_QBC	60	A11_B[0]	B11_B[0]	C11_B[0]	D11_B[0]
B1	N	BM14	GC_QBC	60	A11_B[1]	B11_B[1]	C11_B[1]	D11_B[1]
B2	P	BP15		60	A11_B[2]	B11_B[2]	C11_B[2]	D11_B[2]
B3	N	BP14		60	A11_B[3]	B11_B[3]	C11_B[3]	D11_B[3]
B4	P	BN13		60	A11_B[4]	B11_B[4]	C11_B[4]	D11_B[4]
B5	N	BP13		60	A11_B[5]	B11_B[5]	C11_B[5]	D11_B[5]
B6	P	BK13		60	A11_B[6]	B11_B[6]	C11_B[6]	D11_B[6]
B7	N	BL13		60	A11_B[7]	B11_B[7]	C11_B[7]	D11_B[7]
B8	P	BK12		60	A11_B[8]	B11_B[8]	C11_B[8]	D11_B[8]
B9	N	BL12		60	A11_B[9]	B11_B[9]	C11_B[9]	D11_B[9]
B10	P	BN12	DBC	60	A11_B[10]	B11_B[10]	C11_B[10]	D11_B[10]
B11	N	BN11	DBC	60	A11_B[11]	B11_B[11]	C11_B[11]	D11_B[11]
B12		NC						
B13		NC						
C0	P	BK15	GC	60	A11_C[0]	B11_C[0]	C11_C[0]	D11_C[0]
C1	N	BL15	GC	60	A11_C[1]	B11_C[1]	C11_C[1]	D11_C[1]
C2	P	BK17		60	A11_C[2]	B11_C[2]	C11_C[2]	D11_C[2]
C3	N	BK16		60	A11_C[3]	B11_C[3]	C11_C[3]	D11_C[3]
C4	P	BM17		60	A11_C[4]	B11_C[4]	C11_C[4]	D11_C[4]
C5	N	BN17		60	A11_C[5]	B11_C[5]	C11_C[5]	D11_C[5]
C6	P	BL18		60	A11_C[6]	B11_C[6]	C11_C[6]	D11_C[6]
C7	N	BL17		60	A11_C[7]	B11_C[7]	C11_C[7]	D11_C[7]
C8	P	BN18		60	A11_C[8]	B11_C[8]	C11_C[8]	D11_C[8]
C9	N	BP18		60	A11_C[9]	B11_C[9]	C11_C[9]	D11_C[9]
C10	P	BK20		60	A11_C[10]	B11_C[10]	C11_C[10]	D11_C[10]
C11	N	BL20		60	A11_C[11]	B11_C[11]	C11_C[11]	D11_C[11]
C12		NC						
C13		NC						
D0	P	BM16	GC	60	A11_D[0]	B11_D[0]	C11_D[0]	D11_D[0]
D1	N	BN16	GC	60	A11_D[1]	B11_D[1]	C11_D[1]	D11_D[1]
D2	P	BL19		60	A11_D[2]	B11_D[2]	C11_D[2]	D11_D[2]
D3	N	BM19		60	A11_D[3]	B11_D[3]	C11_D[3]	D11_D[3]
D4	P	BN19	DBC	60	A11_D[4]	B11_D[4]	C11_D[4]	D11_D[4]
D5	N	BP19	DBC	60	A11_D[5]	B11_D[5]	C11_D[5]	D11_D[5]
D6	P	BM21		60	A11_D[6]	B11_D[6]	C11_D[6]	D11_D[6]
D7	N	BM20		60	A11_D[7]	B11_D[7]	C11_D[7]	D11_D[7]
D8	P	BP21		60	A11_D[8]	B11_D[8]	C11_D[8]	D11_D[8]
D9	N	BP20		60	A11_D[9]	B11_D[9]	C11_D[9]	D11_D[9]
D10	P	BN22	DBC	60	A11_D[10]	B11_D[10]	C11_D[10]	D11_D[10]
D11	N	BN21	DBC	60	A11_D[11]	B11_D[11]	C11_D[11]	D11_D[11]
D12	-	BP16		60	A11_D[12]	B11_D[12]	C11_D[12]	D11_D[12]
D13		NC						
VRP	-	BK21	VRP	60	A11_VRP	B11_VRP	C11_VRP	D11_VRP
VRN	-	BM12		60	A11_VRN	B11_VRN	C11_VRN	D11_VRN

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J12 - HR Bank

HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BK28	GC	84	A12_A[0]	B12_A[0]	C12_A[0]	D12_A[0]
A1	N	BL28	GC	84	A12_A[1]	B12_A[1]	C12_A[1]	D12_A[1]
A2	P	BL24		84	A12_A[2]	B12_A[2]	C12_A[2]	D12_A[2]
A3	N	BL23		84	A12_A[3]	B12_A[3]	C12_A[3]	D12_A[3]
A4	P	BM24		84	A12_A[4]	B12_A[4]	C12_A[4]	D12_A[4]
A5	N	BN24		84	A12_A[5]	B12_A[5]	C12_A[5]	D12_A[5]
A6	P	BL22	DBC	84	A12_A[6]	B12_A[6]	C12_A[6]	D12_A[6]
A7	N	BM22	DBC	84	A12_A[7]	B12_A[7]	C12_A[7]	D12_A[7]
A8	P	BN23		84	A12_A[8]	B12_A[8]	C12_A[8]	D12_A[8]
A9	N	BP23		84	A12_A[9]	B12_A[9]	C12_A[9]	D12_A[9]
A10	P	BP25		84	A12_A[10]	B12_A[10]	C12_A[10]	D12_A[10]
A11	N	BP24		84	A12_A[11]	B12_A[11]	C12_A[11]	D12_A[11]
A12	-	BK23		84	A12_A[12]	B12_A[12]	C12_A[12]	D12_A[12]
A13		NC						
B0	P	BK27	GC_QBC	84	A12_B[0]	B12_B[0]	C12_B[0]	D12_B[0]
B1	N	BL27	GC_QBC	84	A12_B[1]	B12_B[1]	C12_B[1]	D12_B[1]
B2	P	BK26		84	A12_B[2]	B12_B[2]	C12_B[2]	D12_B[2]
B3	N	BK25		84	A12_B[3]	B12_B[3]	C12_B[3]	D12_B[3]
B4	P	BN26		84	A12_B[4]	B12_B[4]	C12_B[4]	D12_B[4]
B5	N	BP26		84	A12_B[5]	B12_B[5]	C12_B[5]	D12_B[5]
B6	P	BM27		84	A12_B[6]	B12_B[6]	C12_B[6]	D12_B[6]
B7	N	BN27		84	A12_B[7]	B12_B[7]	C12_B[7]	D12_B[7]
B8	P	BN28		84	A12_B[8]	B12_B[8]	C12_B[8]	D12_B[8]
B9	N	BP28		84	A12_B[9]	B12_B[9]	C12_B[9]	D12_B[9]
B10	P	BL25	DBC	84	A12_B[10]	B12_B[10]	C12_B[10]	D12_B[10]
B11	N	BM25	DBC	84	A12_B[11]	B12_B[11]	C12_B[11]	D12_B[11]
B12		NC						
B13		NC						
C0	P	BL29	GC	94	A12_C[0]	B12_C[0]	C12_C[0]	D12_C[0]
C1	N	BM30	GC	94	A12_C[1]	B12_C[1]	C12_C[1]	D12_C[1]
C2	P	BP29		94	A12_C[2]	B12_C[2]	C12_C[2]	D12_C[2]
C3	N	BP30		94	A12_C[3]	B12_C[3]	C12_C[3]	D12_C[3]
C4	P	BN31		94	A12_C[4]	B12_C[4]	C12_C[4]	D12_C[4]
C5	N	BP31		94	A12_C[5]	B12_C[5]	C12_C[5]	D12_C[5]
C6	P	BM31		94	A12_C[6]	B12_C[6]	C12_C[6]	D12_C[6]
C7	N	BN32		94	A12_C[7]	B12_C[7]	C12_C[7]	D12_C[7]
C8	P	BL32		94	A12_C[8]	B12_C[8]	C12_C[8]	D12_C[8]
C9	N	BM32		94	A12_C[9]	B12_C[9]	C12_C[9]	D12_C[9]
C10	P	BL33		94	A12_C[10]	B12_C[10]	C12_C[10]	D12_C[10]
C11	N	BL34		94	A12_C[11]	B12_C[11]	C12_C[11]	D12_C[11]
C12		NC						
C13		NC						
D0	P	BM29	GC	94	A12_D[0]	B12_D[0]	C12_D[0]	D12_D[0]
D1	N	BN29	GC	94	A12_D[1]	B12_D[1]	C12_D[1]	D12_D[1]
D2	P	BL35		94	A12_D[2]	B12_D[2]	C12_D[2]	D12_D[2]
D3	N	BM35		94	A12_D[3]	B12_D[3]	C12_D[3]	D12_D[3]
D4	P	BM36	DBC	94	A12_D[4]	B12_D[4]	C12_D[4]	D12_D[4]
D5	N	BN36	DBC	94	A12_D[5]	B12_D[5]	C12_D[5]	D12_D[5]
D6	P	BM34		94	A12_D[6]	B12_D[6]	C12_D[6]	D12_D[6]
D7	N	BN34		94	A12_D[7]	B12_D[7]	C12_D[7]	D12_D[7]
D8	P	BP35		94	A12_D[8]	B12_D[8]	C12_D[8]	D12_D[8]
D9	N	BP36		94	A12_D[9]	B12_D[9]	C12_D[9]	D12_D[9]
D10	P	BN33	DBC	94	A12_D[10]	B12_D[10]	C12_D[10]	D12_D[10]
D11	N	BP34	DBC	94	A12_D[11]	B12_D[11]	C12_D[11]	D12_D[11]
D12	-	BP33		94	A12_D[12]	B12_D[12]	C12_D[12]	D12_D[12]
D13		NC						
VRP	-	BL37		94	A12_VRP	B12_VRP	C12_VRP	D12_VRP
VRN	-	BM26		84	A12_VRN	B12_VRN	C12_VRN	D12_VRN

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J13

HT3		XCVU440 - FLGA2892 SLR 2			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	L33	GC	50	A13_A[0]	B13_A[0]	C13_A[0]	D13_A[0]
A1	N	K33	GC	50	A13_A[1]	B13_A[1]	C13_A[1]	D13_A[1]
A2	P	F30		50	A13_A[2]	B13_A[2]	C13_A[2]	D13_A[2]
A3	N	E30		50	A13_A[3]	B13_A[3]	C13_A[3]	D13_A[3]
A4	P	G32		50	A13_A[4]	B13_A[4]	C13_A[4]	D13_A[4]
A5	N	F32		50	A13_A[5]	B13_A[5]	C13_A[5]	D13_A[5]
A6	P	E31	DBC	50	A13_A[6]	B13_A[6]	C13_A[6]	D13_A[6]
A7	N	E32	DBC	50	A13_A[7]	B13_A[7]	C13_A[7]	D13_A[7]
A8	P	G34		50	A13_A[8]	B13_A[8]	C13_A[8]	D13_A[8]
A9	N	F34		50	A13_A[9]	B13_A[9]	C13_A[9]	D13_A[9]
A10	P	G35		50	A13_A[10]	B13_A[10]	C13_A[10]	D13_A[10]
A11	N	F35		50	A13_A[11]	B13_A[11]	C13_A[11]	D13_A[11]
A12	-	F33		50	A13_A[12]	B13_A[12]	C13_A[12]	D13_A[12]
A13		NC						
B0	P	L32	GC_QBC	50	A13_B[0]	B13_B[0]	C13_B[0]	D13_B[0]
B1	N	K32	GC_QBC	50	A13_B[1]	B13_B[1]	C13_B[1]	D13_B[1]
B2	P	K31		50	A13_B[2]	B13_B[2]	C13_B[2]	D13_B[2]
B3	N	J31		50	A13_B[3]	B13_B[3]	C13_B[3]	D13_B[3]
B4	P	J33		50	A13_B[4]	B13_B[4]	C13_B[4]	D13_B[4]
B5	N	H33		50	A13_B[5]	B13_B[5]	C13_B[5]	D13_B[5]
B6	P	J34		50	A13_B[6]	B13_B[6]	C13_B[6]	D13_B[6]
B7	N	H34		50	A13_B[7]	B13_B[7]	C13_B[7]	D13_B[7]
B8	P	K35		50	A13_B[8]	B13_B[8]	C13_B[8]	D13_B[8]
B9	N	J35		50	A13_B[9]	B13_B[9]	C13_B[9]	D13_B[9]
B10	P	H31	DBC	50	A13_B[10]	B13_B[10]	C13_B[10]	D13_B[10]
B11	N	G31	DBC	50	A13_B[11]	B13_B[11]	C13_B[11]	D13_B[11]
B12		NC						
B13		NC						
C0	P	N31	GC	50	A13_C[0]	B13_C[0]	C13_C[0]	D13_C[0]
C1	N	M31	GC	50	A13_C[1]	B13_C[1]	C13_C[1]	D13_C[1]
C2	P	M34		50	A13_C[2]	B13_C[2]	C13_C[2]	D13_C[2]
C3	N	L34		50	A13_C[3]	B13_C[3]	C13_C[3]	D13_C[3]
C4	P	P34		50	A13_C[4]	B13_C[4]	C13_C[4]	D13_C[4]
C5	N	N34		50	A13_C[5]	B13_C[5]	C13_C[5]	D13_C[5]
C6	P	P33		50	A13_C[6]	B13_C[6]	C13_C[6]	D13_C[6]
C7	N	N33		50	A13_C[7]	B13_C[7]	C13_C[7]	D13_C[7]
C8	P	R31		50	A13_C[8]	B13_C[8]	C13_C[8]	D13_C[8]
C9	N	P31		50	A13_C[9]	B13_C[9]	C13_C[9]	D13_C[9]
C10	P	W34		50	A13_C[10]	B13_C[10]	C13_C[10]	D13_C[10]
C11	N	V34		50	A13_C[11]	B13_C[11]	C13_C[11]	D13_C[11]
C12		NC						
C13		NC						
D0	P	N32	GC	50	A13_D[0]	B13_D[0]	C13_D[0]	D13_D[0]
D1	N	M32	GC	50	A13_D[1]	B13_D[1]	C13_D[1]	D13_D[1]
D2	P	U34		50	A13_D[2]	B13_D[2]	C13_D[2]	D13_D[2]
D3	N	T34		50	A13_D[3]	B13_D[3]	C13_D[3]	D13_D[3]
D4	P	T33	DBC	50	A13_D[4]	B13_D[4]	C13_D[4]	D13_D[4]
D5	N	R33	DBC	50	A13_D[5]	B13_D[5]	C13_D[5]	D13_D[5]
D6	P	V32		50	A13_D[6]	B13_D[6]	C13_D[6]	D13_D[6]
D7	N	V33		50	A13_D[7]	B13_D[7]	C13_D[7]	D13_D[7]
D8	P	U32		50	A13_D[8]	B13_D[8]	C13_D[8]	D13_D[8]
D9	N	T32		50	A13_D[9]	B13_D[9]	C13_D[9]	D13_D[9]
D10	P	V31	DBC	50	A13_D[10]	B13_D[10]	C13_D[10]	D13_D[10]
D11	N	U31	DBC	50	A13_D[11]	B13_D[11]	C13_D[11]	D13_D[11]
D12	-	R32		50	A13_D[12]	B13_D[12]	C13_D[12]	D13_D[12]
D13		NC						
VRP	-	W31	VRP	50	A13_VRP	B13_VRP	C13_VRP	D13_VRP
VRN	-	H32		50	A13_VRN	B13_VRN	C13_VRN	D13_VRN

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J14

HT3		XCVU440 - FLGA2892 SLR 2			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	M29	GC	49	A14_A[0]	B14_A[0]	C14_A[0]	D14_A[0]
A1	N	L29	GC	49	A14_A[1]	B14_A[1]	C14_A[1]	D14_A[1]
A2	P	J28		49	A14_A[2]	B14_A[2]	C14_A[2]	D14_A[2]
A3	N	H28		49	A14_A[3]	B14_A[3]	C14_A[3]	D14_A[3]
A4	P	H27		49	A14_A[4]	B14_A[4]	C14_A[4]	D14_A[4]
A5	N	G27		49	A14_A[5]	B14_A[5]	C14_A[5]	D14_A[5]
A6	P	G29	DBC	49	A14_A[6]	B14_A[6]	C14_A[6]	D14_A[6]
A7	N	F29	DBC	49	A14_A[7]	B14_A[7]	C14_A[7]	D14_A[7]
A8	P	F28		49	A14_A[8]	B14_A[8]	C14_A[8]	D14_A[8]
A9	N	E28		49	A14_A[9]	B14_A[9]	C14_A[9]	D14_A[9]
A10	P	F27		49	A14_A[10]	B14_A[10]	C14_A[10]	D14_A[10]
A11	N	E27		49	A14_A[11]	B14_A[11]	C14_A[11]	D14_A[11]
A12	-	G30		49	A14_A[12]	B14_A[12]	C14_A[12]	D14_A[12]
A13		NC						
B0	P	M30	GC_QBC	49	A14_B[0]	B14_B[0]	C14_B[0]	D14_B[0]
B1	N	L30	GC_QBC	49	A14_B[1]	B14_B[1]	C14_B[1]	D14_B[1]
B2	P	K30		49	A14_B[2]	B14_B[2]	C14_B[2]	D14_B[2]
B3	N	J30		49	A14_B[3]	B14_B[3]	C14_B[3]	D14_B[3]
B4	P	L28		49	A14_B[4]	B14_B[4]	C14_B[4]	D14_B[4]
B5	N	K28		49	A14_B[5]	B14_B[5]	C14_B[5]	D14_B[5]
B6	P	L27		49	A14_B[6]	B14_B[6]	C14_B[6]	D14_B[6]
B7	N	K27		49	A14_B[7]	B14_B[7]	C14_B[7]	D14_B[7]
B8	P	M26		49	A14_B[8]	B14_B[8]	C14_B[8]	D14_B[8]
B9	N	M27		49	A14_B[9]	B14_B[9]	C14_B[9]	D14_B[9]
B10	P	J29	DBC	49	A14_B[10]	B14_B[10]	C14_B[10]	D14_B[10]
B11	N	H29	DBC	49	A14_B[11]	B14_B[11]	C14_B[11]	D14_B[11]
B12		NC						
B13		NC						
C0	P	N27	GC	49	A14_C[0]	B14_C[0]	C14_C[0]	D14_C[0]
C1	N	N28	GC	49	A14_C[1]	B14_C[1]	C14_C[1]	D14_C[1]
C2	P	R30		49	A14_C[2]	B14_C[2]	C14_C[2]	D14_C[2]
C3	N	P30		49	A14_C[3]	B14_C[3]	C14_C[3]	D14_C[3]
C4	P	R28		49	A14_C[4]	B14_C[4]	C14_C[4]	D14_C[4]
C5	N	P28		49	A14_C[5]	B14_C[5]	C14_C[5]	D14_C[5]
C6	P	R26		49	A14_C[6]	B14_C[6]	C14_C[6]	D14_C[6]
C7	N	R27		49	A14_C[7]	B14_C[7]	C14_C[7]	D14_C[7]
C8	P	P26		49	A14_C[8]	B14_C[8]	C14_C[8]	D14_C[8]
C9	N	N26		49	A14_C[9]	B14_C[9]	C14_C[9]	D14_C[9]
C10	P	W29		49	A14_C[10]	B14_C[10]	C14_C[10]	D14_C[10]
C11	N	W30		49	A14_C[11]	B14_C[11]	C14_C[11]	D14_C[11]
C12		NC						
C13		NC						
D0	P	P29	GC	49	A14_D[0]	B14_D[0]	C14_D[0]	D14_D[0]
D1	N	N29	GC	49	A14_D[1]	B14_D[1]	C14_D[1]	D14_D[1]
D2	P	V28		49	A14_D[2]	B14_D[2]	C14_D[2]	D14_D[2]
D3	N	V29		49	A14_D[3]	B14_D[3]	C14_D[3]	D14_D[3]
D4	P	U29	DBC	49	A14_D[4]	B14_D[4]	C14_D[4]	D14_D[4]
D5	N	U30	DBC	49	A14_D[5]	B14_D[5]	C14_D[5]	D14_D[5]
D6	P	T27		49	A14_D[6]	B14_D[6]	C14_D[6]	D14_D[6]
D7	N	T28		49	A14_D[7]	B14_D[7]	C14_D[7]	D14_D[7]
D8	P	V27		49	A14_D[8]	B14_D[8]	C14_D[8]	D14_D[8]
D9	N	U27		49	A14_D[9]	B14_D[9]	C14_D[9]	D14_D[9]
D10	P	V26	DBC	49	A14_D[10]	B14_D[10]	C14_D[10]	D14_D[10]
D11	N	U26	DBC	49	A14_D[11]	B14_D[11]	C14_D[11]	D14_D[11]
D12	-	T30		49	A14_D[12]	B14_D[12]	C14_D[12]	D14_D[12]
D13		NC						
VRP	-	T29	VRP	49	A14_VRP	B14_VRP	C14_VRP	D14_VRP
VRN	-	K26		49	A14_VRN	B14_VRN	C14_VRN	D14_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	G50	GC	48	A15_A[0]	B15_A[0]	C15_A[0]	D15_A[0]
A1	N	G51	GC	48	A15_A[1]	B15_A[1]	C15_A[1]	D15_A[1]
A2	P	D53		48	A15_A[2]	B15_A[2]	C15_A[2]	D15_A[2]
A3	N	D54		48	A15_A[3]	B15_A[3]	C15_A[3]	D15_A[3]
A4	P	C52		48	A15_A[4]	B15_A[4]	C15_A[4]	D15_A[4]
A5	N	C53		48	A15_A[5]	B15_A[5]	C15_A[5]	D15_A[5]
A6	P	B51	DBC	48	A15_A[6]	B15_A[6]	C15_A[6]	D15_A[6]
A7	N	B52	DBC	48	A15_A[7]	B15_A[7]	C15_A[7]	D15_A[7]
A8	P	B50		48	A15_A[8]	B15_A[8]	C15_A[8]	D15_A[8]
A9	N	A50		48	A15_A[9]	B15_A[9]	C15_A[9]	D15_A[9]
A10	P	D49		48	A15_A[10]	B15_A[10]	C15_A[10]	D15_A[10]
A11	N	C49		48	A15_A[11]	B15_A[11]	C15_A[11]	D15_A[11]
A12	-	C51		48	A15_A[12]	B15_A[12]	C15_A[12]	D15_A[12]
A13		NC						
B0	P	G49	GC_QBC	48	A15_B[0]	B15_B[0]	C15_B[0]	D15_B[0]
B1	N	F49	GC_QBC	48	A15_B[1]	B15_B[1]	C15_B[1]	D15_B[1]
B2	P	F50		48	A15_B[2]	B15_B[2]	C15_B[2]	D15_B[2]
B3	N	E50		48	A15_B[3]	B15_B[3]	C15_B[3]	D15_B[3]
B4	P	G52		48	A15_B[4]	B15_B[4]	C15_B[4]	D15_B[4]
B5	N	F52		48	A15_B[5]	B15_B[5]	C15_B[5]	D15_B[5]
B6	P	E51		48	A15_B[6]	B15_B[6]	C15_B[6]	D15_B[6]
B7	N	E52		48	A15_B[7]	B15_B[7]	C15_B[7]	D15_B[7]
B8	P	F53		48	A15_B[8]	B15_B[8]	C15_B[8]	D15_B[8]
B9	N	F54		48	A15_B[9]	B15_B[9]	C15_B[9]	D15_B[9]
B10	P	D50	DBC	48	A15_B[10]	B15_B[10]	C15_B[10]	D15_B[10]
B11	N	D51	DBC	48	A15_B[11]	B15_B[11]	C15_B[11]	D15_B[11]
B12		NC						
B13		NC						
C0	P	F47	GC	48	A15_C[0]	B15_C[0]	C15_C[0]	D15_C[0]
C1	N	F48	GC	48	A15_C[1]	B15_C[1]	C15_C[1]	D15_C[1]
C2	P	H46		48	A15_C[2]	B15_C[2]	C15_C[2]	D15_C[2]
C3	N	G46		48	A15_C[3]	B15_C[3]	C15_C[3]	D15_C[3]
C4	P	J45		48	A15_C[4]	B15_C[4]	C15_C[4]	D15_C[4]
C5	N	J46		48	A15_C[5]	B15_C[5]	C15_C[5]	D15_C[5]
C6	P	H48		48	A15_C[6]	B15_C[6]	C15_C[6]	D15_C[6]
C7	N	H49		48	A15_C[7]	B15_C[7]	C15_C[7]	D15_C[7]
C8	P	J48		48	A15_C[8]	B15_C[8]	C15_C[8]	D15_C[8]
C9	N	J49		48	A15_C[9]	B15_C[9]	C15_C[9]	D15_C[9]
C10	P	H54		48	A15_C[10]	B15_C[10]	C15_C[10]	D15_C[10]
C11	N	G54		48	A15_C[11]	B15_C[11]	C15_C[11]	D15_C[11]
C12		NC						
C13		NC						
D0	P	H47	GC	48	A15_D[0]	B15_D[0]	C15_D[0]	D15_D[0]
D1	N	G47	GC	48	A15_D[1]	B15_D[1]	C15_D[1]	D15_D[1]
D2	P	J53		48	A15_D[2]	B15_D[2]	C15_D[2]	D15_D[2]
D3	N	H53		48	A15_D[3]	B15_D[3]	C15_D[3]	D15_D[3]
D4	P	H51	DBC	48	A15_D[4]	B15_D[4]	C15_D[4]	D15_D[4]
D5	N	H52	DBC	48	A15_D[5]	B15_D[5]	C15_D[5]	D15_D[5]
D6	P	J50		48	A15_D[6]	B15_D[6]	C15_D[6]	D15_D[6]
D7	N	J51		48	A15_D[7]	B15_D[7]	C15_D[7]	D15_D[7]
D8	P	K50		48	A15_D[8]	B15_D[8]	C15_D[8]	D15_D[8]
D9	N	K51		48	A15_D[9]	B15_D[9]	C15_D[9]	D15_D[9]
D10	P	K52	DBC	48	A15_D[10]	B15_D[10]	C15_D[10]	D15_D[10]
D11	N	K53	DBC	48	A15_D[11]	B15_D[11]	C15_D[11]	D15_D[11]
D12	-	E48		48	A15_D[12]	B15_D[12]	C15_D[12]	D15_D[12]
D13		NC						
VRP	-	J54	VRP	48	A15_VRP	B15_VRP	C15_VRP	D15_VRP
VRN	-	E53		48	A15_VRN	B15_VRN	C15_VRN	D15_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	M47	GC	47	A16_A[0]	B16_A[0]	C16_A[0]	D16_A[0]
A1	N	L47	GC	47	A16_A[1]	B16_A[1]	C16_A[1]	D16_A[1]
A2	P	P43		47	A16_A[2]	B16_A[2]	C16_A[2]	D16_A[2]
A3	N	N43		47	A16_A[3]	B16_A[3]	C16_A[3]	D16_A[3]
A4	P	N42		47	A16_A[4]	B16_A[4]	C16_A[4]	D16_A[4]
A5	N	M42		47	A16_A[5]	B16_A[5]	C16_A[5]	D16_A[5]
A6	P	L42	DBC	47	A16_A[6]	B16_A[6]	C16_A[6]	D16_A[6]
A7	N	L43	DBC	47	A16_A[7]	B16_A[7]	C16_A[7]	D16_A[7]
A8	P	P41		47	A16_A[8]	B16_A[8]	C16_A[8]	D16_A[8]
A9	N	N41		47	A16_A[9]	B16_A[9]	C16_A[9]	D16_A[9]
A10	P	M40		47	A16_A[10]	B16_A[10]	C16_A[10]	D16_A[10]
A11	N	L40		47	A16_A[11]	B16_A[11]	C16_A[11]	D16_A[11]
A12	-	M41		47	A16_A[12]	B16_A[12]	C16_A[12]	D16_A[12]
A13		NC						
B0	P	N46	GC_QBC	47	A16_B[0]	B16_B[0]	C16_B[0]	D16_B[0]
B1	N	M46	GC_QBC	47	A16_B[1]	B16_B[1]	C16_B[1]	D16_B[1]
B2	P	M45		47	A16_B[2]	B16_B[2]	C16_B[2]	D16_B[2]
B3	N	L45		47	A16_B[3]	B16_B[3]	C16_B[3]	D16_B[3]
B4	P	K45		47	A16_B[4]	B16_B[4]	C16_B[4]	D16_B[4]
B5	N	K46		47	A16_B[5]	B16_B[5]	C16_B[5]	D16_B[5]
B6	P	M44		47	A16_B[6]	B16_B[6]	C16_B[6]	D16_B[6]
B7	N	L44		47	A16_B[7]	B16_B[7]	C16_B[7]	D16_B[7]
B8	P	P45		47	A16_B[8]	B16_B[8]	C16_B[8]	D16_B[8]
B9	N	P46		47	A16_B[9]	B16_B[9]	C16_B[9]	D16_B[9]
B10	P	P44	DBC	47	A16_B[10]	B16_B[10]	C16_B[10]	D16_B[10]
B11	N	N44	DBC	47	A16_B[11]	B16_B[11]	C16_B[11]	D16_B[11]
B12		NC						
B13		NC						
C0	P	N47	GC	47	A16_C[0]	B16_C[0]	C16_C[0]	D16_C[0]
C1	N	N48	GC	47	A16_C[1]	B16_C[1]	C16_C[1]	D16_C[1]
C2	P	M50		47	A16_C[2]	B16_C[2]	C16_C[2]	D16_C[2]
C3	N	L50		47	A16_C[3]	B16_C[3]	C16_C[3]	D16_C[3]
C4	P	M49		47	A16_C[4]	B16_C[4]	C16_C[4]	D16_C[4]
C5	N	L49		47	A16_C[5]	B16_C[5]	C16_C[5]	D16_C[5]
C6	P	P49		47	A16_C[6]	B16_C[6]	C16_C[6]	D16_C[6]
C7	N	N49		47	A16_C[7]	B16_C[7]	C16_C[7]	D16_C[7]
C8	P	P50		47	A16_C[8]	B16_C[8]	C16_C[8]	D16_C[8]
C9	N	P51		47	A16_C[9]	B16_C[9]	C16_C[9]	D16_C[9]
C10	P	M54		47	A16_C[10]	B16_C[10]	C16_C[10]	D16_C[10]
C11	N	L54		47	A16_C[11]	B16_C[11]	C16_C[11]	D16_C[11]
C12		NC						
C13		NC						
D0	P	L52		47	A16_D[0]	B16_D[0]	C16_D[0]	D16_D[0]
D1	N	L53		47	A16_D[1]	B16_D[1]	C16_D[1]	D16_D[1]
D2	P	N51	DBC	47	A16_D[2]	B16_D[2]	C16_D[2]	D16_D[2]
D3	N	N52	DBC	47	A16_D[3]	B16_D[3]	C16_D[3]	D16_D[3]
D4	P	M51		47	A16_D[4]	B16_D[4]	C16_D[4]	D16_D[4]
D5	N	M52		47	A16_D[5]	B16_D[5]	C16_D[5]	D16_D[5]
D6	P	P53		47	A16_D[6]	B16_D[6]	C16_D[6]	D16_D[6]
D7	N	P54		47	A16_D[7]	B16_D[7]	C16_D[7]	D16_D[7]
D8	P	N53	DBC	47	A16_D[8]	B16_D[8]	C16_D[8]	D16_D[8]
D9	N	N54	DBC	47	A16_D[9]	B16_D[9]	C16_D[9]	D16_D[9]
D10	-	P48		47	A16_D[10]	B16_D[10]	C16_D[10]	D16_D[10]
D11		NC						
D12		NC						
D13		NC						
VRP	-	R53	VRP	47	A16_VRP	B16_VRP	C16_VRP	D16_VRP
VRN	-	K47		47	A16_VRN	B16_VRN	C16_VRN	D16_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	R47	GC	46	A17_A[0]	B17_A[0]	C17_A[0]	D17_A[0]
A1	N	R48	GC	46	A17_A[1]	B17_A[1]	C17_A[1]	D17_A[1]
A2	P	V42		46	A17_A[2]	B17_A[2]	C17_A[2]	D17_A[2]
A3	N	U42		46	A17_A[3]	B17_A[3]	C17_A[3]	D17_A[3]
A4	P	T42		46	A17_A[4]	B17_A[4]	C17_A[4]	D17_A[4]
A5	N	T43		46	A17_A[5]	B17_A[5]	C17_A[5]	D17_A[5]
A6	P	R42	DBC	46	A17_A[6]	B17_A[6]	C17_A[6]	D17_A[6]
A7	N	R43	DBC	46	A17_A[7]	B17_A[7]	C17_A[7]	D17_A[7]
A8	P	R40		46	A17_A[8]	B17_A[8]	C17_A[8]	D17_A[8]
A9	N	R41		46	A17_A[9]	B17_A[9]	C17_A[9]	D17_A[9]
A10	P	U40		46	A17_A[10]	B17_A[10]	C17_A[10]	D17_A[10]
A11	N	T40		46	A17_A[11]	B17_A[11]	C17_A[11]	D17_A[11]
A12	-	U41		46	A17_A[12]	B17_A[12]	C17_A[12]	D17_A[12]
A13		NC						
B0	P	U47	GC_QBC	46	A17_B[0]	B17_B[0]	C17_B[0]	D17_B[0]
B1	N	T47	GC_QBC	46	A17_B[1]	B17_B[1]	C17_B[1]	D17_B[1]
B2	P	R45		46	A17_B[2]	B17_B[2]	C17_B[2]	D17_B[2]
B3	N	R46		46	A17_B[3]	B17_B[3]	C17_B[3]	D17_B[3]
B4	P	T44		46	A17_B[4]	B17_B[4]	C17_B[4]	D17_B[4]
B5	N	T45		46	A17_B[5]	B17_B[5]	C17_B[5]	D17_B[5]
B6	P	U44		46	A17_B[6]	B17_B[6]	C17_B[6]	D17_B[6]
B7	N	U45		46	A17_B[7]	B17_B[7]	C17_B[7]	D17_B[7]
B8	P	V46		46	A17_B[8]	B17_B[8]	C17_B[8]	D17_B[8]
B9	N	U46		46	A17_B[9]	B17_B[9]	C17_B[9]	D17_B[9]
B10	P	V43	DBC	46	A17_B[10]	B17_B[10]	C17_B[10]	D17_B[10]
B11	N	V44	DBC	46	A17_B[11]	B17_B[11]	C17_B[11]	D17_B[11]
B12		NC						
B13		NC						
C0	P	T48	GC	46	A17_C[0]	B17_C[0]	C17_C[0]	D17_C[0]
C1	N	T49	GC	46	A17_C[1]	B17_C[1]	C17_C[1]	D17_C[1]
C2	P	W48		46	A17_C[2]	B17_C[2]	C17_C[2]	D17_C[2]
C3	N	V48		46	A17_C[3]	B17_C[3]	C17_C[3]	D17_C[3]
C4	P	U50		46	A17_C[4]	B17_C[4]	C17_C[4]	D17_C[4]
C5	N	T50		46	A17_C[5]	B17_C[5]	C17_C[5]	D17_C[5]
C6	P	W49		46	A17_C[6]	B17_C[6]	C17_C[6]	D17_C[6]
C7	N	W50		46	A17_C[7]	B17_C[7]	C17_C[7]	D17_C[7]
C8	P	W51		46	A17_C[8]	B17_C[8]	C17_C[8]	D17_C[8]
C9	N	V51		46	A17_C[9]	B17_C[9]	C17_C[9]	D17_C[9]
C10	P	R51		46	A17_C[10]	B17_C[10]	C17_C[10]	D17_C[10]
C11	N	R52		46	A17_C[11]	B17_C[11]	C17_C[11]	D17_C[11]
C12		NC						
C13		NC						
D0	P	T52		46	A17_D[0]	B17_D[0]	C17_D[0]	D17_D[0]
D1	N	T53		46	A17_D[1]	B17_D[1]	C17_D[1]	D17_D[1]
D2	P	U54	DBC	46	A17_D[2]	B17_D[2]	C17_D[2]	D17_D[2]
D3	N	T54	DBC	46	A17_D[3]	B17_D[3]	C17_D[3]	D17_D[3]
D4	P	V52		46	A17_D[4]	B17_D[4]	C17_D[4]	D17_D[4]
D5	N	U52		46	A17_D[5]	B17_D[5]	C17_D[5]	D17_D[5]
D6	P	V53		46	A17_D[6]	B17_D[6]	C17_D[6]	D17_D[6]
D7	N	V54		46	A17_D[7]	B17_D[7]	C17_D[7]	D17_D[7]
D8	P	W53	DBC	46	A17_D[8]	B17_D[8]	C17_D[8]	D17_D[8]
D9	N	W54	DBC	46	A17_D[9]	B17_D[9]	C17_D[9]	D17_D[9]
D10	-	R50		46	A17_D[10]	B17_D[10]	C17_D[10]	D17_D[10]
D11		NC						
D12		NC						
D13		NC						
VRP	-	U51	VRP	46	A17_VRP	B17_VRP	C17_VRP	D17_VRP
VRN	-	V47		46	A17_VRN	B17_VRN	C17_VRN	D17_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	Y46	GC	45	A18_A[0]	B18_A[0]	C18_A[0]	D18_A[0]
A1	N	W46	GC	45	A18_A[1]	B18_A[1]	C18_A[1]	D18_A[1]
A2	P	AC42		45	A18_A[2]	B18_A[2]	C18_A[2]	D18_A[2]
A3	N	AC43		45	A18_A[3]	B18_A[3]	C18_A[3]	D18_A[3]
A4	P	AB41		45	A18_A[4]	B18_A[4]	C18_A[4]	D18_A[4]
A5	N	AB42		45	A18_A[5]	B18_A[5]	C18_A[5]	D18_A[5]
A6	P	AA42	DBC	45	A18_A[6]	B18_A[6]	C18_A[6]	D18_A[6]
A7	N	AA43	DBC	45	A18_A[7]	B18_A[7]	C18_A[7]	D18_A[7]
A8	P	Y41		45	A18_A[8]	B18_A[8]	C18_A[8]	D18_A[8]
A9	N	Y42		45	A18_A[9]	B18_A[9]	C18_A[9]	D18_A[9]
A10	P	Y43		45	A18_A[10]	B18_A[10]	C18_A[10]	D18_A[10]
A11	N	W43		45	A18_A[11]	B18_A[11]	C18_A[11]	D18_A[11]
A12	-	W41		45	A18_A[12]	B18_A[12]	C18_A[12]	D18_A[12]
A13		NC						
B0	P	AB47	GC_QBC	45	A18_B[0]	B18_B[0]	C18_B[0]	D18_B[0]
B1	N	AA47	GC_QBC	45	A18_B[1]	B18_B[1]	C18_B[1]	D18_B[1]
B2	P	AC46		45	A18_B[2]	B18_B[2]	C18_B[2]	D18_B[2]
B3	N	AC47		45	A18_B[3]	B18_B[3]	C18_B[3]	D18_B[3]
B4	P	AB45		45	A18_B[4]	B18_B[4]	C18_B[4]	D18_B[4]
B5	N	AB46		45	A18_B[5]	B18_B[5]	C18_B[5]	D18_B[5]
B6	P	AA44		45	A18_B[6]	B18_B[6]	C18_B[6]	D18_B[6]
B7	N	AA45		45	A18_B[7]	B18_B[7]	C18_B[7]	D18_B[7]
B8	P	W44		45	A18_B[8]	B18_B[8]	C18_B[8]	D18_B[8]
B9	N	W45		45	A18_B[9]	B18_B[9]	C18_B[9]	D18_B[9]
B10	P	AC44	DBC	45	A18_B[10]	B18_B[10]	C18_B[10]	D18_B[10]
B11	N	AB44	DBC	45	A18_B[11]	B18_B[11]	C18_B[11]	D18_B[11]
B12		NC						
B13		NC						
C0	P	Y47	GC	45	A18_C[0]	B18_C[0]	C18_C[0]	D18_C[0]
C1	N	Y48	GC	45	A18_C[1]	B18_C[1]	C18_C[1]	D18_C[1]
C2	P	AC49		45	A18_C[2]	B18_C[2]	C18_C[2]	D18_C[2]
C3	N	AB49		45	A18_C[3]	B18_C[3]	C18_C[3]	D18_C[3]
C4	P	AB50		45	A18_C[4]	B18_C[4]	C18_C[4]	D18_C[4]
C5	N	AA50		45	A18_C[5]	B18_C[5]	C18_C[5]	D18_C[5]
C6	P	Y50		45	A18_C[6]	B18_C[6]	C18_C[6]	D18_C[6]
C7	N	Y51		45	A18_C[7]	B18_C[7]	C18_C[7]	D18_C[7]
C8	P	AC51		45	A18_C[8]	B18_C[8]	C18_C[8]	D18_C[8]
C9	N	AB51		45	A18_C[9]	B18_C[9]	C18_C[9]	D18_C[9]
C10	P	AC52		45	A18_C[10]	B18_C[10]	C18_C[10]	D18_C[10]
C11	N	AB52		45	A18_C[11]	B18_C[11]	C18_C[11]	D18_C[11]
C12		NC						
C13		NC						
D0	P	AA52		45	A18_D[0]	B18_D[0]	C18_D[0]	D18_D[0]
D1	N	Y52		45	A18_D[1]	B18_D[1]	C18_D[1]	D18_D[1]
D2	P	AA53	DBC	45	A18_D[2]	B18_D[2]	C18_D[2]	D18_D[2]
D3	N	Y53	DBC	45	A18_D[3]	B18_D[3]	C18_D[3]	D18_D[3]
D4	P	AA54		45	A18_D[4]	B18_D[4]	C18_D[4]	D18_D[4]
D5	N	Y54		45	A18_D[5]	B18_D[5]	C18_D[5]	D18_D[5]
D6	P	AC54		45	A18_D[6]	B18_D[6]	C18_D[6]	D18_D[6]
D7	N	AB54		45	A18_D[7]	B18_D[7]	C18_D[7]	D18_D[7]
D8	P	AD53	DBC	45	A18_D[8]	B18_D[8]	C18_D[8]	D18_D[8]
D9	N	AC53	DBC	45	A18_D[9]	B18_D[9]	C18_D[9]	D18_D[9]
D10	-	AC48		45	A18_D[10]	B18_D[10]	C18_D[10]	D18_D[10]
D11		NC						
D12		NC						
D13		NC						
VRP	-	AD54	VRP	45	A18_VRP	B18_VRP	C18_VRP	D18_VRP
VRN	-	Y45		45	A18_VRN	B18_VRN	C18_VRN	D18_VRN

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HT3		XCVU440 - FLGA2892 SLR 1			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	AG47	GC	44	A19_A[0]	B19_A[0]	C19_A[0]	D19_A[0]
A1	N	AF47	GC	44	A19_A[1]	B19_A[1]	C19_A[1]	D19_A[1]
A2	P	AH42		44	A19_A[2]	B19_A[2]	C19_A[2]	D19_A[2]
A3	N	AH43		44	A19_A[3]	B19_A[3]	C19_A[3]	D19_A[3]
A4	P	AG41		44	A19_A[4]	B19_A[4]	C19_A[4]	D19_A[4]
A5	N	AG42		44	A19_A[5]	B19_A[5]	C19_A[5]	D19_A[5]
A6	P	AF42	DBC	44	A19_A[6]	B19_A[6]	C19_A[6]	D19_A[6]
A7	N	AF43	DBC	44	A19_A[7]	B19_A[7]	C19_A[7]	D19_A[7]
A8	P	AE42		44	A19_A[8]	B19_A[8]	C19_A[8]	D19_A[8]
A9	N	AE43		44	A19_A[9]	B19_A[9]	C19_A[9]	D19_A[9]
A10	P	AE41		44	A19_A[10]	B19_A[10]	C19_A[10]	D19_A[10]
A11	N	AD41		44	A19_A[11]	B19_A[11]	C19_A[11]	D19_A[11]
A12	-	AD43		44	A19_A[12]	B19_A[12]	C19_A[12]	D19_A[12]
A13		NC						
B0	P	AE46	GC_QBC	44	A19_B[0]	B19_B[0]	C19_B[0]	D19_B[0]
B1	N	AD46	GC_QBC	44	A19_B[1]	B19_B[1]	C19_B[1]	D19_B[1]
B2	P	AF45		44	A19_B[2]	B19_B[2]	C19_B[2]	D19_B[2]
B3	N	AE45		44	A19_B[3]	B19_B[3]	C19_B[3]	D19_B[3]
B4	P	AD44		44	A19_B[4]	B19_B[4]	C19_B[4]	D19_B[4]
B5	N	AD45		44	A19_B[5]	B19_B[5]	C19_B[5]	D19_B[5]
B6	P	AG45		44	A19_B[6]	B19_B[6]	C19_B[6]	D19_B[6]
B7	N	AG46		44	A19_B[7]	B19_B[7]	C19_B[7]	D19_B[7]
B8	P	AH46		44	A19_B[8]	B19_B[8]	C19_B[8]	D19_B[8]
B9	N	AH47		44	A19_B[9]	B19_B[9]	C19_B[9]	D19_B[9]
B10	P	AH44	DBC	44	A19_B[10]	B19_B[10]	C19_B[10]	D19_B[10]
B11	N	AG44	DBC	44	A19_B[11]	B19_B[11]	C19_B[11]	D19_B[11]
B12		NC						
B13		NC						
C0	P	AE47	GC	44	A19_C[0]	B19_C[0]	C19_C[0]	D19_C[0]
C1	N	AE48	GC	44	A19_C[1]	B19_C[1]	C19_C[1]	D19_C[1]
C2	P	AD48		44	A19_C[2]	B19_C[2]	C19_C[2]	D19_C[2]
C3	N	AD49		44	A19_C[3]	B19_C[3]	C19_C[3]	D19_C[3]
C4	P	AE50		44	A19_C[4]	B19_C[4]	C19_C[4]	D19_C[4]
C5	N	AD50		44	A19_C[5]	B19_C[5]	C19_C[5]	D19_C[5]
C6	P	AG50		44	A19_C[6]	B19_C[6]	C19_C[6]	D19_C[6]
C7	N	AF50		44	A19_C[7]	B19_C[7]	C19_C[7]	D19_C[7]
C8	P	AH49		44	A19_C[8]	B19_C[8]	C19_C[8]	D19_C[8]
C9	N	AG49		44	A19_C[9]	B19_C[9]	C19_C[9]	D19_C[9]
C10	P	AE51		44	A19_C[10]	B19_C[10]	C19_C[10]	D19_C[10]
C11	N	AD51		44	A19_C[11]	B19_C[11]	C19_C[11]	D19_C[11]
C12		NC						
C13		NC						
D0	P	AE52		44	A19_D[0]	B19_D[0]	C19_D[0]	D19_D[0]
D1	N	AE53		44	A19_D[1]	B19_D[1]	C19_D[1]	D19_D[1]
D2	P	AF52	DBC	44	A19_D[2]	B19_D[2]	C19_D[2]	D19_D[2]
D3	N	AF53	DBC	44	A19_D[3]	B19_D[3]	C19_D[3]	D19_D[3]
D4	P	AG51		44	A19_D[4]	B19_D[4]	C19_D[4]	D19_D[4]
D5	N	AG52		44	A19_D[5]	B19_D[5]	C19_D[5]	D19_D[5]
D6	P	AG54		44	A19_D[6]	B19_D[6]	C19_D[6]	D19_D[6]
D7	N	AF54		44	A19_D[7]	B19_D[7]	C19_D[7]	D19_D[7]
D8	P	AH51	DBC	44	A19_D[8]	B19_D[8]	C19_D[8]	D19_D[8]
D9	N	AH52	DBC	44	A19_D[9]	B19_D[9]	C19_D[9]	D19_D[9]
D10	-	AH48		44	A19_D[10]	B19_D[10]	C19_D[10]	D19_D[10]
D11		NC						
D12		NC						
D13		NC						
VRP	-	AH53	VRP	44	A19_VRP	B19_VRP	C19_VRP	D19_VRP
VRN	-	AF44		44	A19_VRN	B19_VRN	C19_VRN	D19_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	AK47	GC	43	A20_A[0]	B20_A[0]	C20_A[0]	D20_A[0]
A1	N	AK48	GC	43	A20_A[1]	B20_A[1]	C20_A[1]	D20_A[1]
A2	P	AL44		43	A20_A[2]	B20_A[2]	C20_A[2]	D20_A[2]
A3	N	AL45		43	A20_A[3]	B20_A[3]	C20_A[3]	D20_A[3]
A4	P	AL42		43	A20_A[4]	B20_A[4]	C20_A[4]	D20_A[4]
A5	N	AM42		43	A20_A[5]	B20_A[5]	C20_A[5]	D20_A[5]
A6	P	AK43	DBC	43	A20_A[6]	B20_A[6]	C20_A[6]	D20_A[6]
A7	N	AL43	DBC	43	A20_A[7]	B20_A[7]	C20_A[7]	D20_A[7]
A8	P	AK41		43	A20_A[8]	B20_A[8]	C20_A[8]	D20_A[8]
A9	N	AK42		43	A20_A[9]	B20_A[9]	C20_A[9]	D20_A[9]
A10	P	AJ43		43	A20_A[10]	B20_A[10]	C20_A[10]	D20_A[10]
A11	N	AJ44		43	A20_A[11]	B20_A[11]	C20_A[11]	D20_A[11]
A12	-	AM41		43	A20_A[12]	B20_A[12]	C20_A[12]	D20_A[12]
A13		NC						
B0	P	AL47	GC_QBC	43	A20_B[0]	B20_B[0]	C20_B[0]	D20_B[0]
B1	N	AL48	GC_QBC	43	A20_B[1]	B20_B[1]	C20_B[1]	D20_B[1]
B2	P	AJ45		43	A20_B[2]	B20_B[2]	C20_B[2]	D20_B[2]
B3	N	AJ46		43	A20_B[3]	B20_B[3]	C20_B[3]	D20_B[3]
B4	P	AK45		43	A20_B[4]	B20_B[4]	C20_B[4]	D20_B[4]
B5	N	AK46		43	A20_B[5]	B20_B[5]	C20_B[5]	D20_B[5]
B6	P	AM46		43	A20_B[6]	B20_B[6]	C20_B[6]	D20_B[6]
B7	N	AM47		43	A20_B[7]	B20_B[7]	C20_B[7]	D20_B[7]
B8	P	AN46		43	A20_B[8]	B20_B[8]	C20_B[8]	D20_B[8]
B9	N	AN47		43	A20_B[9]	B20_B[9]	C20_B[9]	D20_B[9]
B10	P	AM44	DBC	43	A20_B[10]	B20_B[10]	C20_B[10]	D20_B[10]
B11	N	AM45	DBC	43	A20_B[11]	B20_B[11]	C20_B[11]	D20_B[11]
B12		NC						
B13		NC						
C0	P	AJ48	GC	43	A20_C[0]	B20_C[0]	C20_C[0]	D20_C[0]
C1	N	AJ49	GC	43	A20_C[1]	B20_C[1]	C20_C[1]	D20_C[1]
C2	P	AJ50		43	A20_C[2]	B20_C[2]	C20_C[2]	D20_C[2]
C3	N	AK50		43	A20_C[3]	B20_C[3]	C20_C[3]	D20_C[3]
C4	P	AL50		43	A20_C[4]	B20_C[4]	C20_C[4]	D20_C[4]
C5	N	AM50		43	A20_C[5]	B20_C[5]	C20_C[5]	D20_C[5]
C6	P	AJ51		43	A20_C[6]	B20_C[6]	C20_C[6]	D20_C[6]
C7	N	AK51		43	A20_C[7]	B20_C[7]	C20_C[7]	D20_C[7]
C8	P	AM51		43	A20_C[8]	B20_C[8]	C20_C[8]	D20_C[8]
C9	N	AN51		43	A20_C[9]	B20_C[9]	C20_C[9]	D20_C[9]
C10	P	AK52		43	A20_C[10]	B20_C[10]	C20_C[10]	D20_C[10]
C11	N	AL52		43	A20_C[11]	B20_C[11]	C20_C[11]	D20_C[11]
C12		NC						
C13		NC						
D0	P	AL49	GC	43	A20_D[0]	B20_D[0]	C20_D[0]	D20_D[0]
D1	N	AM49	GC	43	A20_D[1]	B20_D[1]	C20_D[1]	D20_D[1]
D2	P	AJ53		43	A20_D[2]	B20_D[2]	C20_D[2]	D20_D[2]
D3	N	AK53		43	A20_D[3]	B20_D[3]	C20_D[3]	D20_D[3]
D4	P	AH54	DBC	43	A20_D[4]	B20_D[4]	C20_D[4]	D20_D[4]
D5	N	AJ54	DBC	43	A20_D[5]	B20_D[5]	C20_D[5]	D20_D[5]
D6	P	AL53		43	A20_D[6]	B20_D[6]	C20_D[6]	D20_D[6]
D7	N	AL54		43	A20_D[7]	B20_D[7]	C20_D[7]	D20_D[7]
D8	P	AM54		43	A20_D[8]	B20_D[8]	C20_D[8]	D20_D[8]
D9	N	AN54		43	A20_D[9]	B20_D[9]	C20_D[9]	D20_D[9]
D10	P	AN52	DBC	43	A20_D[10]	B20_D[10]	C20_D[10]	D20_D[10]
D11	N	AN53	DBC	43	A20_D[11]	B20_D[11]	C20_D[11]	D20_D[11]
D12	-	AN49		43	A20_D[12]	B20_D[12]	C20_D[12]	D20_D[12]
D11		NC						
D12		NC						
D13		NC						
VRP	-	AM52	VRP	43	A20_VRP	B20_VRP	C20_VRP	D20_VRP
VRN	-	AN48		43	A20_VRN	B20_VRN	C20_VRN	D20_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	AR47	GC	42	A21_A[0]	B21_A[0]	C21_A[0]	D21_A[0]
A1	N	AT47	GC	42	A21_A[1]	B21_A[1]	C21_A[1]	D21_A[1]
A2	P	AT42		42	A21_A[2]	B21_A[2]	C21_A[2]	D21_A[2]
A3	N	AT43		42	A21_A[3]	B21_A[3]	C21_A[3]	D21_A[3]
A4	P	AR42		42	A21_A[4]	B21_A[4]	C21_A[4]	D21_A[4]
A5	N	AR43		42	A21_A[5]	B21_A[5]	C21_A[5]	D21_A[5]
A6	P	AP41	DBC	42	A21_A[6]	B21_A[6]	C21_A[6]	D21_A[6]
A7	N	AR41	DBC	42	A21_A[7]	B21_A[7]	C21_A[7]	D21_A[7]
A8	P	AN43		42	A21_A[8]	B21_A[8]	C21_A[8]	D21_A[8]
A9	N	AN44		42	A21_A[9]	B21_A[9]	C21_A[9]	D21_A[9]
A10	P	AP43		42	A21_A[10]	B21_A[10]	C21_A[10]	D21_A[10]
A11	N	AP44		42	A21_A[11]	B21_A[11]	C21_A[11]	D21_A[11]
A12	-	AN42		42	A21_A[12]	B21_A[12]	C21_A[12]	D21_A[12]
A13		NC						
B0	P	AU46	GC_QBC	42	A21_B[0]	B21_B[0]	C21_B[0]	D21_B[0]
B1	N	AU47	GC_QBC	42	A21_B[1]	B21_B[1]	C21_B[1]	D21_B[1]
B2	P	AP45		42	A21_B[2]	B21_B[2]	C21_B[2]	D21_B[2]
B3	N	AP46		42	A21_B[3]	B21_B[3]	C21_B[3]	D21_B[3]
B4	P	AR45		42	A21_B[4]	B21_B[4]	C21_B[4]	D21_B[4]
B5	N	AR46		42	A21_B[5]	B21_B[5]	C21_B[5]	D21_B[5]
B6	P	AT44		42	A21_B[6]	B21_B[6]	C21_B[6]	D21_B[6]
B7	N	AT45		42	A21_B[7]	B21_B[7]	C21_B[7]	D21_B[7]
B8	P	AU44		42	A21_B[8]	B21_B[8]	C21_B[8]	D21_B[8]
B9	N	AU45		42	A21_B[9]	B21_B[9]	C21_B[9]	D21_B[9]
B10	P	AU41	DBC	42	A21_B[10]	B21_B[10]	C21_B[10]	D21_B[10]
B11	N	AU42	DBC	42	A21_B[11]	B21_B[11]	C21_B[11]	D21_B[11]
B12		NC						
B13		NC						
C0	P	AR48	GC	42	A21_C[0]	B21_C[0]	C21_C[0]	D21_C[0]
C1	N	AT48	GC	42	A21_C[1]	B21_C[1]	C21_C[1]	D21_C[1]
C2	P	AP49		42	A21_C[2]	B21_C[2]	C21_C[2]	D21_C[2]
C3	N	AP50		42	A21_C[3]	B21_C[3]	C21_C[3]	D21_C[3]
C4	P	AT50		42	A21_C[4]	B21_C[4]	C21_C[4]	D21_C[4]
C5	N	AU50		42	A21_C[5]	B21_C[5]	C21_C[5]	D21_C[5]
C6	P	AR50		42	A21_C[6]	B21_C[6]	C21_C[6]	D21_C[6]
C7	N	AR51		42	A21_C[7]	B21_C[7]	C21_C[7]	D21_C[7]
C8	P	AU51		42	A21_C[8]	B21_C[8]	C21_C[8]	D21_C[8]
C9	N	AV51		42	A21_C[9]	B21_C[9]	C21_C[9]	D21_C[9]
C10	P	AR52		42	A21_C[10]	B21_C[10]	C21_C[10]	D21_C[10]
C11	N	AT52		42	A21_C[11]	B21_C[11]	C21_C[11]	D21_C[11]
C12		NC						
C13		NC						
D0	P	AT49	GC	42	A21_D[0]	B21_D[0]	C21_D[0]	D21_D[0]
D1	N	AU49	GC	42	A21_D[1]	B21_D[1]	C21_D[1]	D21_D[1]
D2	P	AP53		42	A21_D[2]	B21_D[2]	C21_D[2]	D21_D[2]
D3	N	AP54		42	A21_D[3]	B21_D[3]	C21_D[3]	D21_D[3]
D4	P	AT54	DBC	42	A21_D[4]	B21_D[4]	C21_D[4]	D21_D[4]
D5	N	AU54	DBC	42	A21_D[5]	B21_D[5]	C21_D[5]	D21_D[5]
D6	P	AR53		42	A21_D[6]	B21_D[6]	C21_D[6]	D21_D[6]
D7	N	AT53		42	A21_D[7]	B21_D[7]	C21_D[7]	D21_D[7]
D8	P	AV53		42	A21_D[8]	B21_D[8]	C21_D[8]	D21_D[8]
D9	N	AV54		42	A21_D[9]	B21_D[9]	C21_D[9]	D21_D[9]
D10	P	AU52	DBC	42	A21_D[10]	B21_D[10]	C21_D[10]	D21_D[10]
D11	N	AV52	DBC	42	A21_D[11]	B21_D[11]	C21_D[11]	D21_D[11]
D12	-	AV49		42	A21_D[12]	B21_D[12]	C21_D[12]	D21_D[12]
D13		NC						
VRP	-	AP51	VRP	42	A21_VRP	B21_VRP	C21_VRP	D21_VRP
VRN	-	AP48		42	A21_VRN	B21_VRN	C21_VRN	D21_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BA49	GC	41	A22_A[0]	B22_A[0]	C22_A[0]	D22_A[0]
A1	N	BA50	GC	41	A22_A[1]	B22_A[1]	C22_A[1]	D22_A[1]
A2	P	AY45		41	A22_A[2]	B22_A[2]	C22_A[2]	D22_A[2]
A3	N	AY46		41	A22_A[3]	B22_A[3]	C22_A[3]	D22_A[3]
A4	P	AW43		41	A22_A[4]	B22_A[4]	C22_A[4]	D22_A[4]
A5	N	AW44		41	A22_A[5]	B22_A[5]	C22_A[5]	D22_A[5]
A6	P	AV42	DBC	41	A22_A[6]	B22_A[6]	C22_A[6]	D22_A[6]
A7	N	AV43	DBC	41	A22_A[7]	B22_A[7]	C22_A[7]	D22_A[7]
A8	P	AV44		41	A22_A[8]	B22_A[8]	C22_A[8]	D22_A[8]
A9	N	AW45		41	A22_A[9]	B22_A[9]	C22_A[9]	D22_A[9]
A10	P	AV46		41	A22_A[10]	B22_A[10]	C22_A[10]	D22_A[10]
A11	N	AW46		41	A22_A[11]	B22_A[11]	C22_A[11]	D22_A[11]
A12	-	AW41		41	A22_A[12]	B22_A[12]	C22_A[12]	D22_A[12]
A13		NC						
B0	P	BB49	GC_QBC	41	A22_B[0]	B22_B[0]	C22_B[0]	D22_B[0]
B1	N	BB50	GC_QBC	41	A22_B[1]	B22_B[1]	C22_B[1]	D22_B[1]
B2	P	AY50		41	A22_B[2]	B22_B[2]	C22_B[2]	D22_B[2]
B3	N	AY51		41	A22_B[3]	B22_B[3]	C22_B[3]	D22_B[3]
B4	P	AW50		41	A22_B[4]	B22_B[4]	C22_B[4]	D22_B[4]
B5	N	AW51		41	A22_B[5]	B22_B[5]	C22_B[5]	D22_B[5]
B6	P	AW48		41	A22_B[6]	B22_B[6]	C22_B[6]	D22_B[6]
B7	N	AW49		41	A22_B[7]	B22_B[7]	C22_B[7]	D22_B[7]
B8	P	AV47		41	A22_B[8]	B22_B[8]	C22_B[8]	D22_B[8]
B9	N	AV48		41	A22_B[9]	B22_B[9]	C22_B[9]	D22_B[9]
B10	P	AY43	DBC	41	A22_B[10]	B22_B[10]	C22_B[10]	D22_B[10]
B11	N	BA44	DBC	41	A22_B[11]	B22_B[11]	C22_B[11]	D22_B[11]
B12		NC						
B13		NC						
C0	P	BA47	GC	41	A22_C[0]	B22_C[0]	C22_C[0]	D22_C[0]
C1	N	BA48	GC	41	A22_C[1]	B22_C[1]	C22_C[1]	D22_C[1]
C2	P	BB47		41	A22_C[2]	B22_C[2]	C22_C[2]	D22_C[2]
C3	N	BC47		41	A22_C[3]	B22_C[3]	C22_C[3]	D22_C[3]
C4	P	BB46		41	A22_C[4]	B22_C[4]	C22_C[4]	D22_C[4]
C5	N	BC46		41	A22_C[5]	B22_C[5]	C22_C[5]	D22_C[5]
C6	P	BA45		41	A22_C[6]	B22_C[6]	C22_C[6]	D22_C[6]
C7	N	BB45		41	A22_C[7]	B22_C[7]	C22_C[7]	D22_C[7]
C8	P	BB44		41	A22_C[8]	B22_C[8]	C22_C[8]	D22_C[8]
C9	N	BC44		41	A22_C[9]	B22_C[9]	C22_C[9]	D22_C[9]
C10	P	AW53		41	A22_C[10]	B22_C[10]	C22_C[10]	D22_C[10]
C11	N	AW54		41	A22_C[11]	B22_C[11]	C22_C[11]	D22_C[11]
C12		NC						
C13		NC						
D0	P	AY47	GC	41	A22_D[0]	B22_D[0]	C22_D[0]	D22_D[0]
D1	N	AY48	GC	41	A22_D[1]	B22_D[1]	C22_D[1]	D22_D[1]
D2	P	AY52		41	A22_D[2]	B22_D[2]	C22_D[2]	D22_D[2]
D3	N	AY53		41	A22_D[3]	B22_D[3]	C22_D[3]	D22_D[3]
D4	P	BA52	DBC	41	A22_D[4]	B22_D[4]	C22_D[4]	D22_D[4]
D5	N	BA53	DBC	41	A22_D[5]	B22_D[5]	C22_D[5]	D22_D[5]
D6	P	BB51		41	A22_D[6]	B22_D[6]	C22_D[6]	D22_D[6]
D7	N	BB52		41	A22_D[7]	B22_D[7]	C22_D[7]	D22_D[7]
D8	P	BA54		41	A22_D[8]	B22_D[8]	C22_D[8]	D22_D[8]
D9	N	BB54		41	A22_D[9]	B22_D[9]	C22_D[9]	D22_D[9]
D10	P	BC51	DBC	41	A22_D[10]	B22_D[10]	C22_D[10]	D22_D[10]
D11	N	BC52	DBC	41	A22_D[11]	B22_D[11]	C22_D[11]	D22_D[11]
D12	-	BC48		41	A22_D[12]	B22_D[12]	C22_D[12]	D22_D[12]
D13		NC						
VRP	-	BC53	VRP	41	A22_VRP	B22_VRP	C22_VRP	D22_VRP
VRN	-	BC49		41	A22_VRN	B22_VRN	C22_VRN	D22_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BH51	GC	40	A23_A[0]	B23_A[0]	C23_A[0]	D23_A[0]
A1	N	BJ51	GC	40	A23_A[1]	B23_A[1]	C23_A[1]	D23_A[1]
A2	P	BG52		40	A23_A[2]	B23_A[2]	C23_A[2]	D23_A[2]
A3	N	BH52		40	A23_A[3]	B23_A[3]	C23_A[3]	D23_A[3]
A4	P	BE52		40	A23_A[4]	B23_A[4]	C23_A[4]	D23_A[4]
A5	N	BF52		40	A23_A[5]	B23_A[5]	C23_A[5]	D23_A[5]
A6	P	BF54	DBC	40	A23_A[6]	B23_A[6]	C23_A[6]	D23_A[6]
A7	N	BG54	DBC	40	A23_A[7]	B23_A[7]	C23_A[7]	D23_A[7]
A8	P	BE53		40	A23_A[8]	B23_A[8]	C23_A[8]	D23_A[8]
A9	N	BF53		40	A23_A[9]	B23_A[9]	C23_A[9]	D23_A[9]
A10	P	BD53		40	A23_A[10]	B23_A[10]	C23_A[10]	D23_A[10]
A11	N	BD54		40	A23_A[11]	B23_A[11]	C23_A[11]	D23_A[11]
A12	-	BC54		40	A23_A[12]	B23_A[12]	C23_A[12]	D23_A[12]
A13		NC						
B0	P	BH49	GC_QBC	40	A23_B[0]	B23_B[0]	C23_B[0]	D23_B[0]
B1	N	BJ49	GC_QBC	40	A23_B[1]	B23_B[1]	C23_B[1]	D23_B[1]
B2	P	BJ50		40	A23_B[2]	B23_B[2]	C23_B[2]	D23_B[2]
B3	N	BK50		40	A23_B[3]	B23_B[3]	C23_B[3]	D23_B[3]
B4	P	BK51		40	A23_B[4]	B23_B[4]	C23_B[4]	D23_B[4]
B5	N	BK52		40	A23_B[5]	B23_B[5]	C23_B[5]	D23_B[5]
B6	P	BJ53		40	A23_B[6]	B23_B[6]	C23_B[6]	D23_B[6]
B7	N	BJ54		40	A23_B[7]	B23_B[7]	C23_B[7]	D23_B[7]
B8	P	BL53		40	A23_B[8]	B23_B[8]	C23_B[8]	D23_B[8]
B9	N	BL54		40	A23_B[9]	B23_B[9]	C23_B[9]	D23_B[9]
B10	P	BH53	DBC	40	A23_B[10]	B23_B[10]	C23_B[10]	D23_B[10]
B11	N	BH54	DBC	40	A23_B[11]	B23_B[11]	C23_B[11]	D23_B[11]
B12		NC						
B13		NC						
C0	P	BG50	GC	40	A23_C[0]	B23_C[0]	C23_C[0]	D23_C[0]
C1	N	BG51	GC	40	A23_C[1]	B23_C[1]	C23_C[1]	D23_C[1]
C2	P	BD51		40	A23_C[2]	B23_C[2]	C23_C[2]	D23_C[2]
C3	N	BE51		40	A23_C[3]	B23_C[3]	C23_C[3]	D23_C[3]
C4	P	BD50		40	A23_C[4]	B23_C[4]	C23_C[4]	D23_C[4]
C5	N	BE50		40	A23_C[5]	B23_C[5]	C23_C[5]	D23_C[5]
C6	P	BD48		40	A23_C[6]	B23_C[6]	C23_C[6]	D23_C[6]
C7	N	BD49		40	A23_C[7]	B23_C[7]	C23_C[7]	D23_C[7]
C8	P	BE48		40	A23_C[8]	B23_C[8]	C23_C[8]	D23_C[8]
C9	N	BF48		40	A23_C[9]	B23_C[9]	C23_C[9]	D23_C[9]
C10	P	BH48		40	A23_C[10]	B23_C[10]	C23_C[10]	D23_C[10]
C11	N	BJ48		40	A23_C[11]	B23_C[11]	C23_C[11]	D23_C[11]
C12		NC						
C13		NC						
D0	P	BF49	GC	40	A23_D[0]	B23_D[0]	C23_D[0]	D23_D[0]
D1	N	BG49	GC	40	A23_D[1]	B23_D[1]	C23_D[1]	D23_D[1]
D2	P	BG47		40	A23_D[2]	B23_D[2]	C23_D[2]	D23_D[2]
D3	N	BH47		40	A23_D[3]	B23_D[3]	C23_D[3]	D23_D[3]
D4	P	BG46	DBC	40	A23_D[4]	B23_D[4]	C23_D[4]	D23_D[4]
D5	N	BH46	DBC	40	A23_D[5]	B23_D[5]	C23_D[5]	D23_D[5]
D6	P	BE47		40	A23_D[6]	B23_D[6]	C23_D[6]	D23_D[6]
D7	N	BF47		40	A23_D[7]	B23_D[7]	C23_D[7]	D23_D[7]
D8	P	BD46		40	A23_D[8]	B23_D[8]	C23_D[8]	D23_D[8]
D9	N	BE46		40	A23_D[9]	B23_D[9]	C23_D[9]	D23_D[9]
D10	P	BE45	DBC	40	A23_D[10]	B23_D[10]	C23_D[10]	D23_D[10]
D11	N	BF45	DBC	40	A23_D[11]	B23_D[11]	C23_D[11]	D23_D[11]
D12	-	BF50		40	A23_D[12]	B23_D[12]	C23_D[12]	D23_D[12]
D13		NC						
VRP	-	BJ46	VRP	40	A23_VRP	B23_VRP	C23_VRP	D23_VRP
VRN	-	BK53		40	A23_VRN	B23_VRN	C23_VRN	D23_VRN

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HT3		XCVU440 - FLGA2892 SLR 0			PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Info	Bank	FPGA A	FPGA B	FPGA C	FPGA D
A0	P	BL47	GC	39	A24_A[0]	B24_A[0]	C24_A[0]	D24_A[0]
A1	N	BM47	GC	39	A24_A[1]	B24_A[1]	C24_A[1]	D24_A[1]
A2	P	BL50		39	A24_A[2]	B24_A[2]	C24_A[2]	D24_A[2]
A3	N	BM50		39	A24_A[3]	B24_A[3]	C24_A[3]	D24_A[3]
A4	P	BN49		39	A24_A[4]	B24_A[4]	C24_A[4]	D24_A[4]
A5	N	BP49		39	A24_A[5]	B24_A[5]	C24_A[5]	D24_A[5]
A6	P	BP50	DBC	39	A24_A[6]	B24_A[6]	C24_A[6]	D24_A[6]
A7	N	BP51	DBC	39	A24_A[7]	B24_A[7]	C24_A[7]	D24_A[7]
A8	P	BM51		39	A24_A[8]	B24_A[8]	C24_A[8]	D24_A[8]
A9	N	BN51		39	A24_A[9]	B24_A[9]	C24_A[9]	D24_A[9]
A10	P	BM52		39	A24_A[10]	B24_A[10]	C24_A[10]	D24_A[10]
A11	N	BN52		39	A24_A[11]	B24_A[11]	C24_A[11]	D24_A[11]
A12	-	BL52		39	A24_A[12]	B24_A[12]	C24_A[12]	D24_A[12]
A13		NC						
B0	P	BM45	GC_QBC	39	A24_B[0]	B24_B[0]	C24_B[0]	D24_B[0]
B1	N	BM46	GC_QBC	39	A24_B[1]	B24_B[1]	C24_B[1]	D24_B[1]
B2	P	BN46		39	A24_B[2]	B24_B[2]	C24_B[2]	D24_B[2]
B3	N	BN47		39	A24_B[3]	B24_B[3]	C24_B[3]	D24_B[3]
B4	P	BP45		39	A24_B[4]	B24_B[4]	C24_B[4]	D24_B[4]
B5	N	BP46		39	A24_B[5]	B24_B[5]	C24_B[5]	D24_B[5]
B6	P	BK47		39	A24_B[6]	B24_B[6]	C24_B[6]	D24_B[6]
B7	N	BK48		39	A24_B[7]	B24_B[7]	C24_B[7]	D24_B[7]
B8	P	BN48		39	A24_B[8]	B24_B[8]	C24_B[8]	D24_B[8]
B9	N	BP48		39	A24_B[9]	B24_B[9]	C24_B[9]	D24_B[9]
B10	P	BL49	DBC	39	A24_B[10]	B24_B[10]	C24_B[10]	D24_B[10]
B11	N	BM49	DBC	39	A24_B[11]	B24_B[11]	C24_B[11]	D24_B[11]
B12		NC						
B13		NC						
C0	P	BL43	GC	39	A24_C[0]	B24_C[0]	C24_C[0]	D24_C[0]
C1	N	BM44	GC	39	A24_C[1]	B24_C[1]	C24_C[1]	D24_C[1]
C2	P	BP43		39	A24_C[2]	B24_C[2]	C24_C[2]	D24_C[2]
C3	N	BP44		39	A24_C[3]	B24_C[3]	C24_C[3]	D24_C[3]
C4	P	BN43		39	A24_C[4]	B24_C[4]	C24_C[4]	D24_C[4]
C5	N	BN44		39	A24_C[5]	B24_C[5]	C24_C[5]	D24_C[5]
C6	P	BN41		39	A24_C[6]	B24_C[6]	C24_C[6]	D24_C[6]
C7	N	BN42		39	A24_C[7]	B24_C[7]	C24_C[7]	D24_C[7]
C8	P	BM41		39	A24_C[8]	B24_C[8]	C24_C[8]	D24_C[8]
C9	N	BM42		39	A24_C[9]	B24_C[9]	C24_C[9]	D24_C[9]
C10	P	BP40		39	A24_C[10]	B24_C[10]	C24_C[10]	D24_C[10]
C11	N	BP41		39	A24_C[11]	B24_C[11]	C24_C[11]	D24_C[11]
C12		NC						
C13		NC						
D0	P	BL44	GC	39	A24_D[0]	B24_D[0]	C24_D[0]	D24_D[0]
D1	N	BL45	GC	39	A24_D[1]	B24_D[1]	C24_D[1]	D24_D[1]
D2	P	BP38		39	A24_D[2]	B24_D[2]	C24_D[2]	D24_D[2]
D3	N	BP39		39	A24_D[3]	B24_D[3]	C24_D[3]	D24_D[3]
D4	P	BM37	DBC	39	A24_D[4]	B24_D[4]	C24_D[4]	D24_D[4]
D5	N	BN37	DBC	39	A24_D[5]	B24_D[5]	C24_D[5]	D24_D[5]
D6	P	BN38		39	A24_D[6]	B24_D[6]	C24_D[6]	D24_D[6]
D7	N	BN39		39	A24_D[7]	B24_D[7]	C24_D[7]	D24_D[7]
D8	P	BM39		39	A24_D[8]	B24_D[8]	C24_D[8]	D24_D[8]
D9	N	BM40		39	A24_D[9]	B24_D[9]	C24_D[9]	D24_D[9]
D10	P	BL39	DBC	39	A24_D[10]	B24_D[10]	C24_D[10]	D24_D[10]
D11	N	BL40	DBC	39	A24_D[11]	B24_D[11]	C24_D[11]	D24_D[11]
D12	-	BL42		39	A24_D[12]	B24_D[12]	C24_D[12]	D24_D[12]
D13		NC						
VRP	-	BL38	VRP	39	A24_VRP	B24_VRP	C24_VRP	D24_VRP
VRN	-	BL48		39	A24_VRN	B24_VRN	C24_VRN	D24_VRN

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Inter-FPGA Connections

High-Speed SerDes Channels

24 GTH high-speed SerDes channels built-in interconnects per FPGA. More information on page 24.

High-Speed SerDes Channels FPGA A / FPGA B

High-Speed SerDes Channels FPGA B / FPGA C

High-Speed SerDes Channels FPGA A / FPGA C

High-Speed SerDes Channels FPGA B / FPGA D

High-Speed SerDes Channels FPGA A / FPGA D

High-Speed SerDes Channels FPGA C / FPGA D

Signal I/O Connections

Fixed inter-FPGA signal I/O connections between FPGAs A and D, and between FPGAs B and C. More information on page 24.

Signal I/O Connections FPGA A / FPGA D

Signal I/O Connections FPGA B / FGPA C

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High-Speed SerDes Channels FPGA A / FPGA B

FPGA A SLR 1			PCB-Trace Names (Partition Mode) HAPS-80 S104		FPGA B SLR 2			
Quad	Pin	Type	FPGA A	FPGA B	Type	Pin	Quad	
226	AF10	P	MGBLINK_AI1_REFCLKP[0]	MGBLINK_BI3_REFCLKP[2]	P	C8	232	150MHz fixed
226	AF9	N	MGBLINK_AI1_REFCLKN[0]	MGBLINK_BI3_REFCLKN[2]	N	C7	232	150MHz fixed
226	AG8	P	MGBLINK_AI1_TO_BI3_FIXED_P[0]		P	C4	232	
226	AG7	N	MGBLINK_AI1_TO_BI3_FIXED_N[0]		N	C3	232	
226	AF6	P	MGBLINK_AI1_TO_BI3_FIXED_P[1]		P	D2	232	
226	AF5	N	MGBLINK_AI1_TO_BI3_FIXED_N[1]		N	D1	232	
226	AE8	P	MGBLINK_AI1_TO_BI3_FIXED_P[2]		P	F2	232	Reserved for
226	AE7	N	MGBLINK_AI1_TO_BI3_FIXED_N[2]		N	F1	232	internal use
226	AD6	P	MGBLINK_AI1_TO_BI3_FIXED_P[3]		P	G4	232	
226	AD5	N	MGBLINK_AI1_TO_BI3_FIXED_N[3]		N	G3	232	
226	AD2	P	MGBLINK_BI3_TO_AI1_FIXED_P[4]		P	G8	232	
226	AD1	N	MGBLINK_BI3_TO_AI1_FIXED_N[4]		N	G7	232	
226	AE4	P	MGBLINK_BI3_TO_AI1_FIXED_P[5]		P	F6	232	
226	AE3	N	MGBLINK_BI3_TO_AI1_FIXED_N[5]		N	F5	232	
226	AF2	P	MGBLINK_BI3_TO_AI1_FIXED_P[6]		P	E4	232	
226	AF1	N	MGBLINK_BI3_TO_AI1_FIXED_N[6]		N	E3	232	
226	AG4	P	MGBLINK_BI3_TO_AI1_FIXED_P[7]		P	D6	232	
226	AG3	N	MGBLINK_BI3_TO_AI1_FIXED_N[7]		N	D5	232	
227	AB10	P	MGBLINK_AI1_REFCLKP[2]	MGBLINK_BI3_REFCLKP[0]	P	H10	231	150MHz fixed
227	AB9	N	MGBLINK_AI1_REFCLKN[2]	MGBLINK_BI3_REFCLKN[0]	N	H9	231	150MHz fixed
227	AC8	P	MGBLINK_AI1_TO_BI3_FIXED_P[4]		P	H2	231	
227	AC7	N	MGBLINK_AI1_TO_BI3_FIXED_N[4]		N	H1	231	
227	AB6	P	MGBLINK_AI1_TO_BI3_FIXED_P[5]		P	J4	231	
227	AB5	N	MGBLINK_AI1_TO_BI3_FIXED_N[5]		N	J3	231	
227	AA8	P	MGBLINK_AI1_TO_BI3_FIXED_P[6]		P	K2	231	
227	AA7	N	MGBLINK_AI1_TO_BI3_FIXED_N[6]		N	K1	231	
227	Y6	P	MGBLINK_AI1_TO_BI3_FIXED_P[7]		P	L4	231	
227	Y5	N	MGBLINK_AI1_TO_BI3_FIXED_N[7]		N	L3	231	
227	Y2	P	MGBLINK_BI3_TO_AI1_FIXED_P[0]		P	L8	231	
227	Y1	N	MGBLINK_BI3_TO_AI1_FIXED_N[0]		N	L7	231	
227	AA4	P	MGBLINK_BI3_TO_AI1_FIXED_P[1]		P	K6	231	
227	AA3	N	MGBLINK_BI3_TO_AI1_FIXED_N[1]		N	K5	231	
227	AB2	P	MGBLINK_BI3_TO_AI1_FIXED_P[2]		P	J8	231	
227	AB1	N	MGBLINK_BI3_TO_AI1_FIXED_N[2]		N	J7	231	
227	AC4	P	MGBLINK_BI3_TO_AI1_FIXED_P[3]		P	H6	231	
227	AC3	N	MGBLINK_BI3_TO_AI1_FIXED_N[3]		N	H5	231	

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High-Speed SerDes Channels FPGA A / FPGA C

FPGA A SLR 2			PCB-Trace Names (Partition Mode) HAPS-80 S104		FPGA C SLR 2			
Quad	Pin	Type	FPGA A	FPGA C	Type	Pin	Quad	
229	T10	P	MGBLINK_AI2_REFCLKP[0]	MGBLINK_CI2_REFCLKP[2]	P	M10	230	150MHz fixed
229	T9	N	MGBLINK_AI2_REFCLKN[0]	MGBLINK_CI2_REFCLKN[2]	N	M9	230	150MHz fixed
229	W8	P	MGBLINK_AI2_TO_CI2_FIXED_P[0]		P	M2	230	
229	W7	N	MGBLINK_AI2_TO_CI2_FIXED_N[0]		N	M1	230	
229	V6	P	MGBLINK_AI2_TO_CI2_FIXED_P[1]		P	N4	230	
229	V5	N	MGBLINK_AI2_TO_CI2_FIXED_N[1]		N	N3	230	
229	U8	P	MGBLINK_AI2_TO_CI2_FIXED_P[2]		P	P2	230	Reserved for
229	U7	N	MGBLINK_AI2_TO_CI2_FIXED_N[2]		N	P1	230	internal use
229	T6	P	MGBLINK_AI2_TO_CI2_FIXED_P[3]		P	R4	230	
229	T5	N	MGBLINK_AI2_TO_CI2_FIXED_N[3]		N	R3	230	
229	T2	P	MGBLINK_CI2_TO_AI2_FIXED_P[4]		P	R8	230	
229	T1	N	MGBLINK_CI2_TO_AI2_FIXED_N[4]		N	R7	230	
229	U4	P	MGBLINK_CI2_TO_AI2_FIXED_P[5]		P	P6	230	
229	U3	N	MGBLINK_CI2_TO_AI2_FIXED_N[5]		N	P5	230	
229	V2	P	MGBLINK_CI2_TO_AI2_FIXED_P[6]		P	N8	230	
229	V1	N	MGBLINK_CI2_TO_AI2_FIXED_N[6]		N	N7	230	
229	W4	P	MGBLINK_CI2_TO_AI2_FIXED_P[7]		P	M6	230	
229	W3	N	MGBLINK_CI2_TO_AI2_FIXED_N[7]		N	M5	230	
230	M10	P	MGBLINK_AI2_REFCLKP[2]	MGBLINK_CI2_REFCLKP[0]	P	T10	229	150MHz fixed
230	M9	N	MGBLINK_AI2_REFCLKN[2]	MGBLINK_CI2_REFCLKN[0]	N	T9	229	150MHz fixed
230	R8	P	MGBLINK_AI2_TO_CI2_FIXED_P[4]		P	T2	229	
230	R7	N	MGBLINK_AI2_TO_CI2_FIXED_N[4]		N	T1	229	
230	P6	P	MGBLINK_AI2_TO_CI2_FIXED_P[5]		P	U4	229	
230	P5	N	MGBLINK_AI2_TO_CI2_FIXED_N[5]		N	U3	229	
230	N8	P	MGBLINK_AI2_TO_CI2_FIXED_P[6]		P	V2	229	
230	N7	N	MGBLINK_AI2_TO_CI2_FIXED_N[6]		N	V1	229	
230	M6	P	MGBLINK_AI2_TO_CI2_FIXED_P[7]		P	W4	229	
230	M5	N	MGBLINK_AI2_TO_CI2_FIXED_N[7]		N	W3	229	
230	M2	P	MGBLINK_CI2_TO_AI2_FIXED_P[0]		P	W8	229	
230	M1	N	MGBLINK_CI2_TO_AI2_FIXED_N[0]		N	W7	229	
230	N4	P	MGBLINK_CI2_TO_AI2_FIXED_P[1]		P	V6	229	
230	N3	N	MGBLINK_CI2_TO_AI2_FIXED_N[1]		N	V5	229	
230	P2	P	MGBLINK_CI2_TO_AI2_FIXED_P[2]		P	U8	229	
230	P1	N	MGBLINK_CI2_TO_AI2_FIXED_N[2]		N	U7	229	
230	R4	P	MGBLINK_CI2_TO_AI2_FIXED_P[3]		P	T6	229	
230	R3	N	MGBLINK_CI2_TO_AI2_FIXED_N[3]		N	T5	229	

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High-Speed SerDes Channels FPGA A / FPGA D

FPGA A SLR 2			PCB-Trace Names (Partition Mode) HAPS-80 S104		FPGA D SLR 1			
Quad	Pin	Type	FPGA A	FPGA D	Type	Pin	Quad	
231	H10	P	MGBLINK_AI3_REFCLKP[0]	MGBLINK_DI1_REFCLKP[2]	P	AB10	227	150MHz fixed
231	H9	N	MGBLINK_AI3_REFCLKN[0]	MGBLINK_DI1_REFCLKN[2]	N	AB9	227	150MHz fixed
231	L8	P	MGBLINK_AI3_TO_DI1_FIXED_P[0]		P	Y2	227	
231	L7	N	MGBLINK_AI3_TO_DI1_FIXED_N[0]		N	Y1	227	
231	K6	P	MGBLINK_AI3_TO_DI1_FIXED_P[1]		P	AA4	227	
231	K5	N	MGBLINK_AI3_TO_DI1_FIXED_N[1]		N	AA3	227	
231	J8	P	MGBLINK_AI3_TO_DI1_FIXED_P[2]		P	AB2	227	Reserved for
231	J7	N	MGBLINK_AI3_TO_DI1_FIXED_N[2]		N	AB1	227	internal use
231	H6	P	MGBLINK_AI3_TO_DI1_FIXED_P[3]		P	AC4	227	
231	H5	N	MGBLINK_AI3_TO_DI1_FIXED_N[3]		N	AC3	227	
231	H2	P	MGBLINK_DI1_TO_AI3_FIXED_P[4]		P	AC8	227	
231	H1	N	MGBLINK_DI1_TO_AI3_FIXED_N[4]		N	AC7	227	
231	J4	P	MGBLINK_DI1_TO_AI3_FIXED_P[5]		P	AB6	227	
231	J3	N	MGBLINK_DI1_TO_AI3_FIXED_N[5]		N	AB5	227	
231	K2	P	MGBLINK_DI1_TO_AI3_FIXED_P[6]		P	AA8	227	
231	K1	N	MGBLINK_DI1_TO_AI3_FIXED_N[6]		N	AA7	227	
231	L4	P	MGBLINK_DI1_TO_AI3_FIXED_P[7]		P	Y6	227	
231	L3	N	MGBLINK_DI1_TO_AI3_FIXED_N[7]		N	Y5	227	
232	C8	P	MGBLINK_AI3_REFCLKP[2]	MGBLINK_DI1_REFCLKP[0]	P	AF10	226	150MHz fixed
232	C7	N	MGBLINK_AI3_REFCLKN[2]	MGBLINK_DI1_REFCLKN[0]	N	AF9	226	150MHz fixed
232	G8	P	MGBLINK_AI3_TO_DI1_FIXED_P[4]		P	AD2	226	
232	G7	N	MGBLINK_AI3_TO_DI1_FIXED_N[4]		N	AD1	226	
232	F6	P	MGBLINK_AI3_TO_DI1_FIXED_P[5]		P	AE4	226	
232	F5	N	MGBLINK_AI3_TO_DI1_FIXED_N[5]		N	AE3	226	
232	E4	P	MGBLINK_AI3_TO_DI1_FIXED_P[6]		P	AF2	226	Reserved for
232	E3	N	MGBLINK_AI3_TO_DI1_FIXED_N[6]		N	AF1	226	internal use
232	D6	P	MGBLINK_AI3_TO_DI1_FIXED_P[7]		P	AG4	226	
232	D5	N	MGBLINK_AI3_TO_DI1_FIXED_N[7]		N	AG3	226	
232	C4	P	MGBLINK_DI1_TO_AI3_FIXED_P[0]		P	AG8	226	
232	C3	N	MGBLINK_DI1_TO_AI3_FIXED_N[0]		N	AG7	226	
232	D2	P	MGBLINK_DI1_TO_AI3_FIXED_P[1]		P	AF6	226	
232	D1	N	MGBLINK_DI1_TO_AI3_FIXED_N[1]		N	AF5	226	
232	F2	P	MGBLINK_DI1_TO_AI3_FIXED_P[2]		P	AE8	226	
232	F1	N	MGBLINK_DI1_TO_AI3_FIXED_N[2]		N	AE7	226	
232	G4	P	MGBLINK_DI1_TO_AI3_FIXED_P[3]		P	AD6	226	
232	G3	N	MGBLINK_DI1_TO_AI3_FIXED_N[3]		N	AD5	226	

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High-Speed SerDes Channels FPGA B / FPGA C

FPGA B SLR 1			PCB-Trace Names (Partition Mode) HAPS-80 S104		FPGA C SLR 2			
Quad	Pin	Type	FPGA B	FPGA C	Type	Pin	Quad	
226	AF10	P	MGBLINK_BI1_REFCLKP[0]	MGBLINK_CI3_REFCLKP[2]	P	C8	232	150MHz fixed
226	AF9	N	MGBLINK_BI1_REFCLKN[0]	MGBLINK_CI3_REFCLKN[2]	N	C7	232	150MHz fixed
226	AG8	P	MGBLINK_BI1_TO_CI3_FIXED_P[0]		P	C4	232	
226	AG7	N	MGBLINK_BI1_TO_CI3_FIXED_N[0]		N	C3	232	
226	AF6	P	MGBLINK_BI1_TO_CI3_FIXED_P[1]		P	D2	232	
226	AF5	N	MGBLINK_BI1_TO_CI3_FIXED_N[1]		N	D1	232	
226	AE8	P	MGBLINK_BI1_TO_CI3_FIXED_P[2]		P	F2	232	
226	AE7	N	MGBLINK_BI1_TO_CI3_FIXED_N[2]		N	F1	232	
226	AD6	P	MGBLINK_BI1_TO_CI3_FIXED_P[3]		P	G4	232	
226	AD5	N	MGBLINK_BI1_TO_CI3_FIXED_N[3]		N	G3	232	
226	AD2	P	MGBLINK_CI3_TO_BI1_FIXED_P[4]		P	G8	232	
226	AD1	N	MGBLINK_CI3_TO_BI1_FIXED_N[4]		N	G7	232	
226	AE4	P	MGBLINK_CI3_TO_BI1_FIXED_P[5]		P	F6	232	
226	AE3	N	MGBLINK_CI3_TO_BI1_FIXED_N[5]		N	F5	232	
226	AF2	P	MGBLINK_CI3_TO_BI1_FIXED_P[6]		P	E4	232	
226	AF1	N	MGBLINK_CI3_TO_BI1_FIXED_N[6]		N	E3	232	
226	AG4	P	MGBLINK_CI3_TO_BI1_FIXED_P[7]		P	D6	232	
226	AG3	N	MGBLINK_CI3_TO_BI1_FIXED_N[7]		N	D5	232	
227	AB10	P	MGBLINK_BI1_REFCLKP[2]	MGBLINK_CI3_REFCLKP[0]	P	H10	231	150MHz fixed
227	AB9	N	MGBLINK_BI1_REFCLKN[2]	MGBLINK_CI3_REFCLKN[0]	N	H9	231	150MHz fixed
227	AC8	P	MGBLINK_BI1_TO_CI3_FIXED_P[4]		P	H2	231	
227	AC7	N	MGBLINK_BI1_TO_CI3_FIXED_N[4]		N	H1	231	
227	AB6	P	MGBLINK_BI1_TO_CI3_FIXED_P[5]		P	J4	231	
227	AB5	N	MGBLINK_BI1_TO_CI3_FIXED_N[5]		N	J3	231	
227	AA8	P	MGBLINK_BI1_TO_CI3_FIXED_P[6]		P	K2	231	
227	AA7	N	MGBLINK_BI1_TO_CI3_FIXED_N[6]		N	K1	231	
227	Y6	P	MGBLINK_BI1_TO_CI3_FIXED_P[7]		P	L4	231	
227	Y5	N	MGBLINK_BI1_TO_CI3_FIXED_N[7]		N	L3	231	
227	Y2	P	MGBLINK_CI3_TO_BI1_FIXED_P[0]		P	L8	231	
227	Y1	N	MGBLINK_CI3_TO_BI1_FIXED_N[0]		N	L7	231	
227	AA4	P	MGBLINK_CI3_TO_BI1_FIXED_P[1]		P	K6	231	
227	AA3	N	MGBLINK_CI3_TO_BI1_FIXED_N[1]		N	K5	231	
227	AB2	P	MGBLINK_CI3_TO_BI1_FIXED_P[2]		P	J8	231	
227	AB1	N	MGBLINK_CI3_TO_BI1_FIXED_N[2]		N	J7	231	
227	AC4	P	MGBLINK_CI3_TO_BI1_FIXED_P[3]		P	H6	231	
227	AC3	N	MGBLINK_CI3_TO_BI1_FIXED_N[3]		N	H5	231	

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High-Speed SerDes Channels FPGA B / FPGA D

FPGA B SLR 2			PCB-Trace Names (Partition Mode) HAPS-80 S104		FPGA D SLR 2			
Quad	Pin	Type	FPGA B	FPGA D	Type	Pin	Quad	
229	T10	P	MGBLINK_BI2_REFCLKP[0]	MGBLINK_DI2_REFCLKP[2]	P	M10	230	150MHz fixed
229	T9	N	MGBLINK_BI2_REFCLKN[0]	MGBLINK_DI2_REFCLKN[2]	N	M9	230	150MHz fixed
229	W8	P	MGBLINK_BI2_TO_DI2_FIXED_P[0]		P	M2	230	
229	W7	N	MGBLINK_BI2_TO_DI2_FIXED_N[0]		N	M1	230	
229	V6	P	MGBLINK_BI2_TO_DI2_FIXED_P[1]		P	N4	230	
229	V5	N	MGBLINK_BI2_TO_DI2_FIXED_N[1]		N	N3	230	
229	U8	P	MGBLINK_BI2_TO_DI2_FIXED_P[2]		P	P2	230	
229	U7	N	MGBLINK_BI2_TO_DI2_FIXED_N[2]		N	P1	230	
229	T6	P	MGBLINK_BI2_TO_DI2_FIXED_P[3]		P	R4	230	
229	T5	N	MGBLINK_BI2_TO_DI2_FIXED_N[3]		N	R3	230	
229	T2	P	MGBLINK_DI2_TO_BI2_FIXED_P[4]		P	R8	230	
229	T1	N	MGBLINK_DI2_TO_BI2_FIXED_N[4]		N	R7	230	
229	U4	P	MGBLINK_DI2_TO_BI2_FIXED_P[5]		P	P6	230	
229	U3	N	MGBLINK_DI2_TO_BI2_FIXED_N[5]		N	P5	230	
229	V2	P	MGBLINK_DI2_TO_BI2_FIXED_P[6]		P	N8	230	
229	V1	N	MGBLINK_DI2_TO_BI2_FIXED_N[6]		N	N7	230	
229	W4	P	MGBLINK_DI2_TO_BI2_FIXED_P[7]		P	M6	230	
229	W3	N	MGBLINK_DI2_TO_BI2_FIXED_N[7]		N	M5	230	
230	M10	P	MGBLINK_BI2_REFCLKP[2]	MGBLINK_DI2_REFCLKP[0]	P	T10	229	150MHz fixed
230	M9	N	MGBLINK_BI2_REFCLKN[2]	MGBLINK_DI2_REFCLKN[0]	N	T9	229	150MHz fixed
230	R8	P	MGBLINK_BI2_TO_DI2_FIXED_P[4]		P	T2	229	
230	R7	N	MGBLINK_BI2_TO_DI2_FIXED_N[4]		N	T1	229	
230	P6	P	MGBLINK_BI2_TO_DI2_FIXED_P[5]		P	U4	229	
230	P5	N	MGBLINK_BI2_TO_DI2_FIXED_N[5]		N	U3	229	
230	N8	P	MGBLINK_BI2_TO_DI2_FIXED_P[6]		P	V2	229	
230	N7	N	MGBLINK_BI2_TO_DI2_FIXED_N[6]		N	V1	229	
230	M6	P	MGBLINK_BI2_TO_DI2_FIXED_P[7]		P	W4	229	
230	M5	N	MGBLINK_BI2_TO_DI2_FIXED_N[7]		N	W3	229	
230	M2	P	MGBLINK_DI2_TO_BI2_FIXED_P[0]		P	W8	229	
230	M1	N	MGBLINK_DI2_TO_BI2_FIXED_N[0]		N	W7	229	
230	N4	P	MGBLINK_DI2_TO_BI2_FIXED_P[1]		P	V6	229	
230	N3	N	MGBLINK_DI2_TO_BI2_FIXED_N[1]		N	V5	229	
230	P2	P	MGBLINK_DI2_TO_BI2_FIXED_P[2]		P	U8	229	
230	P1	N	MGBLINK_DI2_TO_BI2_FIXED_N[2]		N	U7	229	
230	R4	P	MGBLINK_DI2_TO_BI2_FIXED_P[3]		P	T6	229	
230	R3	N	MGBLINK_DI2_TO_BI2_FIXED_N[3]		N	T5	229	

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High-Speed SerDes Channels FPGA C / FPGA D

FPGA C SLR 1			PCB-Trace Names (Partition Mode) HAPS-80 S104		FPGA D SLR 2			
Quad	Pin	Type	FPGA C	FPGA D	Type	Pin	Quad	
226	AF10	P	MGBLINK_CI1_REFCLKP[0]	MGBLINK_DI3_REFCLKP[2]	P	C8	232	150MHz fixed
226	AF9	N	MGBLINK_CI1_REFCLKN[0]	MGBLINK_DI3_REFCLKN[2]	N	C7	232	150MHz fixed
226	AG8	P	MGBLINK_CI1_TO_DI3_FIXED_P[0]		P	C4	232	
226	AG7	N	MGBLINK_CI1_TO_DI3_FIXED_N[0]		N	C3	232	
226	AF6	P	MGBLINK_CI1_TO_DI3_FIXED_P[1]		P	D2	232	
226	AF5	N	MGBLINK_CI1_TO_DI3_FIXED_N[1]		N	D1	232	
226	AE8	P	MGBLINK_CI1_TO_DI3_FIXED_P[2]		P	F2	232	
226	AE7	N	MGBLINK_CI1_TO_DI3_FIXED_N[2]		N	F1	232	
226	AD6	P	MGBLINK_CI1_TO_DI3_FIXED_P[3]		P	G4	232	
226	AD5	N	MGBLINK_CI1_TO_DI3_FIXED_N[3]		N	G3	232	
226	AD2	P	MGBLINK_DI3_TO_CI1_FIXED_P[4]		P	G8	232	
226	AD1	N	MGBLINK_DI3_TO_CI1_FIXED_N[4]		N	G7	232	
226	AE4	P	MGBLINK_DI3_TO_CI1_FIXED_P[5]		P	F6	232	
226	AE3	N	MGBLINK_DI3_TO_CI1_FIXED_N[5]		N	F5	232	
226	AF2	P	MGBLINK_DI3_TO_CI1_FIXED_P[6]		P	E4	232	
226	AF1	N	MGBLINK_DI3_TO_CI1_FIXED_N[6]		N	E3	232	
226	AG4	P	MGBLINK_DI3_TO_CI1_FIXED_P[7]		P	D6	232	
226	AG3	N	MGBLINK_DI3_TO_CI1_FIXED_N[7]		N	D5	232	
227	AB10	P	MGBLINK_CI1_REFCLKP[2]	MGBLINK_DI3_REFCLKP[0]	P	H10	231	150MHz fixed
227	AB9	N	MGBLINK_CI1_REFCLKN[2]	MGBLINK_DI3_REFCLKN[0]	N	H9	231	150MHz fixed
227	AC8	P	MGBLINK_CI1_TO_DI3_FIXED_P[4]		P	H2	231	
227	AC7	N	MGBLINK_CI1_TO_DI3_FIXED_N[4]		N	H1	231	
227	AB6	P	MGBLINK_CI1_TO_DI3_FIXED_P[5]		P	J4	231	
227	AB5	N	MGBLINK_CI1_TO_DI3_FIXED_N[5]		N	J3	231	
227	AA8	P	MGBLINK_CI1_TO_DI3_FIXED_P[6]		P	K2	231	
227	AA7	N	MGBLINK_CI1_TO_DI3_FIXED_N[6]		N	K1	231	
227	Y6	P	MGBLINK_CI1_TO_DI3_FIXED_P[7]		P	L4	231	
227	Y5	N	MGBLINK_CI1_TO_DI3_FIXED_N[7]		N	L3	231	
227	Y2	P	MGBLINK_DI3_TO_CI1_FIXED_P[0]		P	L8	231	
227	Y1	N	MGBLINK_DI3_TO_CI1_FIXED_N[0]		N	L7	231	
227	AA4	P	MGBLINK_DI3_TO_CI1_FIXED_P[1]		P	K6	231	
227	AA3	N	MGBLINK_DI3_TO_CI1_FIXED_N[1]		N	K5	231	
227	AB2	P	MGBLINK_DI3_TO_CI1_FIXED_P[2]		P	J8	231	
227	AB1	N	MGBLINK_DI3_TO_CI1_FIXED_N[2]		N	J7	231	
227	AC4	P	MGBLINK_DI3_TO_CI1_FIXED_P[3]		P	H6	231	
227	AC3	N	MGBLINK_DI3_TO_CI1_FIXED_N[3]		N	H5	231	

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Signal I/O Connections FPGA A / FPGA D

XCVU440 -FLGA2892 FPGA A SLR 2			A - D			XCVU440 -FLGA2892 FPGA D SLR 2		
Bank	Info	Pin	Type	PCB-Trace Name	Type	Pin	Info	Bank
51	DBC	T35	N	AD_FIXED[0]	N	A39		53
51	DBC	U35	P	AD_FIXED[1]	P	B39		53
51		U36	N	AD_FIXED[2]	N	A38		53
51		V36	P	AD_FIXED[3]	P	A37		53
51		U37	N	AD_FIXED[4]	N	B37	DBC	53
51		V37	P	AD_FIXED[5]	P	B36	DBC	53
51	DBC	R37	N	AD_FIXED[6]	N	C38		53
51	DBC	T37	P	AD_FIXED[7]	P	C37		53
51		R38	N	AD_FIXED[8]	N	E38		53
51		T38	P	AD_FIXED[9]	P	E37		53
51		U39	N	AD_FIXED[10]	N	D39	DBC	53
51		V39	P	AD_FIXED[11]	P	D38	DBC	53
51		M36	N	AD_FIXED[12]	N	A35		53
51		N36	P	AD_FIXED[13]	P	A34		53
51		P35	N	AD_FIXED[14]	N	B35		53
51		R35	P	AD_FIXED[15]	P	B34		53
51		P36	N	AD_FIXED[16]	N	C36		53
51		R36	P	AD_FIXED[17]	P	D36		53
51		N38	N	AD_FIXED[18]	N	D35		53
51		P38	P	AD_FIXED[19]	P	E35		53
51	GC	M39	N	AD_FIXED[20]	N	C34	GC_QBC	53
51	GC	N39	P	AD_FIXED[21]	P	C33	GC_QBC	53
51	GC_QBC	L39	N	AD_FIXED[22]	N	C32	GC	53
51	GC_QBC	L38	P	AD_FIXED[23]	P	C31	GC	53
51		H39	N	AD_FIXED[24]	N	A33		53
51		J39	P	AD_FIXED[25]	P	A32		53
51		J40	N	AD_FIXED[26]	N	A30		53
51		K40	P	AD_FIXED[27]	P	B30		53
51		J41	N	AD_FIXED[28]	N	B29		53
51		K41	P	AD_FIXED[29]	P	C29		53
51		J43	N	AD_FIXED[30]	N	D30		53
51		K43	P	AD_FIXED[31]	P	D29		53
51	DBC	L35	N	AD_FIXED[32]	N	A29		53
51	DBC	M35	P	AD_FIXED[33]	P	A28		53
51		K37	N	AD_FIXED[34]	N	C28		53
51		L37	P	AD_FIXED[35]	P	D28		53
51		J36	N	AD_FIXED[36]	N	A27	DBC	53
51		K36	P	AD_FIXED[37]	P	B27	DBC	53
51	DBC	G36	N	AD_FIXED[38]	N	C27		53
51	DBC	H36	P	AD_FIXED[39]	P	C26		53
51		G37	N	AD_FIXED[40]	N	A25		53
51		H37	P	AD_FIXED[41]	P	B25		53
51		F38	N	AD_FIXED[42]	N	D26	DBC	53
51		F37	P	AD_FIXED[43]	P	D25	DBC	53
52	DBC	C48	N	AD_FIXED[44]	N	G40		52
52	DBC	D48	P	AD_FIXED[45]	P	G39		52
52		A49	N	AD_FIXED[46]	N	F40		52
52		B49	P	AD_FIXED[47]	P	F39		52
52		B47	N	AD_FIXED[48]	N	E41	DBC	52
52		C47	P	AD_FIXED[49]	P	E40	DBC	52
52	DBC	A48	N	AD_FIXED[50]	N	D41		52
52	DBC	A47	P	AD_FIXED[51]	P	D40		52
52		C46	N	AD_FIXED[52]	N	E42		52
52		D46	P	AD_FIXED[53]	P	F42		52
52		B46	N	AD_FIXED[54]	N	G42	DBC	52
52		B45	P	AD_FIXED[55]	P	G41	DBC	52
52		H44	N	AD_FIXED[56]	N	A40		52
52		H43	P	AD_FIXED[57]	P	B40		52
52		G45	N	AD_FIXED[58]	N	B41		52
52		G44	P	AD_FIXED[59]	P	C41		52
52		F45	N	AD_FIXED[60]	N	A45		52
52		F44	P	AD_FIXED[61]	P	A44		52
52		E43	N	AD_FIXED[62]	N	A43		52
52		F43	P	AD_FIXED[63]	P	A42		52
52	GC	D45	N	AD_FIXED[64]	N	B44	GC_QBC	52
52	GC	E45	P	AD_FIXED[65]	P	C44	GC_QBC	52
52	GC_QBC	B44	N	AD_FIXED[66]	N	D45	GC	52
52	GC_QBC	C44	P	AD_FIXED[67]	P	E45	GC	52
52		A43	N	AD_FIXED[68]	N	E43		52
52		A42	P	AD_FIXED[69]	P	F43		52

XCVU440 -FLGA2892 FPGA A SLR 2			A - D			XCVU440 -FLGA2892 FPGA D SLR 2		
Bank	Info	Pin	Type	PCB-Trace Name	Type	Pin	Info	Bank
52		A45	N	AD_FIXED[70]	N	F45		52
52		A44	P	AD_FIXED[71]	P	F44		52
52		B41	N	AD_FIXED[72]	N	G45		52
52		C41	P	AD_FIXED[73]	P	G44		52
52		A40	N	AD_FIXED[74]	N	H44		52
52		B40	P	AD_FIXED[75]	P	H43		52
52	DBC	G42	N	AD_FIXED[76]	N	B46		52
52	DBC	G41	P	AD_FIXED[77]	P	B45		52
52		E42	N	AD_FIXED[78]	N	C46		52
52		F42	P	AD_FIXED[79]	P	D46		52
52		D41	N	AD_FIXED[80]	N	A48	DBC	52
52		D40	P	AD_FIXED[81]	P	A47	DBC	52
52	DBC	E41	N	AD_FIXED[82]	N	B47		52
52	DBC	E40	P	AD_FIXED[83]	P	C47		52
52		F40	N	AD_FIXED[84]	N	A49		52
52		F39	P	AD_FIXED[85]	P	B49		52
52		G40	N	AD_FIXED[86]	N	C48	DBC	52
52		G39	P	AD_FIXED[87]	P	D48	DBC	52
53	DBC	D26	N	AD_FIXED[88]	N	F38		51
53	DBC	D25	P	AD_FIXED[89]	P	F37		51
53		A25	N	AD_FIXED[90]	N	G37		51
53		B25	P	AD_FIXED[91]	P	H37		51
53		C27	N	AD_FIXED[92]	N	G36	DBC	51
53		C26	P	AD_FIXED[93]	P	H36	DBC	51
53	DBC	A27	N	AD_FIXED[94]	N	J36		51
53	DBC	B27	P	AD_FIXED[95]	P	K36		51
53		C28	N	AD_FIXED[96]	N	K37		51
53		D28	P	AD_FIXED[97]	P	L37		51
53		A29	N	AD_FIXED[98]	N	L35	DBC	51
53		A28	P	AD_FIXED[99]	P	M35	DBC	51
53		D30	N	AD_FIXED[100]	N	J43		51
53		D29	P	AD_FIXED[101]	P	K43		51
53		B29	N	AD_FIXED[102]	N	J41		51
53		C29	P	AD_FIXED[103]	P	K41		51
53		A30	N	AD_FIXED[104]	N	J40		51
53		B30	P	AD_FIXED[105]	P	K40		51
53		A33	N	AD_FIXED[106]	N	H39		51
53		A32	P	AD_FIXED[107]	P	J39		51
53	GC	C32	N	AD_FIXED[108]	N	L39	GC_QBC	51
53	GC	C31	P	AD_FIXED[109]	P	L38	GC_QBC	51
53	GC_QBC	C34	N	AD_FIXED[110]	N	M39	GC	51
53	GC_QBC	C33	P	AD_FIXED[111]	P	N39	GC	51
53		D35	N	AD_FIXED[112]	N	N38		51
53		E35	P	AD_FIXED[113]	P	P38		51
53		C36	N	AD_FIXED[114]	N	P36		51
53		D36	P	AD_FIXED[115]	P	R36		51
53		B35	N	AD_FIXED[116]	N	P35		51
53		B34	P	AD_FIXED[117]	P	R35		51
53		A35	N	AD_FIXED[118]	N	M36		51
53		A34	P	AD_FIXED[119]	P	N36		51
53	DBC	D39	N	AD_FIXED[120]	N	U39		51
53	DBC	D38	P	AD_FIXED[121]	P	V39		51
53		E38	N	AD_FIXED[122]	N	R38		51
53		E37	P	AD_FIXED[123]	P	T38		51
53		C38	N	AD_FIXED[124]	N	R37	DBC	51
53		C37	P	AD_FIXED[125]	P	T37	DBC	51
53	DBC	B37	N	AD_FIXED[126]	N	U37		51
53	DBC	B36	P	AD_FIXED[127]	P	V37		51
53		A38	N	AD_FIXED[128]	N	U36		51
53		A37	P	AD_FIXED[129]	P	V36		51
53		A39	N	AD_FIXED[130]	N	T35	DBC	51
53		B39	P	AD_FIXED[131]	P	U35	DBC	51
51		P39	-	AD_FIXED[132]	-	E33		53
51		K42	-	AD_FIXED[133]	-	D31		53
51		H38	-	AD_FIXED[134]	-	C39		53
52		E46	-	AD_FIXED[135]	-	B42		52
52		B42	-	AD_FIXED[136]	-	E46		52
52		H42	-	AD_FIXED[137]	-	H42		52
53		D31	-	AD_FIXED[138]	-	K42		51
53		E33	-	AD_FIXED[139]	-	P39		51
53		C39	-	AD_FIXED[140]	-	H38		51

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Signal I/O Connections FPGA B / FGPA C

XCVU440 -FLGA2892 FPGA B SLR 2			B - C			XCVU440 -FLGA2892 FPGA C SLR 2		
Bank	Info	Pin	Type	PCB-Trace Name	Type	Pin	Info	Bank
51	DBC	T35	N	BC_FIXED[0]	N	A39		53
51	DBC	U35	P	BC_FIXED[1]	P	B39		53
51		U36	N	BC_FIXED[2]	N	A38		53
51		V36	P	BC_FIXED[3]	P	A37		53
51		U37	N	BC_FIXED[4]	N	B37	DBC	53
51		V37	P	BC_FIXED[5]	P	B36	DBC	53
51	DBC	R37	N	BC_FIXED[6]	N	C38		53
51	DBC	T37	P	BC_FIXED[7]	P	C37		53
51		R38	N	BC_FIXED[8]	N	E38		53
51		T38	P	BC_FIXED[9]	P	E37		53
51		U39	N	BC_FIXED[10]	N	D39	DBC	53
51		V39	P	BC_FIXED[11]	P	D38	DBC	53
51		M36	N	BC_FIXED[12]	N	A35		53
51		N36	P	BC_FIXED[13]	P	A34		53
51		P35	N	BC_FIXED[14]	N	B35		53
51		R35	P	BC_FIXED[15]	P	B34		53
51		P36	N	BC_FIXED[16]	N	C36		53
51		R36	P	BC_FIXED[17]	P	D36		53
51		N38	N	BC_FIXED[18]	N	D35		53
51		P38	P	BC_FIXED[19]	P	E35		53
51	GC	M39	N	BC_FIXED[20]	N	C34	GC_QBC	53
51	GC	N39	P	BC_FIXED[21]	P	C33	GC_QBC	53
51	GC_QBC	L39	N	BC_FIXED[22]	N	C32	GC	53
51	GC_QBC	L38	P	BC_FIXED[23]	P	C31	GC	53
51		H39	N	BC_FIXED[24]	N	A33		53
51		J39	P	BC_FIXED[25]	P	A32		53
51		J40	N	BC_FIXED[26]	N	A30		53
51		K40	P	BC_FIXED[27]	P	B30		53
51		J41	N	BC_FIXED[28]	N	B29		53
51		K41	P	BC_FIXED[29]	P	C29		53
51		J43	N	BC_FIXED[30]	N	D30		53
51		K43	P	BC_FIXED[31]	P	D29		53
51	DBC	L35	N	BC_FIXED[32]	N	A29		53
51	DBC	M35	P	BC_FIXED[33]	P	A28		53
51		K37	N	BC_FIXED[34]	N	C28		53
51		L37	P	BC_FIXED[35]	P	D28		53
51		J36	N	BC_FIXED[36]	N	A27	DBC	53
51		K36	P	BC_FIXED[37]	P	B27	DBC	53
51	DBC	G36	N	BC_FIXED[38]	N	C27		53
51	DBC	H36	P	BC_FIXED[39]	P	C26		53
51		G37	N	BC_FIXED[40]	N	A25		53
51		H37	P	BC_FIXED[41]	P	B25		53
51		F38	N	BC_FIXED[42]	N	D26	DBC	53
51		F37	P	BC_FIXED[43]	P	D25	DBC	53
52	DBC	C48	N	BC_FIXED[44]	N	G40		52
52	DBC	D48	P	BC_FIXED[45]	P	G39		52
52		A49	N	BC_FIXED[46]	N	F40		52
52		B49	P	BC_FIXED[47]	P	F39		52
52		B47	N	BC_FIXED[48]	N	E41	DBC	52
52		C47	P	BC_FIXED[49]	P	E40	DBC	52
52	DBC	A48	N	BC_FIXED[50]	N	D41		52
52	DBC	A47	P	BC_FIXED[51]	P	D40		52
52		C46	N	BC_FIXED[52]	N	E42		52
52		D46	P	BC_FIXED[53]	P	F42		52
52		B46	N	BC_FIXED[54]	N	G42	DBC	52
52		B45	P	BC_FIXED[55]	P	G41	DBC	52
52		H44	N	BC_FIXED[56]	N	A40		52
52		H43	P	BC_FIXED[57]	P	B40		52
52		G45	N	BC_FIXED[58]	N	B41		52
52		G44	P	BC_FIXED[59]	P	C41		52
52		F45	N	BC_FIXED[60]	N	A45		52
52		F44	P	BC_FIXED[61]	P	A44		52
52		E43	N	BC_FIXED[62]	N	A43		52
52		F43	P	BC_FIXED[63]	P	A42		52
52	GC	D45	N	BC_FIXED[64]	N	B44	GC_QBC	52
52	GC	E45	P	BC_FIXED[65]	P	C44	GC_QBC	52
52	GC_QBC	B44	N	BC_FIXED[66]	N	D45	GC	52
52	GC_QBC	C44	P	BC_FIXED[67]	P	E45	GC	52
52		A43	N	BC_FIXED[68]	N	E43		52
52		A42	P	BC_FIXED[69]	P	F43		52

XCVU440 -FLGA2892 FPGA B SLR 2			B - C			XCVU440 -FLGA2892 FPGA C SLR 2		
Bank	Info	Pin	Type	PCB-Trace Name	Type	Pin	Info	Bank
52		A45	N	BC_FIXED[70]	N	F45		52
52		A44	P	BC_FIXED[71]	P	F44		52
52		B41	N	BC_FIXED[72]	N	G45		52
52		C41	P	BC_FIXED[73]	P	G44		52
52		A40	N	BC_FIXED[74]	N	H44		52
52		B40	P	BC_FIXED[75]	P	H43		52
52	DBC	G42	N	BC_FIXED[76]	N	B46		52
52	DBC	G41	P	BC_FIXED[77]	P	B45		52
52		E42	N	BC_FIXED[78]	N	C46		52
52		F42	P	BC_FIXED[79]	P	D46		52
52		D41	N	BC_FIXED[80]	N	A48	DBC	52
52		D40	P	BC_FIXED[81]	P	A47	DBC	52
52	DBC	E41	N	BC_FIXED[82]	N	B47		52
52	DBC	E40	P	BC_FIXED[83]	P	C47		52
52		F40	N	BC_FIXED[84]	N	A49		52
52		F39	P	BC_FIXED[85]	P	B49		52
52		G40	N	BC_FIXED[86]	N	C48	DBC	52
52		G39	P	BC_FIXED[87]	P	D48	DBC	52
53	DBC	D26	N	BC_FIXED[88]	N	F38		51
53	DBC	D25	P	BC_FIXED[89]	P	F37		51
53		A25	N	BC_FIXED[90]	N	G37		51
53		B25	P	BC_FIXED[91]	P	H37		51
53		C27	N	BC_FIXED[92]	N	G36	DBC	51
53		C26	P	BC_FIXED[93]	P	H36	DBC	51
53	DBC	A27	N	BC_FIXED[94]	N	J36		51
53	DBC	B27	P	BC_FIXED[95]	P	K36		51
53		C28	N	BC_FIXED[96]	N	K37		51
53		D28	P	BC_FIXED[97]	P	L37		51
53		A29	N	BC_FIXED[98]	N	L35	DBC	51
53		A28	P	BC_FIXED[99]	P	M35	DBC	51
53		D30	N	BC_FIXED[100]	N	J43		51
53		D29	P	BC_FIXED[101]	P	K43		51
53		B29	N	BC_FIXED[102]	N	J41		51
53		C29	P	BC_FIXED[103]	P	K41		51
53		A30	N	BC_FIXED[104]	N	J40		51
53		B30	P	BC_FIXED[105]	P	K40		51
53		A33	N	BC_FIXED[106]	N	H39		51
53		A32	P	BC_FIXED[107]	P	J39		51
53	GC	C32	N	BC_FIXED[108]	N	L39	GC_QBC	51
53	GC	C31	P	BC_FIXED[109]	P	L38	GC_QBC	51
53	GC_QBC	C34	N	BC_FIXED[110]	N	M39	GC	51
53	GC_QBC	C33	P	BC_FIXED[111]	P	N39	GC	51
53		D35	N	BC_FIXED[112]	N	N38		51
53		E35	P	BC_FIXED[113]	P	P38		51
53		C36	N	BC_FIXED[114]	N	P36		51
53		D36	P	BC_FIXED[115]	P	R36		51
53		B35	N	BC_FIXED[116]	N	P35		51
53		B34	P	BC_FIXED[117]	P	R35		51
53		A35	N	BC_FIXED[118]	N	M36		51
53		A34	P	BC_FIXED[119]	P	N36		51
53	DBC	D39	N	BC_FIXED[120]	N	U39		51
53	DBC	D38	P	BC_FIXED[121]	P	V39		51
53		E38	N	BC_FIXED[122]	N	R38		51
53		E37	P	BC_FIXED[123]	P	T38		51
53		C38	N	BC_FIXED[124]	N	R37	DBC	51
53		C37	P	BC_FIXED[125]	P	T37	DBC	51
53	DBC	B37	N	BC_FIXED[126]	N	U37		51
53	DBC	B36	P	BC_FIXED[127]	P	V37		51
53		A38	N	BC_FIXED[128]	N	U36		51
53		A37	P	BC_FIXED[129]	P	V36		51
53		A39	N	BC_FIXED[130]	N	T35	DBC	51
53		B39	P	BC_FIXED[131]	P	U35	DBC	51
51		P39	-	BC_FIXED[132]	-	E33		53
51		K42	-	BC_FIXED[133]	-	D31		53
51		H38	-	BC_FIXED[134]	-	C39		53
52		E46	-	BC_FIXED[135]	-	B42		52
52		B42	-	BC_FIXED[136]	-	E46		52
52		H42	-	BC_FIXED[137]	-	H42		52
53		D31	-	BC_FIXED[138]	-	K42		51
53		E33	-	BC_FIXED[139]	-	P39		51
53		C39	-	BC_FIXED[140]	-	H38		51

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MGB1 PCB-Trace Names

MGB		XCVU440 - FLGA2892 SLR 1		PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Bank	FPGA A	FPGA B	FPGA C	FPGA D
5	P	AH6	225	AM1_TXP[0]	BM1_TXP[0]	CM1_TXP[0]	DM1_TXP[0]
7	N	AH5	225	AM1_TXN[0]	BM1_TXN[0]	CM1_TXN[0]	DM1_TXN[0]
11	N	AJ7	225	AM1_TXN[1]	BM1_TXN[1]	CM1_TXN[1]	DM1_TXN[1]
13	P	AJ8	225	AM1_TXP[1]	BM1_TXP[1]	CM1_TXP[1]	DM1_TXP[1]
17	P	AH10	225	AM1_REFCLKP[1]	BM1_REFCLKP[1]	CM1_REFCLKP[1]	DM1_REFCLKP[1]
19	N	AH9	225	AM1_REFCLKN[1]	BM1_REFCLKN[1]	CM1_REFCLKN[1]	DM1_REFCLKN[1]
23	P	AK6	225	AM1_TXP[2]	BM1_TXP[2]	CM1_TXP[2]	DM1_TXP[2]
25	N	AK5	225	AM1_TXN[2]	BM1_TXN[2]	CM1_TXN[2]	DM1_TXN[2]
29	N	AL7	225	AM1_TXN[3]	BM1_TXN[3]	CM1_TXN[3]	DM1_TXN[3]
31	P	AL8	225	AM1_TXP[3]	BM1_TXP[3]	CM1_TXP[3]	DM1_TXP[3]
6	P	AH2	225	AM1_RXP[0]	BM1_RXP[0]	CM1_RXP[0]	DM1_RXP[0]
8	N	AH1	225	AM1_RXN[0]	BM1_RXN[0]	CM1_RXN[0]	DM1_RXN[0]
12	N	AJ3	225	AM1_RXN[1]	BM1_RXN[1]	CM1_RXN[1]	DM1_RXN[1]
14	P	AJ4	225	AM1_RXP[1]	BM1_RXP[1]	CM1_RXP[1]	DM1_RXP[1]
18	P	AK10	225	AM1_REFCLKP[0]	BM1_REFCLKP[0]	CM1_REFCLKP[0]	DM1_REFCLKP[0]
20	N	AK9	225	AM1_REFCLKN[0]	BM1_REFCLKN[0]	CM1_REFCLKN[0]	DM1_REFCLKN[0]
24	P	AK2	225	AM1_RXP[2]	BM1_RXP[2]	CM1_RXP[2]	DM1_RXP[2]
26	N	AK1	225	AM1_RXN[2]	BM1_RXN[2]	CM1_RXN[2]	DM1_RXN[2]
30	N	AL3	225	AM1_RXN[3]	BM1_RXN[3]	CM1_RXN[3]	DM1_RXN[3]
32	P	AL4	225	AM1_RXP[3]	BM1_RXP[3]	CM1_RXP[3]	DM1_RXP[3]
47	P	AM6	224	AM1_TXP[4]	BM1_TXP[4]	CM1_TXP[4]	DM1_TXP[4]
49	N	AM5	224	AM1_TXN[4]	BM1_TXN[4]	CM1_TXN[4]	DM1_TXN[4]
53	N	AN7	224	AM1_TXN[5]	BM1_TXN[5]	CM1_TXN[5]	DM1_TXN[5]
55	P	AN8	224	AM1_TXP[5]	BM1_TXP[5]	CM1_TXP[5]	DM1_TXP[5]
59	P	AM10	224	AM1_REFCLKP[3]	BM1_REFCLKP[3]	CM1_REFCLKP[3]	DM1_REFCLKP[3]
61	N	AM9	224	AM1_REFCLKN[3]	BM1_REFCLKN[3]	CM1_REFCLKN[3]	DM1_REFCLKN[3]
65	P	AP6	224	AM1_TXP[6]	BM1_TXP[6]	CM1_TXP[6]	DM1_TXP[6]
67	N	AP5	224	AM1_TXN[6]	BM1_TXN[6]	CM1_TXN[6]	DM1_TXN[6]
71	N	AR7	224	AM1_TXN[7]	BM1_TXN[7]	CM1_TXN[7]	DM1_TXN[7]
73	P	AR8	224	AM1_TXP[7]	BM1_TXP[7]	CM1_TXP[7]	DM1_TXP[7]
48	P	AM2	224	AM1_RXP[4]	BM1_RXP[4]	CM1_RXP[4]	DM1_RXP[4]
50	N	AM1	224	AM1_RXN[4]	BM1_RXN[4]	CM1_RXN[4]	DM1_RXN[4]
54	N	AN3	224	AM1_RXN[5]	BM1_RXN[5]	CM1_RXN[5]	DM1_RXN[5]
56	P	AN4	224	AM1_RXP[5]	BM1_RXP[5]	CM1_RXP[5]	DM1_RXP[5]
60	P	AP10	224	AM1_REFCLKP[2]	BM1_REFCLKP[2]	CM1_REFCLKP[2]	DM1_REFCLKP[2]
62	N	AP9	224	AM1_REFCLKN[2]	BM1_REFCLKN[2]	CM1_REFCLKN[2]	DM1_REFCLKN[2]
66	P	AP2	224	AM1_RXP[6]	BM1_RXP[6]	CM1_RXP[6]	DM1_RXP[6]
68	N	AP1	224	AM1_RXN[6]	BM1_RXN[6]	CM1_RXN[6]	DM1_RXN[6]
72	N	AR3	224	AM1_RXN[7]	BM1_RXN[7]	CM1_RXN[7]	DM1_RXN[7]
74	P	AR4	224	AM1_RXP[7]	BM1_RXP[7]	CM1_RXP[7]	DM1_RXP[7]

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MGB2 PCB-Trace Names

MGB		XCVU440 - FLGA2892 SLR 0		PCB-Trace Names HAPS-80 S104			
Pin	Type	Pin	Bank	FPGA A	FPGA B	FPGA C	FPGA D
5	P	AT6	222	AM2_TXP[0]	BM2_TXP[0]	CM2_TXP[0]	DM2_TXP[0]
7	N	AT5	222	AM2_TXN[0]	BM2_TXN[0]	CM2_TXN[0]	DM2_TXN[0]
11	N	AU7	222	AM2_TXN[1]	BM2_TXN[1]	CM2_TXN[1]	DM2_TXN[1]
13	P	AU8	222	AM2_TXP[1]	BM2_TXP[1]	CM2_TXP[1]	DM2_TXP[1]
17	P	AT10	222	AM2_REFCLKP[1]	BM2_REFCLKP[1]	CM2_REFCLKP[1]	DM2_REFCLKP[1]
19	N	AT9	222	AM2_REFCLKN[1]	BM2_REFCLKN[1]	CM2_REFCLKN[1]	DM2_REFCLKN[1]
23	P	AV6	222	AM2_TXP[2]	BM2_TXP[2]	CM2_TXP[2]	DM2_TXP[2]
25	N	AV5	222	AM2_TXN[2]	BM2_TXN[2]	CM2_TXN[2]	DM2_TXN[2]
29	N	AW7	222	AM2_TXN[3]	BM2_TXN[3]	CM2_TXN[3]	DM2_TXN[3]
31	P	AW8	222	AM2_TXP[3]	BM2_TXP[3]	CM2_TXP[3]	DM2_TXP[3]
6	P	AT2	222	AM2_RXP[0]	BM2_RXP[0]	CM2_RXP[0]	DM2_RXP[0]
8	N	AT1	222	AM2_RXN[0]	BM2_RXN[0]	CM2_RXN[0]	DM2_RXN[0]
12	N	AU3	222	AM2_RXN[1]	BM2_RXN[1]	CM2_RXN[1]	DM2_RXN[1]
14	P	AU4	222	AM2_RXP[1]	BM2_RXP[1]	CM2_RXP[1]	DM2_RXP[1]
18	P	AV10	222	AM2_REFCLKP[0]	BM2_REFCLKP[0]	CM2_REFCLKP[0]	DM2_REFCLKP[0]
20	N	AV9	222	AM2_REFCLKN[0]	BM2_REFCLKN[0]	CM2_REFCLKN[0]	DM2_REFCLKN[0]
24	P	AV2	222	AM2_RXP[2]	BM2_RXP[2]	CM2_RXP[2]	DM2_RXP[2]
26	N	AV1	222	AM2_RXN[2]	BM2_RXN[2]	CM2_RXN[2]	DM2_RXN[2]
30	N	AW3	222	AM2_RXN[3]	BM2_RXN[3]	CM2_RXN[3]	DM2_RXN[3]
32	P	AW4	222	AM2_RXP[3]	BM2_RXP[3]	CM2_RXP[3]	DM2_RXP[3]
47	P	AY6	221	AM2_TXP[4]	BM2_TXP[4]	CM2_TXP[4]	DM2_TXP[4]
49	N	AY5	221	AM2_TXN[4]	BM2_TXN[4]	CM2_TXN[4]	DM2_TXN[4]
53	N	BA7	221	AM2_TXN[5]	BM2_TXN[5]	CM2_TXN[5]	DM2_TXN[5]
55	P	BA8	221	AM2_TXP[5]	BM2_TXP[5]	CM2_TXP[5]	DM2_TXP[5]
59	P	AY10	221	AM2_REFCLKP[3]	BM2_REFCLKP[3]	CM2_REFCLKP[3]	DM2_REFCLKP[3]
61	N	AY9	221	AM2_REFCLKN[3]	BM2_REFCLKN[3]	CM2_REFCLKN[3]	DM2_REFCLKN[3]
65	P	BB6	221	AM2_TXP[6]	BM2_TXP[6]	CM2_TXP[6]	DM2_TXP[6]
67	N	BB5	221	AM2_TXN[6]	BM2_TXN[6]	CM2_TXN[6]	DM2_TXN[6]
71	N	BC7	221	AM2_TXN[7]	BM2_TXN[7]	CM2_TXN[7]	DM2_TXN[7]
73	P	BC8	221	AM2_TXP[7]	BM2_TXP[7]	CM2_TXP[7]	DM2_TXP[7]
48	P	AY2	221	AM2_RXP[4]	BM2_RXP[4]	CM2_RXP[4]	DM2_RXP[4]
50	N	AY1	221	AM2_RXN[4]	BM2_RXN[4]	CM2_RXN[4]	DM2_RXN[4]
54	N	BA3	221	AM2_RXN[5]	BM2_RXN[5]	CM2_RXN[5]	DM2_RXN[5]
56	P	BA4	221	AM2_RXP[5]	BM2_RXP[5]	CM2_RXP[5]	DM2_RXP[5]
60	P	BB10	221	AM2_REFCLKP[2]	BM2_REFCLKP[2]	CM2_REFCLKP[2]	DM2_REFCLKP[2]
62	N	BB9	221	AM2_REFCLKN[2]	BM2_REFCLKN[2]	CM2_REFCLKN[2]	DM2_REFCLKN[2]
66	P	BB2	221	AM2_RXP[6]	BM2_RXP[6]	CM2_RXP[6]	DM2_RXP[6]
68	N	BB1	221	AM2_RXN[6]	BM2_RXN[6]	CM2_RXN[6]	DM2_RXN[6]
72	N	BC3	221	AM2_RXN[7]	BM2_RXN[7]	CM2_RXN[7]	DM2_RXN[7]
74	P	BC4	221	AM2_RXP[7]	BM2_RXP[7]	CM2_RXP[7]	DM2_RXP[7]

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MGB Link PCB-Trace Names

Eight SATA connectors with one UV440 GTH transceiver from two GTH quads. See FPGA Interconnects, on page 24

MGB Link		XCVU440 - FLGA2892 SLR 0		PCB-Trace Names HAPS-80 S104				
Pin	Type	Pin	Bank	FPGA A	FPGA B	FPGA C	FPGA D	
ML1-4	P	BL8	219	AML1234_REFCLKP	BML1234_REFCLKP	CML1234_REFCLKP	DML1234_REFCLKP	150MHz fixed
ML1-4	N	BL7	219	AML1234_REFCLKN	BML1234_REFCLKN	CML1234_REFCLKN	DML1234_REFCLKN	150MHz fixed
ML1	P	BM6	219	AML1_TXP	BML1_TXP	CML1_TXP	DML1_TXP	
ML1	N	BM5	219	AML1_TXN	BML1_TXN	CML1_TXN	DML1_TXN	
ML1	P	BN4	219	AML1_RXP	BML1_RXP	CML1_RXP	DML1_RXP	
ML1	N	BN3	219	AML1_RXN	BML1_RXN	CML1_RXN	DML1_RXN	
ML2	P	BK6	219	AML2_TXP	BML2_TXP	CML2_TXP	DML2_TXP	
ML2	N	BK5	219	AML2_TXN	BML2_TXN	CML2_TXN	DML2_TXN	
ML2	P	BL4	219	AML2_RXP	BML2_RXP	CML2_RXP	DML2_RXP	
ML2	N	BL3	219	AML2_RXN	BML2_RXN	CML2_RXN	DML2_RXN	
ML3	P	BJ4	219	AML3_TXP	BML3_TXP	CML3_TXP	DML3_TXP	
ML3	N	BJ3	219	AML3_TXN	BML3_TXN	CML3_TXN	DML3_TXN	
ML3	P	BK2	219	AML3_RXP	BML3_RXP	CML3_RXP	DML3_RXP	
ML3	N	BK1	219	AML3_RXN	BML3_RXN	CML3_RXN	DML3_RXN	
ML4	P	BH6	219	AML4_TXP	BML4_TXP	CML4_TXP	DML4_TXP	
ML4	N	BH5	219	AML4_TXN	BML4_TXN	CML4_TXN	DML4_TXN	
ML4	P	BH2	219	AML4_RXP	BML4_RXP	CML4_RXP	DML4_RXP	
ML4	N	BH1	219	AML4_RXN	BML4_RXN	CML4_RXN	DML4_RXN	
ML5-8	P	BF10	220	AML5678_REFCLKP	BML5678_REFCLKP	CML5678_REFCLKP	DML5678_REFCLKP	150MHz fixed
ML5-8	N	BF9	220	AML5678_REFCLKN	BML5678_REFCLKN	CML5678_REFCLKN	DML5678_REFCLKN	150MHz fixed
ML5	P	BD6	220	AML5_TXP	BML5_TXP	CML5_TXP	DML5_TXP	
ML5	N	BD5	220	AML5_TXN	BML5_TXN	CML5_TXN	DML5_TXN	
ML5	P	BD2	220	AML5_RXP	BML5_RXP	CML5_RXP	DML5_RXP	
ML5	N	BD1	220	AML5_RXN	BML5_RXN	CML5_RXN	DML5_RXN	
ML6	P	BE8	220	AML6_TXP	BML6_TXP	CML6_TXP	DML6_TXP	
ML6	N	BE7	220	AML6_TXN	BML6_TXN	CML6_TXN	DML6_TXN	
ML6	P	BE4	220	AML6_RXP	BML6_RXP	CML6_RXP	DML6_RXP	
ML6	N	BE3	220	AML6_RXN	BML6_RXN	CML6_RXN	DML6_RXN	
ML7	P	BF6	220	AML7_TXP	BML7_TXP	CML7_TXP	DML7_TXP	
ML7	N	BF5	220	AML7_TXN	BML7_TXN	CML7_TXN	DML7_TXN	
ML7	P	BF2	220	AML7_RXP	BML7_RXP	CML7_RXP	DML7_RXP	
ML7	N	BF1	220	AML7_RXN	BML7_RXN	CML7_RXN	DML7_RXN	
ML8	P	BG8	220	AML8_TXP	BML8_TXP	CML8_TXP	DML8_TXP	
ML8	N	BG7	220	AML8_TXN	BML8_TXN	CML8_TXN	DML8_TXN	
ML8	P	BG4	220	AML8_RXP	BML8_RXP	CML8_RXP	DML8_RXP	
ML8	N	BG3	220	AML8_RXN	BML8_RXN	CML8_RXN	DML8_RXN	

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Clock PCB-Trace Names

Global Clocks (Define IO Names-Syntesis Mode)		XCVU440 FLGA2892				PCB-Trace Names HAPS-80 S104 (Partition Mode)			
Pin	Type	Pin	Info	Bank	SLR	FPGA A	FPGA B	FPGA C	FPGA D
GCLKP[1]	P	AF48	GC	44	1	GCLK1			
GCLKN[1]	N	AF49	GC	44	1	GCLK1N			
GCLKP[2]	P	AA48	GC	45	1	GCLK2			
GCLKN[2]	N	AA49	GC	45	1	GCLK2N			
GCLKP[3]	P	V49	GC	46	1	GCLK3			
GCLKN[3]	N	U49	GC	46	1	GCLK3N			
GCLKP[4]	P	L48	GC	47	1	GCLK4			
GCLKN[4]	N	K48	GC	47	1	GCLK4N			
GCLKP[5]	P	N37	GC	51	2	GCLK5			
GCLKN[5]	N	M37	GC	51	2	GCLK5N			
GCLKP[6]	P	D43	GC	52	2	GCLK6			
GCLKN[6]	N	D44	GC	52	2	GCLK6N			
GCLKP[7]	P	B31	GC	53	2	GCLK7			
GCLKN[7]	N	B32	GC	53	2	GCLK7N			
GCLKP[8]	P	K38	GC	51	2	GCLK8			
GCLKN[8]	N	J38	GC	51	2	GCLK8N			
GCLKP[9]	P	C42	GC	52	2	GCLK9			
GCLKN[9]	N	C43	GC	52	2	GCLK9N			
GCLKP[10]	P	D33	GC	53	2	GCLK10			
GCLKN[10]	N	D34	GC	53	2	GCLK10N			
GCLKP[11]	P	BD28	GC	65	1	GCLK11			
GCLKN[11]	N	BE28	GC	65	1	GCLK11N			
GCLKP[12]	P	BC29	GC	65	1	GCLK12			
GCLKN[12]	N	BD29	GC	65	1	GCLK12N			
CLKSRC1	N	AY26		65	1	CLK_SRC[1]	CLK_SRC[5]	CD[0]	CD[0]
CLKSRC2	P	AW26		65	1	CLK_SRC[2]	CLK_SRC[6]	CD[1]	CD[1]
CLKSRC3	N	AV26	DBC	65	1	CLK_SRC[3]	BC[0]	CD[2]	CD[2]
CLKSRC4	P	AU26	DBC	65	1	CLK_SRC[4]	BD[0]	BC[0]	BD[0]

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Virtual I/O Pin PCB-Trace Names

Virtual Pin	PCB-Trace Names Define I/O Names			
	FPGA A	FPGA B	FPGA C	FPGA D
USER_RESETN	A_USER_RESETN	B_USER_RESETN	C_USER_RESETN	D_USER_RESETN
CLKSTOPN	A_CLKSTOPN	B_CLKSTOPN	C_CLKSTOPN	D_CLKSTOPN
LED_RED[1]	A_LED_RED[1]	B_LED_RED[1]	C_LED_RED[1]	D_LED_RED[1]
LED_RED[2]	A_LED_RED[2]	B_LED_RED[2]	C_LED_RED[2]	D_LED_RED[2]
LED_GRN[1]	A_LED_GRN[1]	B_LED_GRN[1]	C_LED_GRN[1]	D_LED_GRN[1]
LED_GRN[2]	A_LED_GRN[2]	B_LED_GRN[2]	C_LED_GRN[2]	D_LED_GRN[2]
BUTTON[1]	A_BUTTON[1]	B_BUTTON[1]	C_BUTTON[1]	D_BUTTON[1]
BUTTON[2]	A_BUTTON[2]	B_BUTTON[2]	C_BUTTON[2]	D_BUTTON[2]
GPIO[1]	A_GPIO[1]	B_GPIO[1]	C_GPIO[1]	D_GPIO[1]
GPIO[2]	A_GPIO[2]	B_GPIO[2]	C_GPIO[2]	D_GPIO[2]
GPIO[3]	A_GPIO[3]	B_GPIO[3]	C_GPIO[3]	D_GPIO[3]
GPIO[4]	A_GPIO[4]	B_GPIO[4]	C_GPIO[4]	D_GPIO[4]
GPIO[5]	A_GPIO[5]	B_GPIO[5]	C_GPIO[5]	D_GPIO[5]
GPIO[6]	A_GPIO[6]	B_GPIO[6]	C_GPIO[6]	D_GPIO[6]
GPIO[7]	A_GPIO[7]	B_GPIO[7]	C_GPIO[7]	D_GPIO[7]
GPIO[8]	A_GPIO[8]	B_GPIO[8]	C_GPIO[8]	D_GPIO[8]
GPIO[9]	A_GPIO[9]	B_GPIO[9]	C_GPIO[9]	D_GPIO[9]
GPIO[10]	A_GPIO[10]	B_GPIO[10]	C_GPIO[10]	D_GPIO[10]
MGB1 IO[1]	AM1_IO[1]	BM1_IO[1]	CM1_IO[1]	DM1_IO[1]
MGB1 IO[2]	AM1_IO[2]	BM1_IO[2]	CM1_IO[2]	DM1_IO[2]
MGB1 IO[3]	AM1_IO[3]	BM1_IO[3]	CM1_IO[3]	DM1_IO[3]
MGB1 IO[4]	AM1_IO[4]	BM1_IO[4]	CM1_IO[4]	DM1_IO[4]
MGB1 IO[5]	AM1_IO[5]	BM1_IO[5]	CM1_IO[5]	DM1_IO[5]
MGB1 IO[6]	AM1_IO[6]	BM1_IO[6]	CM1_IO[6]	DM1_IO[6]
MGB1 IO[7]	AM1_IO[7]	BM1_IO[7]	CM1_IO[7]	DM1_IO[7]
MGB1 IO[8]	AM1_IO[8]	BM1_IO[8]	CM1_IO[8]	DM1_IO[8]
MGB1 IO[9]	AM1_IO[9]	BM1_IO[9]	CM1_IO[9]	DM1_IO[9]
MGB1 IO[10]	AM1_IO[10]	BM1_IO[10]	CM1_IO[10]	DM1_IO[10]
MGB2 IO[1]	AM2_IO[1]	BM2_IO[1]	CM2_IO[1]	DM2_IO[1]
MGB2 IO[2]	AM2_IO[2]	BM2_IO[2]	CM2_IO[2]	DM2_IO[2]
MGB2 IO[3]	AM2_IO[3]	BM2_IO[3]	CM2_IO[3]	DM2_IO[3]
MGB2 IO[4]	AM2_IO[4]	BM2_IO[4]	CM2_IO[4]	DM2_IO[4]
MGB2 IO[5]	AM2_IO[5]	BM2_IO[5]	CM2_IO[5]	DM2_IO[5]
MGB2 IO[6]	AM2_IO[6]	BM2_IO[6]	CM2_IO[6]	DM2_IO[6]
MGB2 IO[7]	AM2_IO[7]	BM2_IO[7]	CM2_IO[7]	DM2_IO[7]
MGB2 IO[8]	AM2_IO[8]	BM2_IO[8]	CM2_IO[8]	DM2_IO[8]
MGB2 IO[9]	AM2_IO[9]	BM2_IO[9]	CM2_IO[9]	DM2_IO[9]
MGB2 IO[10]	AM2_IO[10]	BM2_IO[10]	CM2_IO[10]	DM2_IO[10]

*Pin assigned to the PCB-trace name for the corresponding used FPGA. For example,

"`define_haps_io {p:local_logic_reset_n} -haps_io {A_USER_RESETN}`"

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System IP/UMRBus PCB-Trace Names

System IP			XCVU440 -FLGA2892 Bank 65 SLR 1		System Bus Functions HAPS-80 S104			
	Pin	Type	Pin	Info	FPGA A	FPGA B	FPGA C	FPGA D
HAPS_SYSTEM_BUS_IN[3]	GPIOLINK_IN	P	BH28		A_GPIOLINK_IN	B_GPIOLINK_IN	C_GPIOLINK_IN	D_GPIOLINK_IN
HAPS_SYSTEM_BUS_OUT[0]	GPIOLINK_OUT	N	BJ28		A_GPIOLINK_OUT	B_GPIOLINK_OUT	C_GPIOLINK_OUT	D_GPIOLINK_OUT
HAPS_SYSTEM_BUS_IN[4]	UMR_IN_DAT[0]	P	AY28		A_UMR_IN_DAT[0]	B_UMR_IN_DAT[0]	C_UMR_IN_DAT[0]	D_UMR_IN_DAT[0]
HAPS_SYSTEM_BUS_IN[5]	UMR_IN_DAT[1]	N	BA28		A_UMR_IN_DAT[1]	B_UMR_IN_DAT[1]	C_UMR_IN_DAT[1]	D_UMR_IN_DAT[1]
HAPS_SYSTEM_BUS_IN[6]	UMR_IN_DAT[2]	P	AY27		A_UMR_IN_DAT[2]	B_UMR_IN_DAT[2]	C_UMR_IN_DAT[2]	D_UMR_IN_DAT[2]
HAPS_SYSTEM_BUS_IN[7]	UMR_IN_DAT[3]	N	BA27		A_UMR_IN_DAT[3]	B_UMR_IN_DAT[3]	C_UMR_IN_DAT[3]	D_UMR_IN_DAT[3]
HAPS_SYSTEM_BUS_IN[8]	UMR_IN_DAT[4]	P	BD30		A_UMR_IN_DAT[4]	B_UMR_IN_DAT[4]	C_UMR_IN_DAT[4]	D_UMR_IN_DAT[4]
HAPS_SYSTEM_BUS_IN[9]	UMR_IN_DAT[5]	N	BE30		A_UMR_IN_DAT[5]	B_UMR_IN_DAT[5]	C_UMR_IN_DAT[5]	D_UMR_IN_DAT[5]
HAPS_SYSTEM_BUS_IN[10]	UMR_IN_DAT[6]	P	BF28		A_UMR_IN_DAT[6]	B_UMR_IN_DAT[6]	C_UMR_IN_DAT[6]	D_UMR_IN_DAT[6]
HAPS_SYSTEM_BUS_IN[11]	UMR_IN_DAT[7]	N	BF29		A_UMR_IN_DAT[7]	B_UMR_IN_DAT[7]	C_UMR_IN_DAT[7]	D_UMR_IN_DAT[7]
HAPS_SYSTEM_BUS_IN[12]	UMR_IN_EN	P	BE27		A_UMR_IN_EN	B_UMR_IN_EN	C_UMR_IN_EN	D_UMR_IN_EN
HAPS_SYSTEM_BUS_IN[13]	UMR_IN_VALID	N	BF27		A_UMR_IN_VALID	B_UMR_IN_VALID	C_UMR_IN_VALID	D_UMR_IN_VALID
HAPS_SYSTEM_BUS_OUT[1]	UMR_OUT_DAT[0]	P	BD26		A_UMR_OUT_DAT[0]	B_UMR_OUT_DAT[0]	C_UMR_OUT_DAT[0]	D_UMR_OUT_DAT[0]
HAPS_SYSTEM_BUS_OUT[2]	UMR_OUT_DAT[1]	N	BE26		A_UMR_OUT_DAT[1]	B_UMR_OUT_DAT[1]	C_UMR_OUT_DAT[1]	D_UMR_OUT_DAT[1]
HAPS_SYSTEM_BUS_OUT[3]	UMR_OUT_DAT[2]	P	BF30		A_UMR_OUT_DAT[2]	B_UMR_OUT_DAT[2]	C_UMR_OUT_DAT[2]	D_UMR_OUT_DAT[2]
HAPS_SYSTEM_BUS_OUT[4]	UMR_OUT_DAT[3]	N	BG30		A_UMR_OUT_DAT[3]	B_UMR_OUT_DAT[3]	C_UMR_OUT_DAT[3]	D_UMR_OUT_DAT[3]
HAPS_SYSTEM_BUS_OUT[5]	UMR_OUT_DAT[4]	P	BG29		A_UMR_OUT_DAT[4]	B_UMR_OUT_DAT[4]	C_UMR_OUT_DAT[4]	D_UMR_OUT_DAT[4]
HAPS_SYSTEM_BUS_OUT[6]	UMR_OUT_DAT[5]	N	BH29		A_UMR_OUT_DAT[5]	B_UMR_OUT_DAT[5]	C_UMR_OUT_DAT[5]	D_UMR_OUT_DAT[5]
HAPS_SYSTEM_BUS_OUT[7]	UMR_OUT_DAT[6]	P	BJ29	DBC	A_UMR_OUT_DAT[6]	B_UMR_OUT_DAT[6]	C_UMR_OUT_DAT[6]	D_UMR_OUT_DAT[6]
HAPS_SYSTEM_BUS_OUT[8]	UMR_OUT_DAT[7]	N	BJ30	DBC	A_UMR_OUT_DAT[7]	B_UMR_OUT_DAT[7]	C_UMR_OUT_DAT[7]	D_UMR_OUT_DAT[7]
HAPS_SYSTEM_BUS_OUT[9]	UMR_OUT_EN	P	BG27		A_UMR_OUT_EN	B_UMR_OUT_EN	C_UMR_OUT_EN	D_UMR_OUT_EN
HAPS_SYSTEM_BUS_OUT[10]	UMR_OUT_VALID	N	BH27		A_UMR_OUT_VALID	B_UMR_OUT_VALID	C_UMR_OUT_VALID	D_UMR_OUT_VALID
HAPS_SYSTEM_BUS_IN[0]	GCLKP[0]	P	BC27	GC	GCLK0			
HAPS_SYSTEM_BUS_IN[1]	GCLKN[0]	N	BC28	GC	GCLK0N			
HAPS_SYSTEM_BUS_IN[2]	RESETN	N	BB30		RESETN			
HAPS_SYSTEM_BUS_OUT[13]	CLKSTOPN	P	BA30		A_CLKSTOPN	B_CLKSTOPN	C_CLKSTOPN	D_CLKSTOPN

*These pins are not for user assignment. They are included here for information only.

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PCB-Trace Delays

HT3 Connectors				PCB-Trace
FPGA A	FPGA B	FPGA C	FPGA D	Delay
A1	B1	C1	D1	0.904 ns
A2	B2	C2	D2	0.904 ns
A3	B3	C3	D3	0.904 ns
A4	B4	C4	D4	0.904 ns
A5	B5	C5	D5	1.211 ns
A6	B6	C6	D6	1.211 ns
A7	B7	C7	D7	1.211 ns
A8	B8	C8	D8	0.905 ns
A9	B9	C9	D9	0.905 ns
A10	B10	C10	D10	0.905 ns
A11	B11	C11	D11	0.905 ns
A12	B12	C12	D12	1.003 ns
A13	B13	C13	D13	1.002 ns
A14	B14	C14	D14	1.002 ns
A15	B15	C15	D15	0.707 ns
A16	B16	C16	D16	0.707 ns
A17	B17	C17	D17	0.707 ns
A18	B18	C18	D18	0.707 ns
A19	B19	C19	D19	0.707 ns
A20	B20	C20	D20	0.905 ns
A21	B21	C21	D21	0.905 ns
A22	B22	C22	D22	0.905 ns
A23	B23	C23	D23	0.905 ns
A24	B24	C24	D24	0.905 ns

Cables	Delay
CON_CABLE_25_HT3	1.3 ns
CON_CABLE_50_HT3	2.4 ns
CON_CABLE_100_HT3	4.6 ns
CON_CABLE_150_HT3	6.8 ns
CON_CABLE_200_HT3	9.0 ns

Fixed Inter-FPGA		Delay
AB_FIXED	[140:0]	3.200 ns
BC_FIXED	[140:0]	3.200 ns

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