

FPGA Synthesis Collection Index

Symbols

- `__ALLOWNESTEDBLOCKCOMMENTSTART__` directive [476 \(CmdRef\)](#)
- `_conv.prj` file [258 \(UG\)](#)
- `_conv.sdc` file [258 \(UG\)](#)
- `_est.srr` file [1414 \(Ref\)](#)
- `_SEARCHFILENAMEONLY_` directive [474 \(CmdRef\)](#)
- `_ta.srm` file [1419 \(Ref\)](#)
- `!` character, find command [235 \(CmdRef\)](#)
- `?` wildcard
 - Timing Analyzer [539 \(CmdRef\)](#)
- `.*` connection (SystemVerilog) [249 \(HDLRef\)](#)
- `.adc` file [465 \(UG\)](#), [1404 \(Ref\)](#)
- `.areasrr` file [1413 \(Ref\)](#)
- `.cdc` file
 - examples [3374 \(AttrRef\)](#)
 - specifying attributes and directives [119 \(UG\)](#)
- `.edf` file [2108 \(Ref\)](#)
- `.est` file [1414 \(Ref\)](#), [666 \(CmdRef\)](#)
- `.fse` file [1414 \(Ref\)](#)
- `.info` file [1414 \(Ref\)](#)
- `.ini` file [1405 \(Ref\)](#)
 - parallel jobs [760 \(UG\)](#)
- `.lpf` file [1890 \(Ref\)](#), [1892 \(Ref\)](#)
- `.name` connection (SystemVerilog) [248 \(HDLRef\)](#)
- `.ndf` file [2108 \(Ref\)](#)
- `.nrf` file [1405 \(Ref\)](#)
- `.opt` file
 - input [1405 \(Ref\)](#)
 - output [1415 \(Ref\)](#)
- `.prj` file [1405 \(Ref\)](#)
- `.sap`
 - annotated properties for analyst [1416 \(Ref\)](#)
- `.sar` file [1417 \(Ref\)](#)
- `.sdc` file [1405 \(Ref\)](#)
- `.sfp` file [1406 \(Ref\)](#)
- `.srd` file [1417 \(Ref\)](#)
- `.srm` file [1417 \(Ref\)](#)
- `.srp` file [1417 \(Ref\)](#)
- `.srr` file [1421 \(Ref\)](#)
 - See log file
 - watching selected information [1276 \(Ref\)](#)
- `.srs` file [1417 \(Ref\)](#)
 - initial values (Verilog) [1539 \(Ref\)](#)
 - See srs file
- `.sv` file [1406 \(Ref\)](#)
 - SystemVerilog source file [1407 \(Ref\)](#)
- `.ta` file
 - See timing report file [1419 \(Ref\)](#)
- `.tcl` file
 - input [1406 \(Ref\)](#)
 - output [1419 \(Ref\)](#)
- `tcl` file
 - See also Tcl files [1419 \(Ref\)](#)
- `.v` file [1407 \(Ref\)](#)
- `.vhd` file [1407 \(Ref\)](#)
- `.vhm` file [1420 \(Ref\)](#), [1762 \(Ref\)](#), [2172 \(Ref\)](#)
- `.vm` file [1420 \(Ref\)](#), [1763 \(Ref\)](#)
- `.xnf` file (Xilinx). See xnf file (Xilinx)
- ``ifdef` [128 \(HDLRef\)](#)
- `$bits` system function [262 \(HDLRef\)](#)

Numerics

- 3rd party vendor tools
 - invoking [777 \(UG\)](#)
- 64-bit mapping [449 \(CmdRef\)](#)

A

aborting a synthesis run [505 \(CmdRef\)](#)
About this program command [603 \(CmdRef\)](#), [59 \(DebugRef\)](#)

Achronix
 attributes [1764 \(Ref\)](#)
 directives [1764 \(Ref\)](#)
 initial values [1717 \(Ref\)](#)
 Speedster22iHD [1753 \(Ref\)](#)
 technologies [1693 \(Ref\)](#)

ACTgen macros [2048 \(Ref\)](#)

activation command [18 \(DebugRef\)](#)

activations
 auto-saving [4299 \(DebugUG\)](#)
 loading [4299 \(DebugUG\)](#)
 saving [4298 \(DebugUG\)](#)

adc constraints [465 \(UG\)](#)

adc file
 creating [465 \(UG\)](#)
 object names [469 \(UG\)](#)

adc file (analysis design constraint) [1404 \(Ref\)](#)

adc file, using [463 \(UG\)](#)

add files
 -include tcl argument [26 \(CmdRef\)](#)

Add Implementation command [424 \(CmdRef\)](#)

Add P&R Implementation command [626 \(CmdRef\)](#)

Add Place & Route Options File
 command [628 \(CmdRef\)](#)

Add Place and Route Job command [626 \(CmdRef\)](#)

Add Source File command [423 \(CmdRef\)](#)

add_file Tcl command [25 \(CmdRef\)](#)

add_folder Tcl command [30 \(CmdRef\)](#)

add_to_collection command [282 \(CmdRef\)](#)

adder
 SYNCore [1640 \(Ref\)](#)

adders
 SYNCore [1641 \(Ref\)](#)
 wide. *See* wide adders/subtractors.

Additional Products command [602 \(CmdRef\)](#), [59 \(DebugRef\)](#)

adjust pin view (Design Planner) [980 \(UG\)](#)

Adjust Pin View command [662 \(CmdRef\)](#)

Advanced Synthesis
 using [576 \(UG\)](#)

advanced_synthesis
 effect on syn_macro and
 syn_user_instance [3741 \(AttrRef\)](#)

advanced_uram_features_on [152 \(CmdRef\)](#)

aggregate expressions [187 \(HDLRef\)](#)

Align Regions command [661 \(CmdRef\)](#)

all keyword, VHDL 2008 [441 \(HDLRef\)](#)

Allow Docking command [1277 \(Ref\)](#)

alsloc [3393 \(AttrRef\)](#)

alspin [3397 \(AttrRef\)](#)
 bus port pin numbers [2044 \(Ref\)](#)

alspreserve [3401 \(AttrRef\)](#)

Alt key
 column editing [51 \(UG\)](#)
 mapping [426 \(UG\)](#)

Alt key, selecting columns in Text Editor
 [1286 \(Ref\)](#)

altera_io_powerup attribute [3405 \(AttrRef\)](#)

altera_logicclock_location attribute [3409 \(AttrRef\)](#)

altera_logicclock_size attribute [3413 \(AttrRef\)](#)

altpll
 component declaration files [1862 \(Ref\)](#)
 constraints [1863 \(Ref\)](#)
 using [1862 \(Ref\)](#)

altshift_tap, set implementation style [515 \(UG\)](#)

ALTSYNCRAM for LPMs [522 \(UG\)](#)

always blocks
 Verilog [89 \(HDLRef\)](#)
 combinational logic [102 \(HDLRef\)](#)
 event control [103 \(HDLRef\)](#)
 flip-flops [107 \(HDLRef\)](#)
 level-sensitive latches [108 \(HDLRef\)](#)
 multiple event control arguments [89 \(HDLRef\)](#)

always_comb (SystemVerilog) [223 \(HDLRef\)](#)

always_ff (SystemVerilog) [227 \(HDLRef\)](#)

always_latch (SystemVerilog) [225 \(HDLRef\)](#)

always-armed triggering [21 \(DebugRef\)](#)

analysis design constraint file (.adc) [465 \(UG\)](#), [1404 \(Ref\)](#)

analysis design constraints
 design scenarios [464 \(UG\)](#)

analysis design constraints (adc) [463 \(UG\)](#)

analysis design constraints (adc), using
 with sdc [465 \(UG\)](#)

Analyst toolbar [1300 \(Ref\)](#)

Analyst view
 traversing hierarchy [337 \(UG\)](#)

analyzing netlists (Physical Analyst) [1059 \(UG\)](#)

annotated properties for analyst
 .sap [1416 \(Ref\)](#)
 .timing annotated properties (.tap) [1419 \(Ref\)](#)
 object properties for filtering [230 \(CmdRef\)](#)

append_to_collection command [284 \(CmdRef\)](#)

archive file (.sar) [1417 \(Ref\)](#)

archive utility
 SEARCHFILENAMEONLY directive [474 \(CmdRef\)](#)
 copy tcl command [111 \(CmdRef\)](#)
 unarchive tcl command [111 \(CmdRef\)](#)
 using [165 \(UG\)](#)

archiving projects [165 \(UG\)](#)

area estimation
 design modules [666 \(CmdRef\)](#)
 Design Planner regions [667 \(CmdRef\)](#)
 warning settings [669 \(CmdRef\)](#)

area estimation file (.est) [1414 \(Ref\)](#)

area estimation, Design Planner [976 \(UG\)](#)

area, optimizing [533 \(UG\)](#)

areasrr file
 hierarchical area report [1437 \(Ref\)](#)

arithmetic operators
 Verilog [14 \(HDLRef\)](#)

Arrange VHDL files command [500 \(CmdRef\)](#)

Arria [1843 \(Ref\)](#)
 device options [1843 \(Ref\)](#)
 file format options [1846 \(Ref\)](#)
 set_option device options [1845 \(Ref\)](#)

 set_option synthesis options [1846 \(Ref\)](#)

arrow keys, selecting objects in
 Hierarchy Browser [1351 \(Ref\)](#)

arrow pointers for push and pop [1350 \(Ref\)](#)

ASICs [1185 \(UG\)](#)
 clocking different from FPGA [1190 \(UG\)](#)
 converting for FPGA prototyping [1188 \(UG\)](#)
 partitioning [1186 \(UG\)](#)

ASICs, converting
 power considerations [1201 \(UG\)](#)
 UPF file [1202 \(UG\)](#)

assign_to_region Tcl command [39 \(CmdRef\)](#)

assignment operators
 VHDL [292 \(HDLRef\)](#)

assignment statement
 combinational logic (Verilog) [104 \(HDLRef\)](#)
 level-sensitive latches (Verilog) [108 \(HDLRef\)](#)
 VHDL [340 \(HDLRef\)](#)

asterisk wildcard
 Find command [355 \(UG\)](#), [414 \(UG\)](#)

asymmetric RAM
 inferring [1492 \(Ref\)](#)
 instantiating as a black box [1519 \(Ref\)](#)

asymmetric RAM examples [1492 \(Ref\)](#)

asynchronous clock report
 description [1435 \(Ref\)](#)
 generation option [531 \(CmdRef\)](#)

asynchronous clocks [76 \(DebugRef\)](#)

asynchronous sets and resets
 Verilog [111 \(HDLRef\)](#)
 VHDL [353 \(HDLRef\)](#)

asynchronous sets/resets
 and gated clock conversion [860 \(UG\)](#)

asynchronous state machines
 Verilog [121 \(HDLRef\)](#)
 VHDL [363 \(HDLRef\)](#)

ATOM mapping, Intel [1777 \(Ref\)](#)

attr_applied.sdc file [699 \(UG\)](#)

attr_unapplied.sdc file [699 \(UG\)](#)

attributes
 adding [115 \(UG\)](#)

adding in constraint files [244 \(UG\)](#)
 adding in SCOPE [121 \(UG\)](#)
 adding in Verilog [117 \(UG\)](#)
 adding in VHDL [116 \(UG\)](#)
 collections [217 \(UG\)](#)
 custom [3632 \(AttrRef\)](#)
 effects of retiming [545 \(UG\)](#)
 for FSMs [503 \(UG\)](#), [567 \(UG\)](#)
 global attribute summary [3384 \(AttrRef\)](#)
 handling properties [125 \(UG\)](#)
 inferring RAM [1453 \(Ref\)](#)
 Intel [1882 \(Ref\)](#)
 pipelining [539 \(UG\)](#)
 specifying in the SCOPE spreadsheet
 [3372 \(AttrRef\)](#)
 specifying in the source code [133 \(HDLRef\)](#)
 specifying, overview of methods [3372 \(AttrRef\)](#)
 syn_assign_to_region [3493 \(AttrRef\)](#)
 syn_clock_priority [3531 \(AttrRef\)](#)
 syn_direct_reset [3557 \(AttrRef\)](#)
 syn_hier (on compile points) [617 \(UG\)](#)
 syn_highrel_ioconnector [3691 \(AttrRef\)](#)
 syntax, Verilog [133 \(HDLRef\)](#)
 syntax, VHDL [401 \(HDLRef\)](#)
 VHDL package [116 \(UG\)](#)
 attributes (Achronix) [1764 \(Ref\)](#)
 attributes (Microsemi) [2050 \(Ref\)](#)
 attributes (Xilinx) [2173 \(Ref\)](#)
 Attributes demo [1290 \(Ref\)](#)
 attributes in .cdc file [119 \(UG\)](#)
 Attributes panel
 using SCOPE [189 \(UG\)](#)
 Attributes panel, SCOPE [313 \(CmdRef\)](#)
 Attributes panel, SCOPE spreadsheet
 [3372 \(AttrRef\)](#)
 auto constraints [1401 \(Ref\)](#)
 Maximize option [1316 \(Ref\)](#)
 Maximize option (Constraints tab) [452 \(CmdRef\)](#)
 auto constraints, using [470 \(UG\)](#)
 Auto route cross probe insts command
 [1052 \(UG\)](#)
 AutoConstraint_design_name.sdc [473 \(UG\)](#)
 automatic compile points
 compared to manual [586 \(UG\)](#)

flow [605 \(UG\)](#)
 using with manual [620 \(UG\)](#)
 automatic task declaration [62 \(HDLRef\)](#)

B

B.E.S.T [430 \(UG\)](#)
 Back command [417 \(CmdRef\)](#)
 backannotation
 Intel [1127 \(UG\)](#)
 backslash
 escaping dot wildcard in Find
 command [355 \(UG\)](#), [414 \(UG\)](#)
 in Find command (Physical Analyst)
 [1045 \(UG\)](#)
 base synthesis
 using [577 \(UG\)](#)
 batch mode [6 \(UG\)](#), [752 \(UG\)](#), [210 \(CmdRef\)](#)
 using find and expand [212 \(UG\)](#)
 Behavior Extracting Synthesis
 Technology. *See* B.E.S.T
 bit slicing [1013 \(UG\)](#)
 legal primitives [1014 \(UG\)](#)
 bit-stream casting [161 \(HDLRef\)](#)
 bit-string literals [416 \(HDLRef\)](#)
 black [280 \(UG\)](#)
 black box constraints
 VHDL [400 \(HDLRef\)](#)
 black box directives
 black_box_pad_pin [3417 \(AttrRef\)](#)
 black_box_tri_pins [3423 \(AttrRef\)](#)
 syn_black_box [3511 \(AttrRef\)](#)
 syn_force_seq_prim [3649 \(AttrRef\)](#)
 syn_isclock [3717 \(AttrRef\)](#)
 syn_resources [3926 \(AttrRef\)](#)
 syn_tco [4013 \(AttrRef\)](#)
 syn_tpd [4019 \(AttrRef\)](#)
 syn_tristate [4025 \(AttrRef\)](#)
 syn_tsu [4037 \(AttrRef\)](#)
 black box instantiation
 true dual-port asymmetric RAM [1519 \(Ref\)](#)
 black boxes [492 \(UG\)](#), [8 \(DebugRef\)](#)
 See also macros, macro libraries
 adding constraints [496 \(UG\)](#)
 adding constraints in SCOPE [499 \(UG\)](#)
 adding constraints in Verilog [498 \(UG\)](#)

adding constraints in VHDL [497 \(UG\)](#)
continue on error [301 \(UG\)](#)
directives. *See* [black box directives](#)
EDIF naming consistency [500 \(UG\)](#)
for IP cores [2108 \(Ref\)](#)
for predefined macros (Intel) [1776 \(Ref\)](#)
gated clock attributes [850 \(UG\)](#)
in synthesized netlist [280 \(UG\)](#)
instantiating in Verilog [492 \(UG\)](#)
instantiating in VHDL [494 \(UG\)](#)
instantiating, Verilog [124 \(HDLRef\)](#)
instantiating, VHDL [399 \(HDLRef\)](#)
internal startup box (Xilinx) [4141 \(AttrRef\)](#)
Lattice [1905 \(Ref\)](#), [1925 \(Ref\)](#)
Microsemi [1985 \(Ref\)](#)
passing VHDL boolean generics [62 \(UG\)](#)
passing VHDL integer generics [63 \(UG\)](#)
pin attributes [500 \(UG\)](#)
prepared component method (Intel) [527 \(UG\)](#)
setting in hierarchical projects [157 \(UG\)](#)
source code directives [3512 \(AttrRef\)](#)
specifying timing information for Xilinx cores [2108 \(Ref\)](#)
`syn_gatedclk_clock_en` directive [3663 \(AttrRef\)](#)
timing directives [4019 \(AttrRef\)](#)
Verilog [124 \(HDLRef\)](#)
VHDL [399 \(HDLRef\)](#)
Xilinx [2091 \(Ref\)](#)
Xilinx macros [2088 \(Ref\)](#)

`black_box` compile point [592 \(UG\)](#)
`black_box_pad_pin` directive [3417 \(AttrRef\)](#)
`black_box_tri_pins` directive [3423 \(AttrRef\)](#)

Block Inputs Map
Physical Analyst [1073 \(UG\)](#)

block name on end (SystemVerilog) [219 \(HDLRef\)](#)

block RAM
dual-port RAM examples [1468 \(Ref\)](#)
inferring [1455 \(Ref\)](#)
mapping ROM (Xilinx) [2079 \(Ref\)](#)
modes [1451 \(Ref\)](#)
`NO_CHANGE` mode example [1464 \(Ref\)](#)
RAM with control signals examples [1481 \(Ref\)](#)
`READ_FIRST` mode example [1463 \(Ref\)](#)
single-port RAM examples [1465 \(Ref\)](#)
types [1451 \(Ref\)](#)

`WRITE_FIRST` mode example [1461 \(Ref\)](#)

block RAMs
inferring byte enables examples [1525 \(Ref\)](#)
Lattice [1894 \(Ref\)](#)
parity bus, Xilinx [2078 \(Ref\)](#)
`syn_ramstyle` attribute [2052 \(Ref\)](#)
Xilinx single port and dual-port [2078 \(Ref\)](#)

Block Utilization Map
Physical Analyst [1072 \(UG\)](#)

block-based subprojects
compared to instance-based [127 \(UG\)](#)

block-first hierarchical development flow
[24 \(UG\)](#)

blocking-style license queuing [755 \(UG\)](#)

Blocks
initial Block [22 \(HDLRef\)](#)

blocks
defining for hierarchical projects [127 \(UG\)](#)
JTAG communication [4269 \(DebugUG\)](#)
packing I/O (Xilinx) [2089 \(Ref\)](#)
sampling [24 \(DebugRef\)](#)

board file
generation [37 \(DebugRef\)](#)

board query [37 \(DebugRef\)](#)

bookmarks
in source files [51 \(UG\)](#)
using in log files [270 \(UG\)](#)

bottom-up design flow
compile point advantages [584 \(UG\)](#)

bottom-up hierarchical synthesis flow [27 \(UG\)](#)

bottom-up synthesis [769 \(UG\)](#)

boundary scan [34 \(DebugRef\)](#)

boundary-scan registers [4272 \(DebugUG\)](#)

BRAM
debug memory [4318 \(DebugUG\)](#)
IICE buffer type [4244 \(DebugUG\)](#)

breaking up large primitives (Synplify Premier) [1013 \(UG\)](#)

breakpoint icon
color coding [4227 \(DebugUG\)](#)

breakpoints
activating [4287 \(DebugUG\)](#)

activating/deactivating [80 \(DebugRef\)](#)
 combined with watchpoints [23 \(DebugRef\)](#)
 in folded hierarchy [4226 \(DebugUG\)](#)
 instance selection [4227 \(DebugUG\)](#)
 listing available [10 \(DebugRef\)](#)
 listing instrumented [10 \(DebugRef\)](#)
 multiple [22 \(DebugRef\)](#)
 searching [41 \(DebugRef\)](#)
 selecting [4226 \(DebugUG\)](#)
 breakpoints command [19 \(DebugRef\)](#)
 browsers [401 \(UG\)](#)
 buffer
 sample depth [50 \(DebugRef\)](#)
 buffer types
 IICE [4244 \(DebugUG\)](#)
 buffering
 controlling [557 \(UG\)](#)
 buffering, Intel [1840 \(Ref\)](#)
 buffers
 clock. *See* clock buffers
 global. [4137 \(AttrRef\)](#)
 global. *See* global buffers
 instrumenting restrictions [4217 \(DebugUG\)](#)
 output [4131 \(AttrRef\)](#)
 BUFG
 clock priority (Legacy) [251 \(UG\)](#)
 for fanouts [558 \(UG\)](#)
 BUFGCTRL
 false paths (Legacy) [252 \(UG\)](#)
 BUFGDLL [2130 \(Ref\)](#)
 BUFGMUX
 clock priority (Legacy) [251 \(UG\)](#)
 BUFGMUX_1 inference [2128 \(Ref\)](#)
 BUFGMUX_CTRL
 false paths (Legacy) [252 \(UG\)](#)
 BUFGMUX/BUFGMUX_1 inference [2090 \(Ref\)](#), [2128 \(Ref\)](#)
 BUFR clock buffers [2129 \(Ref\)](#)
 Build Project command [396 \(CmdRef\)](#)
 built-in gate primitives (Verilog) [17 \(HDLRef\)](#)
 bus bundling [591 \(CmdRef\)](#)
 bus constraints
 multicycle (Intel) [1876 \(Ref\)](#)
 bus_dimension_separator_style
 command [390 \(CmdRef\)](#)
 bus_naming_style command [390 \(CmdRef\)](#)
 buses
 compressed display [591 \(CmdRef\)](#)
 enabling bit range display [590 \(CmdRef\)](#)
 hiding in flattened Technology views [591 \(CmdRef\)](#)
 INIT values for bits [2118 \(Ref\)](#)
 instrumenting partial [4218 \(DebugUG\)](#)
 RLOC values for bits [2136 \(Ref\)](#)
 buttons and options, Project view [1314 \(Ref\)](#)
 By any transition command [418 \(CmdRef\)](#)
 By input transitions command [418 \(CmdRef\)](#)
 By output transitions command [418 \(CmdRef\)](#)
 Byteblaster cable settings [41 \(DebugRef\)](#)
 byte-enable RAM
 inferring [1525 \(Ref\)](#)
 byte-enable RAM examples [1525 \(Ref\)](#)
 byte-enable RAMs
 SYNCore [1610 \(Ref\)](#)
 byte-wide write enable RAM
 Intel [1782 \(Ref\)](#)

C

c_diff command (collections) [305 \(CmdRef\)](#)
 c_diff command, examples [219 \(UG\)](#)
 c_intersect command (collections) [305 \(CmdRef\)](#)
 c_intersect command, examples [220 \(UG\)](#)
 c_list command
 different from c_print [221 \(UG\)](#)
 example [223 \(UG\)](#)
 using [223 \(UG\)](#)
 c_print command
 different from c_list [221 \(UG\)](#)
 using [223 \(UG\)](#)
 c_print command (collections) [305 \(CmdRef\)](#)
 c_sub command (collections) [305 \(CmdRef\)](#)
 c_syndiff command (collections) [305 \(CmdRef\)](#)

c_symdiff command, examples [220 \(UG\)](#), [245 \(CmdRef\)](#)

c_union command (collections) [305 \(CmdRef\)](#)

c_union command, examples [219 \(UG\)](#)

cable compatibility [40 \(DebugRef\)](#)

cable option settings [26 \(DebugRef\)](#)

cable type [4256 \(DebugUG\)](#)

cable type settings

- Byteblaster [41 \(DebugRef\)](#)
- JTAGTech3710 [44 \(DebugRef\)](#)
- Microsemi [45 \(DebugRef\)](#)
- Xilinx parallel [41 \(DebugRef\)](#)
- Xilinx USB [42 \(DebugRef\)](#)
- Xilinxauto [43 \(DebugRef\)](#)

cable types [25 \(DebugRef\)](#)

cables

- connection [4264 \(DebugUG\)](#)

callback functions, customizing flow [772 \(UG\)](#), [774 \(UG\)](#)

camera mouse pointer [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)

carry chains

- inferring [1931 \(Ref\)](#)

case sensitivity

- Find command (Tcl) [206 \(UG\)](#)

case sensitivity, Tcl find command [224 \(CmdRef\)](#)

case statement

- default [3437 \(AttrRef\)](#)
- VHDL [315 \(HDLRef\)](#)

casting

- static [161 \(HDLRef\)](#)

casting types [161 \(HDLRef\)](#)

cck.rpt file (constraint checking report) [1413 \(Ref\)](#)

cd command [21 \(DebugRef\)](#)

cdc

- syn_black_box example [42 \(UG\)](#)
- syn_keep example [43 \(UG\)](#)

cdc file syntax [119 \(UG\)](#)

CDPL [786 \(UG\)](#), [154 \(CmdRef\)](#)

- setting [787 \(UG\)](#)

cell interior display, enabling/disabling [591 \(CmdRef\)](#)

cells

- enhancing display in Physical Analyst [1030 \(UG\)](#)

chain command [22 \(DebugRef\)](#)

Change File command [423 \(CmdRef\)](#)

Change Implementation Name command [615 \(CmdRef\)](#)

check boxes, Project view [1314 \(Ref\)](#)

check_fdc_query command [40 \(CmdRef\)](#)

check_fdc_query Tcl command [40 \(CmdRef\)](#)

chip regions (Design Planner) [995 \(UG\)](#)

clear command [25 \(DebugRef\)](#)

Clear Parameters command [607 \(CmdRef\)](#)

Clearbox

- features [1860 \(Ref\)](#)
- implementing megafunctions with [666 \(UG\)](#)
- inferring megafunctions [667 \(UG\)](#)
- instantiating megafunctions [671 \(UG\)](#)
- primitives [1861 \(Ref\)](#)
- set_option parameters [180 \(CmdRef\)](#)
- setting options [180 \(CmdRef\)](#)
- using [666 \(UG\)](#)

client-server configuration [4259 \(DebugUG\)](#)

cliquing [1848 \(Ref\)](#)

clock

- sampling [46 \(DebugRef\)](#)

clock alias [535 \(CmdRef\)](#)

clock and path constraints

- setting [190 \(UG\)](#)

clock as object [535 \(CmdRef\)](#)

clock buffering report, log file (.srr) [1424 \(Ref\)](#)

clock buffers [2130 \(Ref\)](#)

- assigning resources [3791 \(AttrRef\)](#)

clock constraints

- setting [190 \(UG\)](#)
- setting (Legacy) [231 \(UG\)](#)

clock conversion report

- accessing [817 \(UG\)](#)
- analyzing [818 \(UG\)](#)

clock DLLs [2130 \(Ref\)](#)

clock edges (VHDL) [344 \(HDLRef\)](#)

- clock enables
 - inferring registers (Intel) [1778 \(Ref\)](#)
 - inferring registers (Xilinx) [2080 \(Ref\)](#)
 - inferring with syn_direct_enable [3552 \(AttrRef\)](#)
 - net assignment [3551 \(AttrRef\)](#)
- clock frequency goals, tradeoffs using different [767 \(UG\)](#)
- clock groups
 - Clock Relationships (timing report) [1433 \(Ref\)](#)
 - effect on false path constraints [204 \(UG\)](#)
- clock groups, SCOPE [297 \(CmdRef\)](#)
- clock option [46 \(DebugRef\)](#)
- clock paths, ignoring [328 \(CmdRef\)](#)
- clock pin drivers, selecting all [1324 \(Ref\)](#)
- clock pins (Design Planner) [986 \(UG\)](#)
- clock priority
 - syn_clock_priority [3531 \(AttrRef\)](#)
- clock relationships, timing report [1433 \(Ref\)](#)
- clock report
 - asynchronous [1427 \(Ref\)](#)
- clock skew example (Synplify Premier) [2132 \(Ref\)](#), [2133 \(Ref\)](#)
- clock skew, Xilinx [2143 \(Ref\)](#)
- Clock Tree, HDL Analyst tool [1324 \(Ref\)](#)
- clock trees [455 \(UG\)](#)
- clocks
 - asynchronous [76 \(DebugRef\)](#)
 - asynchronous report [1435 \(Ref\)](#)
 - converting ASIC to FPGA [1190 \(UG\)](#)
 - declared clock [1429 \(Ref\)](#)
 - defining [1324 \(Ref\)](#)
 - derived clock [1430 \(Ref\)](#)
 - edge selection [22 \(DebugRef\)](#)
 - edges in VHDL [344 \(HDLRef\)](#)
 - implicit false path [204 \(UG\)](#)
 - inferred clock [1429 \(Ref\)](#)
 - on black boxes [3717 \(AttrRef\)](#)
 - sample [21 \(DebugRef\)](#)
 - system clock [1430 \(Ref\)](#)
- Clocks panel
 - using SCOPE [188 \(UG\)](#)
- Clocks panel, SCOPE [296 \(CmdRef\)](#)
- Close command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)
- Close Project command [397 \(CmdRef\)](#)
- code
 - ignoring with pragma translate off/on [3457 \(AttrRef\)](#)
- CoE. *See* continue on error [298 \(UG\)](#)
- Collapse All command [641 \(CmdRef\)](#)
- Collection Commands
 - get_prop [247 \(CmdRef\)](#)
- collection commands
 - c_diff [241 \(CmdRef\)](#)
 - c_intersect [242 \(CmdRef\)](#)
 - c_list [243 \(CmdRef\)](#)
 - c_print [243 \(CmdRef\)](#)
 - c_symdiff [245 \(CmdRef\)](#)
 - c_union [245 \(CmdRef\)](#)
 - SCOPE [305 \(CmdRef\)](#)
- collections
 - adding attributes to [217 \(UG\)](#)
 - adding objects [218 \(UG\)](#)
 - concatenating [218 \(UG\)](#)
 - constraints [216 \(UG\)](#)
 - copying [222 \(UG\)](#)
 - creating from common objects [218 \(UG\)](#)
 - creating from other collections [216 \(UG\)](#)
 - creating in SCOPE [215 \(UG\)](#)
 - creating in Tcl [217 \(UG\)](#)
 - crossprobing objects [216 \(UG\)](#)
 - definition [214 \(UG\)](#)
 - diffing [218 \(UG\)](#)
 - highlighting in HDL Analyst views [221 \(UG\)](#)
 - listing objects [223 \(UG\)](#)
 - listing objects and properties [221 \(UG\)](#)
 - listing objects in a file [222 \(UG\)](#)
 - listing objects in columnar format [221 \(UG\)](#)
 - listing objects with c_list [221 \(UG\)](#)
 - special characters [220 \(UG\)](#)
 - Synopsys standard commands [282 \(CmdRef\)](#)
 - Tcl window and SCOPE comparison [214 \(UG\)](#)
 - using Tcl expand command [210 \(UG\)](#)
 - using Tcl find command [209 \(UG\)](#)
 - viewing [221 \(UG\)](#)
- Collections panel
 - using SCOPE [188 \(UG\)](#)
- Collections panel, SCOPE [304 \(CmdRef\)](#)
- color coding

Text Editor [1286 \(Ref\)](#)
column editing [51 \(UG\)](#)
com command [25 \(DebugRef\)](#)
combination hierarchical synthesis flow
 [31 \(UG\)](#)
combinational logic
 always_comb block (SystemVerilog) [223 \(HDLRef\)](#)
 Verilog [101 \(HDLRef\)](#)
 VHDL [325 \(HDLRef\)](#)
combinational loop errors in state
 machines [364 \(HDLRef\)](#)
combined data, port types (Verilog) [40 \(HDLRef\)](#)
commands
 Add Place & Route Job [626 \(CmdRef\)](#)
 Auto route cross probe insts (Physical Analyst) [1052 \(UG\)](#)
 Go to Location (Physical Analyst) [1047 \(UG\)](#)
 Hierarchy Browser [641 \(CmdRef\)](#)
 Highlight Visible Net Instances (Physical Analyst) [1063 \(UG\)](#)
 Markers [1048 \(UG\)](#)
 menu
 See individual command entries
 netlist editing [1148 \(UG\)](#)
 Select Net Instances [1063 \(UG\)](#)
 Send Crossprobes when selecting (Physical Analyst) [1052 \(UG\)](#)
 set_modules (Tcl) [247 \(CmdRef\)](#)
 Signal Flow [1035 \(UG\)](#)
 slice_primitive [1014 \(UG\)](#)
 Tcl
 See Tcl commands
 Tcl collection [240 \(CmdRef\)](#)
 Tcl command equivalents [16 \(CmdRef\)](#)
 Tcl expand [237 \(CmdRef\)](#)
 Tcl find [221 \(CmdRef\)](#)
 Tcl hooks [774 \(UG\)](#)
comma-separated sensitivity list (Verilog) [41 \(HDLRef\)](#)
Comment Code command [403 \(CmdRef\)](#)
commenting out code (Text Editor) [1286 \(Ref\)](#)
comments
 source files [51 \(UG\)](#)
 Verilog [95 \(HDLRef\)](#)
 VHDL [341 \(HDLRef\)](#)
Common Distributed Processing Library
 [786 \(UG\)](#), [154 \(CmdRef\)](#)
communication cable
 settings [39 \(DebugRef\)](#)
communications settings [4256 \(DebugUG\)](#)
companion parts, Stratix, HardCopy
 [1838 \(Ref\)](#)
compilation process [299 \(UG\)](#)
Compile Only command [498 \(CmdRef\)](#)
Compile Physical Hierarchy command
 [499 \(CmdRef\)](#)
compile point constraints
 editing [643 \(CmdRef\)](#)
 forward-annotating (Cyclone, Arria)
 [1877 \(Ref\)](#)
compile point types
 black_box [592 \(UG\)](#)
 hard [589 \(UG\)](#)
 locked [590 \(UG\)](#)
 locked,partition [592 \(UG\)](#)
compile points
 advantages [584 \(UG\)](#)
 allowed resources [3467 \(AttrRef\)](#)
 analyzing results [618 \(UG\)](#)
 automatic compile point flow [605 \(UG\)](#)
 automatic timing budgeting [597 \(UG\)](#)
 child [587 \(UG\)](#)
 constraint files [594 \(UG\)](#)
 constraints for forward-annotation [604 \(UG\)](#)
 constraints, internal [604 \(UG\)](#)
 continue on error [304 \(UG\)](#)
 creating constraint file [616 \(UG\)](#)
 defined [584 \(UG\)](#)
 defining in constraint files [613 \(UG\)](#)
 described [586 \(UG\)](#)
 fast synthesis [621 \(UG\)](#)
 feature summary [593 \(UG\)](#)
 Identify flow [1145 \(UG\)](#)
 incremental synthesis [623 \(UG\)](#)
 Intel [1841 \(Ref\)](#)
 Intel incremental flows [1087 \(UG\)](#)
 Lattice [1934 \(Ref\)](#)
 manual compile point flow [609 \(UG\)](#)
 Microsemi [2046 \(Ref\)](#)
 multiprocessing [622 \(UG\)](#)
 nested [587 \(UG\)](#)
 optimization [601 \(UG\)](#), [602 \(UG\)](#)
 order of synthesis [601 \(UG\)](#)

- parent [587 \(UG\)](#)
- preserving hierarchy for Xilinx Place and Route [4182 \(AttrRef\)](#)
- preserving with syn_hier [617 \(UG\)](#)
- Quartus II Incremental Compilation [1090 \(UG\)](#)
- resynthesis [603 \(UG\)](#)
- setting constraints [616 \(UG\)](#)
- setting type [614 \(UG\)](#)
- syn_hier [617 \(UG\)](#)
- synthesis process [600 \(UG\)](#)
- synthesizing [604 \(UG\)](#)
- types [588 \(UG\)](#)
- update compile point timing data [1750 \(Ref\)](#)
- updating data (Microsemi) [2031 \(Ref\)](#)
- using automatic and manual compile points together [620 \(UG\)](#)
- using syn_allowed_resources attribute [618 \(UG\)](#)
- Xilinx [2142 \(Ref\)](#)
- Xilinx flow [2170 \(Ref\)](#)
- Xilinx incremental flows [1116 \(UG\)](#)
- compile points and hierarchical project management [22 \(UG\)](#)
- Compile Points panel [189 \(UG\)](#)
- Compile Points panel, SCOPE [316 \(CmdRef\)](#)
- compile_strategy [150 \(CmdRef\)](#), [154 \(CmdRef\)](#)
- compile-point flow
 - Xilinx [1120 \(UG\)](#)
- compile-point synthesis
 - interface logic models [596 \(UG\)](#)
- compile-point synthesis flow
 - defining compile points [613 \(UG\)](#)
 - setting constraints [616 \(UG\)](#)
- compiler
 - loop iteration, loop_limit [3441 \(AttrRef\)](#)
 - loop iteration, syn_looplmit [3735 \(AttrRef\)](#)
- compiler directives [38 \(UG\)](#)
 - using New Constraint File [40 \(UG\)](#)
 - __ALLOWNESTEDBLOCKCOMMENTS_TART__ [476 \(CmdRef\)](#)
 - __SYN_COMPATIBLE_INCLUDEPATH__ [477 \(CmdRef\)](#)
 - __BETA_FEATURES_ON__ [473 \(CmdRef\)](#)
 - __SEARCHFILENAMEONLY__ [474 \(CmdRef\)](#)
 - IGNORE_VERILOG_BLACKBOX_GUTS [472 \(CmdRef\)](#)
 - UI option [464 \(CmdRef\)](#)
 - Verilog [470 \(CmdRef\)](#)
- compiler directives (Verilog)
 - specifying [111 \(UG\)](#)
- compiler directives syntax [41 \(UG\)](#)
- compiler errors
 - continue on error [298 \(UG\)](#)
- compiler report, log file (.srr) [1422 \(Ref\)](#)
- compilers [7 \(UG\)](#)
 - TTFP. *See* TTFP compiler
- complex counter [4240 \(DebugUG\)](#)
 - cycles mode [51 \(DebugRef\)](#)
 - disabling [4308 \(DebugUG\)](#)
 - events mode [51 \(DebugRef\)](#)
 - modes [4307 \(DebugUG\)](#)
 - pulsewidth mode [52 \(DebugRef\)](#)
 - size [4241 \(DebugUG\)](#)
 - watchdog mode [52 \(DebugRef\)](#)
- complex triggering [47 \(DebugRef\)](#), [23 \(DebugRef\)](#)
- components, VHDL. *See* VHDL components
- concurrent signal assignments (VHDL) [321 \(HDLRef\)](#)
- condition operator
 - VHDL 2008 [414 \(HDLRef\)](#)
- conditional signal assignments (VHDL) [323 \(HDLRef\)](#)
- configuration
 - IICE [45 \(DebugRef\)](#)
- configuration statement
 - VHDL [379 \(HDLRef\)](#)
 - VHDL generic mapping [379 \(HDLRef\)](#)
 - VHDL multiple entities [381 \(HDLRef\)](#)
 - VHDL port mapping [380 \(HDLRef\)](#)
- configuration, VHDL
 - declaration [372 \(HDLRef\)](#)
 - specification [369 \(HDLRef\)](#)
- Configure External Programs command [597 \(CmdRef\)](#)
- Configure IICE dialog box [4312 \(DebugUG\)](#)
 - IICE Controller tab [22 \(DebugRef\)](#), [28 \(DebugRef\)](#)

IICE Sampler tab [19 \(DebugRef\)](#)

Configure Mapper Parallel Job command [568 \(CmdRef\)](#)

Configure Verilog Compiler command [568 \(CmdRef\)](#)

Configure VHDL Compiler command [568 \(CmdRef\)](#)

Configure Watch command [607 \(CmdRef\)](#)

congestion

- using estimation report [308 \(UG\)](#)

congestion analysis after logic synthesis using [308 \(UG\)](#)

congestion analysis report [308 \(UG\)](#)

congestion map

- controls [1069 \(UG\)](#)

connectivity, enabling bit range display [590 \(CmdRef\)](#)

console window [24 \(DebugRef\)](#)

- operations [25 \(DebugRef\)](#)

console window operations [4233 \(DebugUG\)](#)

constant function

- syntax restrictions [86 \(HDLRef\)](#)

constant function (Verilog 2001) [43 \(HDLRef\)](#)

constant math function [58 \(HDLRef\)](#)

constants

- extracting from VHDL source code [113 \(UG\)](#)

constants (SystemVerilog) [176 \(HDLRef\)](#)

constants, VHDL [299 \(HDLRef\)](#)

- SNS (Selected Name Support) [328 \(HDLRef\)](#)

Constraint Check command [1440 \(Ref\)](#)

constraint checker

- check_fdc_query command [40 \(CmdRef\)](#)

constraint checking report [1440 \(Ref\)](#)

constraint file

- define_compile_point [392 \(CmdRef\)](#)
- define_current_design [393 \(CmdRef\)](#)
- syn_connect [207 \(CmdRef\)](#)
- syn_create_err_net [208 \(CmdRef\)](#)

constraint files [1367 \(Ref\)](#)

- .sdc [1405 \(Ref\)](#)
- applying to a collection [216 \(UG\)](#)
- automatic. *See* auto constraints
- compile point [594 \(UG\)](#), [604 \(UG\)](#)
- creating in a text editor [243 \(UG\)](#)
- editing [196 \(UG\)](#)
- editing compile point files [643 \(CmdRef\)](#)
- effects of retiming [545 \(UG\)](#)
- fdc and sdc precedence order [1370 \(Ref\)](#)
- forward-annotation, Lattice [1696 \(Ref\)](#), [1890 \(Ref\)](#), [1984 \(Ref\)](#), [2058 \(Ref\)](#)
- Intel Max+Plus II [1876 \(Ref\)](#)
- Microsemi [2042 \(Ref\)](#)
- options [105 \(UG\)](#)
- PLL [1778 \(Ref\)](#)
- SCOPE spreadsheet [294 \(CmdRef\)](#)
- setting for compile points [616 \(UG\)](#)
- tcl script examples [768 \(UG\)](#)
- translating [504 \(CmdRef\)](#)

constraint files (.sdc)

- creating [1299 \(Ref\)](#)

constraint priority [1370 \(Ref\)](#)

constraint_file Tcl command [45 \(CmdRef\)](#)

constraints

- altpll [1863 \(Ref\)](#)
- auto constraints. *See* auto constraints
- automatic. *See* auto constraints
- check constraints [500 \(CmdRef\)](#)
- defining clocks (Legacy) [227 \(UG\)](#)
- defining register delays (Legacy) [228 \(UG\)](#)
- FPGA timing [342 \(CmdRef\)](#)
- non-DC [1378 \(Ref\)](#)
- priority [1370 \(Ref\)](#)
- report file [1440 \(Ref\)](#)
- specifying through points [200 \(UG\)](#)
- styles [1369 \(Ref\)](#)
- translating Intel constraints [124 \(CmdRef\)](#)
- translating Intel I/O constraints [245 \(UG\)](#)
- translating with ise2syn [748 \(UG\)](#)
- translating Xilinx constraints for logic synthesis [254 \(UG\)](#)
- types [188 \(UG\)](#), [1366 \(Ref\)](#)
- types (legacy) [229 \(UG\)](#)
- using FDC template command [186 \(UG\)](#)
- Vivado flow [1097 \(UG\)](#)

Constraints panel

- Implementation Options dialog box [450 \(CmdRef\)](#)

constructs
 interface [155 \(HDLRef\)](#), [253 \(HDLRef\)](#)
 union (SystemVerilog) [157 \(HDLRef\)](#)

context
 for object in filtered view [433 \(UG\)](#)

context declarations
 VHDL 2008 [430 \(HDLRef\)](#)

context help editor [46 \(UG\)](#), [1287 \(Ref\)](#)
 SystemVerilog [46 \(UG\)](#)

context of filtered schematic, displaying
 [1356 \(Ref\)](#)

context sensitive help
 using the F1 key [1252 \(Ref\)](#)

context window (Physical Analyst) [1026 \(UG\)](#)

context-sensitive popup menus
 See popup menus

Continue on Error
 Configure Compile Point Process [571 \(CmdRef\)](#)

continue on error [104 \(UG\)](#), [298 \(UG\)](#)
 analyzing errors [300 \(UG\)](#)
 compilation [298 \(UG\)](#)
 compile points [304 \(UG\)](#)
 reporting [300 \(UG\)](#)

Continue on Error compile point option
 [571 \(CmdRef\)](#)

continuous assignments (Verilog)
 combinational logic [104 \(HDLRef\)](#)

continuous assignments, Verilog
 level-sensitive latches [108 \(HDLRef\)](#)

control panel
 displaying instances [1688 \(Ref\)](#)
 displaying nets [1688 \(Ref\)](#)
 displaying row sites [1688 \(Ref\)](#)
 displaying signal pins [1688 \(Ref\)](#)
 Physical Analyst view [1023 \(UG\)](#), [1687 \(Ref\)](#), [1689 \(Ref\)](#)

control panel (Physical Analyst) [1687 \(Ref\)](#), [1689 \(Ref\)](#)

control-sets, Xilinx [2100 \(Ref\)](#)

convenience functions [74 \(DebugRef\)](#)

conventions
 design hierarchy [13 \(DebugRef\)](#)
 file system [12 \(DebugRef\)](#)
 symbol [15 \(DebugRef\)](#)
 syntax [11 \(DebugRef\)](#)
 tool [12 \(DebugRef\)](#)

Copy command [402 \(CmdRef\)](#), [13 \(DebugRef\)](#)

Copy File command [614 \(CmdRef\)](#)

Copy Implementation command [615 \(CmdRef\)](#)

copy_collection command [285 \(CmdRef\)](#)

copying
 for pasting [1307 \(Ref\)](#), [30 \(DebugRef\)](#), [32 \(DebugRef\)](#)

copying image
 Create Image command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)

core cells
 displaying [689 \(CmdRef\)](#)

core voltage switch [1838 \(Ref\)](#)

core voltage, Stratix III [1838 \(Ref\)](#), [1867 \(Ref\)](#)

CoreGen [2108 \(Ref\)](#)

cores, instantiating in Xilinx designs
 [2108 \(Ref\)](#)

corruption
 power domains [1223 \(UG\)](#)

counter compiler
 SYNCore [1664 \(Ref\)](#)

counters
 SYNCore [1665 \(Ref\)](#)

counterwidth option [47 \(DebugRef\)](#)

CPLD technology
 Xilinx [2157 \(Ref\)](#)

Create Image command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)

Create Place & Route Options file dialog box [629 \(CmdRef\)](#)

Create Sub-project (Design Block) command [631 \(CmdRef\)](#), [632 \(CmdRef\)](#)

create_clock timing constraint [343 \(CmdRef\)](#)

create_fdc_template
 using [186 \(UG\)](#)

create_generated_clock timing constraint
 [345 \(CmdRef\)](#)

create_power_domain

examples [1204 \(UG\)](#)

create_power_domain Tcl command [711 \(CmdRef\)](#)

create_region Tcl command [48 \(CmdRef\)](#)

critical paths [1361 \(Ref\)](#)

- analyzing [1362 \(Ref\)](#)
- creating new schematics [543 \(CmdRef\)](#)
- custom timing reports [530 \(CmdRef\)](#)
- delay [457 \(UG\)](#)
- finding [1362 \(Ref\)](#), [549 \(CmdRef\)](#)
- flat view [456 \(UG\)](#)
- hierarchical view [456 \(UG\)](#)
- negative slack on clock enables (Legacy) [238 \(UG\)](#)
- slack time [457 \(UG\)](#)
- Timing Report panel, Implementation Options dialog box [456 \(CmdRef\)](#)
- using -route [535 \(UG\)](#)
- viewing [455 \(UG\)](#)

critical paths (Design Planner)

- assigning to regions [999 \(UG\)](#)

critical paths (Physical Analyst)

- tracing backward [489 \(UG\)](#)
- tracing forward [487 \(UG\)](#)

cross probing [688 \(CmdRef\)](#)

cross triggering [4242 \(DebugUG\)](#), [4304 \(DebugUG\)](#), [4306 \(DebugUG\)](#), [4315 \(DebugUG\)](#), [76 \(DebugRef\)](#)

- commands [77 \(DebugRef\)](#)
- enabling [4304 \(DebugUG\)](#), [76 \(DebugRef\)](#)
- state machine commands [77 \(DebugRef\)](#)

cross-clock paths, timing analysis [1433 \(Ref\)](#)

cross-hair mouse pointer [1296 \(Ref\)](#)

cross-module referencing

- Verilog [65 \(HDLRef\)](#)

crossprobing [423 \(UG\)](#), [1341 \(Ref\)](#)

- and retiming [545 \(UG\)](#)
- collection objects [216 \(UG\)](#)
- definition [1341 \(Ref\)](#)
- filtering text objects for [427 \(UG\)](#)
- from FSM viewer [429 \(UG\)](#)
- from log file [270 \(UG\)](#)
- from message viewer [286 \(UG\)](#)
- from text files [426 \(UG\)](#)
- from text files to Physical Analyst [1054 \(UG\)](#)
- Hierarchy Browser [356 \(UG\)](#), [423 \(UG\)](#)
- importance of encoding style [429 \(UG\)](#)
- new HDL Analyst views [357 \(UG\)](#)
- paths [426 \(UG\)](#)
- Physical Analyst view [1052 \(UG\)](#)
- RTL view [424 \(UG\)](#)
- schematic views [356 \(UG\)](#)
- Technology view [424 \(UG\)](#)
- Technology view to Physical Analyst [1057 \(UG\)](#)
- Text Editor view [424 \(UG\)](#)
- text file example [426 \(UG\)](#)
- to FSM Viewer [429 \(UG\)](#)
- to place-and-route file [398 \(UG\)](#)
- Verilog file [424 \(UG\)](#)
- VHDL file [424 \(UG\)](#)
- View Cross Probing commands [1052 \(UG\)](#)
- within RTL and Technology views [423 \(UG\)](#)

crossprobing (Physical Analyst)

- auto route crossprobing [1058 \(UG\)](#)
- RTL view [1052 \(UG\)](#), [1056 \(UG\)](#)
- Technology view [1052 \(UG\)](#)

crossprobing commands (Synplify Premier)

- Physical Analyst view [1052 \(UG\)](#)

Ctrl key

- avoiding docking [1298 \(Ref\)](#)
- multiple selection [1295 \(Ref\)](#)
- zooming using the mouse wheel [1297 \(Ref\)](#)

current level

- expanding logic from net [437 \(UG\)](#)
- expanding logic from pin [437 \(UG\)](#)
- searching current level and below [411 \(UG\)](#)

custom attributes [3632 \(AttrRef\)](#)

custom folders

- creating [91 \(UG\)](#)
- hierarchy management [91 \(UG\)](#)
- project_folder Tcl command [123 \(CmdRef\)](#)

customer support, Synopsys [1254 \(Ref\)](#)

customization

- callback functions [772 \(UG\)](#), [774 \(UG\)](#)

Customize command [568 \(CmdRef\)](#)

customizing

- project files [575 \(CmdRef\)](#)

Cut command [402 \(CmdRef\)](#), [13 \(DebugRef\)](#)
cutting (for pasting) [1300 \(Ref\)](#)
cycles mode
 complex counter [51 \(DebugRef\)](#)
Cyclone [1843 \(Ref\)](#)
 device options [1843 \(Ref\)](#)
 file format options [1846 \(Ref\)](#)
 set_option device options [1845 \(Ref\)](#)
 set_option synthesis options [1846 \(Ref\)](#)

D

D flip-flop, active-high reset, set (VHDL)
 asynchronous [354 \(HDLRef\)](#)
 synchronous [356 \(HDLRef\)](#)
data block [631 \(UG\)](#)
data compression [4240 \(DebugUG\)](#), [4292 \(DebugUG\)](#), [4305 \(DebugUG\)](#)
 masking [4292 \(DebugUG\)](#)
data key [631 \(UG\)](#)
data objects (SystemVerilog) [175 \(HDLRef\)](#)
data type conversion [161 \(HDLRef\)](#)
data types
 in SystemVerilog parameters [182 \(HDLRef\)](#)
data types (SystemVerilog) [145 \(HDLRef\)](#)
data types (VHDL) [287 \(HDLRef\)](#)
data types, VHDL
 guidelines [340 \(HDLRef\)](#)
DCM clock priority [3531 \(AttrRef\)](#)
DDR register inference
 Xilinx [2082 \(Ref\)](#)
DDR3
 memory card for debug [4244 \(DebugUG\)](#)
Debugger tool
 invoking [4282 \(DebugUG\)](#)
debugging
 on separate machines [4313 \(DebugUG\)](#)
 performance [4318 \(DebugUG\)](#)
 using BRAM [4318 \(DebugUG\)](#)
declared clock [1429 \(Ref\)](#)
declaring and assigning objects (VHDL)
 [291 \(HDLRef\)](#)
default assignment (VHDL) [361 \(HDLRef\)](#)
default enum encoding [113 \(UG\)](#)

default propagation [334 \(HDLRef\)](#)
define_attribute [124 \(UG\)](#)
 syntax [3373 \(AttrRef\)](#)
define_clock
 forward-annotation, Intel Max+Plus II
 [1876 \(Ref\)](#)
 forward-annotation, Microsemi [2042 \(Ref\)](#)
define_compile_point
 Tcl [392 \(CmdRef\)](#)
define_current_design
 Tcl [393 \(CmdRef\)](#)
define_false_path
 forward-annotation, Microsemi [2043 \(Ref\)](#)
 using with syn_keep [3722 \(AttrRef\)](#)
define_global_attribute
 summary [3384 \(AttrRef\)](#)
 syntax [3373 \(AttrRef\)](#)
define_input_delay
 forward-annotation with
 syn_forward_io_constraints [3653 \(AttrRef\)](#)
 forward-annotation, Intel Max+Plus II
 [1876 \(Ref\)](#)
define_multicycle_path
 forward-annotation, Microsemi [2043 \(Ref\)](#)
 using with syn_keep [3722 \(AttrRef\)](#)
define_output_delay
 forward-annotation with
 syn_forward_io_constraints [3653 \(AttrRef\)](#)
 forward-annotation, Intel Max+Plus II
 [1876 \(Ref\)](#)
define_path_delay
 forward-annotation, Microsemi [2043 \(Ref\)](#)
defining I/O standards [314 \(CmdRef\)](#)
delay paths
 POS [334 \(CmdRef\)](#)
Delay Paths panel
 using SCOPE [189 \(UG\)](#)
Delay Paths panel, SCOPE [310 \(CmdRef\)](#)
delays
 forward annotating [3653 \(AttrRef\)](#)

- forward-annotating with
syn_forward_io_constraints 3653 (AttrRef)
- Delete all bookmarks command 403 (CmdRef)
- Delete Region Assignments command 661 (CmdRef)
- Delete Region command 661 (CmdRef)
- Delete Selected Assignments command 661 (CmdRef)
- deleting
 - See removing
- Demos & Examples 1289 (Ref)
- depth option 50 (DebugRef)
- derived clock 1430 (Ref)
- Design Block Properties command (hierarchical project management) 634 (CmdRef)
- Design Compiler
 - avoiding DesignWare IP black boxes 280 (UG)
- design files
 - writing 89 (DebugRef)
- design flow 4199 (DebugUG)
 - customizing with callback functions 772 (UG), 774 (UG)
- design flows
 - hierarchical project management 22 (UG)
 - Synplify Premier synthesis 18 (UG)
 - synthesis (Intel) 1772 (Ref)
 - synthesis (Xilinx) 2060 (Ref)
 - team design 22 (UG)
- design guidelines 532 (UG)
- design hierarchy 38 (DebugRef)
 - viewing 364 (UG), 431 (UG)
- design hierarchy conventions 13 (DebugRef)
- Design Hierarchy view (hierarchical project management) 1261 (Ref)
- Design Hierarchy view (hierarchical project management) icons 1262 (Ref)
- Design Intent
 - achieving best QoR 1197 (UG)
 - achieving fast turnaround 1195 (UG)
 - running place and route 1198 (UG)
- design parameters (Verilog)
 - extracting 470 (CmdRef)
- design plan
 - options 106 (UG)
- Design Plan Editor 1683 (Ref)
- Design Plan Editor view 1683 (Ref)
 - preserving region resources 994 (UG)
- design plan file
 - logic synthesis 19 (UG)
- design plan file (.sfp) 1406 (Ref)
- Design Plan Hierarchical view 1681 (Ref)
- Design Plan Hierarchy view 1681 (Ref)
- Design Plan view 1683 (Ref)
- design plan view file (.srp) 1417 (Ref), 543 (CmdRef)
- Design Planner
 - assigning pins 983 (UG)
 - creating chip regions 995 (UG)
 - displaying IP core areas 995 (UG)
 - Generation 2 956 (UG)
 - guidelines 955 (UG)
 - logic synthesis 19 (UG)
 - opening 976 (UG)
 - popup menus 673 (CmdRef)
 - Preferences dialog box 668 (CmdRef)
 - Properties command 663 (CmdRef)
 - working with SSI devices 1006 (UG)
- Design Planner (Legacy) 976 (UG)
- design planner constraint files (.sfp)
 - creating 1299 (Ref)
- Design Planner option
 - views 1680 (Ref)
- Design Planner tools menu
 - Preferences command 668 (CmdRef)
 - Show Replicated Assignments command 668 (CmdRef)
- Design Planner view 1680 (Ref)
- design planning 976 (UG)
- Design Planning panel, Implementation Options dialog box 665 (CmdRef)
- design size
 - amount displayed on a sheet 398 (UG)
- design size, schematic sheet
 - setting 1344 (Ref)
- design views

- moving between views [333 \(UG\)](#), [397 \(UG\)](#)
- designs
 - writing instrumented [4208 \(DebugUG\)](#)
- DesignWare
 - avoiding black boxes for IP [280 \(UG\)](#)
 - building blocks [651 \(UG\)](#)
 - DW_Foundation_Arith package [653 \(UG\)](#)
 - foundation library [651 \(UG\)](#)
 - importing cores [649 \(UG\)](#)
 - license queuing [757 \(UG\)](#)
 - minPower library [652 \(UG\)](#)
 - multiprocessing licenses [653 \(UG\)](#)
 - number of licenses [653 \(UG\)](#)
- DesignWare options
 - VHDL panel [461 \(CmdRef\)](#), [467 \(CmdRef\)](#)
- device command [31 \(DebugRef\)](#)
- device ID codes [43 \(DebugRef\)](#)
- device option
 - Update Compile Point Timing Data [1750 \(Ref\)](#)
- device options [1751 \(Ref\)](#), [1952 \(Ref\)](#)
 - See also* implementation options
 - CPLDs (Xilinx) [2157 \(Ref\)](#)
 - iCE65 Lattice technology [1952 \(Ref\)](#)
 - Spartan technologies (Xilinx) [2147 \(Ref\)](#)
 - Virtex technologies (Xilinx) [2147 \(Ref\)](#)
- device options (Microsemi) [2035 \(Ref\)](#)
- Device panel
 - Conservative Register Optimization [170 \(CmdRef\)](#)
 - Implementation Options dialog box [445 \(CmdRef\)](#)
- device view
 - Physical Analyst [1691 \(Ref\)](#)
- dh_module_sources Tcl command [63 \(CmdRef\)](#)
- dialog boxes
 - Configure IICE [4312 \(DebugUG\)](#)
 - Enhanced Instance Display [689 \(CmdRef\)](#)
 - Find Object (Physical Analyst) [699 \(CmdRef\)](#)
 - Implementation Options [444 \(CmdRef\)](#)
 - Physical Analyst Properties [697 \(CmdRef\)](#)
 - Region Properties [663 \(CmdRef\)](#)
 - Replicated Assignments [668 \(CmdRef\)](#)
 - Resolve Selection [703 \(CmdRef\)](#)
- diff_term attribute [3431 \(AttrRef\)](#)
- directives
 - _SEARCHFILENAMEONLY_ [474 \(CmdRef\)](#)
 - adding [115 \(UG\)](#)
 - adding in Verilog [117 \(UG\)](#)
 - adding in VHDL [116 \(UG\)](#)
 - beta features [473 \(CmdRef\)](#)
 - black box [497 \(UG\)](#), [498 \(UG\)](#)
 - black box instantiation (VHDL) [399 \(HDLRef\)](#)
 - for FSMs [503 \(UG\)](#)
 - handling properties [125 \(UG\)](#)
 - ignore syntax check [472 \(CmdRef\)](#)
 - IGNORE_VERILOG_BLACKBOX_GUTS [472 \(CmdRef\)](#)
 - Intel [1882 \(Ref\)](#)
 - specifying [133 \(HDLRef\)](#)
 - specifying for the compiler (Verilog) [470 \(CmdRef\)](#)
 - specifying for Verilog compiler [111 \(UG\)](#)
 - syn_state_machine [566 \(UG\)](#)
 - syn_tco [498 \(UG\)](#)
 - adding black box constraints [497 \(UG\)](#)
 - syn_tpd [498 \(UG\)](#)
 - adding black box constraints [497 \(UG\)](#)
 - syn_tsu [498 \(UG\)](#)
 - adding black box constraints [497 \(UG\)](#)
 - syntax, Verilog [133 \(HDLRef\)](#)
 - syntax, VHDL [401 \(HDLRef\)](#)
- directives (Achronix) [1764 \(Ref\)](#)
- directives (Microsemi) [2050 \(Ref\)](#)
- directives (Xilinx) [2173 \(Ref\)](#)
- directives in .cdc file [119 \(UG\)](#)
- directories
 - changing [21 \(DebugRef\)](#)
 - displaying working [58 \(DebugRef\)](#)
 - instrumentation [4232 \(DebugUG\)](#)
- directory
 - examples delivered with synthesis tool [9 \(UG\)](#)
- disable I/O insertion (Lattice) [1933 \(Ref\)](#)
- Disable Sequential Optimizations (Xilinx) [2141 \(Ref\)](#)
- disabling sequential optimizations [168 \(CmdRef\)](#)
- display settings
 - Project view [575 \(CmdRef\)](#)

Dissolve Instances command [1359](#)
([Ref](#)), [551](#) ([CmdRef](#))

Dissolve to Gates command [551](#) ([CmdRef](#))

dissolving instances [551](#) ([CmdRef](#))

dissolving instances for flattening hierarchy [444](#) ([UG](#))

distributed place and route using [800](#) ([UG](#))

distributed processing [154](#) ([CmdRef](#))
setting CDPL [787](#) ([UG](#))
using [786](#) ([UG](#))

distributed RAM
inferring [1487](#) ([Ref](#))

distributed RAM examples [1490](#) ([Ref](#))

distributed TMR [871](#) ([UG](#))
example [873](#) ([UG](#))

DLLs
defining clocks (Legacy) [237](#) ([UG](#))

docking [1277](#) ([Ref](#))
avoiding [1298](#) ([Ref](#))

docking GUI entities
toolbar [1298](#) ([Ref](#))

dot wildcard
Find command [355](#) ([UG](#)), [414](#) ([UG](#))

do-while loops (SystemVerilog) [212](#)
([HDLRef](#))

drivers
preserving duplicates with syn_keep [549](#) ([UG](#))
selecting [440](#) ([UG](#))

DSP (Xilinx) [3581](#) ([AttrRef](#)), [3589](#) ([AttrRef](#))

DSP blocks
inferencing [1987](#) ([Ref](#))
Intel megafunctions [1789](#) ([Ref](#))
packing resets (Intel) [1814](#) ([Ref](#))

DSP blocks (Intel) [1789](#) ([Ref](#))

DSP48 (Xilinx) [2061](#) ([Ref](#))
converting asynchronous reset registers [3523](#) ([AttrRef](#)), [3531](#) ([AttrRef](#)), [3867](#) ([AttrRef](#))

DSP48 structures (Xilinx) [2061](#) ([Ref](#))

DSP48 Xilinx
inferring XNOR [2069](#) ([Ref](#))
symmetric rounding [2069](#) ([Ref](#))

DSP48E, wide adder inference [2099](#) ([Ref](#))

dual-port RAM
true dual-port RAM
See multi-port RAMs

dual-port RAM examples [1468](#) ([Ref](#))

dual-port RAMs
SYNCore parameters [1593](#) ([Ref](#))

duplicate modules (Verilog)
Tcl option [152](#) ([CmdRef](#)), [157](#) ([CmdRef](#))

DW_Foundation_Arith package [653](#) ([UG](#))

DWC
description [895](#) ([UG](#))

DWC (Duplicate with compare) [870](#) ([UG](#))

dynamic range assignment (VHDL) [292](#)
([HDLRef](#))

E

ECC RAM [922](#) ([UG](#))

edf file. See edif file

EDIF
structural, for Xilinx IP cores [2108](#) ([Ref](#))

edif file
bus name styles [3617](#) ([AttrRef](#))
character case [3605](#) ([AttrRef](#))
port name length [3601](#) ([AttrRef](#))
scalar and array ports [3787](#) ([AttrRef](#))
syn_noarrayports attribute [3787](#) ([AttrRef](#))

EDIF files
reoptimizing [2171](#) ([Ref](#))

edif files
Intel naming requirements [1880](#) ([Ref](#))

Edit Attributes command [642](#) ([CmdRef](#))

Edit Compile Point Constraints command [643](#) ([CmdRef](#))

Edit menu [402](#) ([CmdRef](#)), [13](#) ([DebugRef](#))
Advanced submenu [403](#) ([CmdRef](#))

Edit Module Constraints command [643](#)
([CmdRef](#))

Edit Regions command [661](#) ([CmdRef](#))

Edit Run Configuration command [441](#)
([CmdRef](#))

Editing window [50](#) ([UG](#))

editor
compiler directives [38](#) ([UG](#))

Editor Options command [568](#) ([CmdRef](#))

editor view
 context help [46 \(UG\)](#), [1287 \(Ref\)](#)
 EDK
 specifying cores as white boxes [749 \(UG\)](#)
 EDN core [734 \(UG\)](#)
 else/elsif clauses
 VHDL 2008 [436 \(HDLRef\)](#)
 emacs text editor [55 \(UG\)](#)
 enable
 in std_logic_vector (3 downto 0) [4029 \(AttrRef\)](#)
 enable prepacking [2144 \(Ref\)](#)
 Enable Slack Margin [534 \(CmdRef\)](#)
 enable_io_map.txt file [1779 \(Ref\)](#)
 encoding
 enumeration, default (VHDL) [341 \(HDLRef\)](#), [460 \(CmdRef\)](#)
 state machine
 displaying [612 \(CmdRef\)](#)
 FSM Compiler [563 \(UG\)](#)
 FSM Explorer [567 \(UG\)](#), [1316 \(Ref\)](#)
 guidelines
 Verilog [116 \(HDLRef\)](#)
 encoding styles
 and crossprobing [429 \(UG\)](#)
 default VHDL [113 \(UG\)](#)
 FSM Compiler [564 \(UG\)](#)
 encrypted IP objects (Physical Analyst)
 identifying cells [1050 \(UG\)](#)
 encrypting source files [31 \(DebugRef\)](#)
 encryption
 asymmetric [631 \(UG\)](#)
 methodologies [629 \(UG\)](#)
 symmetric [631 \(UG\)](#)
 synenc [649 \(UG\)](#)
 encryption algorithms [631 \(UG\)](#)
 encryption command [36 \(DebugRef\)](#)
 encryptip output constraints [648 \(UG\)](#)
 encryptip output method
 effect on output netlists [648 \(UG\)](#)
 encryptIP script [645 \(UG\)](#)
 command-line arguments [68 \(CmdRef\)](#)
 encrypting IP [645 \(UG\)](#)
 output methods [646 \(UG\)](#)
 syntax [68 \(CmdRef\)](#)
 encryptP1735 script [71 \(CmdRef\)](#)
 command-line arguments [71 \(CmdRef\)](#)
 public keys repository file [72 \(CmdRef\)](#)
 syntax [71 \(CmdRef\)](#)
 use models [74 \(CmdRef\)](#)
 encryptP1735.pl script [640 \(UG\)](#)
 enhanced display mode [689 \(CmdRef\)](#)
 Enhanced Instance Display dialog box
 [689 \(CmdRef\)](#)
 entity tristate2 is port (input3, input2, input1, input0
 in std_logic_vector (7 downto 0) [4029 \(AttrRef\)](#)
 enumerated types
 syn_enum encoding directive [3631 \(AttrRef\)](#)
 enumerated types (SystemVerilog) [148 \(HDLRef\)](#)
 enumerated types (VHDL) [361 \(HDLRef\)](#)
 enumeration encoding, default (VHDL)
 [341 \(HDLRef\)](#), [460 \(CmdRef\)](#)
 environment variables
 accessing, get_env Tcl command [87 \(CmdRef\)](#)
 SYN_TCL_HOOKS [772 \(UG\)](#)
 error codes [753 \(UG\)](#)
 error correction code. *See* ECC [922 \(UG\)](#)
 error messages
 gated clock report [821 \(UG\)](#)
 error mitigation. *See* high reliability
 errors
 black boxing [300 \(UG\)](#)
 continuing [104 \(UG\)](#), [298 \(UG\)](#)
 definition [49 \(UG\)](#)
 filtering [285 \(UG\)](#)
 sorting [285 \(UG\)](#)
 source files [48 \(UG\)](#)
 Verilog [48 \(UG\)](#)
 VHDL [48 \(UG\)](#)
 essential signal database [4225 \(DebugUG\)](#)
 est file [1414 \(Ref\)](#), [666 \(CmdRef\)](#)
 Estimate All Regions command [667 \(CmdRef\)](#)
 Estimate Area command [499 \(CmdRef\)](#), [666 \(CmdRef\)](#)
 Estimate Regions command [667 \(CmdRef\)](#)

estimation
 area [666 \(CmdRef\)](#), [667 \(CmdRef\)](#)
estimation (setting in Design Planner)
 area
 warning settings [669 \(CmdRef\)](#)
estimation file, area (.est) [1414 \(Ref\)](#), [666 \(CmdRef\)](#)
estimation log file (_est.srr) [1414 \(Ref\)](#)
events mode
 complex counter [51 \(DebugRef\)](#)
events, defining outside process (VHDL) [345 \(HDLRef\)](#)
Example
 ECC of RAM [948 \(UG\)](#)
 fault-tolerant FSMs [949 \(UG\)](#)
 Local TMR [946 \(UG\)](#)
 RAMs [947 \(UG\)](#)
Example 1
 Error Monitoring with DWC [926 \(UG\)](#)
Example 2
 Error Monitoring with DTMR [926 \(UG\)](#)
Example 3
 Error Monitoring with ECC/TMR RAM [927 \(UG\)](#), [929 \(UG\)](#)
Example 4
 Error Monitoring with Safe Case FSM [931 \(UG\)](#)
Example 5
 Error Monitoring with Hamming 3 FSM [933 \(UG\)](#)
examples
 Demos & Examples [1289 \(Ref\)](#)
 Interactive Attribute Examples [1290 \(Ref\)](#)
 Tcl find command syntax [225 \(CmdRef\)](#)
examples delivered with synthesis tool,
 directory [9 \(UG\)](#)
Exit command [397 \(CmdRef\)](#)
exit command [37 \(DebugRef\)](#)
exit statement [319 \(HDLRef\)](#)
expand
 batch mode [212 \(UG\)](#)
Expand command
 connection logic [440 \(UG\)](#)
 connections in Physical Analyst [1065 \(UG\)](#)
 current level [545 \(CmdRef\)](#)
 hierarchical [544 \(CmdRef\)](#)
 pin and net logic [371 \(UG\)](#), [436 \(UG\)](#)
 using [437 \(UG\)](#)
expand command
 different from Tcl search [417 \(UG\)](#)
Expand command (Physical Analyst) [1060 \(UG\)](#)
expand command (Tcl). See Tcl expand command
Expand Inwards command [544 \(CmdRef\)](#)
 using [371 \(UG\)](#), [437 \(UG\)](#)
Expand Path Backward command [489 \(UG\)](#)
Expand Path Forward command [487 \(UG\)](#)
Expand Paths command
 current level [545 \(CmdRef\)](#)
 different from Isolate Paths [440 \(UG\)](#)
 hierarchical [544 \(CmdRef\)](#)
expand pin view (Design Planner) [979 \(UG\)](#)
Expand to Register/Port command
 current level [545 \(CmdRef\)](#)
 hierarchical [544 \(CmdRef\)](#)
 using [437 \(UG\)](#)
Expand to Register/Port command (Physical Analyst) [1060 \(UG\)](#)
Expanded Pin View command [662 \(CmdRef\)](#)
expanding
 connections [440 \(UG\)](#)
 connections (Physical Analyst) [1065 \(UG\)](#)
 paths between schematic objects [544 \(CmdRef\)](#)
 pin and net logic [371 \(UG\)](#), [436 \(UG\)](#)
 pin and net logic (Physical Analyst) [1060 \(UG\)](#)
Explorer, FSM
 enabling [1316 \(Ref\)](#)
 overview [567 \(UG\)](#)
exponential operator [27 \(HDLRef\)](#)
export project Tcl command [81 \(CmdRef\)](#)
extra initialization state, creating (VHDL) [362 \(HDLRef\)](#)
Extract Parameters [470 \(CmdRef\)](#)

F

- factorials
 - calculating [62 \(HDLRef\)](#)
- failures, timing (definition) [1363 \(Ref\)](#)
- false paths
 - architectural [328 \(CmdRef\)](#)
 - clocks as from/to points [337 \(CmdRef\)](#)
 - code-introduced [328 \(CmdRef\)](#)
 - defined [328 \(CmdRef\)](#)
 - defining between clocks (Legacy) [242 \(UG\)](#)
 - I/O paths [204 \(UG\)](#)
 - impact of clock group assignments [204 \(UG\)](#)
 - impact of clock group assignments (Legacy) [242 \(UG\)](#)
 - ports [204 \(UG\)](#)
 - ports (Legacy) [242 \(UG\)](#)
 - POS [334 \(CmdRef\)](#)
 - registers [204 \(UG\)](#)
 - registers (Legacy) [242 \(UG\)](#)
 - setting constraints [204 \(UG\)](#)
 - setting constraints (Legacy) [242 \(UG\)](#)
- fanin (Lattice) [1937 \(Ref\)](#)
- fanout
 - Microsemi [2026 \(Ref\)](#)
 - replicating instances (Design Planner) [999 \(UG\)](#)
- Fanout Guide option (Xilinx) [2139 \(Ref\)](#)
- fanout limits
 - overriding default [3755 \(AttrRef\)](#)
 - syn_maxfan attribute [3755 \(AttrRef\)](#)
- fanouts
 - buffering vs replication [557 \(UG\)](#)
 - hard limits [556 \(UG\)](#)
 - soft global limit [555 \(UG\)](#)
 - soft module-level limit [556 \(UG\)](#)
 - using syn_keep for replication [550 \(UG\)](#)
 - using syn_maxfan [555 \(UG\)](#)
- fanouts (Intel) [1839 \(Ref\)](#)
- fanouts (Lattice) [1933 \(Ref\)](#)
- fanouts (Xilinx) [2138 \(Ref\)](#)
- fast signal database [4309 \(DebugUG\)](#)
- fast synthesis
 - compile points [621 \(UG\)](#)
 - using [574 \(UG\)](#), [579 \(UG\)](#)
- fast turnaround
 - prototypes [1195 \(UG\)](#)
- Fault Injection [940 \(UG\)](#)
- fault injection [935 \(UG\)](#)
 - Fault clock [936 \(UG\)](#)
 - Fault node [936 \(UG\)](#)
- fault tolerance. *See* [high reliability](#)
- FDC
 - create_clock constraint [343 \(CmdRef\)](#)
 - create_generated_clock [345 \(CmdRef\)](#)
 - reset_path [349 \(CmdRef\)](#)
 - set_clock_groups [353 \(CmdRef\)](#)
 - set_clock_latency [360 \(CmdRef\)](#)
 - set_clock_route_delay [362 \(CmdRef\)](#)
 - set_clock_uncertainty [363 \(CmdRef\)](#)
 - set_datapathonly_delay [365 \(CmdRef\)](#)
 - set_false_path [368 \(CmdRef\)](#)
 - set_input_delay [371 \(CmdRef\)](#)
 - set_max_delay [374 \(CmdRef\)](#)
 - set_multicycle_path [380 \(CmdRef\)](#)
 - set_output_delay [384 \(CmdRef\)](#)
 - set_reg_input_delay [387 \(CmdRef\)](#)
 - set_reg_output_delay [388 \(CmdRef\)](#)
 - standard collection commands [282 \(CmdRef\)](#)
- fdc
 - constraint priority [1370 \(Ref\)](#)
 - precedence over sdc [1370 \(Ref\)](#)
- fdc constraints [1372 \(Ref\)](#)
 - generation process [1370 \(Ref\)](#)
- fdc file
 - relationship with other constraint files [1367 \(Ref\)](#)
- feature comparison
 - FPGA tools [1245 \(Ref\)](#)
- FIFO compiler
 - SYNCore [1556 \(Ref\)](#)
- FIFO flags
 - empty/almost empty [1578 \(Ref\)](#)
 - full/almost full [1577 \(Ref\)](#)
 - handshaking [1578 \(Ref\)](#)
 - programmable [1580 \(Ref\)](#)
 - programmable empty [1583 \(Ref\)](#)
 - programmable full [1581 \(Ref\)](#)
- FIFOs
 - compiling with SYNCore [1557 \(Ref\)](#)
- file format options

project command (Intel) [1858 \(Ref\)](#)

File menu

Recent Projects submenu [397 \(CmdRef\)](#)

File Options command [622 \(CmdRef\)](#)

file system conventions [12 \(DebugRef\)](#)

files

- `_est.srr` [1414 \(Ref\)](#)
- `.adc` [1404 \(Ref\)](#)
- `.areasrr` [1413 \(Ref\)](#)
- `.cdc` [1404 \(Ref\)](#)
- `.edf`. *See* edif file
- `.est` [1414 \(Ref\)](#), [666 \(CmdRef\)](#)
- `.fdc` [1404 \(Ref\)](#)
- `.fse` [1414 \(Ref\)](#)
- `.info` [1414 \(Ref\)](#)
- `.ini` [1405 \(Ref\)](#)
- `.lpf` [1890 \(Ref\)](#), [1892 \(Ref\)](#)
- `.nrf` [1405 \(Ref\)](#)
- `.opt` [1405 \(Ref\)](#), [1415 \(Ref\)](#)
- `.prf` file [288 \(UG\)](#)
- `.prj` [11 \(UG\)](#), [1405 \(Ref\)](#)
- `.sar` [1417 \(Ref\)](#)
- `.sdc` [1405 \(Ref\)](#)
- `.sfp` [1406 \(Ref\)](#)
- `.srm` [1417 \(Ref\)](#), [1419 \(Ref\)](#)
- `.srp` [1417 \(Ref\)](#), [543 \(CmdRef\)](#)
- `.srr` [1421 \(Ref\)](#)
 - watching selected information [1276 \(Ref\)](#)
- `.srs` [1417 \(Ref\)](#)
- `.ta` [1419 \(Ref\)](#)
- `.ta` *See also* timing report file [532 \(CmdRef\)](#)
- `.tcl` for Xilinx `xtclsh` [1406 \(Ref\)](#), [1419 \(Ref\)](#)
- `.v` [1406 \(Ref\)](#), [1407 \(Ref\)](#)
- `.vhd` [1407 \(Ref\)](#)
- `.vhm` [1420 \(Ref\)](#)
- `.vm` [1420 \(Ref\)](#)
- `.xnf` (Xilinx). *See* `xnf` file (Xilinx)

adding to project [25 \(CmdRef\)](#), [426 \(CmdRef\)](#)

altpll component declarations [1862 \(Ref\)](#)

area estimation (`.est`) [1414 \(Ref\)](#), [666 \(CmdRef\)](#)

compiler output (`.srs`) [1417 \(Ref\)](#)

constraint [45 \(CmdRef\)](#)

constraint (`.adc`) [1404 \(Ref\)](#)

constraint (`.sdc`) [1405 \(Ref\)](#)

copying [614 \(CmdRef\)](#), [615 \(CmdRef\)](#)

creating [1299 \(Ref\)](#)

customized timing report (`.ta`) [1419 \(Ref\)](#)

dependent list [143 \(UG\)](#)

design component info (`.info`) [1414 \(Ref\)](#)

design plan (`.sfp`) [1406 \(Ref\)](#)

design plan view (`.srp`) [1417 \(Ref\)](#), [543 \(CmdRef\)](#)

encrypting source [31 \(DebugRef\)](#)

estimation log (`_est.srr`) [1414 \(Ref\)](#)

filtered messages [289 \(UG\)](#)

`fsm.info` [565 \(UG\)](#)

`idc` [4214 \(DebugUG\)](#)

IICE core [4232 \(DebugUG\)](#)

include [26 \(CmdRef\)](#)

initialization (`.ini`) [1405 \(Ref\)](#)

`last_run.adb` [4299 \(DebugUG\)](#)

log [267 \(UG\)](#)

log (`.srr`) [1421 \(Ref\)](#)

- watching selected information [1276 \(Ref\)](#)

log. *See* log file

mapper output (`.srm`) [1417 \(Ref\)](#), [1419 \(Ref\)](#)

message filter (`prf`) [288 \(UG\)](#)

Netlist Restructure (`.nrf`) [1405 \(Ref\)](#)

opening recent project [397 \(CmdRef\)](#)

organization into folders [575 \(CmdRef\)](#)

output

- See* output files

partitioned RTL view (`.srp`) [1417 \(Ref\)](#), [543 \(CmdRef\)](#)

physical synthesis netlist (`.srp`) [543 \(CmdRef\)](#)

project [121 \(CmdRef\)](#), [4237 \(DebugUG\)](#)

project (`.prj`) [11 \(UG\)](#), [1405 \(Ref\)](#)

removing from project [423 \(CmdRef\)](#)

replacing in project [429 \(CmdRef\)](#)

`rom.info` [404 \(UG\)](#)

RTL view (`.srs`) [1417 \(Ref\)](#)

searching [162 \(UG\)](#), [61 \(DebugRef\)](#)

`srr` [1421 \(Ref\)](#)

- watching selected information [1276 \(Ref\)](#)

`srs` *See* `srs` file

stand-alone timing report (`.ta`) [519 \(CmdRef\)](#)

state machine encoding (`.fse`) [1414 \(Ref\)](#)

`statemachine.info` [449 \(UG\)](#)

`syn_trigger_utils.tcl` [74 \(DebugRef\)](#)

`synhooks.tcl` [772 \(UG\)](#)

Synopsys archive file (`.sar`) [1417 \(Ref\)](#)

synthesis output [1413 \(Ref\)](#)

Tcl [759 \(UG\)](#)

See also Tcl commands
 Tcl batch script [753 \(UG\)](#)
 Technology view (.srm) [1417 \(Ref\)](#), [1419 \(Ref\)](#)
 temporary [552 \(CmdRef\)](#)
 timing report. *See also* timing report file [532 \(CmdRef\)](#)
 Verdi fast signal database [88 \(DebugRef\)](#)
 Verilog (.v) [1406 \(Ref\)](#), [1407 \(Ref\)](#)
 Verilog Change Dump [93 \(DebugRef\)](#)
 VHDL (.vhd) [1407 \(Ref\)](#)
 writing design [89 \(DebugRef\)](#)
 Xilinx (.opt) [1405 \(Ref\)](#), [1415 \(Ref\)](#)
 files for synthesis [1404 \(Ref\)](#)
 Filter Schematic command [546 \(CmdRef\)](#)
 popup menu [607 \(CmdRef\)](#)
 Filter Schematic command, using [369 \(UG\)](#), [434 \(UG\)](#)
 Filter Schematic icon, using [369 \(UG\)](#), [434 \(UG\)](#)
 filtered schematic
 compared with unfiltered [1327 \(Ref\)](#)
 filtering [369 \(UG\)](#), [434 \(UG\)](#), [1355 \(Ref\)](#)
 advantages over flattening [369 \(UG\)](#), [434 \(UG\)](#)
 commands [1355 \(Ref\)](#)
 compared with flattening [1359 \(Ref\)](#)
 critical paths [549 \(CmdRef\)](#)
 FSM states and transitions [1327 \(Ref\)](#), [418 \(CmdRef\)](#)
 paths from pins or ports [1363 \(Ref\)](#), [550 \(CmdRef\)](#)
 selected objects [546 \(CmdRef\)](#)
 timing reports [531 \(CmdRef\)](#)
 using to restrict search [411 \(UG\)](#)
 filtering (Physical Analyst) [1059 \(UG\)](#)
 filtering critical paths [1362 \(Ref\)](#)
 filtering design objects
 Physical Analyst [701 \(CmdRef\)](#)
 Find again command [403 \(CmdRef\)](#)
 Find command
 [411 \(UG\)](#)
 browsing with [410 \(UG\)](#)
 HDL Analyst [407 \(CmdRef\)](#)
 hierarchical search [412 \(UG\)](#)
 long names [410 \(UG\)](#)
 message viewer [285 \(UG\)](#)
 Physical Analyst view [1043 \(UG\)](#), [686 \(CmdRef\)](#)
 reading long names [413 \(UG\)](#)
 search scope, effect of [414 \(UG\)](#)
 search scope, setting [412 \(UG\)](#)
 searching the mapped database [413 \(UG\)](#)
 searching the output netlist [419 \(UG\)](#)
 setting limit for results [413 \(UG\)](#)
 Text Editor [402 \(CmdRef\)](#)
 using in RTL and Technology views [411 \(UG\)](#)
 using wildcards [355 \(UG\)](#), [414 \(UG\)](#)
 wildcard examples [416 \(UG\)](#)
 find command
 batch mode [103 \(CmdRef\)](#)
 different from Tcl search [417 \(UG\)](#)
 filter properties [230 \(CmdRef\)](#)
 hierarchy [417 \(UG\)](#)
 nuances and differences [418 \(UG\)](#)
 Find command (Physical Analyst) [699 \(CmdRef\)](#)
 using Filter Search option [1046 \(UG\)](#)
 using wildcards [1045 \(UG\)](#)
 find command (Tcl)
 See Tcl find command
 Find Object dialog box
 filtering design objects [701 \(CmdRef\)](#)
 Find Object dialog box (Physical Analyst) [699 \(CmdRef\)](#)
 find option [40 \(DebugRef\)](#)
 finding
 critical paths [1362 \(Ref\)](#), [549 \(CmdRef\)](#)
 information on synthesis tool [1253 \(Ref\)](#)
 GUI [1252 \(Ref\)](#)
 finding objects
 Physical Analyst view [1043 \(UG\)](#)
 finding objects (Physical Analyst) [699 \(CmdRef\)](#)
 finite state machines
 See state machines
 fix gated clocks
 syn_gatedclk_clock_en directive [3663 \(AttrRef\)](#)
 Fix Gated Clocks option. *See* gated clocks
 Flatten Current Schematic command [1359 \(Ref\)](#)

- filtered schematic [547 \(CmdRef\)](#)
- transparent instances [442 \(UG\)](#)
- unfiltered schematic [546 \(CmdRef\)](#)
- using [442 \(UG\)](#)
- Flatten Schematic command [1359 \(Ref\)](#)
- using [442 \(UG\)](#)
- Flattened Critical Path command [544 \(CmdRef\)](#)
- flattened schematic, creating [543 \(CmdRef\)](#)
- Flattened to Gates View command [543 \(CmdRef\)](#)
- Flattened View command [543 \(CmdRef\)](#)
- flattening [381 \(UG\)](#), [441 \(UG\)](#)
 - See also* dissolving commands [1357 \(Ref\)](#)
 - compared to filtering [369 \(UG\)](#), [434 \(UG\)](#)
 - compared with filtering [1359 \(Ref\)](#)
 - dissolving instances [381 \(UG\)](#), [444 \(UG\)](#)
 - hidden instances [443 \(UG\)](#)
 - instances [551 \(CmdRef\)](#)
 - schematics [546 \(CmdRef\)](#)
 - selected instances [1358 \(Ref\)](#)
 - transparent instances [442 \(UG\)](#)
 - using `syn_hier` [553 \(UG\)](#)
 - using `syn_netlist_hierarchy` [553 \(UG\)](#)
- flip-flops
 - Verilog [107 \(HDLRef\)](#)
- flip-flops (VHDL) [342 \(HDLRef\)](#)
- Float command
 - Watch window popup menu [1277 \(Ref\)](#)
- floating
 - toolbar [1298 \(Ref\)](#)
- Floating License Usage command [602 \(CmdRef\)](#)
- floating toolbar popup menu [1298 \(Ref\)](#)
- Floorplan Editor
 - selecting objects [692 \(CmdRef\)](#)
- floorplan file. *See* `sfp` file, design plan file
- floorplan objects [688 \(CmdRef\)](#)
- floorplan. *See* Design Planner
- Floorplanned View command [543 \(CmdRef\)](#)
- folded hierarchy [4223 \(DebugUG\)](#)
- folded signals [4296 \(DebugUG\)](#)
- folded watchpoints [4289 \(DebugUG\)](#)
- folders
 - adding to project [30 \(CmdRef\)](#)
- folders for project files [575 \(CmdRef\)](#)
- `force_async_genclk_conv`
 - example [863 \(UG\)](#)
- `foreach_in_collection` command [286 \(CmdRef\)](#)
- forgotten assignment to next state, detecting (VHDL) [363 \(HDLRef\)](#)
- for-loop statement [317 \(HDLRef\)](#)
- forward annotation
 - frequency constraints [1763 \(Ref\)](#)
 - frequency constraints in Xilinx [2102 \(Ref\)](#)
 - initial values [1539 \(Ref\)](#)
- Forward Annotation of Initial Values Verilog [1539 \(Ref\)](#)
- Forward command [417 \(CmdRef\)](#)
- forward-annotation
 - compile point constraints [604 \(UG\)](#)
 - compile point constraints (Cyclone, Arria) [1877 \(Ref\)](#)
 - constraints [1891 \(Ref\)](#)
 - Intel RAM init values [1539 \(Ref\)](#)
 - `ispLEVER` [1890 \(Ref\)](#)
 - Lattice constraints [1890 \(Ref\)](#)
 - Microsemi [2042 \(Ref\)](#)
 - `RLOC` [4165 \(AttrRef\)](#)
 - `RLOC_ORIGIN` [4165 \(AttrRef\)](#)
 - `syn_forward_io_constraints` attribute [3653 \(AttrRef\)](#)
 - `xc_props` attribute [4159 \(AttrRef\)](#)
 - Xilinx core files [736 \(UG\)](#)
- foundation library [651 \(UG\)](#)
- FPGA Design Constraints Editor
 - using TCL View [194 \(UG\)](#)
- FPGA Implementation Tools command [601 \(CmdRef\)](#)
- FPGA synthesis tools, environment for Identify [4199 \(DebugUG\)](#)
- FPGA timing constraints [342 \(CmdRef\)](#)
- FPGAs
 - partitioning [1186 \(UG\)](#)
- frequency
 - clocks (Legacy) [234 \(UG\)](#)

cross-clock paths [1433 \(Ref\)](#)
defining for non-clock signals (Legacy) [235 \(UG\)](#)
internal clocks (Legacy) [235 \(UG\)](#)
setting global [104 \(UG\)](#)
Frequency (Mhz) option, Project view [1315 \(Ref\)](#)
from constraints [200 \(UG\)](#)
from points
clocks [336 \(CmdRef\)](#)
multiple [331 \(CmdRef\)](#)
object search order (Timing Analyzer) [535 \(CmdRef\)](#)
objects [330 \(CmdRef\)](#)
timing analyzer [535 \(CmdRef\)](#)
fse file [1414 \(Ref\)](#)
FSM coding style
Verilog [116 \(HDLRef\)](#)
VHDL [359 \(HDLRef\)](#)
FSM Compiler
advantages [562 \(UG\)](#)
enabling [564 \(UG\)](#)
FSM Compiler option, Project view [1316 \(Ref\)](#)
FSM Compiler, enabling and disabling globally
with GUI [1316 \(Ref\)](#), [1959 \(Ref\)](#)
FSM default state assignment (Verilog) [119 \(HDLRef\)](#)
FSM encoding
user-defined [505 \(UG\)](#)
using syn_enum_encoding [505 \(UG\)](#)
FSM encoding file (.fse) [1414 \(Ref\)](#)
FSM Error Correction Using Hamming Distance 3 [950 \(UG\)](#)
FSM Explorer [562 \(UG\)](#)
enabling [1316 \(Ref\)](#)
overview [567 \(UG\)](#)
running [568 \(UG\)](#)
when to use [562 \(UG\)](#)
FSM Explorer command [499 \(CmdRef\)](#)
FSM Explorer option, Project view [1316 \(Ref\)](#)
FSM Table command [418 \(CmdRef\)](#)
FSM toolbar [1302 \(Ref\)](#), [1303 \(Ref\)](#), [30 \(DebugRef\)](#)

FSM view
crossprobing from source file [425 \(UG\)](#)
FSM Viewer [447 \(UG\)](#), [1325 \(Ref\)](#)
crossprobing [429 \(UG\)](#)
popup menu [610 \(CmdRef\)](#)
popup menu commands [610 \(CmdRef\)](#)
fsm.info file [565 \(UG\)](#)
FSMs
See also FSM Compiler, FSM Explorer
attributes and directives [503 \(UG\)](#)
defining in Verilog [501 \(UG\)](#)
defining in VHDL [502 \(UG\)](#)
definition [501 \(UG\)](#)
double-bit errors [915 \(UG\)](#)
Hamming3 [915 \(UG\)](#)
optimizing with FSM Compiler [562 \(UG\)](#), [174 \(CmdRef\)](#)
properties [449 \(UG\)](#)
safe. *See* safe FSMs
single-bit errors [915 \(UG\)](#)
state encodings [448 \(UG\)](#)
syn_encoding attribute [3621 \(AttrRef\)](#)
transition diagram [447 \(UG\)](#)
viewing [447 \(UG\)](#)
FSMs (finite state machines)
See state machines
Full View command [416 \(CmdRef\)](#)
full_case directive [3435 \(AttrRef\)](#)
functions
Verilog constant math [58 \(HDLRef\)](#)
Verilog signed [58 \(HDLRef\)](#)
Verilog unsigned [58 \(HDLRef\)](#)
VHDL 2008 predefined [423 \(HDLRef\)](#)
functions, selected name support (VHDL) [329 \(HDLRef\)](#)

G

gate primitives, Verilog [17 \(HDLRef\)](#)
gated clock conversion
deciphering messages [824 \(UG\)](#)
forcing conversion with asynchronous set/reset [860 \(UG\)](#)
non-intuitive messages [824 \(UG\)](#)
gated clocks
attributes for black boxes [850 \(UG\)](#)
conversion example [809 \(UG\)](#)
conversion requirements [809 \(UG\)](#)

defining (Legacy) [240 \(UG\)](#)
error messages [821 \(UG\)](#)
examples [807 \(UG\)](#)
procedure for fixing [816 \(UG\)](#)
restrictions [855 \(UG\)](#)
syn_force_seq_prim directive [3649 \(AttrRef\)](#)
gated clocks (Lattice iCE60/iCE40) [1960 \(Ref\)](#)
gated clocks (Xilinx) [2141 \(Ref\)](#)
gated-clock conversion [480 \(CmdRef\)](#), [481 \(CmdRef\)](#)
 excluding elements [830 \(UG\)](#)
gate-level TMR [871 \(UG\)](#)
Gate-Level TMR Examples [878 \(UG\)](#)
GCC & Prototyping Tools panel [481 \(CmdRef\)](#)
generate statement
 VHDL [397 \(HDLRef\)](#)
generate_instance_constraints Tcl command [84 \(CmdRef\)](#)
generated clocks (Intel) [2141 \(Ref\)](#)
generated clocks (Lattice) [1961 \(Ref\)](#)
Generated Clocks panel
 using SCOPE [188 \(UG\)](#)
Generated Clocks panel, SCOPE [301 \(CmdRef\)](#)
generated-clock conversion [859 \(UG\)](#)
generated-clock optimization [480 \(CmdRef\)](#), [481 \(CmdRef\)](#)
generating [511 \(UG\)](#)
generic technology library [1410 \(Ref\)](#)
generics
 extracting from VHDL source code [113 \(UG\)](#)
 passing boolean [62 \(UG\)](#)
 passing integer [63 \(UG\)](#)
 VHDL 2008 packages [428 \(HDLRef\)](#)
get_env Tcl command [87 \(CmdRef\)](#)
get_object_name command [288 \(CmdRef\)](#)
get_option Tcl command [87 \(CmdRef\)](#)
get_prop
 design get_prop [60 \(CmdRef\)](#)
get_prop TCL command [247 \(CmdRef\)](#)
global attributes summary [3384 \(AttrRef\)](#)
global buffer promotion
 iCE40 [1930 \(Ref\)](#)
global buffers [4137 \(AttrRef\)](#)
 defining [3673 \(AttrRef\)](#)
 xc_global_buffers attribute [4137 \(AttrRef\)](#)
global comments
 initializing Xilinx RAM [2113 \(Ref\)](#)
global optimization options [102 \(UG\)](#)
global sets/resets
 Xilinx designs [2105 \(Ref\)](#)
Go to Location command [1047 \(UG\)](#)
 adding markers [1049 \(UG\)](#)
Go to SolvNet command [601 \(CmdRef\)](#)
Goto command [403 \(CmdRef\)](#)
Goto Net Driver command
 current level [545 \(CmdRef\)](#)
 hierarchical [545 \(CmdRef\)](#)
graphical user interface (GUI), overview
 [1255 \(Ref\)](#), [7 \(DebugRef\)](#)
grey box
 netlist file [677 \(UG\)](#)
grey box flow
 MegaCore with greybox netlist [677 \(UG\)](#)
grey boxes
 using [1862 \(Ref\)](#)
greybox flow
 MegaCore with IP package [681 \(UG\)](#)
 NIOS II cores [685 \(UG\)](#)
 SOPC cores [685 \(UG\)](#)
GSR resource (Lattice) [1933 \(Ref\)](#)
GSR resources [1974 \(Ref\)](#)
GSR, Xilinx [2104 \(Ref\)](#)
GTECH library. *See* generic technology library
gtech.v library [1410 \(Ref\)](#)
GUI
 clearing [25 \(DebugRef\)](#)
gui
 synthesis software [1248 \(Ref\)](#)
GUI (graphical user interface), overview
 [1255 \(Ref\)](#), [7 \(DebugRef\)](#)

H

Hamming 3 Encoding

- double-bit errors [915 \(UG\)](#)
- recovery [915 \(UG\)](#)
- Hamming Distance 3 [915 \(UG\)](#)
- haps command [37 \(DebugRef\)](#)
- HAPS technology selection [100 \(UG\)](#)
- HardCopy
 - companion parts [1838 \(Ref\)](#)
- HDL Analyst
 - See also RTL view, Technology view
 - critical paths [455 \(UG\)](#)
 - crossprobing [356 \(UG\)](#), [423 \(UG\)](#)
 - filtering schematics [369 \(UG\)](#), [434 \(UG\)](#)
 - Find command [407 \(CmdRef\)](#)
 - Push/Pop mode [404 \(UG\)](#), [407 \(UG\)](#)
 - traversing hierarchy with mouse strokes [402 \(UG\)](#)
 - traversing hierarchy with Push/Pop mode [341 \(UG\)](#), [404 \(UG\)](#)
 - using [364 \(UG\)](#), [430 \(UG\)](#)
 - Visual Properties [417 \(CmdRef\)](#)
- HDL Analyst menu [542 \(CmdRef\)](#), [691 \(CmdRef\)](#)
 - Current Level submenu [545 \(CmdRef\)](#)
 - Hierarchical submenu [544 \(CmdRef\)](#)
 - Physical Analyst submenu [691 \(CmdRef\)](#)
 - RTL submenu [543 \(CmdRef\)](#)
 - Select All Schematic submenu [553 \(CmdRef\)](#)
 - Select All Sheet submenu [553 \(CmdRef\)](#)
 - Technology submenu [543 \(CmdRef\)](#)
- HDL Analyst Options command [569 \(CmdRef\)](#)
- HDL Analyst tool [1319 \(Ref\)](#)
 - accessing commands [1328 \(Ref\)](#)
 - analyzing critical paths [1361 \(Ref\)](#)
 - Clock Tree [1324 \(Ref\)](#)
 - crossprobing [1341 \(Ref\)](#)
 - deselecting objects [328 \(UG\)](#), [395 \(UG\)](#)
 - displaying timing information [549 \(CmdRef\)](#)
 - filtering designs [1355 \(Ref\)](#)
 - finding objects [1339 \(Ref\)](#)
 - hierarchical instances. See hierarchical instances
 - object information [1330 \(Ref\)](#)
 - preferences [1344 \(Ref\)](#)
 - push/pop mode [1347 \(Ref\)](#)
 - ROM table viewer [1550 \(Ref\)](#)
 - schematic sheet size [1344 \(Ref\)](#)
 - schematics, filtering [1355 \(Ref\)](#)
 - schematics, multiple-sheet [1344 \(Ref\)](#)
 - selecting/deselecting objects [327 \(UG\)](#), [395 \(UG\)](#)
 - status bar information [1330 \(Ref\)](#)
 - Synplify license [1319 \(Ref\)](#)
 - title bar information [1344 \(Ref\)](#)
- HDL Analyst toolbar
 - See Analyst toolbar
- HDL Analyst views [1320 \(Ref\)](#)
 - highlighting collections [221 \(UG\)](#)
 - See also RTL view, Technology view
- HDL files
 - searching [61 \(DebugRef\)](#)
- HDL files, creating [1299 \(Ref\)](#)
- HDL parameter overrides [89 \(CmdRef\)](#)
- HDL views, annotating timing information [453 \(UG\)](#)
- hdl_define Tcl command [88 \(CmdRef\)](#)
- hdl_param Tcl command [89 \(CmdRef\)](#)
- header, timing report [1428 \(Ref\)](#)
- help
 - online
 - accessing [1252 \(Ref\)](#)
- Help command [602 \(CmdRef\)](#), [59 \(DebugRef\)](#)
- help command [37 \(DebugRef\)](#)
- Help menu [602 \(CmdRef\)](#), [59 \(DebugRef\)](#)
- hidden hierarchical instances [1335 \(Ref\)](#)
 - are not flattened [1359 \(Ref\)](#)
- hidden instances
 - consequences of saving [432 \(UG\)](#)
 - flattening [443 \(UG\)](#)
 - restricting search by hiding [411 \(UG\)](#)
 - specifying [432 \(UG\)](#)
 - status in other views [432 \(UG\)](#)
- Hide command
 - floating toolbar popup menu [1298 \(Ref\)](#)
 - Log Watch window popup menu [1277 \(Ref\)](#)
 - Tcl Window popup menu [1280 \(Ref\)](#)
 - View menu, Rats Nest submenu [662 \(CmdRef\)](#)
- Hide Instances command [550 \(CmdRef\)](#)
- hiding instances [550 \(CmdRef\)](#)
- hierarchical area report [1437 \(Ref\)](#)
 - .areasrr file [1437 \(Ref\)](#)

Hierarchical Critical Path command [543 \(CmdRef\)](#)

hierarchical design

- expanding logic from nets [437 \(UG\)](#)
- expanding logic from pins [371 \(UG\)](#), [436 \(UG\)](#)

hierarchical design, creating

- Verilog [126 \(HDLRef\)](#)
- VHDL [365 \(HDLRef\)](#)

hierarchical designs

- using include files [128 \(HDLRef\)](#)

hierarchical instances [1333 \(Ref\)](#)

- compared with primitive [1332 \(Ref\)](#)
- display in HDL Analyst [1333 \(Ref\)](#)
- dissolving [381 \(UG\)](#), [444 \(UG\)](#)
- hidden [1335 \(Ref\)](#)
- hiding. *See* hidden instances, Hide Instances command
- multiple sheets for internal logic [433 \(UG\)](#)
- opaque [1333 \(Ref\)](#)
- pin name display [435 \(UG\)](#)
- transparent [1333 \(Ref\)](#)
- viewing internal logic [367 \(UG\)](#), [432 \(UG\)](#)

hierarchical objects

- pushing into with mouse stroke [341 \(UG\)](#), [403 \(UG\)](#)
- traversing with Push/Pop mode [341 \(UG\)](#), [404 \(UG\)](#)

hierarchical project management and compile points [22 \(UG\)](#)

hierarchical project management flows

- bottom-up development flow [24 \(UG\)](#)
- bottom-up synthesis flow [27 \(UG\)](#)
- mixed block synthesis flow [31 \(UG\)](#)
- top-down development flow [25 \(UG\)](#)
- top-down synthesis flow [29 \(UG\)](#)

hierarchical project management views [1260 \(Ref\)](#)

hierarchical projects [22 \(UG\)](#)

- analyzing [160 \(UG\)](#)
- configuring for synthesis [156 \(UG\)](#)
- instance-based synthesis [130 \(UG\)](#)
- multiple implementations [145 \(UG\)](#)
- synthesis options [156 \(UG\)](#)

hierarchical schematic sheet, definition [1344 \(Ref\)](#)

hierarchical search [411 \(UG\)](#)

Hierarchical View command [543 \(CmdRef\)](#)

hierarchy

- flattening [381 \(UG\)](#), [441 \(UG\)](#), [546 \(CmdRef\)](#)
 - compared with filtering [1359 \(Ref\)](#)
- flattening with syn_hier [3681 \(AttrRef\)](#)
- folded [4223 \(DebugUG\)](#)
- preserving for Xilinx Place and Route [4181 \(AttrRef\)](#)
- pushing and popping [1347 \(Ref\)](#)
- schematic sheets [1344 \(Ref\)](#)
- traversing [337 \(UG\)](#), [401 \(UG\)](#)
- Verilog [126 \(HDLRef\)](#)

hierarchy (VHDL) [365 \(HDLRef\)](#)

Hierarchy Browser [345 \(UG\)](#), [1351 \(Ref\)](#)

- changing size in view [1320 \(Ref\)](#)
- Clock Tree [1324 \(Ref\)](#)
- commands [641 \(CmdRef\)](#)
- finding schematic objects [1339 \(Ref\)](#)
- moving between objects [1324 \(Ref\)](#)
- popup menu [641 \(CmdRef\)](#)
- refreshing [641 \(CmdRef\)](#)
- RTL view [1320 \(Ref\)](#)
- symbols (legend) [1325 \(Ref\)](#)
- Technology view [1322 \(Ref\)](#)
- trees of objects [1324 \(Ref\)](#)

hierarchy browser

- clock trees [455 \(UG\)](#)
- controlling display [398 \(UG\)](#)
- crossprobing from [356 \(UG\)](#), [423 \(UG\)](#)
- defined [337 \(UG\)](#), [401 \(UG\)](#)
- enabling/disabling display [591 \(CmdRef\)](#)
- finding objects [345 \(UG\)](#), [409 \(UG\)](#)
- popup menu [8 \(DebugRef\)](#)
- traversing hierarchy [401 \(UG\)](#)

hierarchy command [38 \(DebugRef\)](#)

hierarchy management (custom folders) [91 \(UG\)](#)

hierarchy separator [389 \(CmdRef\)](#), [14 \(DebugRef\)](#)

high reliability

- distributed TMR [871 \(UG\)](#)
- ECC RAM [922 \(UG\)](#), [949 \(UG\)](#)
- FSMs with Hamming3 [915 \(UG\)](#)
- local TMR [921 \(UG\)](#)
- safe FSMs [908 \(UG\)](#)
- syn_radhardlevel [3857 \(AttrRef\)](#)
- using safe FSM [908 \(UG\)](#)
- using TMR [871 \(UG\)](#)

high reliability design [865 \(UG\)](#)
High reliability functions [890 \(UG\)](#)
High Reliability panel
Implementation Options dialog box [456 \(CmdRef\)](#)
Highlight Visible Net Instances
command [1063 \(UG\)](#)
HighRel
Gate Level TMR Examples [878 \(UG\)](#)
How to Use Help command [602 \(CmdRef\)](#), [59 \(DebugRef\)](#)
hyper source
example [657 \(UG\)](#)
for IPs [660 \(UG\)](#)
for prototyping [656 \(UG\)](#)
IP design hierarchy [656 \(UG\)](#)
threading signals [656 \(UG\)](#)

I

I/O buffers
inserting [3713 \(AttrRef\)](#)
specifying I/O standards [3821 \(AttrRef\)](#)
I/O constraints
multiple on same port [308 \(CmdRef\)](#)
I/O insertion [560 \(UG\)](#), [1749 \(Ref\)](#), [1973 \(Ref\)](#)
Arria [1844 \(Ref\)](#)
Intel Cyclone [1844 \(Ref\)](#)
Intel Stratix [1844 \(Ref\)](#)
VHDL manual (Xilinx) [2127 \(Ref\)](#)
I/O insertion (Intel) [1838 \(Ref\)](#)
I/O insertion (Microsemi) [2030 \(Ref\)](#)
I/O insertion (Xilinx) [2089 \(Ref\)](#)
I/O locations
assigning automatically (Xilinx) [2122 \(Ref\)](#)
manually assigning (Xilinx) [2127 \(Ref\)](#)
I/O packing
disabling with syn_replicate [3919 \(AttrRef\)](#)
I/O pads
instantiating (Xilinx) [2089 \(Ref\)](#)
specifying I/O standards [193 \(UG\)](#)
I/O paths
false path constraint [204 \(UG\)](#)
I/O registers, power-up mode (Intel) [3405 \(AttrRef\)](#)
I/O standards
QSF constraints [1383 \(Ref\)](#)
specifying [193 \(UG\)](#)
I/O Standards panel
using SCOPE [189 \(UG\)](#)
I/O Standards panel, SCOPE [314 \(CmdRef\)](#)
I/Os
See also ports
auto-constraining [471 \(UG\)](#)
constraining [192 \(UG\)](#)
constraining (Legacy) [241 \(UG\)](#)
inferring Xilinx buffers with syn_diff_io [3545 \(AttrRef\)](#)
packing in Intel designs [1865 \(Ref\)](#)
packing in Xilinx designs [2119 \(Ref\)](#)
preserving [561 \(UG\)](#), [1974 \(Ref\)](#)
specifying pad type (Xilinx) [2133 \(Ref\)](#)
Verilog black boxes [492 \(UG\)](#)
VHDL black boxes [494 \(UG\)](#)
I/Os (Design Planner)
critical paths from pin-locked I/Os [999 \(UG\)](#)
IBUFDS
inference [2129 \(Ref\)](#)
IBUFGDS
inference [2129 \(Ref\)](#)
iCE65 Lattice device options [1952 \(Ref\)](#)
ICG
stability latch removal [838 \(UG\)](#)
idc file
editing [4214 \(DebugUG\)](#)
idcode command [43 \(DebugRef\)](#)
identification register [4279 \(DebugUG\)](#)
Identify
compile points [1145 \(UG\)](#)
Identify debug
TMR instrumentation [940 \(UG\)](#)
Identify Debugger [935 \(UG\)](#)
Identify Instrumentor
launching [1305 \(Ref\)](#)
IEEE 1364 Verilog 95 standard [1408 \(Ref\)](#)
IEEE 1735
encrypting multiple files [643 \(UG\)](#)

IEEE 1801-2009. *See* UPF

ieee library (VHDL) [301 \(HDLRef\)](#)

if-then-else statement (VHDL) [314 \(HDLRef\)](#)

ignored language constructs (Verilog) [15 \(HDLRef\)](#)

ignored language constructs (VHDL) [286 \(HDLRef\)](#)

IICE

- arming [59 \(DebugRef\)](#)
- buffer type [4244 \(DebugUG\)](#)
- communicating with [25 \(DebugRef\)](#)
- cross triggering [4304 \(DebugUG\)](#), [76 \(DebugRef\)](#)
- JTAG connection [4269 \(DebugUG\)](#)
- selecting multiple [45 \(DebugRef\)](#)

iice command [45 \(DebugRef\)](#)

IICE Controller tab [22 \(DebugRef\)](#), [28 \(DebugRef\)](#)

IICE parameters

- buffer type [20 \(DebugRef\)](#)
- individual [4312 \(DebugUG\)](#)

IICE Sampler tab [19 \(DebugRef\)](#)

IICE settings

- sample clock [21 \(DebugRef\)](#)
- sample depth [20 \(DebugRef\)](#)

IICE units

- cross triggering [4242 \(DebugUG\)](#), [4306 \(DebugUG\)](#)

impl Tcl command [93 \(CmdRef\)](#)

Implementation Directory [1271 \(Ref\)](#)

Implementation Maps

- Physical Analyst [1066 \(UG\)](#)

implementation options [99 \(UG\)](#)

- design plan file [106 \(UG\)](#)
- device [99 \(UG\)](#)
- global frequency [104 \(UG\)](#)
- global optimization [102 \(UG\)](#)
- Options Panel [447 \(CmdRef\)](#)
- part selection [99 \(UG\)](#)
- specifying results [107 \(UG\)](#)

Implementation Options command [423 \(CmdRef\)](#), [444 \(CmdRef\)](#)

Implementation Options dialog box [430 \(CmdRef\)](#), [444 \(CmdRef\)](#)

- Constraints panel [450 \(CmdRef\)](#)
- Design Planning panel [665 \(CmdRef\)](#)
- Device panel [445 \(CmdRef\)](#)
- High Reliability panel [456 \(CmdRef\)](#)
- Netlist Restructure panel [665 \(CmdRef\)](#)
- Options panel [447 \(CmdRef\)](#)
- Place and Route panel [483 \(CmdRef\)](#)
- Timing Report panel [455 \(CmdRef\)](#)
- Verilog panel [462 \(CmdRef\)](#)
- VHDL panel [458 \(CmdRef\)](#)

implementation options, device

- partdata tcl command [105 \(CmdRef\)](#)

Implementation Results [1271 \(Ref\)](#)

Implementation Results panel

- Options for implementation dialog box [453 \(CmdRef\)](#)

implementations

- copying [98 \(UG\)](#)
- creating [424 \(CmdRef\)](#)
- deleting [98 \(UG\)](#)
- multiple. *See* multiple implementations.
- naming [615 \(CmdRef\)](#)
- overwriting [98 \(UG\)](#)
- renaming [98 \(UG\)](#)

Import IP

- commands [485 \(CmdRef\)](#)

Import IP menu [485 \(CmdRef\)](#)

Import IP Package command [496 \(CmdRef\)](#)

Import Xilinx ISE Project command [489 \(CmdRef\)](#)

importing projects [57 \(DebugRef\)](#)

include command

- verilog library directories [466 \(CmdRef\)](#)

include files [26 \(CmdRef\)](#)

- hierarchical designs [128 \(HDLRef\)](#)

Incremental Compiler

- using [64 \(UG\)](#)

incremental flows

- Quartus Fast Fit [1088 \(UG\)](#)
- SmartGuide [1117 \(UG\)](#)
- Vivado [1107 \(UG\)](#)
- Xilinx partition [1120 \(UG\)](#)
- Xilinx partition (before ISE 12.1) [1125 \(UG\)](#)

incremental implementations [54 \(DebugRef\)](#)

Incremental Mode option

- using Incremental Compiler [64 \(UG\)](#)

incremental synthesis
 compile points [623 \(UG\)](#)
 locked,partition compile points [592 \(UG\)](#)
 other tools [626 \(UG\)](#)

indenting a block of text [1286 \(Ref\)](#)

indenting text (Text Editor) [1286 \(Ref\)](#)

index_collection command [288 \(CmdRef\)](#)

inference
 BUFGMUX/BUFGMUX_1 [2128 \(Ref\)](#)
 Xilinx BUFGMUX/BUFGMUX_1 [2090 \(Ref\)](#), [2128 \(Ref\)](#)
 Xilinx I/O buffers [2089 \(Ref\)](#), [2128 \(Ref\)](#)

inferencing
 DSP blocks [1987 \(Ref\)](#)

inferred clock [1429 \(Ref\)](#)

info file (design component info) [1414 \(Ref\)](#)

ini file [1405 \(Ref\)](#)

INIT property
 initializing Xilinx RAMs, Verilog [2112 \(Ref\)](#)
 initializing Xilinx RAMs, VHDL [2115 \(Ref\)](#)
 specifying with attributes [2116 \(Ref\)](#)

INIT values
 syntax for forward-annotation [4164 \(AttrRef\)](#)
 Xilinx registers [2117 \(Ref\)](#)

init values
 in RAMs [337 \(HDLRef\)](#)

initial value data file
 Verilog [1536 \(Ref\)](#)

Initial Values
 forward annotation [1539 \(Ref\)](#)

initial values
 \$readmemb [1533 \(Ref\)](#)
 \$readmemh [1533 \(Ref\)](#)
 Achronix [1717 \(Ref\)](#)
 Lattice ICE65/iCE40 [1906 \(Ref\)](#)
 on primitives [514 \(UG\)](#)
 registers (Verilog) [90 \(HDLRef\)](#)
 Verilog [90 \(HDLRef\)](#)

initial values (Verilog)
 netlist file (.srs) [1539 \(Ref\)](#)

initialization file (.ini) [1405 \(Ref\)](#)

initializing [506 \(UG\)](#)

initializing RAM [506 \(UG\)](#)

Input and output constraints
 defining [192 \(UG\)](#)

input constraints, setting [192 \(UG\)](#)

input constraints, setting (Legacy) [240 \(UG\)](#)

input files [1404 \(Ref\)](#)
 .adc [1404 \(Ref\)](#)
 .ini [1405 \(Ref\)](#)
 .nrf [1405 \(Ref\)](#)
 .opt [1405 \(Ref\)](#), [1415 \(Ref\)](#)
 .sdc [1405 \(Ref\)](#)
 .sfp [1406 \(Ref\)](#)
 .sv [1407 \(Ref\)](#)
 .v [1406 \(Ref\)](#), [1407 \(Ref\)](#)
 .vhd [1407 \(Ref\)](#)

Inputs/Outputs panel
 using SCOPE [189 \(UG\)](#)

Inputs/Outputs panel, SCOPE [306 \(CmdRef\)](#)

Insert Sub-project command [442 \(CmdRef\)](#), [636 \(CmdRef\)](#)

inserting
 bookmarks (Text Editor) [1286 \(Ref\)](#)
 level-sensitive latches in design,
 warning [102 \(HDLRef\)](#), [340 \(HDLRef\)](#)

Instance Hierarchy tab [348 \(UG\)](#)

Instance Properties command
 (hierarchical project
 management) [634 \(CmdRef\)](#)

instance-based subproject
 compared to block-based [126 \(UG\)](#)

instance-based synthesis
 hierarchical projects [130 \(UG\)](#)

instances
 controlling optimization [4095 \(AttrRef\)](#)
 dissolving [551 \(CmdRef\)](#)
 expanding paths between [544 \(CmdRef\)](#)
 expansion maximum limit [592 \(CmdRef\)](#)
 expansion maximum limit (per filtered
 sheet) [595 \(CmdRef\)](#)
 expansion maximum limit (per
 unfiltered sheet) [595 \(CmdRef\)](#)
 finding by name [402 \(CmdRef\)](#), [686 \(CmdRef\)](#)
 hiding and unhiding [550 \(CmdRef\)](#)
 hierarchical
 dissolving [1352 \(Ref\)](#)
 making transparent [1352 \(Ref\)](#)

hierarchical. *See* hierarchical instances
isolating paths through [550 \(CmdRef\)](#)
making transparent [551 \(CmdRef\)](#)
name display [590 \(CmdRef\)](#)
preserving with `syn_noprune` [549 \(UG\)](#), [3803 \(AttrRef\)](#)
primitive. *See* primitive instances
properties [320 \(UG\)](#), [390 \(UG\)](#)
properties (Physical Analyst) [697 \(CmdRef\)](#)
properties of pins [390 \(UG\)](#)
selecting all in schematic [553 \(CmdRef\)](#)
instances (Physical Analyst) [1688 \(Ref\)](#)
 adding markers [1048 \(UG\)](#)
 displaying instances [1029 \(UG\)](#)
Instances command
 schematic selection [553 \(CmdRef\)](#)
 sheet selection [553 \(CmdRef\)](#)
instantiating black boxes (Verilog) [124 \(HDLRef\)](#)
instantiating black boxes (VHDL) [399 \(HDLRef\)](#)
instantiating components (VHDL) [304 \(HDLRef\)](#), [326 \(HDLRef\)](#)
instantiating gate primitives, Verilog [17 \(HDLRef\)](#)
instantiation templates [75 \(UG\)](#)
instrumentation
 description [4198 \(DebugUG\)](#)
 partial records [4221 \(DebugUG\)](#)
 post-compile [4214 \(DebugUG\)](#)
instrumentation command [54 \(DebugRef\)](#)
instrumentation directory [4232 \(DebugUG\)](#)
instrumenting partial buses [4218 \(DebugUG\)](#)
instrumentor
 launching [4211 \(DebugUG\)](#)
 running after compilation [4214 \(DebugUG\)](#)
integer data type (VHDL) [289 \(HDLRef\)](#)
Integrated Clock Gating (ICG)
 stability latch removal [838 \(UG\)](#)
integrated P&R [1081 \(UG\)](#)
 custom shell script [1081 \(UG\)](#)
Intel
 asymmetric RAM [1782 \(Ref\)](#)
 attributes [1882 \(Ref\)](#)
Clearbox. *See* Clearbox
clicking. *See* clicking.
constraints [1876 \(Ref\)](#)
device support [1770 \(Ref\)](#)
device support. *See also* Intel technologies [1770 \(Ref\)](#)
directives [1882 \(Ref\)](#)
DSP block inference [1789 \(Ref\)](#)
edif and vqm filenames [1880 \(Ref\)](#)
fanout limits [1839 \(Ref\)](#)
forward annotation [1772 \(Ref\)](#)
forward-annotation, Max+Plus II [1876 \(Ref\)](#)
grey boxes *See* grey boxes
I/O packing [1865 \(Ref\)](#)
I/O registers power-up mode [3405 \(AttrRef\)](#)
inferring LUTRAMs [1474 \(Ref\)](#)
instantiating LPMs as black boxes [522 \(UG\)](#)
IP core support [1774 \(Ref\)](#)
launching MegaWizard [497 \(CmdRef\)](#)
LPM megafunction example (Verilog) [522 \(UG\)](#)
LPM megafunction example (VHDL) [524 \(UG\)](#)
LUTRAMs [1476 \(Ref\)](#)
macro library, Verilog [1774 \(Ref\)](#)
macro library, VHDL [1774 \(Ref\)](#)
macros [1776 \(Ref\)](#)
mapping to ATOMs [1777 \(Ref\)](#)
Max+Plus II forward-annotated constraints [1876 \(Ref\)](#)
P&R file for untranslated settings [699 \(UG\)](#)
packing I/Os [1865 \(Ref\)](#)
pad cell insertion [1779 \(Ref\)](#)
PLLs [1778 \(Ref\)](#)
PLLs. *See* altplls
prepared components method [1816 \(Ref\)](#)
Quartus batch mode [1086 \(UG\)](#)
Quartus integrated flow [1084 \(UG\)](#)
Quartus interactive flow [1085 \(UG\)](#)
RAM inference [1780 \(Ref\)](#)
RAM with control signals [1481 \(Ref\)](#)
RAMs
 inference (Stratix) [1780 \(Ref\)](#)
register inference [1778 \(Ref\)](#)
reports [1871 \(Ref\)](#)
ROM inference [1787 \(Ref\)](#)
shift registers [515 \(UG\)](#)
simulating LPMs [1868 \(Ref\)](#)

SOPC Builder [1380 \(Ref\)](#)
specifying VHDL library [1774 \(Ref\)](#)
syn_useioff attribute [4079 \(AttrRef\)](#)
technology keywords [1858 \(Ref\)](#)
translating PIN file to constraint file [504 \(CmdRef\)](#)
Verilog LPM library [528 \(UG\)](#)
Intel backannotation [1127 \(UG\)](#)
Intel black boxes
pad cell insertion (Intel) [1779 \(Ref\)](#)
Intel Clearbox
megafunctions [1860 \(Ref\)](#)
Intel device options
Arria [1843 \(Ref\)](#)
Cyclone [1843 \(Ref\)](#)
MAX [1850 \(Ref\)](#)
MAX II [1847 \(Ref\)](#)
Stratix [1843 \(Ref\)](#)
Intel file format options
MAX [1853 \(Ref\)](#)
Intel incremental flows [1087 \(UG\)](#)
Intel Mapper
new [1859 \(Ref\)](#)
Intel megafunctions
DSP blocks [1789 \(Ref\)](#)
Intel MegaWizard
generating LPM files [522 \(UG\)](#)
Intel models
Clearbox [180 \(CmdRef\)](#)
set_option syntax [180 \(CmdRef\)](#)
Intel New Mapper
using [1859 \(Ref\)](#)
Intel Quartus [709 \(UG\)](#)
Intel RAM
byte-wide write enable [1782 \(Ref\)](#)
Intel RAMs
\$readmemb/\$readmemh initialization
[1539 \(Ref\)](#)
inference (Arria) [1780 \(Ref\)](#)
inference (Cyclone) [1780 \(Ref\)](#)
Intel shift registers
report [517 \(UG\)](#)
Intel STRATIX (Design Planner)
additional tips [1002 \(UG\)](#)
Intel technologies
MAX [1850 \(Ref\)](#)

Interactive Attribute Examples [1290 \(Ref\)](#)
interface construct [155 \(HDLRef\)](#), [253 \(HDLRef\)](#)
interface information, timing report [1434 \(Ref\)](#)
ILM See interface logic models
interface logic models [596 \(UG\)](#)
interface timing [597 \(UG\)](#)
IOBUFDS
inference [2129 \(Ref\)](#)
IP
encryption-decryption flow [629 \(UG\)](#)
importing from SOPC Builder [686 \(UG\)](#)
license queuing [757 \(UG\)](#)
license queuing syntax [211 \(CmdRef\)](#)
re-encryption [634 \(UG\)](#)
Vivado [718 \(UG\)](#)
IP core areas (Design Planner) [995 \(UG\)](#)
IP core wizard [500 \(CmdRef\)](#)
IP cores [2108 \(Ref\)](#)
Vivado [1097 \(UG\)](#)
IP cores (SYNCore)
building ram models [508 \(CmdRef\)](#)
IP design hierarchy
hyper source [656 \(UG\)](#)
IP encryption
IEEE 1735 [640 \(UG\)](#)
Lattice [1966 \(Ref\)](#)
IP encryption (Lattice) [1966 \(Ref\)](#)
IP encryption flow overview [628 \(UG\)](#)
IP encryption scheme [634 \(UG\)](#)
IP license queuing [757 \(UG\)](#)
IP vendors
directory structure for package [636 \(UG\)](#)
encrypting IP [634 \(UG\)](#)
package file list for encrypted IP flow
[636 \(UG\)](#)
packaging for evaluation [635 \(UG\)](#)
supplying vendor information [637 \(UG\)](#)
IPs
encrypting [634 \(UG\)](#)
encryption flow [628 \(UG\)](#)
Intel [662 \(UG\)](#)
SYNCore byte-enable RAMs [1610 \(Ref\)](#)
SYNCore counters [1665 \(Ref\)](#)

SYNCore FIFOs [1557 \(Ref\)](#)
SYNCore RAMs [1587 \(Ref\)](#)
SYNCore ROMs [1627 \(Ref\)](#)
SYNCore subtractors [1641 \(Ref\)](#)
 using hyper source for debug [660 \(UG\)](#)
is_error_blackbox property [301 \(UG\)](#)
ise2syn
 description [739 \(UG\)](#)
 relationship with ucf2sdc [739 \(UG\)](#)
ise2syn utility
 converting Xilinx projects [739 \(UG\)](#)
 GUI command [489 \(CmdRef\)](#)
 Tcl syntax [95 \(CmdRef\)](#)
 using [739 \(UG\)](#)
Isolate Paths command [550 \(CmdRef\)](#)
 different from Expand Paths [440 \(UG\)](#), [441 \(UG\)](#)
isolating paths from pins or ports [1363 \(Ref\)](#)
isolation power strategy [1206 \(UG\)](#)
ispLEVER
 forward-annotating constraints for [1891 \(Ref\)](#)
iterations
 reducing with compile on error [298 \(UG\)](#)

J

job management
 up-to-date checking [262 \(UG\)](#)
Job Status command [501 \(CmdRef\)](#), [505 \(CmdRef\)](#)
job tcl command [96 \(CmdRef\)](#)
JTAG
 chain tests [4280 \(DebugUG\)](#)
 communication block [4269 \(DebugUG\)](#)
 communication test [4278 \(DebugUG\)](#)
 debugging [4266 \(DebugUG\)](#), [4278 \(DebugUG\)](#)
 direct connection [4271 \(DebugUG\)](#)
 serial connection [4272 \(DebugUG\)](#)
JTAG chain
 settings [4280 \(DebugUG\)](#), [48 \(DebugRef\)](#)
JTAG chains [22 \(DebugRef\)](#)
JTAG registers [4272 \(DebugUG\)](#)
jtag_server command [62 \(DebugRef\)](#)

JTAGTech3710 cable settings [44 \(DebugRef\)](#)

K

key assignments
 customizing [773 \(UG\)](#)
key block [631 \(UG\)](#)
keyboard shortcuts [1306 \(Ref\)](#), [681 \(CmdRef\)](#), [684 \(CmdRef\)](#), [30 \(DebugRef\)](#)
 arrow keys (Hierarchy Browser) [1351 \(Ref\)](#)
keyword completion, Text Editor [1286 \(Ref\)](#)
keywords
 all (VHDL 2008) [441 \(HDLRef\)](#)
 completing in Text Editor [1286 \(Ref\)](#)
 completing words in Text Editor [51 \(UG\)](#)
 SystemVerilog [282 \(HDLRef\)](#)

L

labels, displaying [590 \(CmdRef\)](#)
language
 guidelines (Verilog) [89 \(HDLRef\)](#)
language constructs (Verilog) [14 \(HDLRef\)](#)
language constructs (VHDL) [284 \(HDLRef\)](#), [286 \(HDLRef\)](#)
language guidelines (VHDL) [340 \(HDLRef\)](#)
last_run.adb file [4299 \(DebugUG\)](#)
latches
 always blocks (Verilog) [108 \(HDLRef\)](#)
 concurrent signal assignment (VHDL) [347 \(HDLRef\)](#)
 continuous assignments (Verilog) [108 \(HDLRef\)](#)
 error message (VHDL) [350 \(HDLRef\)](#)
 in timing analysis [1361 \(Ref\)](#)
 level-sensitive
 Verilog [108 \(HDLRef\)](#)
 mapping (Xilinx) [2088 \(Ref\)](#)
 process blocks (VHDL) [348 \(HDLRef\)](#)
 SystemVerilog always_latch [225 \(HDLRef\)](#)
Lattice
 attributes and directives [1976 \(Ref\)](#)
 black boxes [1905 \(Ref\)](#), [1925 \(Ref\)](#)

Block RAM Support [1894 \(Ref\)](#)
 disable I/O insertion [1933 \(Ref\)](#)
 fanin limit [1937 \(Ref\)](#)
 forward annotation [1890 \(Ref\)](#), [1984 \(Ref\)](#), [2058 \(Ref\)](#)
 forward-annotation constraints [1890 \(Ref\)](#)
 generated clocks [1961 \(Ref\)](#)
 GSR resource [1933 \(Ref\)](#)
 I/O insertion [560 \(UG\)](#)
 IP encryption [1966 \(Ref\)](#)
 loc attribute [3439 \(AttrRef\)](#)
 macro libraries [1925 \(Ref\)](#)
 macros [1905 \(Ref\)](#), [1925 \(Ref\)](#)
 map logic to macrocells [1936 \(Ref\)](#)
 maximum cell fanin [1937 \(Ref\)](#)
 maximum terms/macrocell [1937 \(Ref\)](#)
 orca_padtype attribute [3445 \(AttrRef\)](#)
 orca_props attribute [3449 \(AttrRef\)](#)
 pad types (ORCA) [3445 \(AttrRef\)](#)
 percentage of design to optimize for timing [1937 \(Ref\)](#)
 PICs [1966 \(Ref\)](#)
 pipelining [1959 \(Ref\)](#)
 product families [1888 \(Ref\)](#)
 reports [1962 \(Ref\)](#)
 retiming [1960 \(Ref\)](#)
 updating compile points [1934 \(Ref\)](#)

Lattice iCE65/iCE40
 gated clocks [1960 \(Ref\)](#)
 initial values [1906 \(Ref\)](#)

Lattice iCE65/iCE40 options [1953 \(Ref\)](#)

Lattice netlist [1889 \(Ref\)](#)

Lattice options
 LatticeECP2 and LatticeECP/EC [1939 \(Ref\)](#)
 MachXO [1943 \(Ref\)](#)
 ORCA [1937 \(Ref\)](#)

Launch Identify Instrumentor command [506 \(CmdRef\)](#), [507 \(CmdRef\)](#)

Launch Identify Instrumentor icon [1305 \(Ref\)](#)

launch_megawiz command [497 \(CmdRef\)](#)

launch_vivado command [97 \(CmdRef\)](#)

lcell primitive
 Clearbox [666 \(UG\)](#)

LCELLs [1851 \(Ref\)](#)

legacy sdc file. See sdc files, difference between legacy and Synopsys standard

levels
 See hierarchy

level-sensitive latches
 Verilog [108 \(HDLRef\)](#)
 VHDL
 unwanted [350 \(HDLRef\)](#)

level-sensitive latches (VHDL)
 using concurrent signal assignments [347 \(HDLRef\)](#)
 using processes [348 \(HDLRef\)](#)

lib2syn
 using [1411 \(Ref\)](#)

libraries
 general technology [1409 \(Ref\)](#)
 macro, built-in [1407 \(Ref\)](#), [302 \(HDLRef\)](#)
 post-synthesis simulation [1763 \(Ref\)](#)
 technology-independent [1409 \(Ref\)](#)
 Verilog
 macro [124 \(HDLRef\)](#)
 VHDL
 attributes and constraints [1408 \(Ref\)](#), [302 \(HDLRef\)](#)
 IEEE, supported [284 \(HDLRef\)](#)
 Xilinx post-synthesis simulation [2172 \(Ref\)](#)

libraries (VHDL) [300 \(HDLRef\)](#)

library and package rules, VHDL [303 \(HDLRef\)](#)

library extensions [56 \(UG\)](#)

library ieee [4029 \(AttrRef\)](#)

library packages (VHDL), accessing [302 \(HDLRef\)](#)

library statement (VHDL) [303 \(HDLRef\)](#)

library synplify [4029 \(AttrRef\)](#)

license
 floating [602 \(CmdRef\)](#)
 saving [603 \(CmdRef\)](#), [59 \(DebugRef\)](#)
 specifying in batch mode [6 \(UG\)](#), [210 \(CmdRef\)](#)

License Agreement command [602 \(CmdRef\)](#), [59 \(DebugRef\)](#)

license queuing [755 \(UG\)](#), [212 \(CmdRef\)](#)
 blocking-style [755 \(UG\)](#)
 DesignWare IP [757 \(UG\)](#)

- IP [757 \(UG\)](#)
- license release (synthesis)
 - after P&R [1082 \(UG\)](#)
- license_release [1082 \(UG\)](#)
- licenses
 - DesignWare multiprocessing [653 \(UG\)](#)
- Limit Number of Paths [534 \(CmdRef\)](#)
- limitations
 - SystemVerilog [141 \(HDLRef\)](#)
- linkerlog file [1415 \(Ref\)](#)
- Linux, 64-bit mapping [449 \(CmdRef\)](#)
- lists
 - dependent files [143 \(UG\)](#)
- literal
 - bit string [416 \(HDLRef\)](#)
- literals
 - SystemVerilog [145 \(HDLRef\)](#)
- load_upf Tcl command [718 \(CmdRef\)](#)
- loc attribute (Lattice) [3439 \(AttrRef\)](#)
- local TMR [869 \(UG\)](#)
 - RAM [921 \(UG\)](#)
- localparams
 - Verilog 2001 [57 \(HDLRef\)](#)
- location constraints
 - RLOC_ORIGIN [2136 \(Ref\)](#)
 - RLOCs with synthesis attribute [2099 \(Ref\)](#), [2136 \(Ref\)](#)
 - RLOCs with xc_attributes [2134 \(Ref\)](#)
- Log File
 - HTML [420 \(CmdRef\)](#)
 - text [420 \(CmdRef\)](#)
- log file
 - continue on error [300 \(UG\)](#)
 - displaying [416 \(CmdRef\)](#)
 - remote access [273 \(UG\)](#)
 - Tcl commands for filtering [216 \(CmdRef\)](#)
- log file (.srr) [1421 \(Ref\)](#)
 - watching selected information [1276 \(Ref\)](#)
- Log File command
 - View menu [420 \(CmdRef\)](#)
- log file report [1421 \(Ref\)](#)
 - clock buffering [1424 \(Ref\)](#)
 - compiler [1422 \(Ref\)](#)
 - mapper [1423 \(Ref\)](#)
 - net buffering [1424 \(Ref\)](#)
 - resource usage [1425 \(Ref\)](#)
 - retiming [1426 \(Ref\)](#)
 - summary of compile points [1425 \(Ref\)](#)
 - timing [1425 \(Ref\)](#)
- log files
 - checking FSM descriptions [569 \(UG\)](#)
 - checking information [267 \(UG\)](#)
 - crossprobing to Physical Analyst [1054 \(UG\)](#)
 - pipelining description [540 \(UG\)](#)
 - retiming report [544 \(UG\)](#)
 - setting default display [268 \(UG\)](#)
 - shift register report (Intel) [517 \(UG\)](#)
 - state machine descriptions [565 \(UG\)](#)
 - viewing [267 \(UG\)](#)
- Log Watch Configuration dialog box [1278 \(Ref\)](#)
- Log Watch window [1276 \(Ref\)](#)
 - Output Windows [1284 \(Ref\)](#)
 - popup menu [607 \(CmdRef\)](#)
 - positioning commands [1277 \(Ref\)](#)
- Log Watch Window command [416 \(CmdRef\)](#)
- log_filter Tcl command
 - syntax [98 \(CmdRef\)](#)
- log_report Tcl command [100 \(CmdRef\)](#)
- logic
 - expanding between objects [440 \(UG\)](#)
 - expanding from net [373 \(UG\)](#), [437 \(UG\)](#)
 - expanding from net (Physical Analyst) [1063 \(UG\)](#)
 - expanding from pin [371 \(UG\)](#), [436 \(UG\)](#), [1060 \(UG\)](#)
- logic preservation
 - syn_hier [553 \(UG\)](#)
 - syn_keep for nets [549 \(UG\)](#)
 - syn_keep for registers [549 \(UG\)](#)
 - syn_noprune [549 \(UG\)](#)
 - syn_preserve [549 \(UG\)](#)
- logic synthesis
 - translating UCF constraints [254 \(UG\)](#)
 - with design plan [19 \(UG\)](#)
- logical folders
 - creating [91 \(UG\)](#)
- logical operators
 - VHDL 2008 [412 \(HDLRef\)](#)
- loop statement [316 \(HDLRef\)](#)

[loop_limit directive 3441 \(AttrRef\)](#)
[Lowercase command 403 \(CmdRef\)](#)
[LPM_RAM_DQ](#)
 [VHDL example 527 \(UG\)](#)
[LPMs](#)
 [black box method simulation flow 1869 \(Ref\)](#)
 [comparison of Intel instantiation methods 521 \(UG\)](#)
 [creating synthesis projects 702 \(UG\)](#)
 [generics method, Cypress 526 \(UG\)](#)
 [in .vqm 522 \(UG\)](#)
 [instantiating as black boxes 521 \(UG\)](#)
 [instantiating as black boxes \(Intel\) 522 \(UG\)](#)
 [instantiating with a Verilog library 528 \(UG\)](#)
 [instantiating with a Verilog library \(Intel methodology\) 522 \(UG\)](#)
 [instantiating with VHDL prepared components 526 \(UG\)](#)
 [Intel megafunction example \(Verilog\) 522 \(UG\)](#)
 [Intel megafunction example \(VHDL\) 524 \(UG\)](#)
 [prepared components \(Intel\) 1816 \(Ref\)](#)
 [prepared components \(Intel\), example 526 \(UG\)](#)
 [using in Intel simulation flows 1868 \(Ref\)](#)
 [Verilog library simulation flow 1870 \(Ref\)](#)
 [VHDL prepared component simulation flow 1870 \(Ref\)](#)
 [VHDL prepared components instantiation example 527 \(UG\)](#)
[LPMs, Intel 521 \(UG\)](#)
[LUT6_2 primitives 2144 \(Ref\)](#)
[LUTRAM](#)
 [examples 1476 \(Ref\)](#)
[LUTRAMs 1476 \(Ref\)](#)
[LUTRAMs, inferring 1474 \(Ref\), 1476 \(Ref\)](#)

M

[mac_mult primitive](#)
 [Clearbox 666 \(UG\)](#)
[mac_out primitive](#)
 [Clearbox 666 \(UG\)](#)
[macro libraries](#)
 [Intel Verilog 1774 \(Ref\)](#)

[Intel VHDL 1774 \(Ref\)](#)
[Lattice 1925 \(Ref\)](#)
[macro libraries \(Xilinx\) 2102 \(Ref\)](#)
[macromodule 14 \(HDLRef\)](#)
[macros](#)
 [libraries 1407 \(Ref\), 302 \(HDLRef\)](#)
 [MATH18X18 block 1986 \(Ref\)](#)
 [Microsemi 1985 \(Ref\)](#)
 [preserving with syn_macro 3737 \(AttrRef\)](#)
 [SIMBUF 1986 \(Ref\)](#)
[macros \(Lattice\) 1905 \(Ref\), 1925 \(Ref\)](#)
[macros \(Xilinx\) 2102 \(Ref\)](#)
[manhattan distance \(Physical Analyst\) 1050 \(UG\)](#)
[manual compile points](#)
 [compared to automatic 586 \(UG\)](#)
 [flow 609 \(UG\)](#)
 [using with automatic 620 \(UG\)](#)
[map logic to macrocells \(Lattice\) 1936 \(Ref\)](#)
[map primitive 4151 \(AttrRef\)](#)
[mapper output file \(.srm\) 1417 \(Ref\), 1419 \(Ref\)](#)
[mapper report](#)
 [log file \(.srr\) 1423 \(Ref\)](#)
[margin, slack 1362 \(Ref\)](#)
[markers \(Physical Analyst\)](#)
 [adding 1048 \(UG\)](#)
 [adding with Go to Location 1049 \(UG\)](#)
 [deleting 1049 \(UG\)](#)
 [finding objects with 1047 \(UG\)](#)
 [measuring with 1050 \(UG\)](#)
 [moving 1049 \(UG\)](#)
 [navigating between 1050 \(UG\)](#)
 [using 1048 \(UG\)](#)
[Markers command 1048 \(UG\)](#)
[MAX 1850 \(Ref\)](#)
 [device options 1850 \(Ref\)](#)
 [file format options 1853 \(Ref\)](#)
 [set_option device options 1852 \(Ref\)](#)
 [set_option synthesis options 1852 \(Ref\)](#)
[MAX II](#)
 [file format options 1850 \(Ref\)](#)
 [set_option device options 1849 \(Ref\)](#)
 [set_option synthesis options 1849 \(Ref\)](#)
[max_parallel_jobs variable 761 \(UG\)](#)

maximum parallel jobs 760 (UG), 783 (UG), 572 (CmdRef)

maximum terms/macrocell (Lattice) 1937 (Ref)

MaxParallelJobs variable 760 (UG)

measurement tool

- Physical Analyst 693 (CmdRef)

MegaCore

- greybox flow with grey box netlist 677 (UG)
- greybox flow with IP package 681 (UG)

MegaCore IP 682 (UG)

Megacore IPs

- importing in a Quartus design 701 (UG), 702 (UG)

megafunctions

- altplls 1862 (Ref)
- Clearbox 1860 (Ref)
- creating synthesis project 702 (UG)
- grey boxes 1862 (Ref)
- inferring Clearbox information 667 (UG)
- instantiating Clearbox 671 (UG)
- using grey box netlist 677 (UG)

MegaWizard

- importing cores from 682 (UG)
- launching Intel 497 (CmdRef)

Megawizard

- altplls 1862 (Ref)

memory compiler 508 (CmdRef)

memory map information (MMI file) 511 (UG)

memory usage

- maximizing with HDL Analyst 445 (UG)

memory, saving 552 (CmdRef)

menubar 18 (CmdRef), 9 (DebugRef)

Menus

- Import IP 485 (CmdRef)

menus

- context-sensitive
 - See popup menus
- Edit 402 (CmdRef), 13 (DebugRef)
- HDL Analyst 542 (CmdRef), 691 (CmdRef)
- Help 602 (CmdRef), 59 (DebugRef)
- Options 568 (CmdRef), 691 (CmdRef), 56 (DebugRef)
- popup
 - See popup menus

- Project 423 (CmdRef)
- Run 498 (CmdRef), 666 (CmdRef)
- Tools, Synplify Premier DP Design Planner 667 (CmdRef)
- View 415 (CmdRef), 14 (DebugRef)

Message viewer

- filtering messages 286 (UG)
- keyboard shortcuts 285 (UG)
- saving filter expressions 287 (UG)
- searching 285 (UG)
- using 284 (UG)
- using the F3 key to search forward 285 (UG)
- using the Shift-F3 key to search backward 285 (UG)

message viewer

- description 1280 (Ref)

messagefilter.txt file 295 (UG)

Messages

- Tcl Window command 415 (CmdRef), 14 (DebugRef)

messages

- demoting 292 (UG)
- filtering 286 (UG)
- promoting 292 (UG)
- saving filter information from command line 288 (UG)
- saving filter information from GUI 287 (UG)
- severity levels 293 (UG)
- suppressing 292 (UG)
- writing messages to file 289 (UG)

Messages Tab 1280 (Ref)

Microsemi

- ACTgen macros 2048 (Ref)
- alsloc attribute 3393 (AttrRef)
- alspin attribute 3397 (AttrRef)
- alspreserve attribute 3401 (AttrRef)
- assigning I/O ports 3397 (AttrRef)
- attributes 2050 (Ref)
- black boxes 1985 (Ref)
- compile point synthesis 2046 (Ref)
- compile point timing data 2031 (Ref)
- device options 2035 (Ref)
- directives 2050 (Ref)
- features 1984 (Ref)
- forward-annotation, constraints 2042 (Ref)
- I/O insertion 2030 (Ref)

- macro libraries [2047 \(Ref\)](#)
- macros [1985 \(Ref\)](#)
- MATH18X18 block [1986 \(Ref\)](#)
- Operating Condition Device Option [2033 \(Ref\)](#)
- output netlist [1983 \(Ref\)](#)
- pin numbers for bus ports [2044 \(Ref\)](#)
- preserving relative placement [3393 \(AttrRef\)](#)
- product families [1982 \(Ref\)](#)
- reports [2045 \(Ref\)](#)
- retiming [2031 \(Ref\)](#)
- SIMBUF macro [1986 \(Ref\)](#)
- syn_radhardlevel attribute [3857 \(AttrRef\)](#)
- Tcl implementation options [2036 \(Ref\)](#)
- Microsemi implementing RAM [1994 \(Ref\)](#)
- Microsemil
 - cable type settings [45 \(DebugRef\)](#)
- MIF files
 - missing [1789 \(Ref\)](#)
- minPower library [652 \(UG\)](#)
- mitigation technology [865 \(UG\)](#)
- mixed block hierarchical synthesis flow [31 \(UG\)](#)
- mixed designs
 - black boxes [280 \(UG\)](#)
 - troubleshooting [62 \(UG\)](#)
- mixed language files [59 \(UG\)](#)
- model template, VHDL [341 \(HDLRef\)](#)
- models
 - VHDL [94 \(DebugRef\)](#)
- modes
 - cross triggering [50 \(DebugRef\)](#)
- modules
 - renaming [3491 \(AttrRef\)](#), [3917 \(AttrRef\)](#), [4053 \(AttrRef\)](#)
- modules, Verilog [94 \(HDLRef\)](#)
- mouse button operations [1295 \(Ref\)](#)
- mouse operations [1293 \(Ref\)](#)
- Mouse Stroke Tutor [1294 \(Ref\)](#)
- Mouse Stroke Tutor command [602 \(CmdRef\)](#)
- mouse strokes
 - pushing/popping objects [340 \(UG\)](#), [402 \(UG\)](#)
- mouse strokes (Physical Analyst)
 - navigating between views [1025 \(UG\)](#)
- mouse wheel operations [1297 \(Ref\)](#)
- Move command
 - floating toolbar window [1298 \(Ref\)](#)
 - Log Watch window popup menu [1277 \(Ref\)](#)
 - Tcl window popup menu [1280 \(Ref\)](#)
- moving between objects in the Hierarchy Browser [1324 \(Ref\)](#)
- moving GUI entities
 - toolbar [1298 \(Ref\)](#)
- multicycle constraints
 - forward-annotating [1891 \(Ref\)](#)
 - forward-annotation (Intel) [1876 \(Ref\)](#)
- multicycle paths
 - clocks as from/to points [336 \(CmdRef\)](#)
 - examples [326 \(CmdRef\)](#)
 - POS [334 \(CmdRef\)](#)
 - setting constraints [190 \(UG\)](#)
 - setting constraints (Legacy) [232 \(UG\)](#)
 - syn_reference_clock [3908 \(AttrRef\)](#)
 - using different start/end clocks [325 \(CmdRef\)](#)
- multidimensional array
 - syntax restrictions [86 \(HDLRef\)](#)
 - Verilog 2001 [63 \(HDLRef\)](#)
- multi-IICE
 - tabs [4312 \(DebugUG\)](#)
- multi-IICE selection [45 \(DebugRef\)](#)
- multiple drivers
 - resolving [182 \(CmdRef\)](#)
- Multiple File Compilation Unit
 - Verilog panel [465 \(CmdRef\)](#)
- multiple implementations [97 \(UG\)](#), [54 \(DebugRef\)](#)
 - hierarchical projects [144 \(UG\)](#)
 - running from project [97 \(UG\)](#)
- multiple projects
 - displaying project files [576 \(CmdRef\)](#)
- multiple signal values [4296 \(DebugUG\)](#), [4297 \(DebugUG\)](#)
- multiple target technologies,
 - synthesizing with Tcl script [766 \(UG\)](#)
- multiple-sheet schematics [1344 \(Ref\)](#)
- multiplexed groups

- assigning [4222 \(DebugUG\)](#), [11 \(DebugRef\)](#)
- selecting [4288 \(DebugUG\)](#)
- multiplexer (Verilog) [103 \(HDLRef\)](#)
- multipliers
 - DSP blocks [1987 \(Ref\)](#)
 - pipelining restriction [538 \(UG\)](#)
- multipliers, pipelining [537 \(UG\)](#)
- multi-port RAMs
 - Xilinx implementations [2078 \(Ref\)](#)
- MultiProcessing
 - Continue on Error mode [571 \(CmdRef\)](#)
- multiprocessing
 - compile points [622 \(UG\)](#)
 - DesignWare licenses [653 \(UG\)](#)
 - maximum parallel jobs [760 \(UG\)](#), [783 \(UG\)](#), [572 \(CmdRef\)](#)
- multisheet schematics [396 \(UG\)](#)
 - for nested internal logic [433 \(UG\)](#)
 - searching just one sheet [411 \(UG\)](#)
 - transparent hierarchical instances [1346 \(Ref\)](#)
 - transparent instances [396 \(UG\)](#)

N

- name spaces
 - output netlist [419 \(UG\)](#)
 - technology view [413 \(UG\)](#)
- name_format Tcl command [720 \(CmdRef\)](#)
- naming
 - objects (VHDL) [291 \(HDLRef\)](#)
 - region [663 \(CmdRef\)](#)
- naming rules [388 \(CmdRef\)](#)
- navigating
 - among hierarchical levels
 - by pushing and popping [1347 \(Ref\)](#)
 - with the Hierarchy Browser [1351 \(Ref\)](#)
 - among the sheets of a schematic [1344 \(Ref\)](#)
- navigating among design views [333 \(UG\)](#), [397 \(UG\)](#)
- ncf file
 - cores [736 \(UG\)](#)
- ncf files
 - output physical constraints (Legacy) [248 \(UG\)](#)
 - translating to sdc [257 \(UG\)](#)

- using as input for logic design [254 \(UG\)](#)
- nesting design details (display) [1352 \(Ref\)](#)
- net buffering report, log file [1424 \(Ref\)](#)
- net drivers
 - displaying and selecting [545 \(CmdRef\)](#)
- netlist editing [1147 \(UG\)](#)
 - commands [1148 \(UG\)](#)
 - RTL-level [1147 \(UG\)](#)
 - Tcl commands [1148 \(UG\)](#)
- Netlist Editing Commands
 - get_prop [758 \(CmdRef\)](#)
- netlist editing commands [1148 \(UG\)](#)
- netlist file [1420 \(Ref\)](#)
 - initial values (Verilog) [1539 \(Ref\)](#)
- netlist formats
 - Implementation Options dialog box, Implementation Results panel [455 \(CmdRef\)](#)
- Netlist Restructure file (.nrf) [1405 \(Ref\)](#)
- Netlist Restructure panel, Implementation Options dialog box [665 \(CmdRef\)](#)
- netlists
 - importing from Vivado [718 \(UG\)](#)
- netlists (Physical Analyst)
 - analyzing [1059 \(UG\)](#)
- netlists for different vendors [1695 \(Ref\)](#), [1889 \(Ref\)](#), [1983 \(Ref\)](#), [2057 \(Ref\)](#)
- nets
 - expanding hierarchically from pins and ports [544 \(CmdRef\)](#)
 - expanding logic from [373 \(UG\)](#), [437 \(UG\)](#)
 - finding by name [402 \(CmdRef\)](#), [686 \(CmdRef\)](#)
 - preserving for probing with syn_probe [549 \(UG\)](#)
 - preserving with syn_keep [549 \(UG\)](#), [3721 \(AttrRef\)](#)
 - properties [320 \(UG\)](#), [390 \(UG\)](#)
 - properties (Physical Analyst) [698 \(CmdRef\)](#)
 - selecting drivers [440 \(UG\)](#)
 - selecting instances on [545 \(CmdRef\)](#)
- nets (Physical Analyst)
 - adding markers [1048 \(UG\)](#)
 - expanding logic from [1063 \(UG\)](#)

- resetting the display [1035 \(UG\)](#)
- routing [1033 \(UG\)](#)
- selecting instances [1063 \(UG\)](#)
- signal flow [1035 \(UG\)](#)
- unfiltering for Find command [1043 \(UG\)](#)
- nets (SystemVerilog) [176 \(HDLRef\)](#)
- New command [396 \(CmdRef\)](#), [658 \(CmdRef\)](#), [8 \(DebugRef\)](#)
- new Hierarchy Browser [346 \(UG\)](#)
- New Implementation command [430 \(CmdRef\)](#)
- New Project command [397 \(CmdRef\)](#)
- New property [392 \(UG\)](#)
- Next Bookmark command [403 \(CmdRef\)](#)
- Next Error command [501 \(CmdRef\)](#)
- Next Sheet command [417 \(CmdRef\)](#)
- next statement [319 \(HDLRef\)](#)
- NGC cores [734 \(UG\)](#)
- NGO core [734 \(UG\)](#)
- NIOS II, importing as greybox [685 \(UG\)](#)
- non-secure core flow
 - synthesis [737 \(UG\)](#)
- Normal View command [416 \(CmdRef\)](#)
- notes
 - filtering [285 \(UG\)](#)
 - sorting [285 \(UG\)](#)
- notes, definition [49 \(UG\)](#)
- nram
 - Xilinx implementations [2078 \(Ref\)](#)
- nrf file [1405 \(Ref\)](#)
- numeric_bit IEEE package (VHDL) [301 \(HDLRef\)](#)
- numeric_std IEEE package (VHDL) [301 \(HDLRef\)](#)

O

- object information
 - status bar, HDL Analyst tool [1330 \(Ref\)](#)
 - viewing in HDL Analyst tool [1330 \(Ref\)](#)
- object prefixes
 - Tcl find command [223 \(CmdRef\)](#)
- object properties

- annotated properties for analyst [230 \(CmdRef\)](#)
- object search order (Timing Analyzer) [535 \(CmdRef\)](#)
- object types
 - Tcl find command [223 \(CmdRef\)](#)
- objects
 - crossprobing [1341 \(Ref\)](#)
 - displaying compactly [591 \(CmdRef\)](#)
 - dissolving [1352 \(Ref\)](#)
 - expanding paths between [544 \(CmdRef\)](#)
 - filtering [546 \(CmdRef\)](#)
 - finding [699 \(CmdRef\)](#)
 - finding on current sheet [411 \(UG\)](#)
 - flagging by property [391 \(UG\)](#)
 - making transparent [1352 \(Ref\)](#)
 - selecting in Floorplan Editor [692 \(CmdRef\)](#)
 - selecting overlapping in Physical Analyst view [703 \(CmdRef\)](#)
 - selecting/deselecting [395 \(UG\)](#)
 - unselecting
 - all in schematic [553 \(CmdRef\)](#)
- objects (Physical Analyst)
 - finding [1043 \(UG\)](#)
 - finding by location [1047 \(UG\)](#)
 - overlapping [1036 \(UG\)](#)
 - select overlapping [1036 \(UG\)](#)
 - selecting [1035 \(UG\)](#)
- objects (VHDL)
 - naming [291 \(HDLRef\)](#)
- objects, schematic
 - See schematic objects
- OBUFDS
 - inference [2129 \(Ref\)](#)
- OBUFTDS
 - inference [2129 \(Ref\)](#)
- OEM Content
 - subproject supported only for Lattice [636 \(CmdRef\)](#)
- OFFSET constraints
 - unsupported [1396 \(Ref\)](#)
- OFFSET I/O constraints (Xilinx) [4187 \(AttrRef\)](#)
- Online help
 - F1 key [1252 \(Ref\)](#)
- online help [37 \(DebugRef\)](#)
 - accessing [1252 \(Ref\)](#)

opaque hierarchical instances 1333 (Ref)
 are not flattened 1359 (Ref)

Open command
 File menu 396 (CmdRef), 426 (CmdRef), 8 (DebugRef)

Open Project command 396 (CmdRef)

open_design
 with find and expand 213 (UG)

open_design command 103 (CmdRef)

open_file command 104 (CmdRef)

opening
 project 396 (CmdRef)

operators
 exponential 27 (HDLRef)
 set membership (SystemVerilog) 200 (HDLRef)
 state machine 73 (DebugRef)
 streaming (SystemVerilog) 197 (HDLRef)
 Tcl collection 240 (CmdRef)
 type (SystemVerilog) 206 (HDLRef)
 Verilog 14 (HDLRef)

VHDL
 assignment 292 (HDLRef)
 Selected Name Support (SNS) 330 (HDLRef)
 sharing in case statements 325 (HDLRef)
 SNS 330 (HDLRef)
 VHDL 2008 condition 414 (HDLRef)
 VHDL 2008 logical 412 (HDLRef)
 VHDL 2008 relational 416 (HDLRef)

operators (SystemVerilog) 186 (HDLRef)

operators (VHDL) 306 (HDLRef)

opt file 1405 (Ref), 1415 (Ref)

optimization
 for area 533 (UG)
 for timing 534 (UG)
 generated clock 859 (UG)
 logic preservation. *See* logic preservation.
 mapper effort. *See* fast synthesis 535 (UG)
 preserving hierarchy 553 (UG)
 preserving objects 549 (UG)
 state machines 563 (UG)
 tips for 532 (UG)

option settings
 reporting 87 (CmdRef)

options
 Achronix Speedster22iHD 1753 (Ref)
 CPLDs (Xilinx) 2159 (Ref)
 Intel Cyclone 1843 (Ref)
 Intel Stratix 1846 (Ref)
 Lattice iCE65/iCE40 1953 (Ref)
 LatticeSC/SCM and LatticeXP 1941 (Ref)
 Project view 1314 (Ref)
 Frequency (Mhz) 1315 (Ref)
 FSM Compiler 1316 (Ref)
 FSM Explorer 1316 (Ref)
 Pipelining 1317 (Ref)
 Resource Sharing 1317 (Ref)
 Retiming 1317 (Ref)
 prototyping 481 (CmdRef)
 setting 149 (CmdRef)
 setting with set_option Tcl command 768 (UG)
 Spartan (Xilinx) 2150 (Ref)
 Virtex (Xilinx) 2150 (Ref)

options (Microsemi) 2036 (Ref)

Options command
 Xilinx submenu 569 (CmdRef)

Options for implementation dialog box
 Implementation Results panel 453 (CmdRef)

Options menu 568 (CmdRef), 691 (CmdRef), 56 (DebugRef)
 Quartus submenu (Intel) 569 (CmdRef)

Options panel
 Implementation Options dialog box 447 (CmdRef)

orca_padtype attribute (Lattice) 3445 (AttrRef)

orca_props attribute 3449 (AttrRef)

orig_inst_of property 393 (UG)

original source files
 searchpath 4313 (DebugUG)

original sources 4313 (DebugUG)

output buffers
 selection 4131 (AttrRef)

output constraints, setting 192 (UG)

output constraints, setting (Legacy) 240 (UG)

output drivers
 slowing transition times 4179 (AttrRef)
 transition time 4127 (AttrRef)

output files [1413 \(Ref\)](#)
 _est.srr [1414 \(Ref\)](#)
 .areasrr [1413 \(Ref\)](#)
 .edf. *See* edif file
 .est [1414 \(Ref\)](#), [666 \(CmdRef\)](#)
 .info [1414 \(Ref\)](#)
 .sar [1417 \(Ref\)](#)
 .srm [1417 \(Ref\)](#), [1419 \(Ref\)](#)
 .srp [1417 \(Ref\)](#), [543 \(CmdRef\)](#)
 .srr [1421 \(Ref\)](#)
 watching selected information [1276 \(Ref\)](#)
 .srs [1417 \(Ref\)](#)
 .ta [1419 \(Ref\)](#)
 .vhm [1420 \(Ref\)](#)
 .vm [1420 \(Ref\)](#)
 .xnf (Xilinx). *See* xnf files (Xilinx). [2056 \(Ref\)](#)
 log. *See* log file
 netlist [1420 \(Ref\)](#)
 specifying [107 \(UG\)](#)
 srs
 See srs file
 See also files
 output netlists
 finding objects [419 \(UG\)](#)
 Output Windows [1284 \(Ref\)](#)
 overlapping objects
 selecting in Physical Analyst view [703 \(CmdRef\)](#)
 overriding FSM Compiler [1844 \(Ref\)](#), [1847 \(Ref\)](#), [168 \(CmdRef\)](#)
 overriding parameter value, Verilog [97 \(HDLRef\)](#)
 overutilization [280 \(UG\)](#)
 Overview of the Synopsys FPGA Synthesis Tools [1242 \(Ref\)](#)

P

package library, adding [82 \(UG\)](#)
 packages [240 \(HDLRef\)](#)
 VHDL 2008 [425 \(HDLRef\)](#)
 VHDL 2008 generics [428 \(HDLRef\)](#)
 packages, VHDL [300 \(HDLRef\)](#)
 pad cell insertion file, Intel [1779 \(Ref\)](#)
 pad locations
 See also pin locations

pad types
 industry standards [193 \(UG\)](#)
 Lattice ORCA [3445 \(AttrRef\)](#)
 Xilinx [4157 \(AttrRef\)](#)
 pads
 disabling I/O insertion [1749 \(Ref\)](#)
 disabling I/O insertion (Xilinx) [2089 \(Ref\)](#)
 Pan command [416 \(CmdRef\)](#)
 panels
 Implementation Options dialog box
 Design Planning [665 \(CmdRef\)](#)
 Netlist Restructure [665 \(CmdRef\)](#)
 parallel jobs [760 \(UG\)](#)
 parallel_case directive [3453 \(AttrRef\)](#)
 parameter data types
 SystemVerilog [178 \(HDLRef\)](#)
 parameter passing [63 \(UG\)](#)
 boolean generics [62 \(UG\)](#)
 parameterized modules
 instrumenting [4214 \(DebugUG\)](#)
 parameters
 extracting from Verilog source code [111 \(UG\)](#)
 overriding HDL [89 \(CmdRef\)](#)
 SYNCore adder/subtractor [1649 \(Ref\)](#)
 SYNCore byte-enable RAM [1617 \(Ref\)](#)
 SYNCore counter [1671 \(Ref\)](#)
 SYNCore FIFO [1562 \(Ref\)](#)
 SYNCore RAM [1595 \(Ref\)](#)
 SYNCore ROM [1632 \(Ref\)](#)
 parity bus, Xilinx block RAM [2078 \(Ref\)](#)
 part selection options [99 \(UG\)](#)
 partdata tcl command [105 \(CmdRef\)](#)
 partial buses
 instrumenting [4218 \(DebugUG\)](#)
 partition flow, Xilinx [1120 \(UG\)](#)
 partitioned RTL view file (.srp) [1417 \(Ref\)](#), [543 \(CmdRef\)](#)
 partitioning (Synplify Premier)
 bit slicing [1013 \(UG\)](#)
 partitioning of schematics into sheets
 [1344 \(Ref\)](#)
 passwords
 encryption [36 \(DebugRef\)](#)
 encryption/decryption [31 \(DebugRef\)](#)

Paste - Replicate command [661 \(CmdRef\)](#)
Paste command [402 \(CmdRef\)](#), [13 \(DebugRef\)](#)
pasting [1300 \(Ref\)](#)
path constraints
 false paths [204 \(UG\)](#)
 false paths (Legacy) [242 \(UG\)](#)
path delays
 clocks as from/to points [337 \(CmdRef\)](#)
path filtering [534 \(CmdRef\)](#)
path names [14 \(DebugRef\)](#)
path separator [12 \(DebugRef\)](#)
pathnames
 using wildcards for long names (Find) [414 \(UG\)](#)
paths
 crossprobing [426 \(UG\)](#)
 expanding hierarchically from pins and ports [544 \(CmdRef\)](#)
 tracing between objects [440 \(UG\)](#)
 tracing from net [373 \(UG\)](#), [437 \(UG\)](#)
 tracing from pin [371 \(UG\)](#), [436 \(UG\)](#)
paths (Physical Analyst)
 tracing between objects [1065 \(UG\)](#)
 tracing from net [1063 \(UG\)](#)
 tracing from pin [1060 \(UG\)](#)
pattern matching
 Find command (Tcl) [206 \(UG\)](#)
pattern searching [162 \(UG\)](#)
pd_strategy property, UPF [1227 \(UG\)](#)
PDF
 cutting from [51 \(UG\)](#)
percentage of design to optimize for timing
 Lattice [1937 \(Ref\)](#)
performance summary, timing report [1428 \(Ref\)](#)
Physical Analyst
 analyzing netlists [1059 \(UG\)](#)
 command summary [692 \(CmdRef\)](#)
 context window [1026 \(UG\)](#)
 control panel [1023 \(UG\)](#), [1687 \(Ref\)](#), [1689 \(Ref\)](#)
 cross probing [688 \(CmdRef\)](#)
 crossprobing from text files [1054 \(UG\)](#)
 crossprobing RTL view [1056 \(UG\)](#)
 crossprobing to Technology view [1057 \(UG\)](#)
 device view [1691 \(Ref\)](#)
 displaying instances [1029 \(UG\)](#)
 Enhanced Instance Display [689 \(CmdRef\)](#)
 identifying encrypted IP objects [1050 \(UG\)](#)
 input files [1689 \(Ref\)](#)
 instance commands [694 \(CmdRef\)](#)
 net commands [696 \(CmdRef\)](#)
 opening [1022 \(UG\)](#)
 overlapping objects [1036 \(UG\)](#)
 properties [1038 \(UG\)](#), [697 \(CmdRef\)](#)
 routing nets [1688 \(Ref\)](#)
 using Block Inputs Map [1073 \(UG\)](#)
 using Block Utilization Map [1072 \(UG\)](#)
 using implementation maps [1066 \(UG\)](#)
 using Routing Congestion map [1070 \(UG\)](#)
 using Slack Map [1074 \(UG\)](#)
Physical Analyst view
 adding markers [1049 \(UG\)](#)
 Configure Enhanced Instance Display command [687 \(CmdRef\)](#)
 critical paths [484 \(UG\)](#)
 Cross Probing command [687 \(CmdRef\)](#)
 crossprobing [1052 \(UG\)](#)
 displaying net signal flow [1035 \(UG\)](#)
 Expand commands [1060 \(UG\)](#)
 filter command [687 \(CmdRef\)](#)
 filtering [1059 \(UG\)](#)
 Find command [699 \(CmdRef\)](#)
 finding objects [1043 \(UG\)](#), [699 \(CmdRef\)](#)
 Go to Location command [1047 \(UG\)](#), [688 \(CmdRef\)](#)
 instance properties [697 \(CmdRef\)](#)
 net properties [698 \(CmdRef\)](#)
 Physical Analyst Properties command [687 \(CmdRef\)](#)
 selecting objects [1035 \(UG\)](#)
 Selection Transcription command [687 \(CmdRef\)](#)
 Show Critical Path command [687 \(CmdRef\)](#)
 tool tips (Physical Analyst) [1041 \(UG\)](#)
 unfilter command [687 \(CmdRef\)](#), [693 \(CmdRef\)](#)
 using markers [1048 \(UG\)](#)
 zoom selected objects [1024 \(UG\)](#)
physical constraints

- design-plan based logic synthesis [19 \(UG\)](#)
- translating QSF constraints [1382 \(Ref\)](#), [124 \(CmdRef\)](#)
- Xilinx output file (Legacy) [248 \(UG\)](#)
- physical constraints (Design Planner - Intel)
 - Intel guidelines [1002 \(UG\)](#)
- physical constraints (Design Planner - Xilinx)
 - Xilinx guidelines [1011 \(UG\)](#)
- physical coordinates
 - marking [1048 \(UG\)](#)
- physical optimization
 - description [1244 \(Ref\)](#)
- physical synthesis
 - translating QSF constraints [124 \(CmdRef\)](#)
- physical synthesis netlist file (.srp) [543 \(CmdRef\)](#)
- PICs [1966 \(Ref\)](#)
- pin assignment (Design Planner) [983 \(UG\)](#)
 - assigning clock pins [986 \(UG\)](#)
 - crossprobing [991 \(UG\)](#)
 - temporary assigns [988 \(UG\)](#)
- pin assignment tool (Design Planner) [979 \(UG\)](#)
- pin assignments (Design Planner)
 - temporary [988 \(UG\)](#)
- pin location constraints
 - QSF [1382 \(Ref\)](#)
- pin locations
 - forward annotating [3729 \(AttrRef\)](#)
 - Lattice [3439 \(AttrRef\)](#)
 - Microsemi [3397 \(AttrRef\)](#)
 - specifying (Xilinx) [2090 \(Ref\)](#), [2122 \(Ref\)](#)
- pin names, displaying [435 \(UG\)](#)
- pins
 - displaying
 - on transparent instances [1337 \(Ref\)](#)
 - displaying names [590 \(CmdRef\)](#)
 - displaying on technology-specific primitives [1338 \(Ref\)](#)
 - displaying on transparent instances [551 \(CmdRef\)](#)
 - expanding hierarchically from [544 \(CmdRef\)](#)
 - expanding logic from [371 \(UG\)](#), [436 \(UG\)](#), [1060 \(UG\)](#)
 - expanding paths between [544 \(CmdRef\)](#)
 - isolating paths from [1363 \(Ref\)](#), [550 \(CmdRef\)](#)
 - maximum on schematic sheet [595 \(CmdRef\)](#)
 - properties [320 \(UG\)](#), [390 \(UG\)](#)
- pipelining
 - adding attribute [539 \(UG\)](#)
 - definition [537 \(UG\)](#)
 - multipliers [538 \(UG\)](#)
 - option [1317 \(Ref\)](#)
 - prerequisites [537 \(UG\)](#)
 - syn_pipeline attribute [3827 \(AttrRef\)](#)
 - whole design [538 \(UG\)](#)
- pipelining (Lattice) [1959 \(Ref\)](#)
- pipelining (Xilinx) [2140 \(Ref\)](#)
- Pipelining option, Project view [1317 \(Ref\)](#)
- Place & Route
 - creating a new options file for Xilinx [629 \(CmdRef\)](#)
- place & route
 - run from the synthesis tool [627 \(CmdRef\)](#)
- Place & Route options file [628 \(CmdRef\)](#)
 - adding for Xilinx [628 \(CmdRef\)](#)
- place & route options file
 - specifying [628 \(CmdRef\)](#)
- place & route timing correlation tab [524 \(CmdRef\)](#)
- place and route
 - black boxes [280 \(UG\)](#)
- Place and Route constraint file (Microsemi) [2042 \(Ref\)](#)
- Place and Route panel
 - Implementation Options dialog box [483 \(CmdRef\)](#)
- place and route tcl commands
 - job [96 \(CmdRef\)](#)
- place-and-route
 - customizing Vivado option file [1103 \(UG\)](#)
- Platform Designer [706 \(UG\)](#)
- PLL constraints [1778 \(Ref\)](#)
- PLLs
 - defining clocks (Legacy) [237 \(UG\)](#)
- pointers, mouse

- cross-hairs [1296 \(Ref\)](#)
- push/pop arrows [1350 \(Ref\)](#)
- zoom [416 \(CmdRef\)](#)
- popping up design hierarchy [1347 \(Ref\)](#)
- popup menus
 - floating toolbar [1298 \(Ref\)](#)
 - FSM Viewer [610 \(CmdRef\)](#)
 - Hierarchy Browser [641 \(CmdRef\)](#)
 - Log Watch window [1277 \(Ref\)](#), [1278 \(Ref\)](#), [607 \(CmdRef\)](#)
 - Log Watch window positioning [1277 \(Ref\)](#)
 - Project view [613 \(CmdRef\)](#)
 - RTL view [641 \(CmdRef\)](#), [10 \(DebugRef\)](#)
 - Tcl window [1280 \(Ref\)](#), [607 \(CmdRef\)](#), [9 \(DebugRef\)](#)
 - Technology view [641 \(CmdRef\)](#), [10 \(DebugRef\)](#)
- port context [154 \(UG\)](#)
- port mismatches
 - black boxes in synthesized netlist [281 \(UG\)](#)
- port placement [4147 \(AttrRef\)](#)
- ports
 - displaying names [590 \(CmdRef\)](#)
 - expanding hierarchically from [544 \(CmdRef\)](#)
 - expanding paths between [544 \(CmdRef\)](#)
 - false path constraint [204 \(UG\)](#)
 - false path constraint (Legacy) [242 \(UG\)](#)
 - finding by name [402 \(CmdRef\)](#)
 - isolating paths from [550 \(CmdRef\)](#)
 - properties [320 \(UG\)](#), [390 \(UG\)](#)
 - selecting all in schematic [553 \(CmdRef\)](#)
- ports (VHDL) [297 \(HDLRef\)](#)
- Ports command
 - schematic [553 \(CmdRef\)](#)
 - sheet [553 \(CmdRef\)](#)
- ports connections (SystemVerilog) [248 \(HDLRef\)](#)
- POS
 - interface [333 \(CmdRef\)](#)
- POS interface
 - using [200 \(UG\)](#)
- post place and route resynthesis [1129 \(UG\)](#)
 - Intel [1129 \(UG\)](#)
 - Xilinx [1133 \(UG\)](#)
- post_route.dcp file [1110 \(UG\)](#)
- post-compile instrumentation [4214 \(DebugUG\)](#)
- post-synthesis constraints with adc [464 \(UG\)](#)
- post-synthesis simulation [1762 \(Ref\)](#)
- post-synthesis simulation, Xilinx [2172 \(Ref\)](#)
- power domains
 - selective corruption [1223 \(UG\)](#)
- power domains, UPF [1203 \(UG\)](#)
- power_domain property, UPF [1227 \(UG\)](#)
- pragma translate_off directive [3457 \(AttrRef\)](#)
- pragma translate_on directive [3457 \(AttrRef\)](#)
- precedence of constraint files [1370 \(Ref\)](#)
- pre-configured triggers [4291 \(DebugUG\)](#)
- predefined enumeration types (VHDL) [287 \(HDLRef\)](#)
- predefined functions
 - VHDL 2008 [423 \(HDLRef\)](#)
- predefined packages (VHDL) [301 \(HDLRef\)](#)
- preferences
 - crossprobing to place-and-route file [398 \(UG\)](#)
 - displaying Hierarchy Browser [398 \(UG\)](#)
 - displaying labels [399 \(UG\)](#)
 - HDL Analyst tool [1344 \(Ref\)](#)
 - project file display [575 \(CmdRef\)](#)
 - RTL and Technology views [398 \(UG\)](#)
 - sheet size (UI) [398 \(UG\)](#)
- Preferences command
 - Design Planner tools menu [668 \(CmdRef\)](#)
- Preferences dialog box
 - Design Planner [668 \(CmdRef\)](#)
- Preferred License Selection command
 - [603 \(CmdRef\)](#), [59 \(DebugRef\)](#)
- prefixes
 - Timing Analyzer points [535 \(CmdRef\)](#)
- PREP benchmarks
 - Verilog [125 \(HDLRef\)](#)
 - VHDL [405 \(HDLRef\)](#)
- prepared components
 - Intel VHDL [1816 \(Ref\)](#)
- preserving region resources

Design Plan Editor view [994 \(UG\)](#)

Previous bookmark command [403 \(CmdRef\)](#)

Previous Error/Warning command [501 \(CmdRef\)](#)

Previous Sheet command [417 \(CmdRef\)](#)

primitive instances [1332 \(Ref\)](#)

primitives

- dividing [195 \(CmdRef\)](#)
- initial values [514 \(UG\)](#)
- internal logic, displaying [591 \(CmdRef\)](#)
- pin name display [435 \(UG\)](#)
- pin names in Technology view [1338 \(Ref\)](#)
- pushing into with mouse stroke [341 \(UG\)](#), [403 \(UG\)](#)
- viewing internal hierarchy [431 \(UG\)](#)

primitives (Synplify Premier)

- breaking up large [1013 \(UG\)](#)

primitives, Verilog [17 \(HDLRef\)](#)

Print command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)

Print Setup command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)

printing

- view [396 \(CmdRef\)](#)

printing image

- Create Image command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)

priority encoding [3453 \(AttrRef\)](#)

private key [631 \(UG\)](#)

prj file [11 \(UG\)](#), [1405 \(Ref\)](#)

probes

- adding in source code [570 \(UG\)](#)
- definition [570 \(UG\)](#)
- inserting [3849 \(AttrRef\)](#)
- retiming [547 \(UG\)](#)

process keyword (VHDL) [311 \(HDLRef\)](#)

process template (VHDL)

- modeling combinational logic [311 \(HDLRef\)](#)

process template, VHDL [343 \(HDLRef\)](#)

Process View [1272 \(Ref\)](#)

processes, VHDL [340 \(HDLRef\)](#)

process-level hierarchy [1013 \(UG\)](#)

Product of Sums

- See POS

Product of Sums interface. See POS interface

program_terminate command [109 \(CmdRef\)](#)

program_version command [110 \(CmdRef\)](#)

project command [57 \(DebugRef\)](#)

- archiving projects [165 \(UG\)](#)
- copying projects [175 \(UG\)](#)
- CPLDs (Xilinx) [2161 \(Ref\)](#)
- Intel file formats [1858 \(Ref\)](#)
- Spartan (Xilinx) [2157 \(Ref\)](#)
- unarchiving projects [171 \(UG\)](#)
- Virtex (Xilinx) [2157 \(Ref\)](#)
- XC4000 (Xilinx) [2157 \(Ref\)](#)

project file hierarchy [91 \(UG\)](#)

project files [4237 \(DebugUG\)](#)

- adding files [84 \(UG\)](#)
- adding source files [80 \(UG\)](#)
- batch mode [752 \(UG\)](#)
- creating [80 \(UG\)](#)
- definition [80 \(UG\)](#)
- deleting files from [84 \(UG\)](#)
- opening [84 \(UG\)](#)
- organization into folders [575 \(CmdRef\)](#)
- replacing files in [84 \(UG\)](#)
- updating include paths [89 \(UG\)](#)
- VHDL library [82 \(UG\)](#)

project files (.prj) [11 \(UG\)](#), [1405 \(Ref\)](#)

Project Files view [1260 \(Ref\)](#)

Project menu [423 \(CmdRef\)](#)

- commands [423 \(CmdRef\)](#)

Project Options command [617 \(CmdRef\)](#)

project results

- Implementation Directory [1271 \(Ref\)](#)
- Process View [1272 \(Ref\)](#)
- Project Status View [1263 \(Ref\)](#)

Project Results View [1263 \(Ref\)](#)

project status report

- remote access [273 \(UG\)](#)

Project Status View [1263 \(Ref\)](#)

project Tcl command [111 \(CmdRef\)](#)

Project toolbar [1299 \(Ref\)](#)

Project view [1256 \(Ref\)](#)

- buttons and options [1314 \(Ref\)](#)
- display settings [575 \(CmdRef\)](#)
- options [1314 \(Ref\)](#)

popup menu [613 \(CmdRef\)](#)
 setting up [573 \(CmdRef\)](#)
 Synplify Premier/DP [1256 \(Ref\)](#)
 Synplify Pro [1256 \(Ref\)](#)
 Synplify tool [1256 \(Ref\)](#)
 Project View Options command [568 \(CmdRef\)](#)
 Project window [1256 \(Ref\)](#)
 project_data Tcl command [120 \(CmdRef\)](#)
 project_file Tcl command [121 \(CmdRef\)](#)
 project_folder
 Tcl command [123 \(CmdRef\)](#)
 project_name_cck.rpt file [1440 \(Ref\)](#)
 projects
 adding files [426 \(CmdRef\)](#)
 archiving [165 \(UG\)](#)
 closing [397 \(CmdRef\)](#)
 copying [175 \(UG\)](#)
 creating (Build Project) [396 \(CmdRef\)](#)
 creating (New) [397 \(CmdRef\)](#)
 creating new [57 \(DebugRef\)](#)
 displaying multiple [576 \(CmdRef\)](#)
 files after importing from Quartus [699 \(UG\)](#)
 importing [57 \(DebugRef\)](#)
 importing from Quartus [695 \(UG\)](#)
 instrumenting [4237 \(DebugUG\)](#)
 opening [396 \(CmdRef\)](#), [57 \(DebugRef\)](#)
 restoring archives [171 \(UG\)](#)
 Promote Global Buffer Threshold (Microsemi) [2029 \(Ref\)](#)
 properties
 copying and pasting (Physical Analyst) [1042 \(UG\)](#)
 displaying with tooltip [320 \(UG\)](#), [390 \(UG\)](#)
 encrypted IP cells (Physical Analyst) [1050 \(UG\)](#)
 find command [230 \(CmdRef\)](#)
 finding objects with Tcl find -filter [207 \(UG\)](#)
 orig_inst_of [393 \(UG\)](#)
 Physical Analyst [697 \(CmdRef\)](#)
 project [120 \(CmdRef\)](#)
 reporting for collections [221 \(UG\)](#)
 viewing for individual objects [320 \(UG\)](#), [390 \(UG\)](#)
 Properties command
 Design Planner [663 \(CmdRef\)](#)
 instances in Physical Analyst [697 \(CmdRef\)](#)
 nets in Physical Analyst [698 \(CmdRef\)](#)
 View menu
 Synplify Premier DP Design Planner [662 \(CmdRef\)](#)
 prototypes
 fast turnaround [1195 \(UG\)](#)
 initial [1193 \(UG\)](#)
 optimizing timing [1196 \(UG\)](#)
 QoR [1196 \(UG\)](#)
 prototyping [1185 \(UG\)](#)
 converting ASIC designs [1188 \(UG\)](#)
 guidelines [1189 \(UG\)](#)
 using hyper source threading [656 \(UG\)](#)
 prototyping options [481 \(CmdRef\)](#)
 public key [631 \(UG\)](#)
 pulsewidth mode
 complex counter [52 \(DebugRef\)](#)
 Push Tristates
 Verilog panel [465 \(CmdRef\)](#)
 Push/Pop Hierarchy command [417 \(CmdRef\)](#)
 Push/Pop mode
 HDL Analyst [402 \(UG\)](#)
 keyboard shortcut [404 \(UG\)](#)
 using [340 \(UG\)](#), [341 \(UG\)](#), [402 \(UG\)](#), [404 \(UG\)](#)
 push/pop mode, HDL Analyst tool [1347 \(Ref\)](#)
 pwd command [58 \(DebugRef\)](#)

Q

QoR
 prototypes [1196 \(UG\)](#)
 qout
 out std_logic_vector (7 [4029 \(AttrRef\)](#))
 qsf
 importing [696 \(UG\)](#)
 translating I/O constraints [245 \(UG\)](#)
 QSF constraints
 example [1383 \(Ref\)](#)
 qsf file
 translated files for synthesis [699 \(UG\)](#)
 qsf2sdc
 syntax [124 \(CmdRef\)](#)

translating constraints [245 \(UG\)](#)
 qsf2syn utility [125 \(CmdRef\)](#)
 syntax [125 \(CmdRef\)](#)
 qsf2syn.log file [698 \(UG\)](#)
 Qsys [706 \(UG\)](#)
 qualified sampling [4304 \(DebugUG\)](#), [20 \(DebugRef\)](#)
 Quartus
 batch mode [1086 \(UG\)](#)
 converting constraints to sdc [1382 \(Ref\)](#), [124 \(CmdRef\)](#)
 edif and vqm file names [1880 \(Ref\)](#)
 imported settings and constraints [700 \(UG\)](#)
 importing design with Megacore IP [701 \(UG\)](#)
 importing design with megafunctions [702 \(UG\)](#)
 importing LPMs [702 \(UG\)](#)
 importing megafunctions [702 \(UG\)](#)
 importing projects from [695 \(UG\)](#)
 importing projects from, qsf2syn syntax [125 \(CmdRef\)](#)
 incremental flows [1087 \(UG\)](#)
 integrated flow [1084 \(UG\)](#)
 interactive flow [1085 \(UG\)](#)
 library versions [1774 \(Ref\)](#)
 qsf2sdc utility. See [qsf2sdc 1382 \(Ref\)](#), [124 \(CmdRef\)](#)
 supported constraints for import [700 \(UG\)](#)
 supported project settings for import [700 \(UG\)](#)
 synthesis project files [699 \(UG\)](#)
 Quartus Fast Fit flow [1088 \(UG\)](#)
 Quartus II Incremental Compilation flow [1089 \(UG\)](#)
 Quartus II Incremental Synthesis running [1089 \(UG\)](#)
 Quartus incremental compilation flow [1087 \(UG\)](#)
 Quartus megafunctions
 pad cell insertion [1779 \(Ref\)](#)
 Quartus Prime [1084 \(UG\)](#)
 QUARTUS_ROOTDIR variable
 inferring Clearbox megafunctions [668 \(UG\)](#), [706 \(UG\)](#)
 instantiating Clearbox [671 \(UG\)](#)

question mark wildcard, Find command [355 \(UG\)](#), [414 \(UG\)](#)
 quitting a synthesis run [505 \(CmdRef\)](#)

R

radiation effects. See [high reliability](#)
 radix
 sampled data [4294 \(DebugUG\)](#)
 RAM
 byte-wide write enable RAM (Intel) [1782 \(Ref\)](#)
 local TMR [921 \(UG\)](#)
 MMI file [511 \(UG\)](#)
 UPF retention strategy [1219 \(UG\)](#)
 RAM implementations
 Microsemi [1994 \(Ref\)](#)
 RAM inference [1451 \(Ref\)](#)
 Arria [1780 \(Ref\)](#)
 Cyclone [1780 \(Ref\)](#)
 Intel Stratix [1780 \(Ref\)](#)
 using attributes [1453 \(Ref\)](#)
 RAM inference (Intel) [1780 \(Ref\)](#)
 RAM mapping
 Intel Stratix [1781 \(Ref\)](#)
 RAM MMI file
 syn_ram_write_mem attribute [3867 \(AttrRef\)](#)
 RAM resources [20 \(DebugRef\)](#)
 RAM with control signals examples [1481 \(Ref\)](#)
 ram_block primitive
 Clearbox [666 \(UG\)](#)
 RAMs [506 \(UG\)](#)
 compiling with SYNCORE [1587 \(Ref\)](#)
 ECC [922 \(UG\)](#)
 implementation styles [3871 \(AttrRef\)](#)
 inferring block RAM [1455 \(Ref\)](#)
 initial values (Verilog) [1533 \(Ref\)](#)
 initializing [506 \(UG\)](#)
 initializing values (Xilinx) [2111 \(Ref\)](#)
 mapping LUTRAMs [1474 \(Ref\)](#)
 multi-port, Xilinx [2078 \(Ref\)](#)
 SYNCORE [1587 \(Ref\)](#)
 SYNCORE, byte-enable [1610 \(Ref\)](#)
 technology support [3875 \(AttrRef\)](#)
 TMR [921 \(UG\)](#)

- RAMs, inferring
 - advantages [1450 \(Ref\)](#)
- recent projects, opening [397 \(CmdRef\)](#)
- recording command [133 \(CmdRef\)](#)
- records
 - partially instrumented [4221 \(DebugUG\)](#)
- Redo command [402 \(CmdRef\)](#), [13 \(DebugRef\)](#)
- reference manual, role in document set [1241 \(Ref\)](#)
- Refresh command [607 \(CmdRef\)](#)
- region clock buffers (BUFR) [2129 \(Ref\)](#)
- Region Properties dialog box [663 \(CmdRef\)](#)
- regions
 - assigning critical paths [39 \(CmdRef\)](#)
 - creating [48 \(CmdRef\)](#)
 - retiming [548 \(UG\)](#)
- regions (Design Planner)
 - preserving logic and memory resources [994 \(UG\)](#)
 - replicating logic manually
 - replicating instances (Design Planner) [999 \(UG\)](#)
- regions, naming [663 \(CmdRef\)](#)
- register balancing. *See* retiming
- register constraints, setting (Legacy) [232 \(UG\)](#)
- register inference (Xilinx) [2080 \(Ref\)](#)
- Register Naming Guidelines for Local TMR [902 \(UG\)](#)
- register packing
 - See also* syn_useioff attribute [2119 \(Ref\)](#)
 - Intel [1865 \(Ref\)](#)
 - syn_useioff attribute, Intel [4079 \(AttrRef\)](#)
 - Xilinx [2119 \(Ref\)](#)
- registers
 - boundary scan [4272 \(DebugUG\)](#)
 - DDR (Xilinx) [2082 \(Ref\)](#)
 - false path constraint [204 \(UG\)](#)
 - false path constraint (Legacy) [242 \(UG\)](#)
 - inferring clock enables (Xilinx) [2080 \(Ref\)](#)
 - INIT value [2117 \(Ref\)](#)
 - preserving with syn_preserve [3833 \(AttrRef\)](#)
 - UPF retention strategy [1216 \(UG\)](#)
- registers (VHDL) [342 \(HDLRef\)](#)
- Registers panel
 - using SCOPE [189 \(UG\)](#)
- Registers panel, SCOPE [309 \(CmdRef\)](#)
- regular expressions
 - Tcl find command [224 \(CmdRef\)](#)
- relational operators
 - VHDL 2008 [416 \(HDLRef\)](#)
- relative location
 - alsloc (Microsemi) [3393 \(AttrRef\)](#)
 - xc_map (Xilinx) [4151 \(AttrRef\)](#)
 - xc_rloc [4173 \(AttrRef\)](#)
 - xc_uset [4193 \(AttrRef\)](#)
- relative placement. *See* RLOCs
- relative position, Xilinx components [2099 \(Ref\)](#)
- Reload command [641 \(CmdRef\)](#)
- remote access
 - status reports [273 \(UG\)](#)
- Remove Files From Project command [423 \(CmdRef\)](#)
- Remove Implementation command [615 \(CmdRef\)](#)
- remove_from_collection command [290 \(CmdRef\)](#)
- removing
 - bookmark (Text Editor) [1286 \(Ref\)](#)
 - window (view) [1298 \(Ref\)](#)
- Replace command
 - Text Editor [403 \(CmdRef\)](#)
- replacing
 - text [413 \(CmdRef\)](#)
- Replicated Assignments dialog box [668 \(CmdRef\)](#)
- replication
 - controlling [557 \(UG\)](#)
 - disabling [3919 \(AttrRef\)](#)
 - Intel [1840 \(Ref\)](#)
- report_clocks command [134 \(CmdRef\)](#)
- report_messages command [136 \(CmdRef\)](#)
- reports
 - constraint checking (cck.rpt) [1440 \(Ref\)](#)
 - gated clock conversion [818 \(UG\)](#)
 - hierarchical area report [1437 \(Ref\)](#)
 - resource usage (Xilinx) [2163 \(Ref\)](#)
 - resource usage, Intel [1871 \(Ref\)](#)
 - resource usage, Lattice [1962 \(Ref\)](#)

- shift registers, Intel [517 \(UG\)](#)
 - timing report (.ta file) [519 \(CmdRef\)](#)
- reports (Lattice) [1962 \(Ref\)](#)
- reset_path timing constraint [349 \(CmdRef\)](#)
- resets
 - packing in Intel DSP blocks [1814 \(Ref\)](#)
 - Verilog [110 \(HDLRef\)](#)
 - VHDL [353 \(HDLRef\)](#)
 - detecting problems [362 \(HDLRef\)](#)
- Resolve Multiple Drivers option [182 \(CmdRef\)](#)
- Resolve Selection dialog box [703 \(CmdRef\)](#)
- resolving conflicting timing constraints [338 \(CmdRef\)](#)
- Resource Center
 - See Technical Resource Center
- resource library (VHDL), creating [303 \(HDLRef\)](#)
- resource sharing [1974 \(Ref\)](#)
 - optimization technique [533 \(UG\)](#)
 - overriding option with syn_sharing [560 \(UG\)](#)
 - Resource Sharing option [450 \(CmdRef\)](#)
 - results example [560 \(UG\)](#)
 - syn_sharing directive [3969 \(AttrRef\)](#)
 - using [559 \(UG\)](#)
 - VHDL [325 \(HDLRef\)](#)
- Resource Sharing option, Project view [1317 \(Ref\)](#)
- resource usage [279 \(UG\)](#)
- resource usage report, log file [1425 \(Ref\)](#)
- resource utilization. See resource usage
- resourceUsage61 [2164 \(Ref\)](#)
- restrictions
 - instrumenting buffers [4217 \(DebugUG\)](#)
- resynthesis
 - compile points [603 \(UG\)](#)
 - forcing with Resynthesize All [603 \(UG\)](#)
 - forcing with Update Compile Point Timing Data [603 \(UG\)](#)
- Resynthesize All command [498 \(CmdRef\)](#)
- retention
 - RAMs [1218 \(UG\)](#)
- retention power strategy [1215 \(UG\)](#)
- retiming
 - effect on attributes and constraints [545 \(UG\)](#)
 - example [543 \(UG\)](#)
 - overview [541 \(UG\)](#)
 - probes [547 \(UG\)](#)
 - regions [548 \(UG\)](#)
 - report [544 \(UG\)](#)
 - report, log file [1426 \(Ref\)](#)
 - simulation behavior [546 \(UG\)](#)
 - syn_allow_retiming attribute [3461 \(AttrRef\)](#)
- retiming (Lattice) [1960 \(Ref\)](#)
- retiming (Microsemi) [2031 \(Ref\)](#)
- retiming (Xilinx) [2140 \(Ref\)](#)
- Retiming option, Project view [1317 \(Ref\)](#)
- return codes [753 \(UG\)](#)
- RLOC_ORIGINS
 - specifying [2136 \(Ref\)](#)
- RLOCs [2099 \(Ref\)](#), [2134 \(Ref\)](#), [2136 \(Ref\)](#)
 - specifying with synthesis attribute [2099 \(Ref\)](#), [2136 \(Ref\)](#)
 - specifying with xc attributes [2134 \(Ref\)](#)
- ROM
 - block RAM mapping (Xilinx) [2079 \(Ref\)](#)
- ROM compiler
 - SYNCore [1625 \(Ref\)](#)
- ROM inference (Intel) [1787 \(Ref\)](#)
- ROM inference examples [1550 \(Ref\)](#)
- ROM initialization
 - with rom.info file [1553 \(Ref\)](#)
 - with Verilog generate block [1554 \(Ref\)](#)
- rom.info file [404 \(UG\)](#), [1550 \(Ref\)](#)
- ROMs
 - Intel implementations [1788 \(Ref\)](#)
 - pipelining [537 \(UG\)](#)
 - SYNCore [1627 \(Ref\)](#)
 - viewing data table [404 \(UG\)](#)
- routability synthesis
 - using [576 \(UG\)](#)
- Routing Congestion map
 - Physical Analyst [1070 \(UG\)](#)
- routing nets (Physical Analyst) [1688 \(Ref\)](#)
- RTL
 - netlist editing [1147 \(UG\)](#)
- RTL static analysis

- using SpyGlass linting [71 \(UG\)](#)
- RTL view [1320 \(Ref\)](#)
 - See also HDL Analyst
 - analyzing clock trees [455 \(UG\)](#)
 - continue on error [301 \(UG\)](#)
 - crossprobing collection objects [216 \(UG\)](#)
 - crossprobing description [423 \(UG\)](#)
 - crossprobing from [424 \(UG\)](#)
 - crossprobing from Text Editor [425 \(UG\)](#)
 - defined [388 \(UG\)](#)
 - description [387 \(UG\)](#)
 - displaying [1301 \(Ref\)](#), [104 \(CmdRef\)](#)
 - file (.srs) [1417 \(Ref\)](#)
 - filtering [369 \(UG\)](#), [434 \(UG\)](#)
 - finding objects with Find [411 \(UG\)](#)
 - finding objects with Hierarchy Browser [345 \(UG\)](#), [409 \(UG\)](#)
 - flattening hierarchy [381 \(UG\)](#), [441 \(UG\)](#)
 - highlighting collections [221 \(UG\)](#)
 - opening [317 \(UG\)](#), [389 \(UG\)](#)
 - opening hierarchical view [543 \(CmdRef\)](#)
 - popup menu [641 \(CmdRef\)](#), [10 \(DebugRef\)](#)
 - popup menu commands [641 \(CmdRef\)](#)
 - primitives
 - Verilog [113 \(HDLRef\)](#)
 - VHDL [354 \(HDLRef\)](#)
 - selecting/deselecting objects [395 \(UG\)](#)
 - sequential shift components [516 \(UG\)](#)
 - setting preferences [398 \(UG\)](#)
 - state machine implementation [565 \(UG\)](#)
 - traversing hierarchy [401 \(UG\)](#)
- RTL views
 - hierarchical projects [160 \(UG\)](#)
 - hierarchical subprojects [142 \(UG\)](#)
- rules
 - library and package, VHDL [303 \(HDLRef\)](#)
- Run All Implementations command [501 \(CmdRef\)](#)
- Run Background Compile command [569 \(CmdRef\)](#)
- run command [4290 \(DebugUG\)](#), [59 \(DebugRef\)](#), [15 \(DebugRef\)](#)
- Run Foreground Compile command [569 \(CmdRef\)](#)
- Run menu [498 \(CmdRef\)](#), [666 \(CmdRef\)](#)
- Run Tcl Script command [501 \(CmdRef\)](#)
- run_vivado.tcl
 - See also Vivado, options file
- run_vivado.tcl file [1103 \(UG\)](#)
- running P&R
 - license release (synthesis) [1082 \(UG\)](#)
- running place & route [627 \(CmdRef\)](#)
- runtime
 - continue on error [298 \(UG\)](#)

S

- safe case [910 \(UG\)](#)
- Safe Case FSMs [949 \(UG\)](#)
- Safe Encoding FSMs [950 \(UG\)](#)
- safe FSM [908 \(UG\)](#)
 - using Hamming Distance 3 [915 \(UG\)](#)
 - using safe case [910 \(UG\)](#)
- sample buffer [4294 \(DebugUG\)](#)
 - trigger position [4293 \(DebugUG\)](#)
- sample clock [936 \(UG\)](#), [21 \(DebugRef\)](#)
- sample data [91 \(DebugRef\)](#)
- sample modes [4304 \(DebugUG\)](#)
- sampled data
 - changing radix [4294 \(DebugUG\)](#)
 - compressing [4240 \(DebugUG\)](#), [4292 \(DebugUG\)](#), [4305 \(DebugUG\)](#)
 - display controls [4294 \(DebugUG\)](#)
 - masking [4292 \(DebugUG\)](#)
- sampling
 - in folded hierarchy [4223 \(DebugUG\)](#)
 - qualified [20 \(DebugRef\)](#)
- sampling block [24 \(DebugRef\)](#)
- sampling signals [4216 \(DebugUG\)](#), [4217 \(DebugUG\)](#), [4223 \(DebugUG\)](#), [4226 \(DebugUG\)](#), [4228 \(DebugUG\)](#), [4231 \(DebugUG\)](#), [10 \(DebugRef\)](#), [19 \(DebugRef\)](#)
- sar file
 - Archive Project command [433 \(CmdRef\)](#)
- Save All command [396 \(CmdRef\)](#), [8 \(DebugRef\)](#)
- Save As command [396 \(CmdRef\)](#)
- Save command [396 \(CmdRef\)](#)
- scalable adder, creating (Verilog) [97 \(HDLRef\)](#)
- scalable architecture, using (VHDL) [395 \(HDLRef\)](#)

scalable designs (VHDL) [393 \(HDLRef\)](#)
scaling by overriding parameter value,
Verilog
 with # [97 \(HDLRef\)](#)
 with defparam [97 \(HDLRef\)](#)

scan chains
 Intel DSP blocks [1792 \(Ref\)](#)

schematic objects
 crossprobing [1341 \(Ref\)](#)
 definition [1330 \(Ref\)](#)
 displaying compactly [591 \(CmdRef\)](#)
 dissolving [1352 \(Ref\)](#)
 expanding paths between [544 \(CmdRef\)](#)
 filtering [546 \(CmdRef\)](#)
 finding [1339 \(Ref\)](#)
 making transparent [1352 \(Ref\)](#)
 status bar information [1330 \(Ref\)](#)
 unselecting all [553 \(CmdRef\)](#)

Schematic Options [348 \(UG\)](#)

schematic sheets [1344 \(Ref\)](#)
 hierarchical (definition) [1344 \(Ref\)](#)
 navigating among [1344 \(Ref\)](#)
 setting size [1344 \(Ref\)](#)

schematics
 configuring amount of logic on a sheet
 [1344 \(Ref\)](#)
 crossprobing [1341 \(Ref\)](#)
 displaying labels [590 \(CmdRef\)](#)
 filtered [1327 \(Ref\)](#)
 filtering commands [1355 \(Ref\)](#)
 flattening [546 \(CmdRef\)](#)
 flattening compared with filtering [1359 \(Ref\)](#)
 flattening selectively [1358 \(Ref\)](#)
 hierarchical (definition) [1344 \(Ref\)](#)
 multiple-sheet [1344 \(Ref\)](#)
 multiple-sheet. *See also* schematic sheets
 multisheet. *See* multisheet schematics
 navigating sheets [416 \(CmdRef\)](#)
 object information [1330 \(Ref\)](#)
 opening hierarchical RTL [543 \(CmdRef\)](#)
 page size [398 \(UG\)](#)
 partitioning into sheets [1344 \(Ref\)](#)
 selecting/deselecting objects [327 \(UG\)](#), [395 \(UG\)](#)
 sheet connectors [1331 \(Ref\)](#), [591 \(CmdRef\)](#)
 sheets
 navigating among [1344 \(Ref\)](#)
 size, setting [1344 \(Ref\)](#)

size in view, changing [1320 \(Ref\)](#)
unfiltered [1327 \(Ref\)](#)
unfiltering [1356 \(Ref\)](#)
unselecting objects [553 \(CmdRef\)](#)

SCOPE

 adding attributes [121 \(UG\)](#)
 adding probe insertion attribute [571 \(UG\)](#)
 assigning Xilinx pin locations [2123 \(Ref\)](#)
 Attributes panel [189 \(UG\)](#), [313 \(CmdRef\)](#)
 case sensitivity for Verilog designs [206 \(UG\)](#)
 clock groups [297 \(CmdRef\)](#)
 Clocks panel [188 \(UG\)](#), [296 \(CmdRef\)](#)
 collections compared to Tcl script window [214 \(UG\)](#)
 Collections panel [188 \(UG\)](#), [304 \(CmdRef\)](#)
 Compile Points panel [189 \(UG\)](#), [316 \(CmdRef\)](#)
 creating compile-point constraint file [616 \(UG\)](#)
 defining compile points [612 \(UG\)](#)
 Delay Paths panel [189 \(UG\)](#), [310 \(CmdRef\)](#)
 drag and drop [197 \(UG\)](#)
 editing operations [198 \(UG\)](#)
 for legacy sdc [1374 \(Ref\)](#)
 Generated Clocks panel [188 \(UG\)](#), [301 \(CmdRef\)](#)
 I/O pad type [193 \(UG\)](#)
 I/O Standards panel [189 \(UG\)](#), [314 \(CmdRef\)](#)
 Inputs/Outputs panel [189 \(UG\)](#), [306 \(CmdRef\)](#)
 multicycle paths [203 \(UG\)](#)
 pipelining attribute [539 \(UG\)](#)
 Registers panel [189 \(UG\)](#), [309 \(CmdRef\)](#)
 setting compile point constraints [616 \(UG\)](#)
 setting constraints (FDC) [182 \(UG\)](#)
 specifying constraints [188 \(UG\)](#)
 specifying RLOCs [2099 \(Ref\)](#), [2134 \(Ref\)](#), [2136 \(Ref\)](#)
 state machine attributes [503 \(UG\)](#)
 TCL View [189 \(UG\)](#), [319 \(CmdRef\)](#)

SCOPE editor
 using [182 \(UG\)](#)

SCOPE panels
 entering and editing constraints [188 \(UG\)](#)

SCOPE spreadsheet
 Attributes panel [3372 \(AttrRef\)](#)

- popup menu commands [606 \(CmdRef\)](#)
- starting [294 \(CmdRef\)](#)
- SCOPE TCL View
 - using [194 \(UG\)](#)
- SCOPE timing constraints summary [295 \(CmdRef\)](#)
- sdc
 - converting from Xilinx ucf [257 \(UG\)](#)
 - fdc precedence [1370 \(Ref\)](#)
 - SCOPE for legacy files [1374 \(Ref\)](#)
 - standard sdc collection commands [282 \(CmdRef\)](#)
- SDC constraints
 - from Intel QSF [1382 \(Ref\)](#)
- sdc constraints
 - manually converting UCF [253 \(UG\)](#)
- sdc file
 - difference between legacy and Synopsys standard [1369 \(Ref\)](#)
 - translated UCF constraint examples [1386 \(Ref\)](#)
- sdc2fdc utility [1376 \(Ref\)](#), [147 \(CmdRef\)](#)
- search
 - browsing objects with the Find command [410 \(UG\)](#)
 - browsing with the Hierarchy Browser [345 \(UG\)](#), [409 \(UG\)](#)
 - finding objects on current sheet [411 \(UG\)](#)
 - setting limit for results [413 \(UG\)](#)
 - setting scope [412 \(UG\)](#)
 - using the Find command in HDL Analyst views [411 \(UG\)](#)
- search in Analyst
 - browsing objects with the Find command [350 \(UG\)](#)
- Search SolvNet
 - using [1292 \(Ref\)](#)
- searching [40 \(DebugRef\)](#)
- searchpath command [61 \(DebugRef\)](#)
- SEC_DED [3657 \(AttrRef\)](#)
- SEC-DED
 - double-bit error detection [915 \(UG\)](#)
 - single-bit error correction [915 \(UG\)](#)
- secure core flow
 - synthesis [737 \(UG\)](#)
- See also* search
- Select All command [403 \(CmdRef\)](#)
- Select All States command [418 \(CmdRef\)](#)
- Select in Analyst command [608 \(CmdRef\)](#)
- Select Net Driver command
 - current level [545 \(CmdRef\)](#)
 - hierarchical [545 \(CmdRef\)](#)
- Select Net Instances command
 - current level [545 \(CmdRef\)](#)
 - hierarchical [545 \(CmdRef\)](#)
- Select Net Instances command (Physical Analyst) [1063 \(UG\)](#)
- Select Place & Route option file dialog box [628 \(CmdRef\)](#)
- select RAM
 - initializing [2117 \(Ref\)](#)
- Selected command [418 \(CmdRef\)](#)
- Selected Name Support (SNS), VHDL [328 \(HDLRef\)](#)
- selecting
 - text column (Text Editor) [1286 \(Ref\)](#)
- selecting multiple objects using the Ctrl key [1295 \(Ref\)](#)
- selecting objects (Physical Analyst) [1035 \(UG\)](#)
- Send Crossprobes when selecting command [1052 \(UG\)](#)
- sensitivity list (VHDL) [312 \(HDLRef\)](#)
- separator
 - hierarchy [14 \(DebugRef\)](#)
 - path [12 \(DebugRef\)](#)
- sequential elements
 - naming [389 \(CmdRef\)](#)
- sequential logic
 - SystemVerilog
 - sequential logic [227 \(HDLRef\)](#)
 - VHDL
 - examples [404 \(HDLRef\)](#)
- sequential logic (Verilog) [106 \(HDLRef\)](#)
- sequential logic (VHDL) [325 \(HDLRef\)](#)
- sequential optimization, preventing with syn_preserve [3833 \(AttrRef\)](#)
- sequential optimizations
 - disabling [1844 \(Ref\)](#), [1847 \(Ref\)](#), [168 \(CmdRef\)](#)
 - disabling (Intel) [1839 \(Ref\)](#)
 - disabling (Xilinx) [2141 \(Ref\)](#)

sequential shift components

- Altshift_tap [515 \(UG\)](#)
- mapping [515 \(UG\)](#)
- SRL16 primitives [515 \(UG\)](#)
- Verilog [520 \(UG\)](#)
- VHDL [519 \(UG\)](#)

sequential shift components *See* shift registers

sequential shifters

- UPF retention strategy [1220 \(UG\)](#)

server configuration [62 \(DebugRef\)](#)

SET (single event transient) fault [869 \(UG\)](#)

set and reset signals (VHDL) [353 \(HDLRef\)](#)

set command

- collections [222 \(UG\)](#)

Set Library command [424 \(CmdRef\)](#)

set modules command (collections) [305 \(CmdRef\)](#)

set modules_copy command (collections) [305 \(CmdRef\)](#)

Set Slack Margin command [549 \(CmdRef\)](#)

Set VHDL Library command [424 \(CmdRef\)](#)

set_case_analysis timing constraint [351 \(CmdRef\)](#)

set_clock_groups timing constraint [353 \(CmdRef\)](#)

set_clock_latency timing constraint [360 \(CmdRef\)](#)

set_clock_route_delay timing constraint [362 \(CmdRef\)](#)

set_clock_uncertainty timing constraint [363 \(CmdRef\)](#)

set_datapathonly_delay timing constraint [365 \(CmdRef\)](#)

set_false_path timing constraint [368 \(CmdRef\)](#)

set_hierarchy_separator command [389 \(CmdRef\)](#)

set_input_delay timing constraint [371 \(CmdRef\)](#)

set_isolation Tcl command [726 \(CmdRef\)](#)

set_isolation_control Tcl command [730 \(CmdRef\)](#)

set_max_delay timing constraint [374 \(CmdRef\)](#)

set_min_delay constraint [377 \(CmdRef\)](#)

set_multicycle_path timing constraint [380 \(CmdRef\)](#)

set_option

- Resolve Multiple Drivers [182 \(CmdRef\)](#)

set_option command [101 \(UG\)](#)

- Intel description [1853 \(Ref\)](#)

- Intel MAX device syntax [1852 \(Ref\)](#)

- Intel MAX II and APEX device syntax [1849 \(Ref\)](#)

- Intel MAX II and APEX synthesis syntax [1849 \(Ref\)](#)

- Intel MAX synthesis syntax [1852 \(Ref\)](#)

- Intel Stratix, Cyclone, and Arria device syntax [1845 \(Ref\)](#)

- Intel Stratix, Cyclone, and Arria synthesis syntax [1846 \(Ref\)](#)

set_option Tcl command [149 \(CmdRef\)](#)

set_output_delay timing constraint [384 \(CmdRef\)](#)

set_reg_input_delay timing constraint [387 \(CmdRef\)](#)

set_reg_output_delay timing constraint [388 \(CmdRef\)](#)

set_retention Tcl command [733 \(CmdRef\)](#)

set_retention_control Tcl command [735 \(CmdRef\)](#)

set_rtl_ff_names [1378 \(Ref\)](#)

set_rtl_ff_names command [389 \(CmdRef\)](#)

set_scope Tcl command [736 \(CmdRef\)](#)

set/reset priority (Microsemi) [3843 \(AttrRef\)](#)

sets and resets

- VHDL [353 \(HDLRef\)](#)

sets and resets (Verilog) [110 \(HDLRef\)](#)

settings

- cable [39 \(DebugRef\)](#)

- JTAG chain [4280 \(DebugUG\)](#), [48 \(DebugRef\)](#)

- reporting option [87 \(CmdRef\)](#)

- sample clock [21 \(DebugRef\)](#)

- sample depth [20 \(DebugRef\)](#)

SEU (single event upset) fault [869 \(UG\)](#)

sfp file

- logic synthesis [19 \(UG\)](#)

sheet connectors [1331 \(Ref\)](#), [591 \(CmdRef\)](#)

navigating with [397 \(UG\)](#)

sheet size

setting number of objects [398 \(UG\)](#)

schematic view

setting preferences (New Analyst) [334 \(UG\)](#)

Shift key [1298 \(Ref\)](#)

shift register lookup table. *See* sequential shift components

shift registers

inferring [515 \(UG\)](#)

Intel definition [1778 \(Ref\)](#)

Shift-F3 key

Message Viewer [285 \(UG\)](#)

shortcuts

keyboard

See keyboard shortcuts

Show All Hier Pins command [551 \(CmdRef\)](#)

Show All Regions command [662 \(CmdRef\)](#)

Show Cell Interior option [431 \(UG\)](#)

Show command [662 \(CmdRef\)](#)

Show Compile Points command [617 \(CmdRef\)](#)

Show Context command [550 \(CmdRef\)](#)

different from Expand [433 \(UG\)](#)

using [433 \(UG\)](#)

Show Critical Path command [549 \(CmdRef\)](#)

Show Replicated Assignments command [667 \(CmdRef\)](#), [668 \(CmdRef\)](#)

Show Selected command [662 \(CmdRef\)](#)

Show Timing Information command [549 \(CmdRef\)](#)

sign casting [161 \(HDLRef\)](#)

signal assignments

Verilog, always blocks [107 \(HDLRef\)](#)

VHDL

conditional [323 \(HDLRef\)](#)

simple and selected [322 \(HDLRef\)](#)

signal assignments (VHDL) [292 \(HDLRef\)](#)

concurrent [321 \(HDLRef\)](#)

signal flow (Physical Analyst) [1035 \(UG\)](#)

displaying [1035 \(UG\)](#)

Signal Flow command [1035 \(UG\)](#)

signal pins (Physical Analyst)

displaying [1032 \(UG\)](#), [1688 \(Ref\)](#)

signal values

displaying multiple [4296 \(DebugUG\)](#), [4297 \(DebugUG\)](#)

signals

disabling sampling [4218 \(DebugUG\)](#)

exporting trigger [4308 \(DebugUG\)](#), [27 \(DebugRef\)](#)

folded [4296 \(DebugUG\)](#)

instance selection [4224 \(DebugUG\)](#)

listing available [10 \(DebugRef\)](#), [19 \(DebugRef\)](#)

listing instrumented [10 \(DebugRef\)](#), [19 \(DebugRef\)](#)

multiply instrumented [4296 \(DebugUG\)](#), [4297 \(DebugUG\)](#)

partially instrumented [4297 \(DebugUG\)](#)

sampling selection [4216 \(DebugUG\)](#), [4217 \(DebugUG\)](#), [4223 \(DebugUG\)](#), [4226 \(DebugUG\)](#), [4228 \(DebugUG\)](#), [4231 \(DebugUG\)](#), [10 \(DebugRef\)](#), [19 \(DebugRef\)](#)

status [84 \(DebugRef\)](#)

threading with hyper source. *See* hyper source

signals command

debug logic [66 \(DebugRef\)](#)

signed arithmetic (VHDL) [289 \(HDLRef\)](#)

signed functions [58 \(HDLRef\)](#)

signed multipliers (Verilog) [88 \(HDLRef\)](#)

signed signals, Verilog 2001 [42 \(HDLRef\)](#), [61 \(HDLRef\)](#)

SIMBUF macro [1986 \(Ref\)](#)

SIMD mode

using `syn_dspstyle` attribute [3595 \(AttrRef\)](#)

simple component instantiation (VHDL) [326 \(HDLRef\)](#)

simple gates, Verilog [17 \(HDLRef\)](#)

simple signal assignments, VHDL [322 \(HDLRef\)](#)

simple triggering [23 \(DebugRef\)](#)

simulation

using enumerated types, VHDL [362 \(HDLRef\)](#)

simulation mismatches

`full_case` directive [3438 \(AttrRef\)](#)

simulation, effect of retiming [546 \(UG\)](#)
 single-port RAM examples [1465 \(Ref\)](#)
 single-port RAMs
 SYNCore parameters [1592 \(Ref\)](#)
 site columns
 properties (Physical Analyst) [1041 \(UG\)](#)
 sites (Physical Analyst) [1688 \(Ref\)](#)
 properties [1041 \(UG\)](#)
 size casting [161 \(HDLRef\)](#)
 sizeof_collection command [291 \(CmdRef\)](#)
 slack [458 \(UG\)](#)
 cross-clock paths [1434 \(Ref\)](#)
 defined [1429 \(Ref\)](#)
 margin
 definition [1363 \(Ref\)](#)
 setting [1362 \(Ref\)](#), [549 \(CmdRef\)](#)
 setting margins [455 \(UG\)](#)
 slack margin [534 \(CmdRef\)](#)
 Slack Map
 Physical Analyst [1074 \(UG\)](#)
 slack time display [452 \(UG\)](#)
 slice_primitive command [1014 \(UG\)](#)
 slice_primitive Tcl command [195 \(CmdRef\)](#)
 Slow property [392 \(UG\)](#)
 SLR (Super Logic Regions) [2059 \(Ref\)](#)
 SmartGuide flow [1117 \(UG\)](#)
 SNS (Selected Name Support), VHDL [330 \(HDLRef\)](#)
 constants [328 \(HDLRef\)](#)
 demand loading [333 \(HDLRef\)](#)
 functions and operators [329 \(HDLRef\)](#)
 user-defined function support [331 \(HDLRef\)](#)
 SoC [1185 \(UG\)](#)
 SolvNet
 search [1292 \(Ref\)](#)
 SolvNet Support command [598 \(CmdRef\)](#)
 SOPC Builder
 importing embedded systems [685 \(UG\)](#)
 SOPC2Syn [1380 \(Ref\)](#), [197 \(CmdRef\)](#)
 source code
 adding pipelining attribute [539 \(UG\)](#)
 commenting with synthesis on/off [114 \(UG\)](#)
 crossprobing from Tcl window [428 \(UG\)](#)
 defining FSMs [501 \(UG\)](#)
 fixing errors [52 \(UG\)](#)
 opening automatically to crossprobe [425 \(UG\)](#)
 optimizing [532 \(UG\)](#)
 specifying RLOCs [2099 \(Ref\)](#), [2134 \(Ref\)](#), [2136 \(Ref\)](#)
 source command [71 \(DebugRef\)](#)
 source files
 See also Verilog, VHDL.
 See also files
 adding comments [51 \(UG\)](#)
 adding files [80 \(UG\)](#)
 adding to VHDL design library [300 \(HDLRef\)](#)
 checking [48 \(UG\)](#)
 column editing [51 \(UG\)](#)
 copying [4313 \(DebugUG\)](#)
 copying examples from PDF [51 \(UG\)](#)
 creating [36 \(UG\)](#), [1299 \(Ref\)](#)
 crossprobing [425 \(UG\)](#), [426 \(UG\)](#)
 crossprobing to Physical Analyst [1054 \(UG\)](#)
 editing [50 \(UG\)](#)
 editing operations [50 \(UG\)](#)
 encrypting [31 \(DebugRef\)](#)
 mixed language [59 \(UG\)](#)
 specifying default encoding style [113 \(UG\)](#)
 specifying top level file for mixed language projects [60 \(UG\)](#)
 specifying top-level file [113 \(UG\)](#)
 state machine attributes [503 \(UG\)](#)
 using bookmarks [51 \(UG\)](#)
 special characters
 Tcl collections [220 \(UG\)](#)
 spy_glass Tcl command [201 \(CmdRef\)](#)
 SpyGlass tool [71 \(UG\)](#)
 spy_glass Tcl command [201 \(CmdRef\)](#)
 srd file [1417 \(Ref\)](#)
 SRL tables (Xilinx) [2086 \(Ref\)](#)
 SRLs *See* shift registers
 srm file [1417 \(Ref\)](#), [1419 \(Ref\)](#)
 hidden logic not saved [552 \(CmdRef\)](#)
 srp file [1417 \(Ref\)](#), [543 \(CmdRef\)](#)
 srr file [1421 \(Ref\)](#)
 See log file
 watching selected information [1276 \(Ref\)](#)

- srs file [1417 \(Ref\)](#)
 - hidden logic not saved
 - initial values (Verilog) [1539 \(Ref\)](#)
- STA [460 \(UG\)](#)
- STA, generating custom timing reports [460 \(UG\)](#)
- STA, using analysis design constraints (adc) [463 \(UG\)](#)
- stability latches
 - ICG [838 \(UG\)](#)
- Stacked Silicon Interconnect
 - Xilinx technology [2059 \(Ref\)](#)
- stand-alone timing analyst. *See* STA
- standard IEEE package (VHDL) [301 \(HDLRef\)](#)
- standards, supported
 - Verilog [1408 \(Ref\)](#)
 - VHDL [1407 \(Ref\)](#)
- Start Design Manager command [569 \(CmdRef\)](#)
- Start Floorplanner command [569 \(CmdRef\)](#)
- Start ISE Project Navigator command [569 \(CmdRef\)](#)
- start/end points
 - Timing Report panel, Implementation Options dialog box [456 \(CmdRef\)](#)
- starting Synplify [5 \(UG\)](#)
- starting Synplify Premier [5 \(UG\)](#)
- starting Synplify Premier DP [5 \(UG\)](#)
- starting Synplify Pro [5 \(UG\)](#)
- startup block (Xilinx) [2104 \(Ref\)](#)
- startup blocks
 - Xilinx [4141 \(AttrRef\)](#)
- state machines
 - See also* FSM Compiler, FSM Explorer, FSM viewer, FSMs.
 - See also* FSM Compiler, FSM viewer, FSMs.
 - asynchronous
 - Verilog [121 \(HDLRef\)](#)
 - VHDL [353 \(HDLRef\)](#)
 - attributes [503 \(UG\)](#)
 - configuring [72 \(DebugRef\)](#)
 - descriptions in log file [565 \(UG\)](#)
 - displaying in FSM viewer [553 \(CmdRef\)](#)
 - encoding
 - displaying [1327 \(Ref\)](#), [612 \(CmdRef\)](#)
 - FSM Compiler [563 \(UG\)](#)
 - FSM Explorer [567 \(UG\)](#), [1316 \(Ref\)](#)
 - syn_encoding attribute
 - Verilog** [117 \(HDLRef\)](#)
 - VHDL** [358 \(HDLRef\)](#)
 - encoding file (.fse) [1414 \(Ref\)](#)
 - enumerated type, VHDL [361 \(HDLRef\)](#)
 - enumerated types [3631 \(AttrRef\)](#)
 - extracting [3985 \(AttrRef\)](#), [4005 \(AttrRef\)](#)
 - filtering states and transitions [1327 \(Ref\)](#), [418 \(CmdRef\)](#)
 - implementation [565 \(UG\)](#)
 - operators [73 \(DebugRef\)](#)
 - optimization [563 \(UG\)](#)
 - parameter and 'define comparison [502 \(UG\)](#)
 - state encoding, displaying [1327 \(Ref\)](#)
 - SystemVerilog example with enumerated types [149 \(HDLRef\)](#)
 - triggering [4320 \(DebugUG\)](#), [47 \(DebugRef\)](#), [24 \(DebugRef\)](#)
 - UPF retention strategy [1218 \(UG\)](#)
 - Verilog [119 \(HDLRef\)](#), [120 \(HDLRef\)](#)
- state machines (Verilog) [116 \(HDLRef\)](#)
- state machines (VHDL) [357 \(HDLRef\)](#)
- state values (FSM), Verilog [120 \(HDLRef\)](#)
- statemachine command [72 \(DebugRef\)](#), [36 \(DebugRef\)](#)
- state-machine triggering [23 \(DebugRef\)](#)
- statemachine.info file [449 \(UG\)](#)
- static casting [161 \(HDLRef\)](#)
- Status Bar command [415 \(CmdRef\)](#), [14 \(DebugRef\)](#)
- status bar information, HDL Analyst tool [1330 \(Ref\)](#)
- status reporting [84 \(DebugRef\)](#)
- status_report Tcl command [202 \(CmdRef\)](#)
- std IEEE library (VHDL) [301 \(HDLRef\)](#)
- std_logic_1164 IEEE package (VHDL) [301 \(HDLRef\)](#)
- std_logic_arith IEEE package (VHDL) [302 \(HDLRef\)](#)
- std_logic_signed IEEE package (VHDL) [302 \(HDLRef\)](#)

std_logic_unsigned IEEE package (VHDL) [302 \(HDLRef\)](#)

stop command [80 \(DebugRef\)](#), [84 \(DebugRef\)](#)

stopping a synthesis run [505 \(CmdRef\)](#)

Stratix [1843 \(Ref\)](#)

- companion parts [1838 \(Ref\)](#)
- core voltage for Stratix III [1838 \(Ref\)](#)
- device options [1843 \(Ref\)](#)
- file format options [1846 \(Ref\)](#)
- set_option device options [1845 \(Ref\)](#)
- set_option synthesis options [1846 \(Ref\)](#)

streaming operator

- SystemVerilog [197 \(HDLRef\)](#)

structural designs, Verilog [126 \(HDLRef\)](#)

structural netlist file (.vhm) [1420 \(Ref\)](#)

structural netlist file (.vm) [1420 \(Ref\)](#)

Structural Verilog flow [66 \(UG\)](#)

sub-projects

- creating [127 \(UG\)](#)
- linking updates to top level [129 \(UG\)](#)
- multiple implementations [145 \(UG\)](#)
- synchronizing device options with top level [159 \(UG\)](#)

subprojects

- block-based [127 \(UG\)](#)
- compiling [141 \(UG\)](#)
- differences between instance-based and block-based [126 \(UG\)](#)
- generating port context [154 \(UG\)](#)
- instance-based [130 \(UG\)](#)
- nested [138 \(UG\)](#)

subtractor

- SYNCore [1640 \(Ref\)](#)

subtractors

- SYNCore [1641 \(Ref\)](#)

summary of compile points report

- log file (.srr) [1425 \(Ref\)](#)

Super Logic Regions [2059 \(Ref\)](#)

supported language constructs (Verilog) [14 \(HDLRef\)](#)

supported language constructs (VHDL) [284 \(HDLRef\)](#)

supported standards

- Verilog [1408 \(Ref\)](#)
- VHDL [1407 \(Ref\)](#)

sxml2pxml Tcl command

- using the standalone XML converter [213 \(CmdRef\)](#)

symbol conventions [15 \(DebugRef\)](#)

symbols

- enabling name display [590 \(CmdRef\)](#)
- finding by name [402 \(CmdRef\)](#), [686 \(CmdRef\)](#)
- Hierarchy Browser (legend) [1325 \(Ref\)](#)

symmetric rounding

- DSP48 blocks [2069 \(Ref\)](#)

syn_allow_retiming

- using for retiming [542 \(UG\)](#)

syn_allow_retiming attribute [3461 \(AttrRef\)](#)

syn_allowed_resources

- compile points [618 \(UG\)](#)

syn_append_submodules directive [3491 \(AttrRef\)](#)

syn_assign_to_region attribute [3493 \(AttrRef\)](#)

syn_assign_to_slr attribute [3495 \(AttrRef\)](#)

syn_async_reg attribute [3499 \(AttrRef\)](#)

syn_auto_insert_bufg attribute [3503 \(AttrRef\)](#)

syn_black_box

- instantiating LPMs (Intel) [522 \(UG\)](#)

syn_black_box directive [3511 \(AttrRef\)](#)

syn_clean_reset attribute [3523 \(AttrRef\)](#)

syn_clock_gmux_proxy attribute [3527 \(AttrRef\)](#)

syn_clock_priority attribute [3531 \(AttrRef\)](#)

syn_connect [207 \(CmdRef\)](#)

syn_connect_hrefs directive [3535 \(AttrRef\)](#)

syn_cp_use_fast_synthesis attribute [3543 \(AttrRef\)](#)

syn_create_err_net [208 \(CmdRef\)](#)

syn_diff_io attribute [3545 \(AttrRef\)](#)

syn_direct_enable attribute [3551 \(AttrRef\)](#)

syn_direct_reset Attribute [3557 \(AttrRef\)](#)

syn_direct_set attribute [3563 \(AttrRef\)](#)

syn_disable_purifyclock attribute [3569 \(AttrRef\)](#)

syn_dont_infer_iddr attribute [3577 \(AttrRef\)](#)

`syn_donot_infer_oddr` attribute 3573 (AttrRef), 3577 (AttrRef)

`syn_dspstyle` 3581 (AttrRef)

`syn_dspstyle` attribute 3581 (AttrRef)
inferring wide adders/subtractors 2106 (Ref)
using SIMD mode 3595 (AttrRef)

`syn_edif_bit_format` attribute 2108 (Ref), 3617 (AttrRef)

`syn_edif_name_length` attribute 3601 (AttrRef)

`syn_edif_scalar_format` attribute 2108 (Ref), 3605 (AttrRef)

`syn_encoding`
compared with `syn_enum_encoding` directive 3632 (AttrRef)
using with `enum_encoding` 3633 (AttrRef)

`syn_encoding` attribute 504 (UG), 3621 (AttrRef)
FSM encoding style
Verilog 117 (HDLRef)
VHDL 358 (HDLRef)

`syn_enum_encoding`
using with `enum_encoding` 3633 (AttrRef)

`syn_enum_encoding` directive 3631 (AttrRef)
compared with `syn_encoding` attribute 3632 (AttrRef)
FSM encoding 505 (UG)
not for FSM encoding 359 (HDLRef)

`syn_fast_auto` attribute 3637 (AttrRef)

`syn_force_pad` attribute
using 560 (UG), 1973 (Ref)

`syn_force_pads` attribute 3645 (AttrRef)

`syn_force_seq_prim` directive 3649 (AttrRef)

`syn_forward_io_constraints`
effect on forward-annotation (Intel) 1876 (Ref)

`syn_forward_io_constraints` attribute 3653 (AttrRef)

`syn_fsm_correction` 3657 (AttrRef)
distributed TMR 871 (UG)

`syn_fsm_correction` directive 3657 (AttrRef)

`syn_gatedclk_clock_en` directive 3663 (AttrRef)

`syn_gatedclk_clock_en_polarity` directive 3667 (AttrRef)

`syn_global_buffers`
and `xc_global_buffers` 3674 (AttrRef)

`syn_global_buffers` attribute 3673 (AttrRef)

`syn_hier` attribute 3681 (AttrRef)
and `xc_use_keep_hierarchy` 4182 (AttrRef)
controlling flattening 553 (UG)
Intel Quartus II Incremental Compilation flow 1091 (UG)
preserving hierarchy 553 (UG)
using with compile points 617 (UG)

`syn_highrel_ioconnector`
using 899 (UG)

`syn_highrel_ioconnector` attribute 3691 (AttrRef)

`syn_insert_buffer` attribute 3701 (AttrRef)
BUFGMUX 2128 (Ref)

`syn_insert_pad` attribute 3713 (AttrRef)

`syn_isclock`
black box clock pins 500 (UG)

`syn_isclock` directive 3717 (AttrRef)

`syn_keep`
compared with `syn_preserve` and `syn_noprune` directives 3723 (AttrRef)
DSP block inference, Intel 1813 (Ref)
inferring Intel shift registers 516 (UG)
inferring Lattice PICs 1967 (Ref)
replicating redundant logic 550 (UG)

`syn_keep` attribute
preserving nets 549 (UG)
preserving shared registers 549 (UG)

`syn_keep` directive 3721 (AttrRef)
effect on buffering 557 (UG)

`syn_loc` attribute 3729 (AttrRef)
translating Intel QSF constraints 1383 (Ref)

`syn_looplmit` directive 3735 (AttrRef)

`syn_macro`
specifying encrypted IP as white box 647 (UG)
white-boxing non-secure cores 737 (UG)

`syn_macro` directive 3737 (AttrRef)

`syn_map_dffrs` attribute 3743 (AttrRef)

`syn_max_memsized_reg` attribute 3749 (AttrRef)

`syn_maxfan`
fanout limits (Microsemi) 2026 (Ref)

`syn_maxfan` attribute 3755 (AttrRef)
Intel 1840 (Ref)
setting fanout limits 555 (UG)
Xilinx buffers 558 (UG)
Xilinx designs 2139 (Ref)

`syn_modify_ram_contents` attribute 3867 (AttrRef)

`syn_multstyle`
DSP block inference, Intel 1813 (Ref)

`syn_multstyle` attribute 3763 (AttrRef)

`syn_netlist_hierarchy` attribute 3775 (AttrRef)

`syn_no_compile_point` attribute 3783 (AttrRef)

`syn_noarrayports` attribute 3787 (AttrRef)
use with `alspin` 2044 (Ref)

`syn_noclockbuf` attribute 3791 (AttrRef)
using with fanout guides 3756 (AttrRef)

`syn_noclockpad` attribute 3797 (AttrRef)

`syn_noprune` directive 3803 (AttrRef)
inferring Intel shift registers 516 (UG)
preserving instances 549 (UG)

`syn_pad_type` attribute 3821 (AttrRef)

`syn_pipeline` attribute 539 (UG)

`syn_preserve`
compared with `syn_keep` and `syn_noprune` 3834 (AttrRef)
DSP block inference, Intel 1813 (Ref)
effect on buffering 557 (UG)
preserving power-on for retiming 543 (UG)
preserving registers with INIT values 2117 (Ref)

`syn_preserve` directive 3833 (AttrRef)
preserving FSMs from optimization 503 (UG)
preserving logic 549 (UG)

`syn_preserve_sr_priority` attribute (Microsemi) 3843 (AttrRef)

`syn_probe` attribute 570 (UG), 3849 (AttrRef)
inserting probes 570 (UG)
preserving nets 549 (UG)

`syn_radhardlevel` 3857 (AttrRef)
distributed DWC 895 (UG)
distributed TMR 871 (UG), 902 (UG), 947 (UG)
Intel and Xilinx options 3858 (AttrRef)
Intel and Xilinx syntax 3859 (AttrRef)
TMR. *See* TMR, distributed TMR

`syn_radhardlevel` attribute
TMR 3857 (AttrRef)

`syn_ram_write_mem` attribute 3867 (AttrRef)

`syn_ramstyle` attribute 3871 (AttrRef)

`syn_reduce_controlset_size` (Achronix) 3901 (AttrRef)

`syn_reduce_controlset_size` attribute (Lattice, Xilinx) 3887 (AttrRef)

`syn_reference_clock` attribute 3907 (AttrRef)
effect on multiple I/O constraints 309 (CmdRef)

`syn_reference_clock` constraint (Legacy) 227 (UG)

`syn_register_correction` attribute 3911 (AttrRef)

`syn_rename_module` directive 3917 (AttrRef)

`syn_replicate`
using with fanout guides 3756 (AttrRef)

`syn_replicate` attribute 3919 (AttrRef)
Intel fanouts 1840 (Ref)
using buffering 557 (UG)

`syn_resources` attribute 3925 (AttrRef)

`syn_romstyle` attribute 3939 (AttrRef), 3948 (AttrRef)

`syn_rw_conflict_logic` attribute 3953 (AttrRef)

`syn_safe_case` directive 3961 (AttrRef)

`syn_safefsm_pipe` directive 3965 (AttrRef)

`syn_sharing` directive 3969 (AttrRef)
overriding default 560 (UG)

`syn_shift_resetphase` 3975 (AttrRef)

`syn_slow` attribute 3981 (AttrRef)

`syn_smhigh effort` attribute 3985 (AttrRef)

`syn_srl_mindepth` attribute 3991 (AttrRef)

`syn_srlstyle` attribute 3995 (AttrRef)

altshift_tap [515 \(UG\)](#)
 mapping sequential shift components to registers [515 \(UG\)](#)
 setting shift register style [515 \(UG\)](#)
 syn_state_machine attribute [3985 \(AttrRef\)](#)
 syn_state_machine directive [4005 \(AttrRef\)](#)
 using with value=0 [566 \(UG\)](#)
 syn_sxaml2pxml Tcl command [213 \(CmdRef\)](#)
 SYN_TCL_HOOKS environment variable [772 \(UG\)](#)
 SYN_TCL_HOOKS variable [774 \(UG\)](#)
 syn_tco attribute
 adding in SCOPE [499 \(UG\)](#)
 syn_tco directive [498 \(UG\)](#), [4013 \(AttrRef\)](#)
 adding black box constraints [497 \(UG\)](#)
 syn_tpd attribute
 adding in SCOPE [499 \(UG\)](#)
 syn_tpd directive [498 \(UG\)](#), [4019 \(AttrRef\)](#)
 adding black box constraints [497 \(UG\)](#)
 black-box timing [4019 \(AttrRef\)](#), [4037 \(AttrRef\)](#)
 syn_trigger_utils.tcl file [74 \(DebugRef\)](#)
 syn_tristate directive [4025 \(AttrRef\)](#)
 syn_tristatetomux attribute [4029 \(AttrRef\)](#)
 effect of tristate pushing [469 \(CmdRef\)](#)
 syn_tsu attribute
 adding in SCOPE [499 \(UG\)](#)
 syn_tsu directive [498 \(UG\)](#), [4037 \(AttrRef\)](#)
 adding black box constraints [497 \(UG\)](#)
 black-box timing [4037 \(AttrRef\)](#)
 syn_unconnected_inputs attribute [4043 \(AttrRef\)](#)
 syn_unique_inst_module directive [4053 \(AttrRef\)](#)
 syn_use_carry_chain attribute [4059 \(AttrRef\)](#)
 using [1931 \(Ref\)](#)
 syn_useenables attribute [4073 \(AttrRef\)](#)
 syn_useioff
 DSP block inference, Intel [1813 \(Ref\)](#)
 preventing flops from moving during retiming [543 \(UG\)](#)
 syn_useioff attribute
 inferring Intel shift registers [516 \(UG\)](#)
 Intel [4079 \(AttrRef\)](#)
 packing registers (Intel) [1865 \(Ref\)](#)
 packing registers (Xilinx) [2119 \(Ref\)](#)
 syn_user_instance
 comparison with syn_macro [3740 \(AttrRef\)](#)
 syn_user_instance attribute [4095 \(AttrRef\)](#)
 syn_vote_loops Attribute [4101 \(AttrRef\)](#)
 syn_vote_register Attribute [4105 \(AttrRef\)](#)
 syn_vote_register attribute [4105 \(AttrRef\)](#)
 synchronous FSM from concurrent assignment statement (VHDL) [364 \(HDLRef\)](#)
 synchronous sets and resets
 Verilog [112 \(HDLRef\)](#)
 synchronous sets and resets (VHDL) [354 \(HDLRef\)](#)
 synchronous sets/resets
 inferring registers with (Intel) [1778 \(Ref\)](#)
 Xilinx [2080 \(Ref\)](#)
 SYNCore
 adder/subtractor [1640 \(Ref\)](#)
 adder/subtractor parameters [1649 \(Ref\)](#)
 adders [1641 \(Ref\)](#)
 byte-enable RAM compiler
 byte-enable RAM compiler **SYNCore** [1609 \(Ref\)](#)
 byte-enable RAM parameters [1617 \(Ref\)](#)
 counter compiler [1664 \(Ref\)](#)
 counter parameters [1671 \(Ref\)](#)
 counters [1665 \(Ref\)](#)
 FIFO compiler [1556 \(Ref\)](#), [1557 \(Ref\)](#)
 FIFO parameters [1562 \(Ref\)](#)
 RAM compiler
 RAM compiler **SYNCore** [1587 \(Ref\)](#)
 RAM parameters [1595 \(Ref\)](#)
 RAMs [1587 \(Ref\)](#)
 RAMs, byte-enable [1610 \(Ref\)](#)
 RAMs, dual-port parameters [1593 \(Ref\)](#)
 RAMs, single-port parameters [1592 \(Ref\)](#)
 ROM compiler [1625 \(Ref\)](#)
 ROM parameters [1632 \(Ref\)](#)
 ROMs [1627 \(Ref\)](#)
 ROMs, parameters [1631 \(Ref\)](#)
 subtractors [1641 \(Ref\)](#)
 SYNCore adder/subtractor
 adders [1652 \(Ref\)](#)
 dynamic adder/subtractor [1658 \(Ref\)](#)

functional description [1640 \(Ref\)](#)
subtractors [1655 \(Ref\)](#)

SYNCore FIFOs
definition [1556 \(Ref\)](#)
parameter definitions [1575 \(Ref\)](#)
port list [1572 \(Ref\)](#)
read operations [1572 \(Ref\)](#)
status flags [1577 \(Ref\)](#)
write operations [1571 \(Ref\)](#)

SYNCore ROMs
clock latency [1639 \(Ref\)](#)
dual-port read [1637 \(Ref\)](#)
parameter list [1638 \(Ref\)](#)
single-port read [1636 \(Ref\)](#)

SYNCore wizard [500 \(CmdRef\)](#), [508 \(CmdRef\)](#)

synenc encryption [649 \(UG\)](#)

synhooks
automating message filtering [289 \(UG\)](#)

synhooks.tcl file [772 \(UG\)](#), [774 \(UG\)](#)

Synopsys
FPGA product family [2 \(UG\)](#)

Synopsys customer support, contacting [1254 \(Ref\)](#)

Synopsys FPGA implementation tools
product information [601 \(CmdRef\)](#)

Synopsys FPGA products [601 \(CmdRef\)](#)

Synopsys FPGA Synthesis Tools
overview [1242 \(Ref\)](#)

Synopsys Home Page command [601 \(CmdRef\)](#)

Synopsys standard sdc file. *See* sdc files, difference between legacy and Synopsys standard

Synopsys Training Page command [601 \(CmdRef\)](#)

synplicity.ucf file
non-secure cores [736 \(UG\)](#)
relation to ncf file (Legacy) [248 \(UG\)](#)
secure cores [736 \(UG\)](#)

synplify command-line command [6 \(UG\)](#), [210 \(CmdRef\)](#)

Synplify Premier
list of design flows [18 \(UG\)](#)
logic synthesis flows [18 \(UG\)](#)

synplify premier command-line
command [6 \(UG\)](#), [210 \(CmdRef\)](#)

synplify premier dp command-line
command [6 \(UG\)](#), [210 \(CmdRef\)](#)

Synplify Premier synthesis tool
overview [2 \(UG\)](#)

Synplify Premier/DP
Project view [1256 \(Ref\)](#)

Synplify Premier/DP tools
user interface [1248 \(Ref\)](#)

Synplify Pro synthesis tool
overview [2 \(UG\)](#)

Synplify Pro tool
Project view [1256 \(Ref\)](#)
user interface [1248 \(Ref\)](#)

Synplify tool
Project view [1256 \(Ref\)](#)
user interface [1248 \(Ref\)](#)

synplify_pro command-line command [6 \(UG\)](#), [210 \(CmdRef\)](#)

SYNPLIFY_REMOTE_REPORT_LOCATION [275 \(UG\)](#)

synplify.ucf [258 \(UG\)](#)

synplify.vhd [1763 \(Ref\)](#), [2172 \(Ref\)](#)

syntax
bus dimension separator [390 \(CmdRef\)](#)
bus naming [390 \(CmdRef\)](#)
checking source files [48 \(UG\)](#)

syntax check [48 \(UG\)](#)

Syntax Check command [500 \(CmdRef\)](#)

syntax conventions [11 \(DebugRef\)](#)

syntax restrictions
constant function [86 \(HDLRef\)](#)
multidimensional array [86 \(HDLRef\)](#)

synthesis
attributes and directives (VHDL) [401 \(HDLRef\)](#)
attributes and directives, Verilog [133 \(HDLRef\)](#)
examples, VHDL [403 \(HDLRef\)](#)
guidelines
Verilog [81 \(HDLRef\)](#)
guidelines (VHDL) [339 \(HDLRef\)](#)
hierarchical projects [156 \(UG\)](#)
log file (.srr) [1421 \(Ref\)](#)

- watching selected information [1276 \(Ref\)](#)
 - stopping [505 \(CmdRef\)](#)
 - Xilinx non-secure cores [737 \(UG\)](#)
 - Xilinx secure cores [737 \(UG\)](#)
- synthesis check [48 \(UG\)](#)
- Synthesis Check command [500 \(CmdRef\)](#)
- synthesis jobs
 - monitoring [505 \(CmdRef\)](#)
- synthesis macro, Verilog [128 \(HDLRef\)](#)
- synthesis software
 - flow [7 \(UG\)](#)
 - gui [1248 \(Ref\)](#)
- synthesis strategy
 - Tcl command [175 \(CmdRef\)](#)
 - using [573 \(UG\)](#)
- synthesis_off directive [4112 \(AttrRef\)](#)
- synthesis_off directive, handling [460 \(CmdRef\)](#)
- synthesis_on directive [4112 \(AttrRef\)](#)
- synthesis_on directive, handling [460 \(CmdRef\)](#)
- synthesis_on/off
 - using [114 \(UG\)](#)
- Synthesize command [498 \(CmdRef\)](#)
- synthesizing designs [4232 \(DebugUG\)](#)
- Synthesizing Your Design [262 \(UG\)](#)
- system clock [1430 \(Ref\)](#)
- SystemVerilog [155 \(HDLRef\)](#), [240 \(HDLRef\)](#), [253 \(HDLRef\)](#), [464 \(CmdRef\)](#)
 - .* connection [249 \(HDLRef\)](#)
 - .name connection [248 \(HDLRef\)](#)
 - \$bits system function [262 \(HDLRef\)](#)
 - always_comb [223 \(HDLRef\)](#)
 - always_ff [227 \(HDLRef\)](#)
 - always_latch [225 \(HDLRef\)](#)
 - block name on end [219 \(HDLRef\)](#)
 - constants [176 \(HDLRef\)](#)
 - data objects [175 \(HDLRef\)](#)
 - data types [145 \(HDLRef\)](#)
 - do-while loops [212 \(HDLRef\)](#)
 - enumerated types [148 \(HDLRef\)](#)
 - ignoring code with synthesis_off/on [4112 \(AttrRef\)](#)
 - interface construct [155 \(HDLRef\)](#), [253 \(HDLRef\)](#)
 - keywords [282 \(HDLRef\)](#)

- limitations [141 \(HDLRef\)](#)
 - literals [145 \(HDLRef\)](#)
 - nets [176 \(HDLRef\)](#)
 - operators [186 \(HDLRef\)](#)
 - packages [240 \(HDLRef\)](#)
 - procedural blocks [223 \(HDLRef\)](#)
 - type casting [152 \(HDLRef\)](#)
 - typedef [146 \(HDLRef\)](#)
 - unnamed blocks [219 \(HDLRef\)](#)
 - variables [176 \(HDLRef\)](#)

SystemVerilog keywords
 context help [46 \(UG\)](#), [1287 \(Ref\)](#)

T

- ta file [460 \(UG\)](#)
- ta file (customized timing report) [1419 \(Ref\)](#)
- tables
 - idcode [43 \(DebugRef\)](#)
- TAP controller [4270 \(DebugUG\)](#)
- target device [31 \(DebugRef\)](#)
- task declaration
 - automatic [62 \(HDLRef\)](#)
- Tcl
 - c_diff collection command [241 \(CmdRef\)](#)
 - c_intersect collection command [242 \(CmdRef\)](#)
 - c_list collection command [243 \(CmdRef\)](#)
 - c_print collection command [243 \(CmdRef\)](#)
 - c_symdiff collection command [245 \(CmdRef\)](#)
 - c_union collection command [245 \(CmdRef\)](#)
 - collection commands [240 \(CmdRef\)](#)
 - max_parallel_jobs variable [761 \(UG\)](#)
 - set_modules collection command [247 \(CmdRef\)](#)
 - verilog argument [25 \(CmdRef\)](#)
 - vhdl argument [25 \(CmdRef\)](#)
- Tcl (Tool Command Language) [16 \(CmdRef\)](#), [8 \(DebugRef\)](#)
- tcl argument
 - _include [26 \(CmdRef\)](#)
- tcl callbacks
 - customizing key assignments [773 \(UG\)](#)
- Tcl collection commands [240 \(CmdRef\)](#)

- c_diff [241 \(CmdRef\)](#)
- c_intersect [242 \(CmdRef\)](#)
- c_list [243 \(CmdRef\)](#)
- c_print [243 \(CmdRef\)](#)
- c_symdiff [245 \(CmdRef\)](#)
- c_union [245 \(CmdRef\)](#)
- set_modules [247 \(CmdRef\)](#)
- Tcl collection operators [240 \(CmdRef\)](#)
- Tcl commands
 - add_file [25 \(CmdRef\)](#)
 - add_folder [30 \(CmdRef\)](#)
 - assign_to_region [39 \(CmdRef\)](#)
 - batch script [753 \(UG\)](#)
 - collections [305 \(CmdRef\)](#)
 - constraint files [1373 \(Ref\)](#)
 - constraint_file [45 \(CmdRef\)](#)
 - create_region [48 \(CmdRef\)](#)
 - dh_module_sources [63 \(CmdRef\)](#)
 - generate_instance_constraints [84 \(CmdRef\)](#)
 - get_env [87 \(CmdRef\)](#)
 - get_option [87 \(CmdRef\)](#)
 - hdl_param [89 \(CmdRef\)](#)
 - impl [93 \(CmdRef\)](#)
 - log file commands [216 \(CmdRef\)](#)
 - netlist editing [1148 \(UG\)](#)
 - pasting [1280 \(Ref\)](#)
 - project [111 \(CmdRef\)](#)
 - project_data [120 \(CmdRef\)](#)
 - project_file [121 \(CmdRef\)](#)
 - project_folder [123 \(CmdRef\)](#)
 - running [759 \(UG\)](#)
 - set_option [149 \(CmdRef\)](#)
 - slice_primitive [195 \(CmdRef\)](#)
 - syn_sxml2pxml [213 \(CmdRef\)](#)
 - syntax for Tcl hooks [774 \(UG\)](#)
- Tcl conventions [16 \(CmdRef\)](#), [8 \(DebugRef\)](#)
- Tcl expand
 - using [205 \(UG\)](#)
- Tcl expand command [237 \(CmdRef\)](#)
 - crossprobing objects [216 \(UG\)](#)
 - usage tips [210 \(UG\)](#)
 - using in SCOPE [215 \(UG\)](#)
- Tcl files [759 \(UG\)](#)
 - creating [761 \(UG\)](#)
 - for bottom-up synthesis [765 \(UG\)](#)
 - guidelines [68 \(UG\)](#)
 - naming conventions [69 \(UG\)](#)
 - recording from commands [760 \(UG\)](#)

- synhooks.tcl [772 \(UG\)](#)
- using variables [763 \(UG\)](#)
- wildcards [69 \(UG\)](#)
- Tcl find
 - batch mode [212 \(UG\)](#)
 - filtering results by property [207 \(UG\)](#)
 - search patterns [205 \(UG\)](#)
 - using [205 \(UG\)](#)
- Tcl find command [221 \(CmdRef\)](#)
 - annotating properties [207 \(UG\)](#)
 - case sensitivity [206 \(UG\)](#), [224 \(CmdRef\)](#)
 - crossprobing objects [216 \(UG\)](#)
 - database differences [215 \(UG\)](#)
 - examples [225 \(CmdRef\)](#)
 - object prefixes [223 \(CmdRef\)](#)
 - object types [223 \(CmdRef\)](#)
 - pattern matching [206 \(UG\)](#)
 - regular expression syntax [224 \(CmdRef\)](#)
 - special characters [224 \(CmdRef\)](#)
 - Tcl window vs SCOPE [214 \(UG\)](#)
 - usage tips [209 \(UG\)](#)
 - useful -filter examples [209 \(UG\)](#)
 - using in SCOPE [215 \(UG\)](#)
 - wildcards [224 \(CmdRef\)](#)
- TCL Help command [602 \(CmdRef\)](#), [59 \(DebugRef\)](#)
- Tcl Script
 - Tcl Window command [415 \(CmdRef\)](#), [14 \(DebugRef\)](#)
- Tcl Script window
 - crossprobing [428 \(UG\)](#)
 - message viewer [284 \(UG\)](#)
 - Output Windows [1284 \(Ref\)](#)
- Tcl script window
 - collections compared to SCOPE [214 \(UG\)](#)
- Tcl scripts [71 \(DebugRef\)](#)
 - examples [766 \(UG\)](#)
 - running [501 \(CmdRef\)](#)
 - See Tcl files.
- Tcl shell command
 - sdc2fdc [1376 \(Ref\)](#), [147 \(CmdRef\)](#)
- TCL View [194 \(UG\)](#)
 - using [194 \(UG\)](#)
 - using SCOPE [189 \(UG\)](#)
- TCL View, SCOPE [319 \(CmdRef\)](#)
- Tcl window
 - popup menu [607 \(CmdRef\)](#), [9 \(DebugRef\)](#)
 - popup menu commands [1280 \(Ref\)](#)

- popup menus [1280 \(Ref\)](#)
- Tcl Window command [415 \(CmdRef\)](#), [14 \(DebugRef\)](#)
- tclcmd [752 \(UG\)](#)
- team design. *See* hierarchical projects, hierarchical project management flows
- Technical Resource Center
 - accessing [601 \(CmdRef\)](#)
 - specifying PDF reader (UNIX) [597 \(CmdRef\)](#)
 - specifying web browser (UNIX) [597 \(CmdRef\)](#)
- technologies
 - CPLD (Xilinx) [2161 \(Ref\)](#)
 - Spartan (Xilinx) [2155 \(Ref\)](#)
 - Virtex (Xilinx) [2155 \(Ref\)](#)
- Technology view [1322 \(Ref\)](#)
 - See also* HDL Analyst
 - creating [543 \(CmdRef\)](#)
 - critical paths [455 \(UG\)](#)
 - crossprobing [423 \(UG\)](#), [424 \(UG\)](#)
 - crossprobing collection objects [216 \(UG\)](#)
 - crossprobing from source file [425 \(UG\)](#)
 - displaying [1301 \(Ref\)](#)
 - file (.srm) [1417 \(Ref\)](#), [1419 \(Ref\)](#)
 - filtering [369 \(UG\)](#), [434 \(UG\)](#)
 - finding objects [413 \(UG\)](#)
 - finding objects with Find [411 \(UG\)](#)
 - finding objects with Hierarchy Browser [345 \(UG\)](#), [409 \(UG\)](#)
 - flattening hierarchy [381 \(UG\)](#), [441 \(UG\)](#)
 - general description [387 \(UG\)](#)
 - highlighting collections [221 \(UG\)](#)
 - opening [389 \(UG\)](#)
 - popup menu [641 \(CmdRef\)](#), [10 \(DebugRef\)](#)
 - popup menu commands [641 \(CmdRef\)](#)
 - selecting/deselecting objects [395 \(UG\)](#)
 - setting preferences [398 \(UG\)](#)
 - state machine implementation in [565 \(UG\)](#)
 - traversing hierarchy [401 \(UG\)](#)
- technology view
 - displaying [104 \(CmdRef\)](#)
- template, module (Verilog) [94 \(HDLRef\)](#)
- temporary assigns (Design Planner) [988 \(UG\)](#)
 - drag and drop [988 \(UG\)](#)
 - empty [988 \(UG\)](#)
 - return assignment [988 \(UG\)](#)
- text
 - copying, cutting and pasting [402 \(CmdRef\)](#), [13 \(DebugRef\)](#)
 - replacing [413 \(CmdRef\)](#)
- Text Editor
 - features [1286 \(Ref\)](#)
 - indenting a block of text [1286 \(Ref\)](#)
 - opening [1285 \(Ref\)](#)
 - popup menu commands [607 \(CmdRef\)](#)
 - selecting text column [1286 \(Ref\)](#)
 - view [1284 \(Ref\)](#)
- text editor
 - built-in [50 \(UG\)](#)
 - completing keywords [1286 \(Ref\)](#)
 - external [55 \(UG\)](#)
 - using [50 \(UG\)](#)
- Text Editor view [1284 \(Ref\)](#)
 - crossprobing [424 \(UG\)](#)
- Text Editor window
 - colors [53 \(UG\)](#)
 - crossprobing [53 \(UG\)](#)
 - fonts [53 \(UG\)](#)
- text files
 - crossprobing [426 \(UG\)](#)
- text macro
 - Verilog [129 \(HDLRef\)](#)
- the [95 \(CmdRef\)](#)
- The Synopsys FPGA Product Family [2 \(UG\)](#)
- third-party vendor tools
 - invoking [777 \(UG\)](#)
- through constraints [200 \(UG\)](#)
 - AND lists [201 \(UG\)](#)
 - OR lists [200 \(UG\)](#)
 - point-to-point delays [311 \(CmdRef\)](#)
- through points
 - clocks [337 \(CmdRef\)](#)
 - lists, multiple [333 \(CmdRef\)](#)
 - lists, single [332 \(CmdRef\)](#)
 - multiple [333 \(CmdRef\)](#)
 - product of sums UI [333 \(CmdRef\)](#)
 - single [332 \(CmdRef\)](#)
 - specifying for timing exceptions [332 \(CmdRef\)](#)
 - specifying for timing report [533 \(CmdRef\)](#)
- tie_pin command [772 \(CmdRef\)](#)

time borrowing [1749 \(Ref\)](#)

time stamp, checking on files [85 \(UG\)](#)

time stamps

- Xilinx partition flow [1123 \(UG\)](#)

TimeQuest

- supported constraints for import [701 \(UG\)](#)

TIMESPEC I/O constraint (Xilinx)

- xc_use_timespec_for_io attribute [4187 \(AttrRef\)](#)

timing

- prototypes [1196 \(UG\)](#)
- syn_tco directive [4013 \(AttrRef\)](#)
- syn_tpd directive [4019 \(AttrRef\)](#)
- syn_tsu directive [4037 \(AttrRef\)](#)

timing analysis [452 \(UG\)](#)

timing analysis of critical paths (HDL Analyst tool) [1361 \(Ref\)](#)

timing analysis using STA [460 \(UG\)](#)

timing analyst

- cross-clock paths [1433 \(Ref\)](#)
- generating report [519 \(CmdRef\)](#)

timing analyzer

- wildcards [538 \(CmdRef\)](#)

timing annotated properties (.tap) [1419 \(Ref\)](#)

timing budgeting

- compile points [597 \(UG\)](#)

timing constraints

- checking [500 \(CmdRef\)](#)
- conflict resolution [338 \(CmdRef\)](#)
- constraint priority [338 \(CmdRef\)](#)
- create_clock [343 \(CmdRef\)](#)
- create_generated_clock [345 \(CmdRef\)](#)
- FPGA [342 \(CmdRef\)](#)
- reset_path [349 \(CmdRef\)](#)
- See also FPGA timing constraints
- See constraints
- set_case_analysis [351 \(CmdRef\)](#)
- set_clock_groups [353 \(CmdRef\)](#)
- set_clock_latency [360 \(CmdRef\)](#)
- set_clock_route_delay [362 \(CmdRef\)](#)
- set_clock_uncertainty [363 \(CmdRef\)](#)
- set_datapathonly_delay [365 \(CmdRef\)](#)
- set_false_path [368 \(CmdRef\)](#)
- set_input_delay [371 \(CmdRef\)](#)
- set_max_delay [374 \(CmdRef\)](#)
- set_min_delay [377 \(CmdRef\)](#)
- set_multicycle_path [380 \(CmdRef\)](#)
- set_output_delay [384 \(CmdRef\)](#)
- set_reg_input_delay [387 \(CmdRef\)](#)
- set_reg_output_delay [388 \(CmdRef\)](#)
- translating qsf [699 \(UG\)](#)
- Xilinx output file (Legacy) [248 \(UG\)](#)

timing constraints (Legacy) [227 \(UG\)](#)

timing exceptions

- False Paths panel [328 \(CmdRef\)](#)
- multicycle paths [325 \(CmdRef\)](#)
- priority [338 \(CmdRef\)](#)
- specifying paths/points [328 \(CmdRef\)](#)

timing exceptions, adding constraints after synthesis [464 \(UG\)](#)

timing exceptions, modifying with adc [464 \(UG\)](#)

timing failures [458 \(UG\)](#)

timing failures, definition [1363 \(Ref\)](#)

timing information commands [452 \(UG\)](#)

timing information in HDL views [453 \(UG\)](#)

timing information, critical paths [457 \(UG\)](#)

timing information, displaying (HDL Analyst tool) [549 \(CmdRef\)](#)

timing optimization [534 \(UG\)](#)

timing report [1427 \(Ref\)](#)

- asynchronous clock report [531 \(CmdRef\)](#)
- clock relationships [1433 \(Ref\)](#)
- customized (.ta file) [1419 \(Ref\)](#)
- defining through points [533 \(CmdRef\)](#)
- file (.ta) [1419 \(Ref\)](#), [519 \(CmdRef\)](#)
- header [1428 \(Ref\)](#)
- interface information [1434 \(Ref\)](#)
- performance summary [1428 \(Ref\)](#)
- specifying slack margin [534 \(CmdRef\)](#)
- using path filtering [534 \(CmdRef\)](#)

timing report file

- generating custom [530 \(CmdRef\)](#)
- stand-alone [532 \(CmdRef\)](#)

Timing Report panel

- Implementation Options dialog box [455 \(CmdRef\)](#)
- Number of Critical Paths [456 \(CmdRef\)](#)
- Start/End Points [456 \(CmdRef\)](#)

Timing Report View [475 \(UG\)](#), [520 \(CmdRef\)](#)

- accessing from Project Status View [1270 \(Ref\)](#)
- options [520 \(CmdRef\)](#)
- using [475 \(UG\)](#)
- timing report, stand-alone [460 \(UG\)](#)
- timing reports
 - asynchronous clocks [1435 \(Ref\)](#)
 - file. *See* timing report file
 - filtering [531 \(CmdRef\)](#)
 - log file (.srr) [1425 \(Ref\)](#)
 - parameters [519 \(CmdRef\)](#)
 - specifying format options [108 \(UG\)](#)
 - stand-alone [519 \(CmdRef\)](#)
 - stand-alone (.ta file) [519 \(CmdRef\)](#)
- timing reports, custom [460 \(UG\)](#)
- timing_applied.sdc file [699 \(UG\)](#)
- timing_unapplied.sdc file [699 \(UG\)](#)
- Tip of the Day command [603 \(CmdRef\)](#)
- tips
 - memory usage [445 \(UG\)](#)
- title bar information, HDL Analyst tool [1344 \(Ref\)](#)
- TMR
 - description [869 \(UG\)](#)
 - distributed [871 \(UG\)](#)
 - gate-level netlist [871 \(UG\)](#)
 - local. *See* local TMR [921 \(UG\)](#)
 - Microsemi syn_radhardlevel [3859 \(AttrRef\)](#)
 - physical separation of triplicates [885 \(UG\)](#)
 - physical separation of triplicates using Design Planner. [886 \(UG\)](#)
 - syn_radhardlevel attribute [3857 \(AttrRef\)](#)
 - using [871 \(UG\)](#)
 - using for ECC [921 \(UG\)](#)
 - using for RAM [921 \(UG\)](#)
 - using Identify debug [940 \(UG\)](#)
 - voter insertion examples [873 \(UG\)](#)
- TMR technique [936 \(UG\)](#)
- to constraints
 - specifying [200 \(UG\)](#)
- to points [535 \(CmdRef\)](#)
 - clocks [336 \(CmdRef\)](#)
 - multiple [331 \(CmdRef\)](#)
 - objects [330 \(CmdRef\)](#)
 - Timing Analyzer [535 \(CmdRef\)](#)
- Toggle bookmark command [403 \(CmdRef\)](#)
- tool conventions [12 \(DebugRef\)](#)
- tool tags
 - creating [777 \(UG\)](#)
 - definition [777 \(UG\)](#)
- tool tips
 - Physical Analyst [1041 \(UG\)](#)
- toolbars [1298 \(Ref\)](#), [26 \(DebugRef\)](#)
 - FSM [1302 \(Ref\)](#), [1303 \(Ref\)](#), [30 \(DebugRef\)](#)
 - moving and docking [1298 \(Ref\)](#)
- Toolbars command [415 \(CmdRef\)](#), [14 \(DebugRef\)](#)
- tools
 - invoking Debugger [4282 \(DebugUG\)](#)
- Tools menu [667 \(CmdRef\)](#)
 - commands [667 \(CmdRef\)](#)
- tooltips
 - displaying [419 \(CmdRef\)](#), [15 \(DebugRef\)](#)
- tooltips (Physical Analyst)
 - copying information from [1042 \(UG\)](#)
- top level
 - specifying [113 \(UG\)](#)
- top-down design flow
 - compile point advantages [584 \(UG\)](#)
- top-down hierarchical development flow
 - subprojects [127 \(UG\)](#)
- top-down hierarchical synthesis flow [29 \(UG\)](#)
- top-first hierarchical development flow [25 \(UG\)](#)
- transition watchpoint [13 \(DebugRef\)](#)
- Translate Vendor IO command [499 \(CmdRef\)](#)
- translate_off directive [4111 \(AttrRef\)](#)
- translate_on directive [4111 \(AttrRef\)](#)
- translating constraints [504 \(CmdRef\)](#)
- transparent hierarchical instances [1334 \(Ref\)](#)
 - lower-level logic on multiple sheets [1346 \(Ref\)](#)
 - operations resulting in [1354 \(Ref\)](#)
 - pins and pin names [1337 \(Ref\)](#)
- transparent instances
 - displaying pins [551 \(CmdRef\)](#)
 - flattening [442 \(UG\)](#)

lower-level logic on multiple sheets [396 \(UG\)](#)
 trees of objects, Hierarchy Browser [1324 \(Ref\)](#)
 trees, browser, collapsing and expanding [1324 \(Ref\)](#)
 trigger conditions [19 \(DebugRef\)](#)
 trigger settings
 reloading [18 \(DebugRef\)](#)
 saving [18 \(DebugRef\)](#)
 trigger signal
 exporting [4308 \(DebugUG\)](#), [27 \(DebugRef\)](#)
 triggering
 advance mode [23 \(DebugRef\)](#)
 always-armed [21 \(DebugRef\)](#)
 between IICEs [4304 \(DebugUG\)](#), [76 \(DebugRef\)](#)
 complex [47 \(DebugRef\)](#), [23 \(DebugRef\)](#)
 modes [4238 \(DebugUG\)](#), [4300 \(DebugUG\)](#)
 simple [23 \(DebugRef\)](#)
 state machine [4320 \(DebugUG\)](#), [23 \(DebugRef\)](#), [24 \(DebugRef\)](#)
 state machines [47 \(DebugRef\)](#)
 triggermode option [52 \(DebugRef\)](#)
 triggers [82 \(DebugRef\)](#)
 complex [4240 \(DebugUG\)](#)
 pre-configured [4291 \(DebugUG\)](#)
 triggerstates option [47 \(DebugRef\)](#)
 triggerstime option [51 \(DebugRef\)](#)
 TriMatrix memory [1781 \(Ref\)](#)
 triple modular redundancy. *See* TMR
 tristates
 black_box_tri_pins directive [3423 \(AttrRef\)](#)
 converting drivers to muxes [4029 \(AttrRef\)](#)
 pushing tristates, description [468 \(CmdRef\)](#)
 pushing tristates, example [468 \(CmdRef\)](#)
 pushing tristates, pros and cons [468 \(CmdRef\)](#)
 syn_tristate directive [4025 \(AttrRef\)](#)
 tristates, Verilog [18 \(HDLRef\)](#)
 true dual-port block RAM [2078 \(Ref\)](#)
 true dual-port RAM
 See also multi-port RAMs
 TTFP compiler

initial prototype [1195 \(UG\)](#)
 type casting [161 \(HDLRef\)](#)
 SystemVerilog [152 \(HDLRef\)](#)
 typedef (SystemVerilog) [146 \(HDLRef\)](#)

U

UCF
 clock priority with syn_clock_priority [3531 \(AttrRef\)](#)
 Vivado support [1097 \(UG\)](#)
 UCF constraints [253 \(UG\)](#)
 converting to sdc manually [253 \(UG\)](#)
 input files [257 \(UG\)](#)
 supported [259 \(UG\)](#)
 supported constraints [1384 \(Ref\)](#)
 translating for logic synthesis [254 \(UG\)](#)
 translation examples [1386 \(Ref\)](#)
 unsupported [260 \(UG\)](#)
 ucf file
 using as input for logic design [254 \(UG\)](#)
 ucf file (Legacy). *See also* synplicity.ucf
 ucf2sdc [253 \(UG\)](#)
 ucf2sdc.log file [258 \(UG\)](#)
 UINISIM library
 simulation [2172 \(Ref\)](#)
 UMRBus [4266 \(DebugUG\)](#)
 Uncomment Code [403 \(CmdRef\)](#)
 Undo command [402 \(CmdRef\)](#), [13 \(DebugRef\)](#)
 Unfilter command [418 \(CmdRef\)](#)
 unfiltered schematic, compared with filtered [1327 \(Ref\)](#)
 unfiltering [550 \(CmdRef\)](#)
 FSM diagram [418 \(CmdRef\)](#)
 schematic [550 \(CmdRef\)](#)
 unfiltering schematic [1356 \(Ref\)](#)
 Unflatten Current Schematic command [547 \(CmdRef\)](#)
 Unhide Instances command [550 \(CmdRef\)](#)
 unhiding hidden instance [550 \(CmdRef\)](#)
 Unified Power Format commands [705 \(CmdRef\)](#)
 Unified Power Format. *See* UPF

- union construct (SystemVerilog) [157](#)
([HDLRef](#))
- unisim libraries
 - Virtex 2 with ISE 11 [2102](#) ([Ref](#))
- UNISIM library [2102](#) ([Ref](#))
- UNIX
 - configure external programs [569](#)
([CmdRef](#))
- unnamed blocks (SystemVerilog) [219](#)
([HDLRef](#))
- Unselect All command [553](#) ([CmdRef](#))
 - View menu (FSM Viewer) [418](#) ([CmdRef](#))
- unsigned arithmetic (VHDL) [289](#) ([HDLRef](#))
- unsigned functions [58](#) ([HDLRef](#))
- unsupported language constructs
 - VHDL
 - configuration declaration [378](#) ([HDLRef](#))
 - configuration specification [372](#)
([HDLRef](#))
- unsupported language constructs
(VHDL) [285](#) ([HDLRef](#))
- unsupported.ucf [258](#) ([UG](#))
- UpdateMEM
 - using [511](#) ([UG](#))
- updates from the Resource Center [601](#)
([CmdRef](#))
- UPF
 - checking implementation [1225](#) ([UG](#))
 - description [1201](#) ([UG](#))
 - properties for schematic viewing [1227](#)
([UG](#))
 - specifying commands for [1202](#) ([UG](#))
 - specifying isolation cells [1206](#) ([UG](#))
 - specifying power domains [1203](#) ([UG](#))
 - specifying retention registers [1215](#) ([UG](#))
 - verification [1230](#) ([UG](#))
- UPF commands [705](#) ([CmdRef](#))
 - create_power_domain [711](#) ([CmdRef](#))
 - load_upf [718](#) ([CmdRef](#))
 - name_format [720](#) ([CmdRef](#))
 - set_isolation [726](#) ([CmdRef](#))
 - set_isolation_control [730](#) ([CmdRef](#))
 - set_retention [733](#) ([CmdRef](#))
 - set_retention_control [735](#) ([CmdRef](#))
 - set_scope [736](#) ([CmdRef](#))
- Uppercase command [403](#) ([CmdRef](#))
- up-to-date checking [262](#) ([UG](#))
 - copying job logs to log file [264](#) ([UG](#))
 - limitations [265](#) ([UG](#))
- use ieee.std_logic_1164.all [4029](#) ([AttrRef](#))
- Use OFFSET for I/O constraints option
[4187](#) ([AttrRef](#))
- use statement (VHDL) [303](#) ([HDLRef](#))
- use synplify.attributes.all [4029](#) ([AttrRef](#))
- user interface
 - Synplify Premier/DP tools [1248](#) ([Ref](#))
 - Synplify Pro tool [1248](#) ([Ref](#))
 - Synplify tool [1248](#) ([Ref](#))
- user interface, overview [1255](#) ([Ref](#)), [7](#)
([DebugRef](#))
- user-defined enumeration data types
(VHDL) [288](#) ([HDLRef](#))
- user-defined functions, SNS (VHDL) [331](#)
([HDLRef](#))
- using [66](#) ([UG](#))
- using the mouse [1293](#) ([Ref](#))
- utilities
 - lib2syn [1411](#) ([Ref](#))
 - sdcc2fdc [1376](#) ([Ref](#)), [147](#) ([CmdRef](#))

V

- v file [1406](#) ([Ref](#)), [1407](#) ([Ref](#))
- variables
 - accessing, get_env Tcl command [87](#)
([CmdRef](#))
 - reporting [87](#) ([CmdRef](#))
 - SystemVerilog [176](#) ([HDLRef](#))
- variables (VHDL) [299](#) ([HDLRef](#))
- VCS Simulator command [501](#) ([CmdRef](#))
- VCS-Analyst Integration tool [1157](#) ([UG](#))
 - using [1157](#) ([UG](#))
- Vendor Constraints
 - Implementation Results panel,
Implementation Options dialog
box [455](#) ([CmdRef](#))
 - writing [455](#) ([CmdRef](#))
- vendor technologies
 - Achronix [1693](#) ([Ref](#))
 - Intel [1769](#) ([Ref](#))
 - Lattice [1887](#) ([Ref](#))
 - Microsemi [1981](#) ([Ref](#))

vendor-specific netlists 1695 (Ref), 1889 (Ref), 1983 (Ref), 2057 (Ref)
vendor-specific Tcl commands 774 (UG)
Verdi 733 (UG)
Verdi nWave viewer 4309 (DebugUG), 4310 (DebugUG)
Verdi platform 4225 (DebugUG)
verification
 UPF 1230 (UG)
Verilog
 'define statements 111 (UG)
 'ifdef and 'define statements 470 (CmdRef)
 'ifdef 128 (HDLRef)
 adding attributes and directives 117 (UG)
 adding probes 570 (UG)
 allow duplicate modules (Tcl option) 152 (CmdRef), 157 (CmdRef)
 always blocks 89 (HDLRef)
 combinational logic 102 (HDLRef)
 event control 103 (HDLRef)
 level-sensitive latches 108 (HDLRef)
 multiple event control arguments 89 (HDLRef)
 asynchronous sets and resets 111 (HDLRef)
 asynchronous state machines 121 (HDLRef)
 attribute syntax 133 (HDLRef)
 beta features 473 (CmdRef)
 black boxes 492 (UG), 124 (HDLRef)
 black boxes, instantiating 492 (UG)
 built-in gate primitives 17 (HDLRef)
 case sensitivity for Tcl Find command 206 (UG)
 checking source files 48 (UG)
 choosing a compiler 110 (UG)
 clock DLLs 2131 (Ref)
 combinational logic 101 (HDLRef)
 combined data, port types 40 (HDLRef)
 comma-separated sensitivity list 41 (HDLRef)
 comments, syntax 95 (HDLRef)
 compiler, configuring 568 (CmdRef)
 constant function (Verilog 2001) 43 (HDLRef)
 continuous assignments 104 (HDLRef), 108 (HDLRef)
 creating source files 36 (UG)

cross-module referencing 65 (HDLRef)
crossprobing from HDL Analyst view 424 (UG)
crossprobing to Physical Analyst 1054 (UG)
defining FSMs 501 (UG)
defining state machines with parameter and 'define 502 (UG)
directive syntax 133 (HDLRef)
editing operations 50 (UG)
extract design parameters 470 (CmdRef)
extracting parameters 111 (UG)
flip-flops using always blocks 107 (HDLRef)
Forward Annotation of Initial Values 1539 (Ref)
gate primitives 17 (HDLRef)
generic technology library 1410 (Ref)
hierarchical design 126 (HDLRef)
hierarchy 126 (HDLRef)
ignored language constructs 15 (HDLRef)
ignoring code with 'ifdef 128 (HDLRef)
ignoring code with translate off/on 4111 (AttrRef)
include paths, updating 89 (UG)
initial value data file 1536 (Ref)
initial values 90 (HDLRef)
initial values for RAMs 1533 (Ref)
initial values for registers 90 (HDLRef)
initializing RAMs 506 (UG)
instantiating
 black boxes 124 (HDLRef)
 gate primitives 17 (HDLRef)
instantiating LPMs as black boxes (Intel) 522 (UG)
Intel LPM library 528 (UG)
Intel LPM megafunction example 522 (UG)
Intel PLLs 1862 (Ref)
language
 constructs 14 (HDLRef)
language guidelines 89 (HDLRef)
level-sensitive latches 108 (HDLRef)
library directories 466 (CmdRef)
localparams (Verilog 2001) 57 (HDLRef)
macro library (Xilinx) 2102 (Ref)
Microsemi ACTgen macros 2048 (Ref)
mixed language files 59 (UG)
module template 94 (HDLRef)
multidimensional array (Verilog 2001) 63 (HDLRef)
multiplexer 103 (HDLRef)

netlist file [1420 \(Ref\)](#)
operators [14 \(HDLRef\)](#)
overriding parameter value
 with # [97 \(HDLRef\)](#)
 with defparam [97 \(HDLRef\)](#)
PREP benchmarks [125 \(HDLRef\)](#)
primitives [17 \(HDLRef\)](#)
RLOCs [2135 \(Ref\)](#)
ROM inference [1550 \(Ref\)](#)
scalable adder, creating [97 \(HDLRef\)](#)
scalable modules [95 \(HDLRef\)](#)
scaling by overriding parameter value
 with # (example) [97 \(HDLRef\)](#)
 with defparam (example) [97 \(HDLRef\)](#)
sequential logic [106 \(HDLRef\)](#), [108 \(HDLRef\)](#)
sequential shift components [520 \(UG\)](#)
sets and resets [110 \(HDLRef\)](#)
signal assignments always blocks [107 \(HDLRef\)](#)
signed multipliers [88 \(HDLRef\)](#)
signed signals (Verilog 2001) [42 \(HDLRef\)](#), [58 \(HDLRef\)](#), [61 \(HDLRef\)](#)
simple gates [17 \(HDLRef\)](#)
source files (.v) [1406 \(Ref\)](#), [1407 \(Ref\)](#)
specifying compiler directives [111 \(UG\)](#), [470 \(CmdRef\)](#)
specifying top-level module [113 \(UG\)](#)
state machines [116 \(HDLRef\)](#)
state values (FSM) [120 \(HDLRef\)](#)
structural netlist file (.vm) [1420 \(Ref\)](#)
structural Verilog [126 \(HDLRef\)](#)
supported language constructs [14 \(HDLRef\)](#)
supported standards [1408 \(Ref\)](#)
syn_keep on multiple nets [3722 \(AttrRef\)](#)
synchronous sets and resets [112 \(HDLRef\)](#)
synthesis macro [128 \(HDLRef\)](#)
synthesis text macro [128 \(HDLRef\)](#)
text macro [129 \(HDLRef\)](#)
tristate gates [18 \(HDLRef\)](#)
using library extensions [56 \(UG\)](#)
wildcard (*) in sensitivity list [39 \(HDLRef\)](#), [41 \(HDLRef\)](#)
Verilog 2001 [1408 \(Ref\)](#)
 constant statement [43 \(HDLRef\)](#)
 localparams [57 \(HDLRef\)](#)
 multidimensional array [63 \(HDLRef\)](#)
 setting global option from the Project view [110 \(UG\)](#)
 setting option per file [110 \(UG\)](#)
 signed signals [42 \(HDLRef\)](#), [58 \(HDLRef\)](#), [61 \(HDLRef\)](#)
 Verilog panel [464 \(CmdRef\)](#)
Verilog 2001 support [39 \(HDLRef\)](#)
Verilog 95 [1408 \(Ref\)](#)
-verilog argument
 Tcl [25 \(CmdRef\)](#)
Verilog include files
 hierarchical designs [128 \(HDLRef\)](#)
 using _SEARCHFILENAMEONLY_ directive [474 \(CmdRef\)](#)
Verilog language support [13 \(HDLRef\)](#), [137 \(HDLRef\)](#)
Verilog library files
 using library extensions [56 \(UG\)](#)
Verilog macro libraries
 Lattice [1925 \(Ref\)](#)
 Microsemi [2047 \(Ref\)](#)
Verilog model (.vmd) [596 \(UG\)](#)
Verilog panel [464 \(CmdRef\)](#)
 Implementation Options dialog box [462 \(CmdRef\)](#)
 Multiple File Compilation Unit [465 \(CmdRef\)](#)
 options [464 \(CmdRef\)](#)
 Push Tristates [465 \(CmdRef\)](#)
 SystemVerilog [464 \(CmdRef\)](#)
Verilog source file (.v) [1407 \(Ref\)](#)
Verilog synthesis guidelines [81 \(HDLRef\)](#)
version information [603 \(CmdRef\)](#), [59 \(DebugRef\)](#)
vhd file [1407 \(Ref\)](#)
vhd source file [1407 \(Ref\)](#)
VHDL
 accessing packages [302 \(HDLRef\)](#)
 adding attributes and directives [116 \(UG\)](#)
 adding probes [570 \(UG\)](#)
 adding source files to design library [300 \(HDLRef\)](#)
 assignment operators [292 \(HDLRef\)](#)
 assignments [340 \(HDLRef\)](#)
 asynchronous FSM created with process [364 \(HDLRef\)](#)
 asynchronous sets and resets [353 \(HDLRef\)](#)

asynchronous state machines 363 (HDLRef)

attribute syntax 401 (HDLRef)

attributes package 401 (HDLRef)

black boxes 494 (UG), 399 (HDLRef)

black boxes, instantiating 494 (UG)

case sensitivity for Tcl Find command 206 (UG)

case statement 315 (HDLRef)

checking source file 48 (UG)

clock DLLs 2131 (Ref)

clock edges 344 (HDLRef)

clock edges, wait statements 346 (HDLRef)

combinational logic

- definition 325 (HDLRef)
- examples 403 (HDLRef)

comments, syntax 341 (HDLRef)

compiler, configuring 568 (CmdRef)

compiling design units into libraries 300 (HDLRef)

component instantiation 326 (HDLRef)

concurrent signal assignments 321 (HDLRef)

conditional signal assignments 323 (HDLRef)

configuration

- declaration 372 (HDLRef)
- specification 369 (HDLRef)

configuration statement 379 (HDLRef)

constants 113 (UG), 299 (HDLRef)

- SNS (Selected Name Support) 328 (HDLRef)

creating source files 36 (UG)

crossprobing from HDL Analyst view 424 (UG)

crossprobing to Physical Analyst 1054 (UG)

D flip-flop with active-high reset, set

- asynchronous 354 (HDLRef)
- synchronous 356 (HDLRef)

data types 287 (HDLRef)

- guidelines 340 (HDLRef)

declaring and assigning objects 291 (HDLRef)

default assignment 361 (HDLRef)

defining FSMs 502 (UG)

demand loading 333 (HDLRef)

design libraries 300 (HDLRef)

detecting reset problems 362 (HDLRef)

directive syntax 401 (HDLRef)

dynamic range assignment 292 (HDLRef)

editing operations 50 (UG)

enumerated types as state values 361 (HDLRef)

enumeration encoding, default 341 (HDLRef), 460 (CmdRef)

events, defining outside process 345 (HDLRef)

extracting generics 113 (UG)

flip-flops 342 (HDLRef)

forgotten assignment to next state, detecting 363 (HDLRef)

FSM coding style 359 (HDLRef)

generics for scalable designs 394 (HDLRef)

global signals in mixed designs 62 (UG)

hierarchical designs 365 (HDLRef)

if-then-else statement 314 (HDLRef)

ignored language constructs 286 (HDLRef)

ignoring code with synthesis off/on 460 (CmdRef)

initialization state, extra 362 (HDLRef)

initializing RAMs with variable declarations 509 (UG)

initializing with signal declarations 507 (UG)

instantiating

- black boxes 399 (HDLRef)
- components 304 (HDLRef), 326 (HDLRef)

instantiating components 304 (HDLRef)

instantiating LPMs as black boxes (Intel) 522 (UG)

integer data type 289 (HDLRef)

Intel LPM megafunction example 524 (UG)

Intel PLLs 1862 (Ref)

language

- constructs 284 (HDLRef), 286 (HDLRef)
- guidelines 340 (HDLRef)
- support 283 (HDLRef)

latch error, example 350 (HDLRef)

level-sensitive latches

- concurrent signal assignment 347 (HDLRef)
- process blocks 348 (HDLRef)
- unwanted 350 (HDLRef)

libraries 300 (HDLRef)

- attributes, supplied with synthesis tool 1408 (Ref), 302 (HDLRef)

library and package rules 303 (HDLRef)

library packages

- accessing 302 (HDLRef)

attributes package [401 \(HDLRef\)](#)
IEEE support [284 \(HDLRef\)](#)
predefined [301 \(HDLRef\)](#)
library statement [303 \(HDLRef\)](#)
LPM instantiation example [527 \(UG\)](#)
macro libraries, Microsemi [2047 \(Ref\)](#)
macro library (Xilinx) [2102 \(Ref\)](#)
mixed language files [59 \(UG\)](#)
model template [341 \(HDLRef\)](#)
naming objects [291 \(HDLRef\)](#)
object naming syntax [291 \(HDLRef\)](#)
operators [306 \(HDLRef\)](#)
packages [300 \(HDLRef\)](#)
ports [297 \(HDLRef\)](#)
predefined enumeration types [287 \(HDLRef\)](#)
predefined packages [301 \(HDLRef\)](#)
PREP benchmarks [405 \(HDLRef\)](#)
prepared components method of instantiation [527 \(UG\)](#)
process keyword [311 \(HDLRef\)](#)
process template [343 \(HDLRef\)](#)
 modeling combinational logic [311 \(HDLRef\)](#)
processes [340 \(HDLRef\)](#)
 creating flip-flops and registers [342 \(HDLRef\)](#)
registers [342 \(HDLRef\)](#)
reset signals [353 \(HDLRef\)](#)
resource library, creating [303 \(HDLRef\)](#)
resource sharing [325 \(HDLRef\)](#)
RLOCs [2135 \(Ref\)](#)
RTL view primitives [354 \(HDLRef\)](#)
scalable architecture, using [395 \(HDLRef\)](#)
scalable design
 creating using generate statements [397 \(HDLRef\)](#)
 creating using generics [394 \(HDLRef\)](#)
 creating using unconstrained vector ports [393 \(HDLRef\)](#)
scalable designs [393 \(HDLRef\)](#)
 generate statement [397 \(HDLRef\)](#)
 generics [394 \(HDLRef\)](#)
 unconstrained vector ports [393 \(HDLRef\)](#)
Selected Name Support (SNS) [328 \(HDLRef\)](#)
selected signal assignments [323 \(HDLRef\)](#)
sensitivity list [312 \(HDLRef\)](#)
sequential logic [325 \(HDLRef\)](#)
 examples [404 \(HDLRef\)](#)
sequential shift components [519 \(UG\)](#)
sequential statements [313 \(HDLRef\)](#)
set signals [353 \(HDLRef\)](#)
sharing operators in case statements [325 \(HDLRef\)](#)
signal assignments [292 \(HDLRef\)](#)
 concurrent [321 \(HDLRef\)](#)
 conditional [323 \(HDLRef\)](#)
 selected [323 \(HDLRef\)](#)
 simple [322 \(HDLRef\)](#)
signals [297 \(HDLRef\)](#)
simple component instantiation [326 \(HDLRef\)](#)
simple signal assignments [322 \(HDLRef\)](#)
simulation using enumerated types [362 \(HDLRef\)](#)
SNS [328 \(HDLRef\)](#)
 constants [328 \(HDLRef\)](#)
 demand loading [333 \(HDLRef\)](#)
 functions and operators [329 \(HDLRef\)](#)
 user-defined function support [331 \(HDLRef\)](#)
source files (.vhd) [1407 \(Ref\)](#)
specifying top-level entity [113 \(UG\)](#)
state machines [357 \(HDLRef\)](#)
statements
 case [315 \(HDLRef\)](#)
 generate [397 \(HDLRef\)](#)
 if-then-else [314 \(HDLRef\)](#)
 library [303 \(HDLRef\)](#)
 use [303 \(HDLRef\)](#)
 wait [346 \(HDLRef\)](#)
structural netlist file (.vhm) [1420 \(Ref\)](#)
supported language constructs [284 \(HDLRef\)](#)
supported standards [1407 \(Ref\)](#)
synchronous FSM from concurrent assignment statement [364 \(HDLRef\)](#)
synchronous sets and resets [354 \(HDLRef\)](#)
synthesis
 attributes and directives [401 \(HDLRef\)](#)
 examples [403 \(HDLRef\)](#)
 guidelines [339 \(HDLRef\)](#)
unsupported language constructs [285 \(HDLRef\)](#)
 configuration declaration [378 \(HDLRef\)](#)
 configuration specification [372 \(HDLRef\)](#)
 use statement [303 \(HDLRef\)](#)

- user-defined enumeration data types
 - 288 (HDLRef)
- variables 299 (HDLRef)
- wait statement inside process 346 (HDLRef)
- VHDL 2008 411 (HDLRef)
 - enabling 427 (HDLRef)
 - operators 412 (HDLRef)
 - packages 425 (HDLRef)
- vhdl argument
 - Tcl 25 (CmdRef)
- VHDL assignment
 - dynamic range 292 (HDLRef)
- VHDL components
 - configuration declarations 372 (HDLRef)
 - creating resource library 304 (HDLRef)
 - instantiating 304 (HDLRef), 326 (HDLRef)
 - specifying configurations 370 (HDLRef)
 - vendor macro libraries 304 (HDLRef)
- VHDL files
 - adding library 82 (UG)
 - adding third-party package library 82 (UG)
- VHDL generic mapping
 - configuration statement 379 (HDLRef)
- VHDL libraries
 - compiling design units 300 (HDLRef)
 - setting up 429 (CmdRef)
- VHDL library
 - specifying non-default (Intel) 1774 (Ref)
- VHDL macro libraries
 - Lattice 1926 (Ref)
- VHDL models 94 (DebugRef)
- VHDL multiple entities
 - configuration statement 381 (HDLRef)
- VHDL panel
 - DesignWare options 461 (CmdRef), 467 (CmdRef)
 - Implementation Options dialog box 458 (CmdRef)
- VHDL port mapping
 - configuration statement 380 (HDLRef)
- VHDL source file (.vhd) 1407 (Ref)
- vhm file 1420 (Ref)
- vi text editor 55 (UG)
- View FSM command 553 (CmdRef)
- View FSM Info File command 553 (CmdRef)
- View Log File command 416 (CmdRef)
- View menu 415 (CmdRef), 14 (DebugRef)
 - Filter submenu 418 (CmdRef)
 - Log File command 420 (CmdRef)
 - Rats Nest submenu 662 (CmdRef)
 - RTL and Technology view commands 416 (CmdRef)
- View Result File command 416 (CmdRef)
- View Sheets command 417 (CmdRef)
- views 1275 (Ref), 1680 (Ref)
 - FSM 1325 (Ref)
 - Project 1256 (Ref)
 - removing 1298 (Ref)
 - RTL 1320 (Ref)
 - Technology 1322 (Ref)
- Virtex
 - clock buffers 2130 (Ref)
 - I/O buffers 2133 (Ref)
 - netlist 2057 (Ref)
 - PCI core 2108 (Ref)
- virtual clock, setting (Legacy) 231 (UG)
- Visual Properties command 417 (CmdRef)
- Vivado
 - environment variables 1098 (UG)
 - flow 1096 (UG)
 - launching 97 (CmdRef)
 - netlists 1096 (UG)
 - options file 1103 (UG), 1104 (UG)
 - running 1099 (UG)
 - running incrementally 1107 (UG)
 - running place-and-route 1095 (UG)
- Vivado IP 718 (UG)
 - importing 718 (UG)
 - importing netlists 718 (UG)
- vm file 1420 (Ref)
- vqm
 - inferred Clearbox 668 (UG)
 - instantiated Clearbox 671 (UG)
- vqm files
 - naming requirements 1880 (Ref)

W

- wait statement, inside process (VHDL) 346 (HDLRef)

- warning messages
 - definition [49 \(UG\)](#)
- warnings
 - feedback muxes [535 \(UG\)](#)
 - filtering [285 \(UG\)](#)
 - sorting [285 \(UG\)](#)
- watch command [82 \(DebugRef\)](#)
- watch icon
 - color coding [4224 \(DebugUG\)](#)
- Watch window [277 \(UG\)](#)
 - moving [278 \(UG\)](#), [284 \(UG\)](#)
 - multiple implementations [98 \(UG\)](#)
 - resizing [278 \(UG\)](#), [284 \(UG\)](#)
- Watch Window. *See* Log Watch window
- watchdog mode
 - complex counter [52 \(DebugRef\)](#)
- watchpoints [82 \(DebugRef\)](#), [20 \(DebugRef\)](#)
 - activating [4285 \(DebugUG\)](#), [4287 \(DebugUG\)](#)
 - combined with breakpoints [23 \(DebugRef\)](#)
 - deactivating [4286 \(DebugUG\)](#)
 - folded [4289 \(DebugUG\)](#)
 - hexadecimal values [14 \(DebugRef\)](#)
 - multiple [23 \(DebugRef\)](#)
 - searching [41 \(DebugRef\)](#)
 - transition [13 \(DebugRef\)](#)
- waveform command [86 \(DebugRef\)](#)
- waveform display [4282 \(DebugUG\)](#), [34 \(DebugRef\)](#), [53 \(DebugRef\)](#)
- waveform viewers
 - Verdi [4309 \(DebugUG\)](#)
- web browser
 - specifying for UNIX [597 \(CmdRef\)](#)
- web updates [601 \(CmdRef\)](#)
- What's Cool [1289 \(Ref\)](#)
- What's New [1289 \(Ref\)](#)
- while-loop statement [317 \(HDLRef\)](#)
- white boxes
 - defined for ise2syn flow [749 \(UG\)](#)
 - EDK cores [749 \(UG\)](#)
 - ise2syn [491 \(CmdRef\)](#)
 - using syn_macro on non-secure cores [737 \(UG\)](#)
- wide adder/subtractor [2099 \(Ref\)](#)
- wide adders/subtractors
 - example [2107 \(Ref\)](#)
 - inferring [2105 \(Ref\)](#)
 - prerequisites for inference [2106 \(Ref\)](#)
- wildcards
 - effect of search scope [414 \(UG\)](#)
 - Find command (Tcl) [206 \(UG\)](#)
 - in hierarchies [14 \(DebugRef\)](#)
 - in path names [12 \(DebugRef\)](#)
 - message filter [287 \(UG\)](#)
 - Tcl find command [224 \(CmdRef\)](#)
 - text Find [404 \(CmdRef\)](#), [28 \(DebugRef\)](#), [35 \(DebugRef\)](#)
 - text replacement [413 \(CmdRef\)](#)
 - timing analyzer [538 \(CmdRef\)](#)
 - Verilog sensitivity list [39 \(HDLRef\)](#), [41 \(HDLRef\)](#)
- wildcards (Find)
 - examples [416 \(UG\)](#)
 - how they work [355 \(UG\)](#), [414 \(UG\)](#)
- wildcards (Physical Analyst)
 - in Find command [1045 \(UG\)](#)
- window
 - Project [1256 \(Ref\)](#)
- windows [1275 \(Ref\)](#), [1680 \(Ref\)](#)
 - closing [1308 \(Ref\)](#), [30 \(DebugRef\)](#), [32 \(DebugRef\)](#)
 - console [24 \(DebugRef\)](#)
 - log watch [1276 \(Ref\)](#)
 - removing [1298 \(Ref\)](#)
- Windows, 64-bit mapping [449 \(CmdRef\)](#)
- wires, preserving with syn_keep directive [3721 \(AttrRef\)](#)
- WNID_UG_PNR_SCRIPTS [1081 \(UG\)](#)
- working directory
 - displaying [58 \(DebugRef\)](#)
- write fsdb command [88 \(DebugRef\)](#)
- write instrumentation command [89 \(DebugRef\)](#)
- Write Output Netlist Only command [499 \(CmdRef\)](#)
- write samples command [91 \(DebugRef\)](#)
- write vcd command [93 \(DebugRef\)](#)
- write vhdlmodel command [94 \(DebugRef\)](#)
- write_vhdl [152 \(CmdRef\)](#)

X

`xc_area_group` (Xilinx) [4115 \(AttrRef\)](#)
`xc_clockbuftype` attribute [4121 \(AttrRef\)](#)
 specifying [2130 \(Ref\)](#)
`xc_fast` attribute [4127 \(AttrRef\)](#)
 for critical paths [2101 \(Ref\)](#)
`xc_fast_auto` attribute [4131 \(AttrRef\)](#)
`xc_global_buffers`
 and `syn_global_buffers` [4137 \(AttrRef\)](#)
`xc_global_buffers` attribute [4137 \(AttrRef\)](#)
`xc_isgsr` directive [4141 \(AttrRef\)](#)
`xc_loc` attribute [4147 \(AttrRef\)](#)
 assigning locations in SCOPE [2123 \(Ref\)](#)
`xc_map` attribute [4151 \(AttrRef\)](#)
 relative location [2134 \(Ref\)](#)
`xc_padtype` attribute [4157 \(AttrRef\)](#)
 specifying I/Os [2133 \(Ref\)](#)
`xc_props` attribute [4159 \(AttrRef\)](#)
`xc_pulldown` attribute [4167 \(AttrRef\)](#)
`xc_pullup` attribute [4167 \(AttrRef\)](#)
`xc_rloc` attribute [4173 \(AttrRef\)](#)
 specifying relative location [2135 \(Ref\)](#)
`xc_slow` attribute [4179 \(AttrRef\)](#)
`xc_use_keep_hierarchy` attribute [4181 \(AttrRef\)](#)
`xc_use_timespec_for_io` attribute [4187 \(AttrRef\)](#)
`xc_uset` attribute [4193 \(AttrRef\)](#)
 grouping instances for relative placement [2135 \(Ref\)](#)
 using to group instances [2135 \(Ref\)](#)
`xcf` files
 translating to `sdc` [257 \(UG\)](#)
`xdc2fdc`
 debugging translation [731 \(UG\)](#)
`xflow` and `xtclsh` [2169 \(Ref\)](#)
Xilinx
 asymmetric block RAM [2077 \(Ref\)](#)
 attributes [2173 \(Ref\)](#)
 black boxes [2088 \(Ref\)](#), [2091 \(Ref\)](#)
 block RAMs [2078 \(Ref\)](#)
 byte-enable RAM [1525 \(Ref\)](#)
 byte-enable RAM inference [1525 \(Ref\)](#)
 clock buffers [2130 \(Ref\)](#)

clock skew [2143 \(Ref\)](#)
compile point timing data [2142 \(Ref\)](#)
compile points [2170 \(Ref\)](#)
CoreGen [2108 \(Ref\)](#)
CPLD device options [2157 \(Ref\)](#)
CPLD options [2159 \(Ref\)](#)
CPLD project command [2161 \(Ref\)](#)
CPLD technologies [2157 \(Ref\)](#), [2161 \(Ref\)](#)
DDR register inference [2082 \(Ref\)](#)
design guidelines [2101 \(Ref\)](#)
directives [2173 \(Ref\)](#)
distributed RAM [1490 \(Ref\)](#)
distributed RAM inference [1487 \(Ref\)](#)
DSP component [3581 \(AttrRef\)](#), [3589 \(AttrRef\)](#)
dynamic SRL tables [2086 \(Ref\)](#)
fanout limits [2138 \(Ref\)](#)
forward-annotating properties [4159 \(AttrRef\)](#)
gated clocks [2141 \(Ref\)](#)
generated clocks [2141 \(Ref\)](#)
GSR [2104 \(Ref\)](#)
I/O buffers [2133 \(Ref\)](#)
I/O insertion, manual [2127 \(Ref\)](#)
I/O locations [2090 \(Ref\)](#), [2122 \(Ref\)](#)
including cores for synthesis [737 \(UG\)](#)
inferring dynamic SRL [2086 \(Ref\)](#)
inferring I/O buffers with `syn_diff_io` [3545 \(AttrRef\)](#)
INIT property [2112 \(Ref\)](#)
INIT property, VHDL [2115 \(Ref\)](#)
instantiating I/O pads [2089 \(Ref\)](#)
IP cores [734 \(UG\)](#), [2108 \(Ref\)](#)
launching Vivado [97 \(CmdRef\)](#)
macro libraries [2102 \(Ref\)](#)
macros [2102 \(Ref\)](#)
mapping latches [2088 \(Ref\)](#)
multi-port RAMs [2078 \(Ref\)](#)
non-secure core flow [737 \(UG\)](#)
OFFSET for I/O constraints [4187 \(AttrRef\)](#)
packing IOBs [2089 \(Ref\)](#)
packing registers [2119 \(Ref\)](#)
pad types [4157 \(AttrRef\)](#)
partition flow [1116 \(UG\)](#)
pipelining [2140 \(Ref\)](#)
place & route options file [628 \(CmdRef\)](#)
place-and-route option file, Vivado [1103 \(UG\)](#)
post-synthesis simulation [2172 \(Ref\)](#)
register balancing [2140 \(Ref\)](#)

register inference [2080 \(Ref\)](#)
relative locations attributes [2099 \(Ref\)](#)
resource usage report [2163 \(Ref\)](#)
retiming [2140 \(Ref\)](#)
running from synthesis tool [569 \(CmdRef\)](#)
secure core flow [737 \(UG\)](#)
shift registers [515 \(UG\)](#)
SLR [2059 \(Ref\)](#)
Spartan device options [2147 \(Ref\)](#)
Spartan options [2150 \(Ref\)](#)
Spartan project command [2157 \(Ref\)](#)
Spartan technologies [2155 \(Ref\)](#)
specifying pin location [2090 \(Ref\)](#), [2122 \(Ref\)](#)
startup blocks [2104 \(Ref\)](#)
synthesis constraint files (Legacy) [248 \(UG\)](#)
synthesis design flows [2060 \(Ref\)](#)
technologies [2055 \(Ref\)](#)
TIMESPEC for I/O constraints [4187 \(AttrRef\)](#)
tips for optimizing [2101 \(Ref\)](#)
translating PAD file to constraint file [504 \(CmdRef\)](#)
true dual-port RAM. *See* multi-port RAMs
updating compile points [2142 \(Ref\)](#)
using BUFR [2129 \(Ref\)](#)
Virtex device options [2147 \(Ref\)](#)
Virtex options [2150 \(Ref\)](#)
Virtex project command [2157 \(Ref\)](#)
Virtex technologies [2155 \(Ref\)](#)
XC4000 project command [2157 \(Ref\)](#)
Xilinx differential I/O buffer inference [2089 \(Ref\)](#), [2128 \(Ref\)](#)
Xilinx DSP48 register conversion [3523 \(AttrRef\)](#), [3531 \(AttrRef\)](#), [3867 \(AttrRef\)](#)
Xilinx forward-annotation
 datapath only [365 \(CmdRef\)](#)
Xilinx parallel cable settings [41 \(DebugRef\)](#)
Xilinx Parameterized Macro [75 \(UG\)](#)
Xilinx Partition Flow
 using the standalone XML converter [213 \(CmdRef\)](#)
Xilinx Partition flow
 syn_sxml2pxml Tcl command [213 \(CmdRef\)](#)
Xilinx projects
 converting with ise2syn [739 \(UG\)](#), [489 \(CmdRef\)](#)
Xilinx SSI technology [2059 \(Ref\)](#)
Xilinx USB cable settings [42 \(DebugRef\)](#)
Xilinx Vivado 2018.3 [75 \(UG\)](#)
XILINX_VIVADO [76 \(UG\)](#)
Xilinxauto cable settings [43 \(DebugRef\)](#)
XML converter
 using Xilinx Partition Flow [213 \(CmdRef\)](#)
xnf file (Xilinx) [2056 \(Ref\)](#)
xpartition.pxml file [1123 \(UG\)](#)
XPM [75 \(UG\)](#)
XPM-memory [76 \(UG\)](#)
xtclsh executable [2169 \(Ref\)](#)

Z

zoom
 using the mouse wheel and Ctrl key [1297 \(Ref\)](#)
zoom mouse pointer [416 \(CmdRef\)](#)
Zoom Out command [416 \(CmdRef\)](#)
Zoom Selected command
 Physical Analyst view [688 \(CmdRef\)](#)
zoom selected objects (Physical Analyst) [1024 \(UG\)](#)

