Prodigy™ S7-19P Logic System

Reference Manual

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Preface: Product Components

List of all components included in the **Prodigy Single-VU19P** product:

Quantity	Item
Electronic Components	
1	Single-VU19P Prodigy Logic System *For reference only, the Logic system is comprised of the following 7 sub-systems:* • *FPGA Module VU19P (top board)* • *PCM VU19PS (internal board)* • *Smart Power Switch Module Type C* • *Power Supply Unit (PSU) Smart Power Switch Module* • *PSU power supply (Input AC 100~240V; Output DC 12V, 37A)* • *Cooling fan with heat sink on FPGA Module (top board)* • *Cooling fan for PCM (internal)*
1	System Clock Control Module Type D
1	Prodigy GT I/O Testing Module V2.0
1	Prodigy I/O Testing Module
1	DDR4 I/O Testing Module
1	Micro SD card
Cables	
1	USB cable
2	Ethernet cable
1	PSU AC power cable
Miscellaneous Components	
10	I/O connector caps (8 Prodigy connectors; 2 PGT connectors)
6	Daughter card support brackets
32	Screws
12	Nuts
12	Standoffs

Important: The Logic System is not meant to be disassembled. The FPGA module and Power Control Module (upper and lower boards) are tightly coupled, and proper assembly can only be guaranteed with factory tooling.

Any attempt to disassemble the system will **void the warranty**.

1 Overview

The **Single-VU19P Prodigy™ Logic System** (“Single-VU19P”) is S2C’s 7th generation SoC/ASIC prototyping hardware. The Single-VU19P is built around a single Xilinx UltraScale+ **XCVU19P-FSVA3824** FPGA. Each **XCVU19P-FSVA3824** FPGA contains 8,938K System Logic Cells, 224Mbits internal Memory and 3,840 DSP slices. The Single-VU19P System is designed for rapid SoC/ASIC prototyping and support using S2C’s Prodigy IP – a configurable FPGA-based IP format – to efficiently create prototype designs.

The Single-VU19P is comprised of two distinct modules: one **FPGA Module VU19P** and one **PCM VU19PS**. These two modules are interconnected through two Samtec SEAF/SEAM 400-pin connectors and two Samtec SEAF/SEAM 300-pin connectors which are securely coupled using six standoffs. The Single-VU19P FPGA Module sits on top providing full access to all I/O connectors and switches, with the PCM residing just below.

Figure 1-1 Single VU19P Logic System

1.1 System Features

Large Flexible I/O

- Prodigy connector I/O voltage can be adjusted to 1.2V, 1.35V, 1.5V or 1.8V through runtime software in GUI with 4 status LEDs on-board to indicate I/O voltage value
- Each Prodigy GT connector is fully populated 16 I/Os and 8 Gigabit Transceivers
- Prodigy GT connector I/O voltage is fixed to 1.8V
- DM connector provides 4 Gigabit Transceivers for Debug Module application
- Two on-board vertical DDR4-SODIMM support up to 72-bit 16GB DDR4 Memory Module

Figure 1-2 Vertical DDR4-SODIMM

Important: The DDR4-SODIMM connectors must be attached vertically! If connected improperly socket pins can be deformed or holding rail ends can become damaged.

Advanced Clock Management

- 8 global clocks to be selected from:
  - 8 programmable clock sources (0.2-350MHz)
  - 5 pairs of external clocks through MMCX connectors
  - 1 OSC socket
- 3 feedback clock outputs through 3 pairs of MMCX connector
- 3 global resets to be selected from:
  - 3 global reset sourced from on board push buttons
  - 2 global reset sourced from SC Clock Module Type D
  - 2 global reset sourced from runtime software in GUI

Dedicated LVDS TDM Circuitry

- LVDS TDM operating clock (0.2-350MHz)
- LVDS TDM reset from one dedicated push button
- LVDS TDM training successful indication LED

Advanced Board Features

- Equal trace length for I/Os from same Prodigy connector
- 50-ohm single-ended impedance and 100-ohm differential impedance for all signals
- FPGA voltage, current, and temperature detection and alarm
- Fan cooling with PWM function
- Battery back-up encryption key
- Daughter card detection and authentication
- Expandable through Samtec 300-pin cables, interconnection modules

User I/O

- 1x 4-position DIP Switch
- 2x push buttons
- 3x LEDs

- 8x GPIOs on pin header
- 2x 3-pin UART

FPGA Configuration Options

- Download through Intel JTAG interface
- Con through Micro-USB from PlayerPro runtime software
- Download through 10/100/1000Mbps Ethernet Port
- Configure from on-board Micro SD card

Software and Remote Capabilities – Player Pro™

- Generate programmable clocks
- Adjust dedicated I/O voltages
- FPGA pin self-test, guided by Software Wizard
- Read back global clock frequency
- Program Micro SD card (used to configure FPGA)

1.2 FPGA Module VU19P

The **FPGA Module** provides all user I/O and main prototyping interface. It has 1,152 I/Os and 28 (gigabit) Transceivers on eight Prodigy connectors, 32 I/Os and 16 (gigabit) Transceivers on two Prodigy GT connectors, 270 I/Os on two 72-bit DDR4 SODIMMs, reserve 276 common-interconnections between two VU19P FPGA. One DM connector supports 4 (gigabit) Transceivers. Also, there are 17 user I/Os and one JTAG header on the module.

Figure 1-3 FPGA Module – I/O, Controls, and Indicators

1.3 PCM VU19PS

The PCM VU19PS has two DM connectors, one **SC connector**, one Micro **USB** port, one **Ethernet** port, and one Micro **SD** card. In addition to the existing Micro USB port for our runtime features such as FPGA download, programmable clock generations and self-test, the PCM VU19PS also supports these runtime features through Ethernet port so you can remotely control your FPGA hardware. Additionally, there are many runtime features such as I/O voltage setting, clock frequency, virtual I/O and firmware version read-back through software control.

Figure 1-4 PCM VU19PS – Connections and Controls

1.4 Chassis Front Panel

The VU19P Chassis front panel has a main power switch, auxiliary outlets for powering daughter cards (1.8v, 3.3v, and 5v supplies), plus an Ethernet connection for Remote Power control.

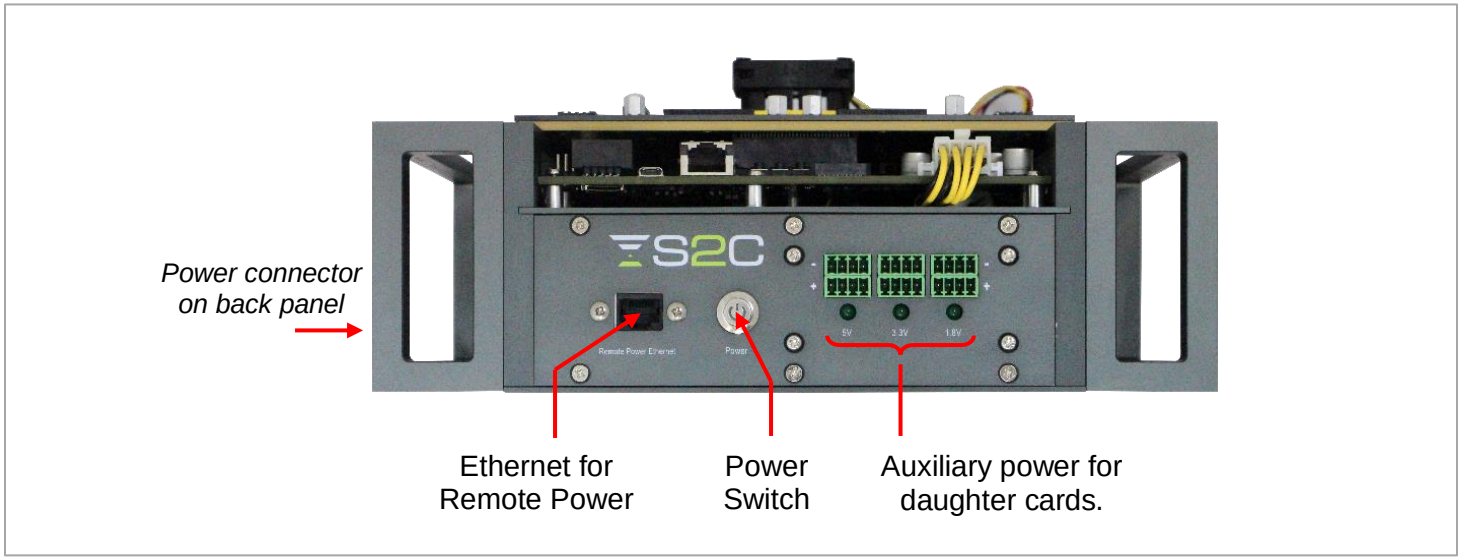

Figure 1-5 Chassis Front Panel

2 System Specifications

These specifications apply to Logic Systems populated with **XCVU19P-FSVA3824** devices.

Table 2-1 Maximum Operating Conditions

Parameter	Specification
Supply Voltage	12v
Dedicated I/O Voltage	1.2v – 1.8v

Table 2-2 Gate & Memory Capacity

Parameter		Specification
FPGA Specs		
	System Logic Cell	8.938M
	Internal Memory	224Mb
	DSP Slices	3,840

Table 2-3 System I/O – Signals, Clocks, & Reset

Signal Description		Quantity	Notes
Total Available I/O		1,471	
Dedicated I/O		1,184	8x Prodigy connectors + 2x Prodigy GT connectors
SODIMM I/O		270	2x 72-bit DDR4 SODIMM
User I/O		17	
Number of Transceivers		48	
Global Clocks		8 (Differential pairs)	
	Programmable Clock Inputs	8	Adjustable from 0.2–350 MHz
	MMCX Clock Inputs	5	
	OSC Clock Inputs	1	
MMCX Clock Outputs		3 (LVDS pairs)	
Global Reset		3 (Single-ended)	
TDM Reset		1 (Single-ended)	

See Global Clocks for detailed clock pin-outs.

Table 2-4 I/O Connector Descriptions

Connector	Signals	Notes
J1	Std I/O: 144 + G-bit transceivers: 4	Voltage adjustable from 1.2 to 1.8v
J2	Std I/O: 144 *(no transceivers)*	
J3	Std I/O: 144 + G-bit transceivers: 4	
J4	Std I/O: 144 + G-bit transceivers: 4	
J5	Std I/O: 144 + G-bit transceivers: 4	
J6	Std I/O: 144 + G-bit transceivers: 4	
J7	Std I/O: 144 + G-bit transceivers: 4	
J8	Std I/O: 144 + G-bit transceivers: 4	
JX1	Std I/O: 16 + G-bit transceivers: 8	Fixed @ 1.8 v
JX2	Std I/O: 16 + G-bit transceivers: 8	
J11	Std I/O: 135 *(memory I/O)*	For DDR4 SODIMM
J12	Std I/O: 135 *(memory I/O)*	For DDR4 SODIMM
P_JD2	G-bit transceivers: 4	For Debug Module

See Dedicated I/O, SODIMM I/O and Gigabit Transceiver I/O for detailed pin outs.

Table 2-5 System-level Peripheral Interfaces

Interface	Notes
USB	Micro-USB connector on PCM (P_J3)
Ethernet	Connector on PCM (P_J4)
MicroSD	Connector on underside of PCM (P_J5)
JTAG	Connector on FPGA Module (J15)

3 System Architecture

Prodigy VU19P Logic System hardware architecture is designed for both flexibility and scalability. It includes **FPGA Module VU19P** and **PCM VU19PS**. These two modules are stacked together with two SEAM/SEAF 400-pin connectors (J13 and J14). And two SEAM/SEAF 300-pin connectors (J9 and J10). When only one Prodigy Logic System is used, most of the FPGA I/Os are brought out directly for maximum flexibility.

When capacity expansion is needed, multiple Prodigy Logic Systems can be used to expand through Samtec 300-Pin cables, interconnection modules or mother board. The Prodigy VU19P Logic System also includes a dedicated section that controls such functionality as dynamic interconnect bus technology, embedded integrated logic analyzer, powerful clock generation, co-emulation with simulators, and transaction-based co-modeling.

The following section illustrates Prodigy VU19P Logic System's general, clock, and I/O architectures.

3.1 FPGA Module Architecture

The general architecture of the basic system components and their connections are as follows:

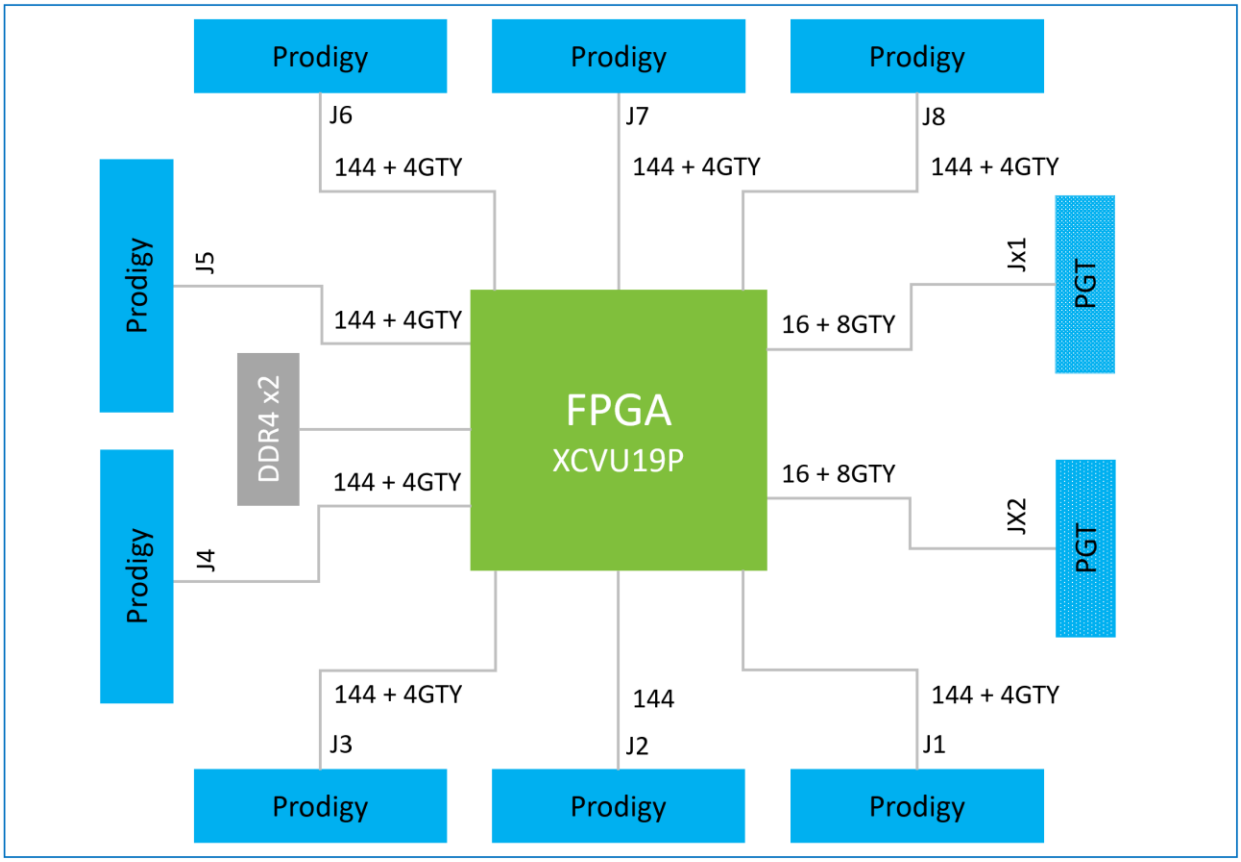

Figure 3-1 FPGA Module VU19P General Architecture

3.2 PCM Architecture

The general architecture of the basic system components and their connections are as follows:

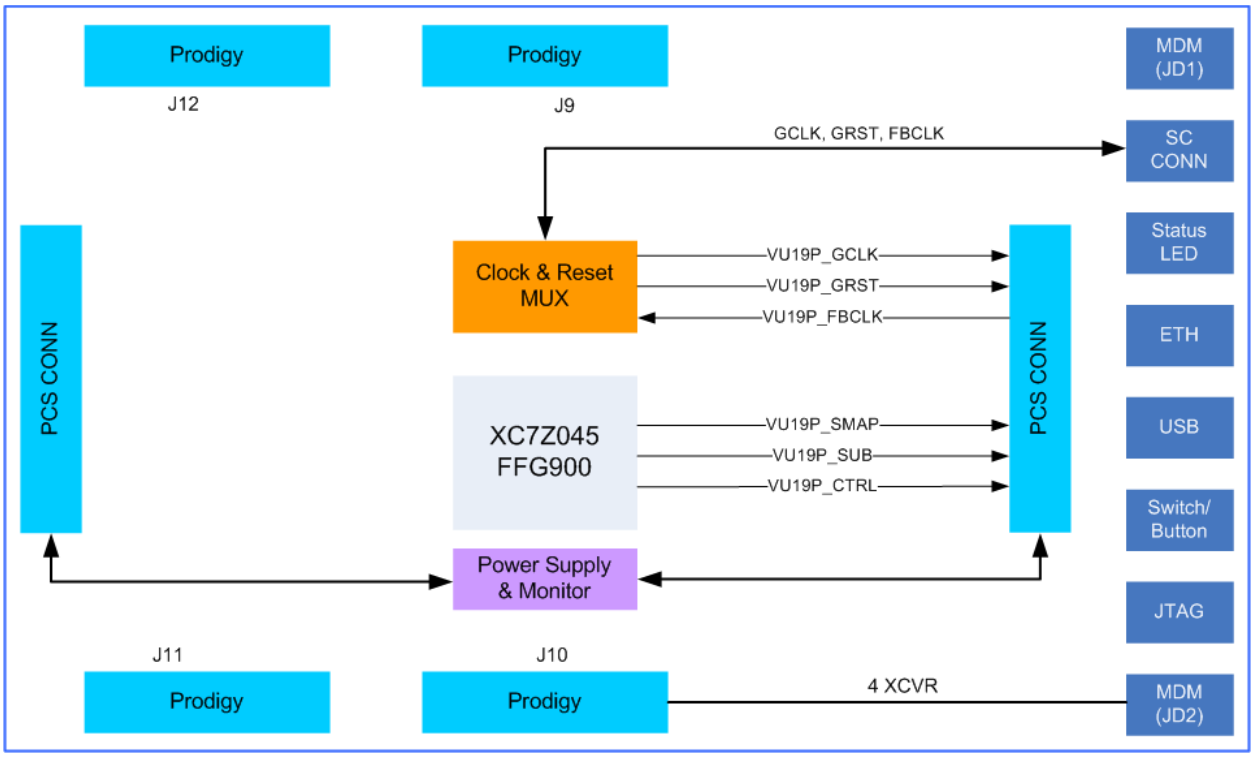

Figure 3-2 PCM VU19PS General Architecture

3.3 Clock Architecture

A total of 8 global clocks can be input from 8 pairs of programmable LVDS clocks or 6 pairs of LVDS clocks from SC Clock Module Type D.

6 pairs of programmable LVDS clocks and 6 pairs of LVDS clocks from SC Clock Module Type D are respectively selected through runtime software in GUI. The last two pairs of programmable LVDS clock is always selected. 7th programmable LVDS clock is recommended for J11 DDR4 SODIMM on board; 8th programmable LVDS clock is recommended for J12 DDR4 SODIMM on board.

3 pairs of LVDS feedback clocks from the user FPGA output to SC Clock Module Type D.

SC Clock Module Type D provides 5 pairs of LVDS clock inputs on MMCX, 1 single-ended OSC socket and 3 pairs of LVDS clock outputs on MMCX.

SC Clock Module Type D comes with Single VU19P Logic System package.

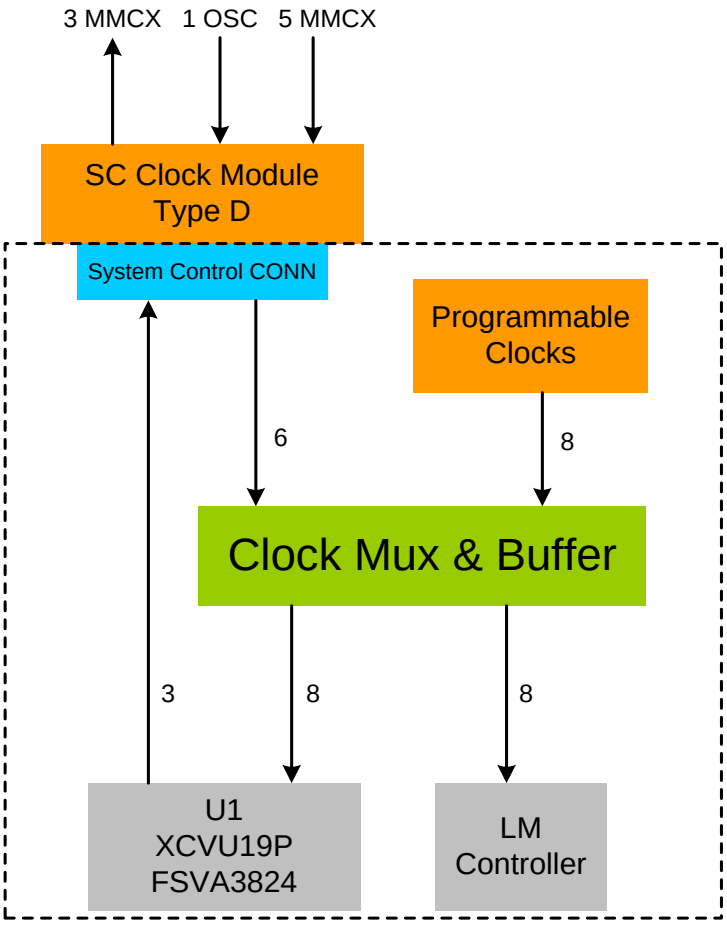

Figure 3-3 Single VU19P Logic System External Clock Architecture

3.4 External I/O Architecture

FPGA Module VU19P contains four External I/O types: Gigabit Transceivers, Dedicated I/O, DDR4 SODIMM I/O and User I/O.

There are **2 Prodigy GT connectors** on FPGA Module VU19P. Each Prodigy GT connector has 8 Gigabit transceivers and 16 I/Os on the Samtec SEAF/SEAM 120-pin connector. There are total 16 Gigabit Transceivers and 32 I/Os on Prodigy GT connectors for user applications.

There are **8 Prodigy connectors** on FPGA Module VU19P. Each Prodigy connector is fully populated with 144 I/Os and 4 Gigabit Transceivers except for J2 which are populated with 144 I/Os only. There are total 1,152 I/Os and 28 Gigabit Transceivers on Prodigy connectors for user applications.

There are **2 DDR4 SODIMM** (with ECC) on FPGA Module VU19P which is labelled J11 and J12. Both of them support 72-bit ECC, dual rank DDR4 memory module.

There are **17 user I/Os** on FPGA Module VU19P including **1x** 4-position DIP Switch, **2x** pushbuttons, **3x** LEDs and **8x** GPIOs on pin header respectively.

There are **2x UART** on FPGA Module VU19P through 3x2 pin header J19.

3.5 Peripheral Architecture

The PCM VU19PS supports one SC connector (**P_JS1**) to bridge SC Clock Module Type D which has **6 pairs of LVDS clock input**, **3 pairs of LVDS clock output**, and **2 single-ended reset** input.

The PCM VU19PS supports a **RJ-45 10/100/1000 base-T Ethernet** (**P_J4**) using an external Marvell 88E1116R PHY and the HPS EMAC. The PHY-to-MAC interface employs RGMII connection.

The PCM VU19PS supports a **Micro USB** (**P_J3**) using an external SMSC USB3320 PHY and the HPS EMAC. The PHY-to-MAC interface employs ULPI connection.

The PCM VU19PS supports a **Micro SD card** interface (**P_J5**) using x4 data lines. The Micro SD card can store up to 16 sets of XCVU19P-FSVA3824 FPGA configuration files. The **4-position DIP Switch** (**P_S3**) is used to select the configuration files and pushbutton (**P_SW3**) is used to reconfigure the FPGA through Micro SD card.

The PCM VU19PS provides some LEDs to indicate the status of Single-VU19P Logic System. When ***red*** LEDs light, please turn off Single-VU19P Logic System immediately.

The PCM VU19PS provides three on-board push buttons (**P_SW4**, **P_SW5** & **P_SW6**) which can be used for **global reset input**.

4 System Operation

The Single VU19P comes with the **PlayerPro Runtime** software that includes a hardware self-test feature. Runtime is used to download and configure the Single VU19P, as well as specify clocks, I/O voltages, and other parameters.

4.1 Required Manual

Next is to install the PlayerPro software so you can use the Runtime utilities. For this you will need to follow the instructions in the Software Installation and Hardware Self-test Manual

4.2 Setting Up Hardware

Setting up Single VU19P Logic System is simple and straightforward:

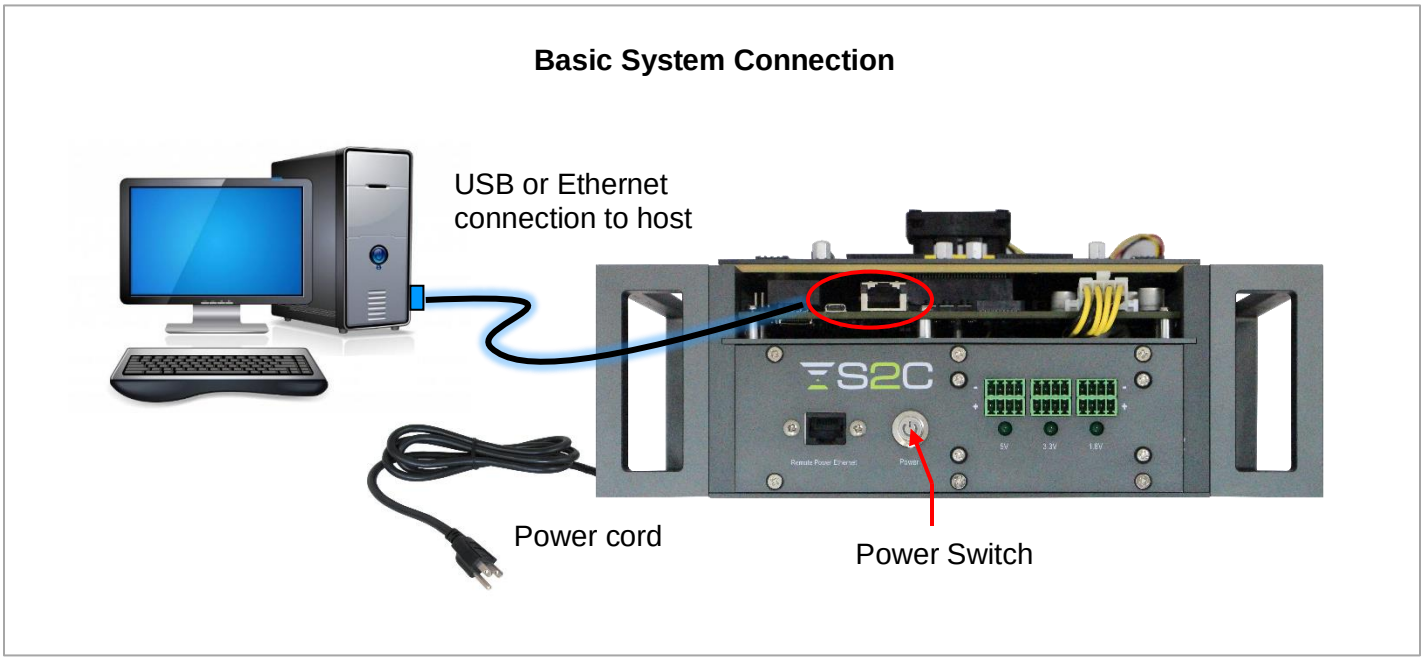

Figure 4-1 Single-VU19P Front Panel and Basic Connections

Once the PCM VU19PS is powered on, the power status **P_LED7** will light up. Then you will find **P_LED1** and **P_LED2** light up soon afterwards. It indicates that S2C's bit file has been downloaded to LM controller successfully.

Warning: If any of the red LEDs (**P_LED10, P_LED11, P_LED12 and P_LED13**) light up, it indicates a power fault has occurred. Turn power off immediately and contact your S2C support.

Please note that when the FPGA is powered on, the temperature may rise. Single VU19P Logic System supports temperature monitor capability and provides a mechanism to shut down the FPGA Module VU19P when the temperature surpasses the prescribed limit. Please take adequate care and follow safety guidelines discussed in Chapter 8, "Care and Handling" to avoid Intel FPGA overheating. If you have an overheating problem, contact S2C support.

If your design requires interfacing with a target board, it can be directly mounted onto FPGA Module VU19P or connected through a Samtec 300-pin cable (refer to Figure 6-1 for more details).

4.3 Dedicated I/O Voltage Adjustment

User FPGA **(U1)** on FPGA Module VU19P has 1,152 Dedicated I/Os that can be accessed from eight Prodigy connectors J1, J2, J3, J4, J5, J6, J7 and J8. All Dedicated I/O voltages can be easily adjusted to 1.2V, 1.35V, 1.5V or 1.8V through runtime software in GUI.

These eight Prodigy connectors are separated into 8 power regions, each being controlled by the LM controller. Once being powered on, LM controller will configure the Dedicated I/O voltages according to the last saved configuration.

Table 4-1 Default Switch Settings – FPGA Module VU19P

Switch	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
S1	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S2	ON	ON	ON	ON						

Table 4-2 Default Switch Settings – PCM VU19PS

Switch	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
P_S1	ON	OFF	ON	OFF	ON	OFF	ON	OFF
P_S2	OFF	ON	ON	ON	ON	ON		
P_S3	OFF	OFF	OFF	OFF	OFF	OFF		
P_S4	ON	ON	ON	ON				
P_S5	ON	ON	ON	ON	ON	ON	ON	ON
P_S6	ON	ON	ON	ON	ON	ON		
P_S7	ON	ON						
P_S8	ON	ON	ON	ON	ON	ON		

4.4 Downloading Hardware

You have four different options to download the design file into the user FPGA. Using Micro USB port, Xilinx USB-Blaster, Micro SD card or Ethernet port. For downloading design using Micro USB port **(P_J3)**, Ethernet port **(P_J4)** or Micro SD card **(P_J5)**, please refer to **Player Pro Reference Manual**. These three ports are on PCM VU19PS.

For downloading design using Xilinx USB-Blaster, plug the USB-Blaster into JTAG header **(J15)** and refer to Xilinx documentation. (For JTAG pins and signal information refer to the appendix). The JTAG header is on FPGA Module VU19P.

When the user FPGA U1 download is successful, LED1 will light up.

Table 4-3 displays the default status for all LEDs on FPGA Module VU19P; Table 4-4 displays the default status for all LEDs on PCM VU19PS. Please check them after power on the Single VU19P Logic System.

Table 4-3 LED Default Status on FPGA Module

LED	Status	Description
LED1 (Green)	ON	User FPGA Config Done
LED2 (Green)	ON	TDM Done
LED3 (Green)	OFF	Power supply of J1 is +1.8V
LED4 (Green)	OFF	Power supply of J1 is +1.5V
LED5 (Green)	OFF	Power supply of J1 is +1.35V
LED6 (Green)	ON	Power supply of J1 is +1.2V
LED7 (Green)	OFF	Power supply of J2 is +1.8V
LED8 (Green)	OFF	Power supply of J2 is +1.5V
LED9 (Green)	OFF	Power supply of J2 is +1.35V
LED10 (Green)	ON	Power supply of J2 is +1.2V
LED11 (Green)	OFF	Power supply of J3 is +1.8V
LED12 (Green)	OFF	Power supply of J3 is +1.5V
LED13 (Green)	OFF	Power supply of J3 is +1.35V
LED14 (Green)	ON	Power supply of J3 is +1.2V
LED15 (Green)	OFF	Power supply of J4 is +1.8V
LED16 (Green)	OFF	Power supply of J4 is +1.5V
LED17 (Green)	OFF	Power supply of J4 is +1.35V
LED18 (Green)	ON	Power supply of J4 is +1.2V
LED19 (Green)	OFF	Power supply of J5 is +1.8V
LED20 (Green)	OFF	Power supply of J5 is +1.5V
LED21 (Green)	OFF	Power supply of J5 is +1.35V
LED22 (Green)	ON	Power supply of J5 is +1.2V
LED23 (Green)	OFF	Power supply of J6 is +1.8V
LED24 (Green)	OFF	Power supply of J6 is +1.5V
LED25 (Green)	OFF	Power supply of J6 is +1.35V
LED26 (Green)	ON	Power supply of J6 is +1.2V
LED27 (Green)	OFF	Power supply of J7 is +1.8V
LED28 (Green)	OFF	Power supply of J7 is +1.5V
LED29 (Green)	OFF	Power supply of J7 is +1.35V
LED30 (Green)	ON	Power supply of J7 is +1.2V
LED31 (Green)	OFF	Power supply of J8 is +1.8V
LED32 (Green)	OFF	Power supply of J8 is +1.5V
LED33 (Green)	OFF	Power supply of J8 is +1.35V
LED34 (Green)	ON	Power supply of J8 is +1.2V
LED35 (Green)	OFF	User LED1
LED36 (Green)	OFF	User LED2
LED37 (Green)	OFF	User LED3

Table 4-4 LED Default Status on PCM

LED	Status	Description
P_LED1 (Green)	ON	SoC FPGA Config Done
P_LED2 (Green)	ON	SoC ARM Boot Done
P_LED3 (Green)	ON	12V Power On
P_LED4 (Green)	ON	Power supply of User FPGA is correct
P_LED5 (Green)	ON	Power supply of User FPGA is correct
P_LED6 (Red)	OFF	Power supply of User FPGA occurred fault1
P_LED7 (Red)	OFF	Power supply of User FPGA occurred fault2
P_LED8 (Green)	ON	Power supply of SoC FPGA is correct
P_LED9 (Green)	ON	Power supply of SoC FPGA is correct
P_LED10 (Red)	OFF	Power supply of User FPGA occurred fault1
P_LED11 (Red)	OFF	Power supply of User FPGA occurred fault2

5 Appendix 1: External Connector Tables

Single VU19P Logic System has six types of I/O:

- Global clock I/O
- Gigabit transceiver I/O
- Dedicated I/O
- Interconnection I/O
- DDR4 SODIMM I/O
- User I/O

This section provides the relationship between the various I/Os and their corresponding FPGA pinout.

J1, J2, J3, J4, J5, J6, J7 and J8 use Samtec SEAF 300-pin connectors. They are on top side of FPGA Module VU19P. They have pin orientations corresponding to the layout indicated in the figure below.

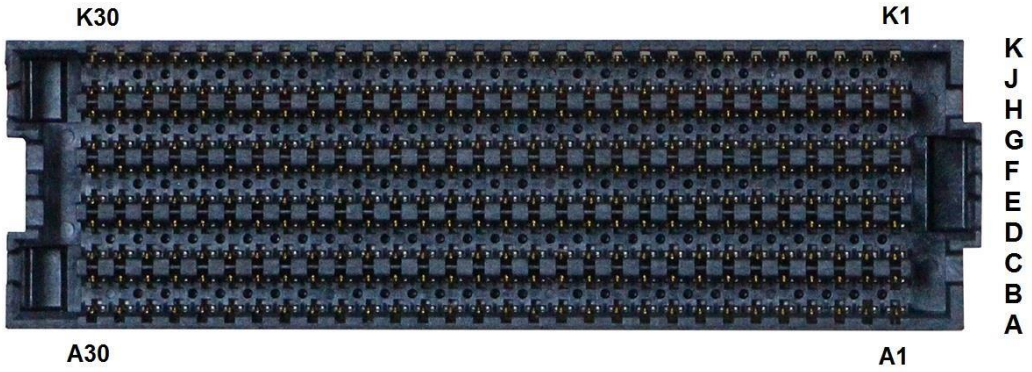

Figure 5-1 FPGA Module VU19P SEAF 300-pin Connector Locations

JX1 and JX2 use Samtec SEAF 120-pin connectors. They are on top side of FPGA Module VU19P. They have pin orientations corresponding to the layout indicated in the figure below:

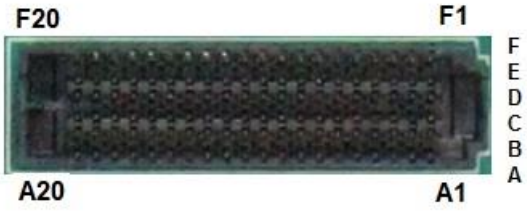

Figure 5-2 FPGA Module VU19P SEAF 120-pin Connector Locations

5.1 Global Clocks

A total of 8 global clocks can be input from 8 pairs of programmable LVDS clocks or System Control Connector **P_JS1**, which are respectively selected through runtime software in GUI.

These 8 global clocks are routed to the GC pins of the user FPGA. Otherwise there are 3 pairs of LVDS clock output from the user FPGA to the System Control Connector **P_JS1**.

SC Clock Module Type D provides 5 pairs of LVDS clock inputs on MMCX, 1 single-ended OSC socket and 3 pairs of LVDS clock outputs on MMCX. The following table provides detailed information on the 8 global clock input and 3 clock output.

Table 5-1 Global Clock Properties

Global Clock	Clock source	U1 Pin No.	I/O standard	Differential Termination Attribute
Programmable clock pair1 or JS1 clock pair1	U23.22(P)/U23.21(N)	CA17(P)/CA16(N)	LVDS	DIFF_TERM = TRUE
	JS1.03(P)/JS1.01(N)			
Programmable clock pair2 or JS1 clock pair2	U23.18(P)/U23.17(N)	CB19(P)/CB18(N)	LVDS	DIFF_TERM = TRUE
	JS1.07(P)/JS1.05(N)			
Programmable clock pair3 or JS1 clock pair3	U23.14(P)/U23.13(N)	BY38(P)/BY39(N)	LVDS	DIFF_TERM = TRUE
	JS1.11(P)/JS1.09(N)			
Programmable clock pair4 or JS1 clock pair4	U24.22(P)/U24.21(N)	CA36(P)/CA37(N)	LVDS	DIFF_TERM = TRUE
	JS1.15(P)/JS1.13(N)			
Programmable clock pair5 or JS1 clock pair5	U24.18(P)/U24.17(N)	C35(P)/C36(N)	LVDS	DIFF_TERM = TRUE
	JS1.19(P)/JS1.17(N)			
Programmable clock pair6 or JS1 clock pair6	U24.14(P)/U24.13(N)	R42(P)/R43(N)	LVDS	DIFF_TERM = TRUE
	JS1.23(P)/JS1.21(N)			
Programmable clock pair7	U23.10(P)/U23.9(N)	Y52(P)/Y53(N)	LVDS	DIFF_TERM = FALSE
Programmable clock pair8	U24.10(P)/U24.9(N)	AY50(P)/BA50(N)	LVDS	DIFF_TERM = FALSE
Clock output pair1	JS1.31(P)/JS1.29(N)	BR37(P)/BR38(N)	LVDS	
Clock output pair2	JS1.35(P)/JS1.33(N)	BU36(P)/BV36(N)	LVDS	
Clock output pair3	JS1.39(P)/JS1.37(N)	BU38(P)/BV38(N)	LVDS	

5.2 Gigabit Transceiver I/O

The user FPGA has 16 XCVR (Gigabit transceivers), which are connected to the Prodigy GT connectors JX1 and JX2. The function of each of the 16 XCVR is defined by the user.

Table 5-2 PGT Connector – JX1

JX1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
C19	BE10	MGTREFCLK0N_226	Bank226	
D19	BE11	MGTREFCLK0P_226	Bank226	
A16	BD3	MGTYRXN0_226	Bank226	
B16	BD4	MGTYRXP0_226	Bank226	
A14	BC1	MGTYRXN1_226	Bank226	
B14	BC2	MGTYRXP1_226	Bank226	
A12	BB3	MGTYRXN2_226	Bank226	
B12	BB4	MGTYRXP2_226	Bank226	
A10	BA1	MGTYRXN3_226	Bank226	
B10	BA2	MGTYRXP3_226	Bank226	
C17	BF8	MGTYTXN0_226	Bank226	
D17	BF9	MGTYTXP0_226	Bank226	
C15	BE6	MGTYTXN1_226	Bank226	
D15	BE7	MGTYTXP1_226	Bank226	
C13	BD8	MGTYTXN2_226	Bank226	
D13	BD9	MGTYTXP2_226	Bank226	
C11	BC6	MGTYTXN3_226	Bank226	
D11	BC7	MGTYTXP3_226	Bank226	
A18	BA10	MGTREFCLK0N_227	Bank227	
B18	BA11	MGTREFCLK0P_227	Bank227	
A8	AY3	MGTYRXN0_227	Bank227	
B8	AY4	MGTYRXP0_227	Bank227	
A6	AW1	MGTYRXN1_227	Bank227	
B6	AW2	MGTYRXP1_227	Bank227	
A4	AV3	MGTYRXN2_227	Bank227	
B4	AV4	MGTYRXP2_227	Bank227	
A2	AU1	MGTYRXN3_227	Bank227	
B2	AU2	MGTYRXP3_227	Bank227	
C9	BB8	MGTYTXN0_227	Bank227	
D9	BB9	MGTYTXP0_227	Bank227	
C7	BA6	MGTYTXN1_227	Bank227	
D7	BA7	MGTYTXP1_227	Bank227	
C5	AY8	MGTYTXN2_227	Bank227	
D5	AY9	MGTYTXP2_227	Bank227	
C3	AW6	MGTYTXN3_227	Bank227	

JX1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D3	AW7	MGTYTXP3_227	Bank227	
E2	BY13	IO_L23N_T3U_N9_59	Bank59	1.8V
F2	BW13	IO_L23P_T3U_N8_59	Bank59	1.8V
E4	BY17	IO_L15N_T2L_N5_AD11N_59	Bank59	1.8V
F4	BW17	IO_L15P_T2L_N4_AD11P_59	Bank59	1.8V
E6	CA11	IO_L21N_T3L_N5_AD8N_59	Bank59	1.8V
F6	CA12	IO_L21P_T3L_N4_AD8P_59	Bank59	1.8V
E12	CC11	IO_L19N_T3L_N1_DBC_AD9N_59	Bank59	1.8V
E14	CB16	IO_L14N_T2L_N3_GC_59	Bank59	1.8V
F14	CB17	IO_L14P_T2L_N2_GC_59	Bank59	1.8V
F12	CB11	IO_L19P_T3L_N0_DBC_AD9P_59	Bank59	1.8V
E16	CB13	IO_L24P_T3U_N10_59	Bank59	1.8V
F16	CB12	IO_L24N_T3U_N11_59	Bank59	1.8V
E18	CB14	IO_L20N_T3L_N3_AD1N_59	Bank59	1.8V
F18	CC13	IO_L22N_T3U_N7_DBC_AD0N_59	Bank59	1.8V
E20	CA14	IO_L20P_T3L_N2_AD1P_59	Bank59	1.8V
F20	CC14	IO_L22P_T3U_N6_DBC_AD0P_59	Bank59	1.8V

Note: There is on board LVDS oscillator X2 which is 156.25MHz. It is connected to Bank226 MGTREFCLK1P_226/ MGTREFCLK1N_226 (BC11/BC10).

Table 5-3 PGT Connector – JX2

JX2 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
C19	AU10	MGTREFCLK0N_230	Bank230	
D19	AU11	MGTREFCLK0P_230	Bank230	
A16	AT3	MGTYRXN0_230	Bank230	
B16	AT4	MGTYRXP0_230	Bank230	
A14	AR1	MGTYRXN1_230	Bank230	
B14	AR2	MGTYRXP1_230	Bank230	
A12	AP3	MGTYRXN2_230	Bank230	
B12	AP4	MGTYRXP2_230	Bank230	
A10	AN1	MGTYRXN3_230	Bank230	
B10	AN2	MGTYRXP3_230	Bank230	
C17	AV8	MGTYTXN0_230	Bank230	
D17	AV9	MGTYTXP0_230	Bank230	
C15	AU6	MGTYTXN1_230	Bank230	
D15	AU7	MGTYTXP1_230	Bank230	
C13	AT8	MGTYTXN2_230	Bank230	
D13	AT9	MGTYTXP2_230	Bank230	
C11	AR6	MGTYTXN3_230	Bank230	

JX2 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D11	AR7	MGTYTXP3_230	Bank230	
A18	AR10	MGTREFCLK0N_231	Bank231	
B18	AR11	MGTREFCLK0P_231	Bank231	
A8	AM3	MGTYRXN0_231	Bank231	
B8	AM4	MGTYRXP0_231	Bank231	
A6	AL1	MGTYRXN1_231	Bank231	
B6	AL2	MGTYRXP1_231	Bank231	
A4	AK3	MGTYRXN2_231	Bank231	
B4	AK4	MGTYRXP2_231	Bank231	
A2	AJ1	MGTYRXN3_231	Bank231	
B2	AJ2	MGTYRXP3_231	Bank231	
C9	AP8	MGTYTXN0_231	Bank231	
D9	AP9	MGTYTXP0_231	Bank231	
C7	AN6	MGTYTXN1_231	Bank231	
D7	AN7	MGTYTXP1_231	Bank231	
C5	AM8	MGTYTXN2_231	Bank231	
D5	AM9	MGTYTXP2_231	Bank231	
C3	AL6	MGTYTXN3_231	Bank231	
D3	AL7	MGTYTXP3_231	Bank231	
E2	BW21	IO_L5N_T0U_N9_AD14N_59	Bank59	1.8V
F2	BV21	IO_L5P_T0U_N8_AD14P_59	Bank59	1.8V
E4	BV19	IO_L10N_T1U_N7_QBC_AD4N_59	Bank59	1.8V
F4	BV20	IO_L10P_T1U_N6_QBC_AD4P_59	Bank59	1.8V
E6	BY22	IO_L1N_T0L_N1_DBC_59	Bank59	1.8V
F6	BW22	IO_L3N_T0L_N5_AD15N_59	Bank59	1.8V
E12	CB21	IO_L4N_T0U_N7_DBC_AD7N_59	Bank59	1.8V
E14	CA19	IO_L11N_T1U_N9_GC_59	Bank59	1.8V
F14	BY19	IO_L11P_T1U_N8_GC_59	Bank59	1.8V
F12	CA21	IO_L6N_T0U_N11_AD6N_59	Bank59	1.8V
E16	CB22	IO_L4P_T0U_N6_DBC_AD7P_59	Bank59	1.8V
F16	CA22	IO_L6P_T0U_N10_AD6P_59	Bank59	1.8V
E18	CB23	IO_L2P_T0L_N2_59	Bank59	1.8V
F18	CC23	IO_L2N_T0L_N3_59	Bank59	1.8V
E20	BW23	IO_L3P_T0L_N4_AD15P_59	Bank59	1.8V
F20	BY23	IO_L1P_T0L_N0_DBC_59	Bank59	1.8V

Note: There is on board LVDS oscillator X3 which is 156.25MHz. It is connected to Bank231 MGTREFCLK1P_231/ MGTREFCLK1N_231 (AP13/AP12).

5.3 Dedicated I/O

Dedicated I/O connectors are labeled as J1, J2, J3, J4, J5, J6, J7 and J8. They are used to connect Prodigy Logic System to user Prodigy daughter cards or Prodigy cables. Every I/O is directly wire-linked to one FPGA I/O pin.

J1, J3, J4, J5, J6, J7, J8 support 72 differential pairs or 144 single-ended I/O plus 4 GTY. J2 only support 72 differential pairs or 144 single-ended I/O. The following table shows the connections of all dedicated I/O connector pins and their corresponding FPGA pins.

Table 5-4 Prodigy Connector – J1

J1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	AH3	MGTYRXN0_232	Bank232	
A14	AH4	MGTYRXP0_232	Bank232	
A11	AG1	MGTYRXN1_232	Bank232	
A10	AG2	MGTYRXP1_232	Bank232	
A7	AF3	MGTYRXN2_232	Bank232	
A6	AF4	MGTYRXP2_232	Bank232	
A3	AE1	MGTYRXN3_232	Bank232	
A2	AE2	MGTYRXP3_232	Bank232	
B17	AK8	MGTYTXN0_232	Bank232	
B16	AK9	MGTYTXP0_232	Bank232	
B13	AJ6	MGTYTXN1_232	Bank232	
B12	AJ7	MGTYTXP1_232	Bank232	
B9	AH8	MGTYTXN2_232	Bank232	
B8	AH9	MGTYTXP2_232	Bank232	
B5	AG6	MGTYTXN3_232	Bank232	
B4	AG7	MGTYTXP3_232	Bank232	
A19	AN10	MGTREFCLK0N_232	Bank232	
A18	AN11	MGTREFCLK0P_232	Bank232	
B21	AL10	MGTREFCLK1N_232	Bank232	
B20	AL11	MGTREFCLK1P_232	Bank232	
C3	R15	IO_L1N_T0L_N1_DBC_76	Bank76	1.2V,1.35V,1.5V,1.8V
C2	T15	IO_L1P_T0L_N0_DBC_76	Bank76	1.2V,1.35V,1.5V,1.8V
C7	M14	IO_L2N_T0L_N3_76	Bank76	1.2V,1.35V,1.5V,1.8V
C6	N14	IO_L2P_T0L_N2_76	Bank76	1.2V,1.35V,1.5V,1.8V
C11	N15	IO_L3N_T0L_N5_AD15N_76	Bank76	1.2V,1.35V,1.5V,1.8V
C10	P15	IO_L3P_T0L_N4_AD15P_76	Bank76	1.2V,1.35V,1.5V,1.8V
D2	P13	IO_L4N_T0U_N7_DBC_AD7N_76	Bank76	1.2V,1.35V,1.5V,1.8V
D1	R13	IO_L4P_T0U_N6_DBC_AD7P_76	Bank76	1.2V,1.35V,1.5V,1.8V
D5	R14	IO_L5N_T0U_N9_AD14N_76	Bank76	1.2V,1.35V,1.5V,1.8V
D4	T14	IO_L5P_T0U_N8_AD14P_76	Bank76	1.2V,1.35V,1.5V,1.8V
D8	M13	IO_L6N_T0U_N11_AD6N_76	Bank76	1.2V,1.35V,1.5V,1.8V

J1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D7	N13	IO_L6P_T0U_N10_AD6P_76	Bank76	1.2V,1.35V,1.5V,1.8V
E3	K12	IO_L7N_T1L_N1_QBC_AD13N_76	Bank76	1.2V,1.35V,1.5V,1.8V
E2	L12	IO_L7P_T1L_N0_QBC_AD13P_76	Bank76	1.2V,1.35V,1.5V,1.8V
E6	J12	IO_L8N_T1L_N3_AD5N_76	Bank76	1.2V,1.35V,1.5V,1.8V
E5	J13	IO_L8P_T1L_N2_AD5P_76	Bank76	1.2V,1.35V,1.5V,1.8V
E9	K13	IO_L9N_T1L_N5_AD12N_76	Bank76	1.2V,1.35V,1.5V,1.8V
E8	K14	IO_L9P_T1L_N4_AD12P_76	Bank76	1.2V,1.35V,1.5V,1.8V
F2	J15	IO_L10N_T1U_N7_QBC_AD4N_76	Bank76	1.2V,1.35V,1.5V,1.8V
F1	K15	IO_L10P_T1U_N6_QBC_AD4P_76	Bank76	1.2V,1.35V,1.5V,1.8V
F5	H14	IO_L11N_T1U_N9_GC_76	Bank76	1.2V,1.35V,1.5V,1.8V
F4	H15	IO_L11P_T1U_N8_GC_76	Bank76	1.2V,1.35V,1.5V,1.8V
F8	G13	IO_L12N_T1U_N11_GC_76	Bank76	1.2V,1.35V,1.5V,1.8V
F7	H13	IO_L12P_T1U_N10_GC_76	Bank76	1.2V,1.35V,1.5V,1.8V
G3	F14	IO_L13N_T2L_N1_GC_QBC_76	Bank76	1.2V,1.35V,1.5V,1.8V
G2	G14	IO_L13P_T2L_N0_GC_QBC_76	Bank76	1.2V,1.35V,1.5V,1.8V
G6	E15	IO_L14N_T2L_N3_GC_76	Bank76	1.2V,1.35V,1.5V,1.8V
G5	F15	IO_L14P_T2L_N2_GC_76	Bank76	1.2V,1.35V,1.5V,1.8V
G9	D15	IO_L15N_T2L_N5_AD11N_76	Bank76	1.2V,1.35V,1.5V,1.8V
G8	D16	IO_L15P_T2L_N4_AD11P_76	Bank76	1.2V,1.35V,1.5V,1.8V
G12	E13	IO_L16N_T2U_N7_QBC_AD3N_76	Bank76	1.2V,1.35V,1.5V,1.8V
G11	E14	IO_L16P_T2U_N6_QBC_AD3P_76	Bank76	1.2V,1.35V,1.5V,1.8V
H2	F12	IO_L17N_T2U_N9_AD10N_76	Bank76	1.2V,1.35V,1.5V,1.8V
H1	G12	IO_L17P_T2U_N8_AD10P_76	Bank76	1.2V,1.35V,1.5V,1.8V
H5	D12	IO_L18N_T2U_N11_AD2N_76	Bank76	1.2V,1.35V,1.5V,1.8V
H4	E12	IO_L18P_T2U_N10_AD2P_76	Bank76	1.2V,1.35V,1.5V,1.8V
H8	A16	IO_L19N_T3L_N1_DBC_AD9N_76	Bank76	1.2V,1.35V,1.5V,1.8V
H7	B16	IO_L19P_T3L_N0_DBC_AD9P_76	Bank76	1.2V,1.35V,1.5V,1.8V
J3	A12	IO_L20N_T3L_N3_AD1N_76	Bank76	1.2V,1.35V,1.5V,1.8V
J2	B12	IO_L20P_T3L_N2_AD1P_76	Bank76	1.2V,1.35V,1.5V,1.8V
J6	B14	IO_L21N_T3L_N5_AD8N_76	Bank76	1.2V,1.35V,1.5V,1.8V
J5	C14	IO_L21P_T3L_N4_AD8P_76	Bank76	1.2V,1.35V,1.5V,1.8V
J9	C13	IO_L22N_T3U_N7_DBC_AD0N_76	Bank76	1.2V,1.35V,1.5V,1.8V
J8	D13	IO_L22P_T3U_N6_DBC_AD0P_76	Bank76	1.2V,1.35V,1.5V,1.8V
K2	A14	IO_L23N_T3U_N9_76	Bank76	1.2V,1.35V,1.5V,1.8V
K1	A15	IO_L23P_T3U_N8_76	Bank76	1.2V,1.35V,1.5V,1.8V
K5	C15	IO_L24N_T3U_N11_76	Bank76	1.2V,1.35V,1.5V,1.8V
K4	C16	IO_L24P_T3U_N10_76	Bank76	1.2V,1.35V,1.5V,1.8V
C15	M8	IO_L1N_T0L_N1_DBC_77	Bank77	1.2V,1.35V,1.5V,1.8V
C14	N8	IO_L1P_T0L_N0_DBC_77	Bank77	1.2V,1.35V,1.5V,1.8V
C19	M11	IO_L2N_T0L_N3_77	Bank77	1.2V,1.35V,1.5V,1.8V
C18	N11	IO_L2P_T0L_N2_77	Bank77	1.2V,1.35V,1.5V,1.8V
C23	M9	IO_L3N_T0L_N5_AD15N_77	Bank77	1.2V,1.35V,1.5V,1.8V
C22	N9	IO_L3P_T0L_N4_AD15P_77	Bank77	1.2V,1.35V,1.5V,1.8V

J1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D13	P11	IO_L4N_T0U_N7_DBC_AD7N_77	Bank77	1.2V,1.35V,1.5V,1.8V
D12	R11	IO_L4P_T0U_N6_DBC_AD7P_77	Bank77	1.2V,1.35V,1.5V,1.8V
D17	N10	IO_L5N_T0U_N9_AD14N_77	Bank77	1.2V,1.35V,1.5V,1.8V
D16	P10	IO_L5P_T0U_N8_AD14P_77	Bank77	1.2V,1.35V,1.5V,1.8V
D20	P12	IO_L6N_T0U_N11_AD6N_77	Bank77	1.2V,1.35V,1.5V,1.8V
D19	R12	IO_L6P_T0U_N10_AD6P_77	Bank77	1.2V,1.35V,1.5V,1.8V
E12	K7	IO_L7N_T1L_N1_QBC_AD13N_77	Bank77	1.2V,1.35V,1.5V,1.8V
E11	L7	IO_L7P_T1L_N0_QBC_AD13P_77	Bank77	1.2V,1.35V,1.5V,1.8V
E15	J7	IO_L8N_T1L_N3_AD5N_77	Bank77	1.2V,1.35V,1.5V,1.8V
E14	J8	IO_L8P_T1L_N2_AD5P_77	Bank77	1.2V,1.35V,1.5V,1.8V
E18	H11	IO_L9N_T1L_N5_AD12N_77	Bank77	1.2V,1.35V,1.5V,1.8V
E17	J11	IO_L9P_T1L_N4_AD12P_77	Bank77	1.2V,1.35V,1.5V,1.8V
F11	L10	IO_L10N_T1U_N7_QBC_AD4N_77	Bank77	1.2V,1.35V,1.5V,1.8V
F10	L11	IO_L10P_T1U_N6_QBC_AD4P_77	Bank77	1.2V,1.35V,1.5V,1.8V
F14	J10	IO_L11N_T1U_N9_GC_77	Bank77	1.2V,1.35V,1.5V,1.8V
F13	K10	IO_L11P_T1U_N8_GC_77	Bank77	1.2V,1.35V,1.5V,1.8V
F17	K8	IO_L12N_T1U_N11_GC_77	Bank77	1.2V,1.35V,1.5V,1.8V
F16	K9	IO_L12P_T1U_N10_GC_77	Bank77	1.2V,1.35V,1.5V,1.8V
G15	F9	IO_L13N_T2L_N1_GC_QBC_77	Bank77	1.2V,1.35V,1.5V,1.8V
G14	G9	IO_L13P_T2L_N0_GC_QBC_77	Bank77	1.2V,1.35V,1.5V,1.8V
G18	H9	IO_L14N_T2L_N3_GC_77	Bank77	1.2V,1.35V,1.5V,1.8V
G17	H10	IO_L14P_T2L_N2_GC_77	Bank77	1.2V,1.35V,1.5V,1.8V
G21	F11	IO_L15N_T2L_N5_AD11N_77	Bank77	1.2V,1.35V,1.5V,1.8V
G20	G11	IO_L15P_T2L_N4_AD11P_77	Bank77	1.2V,1.35V,1.5V,1.8V
H11	G7	IO_L16N_T2U_N7_QBC_AD3N_77	Bank77	1.2V,1.35V,1.5V,1.8V
H10	G8	IO_L16P_T2U_N6_QBC_AD3P_77	Bank77	1.2V,1.35V,1.5V,1.8V
H14	E8	IO_L17N_T2U_N9_AD10N_77	Bank77	1.2V,1.35V,1.5V,1.8V
H13	E9	IO_L17P_T2U_N8_AD10P_77	Bank77	1.2V,1.35V,1.5V,1.8V
H17	E10	IO_L18N_T2U_N11_AD2N_77	Bank77	1.2V,1.35V,1.5V,1.8V
H16	F10	IO_L18P_T2U_N10_AD2P_77	Bank77	1.2V,1.35V,1.5V,1.8V
H20	C10	IO_L19N_T3L_N1_DBC_AD9N_77	Bank77	1.2V,1.35V,1.5V,1.8V
H19	C11	IO_L19P_T3L_N0_DBC_AD9P_77	Bank77	1.2V,1.35V,1.5V,1.8V
J12	D10	IO_L20N_T3L_N3_AD1N_77	Bank77	1.2V,1.35V,1.5V,1.8V
J11	D11	IO_L20P_T3L_N2_AD1P_77	Bank77	1.2V,1.35V,1.5V,1.8V
J15	A11	IO_L21N_T3L_N5_AD8N_77	Bank77	1.2V,1.35V,1.5V,1.8V
J14	B11	IO_L21P_T3L_N4_AD8P_77	Bank77	1.2V,1.35V,1.5V,1.8V
J18	C8	IO_L22N_T3U_N7_DBC_AD0N_77	Bank77	1.2V,1.35V,1.5V,1.8V
J17	C9	IO_L22P_T3U_N6_DBC_AD0P_77	Bank77	1.2V,1.35V,1.5V,1.8V
K11	A9	IO_L23N_T3U_N9_77	Bank77	1.2V,1.35V,1.5V,1.8V
K10	A10	IO_L23P_T3U_N8_77	Bank77	1.2V,1.35V,1.5V,1.8V
K14	B8	IO_L24N_T3U_N11_77	Bank77	1.2V,1.35V,1.5V,1.8V
K13	B9	IO_L24P_T3U_N10_77	Bank77	1.2V,1.35V,1.5V,1.8V
C27	A7	IO_L1N_T0L_N1_DBC_78	Bank78	1.2V,1.35V,1.5V,1.8V

J1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
C26	B7	IO_L1P_T0L_N0_DBC_78	Bank78	1.2V,1.35V,1.5V,1.8V
C30	C5	IO_L2N_T0L_N3_78	Bank78	1.2V,1.35V,1.5V,1.8V
C29	D5	IO_L2P_T0L_N2_78	Bank78	1.2V,1.35V,1.5V,1.8V
D25	A5	IO_L3N_T0L_N5_AD15N_78	Bank78	1.2V,1.35V,1.5V,1.8V
D24	A6	IO_L3P_T0L_N4_AD15P_78	Bank78	1.2V,1.35V,1.5V,1.8V
D28	F6	IO_L4N_T0U_N7_DBC_AD7N_78	Bank78	1.2V,1.35V,1.5V,1.8V
D27	F7	IO_L4P_T0U_N6_DBC_AD7P_78	Bank78	1.2V,1.35V,1.5V,1.8V
E21	B6	IO_L5N_T0U_N9_AD14N_78	Bank78	1.2V,1.35V,1.5V,1.8V
E20	C6	IO_L5P_T0U_N8_AD14P_78	Bank78	1.2V,1.35V,1.5V,1.8V
E24	D6	IO_L6N_T0U_N11_AD6N_78	Bank78	1.2V,1.35V,1.5V,1.8V
E23	D7	IO_L6P_T0U_N10_AD6P_78	Bank78	1.2V,1.35V,1.5V,1.8V
E27	B4	IO_L7N_T1L_N1_QBC_AD13N_78	Bank78	1.2V,1.35V,1.5V,1.8V
E26	C4	IO_L7P_T1L_N0_QBC_AD13P_78	Bank78	1.2V,1.35V,1.5V,1.8V
E30	E2	IO_L8N_T1L_N3_AD5N_78	Bank78	1.2V,1.35V,1.5V,1.8V
E29	E3	IO_L8P_T1L_N2_AD5P_78	Bank78	1.2V,1.35V,1.5V,1.8V
F20	C3	IO_L9N_T1L_N5_AD12N_78	Bank78	1.2V,1.35V,1.5V,1.8V
F19	D3	IO_L9P_T1L_N4_AD12P_78	Bank78	1.2V,1.35V,1.5V,1.8V
F23	F1	IO_L10N_T1U_N7_QBC_AD4N_78	Bank78	1.2V,1.35V,1.5V,1.8V
F22	F2	IO_L10P_T1U_N6_QBC_AD4P_78	Bank78	1.2V,1.35V,1.5V,1.8V
F26	E4	IO_L11N_T1U_N9_GC_78	Bank78	1.2V,1.35V,1.5V,1.8V
F25	E5	IO_L11P_T1U_N8_GC_78	Bank78	1.2V,1.35V,1.5V,1.8V
F29	F4	IO_L12N_T1U_N11_GC_78	Bank78	1.2V,1.35V,1.5V,1.8V
F28	F5	IO_L12P_T1U_N10_GC_78	Bank78	1.2V,1.35V,1.5V,1.8V
G24	G3	IO_L13N_T2L_N1_GC_QBC_78	Bank78	1.2V,1.35V,1.5V,1.8V
G23	G4	IO_L13P_T2L_N0_GC_QBC_78	Bank78	1.2V,1.35V,1.5V,1.8V
G27	H3	IO_L14N_T2L_N3_GC_78	Bank78	1.2V,1.35V,1.5V,1.8V
G26	H4	IO_L14P_T2L_N2_GC_78	Bank78	1.2V,1.35V,1.5V,1.8V
G30	G1	IO_L15N_T2L_N5_AD11N_78	Bank78	1.2V,1.35V,1.5V,1.8V
G29	G2	IO_L15P_T2L_N4_AD11P_78	Bank78	1.2V,1.35V,1.5V,1.8V
H23	J2	IO_L16N_T2U_N7_QBC_AD3N_78	Bank78	1.2V,1.35V,1.5V,1.8V
H22	J3	IO_L16P_T2U_N6_QBC_AD3P_78	Bank78	1.2V,1.35V,1.5V,1.8V
H26	H1	IO_L17N_T2U_N9_AD10N_78	Bank78	1.2V,1.35V,1.5V,1.8V
H25	J1	IO_L17P_T2U_N8_AD10P_78	Bank78	1.2V,1.35V,1.5V,1.8V
H29	H5	IO_L18N_T2U_N11_AD2N_78	Bank78	1.2V,1.35V,1.5V,1.8V
H28	H6	IO_L18P_T2U_N10_AD2P_78	Bank78	1.2V,1.35V,1.5V,1.8V
J21	K5	IO_L19N_T3L_N1_DBC_AD9N_78	Bank78	1.2V,1.35V,1.5V,1.8V
J20	L5	IO_L19P_T3L_N0_DBC_AD9P_78	Bank78	1.2V,1.35V,1.5V,1.8V
J24	J5	IO_L20N_T3L_N3_AD1N_78	Bank78	1.2V,1.35V,1.5V,1.8V
J23	J6	IO_L20P_T3L_N2_AD1P_78	Bank78	1.2V,1.35V,1.5V,1.8V
J27	K2	IO_L21N_T3L_N5_AD8N_78	Bank78	1.2V,1.35V,1.5V,1.8V
J26	K3	IO_L21P_T3L_N4_AD8P_78	Bank78	1.2V,1.35V,1.5V,1.8V
J30	L4	IO_L22N_T3U_N7_DBC_AD0N_78	Bank78	1.2V,1.35V,1.5V,1.8V
J29	M4	IO_L22P_T3U_N6_DBC_AD0P_78	Bank78	1.2V,1.35V,1.5V,1.8V

J1 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
K20	L1	IO_L23N_T3U_N9_78	Bank78	1.2V,1.35V,1.5V,1.8V
K19	L2	IO_L23P_T3U_N8_78	Bank78	1.2V,1.35V,1.5V,1.8V
K23	L6	IO_L24N_T3U_N11_78	Bank78	1.2V,1.35V,1.5V,1.8V
K22	M6	IO_L24P_T3U_N10_78	Bank78	1.2V,1.35V,1.5V,1.8V

Table 5-5 Prodigy Connector – J2

J2 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
C3	W22	IO_L1N_T0L_N1_DBC_73	Bank73	1.2V,1.35V,1.5V,1.8V
C2	W23	IO_L1P_T0L_N0_DBC_73	Bank73	1.2V,1.35V,1.5V,1.8V
C7	U24	IO_L2N_T0L_N3_73	Bank73	1.2V,1.35V,1.5V,1.8V
C6	V24	IO_L2P_T0L_N2_73	Bank73	1.2V,1.35V,1.5V,1.8V
C11	T22	IO_L3N_T0L_N5_AD15N_73	Bank73	1.2V,1.35V,1.5V,1.8V
C10	U22	IO_L3P_T0L_N4_AD15P_73	Bank73	1.2V,1.35V,1.5V,1.8V
D2	V25	IO_L4N_T0U_N7_DBC_AD7N_73	Bank73	1.2V,1.35V,1.5V,1.8V
D1	W25	IO_L4P_T0U_N6_DBC_AD7P_73	Bank73	1.2V,1.35V,1.5V,1.8V
D5	U23	IO_L5N_T0U_N9_AD14N_73	Bank73	1.2V,1.35V,1.5V,1.8V
D4	V23	IO_L5P_T0U_N8_AD14P_73	Bank73	1.2V,1.35V,1.5V,1.8V
D8	T26	IO_L6N_T0U_N11_AD6N_73	Bank73	1.2V,1.35V,1.5V,1.8V
D7	U26	IO_L6P_T0U_N10_AD6P_73	Bank73	1.2V,1.35V,1.5V,1.8V
E3	P25	IO_L7N_T1L_N1_QBC_AD13N_73	Bank73	1.2V,1.35V,1.5V,1.8V
E2	P26	IO_L7P_T1L_N0_QBC_AD13P_73	Bank73	1.2V,1.35V,1.5V,1.8V
E6	R24	IO_L8N_T1L_N3_AD5N_73	Bank73	1.2V,1.35V,1.5V,1.8V
E5	T24	IO_L8P_T1L_N2_AD5P_73	Bank73	1.2V,1.35V,1.5V,1.8V
E9	N21	IO_L9N_T1L_N5_AD12N_73	Bank73	1.2V,1.35V,1.5V,1.8V
E8	P21	IO_L9P_T1L_N4_AD12P_73	Bank73	1.2V,1.35V,1.5V,1.8V
F2	R25	IO_L10N_T1U_N7_QBC_AD4N_73	Bank73	1.2V,1.35V,1.5V,1.8V
F1	T25	IO_L10P_T1U_N6_QBC_AD4P_73	Bank73	1.2V,1.35V,1.5V,1.8V
F5	P22	IO_L11N_T1U_N9_GC_73	Bank73	1.2V,1.35V,1.5V,1.8V
F4	R22	IO_L11P_T1U_N8_GC_73	Bank73	1.2V,1.35V,1.5V,1.8V
F8	P23	IO_L12N_T1U_N11_GC_73	Bank73	1.2V,1.35V,1.5V,1.8V
F7	R23	IO_L12P_T1U_N10_GC_73	Bank73	1.2V,1.35V,1.5V,1.8V
G3	M23	IO_L13N_T2L_N1_GC_QBC_73	Bank73	1.2V,1.35V,1.5V,1.8V
G2	N23	IO_L13P_T2L_N0_GC_QBC_73	Bank73	1.2V,1.35V,1.5V,1.8V
G6	M24	IO_L14N_T2L_N3_GC_73	Bank73	1.2V,1.35V,1.5V,1.8V
G5	N24	IO_L14P_T2L_N2_GC_73	Bank73	1.2V,1.35V,1.5V,1.8V
G9	L24	IO_L15N_T2L_N5_AD11N_73	Bank73	1.2V,1.35V,1.5V,1.8V
G8	L25	IO_L15P_T2L_N4_AD11P_73	Bank73	1.2V,1.35V,1.5V,1.8V
G12	L21	IO_L16N_T2U_N7_QBC_AD3N_73	Bank73	1.2V,1.35V,1.5V,1.8V
G11	M21	IO_L16P_T2U_N6_QBC_AD3P_73	Bank73	1.2V,1.35V,1.5V,1.8V
H2	M26	IO_L17N_T2U_N9_AD10N_73	Bank73	1.2V,1.35V,1.5V,1.8V
H1	N26	IO_L17P_T2U_N8_AD10P_73	Bank73	1.2V,1.35V,1.5V,1.8V
H5	L22	IO_L18N_T2U_N11_AD2N_73	Bank73	1.2V,1.35V,1.5V,1.8V

J2 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
H4	M22	IO_L18P_T2U_N10_AD2P_73	Bank73	1.2V,1.35V,1.5V,1.8V
H8	H23	IO_L19N_T3L_N1_DBC_AD9N_73	Bank73	1.2V,1.35V,1.5V,1.8V
H7	H24	IO_L19P_T3L_N0_DBC_AD9P_73	Bank73	1.2V,1.35V,1.5V,1.8V
J3	J22	IO_L20N_T3L_N3_AD1N_73	Bank73	1.2V,1.35V,1.5V,1.8V
J2	K22	IO_L20P_T3L_N2_AD1P_73	Bank73	1.2V,1.35V,1.5V,1.8V
J6	H25	IO_L21N_T3L_N5_AD8N_73	Bank73	1.2V,1.35V,1.5V,1.8V
J5	J25	IO_L21P_T3L_N4_AD8P_73	Bank73	1.2V,1.35V,1.5V,1.8V
J9	J23	IO_L22N_T3U_N7_DBC_AD0N_73	Bank73	1.2V,1.35V,1.5V,1.8V
J8	K23	IO_L22P_T3U_N6_DBC_AD0P_73	Bank73	1.2V,1.35V,1.5V,1.8V
K2	H26	IO_L23N_T3U_N9_73	Bank73	1.2V,1.35V,1.5V,1.8V
K1	J26	IO_L23P_T3U_N8_73	Bank73	1.2V,1.35V,1.5V,1.8V
K5	K24	IO_L24N_T3U_N11_73	Bank73	1.2V,1.35V,1.5V,1.8V
K4	K25	IO_L24P_T3U_N10_73	Bank73	1.2V,1.35V,1.5V,1.8V
C15	D25	IO_L1N_T0L_N1_DBC_74	Bank74	1.2V,1.35V,1.5V,1.8V
C14	D26	IO_L1P_T0L_N0_DBC_74	Bank74	1.2V,1.35V,1.5V,1.8V
C19	A25	IO_L2N_T0L_N3_74	Bank74	1.2V,1.35V,1.5V,1.8V
C18	A26	IO_L2P_T0L_N2_74	Bank74	1.2V,1.35V,1.5V,1.8V
C23	C24	IO_L3N_T0L_N5_AD15N_74	Bank74	1.2V,1.35V,1.5V,1.8V
C22	C25	IO_L3P_T0L_N4_AD15P_74	Bank74	1.2V,1.35V,1.5V,1.8V
D13	A24	IO_L4N_T0U_N7_DBC_AD7N_74	Bank74	1.2V,1.35V,1.5V,1.8V
D12	B24	IO_L4P_T0U_N6_DBC_AD7P_74	Bank74	1.2V,1.35V,1.5V,1.8V
D17	C23	IO_L5N_T0U_N9_AD14N_74	Bank74	1.2V,1.35V,1.5V,1.8V
D16	D23	IO_L5P_T0U_N8_AD14P_74	Bank74	1.2V,1.35V,1.5V,1.8V
D20	B26	IO_L6N_T0U_N11_AD6N_74	Bank74	1.2V,1.35V,1.5V,1.8V
D19	C26	IO_L6P_T0U_N10_AD6P_74	Bank74	1.2V,1.35V,1.5V,1.8V
E12	A17	IO_L7N_T1L_N1_QBC_AD13N_74	Bank74	1.2V,1.35V,1.5V,1.8V
E11	B17	IO_L7P_T1L_N0_QBC_AD13P_74	Bank74	1.2V,1.35V,1.5V,1.8V
E15	A19	IO_L8N_T1L_N3_AD5N_74	Bank74	1.2V,1.35V,1.5V,1.8V
E14	B19	IO_L8P_T1L_N2_AD5P_74	Bank74	1.2V,1.35V,1.5V,1.8V
E18	B18	IO_L9N_T1L_N5_AD12N_74	Bank74	1.2V,1.35V,1.5V,1.8V
E17	C18	IO_L9P_T1L_N4_AD12P_74	Bank74	1.2V,1.35V,1.5V,1.8V
F11	A21	IO_L10N_T1U_N7_QBC_AD4N_74	Bank74	1.2V,1.35V,1.5V,1.8V
F10	A22	IO_L10P_T1U_N6_QBC_AD4P_74	Bank74	1.2V,1.35V,1.5V,1.8V
F14	C19	IO_L11N_T1U_N9_GC_74	Bank74	1.2V,1.35V,1.5V,1.8V
F13	C20	IO_L11P_T1U_N8_GC_74	Bank74	1.2V,1.35V,1.5V,1.8V
F17	B21	IO_L12N_T1U_N11_GC_74	Bank74	1.2V,1.35V,1.5V,1.8V
F16	B22	IO_L12P_T1U_N10_GC_74	Bank74	1.2V,1.35V,1.5V,1.8V
G15	D20	IO_L13N_T2L_N1_GC_QBC_74	Bank74	1.2V,1.35V,1.5V,1.8V
G14	E20	IO_L13P_T2L_N0_GC_QBC_74	Bank74	1.2V,1.35V,1.5V,1.8V
G18	C21	IO_L14N_T2L_N3_GC_74	Bank74	1.2V,1.35V,1.5V,1.8V
G17	D21	IO_L14P_T2L_N2_GC_74	Bank74	1.2V,1.35V,1.5V,1.8V
G21	E17	IO_L15N_T2L_N5_AD11N_74	Bank74	1.2V,1.35V,1.5V,1.8V
G20	F17	IO_L15P_T2L_N4_AD11P_74	Bank74	1.2V,1.35V,1.5V,1.8V
H11	D17	IO_L16N_T2U_N7_QBC_AD3N_74	Bank74	1.2V,1.35V,1.5V,1.8V

J2 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
H10	D18	IO_L16P_T2U_N6_QBC_AD3P_74	Bank74	1.2V,1.35V,1.5V,1.8V
H14	F19	IO_L17N_T2U_N9_AD10N_74	Bank74	1.2V,1.35V,1.5V,1.8V
H13	F20	IO_L17P_T2U_N8_AD10P_74	Bank74	1.2V,1.35V,1.5V,1.8V
H17	E18	IO_L18N_T2U_N11_AD2N_74	Bank74	1.2V,1.35V,1.5V,1.8V
H16	E19	IO_L18P_T2U_N10_AD2P_74	Bank74	1.2V,1.35V,1.5V,1.8V
H20	E23	IO_L19N_T3L_N1_DBC_AD9N_74	Bank74	1.2V,1.35V,1.5V,1.8V
H19	F24	IO_L19P_T3L_N0_DBC_AD9P_74	Bank74	1.2V,1.35V,1.5V,1.8V
J12	F22	IO_L20N_T3L_N3_AD1N_74	Bank74	1.2V,1.35V,1.5V,1.8V
J11	G22	IO_L20P_T3L_N2_AD1P_74	Bank74	1.2V,1.35V,1.5V,1.8V
J15	F25	IO_L21N_T3L_N5_AD8N_74	Bank74	1.2V,1.35V,1.5V,1.8V
J14	F26	IO_L21P_T3L_N4_AD8P_74	Bank74	1.2V,1.35V,1.5V,1.8V
J18	D22	IO_L22N_T3U_N7_DBC_AD0N_74	Bank74	1.2V,1.35V,1.5V,1.8V
J17	E22	IO_L22P_T3U_N6_DBC_AD0P_74	Bank74	1.2V,1.35V,1.5V,1.8V
K11	G23	IO_L23N_T3U_N9_74	Bank74	1.2V,1.35V,1.5V,1.8V
K10	G24	IO_L23P_T3U_N8_74	Bank74	1.2V,1.35V,1.5V,1.8V
K14	E24	IO_L24N_T3U_N11_74	Bank74	1.2V,1.35V,1.5V,1.8V
K13	E25	IO_L24P_T3U_N10_74	Bank74	1.2V,1.35V,1.5V,1.8V
C27	W20	IO_L1N_T0L_N1_DBC_75	Bank75	1.2V,1.35V,1.5V,1.8V
C26	W21	IO_L1P_T0L_N0_DBC_75	Bank75	1.2V,1.35V,1.5V,1.8V
C30	U18	IO_L2N_T0L_N3_75	Bank75	1.2V,1.35V,1.5V,1.8V
C29	U19	IO_L2P_T0L_N2_75	Bank75	1.2V,1.35V,1.5V,1.8V
D25	V19	IO_L3N_T0L_N5_AD15N_75	Bank75	1.2V,1.35V,1.5V,1.8V
D24	V20	IO_L3P_T0L_N4_AD15P_75	Bank75	1.2V,1.35V,1.5V,1.8V
D28	U16	IO_L4N_T0U_N7_DBC_AD7N_75	Bank75	1.2V,1.35V,1.5V,1.8V
D27	U17	IO_L4P_T0U_N6_DBC_AD7P_75	Bank75	1.2V,1.35V,1.5V,1.8V
E21	V18	IO_L5N_T0U_N9_AD14N_75	Bank75	1.2V,1.35V,1.5V,1.8V
E20	W18	IO_L5P_T0U_N8_AD14P_75	Bank75	1.2V,1.35V,1.5V,1.8V
E24	T16	IO_L6N_T0U_N11_AD6N_75	Bank75	1.2V,1.35V,1.5V,1.8V
E23	T17	IO_L6P_T0U_N10_AD6P_75	Bank75	1.2V,1.35V,1.5V,1.8V
E27	R20	IO_L7N_T1L_N1_QBC_AD13N_75	Bank75	1.2V,1.35V,1.5V,1.8V
E26	T20	IO_L7P_T1L_N0_QBC_AD13P_75	Bank75	1.2V,1.35V,1.5V,1.8V
E30	R17	IO_L8N_T1L_N3_AD5N_75	Bank75	1.2V,1.35V,1.5V,1.8V
E29	R18	IO_L8P_T1L_N2_AD5P_75	Bank75	1.2V,1.35V,1.5V,1.8V
F20	R19	IO_L9N_T1L_N5_AD12N_75	Bank75	1.2V,1.35V,1.5V,1.8V
F19	T19	IO_L9P_T1L_N4_AD12P_75	Bank75	1.2V,1.35V,1.5V,1.8V
F23	N16	IO_L10N_T1U_N7_QBC_AD4N_75	Bank75	1.2V,1.35V,1.5V,1.8V
F22	P16	IO_L10P_T1U_N6_QBC_AD4P_75	Bank75	1.2V,1.35V,1.5V,1.8V
F26	N18	IO_L11N_T1U_N9_GC_75	Bank75	1.2V,1.35V,1.5V,1.8V
F25	N19	IO_L11P_T1U_N8_GC_75	Bank75	1.2V,1.35V,1.5V,1.8V
F29	P17	IO_L12N_T1U_N11_GC_75	Bank75	1.2V,1.35V,1.5V,1.8V
F28	P18	IO_L12P_T1U_N10_GC_75	Bank75	1.2V,1.35V,1.5V,1.8V
G24	M18	IO_L13N_T2L_N1_GC_QBC_75	Bank75	1.2V,1.35V,1.5V,1.8V
G23	M19	IO_L13P_T2L_N0_GC_QBC_75	Bank75	1.2V,1.35V,1.5V,1.8V
G27	K19	IO_L14N_T2L_N3_GC_75	Bank75	1.2V,1.35V,1.5V,1.8V

J2 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
G26	L19	IO_L14P_T2L_N2_GC_75	Bank75	1.2V,1.35V,1.5V,1.8V
G30	M16	IO_L15N_T2L_N5_AD11N_75	Bank75	1.2V,1.35V,1.5V,1.8V
G29	M17	IO_L15P_T2L_N4_AD11P_75	Bank75	1.2V,1.35V,1.5V,1.8V
H23	L16	IO_L16N_T2U_N7_QBC_AD3N_75	Bank75	1.2V,1.35V,1.5V,1.8V
H22	L17	IO_L16P_T2U_N6_QBC_AD3P_75	Bank75	1.2V,1.35V,1.5V,1.8V
H26	K20	IO_L17N_T2U_N9_AD10N_75	Bank75	1.2V,1.35V,1.5V,1.8V
H25	L20	IO_L17P_T2U_N8_AD10P_75	Bank75	1.2V,1.35V,1.5V,1.8V
H29	K17	IO_L18N_T2U_N11_AD2N_75	Bank75	1.2V,1.35V,1.5V,1.8V
H28	K18	IO_L18P_T2U_N10_AD2P_75	Bank75	1.2V,1.35V,1.5V,1.8V
J21	G19	IO_L19N_T3L_N1_DBC_AD9N_75	Bank75	1.2V,1.35V,1.5V,1.8V
J20	H19	IO_L19P_T3L_N0_DBC_AD9P_75	Bank75	1.2V,1.35V,1.5V,1.8V
J24	J17	IO_L20N_T3L_N3_AD1N_75	Bank75	1.2V,1.35V,1.5V,1.8V
J23	J18	IO_L20P_T3L_N2_AD1P_75	Bank75	1.2V,1.35V,1.5V,1.8V
J27	H20	IO_L21N_T3L_N5_AD8N_75	Bank75	1.2V,1.35V,1.5V,1.8V
J26	J20	IO_L21P_T3L_N4_AD8P_75	Bank75	1.2V,1.35V,1.5V,1.8V
J30	G17	IO_L22N_T3U_N7_DBC_AD0N_75	Bank75	1.2V,1.35V,1.5V,1.8V
J29	G18	IO_L22P_T3U_N6_DBC_AD0P_75	Bank75	1.2V,1.35V,1.5V,1.8V
K20	H21	IO_L23N_T3U_N9_75	Bank75	1.2V,1.35V,1.5V,1.8V
K19	J21	IO_L23P_T3U_N8_75	Bank75	1.2V,1.35V,1.5V,1.8V
K23	H16	IO_L24N_T3U_N11_75	Bank75	1.2V,1.35V,1.5V,1.8V
K22	J16	IO_L24P_T3U_N10_75	Bank75	1.2V,1.35V,1.5V,1.8V

Table 5-6 Prodigy Connector – J3

J3 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	Y3	MGTYRXN0_236	Bank236	
A14	Y4	MGTYRXP0_236	Bank236	
A11	W1	MGTYRXN1_236	Bank236	
A10	W2	MGTYRXP1_236	Bank236	
A7	V3	MGTYRXN2_236	Bank236	
A6	V4	MGTYRXP2_236	Bank236	
A3	U1	MGTYRXN3_236	Bank236	
A2	U2	MGTYRXP3_236	Bank236	
B17	AB8	MGTYTXN0_236	Bank236	
B16	AB9	MGTYTXP0_236	Bank236	
B13	AA6	MGTYTXN1_236	Bank236	
B12	AA7	MGTYTXP1_236	Bank236	
B9	Y8	MGTYTXN2_236	Bank236	
B8	Y9	MGTYTXP2_236	Bank236	
B5	W6	MGTYTXN3_236	Bank236	
B4	W7	MGTYTXP3_236	Bank236	

J3 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A19	AE10	MGTREFCLK0N_236	Bank236	
A18	AE11	MGTREFCLK0P_236	Bank236	
B21	AC10	MGTREFCLK1N_236	Bank236	
B20	AC11	MGTREFCLK1P_236	Bank236	
C3	R40	IO_L1N_T0L_N1_DBC_70	Bank70	1.2V,1.35V,1.5V,1.8V
C2	R39	IO_L1P_T0L_N0_DBC_70	Bank70	1.2V,1.35V,1.5V,1.8V
C7	V40	IO_L2N_T0L_N3_70	Bank70	1.2V,1.35V,1.5V,1.8V
C6	W40	IO_L2P_T0L_N2_70	Bank70	1.2V,1.35V,1.5V,1.8V
C11	U38	IO_L3N_T0L_N5_AD15N_70	Bank70	1.2V,1.35V,1.5V,1.8V
C10	U37	IO_L3P_T0L_N4_AD15P_70	Bank70	1.2V,1.35V,1.5V,1.8V
D2	U39	IO_L4N_T0U_N7_DBC_AD7N_70	Bank70	1.2V,1.35V,1.5V,1.8V
D1	V39	IO_L4P_T0U_N6_DBC_AD7P_70	Bank70	1.2V,1.35V,1.5V,1.8V
D5	V38	IO_L5N_T0U_N9_AD14N_70	Bank70	1.2V,1.35V,1.5V,1.8V
D4	W38	IO_L5P_T0U_N8_AD14P_70	Bank70	1.2V,1.35V,1.5V,1.8V
D8	T40	IO_L6N_T0U_N11_AD6N_70	Bank70	1.2V,1.35V,1.5V,1.8V
D7	T39	IO_L6P_T0U_N10_AD6P_70	Bank70	1.2V,1.35V,1.5V,1.8V
E3	M39	IO_L7N_T1L_N1_QBC_AD13N_70	Bank70	1.2V,1.35V,1.5V,1.8V
E2	N39	IO_L7P_T1L_N0_QBC_AD13P_70	Bank70	1.2V,1.35V,1.5V,1.8V
E6	N40	IO_L8N_T1L_N3_AD5N_70	Bank70	1.2V,1.35V,1.5V,1.8V
E5	P40	IO_L8P_T1L_N2_AD5P_70	Bank70	1.2V,1.35V,1.5V,1.8V
E9	L37	IO_L9N_T1L_N5_AD12N_70	Bank70	1.2V,1.35V,1.5V,1.8V
E8	M37	IO_L9P_T1L_N4_AD12P_70	Bank70	1.2V,1.35V,1.5V,1.8V
F2	L40	IO_L10N_T1U_N7_QBC_AD4N_70	Bank70	1.2V,1.35V,1.5V,1.8V
F1	L39	IO_L10P_T1U_N6_QBC_AD4P_70	Bank70	1.2V,1.35V,1.5V,1.8V
F5	P37	IO_L11N_T1U_N9_GC_70	Bank70	1.2V,1.35V,1.5V,1.8V
F4	R37	IO_L11P_T1U_N8_GC_70	Bank70	1.2V,1.35V,1.5V,1.8V
F8	N38	IO_L12N_T1U_N11_GC_70	Bank70	1.2V,1.35V,1.5V,1.8V
F7	P38	IO_L12P_T1U_N10_GC_70	Bank70	1.2V,1.35V,1.5V,1.8V
G3	P36	IO_L13N_T2L_N1_GC_QBC_70	Bank70	1.2V,1.35V,1.5V,1.8V
G2	P35	IO_L13P_T2L_N0_GC_QBC_70	Bank70	1.2V,1.35V,1.5V,1.8V
G6	N36	IO_L14N_T2L_N3_GC_70	Bank70	1.2V,1.35V,1.5V,1.8V
G5	N35	IO_L14P_T2L_N2_GC_70	Bank70	1.2V,1.35V,1.5V,1.8V
G9	L36	IO_L15N_T2L_N5_AD11N_70	Bank70	1.2V,1.35V,1.5V,1.8V
G8	M36	IO_L15P_T2L_N4_AD11P_70	Bank70	1.2V,1.35V,1.5V,1.8V
G12	K35	IO_L16N_T2U_N7_QBC_AD3N_70	Bank70	1.2V,1.35V,1.5V,1.8V
G11	K34	IO_L16P_T2U_N6_QBC_AD3P_70	Bank70	1.2V,1.35V,1.5V,1.8V
H2	M34	IO_L17N_T2U_N9_AD10N_70	Bank70	1.2V,1.35V,1.5V,1.8V
H1	N34	IO_L17P_T2U_N8_AD10P_70	Bank70	1.2V,1.35V,1.5V,1.8V
H5	L35	IO_L18N_T2U_N11_AD2N_70	Bank70	1.2V,1.35V,1.5V,1.8V
H4	L34	IO_L18P_T2U_N10_AD2P_70	Bank70	1.2V,1.35V,1.5V,1.8V
H8	U34	IO_L19N_T3L_N1_DBC_AD9N_70	Bank70	1.2V,1.35V,1.5V,1.8V
H7	V34	IO_L19P_T3L_N0_DBC_AD9P_70	Bank70	1.2V,1.35V,1.5V,1.8V

J3 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
J3	R35	IO_L20N_T3L_N3_AD1N_70	Bank70	1.2V,1.35V,1.5V,1.8V
J2	R34	IO_L20P_T3L_N2_AD1P_70	Bank70	1.2V,1.35V,1.5V,1.8V
J6	W37	IO_L21N_T3L_N5_AD8N_70	Bank70	1.2V,1.35V,1.5V,1.8V
J5	W36	IO_L21P_T3L_N4_AD8P_70	Bank70	1.2V,1.35V,1.5V,1.8V
J9	T35	IO_L22N_T3U_N7_DBC_AD0N_70	Bank70	1.2V,1.35V,1.5V,1.8V
J8	T34	IO_L22P_T3U_N6_DBC_AD0P_70	Bank70	1.2V,1.35V,1.5V,1.8V
K2	V36	IO_L23N_T3U_N9_70	Bank70	1.2V,1.35V,1.5V,1.8V
K1	V35	IO_L23P_T3U_N8_70	Bank70	1.2V,1.35V,1.5V,1.8V
K5	T36	IO_L24N_T3U_N11_70	Bank70	1.2V,1.35V,1.5V,1.8V
K4	U36	IO_L24P_T3U_N10_70	Bank70	1.2V,1.35V,1.5V,1.8V
C15	D27	IO_L1N_T0L_N1_DBC_71	Bank71	1.2V,1.35V,1.5V,1.8V
C14	D28	IO_L1P_T0L_N0_DBC_71	Bank71	1.2V,1.35V,1.5V,1.8V
C19	A27	IO_L2N_T0L_N3_71	Bank71	1.2V,1.35V,1.5V,1.8V
C18	B27	IO_L2P_T0L_N2_71	Bank71	1.2V,1.35V,1.5V,1.8V
C23	C29	IO_L3N_T0L_N5_AD15N_71	Bank71	1.2V,1.35V,1.5V,1.8V
C22	C30	IO_L3P_T0L_N4_AD15P_71	Bank71	1.2V,1.35V,1.5V,1.8V
D13	A29	IO_L4N_T0U_N7_DBC_AD7N_71	Bank71	1.2V,1.35V,1.5V,1.8V
D12	A30	IO_L4P_T0U_N6_DBC_AD7P_71	Bank71	1.2V,1.35V,1.5V,1.8V
D17	D30	IO_L5N_T0U_N9_AD14N_71	Bank71	1.2V,1.35V,1.5V,1.8V
D16	E30	IO_L5P_T0U_N8_AD14P_71	Bank71	1.2V,1.35V,1.5V,1.8V
D20	B28	IO_L6N_T0U_N11_AD6N_71	Bank71	1.2V,1.35V,1.5V,1.8V
D19	B29	IO_L6P_T0U_N10_AD6P_71	Bank71	1.2V,1.35V,1.5V,1.8V
E12	A31	IO_L7N_T1L_N1_QBC_AD13N_71	Bank71	1.2V,1.35V,1.5V,1.8V
E11	A32	IO_L7P_T1L_N0_QBC_AD13P_71	Bank71	1.2V,1.35V,1.5V,1.8V
E15	C33	IO_L8N_T1L_N3_AD5N_71	Bank71	1.2V,1.35V,1.5V,1.8V
E14	D33	IO_L8P_T1L_N2_AD5P_71	Bank71	1.2V,1.35V,1.5V,1.8V
E18	B31	IO_L9N_T1L_N5_AD12N_71	Bank71	1.2V,1.35V,1.5V,1.8V
E17	C31	IO_L9P_T1L_N4_AD12P_71	Bank71	1.2V,1.35V,1.5V,1.8V
F11	B32	IO_L10N_T1U_N7_QBC_AD4N_71	Bank71	1.2V,1.35V,1.5V,1.8V
F10	B33	IO_L10P_T1U_N6_QBC_AD4P_71	Bank71	1.2V,1.35V,1.5V,1.8V
F14	D31	IO_L11N_T1U_N9_GC_71	Bank71	1.2V,1.35V,1.5V,1.8V
F13	D32	IO_L11P_T1U_N8_GC_71	Bank71	1.2V,1.35V,1.5V,1.8V
F17	E32	IO_L12N_T1U_N11_GC_71	Bank71	1.2V,1.35V,1.5V,1.8V
F16	F32	IO_L12P_T1U_N10_GC_71	Bank71	1.2V,1.35V,1.5V,1.8V
G15	G31	IO_L13N_T2L_N1_GC_QBC_71	Bank71	1.2V,1.35V,1.5V,1.8V
G14	G32	IO_L13P_T2L_N0_GC_QBC_71	Bank71	1.2V,1.35V,1.5V,1.8V
G18	F30	IO_L14N_T2L_N3_GC_71	Bank71	1.2V,1.35V,1.5V,1.8V
G17	F31	IO_L14P_T2L_N2_GC_71	Bank71	1.2V,1.35V,1.5V,1.8V
G21	H31	IO_L15N_T2L_N5_AD11N_71	Bank71	1.2V,1.35V,1.5V,1.8V
G20	J31	IO_L15P_T2L_N4_AD11P_71	Bank71	1.2V,1.35V,1.5V,1.8V
H11	H30	IO_L16N_T2U_N7_QBC_AD3N_71	Bank71	1.2V,1.35V,1.5V,1.8V
H10	J30	IO_L16P_T2U_N6_QBC_AD3P_71	Bank71	1.2V,1.35V,1.5V,1.8V
H14	J32	IO_L17N_T2U_N9_AD10N_71	Bank71	1.2V,1.35V,1.5V,1.8V

J3 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
H13	J33	IO_L17P_T2U_N8_AD10P_71	Bank71	1.2V,1.35V,1.5V,1.8V
H17	G33	IO_L18N_T2U_N11_AD2N_71	Bank71	1.2V,1.35V,1.5V,1.8V
H16	H33	IO_L18P_T2U_N10_AD2P_71	Bank71	1.2V,1.35V,1.5V,1.8V
H20	G28	IO_L19N_T3L_N1_DBC_AD9N_71	Bank71	1.2V,1.35V,1.5V,1.8V
H19	G29	IO_L19P_T3L_N0_DBC_AD9P_71	Bank71	1.2V,1.35V,1.5V,1.8V
J12	F27	IO_L20N_T3L_N3_AD1N_71	Bank71	1.2V,1.35V,1.5V,1.8V
J11	G27	IO_L20P_T3L_N2_AD1P_71	Bank71	1.2V,1.35V,1.5V,1.8V
J15	H28	IO_L21N_T3L_N5_AD8N_71	Bank71	1.2V,1.35V,1.5V,1.8V
J14	H29	IO_L21P_T3L_N4_AD8P_71	Bank71	1.2V,1.35V,1.5V,1.8V
J18	E29	IO_L22N_T3U_N7_DBC_AD0N_71	Bank71	1.2V,1.35V,1.5V,1.8V
J17	F29	IO_L22P_T3U_N6_DBC_AD0P_71	Bank71	1.2V,1.35V,1.5V,1.8V
K11	J27	IO_L23N_T3U_N9_71	Bank71	1.2V,1.35V,1.5V,1.8V
K10	J28	IO_L23P_T3U_N8_71	Bank71	1.2V,1.35V,1.5V,1.8V
K14	E27	IO_L24N_T3U_N11_71	Bank71	1.2V,1.35V,1.5V,1.8V
K13	E28	IO_L24P_T3U_N10_71	Bank71	1.2V,1.35V,1.5V,1.8V
C27	P32	IO_L1N_T0L_N1_DBC_72	Bank72	1.2V,1.35V,1.5V,1.8V
C26	P33	IO_L1P_T0L_N0_DBC_72	Bank72	1.2V,1.35V,1.5V,1.8V
C30	K32	IO_L2N_T0L_N3_72	Bank72	1.2V,1.35V,1.5V,1.8V
C29	K33	IO_L2P_T0L_N2_72	Bank72	1.2V,1.35V,1.5V,1.8V
D25	N31	IO_L3N_T0L_N5_AD15N_72	Bank72	1.2V,1.35V,1.5V,1.8V
D24	P31	IO_L3P_T0L_N4_AD15P_72	Bank72	1.2V,1.35V,1.5V,1.8V
D28	L31	IO_L4N_T0U_N7_DBC_AD7N_72	Bank72	1.2V,1.35V,1.5V,1.8V
D27	L32	IO_L4P_T0U_N6_DBC_AD7P_72	Bank72	1.2V,1.35V,1.5V,1.8V
E21	M33	IO_L5N_T0U_N9_AD14N_72	Bank72	1.2V,1.35V,1.5V,1.8V
E20	N33	IO_L5P_T0U_N8_AD14P_72	Bank72	1.2V,1.35V,1.5V,1.8V
E24	M31	IO_L6N_T0U_N11_AD6N_72	Bank72	1.2V,1.35V,1.5V,1.8V
E23	M32	IO_L6P_T0U_N10_AD6P_72	Bank72	1.2V,1.35V,1.5V,1.8V
E27	W32	IO_L7N_T1L_N1_QBC_AD13N_72	Bank72	1.2V,1.35V,1.5V,1.8V
E26	W33	IO_L7P_T1L_N0_QBC_AD13P_72	Bank72	1.2V,1.35V,1.5V,1.8V
E30	U33	IO_L8N_T1L_N3_AD5N_72	Bank72	1.2V,1.35V,1.5V,1.8V
E29	V33	IO_L8P_T1L_N2_AD5P_72	Bank72	1.2V,1.35V,1.5V,1.8V
F20	W30	IO_L9N_T1L_N5_AD12N_72	Bank72	1.2V,1.35V,1.5V,1.8V
F19	W31	IO_L9P_T1L_N4_AD12P_72	Bank72	1.2V,1.35V,1.5V,1.8V
F23	R32	IO_L10N_T1U_N7_QBC_AD4N_72	Bank72	1.2V,1.35V,1.5V,1.8V
F22	R33	IO_L10P_T1U_N6_QBC_AD4P_72	Bank72	1.2V,1.35V,1.5V,1.8V
F26	U31	IO_L11N_T1U_N9_GC_72	Bank72	1.2V,1.35V,1.5V,1.8V
F25	U32	IO_L11P_T1U_N8_GC_72	Bank72	1.2V,1.35V,1.5V,1.8V
F29	T31	IO_L12N_T1U_N11_GC_72	Bank72	1.2V,1.35V,1.5V,1.8V
F28	T32	IO_L12P_T1U_N10_GC_72	Bank72	1.2V,1.35V,1.5V,1.8V
G24	T29	IO_L13N_T2L_N1_GC_QBC_72	Bank72	1.2V,1.35V,1.5V,1.8V
G23	T30	IO_L13P_T2L_N0_GC_QBC_72	Bank72	1.2V,1.35V,1.5V,1.8V
G27	R29	IO_L14N_T2L_N3_GC_72	Bank72	1.2V,1.35V,1.5V,1.8V
G26	R30	IO_L14P_T2L_N2_GC_72	Bank72	1.2V,1.35V,1.5V,1.8V

J3 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
G30	V28	IO_L15N_T2L_N5_AD11N_72	Bank72	1.2V,1.35V,1.5V,1.8V
G29	W28	IO_L15P_T2L_N4_AD11P_72	Bank72	1.2V,1.35V,1.5V,1.8V
H23	U28	IO_L16N_T2U_N7_QBC_AD3N_72	Bank72	1.2V,1.35V,1.5V,1.8V
H22	U29	IO_L16P_T2U_N6_QBC_AD3P_72	Bank72	1.2V,1.35V,1.5V,1.8V
H26	V29	IO_L17N_T2U_N9_AD10N_72	Bank72	1.2V,1.35V,1.5V,1.8V
H25	V30	IO_L17P_T2U_N8_AD10P_72	Bank72	1.2V,1.35V,1.5V,1.8V
H29	T27	IO_L18N_T2U_N11_AD2N_72	Bank72	1.2V,1.35V,1.5V,1.8V
H28	U27	IO_L18P_T2U_N10_AD2P_72	Bank72	1.2V,1.35V,1.5V,1.8V
J21	L29	IO_L19N_T3L_N1_DBC_AD9N_72	Bank72	1.2V,1.35V,1.5V,1.8V
J20	L30	IO_L19P_T3L_N0_DBC_AD9P_72	Bank72	1.2V,1.35V,1.5V,1.8V
J24	P27	IO_L20N_T3L_N3_AD1N_72	Bank72	1.2V,1.35V,1.5V,1.8V
J23	P28	IO_L20P_T3L_N2_AD1P_72	Bank72	1.2V,1.35V,1.5V,1.8V
J27	L27	IO_L21N_T3L_N5_AD8N_72	Bank72	1.2V,1.35V,1.5V,1.8V
J26	M27	IO_L21P_T3L_N4_AD8P_72	Bank72	1.2V,1.35V,1.5V,1.8V
J30	N28	IO_L22N_T3U_N7_DBC_AD0N_72	Bank72	1.2V,1.35V,1.5V,1.8V
J29	N29	IO_L22P_T3U_N6_DBC_AD0P_72	Bank72	1.2V,1.35V,1.5V,1.8V
K20	N30	IO_L23N_T3U_N9_72	Bank72	1.2V,1.35V,1.5V,1.8V
K19	P30	IO_L23P_T3U_N8_72	Bank72	1.2V,1.35V,1.5V,1.8V
K23	M28	IO_L24N_T3U_N11_72	Bank72	1.2V,1.35V,1.5V,1.8V
K22	M29	IO_L24P_T3U_N10_72	Bank72	1.2V,1.35V,1.5V,1.8V

Table 5-7 Prodigy Connector – J4

J4 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	T3	MGTYRXN0_237	Bank237	
A14	T4	MGTYRXP0_237	Bank237	
A11	R1	MGTYRXN1_237	Bank237	
A10	R2	MGTYRXP1_237	Bank237	
A7	P3	MGTYRXN2_237	Bank237	
A6	P4	MGTYRXP2_237	Bank237	
A3	N1	MGTYRXN3_237	Bank237	
A2	N2	MGTYRXP3_237	Bank237	
B17	V8	MGTYTXN0_237	Bank237	
B16	V9	MGTYTXP0_237	Bank237	
B13	U6	MGTYTXN1_237	Bank237	
B12	U7	MGTYTXP1_237	Bank237	
B9	T8	MGTYTXN2_237	Bank237	
B8	T9	MGTYTXP2_237	Bank237	
B5	R6	MGTYTXN3_237	Bank237	
B4	R7	MGTYTXP3_237	Bank237	
A19	AA10	MGTREFCLK0N_237	Bank237	
A18	AA11	MGTREFCLK0P_237	Bank237	
B21	W10	MGTREFCLK1N_237	Bank237	

J4 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
B20	W11	MGTREFCLK1P_237	Bank237	
C3	R59	IO_L1N_T0L_N1_DBC_34	Bank34	1.2V,1.35V,1.5V,1.8V
C2	T59	IO_L1P_T0L_N0_DBC_34	Bank34	1.2V,1.35V,1.5V,1.8V
C7	T62	IO_L2N_T0L_N3_34	Bank34	1.2V,1.35V,1.5V,1.8V
C6	T61	IO_L2P_T0L_N2_34	Bank34	1.2V,1.35V,1.5V,1.8V
C11	R60	IO_L3N_T0L_N5_AD15N_34	Bank34	1.2V,1.35V,1.5V,1.8V
C10	T60	IO_L3P_T0L_N4_AD15P_34	Bank34	1.2V,1.35V,1.5V,1.8V
D2	R63	IO_L4N_T0U_N7_DBC_AD7N_34	Bank34	1.2V,1.35V,1.5V,1.8V
D1	R62	IO_L4P_T0U_N6_DBC_AD7P_34	Bank34	1.2V,1.35V,1.5V,1.8V
D5	P61	IO_L5N_T0U_N9_AD14N_34	Bank34	1.2V,1.35V,1.5V,1.8V
D4	P60	IO_L5P_T0U_N8_AD14P_34	Bank34	1.2V,1.35V,1.5V,1.8V
D8	N63	IO_L6N_T0U_N11_AD6N_34	Bank34	1.2V,1.35V,1.5V,1.8V
D7	P63	IO_L6P_T0U_N10_AD6P_34	Bank34	1.2V,1.35V,1.5V,1.8V
E3	M59	IO_L7N_T1L_N1_QBC_AD13N_34	Bank34	1.2V,1.35V,1.5V,1.8V
E2	N59	IO_L7P_T1L_N0_QBC_AD13P_34	Bank34	1.2V,1.35V,1.5V,1.8V
E6	M63	IO_L8N_T1L_N3_AD5N_34	Bank34	1.2V,1.35V,1.5V,1.8V
E5	M62	IO_L8P_T1L_N2_AD5P_34	Bank34	1.2V,1.35V,1.5V,1.8V
E9	N61	IO_L9N_T1L_N5_AD12N_34	Bank34	1.2V,1.35V,1.5V,1.8V
E8	N60	IO_L9P_T1L_N4_AD12P_34	Bank34	1.2V,1.35V,1.5V,1.8V
F2	L62	IO_L10N_T1U_N7_QBC_AD4N_34	Bank34	1.2V,1.35V,1.5V,1.8V
F1	L61	IO_L10P_T1U_N6_QBC_AD4P_34	Bank34	1.2V,1.35V,1.5V,1.8V
F5	L60	IO_L11N_T1U_N9_GC_34	Bank34	1.2V,1.35V,1.5V,1.8V
F4	L59	IO_L11P_T1U_N8_GC_34	Bank34	1.2V,1.35V,1.5V,1.8V
F8	K60	IO_L12N_T1U_N11_GC_34	Bank34	1.2V,1.35V,1.5V,1.8V
F7	K59	IO_L12P_T1U_N10_GC_34	Bank34	1.2V,1.35V,1.5V,1.8V
G3	J61	IO_L13N_T2L_N1_GC_QBC_34	Bank34	1.2V,1.35V,1.5V,1.8V
G2	J60	IO_L13P_T2L_N0_GC_QBC_34	Bank34	1.2V,1.35V,1.5V,1.8V
G6	H61	IO_L14N_T2L_N3_GC_34	Bank34	1.2V,1.35V,1.5V,1.8V
G5	H60	IO_L14P_T2L_N2_GC_34	Bank34	1.2V,1.35V,1.5V,1.8V
G9	K63	IO_L15N_T2L_N5_AD11N_34	Bank34	1.2V,1.35V,1.5V,1.8V
G8	K62	IO_L15P_T2L_N4_AD11P_34	Bank34	1.2V,1.35V,1.5V,1.8V
G12	G63	IO_L16N_T2U_N7_QBC_AD3N_34	Bank34	1.2V,1.35V,1.5V,1.8V
G11	H63	IO_L16P_T2U_N6_QBC_AD3P_34	Bank34	1.2V,1.35V,1.5V,1.8V
H2	J63	IO_L17N_T2U_N9_AD10N_34	Bank34	1.2V,1.35V,1.5V,1.8V
H1	J62	IO_L17P_T2U_N8_AD10P_34	Bank34	1.2V,1.35V,1.5V,1.8V
H5	G62	IO_L18N_T2U_N11_AD2N_34	Bank34	1.2V,1.35V,1.5V,1.8V
H4	G61	IO_L18P_T2U_N10_AD2P_34	Bank34	1.2V,1.35V,1.5V,1.8V
H8	F59	IO_L19N_T3L_N1_DBC_AD9N_34	Bank34	1.2V,1.35V,1.5V,1.8V
H7	G59	IO_L19P_T3L_N0_DBC_AD9P_34	Bank34	1.2V,1.35V,1.5V,1.8V
J3	D62	IO_L20N_T3L_N3_AD1N_34	Bank34	1.2V,1.35V,1.5V,1.8V
J2	E62	IO_L20P_T3L_N2_AD1P_34	Bank34	1.2V,1.35V,1.5V,1.8V
J6	E60	IO_L21N_T3L_N5_AD8N_34	Bank34	1.2V,1.35V,1.5V,1.8V
J5	F60	IO_L21P_T3L_N4_AD8P_34	Bank34	1.2V,1.35V,1.5V,1.8V
J9	D61	IO_L22N_T3U_N7_DBC_AD0N_34	Bank34	1.2V,1.35V,1.5V,1.8V

J4 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
J8	D60	IO_L22P_T3U_N6_DBC_AD0P_34	Bank34	1.2V,1.35V,1.5V,1.8V
K2	F62	IO_L23N_T3U_N9_34	Bank34	1.2V,1.35V,1.5V,1.8V
K1	F61	IO_L23P_T3U_N8_34	Bank34	1.2V,1.35V,1.5V,1.8V
K5	C61	IO_L24N_T3U_N11_34	Bank34	1.2V,1.35V,1.5V,1.8V
K4	C60	IO_L24P_T3U_N10_34	Bank34	1.2V,1.35V,1.5V,1.8V
C15	C59	IO_L1N_T0L_N1_DBC_35	Bank35	1.2V,1.35V,1.5V,1.8V
C14	C58	IO_L1P_T0L_N0_DBC_35	Bank35	1.2V,1.35V,1.5V,1.8V
C19	D58	IO_L2N_T0L_N3_35	Bank35	1.2V,1.35V,1.5V,1.8V
C18	D57	IO_L2P_T0L_N2_35	Bank35	1.2V,1.35V,1.5V,1.8V
C23	A59	IO_L3N_T0L_N5_AD15N_35	Bank35	1.2V,1.35V,1.5V,1.8V
C22	B59	IO_L3P_T0L_N4_AD15P_35	Bank35	1.2V,1.35V,1.5V,1.8V
D13	A56	IO_L4N_T0U_N7_DBC_AD7N_35	Bank35	1.2V,1.35V,1.5V,1.8V
D12	B56	IO_L4P_T0U_N6_DBC_AD7P_35	Bank35	1.2V,1.35V,1.5V,1.8V
D17	B58	IO_L5N_T0U_N9_AD14N_35	Bank35	1.2V,1.35V,1.5V,1.8V
D16	B57	IO_L5P_T0U_N8_AD14P_35	Bank35	1.2V,1.35V,1.5V,1.8V
D20	C56	IO_L6N_T0U_N11_AD6N_35	Bank35	1.2V,1.35V,1.5V,1.8V
D19	D56	IO_L6P_T0U_N10_AD6P_35	Bank35	1.2V,1.35V,1.5V,1.8V
E12	J57	IO_L7N_T1L_N1_QBC_AD13N_35	Bank35	1.2V,1.35V,1.5V,1.8V
E11	J56	IO_L7P_T1L_N0_QBC_AD13P_35	Bank35	1.2V,1.35V,1.5V,1.8V
E15	H58	IO_L8N_T1L_N3_AD5N_35	Bank35	1.2V,1.35V,1.5V,1.8V
E14	J58	IO_L8P_T1L_N2_AD5P_35	Bank35	1.2V,1.35V,1.5V,1.8V
E18	G56	IO_L9N_T1L_N5_AD12N_35	Bank35	1.2V,1.35V,1.5V,1.8V
E17	H56	IO_L9P_T1L_N4_AD12P_35	Bank35	1.2V,1.35V,1.5V,1.8V
F11	G58	IO_L10N_T1U_N7_QBC_AD4N_35	Bank35	1.2V,1.35V,1.5V,1.8V
F10	G57	IO_L10P_T1U_N6_QBC_AD4P_35	Bank35	1.2V,1.35V,1.5V,1.8V
F14	E58	IO_L11N_T1U_N9_GC_35	Bank35	1.2V,1.35V,1.5V,1.8V
F13	E57	IO_L11P_T1U_N8_GC_35	Bank35	1.2V,1.35V,1.5V,1.8V
F17	F57	IO_L12N_T1U_N11_GC_35	Bank35	1.2V,1.35V,1.5V,1.8V
F16	F56	IO_L12P_T1U_N10_GC_35	Bank35	1.2V,1.35V,1.5V,1.8V
G15	E54	IO_L13N_T2L_N1_GC_QBC_35	Bank35	1.2V,1.35V,1.5V,1.8V
G14	F54	IO_L13P_T2L_N0_GC_QBC_35	Bank35	1.2V,1.35V,1.5V,1.8V
G18	E55	IO_L14N_T2L_N3_GC_35	Bank35	1.2V,1.35V,1.5V,1.8V
G17	F55	IO_L14P_T2L_N2_GC_35	Bank35	1.2V,1.35V,1.5V,1.8V
G21	G53	IO_L15N_T2L_N5_AD11N_35	Bank35	1.2V,1.35V,1.5V,1.8V
G20	H53	IO_L15P_T2L_N4_AD11P_35	Bank35	1.2V,1.35V,1.5V,1.8V
H11	H55	IO_L16N_T2U_N7_QBC_AD3N_35	Bank35	1.2V,1.35V,1.5V,1.8V
H10	J55	IO_L16P_T2U_N6_QBC_AD3P_35	Bank35	1.2V,1.35V,1.5V,1.8V
H14	F52	IO_L17N_T2U_N9_AD10N_35	Bank35	1.2V,1.35V,1.5V,1.8V
H13	G52	IO_L17P_T2U_N8_AD10P_35	Bank35	1.2V,1.35V,1.5V,1.8V
H17	G54	IO_L18N_T2U_N11_AD2N_35	Bank35	1.2V,1.35V,1.5V,1.8V
H16	H54	IO_L18P_T2U_N10_AD2P_35	Bank35	1.2V,1.35V,1.5V,1.8V
H20	D53	IO_L19N_T3L_N1_DBC_AD9N_35	Bank35	1.2V,1.35V,1.5V,1.8V
H19	D52	IO_L19P_T3L_N0_DBC_AD9P_35	Bank35	1.2V,1.35V,1.5V,1.8V
J12	B54	IO_L20N_T3L_N3_AD1N_35	Bank35	1.2V,1.35V,1.5V,1.8V

J4 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
J11	B53	IO_L20P_T3L_N2_AD1P_35	Bank35	1.2V,1.35V,1.5V,1.8V
J15	C54	IO_L21N_T3L_N5_AD8N_35	Bank35	1.2V,1.35V,1.5V,1.8V
J14	C53	IO_L21P_T3L_N4_AD8P_35	Bank35	1.2V,1.35V,1.5V,1.8V
J18	A55	IO_L22N_T3U_N7_DBC_AD0N_35	Bank35	1.2V,1.35V,1.5V,1.8V
J17	A54	IO_L22P_T3U_N6_DBC_AD0P_35	Bank35	1.2V,1.35V,1.5V,1.8V
K11	C55	IO_L23N_T3U_N9_35	Bank35	1.2V,1.35V,1.5V,1.8V
K10	D55	IO_L23P_T3U_N8_35	Bank35	1.2V,1.35V,1.5V,1.8V
K14	A52	IO_L24N_T3U_N11_35	Bank35	1.2V,1.35V,1.5V,1.8V
K13	B52	IO_L24P_T3U_N10_35	Bank35	1.2V,1.35V,1.5V,1.8V
C27	U49	IO_L1N_T0L_N1_DBC_36	Bank36	1.2V,1.35V,1.5V,1.8V
C26	V49	IO_L1P_T0L_N0_DBC_36	Bank36	1.2V,1.35V,1.5V,1.8V
C30	V50	IO_L2N_T0L_N3_36	Bank36	1.2V,1.35V,1.5V,1.8V
C29	W50	IO_L2P_T0L_N2_36	Bank36	1.2V,1.35V,1.5V,1.8V
D25	U48	IO_L3N_T0L_N5_AD15N_36	Bank36	1.2V,1.35V,1.5V,1.8V
D24	V48	IO_L3P_T0L_N4_AD15P_36	Bank36	1.2V,1.35V,1.5V,1.8V
D28	W48	IO_L4N_T0U_N7_DBC_AD7N_36	Bank36	1.2V,1.35V,1.5V,1.8V
D27	W47	IO_L4P_T0U_N6_DBC_AD7P_36	Bank36	1.2V,1.35V,1.5V,1.8V
E21	U46	IO_L5N_T0U_N9_AD14N_36	Bank36	1.2V,1.35V,1.5V,1.8V
E20	V46	IO_L5P_T0U_N8_AD14P_36	Bank36	1.2V,1.35V,1.5V,1.8V
E24	T47	IO_L6N_T0U_N11_AD6N_36	Bank36	1.2V,1.35V,1.5V,1.8V
E23	U47	IO_L6P_T0U_N10_AD6P_36	Bank36	1.2V,1.35V,1.5V,1.8V
E27	R48	IO_L7N_T1L_N1_QBC_AD13N_36	Bank36	1.2V,1.35V,1.5V,1.8V
E26	R47	IO_L7P_T1L_N0_QBC_AD13P_36	Bank36	1.2V,1.35V,1.5V,1.8V
E30	R50	IO_L8N_T1L_N3_AD5N_36	Bank36	1.2V,1.35V,1.5V,1.8V
E29	R49	IO_L8P_T1L_N2_AD5P_36	Bank36	1.2V,1.35V,1.5V,1.8V
F20	N46	IO_L9N_T1L_N5_AD12N_36	Bank36	1.2V,1.35V,1.5V,1.8V
F19	P46	IO_L9P_T1L_N4_AD12P_36	Bank36	1.2V,1.35V,1.5V,1.8V
F23	N50	IO_L10N_T1U_N7_QBC_AD4N_36	Bank36	1.2V,1.35V,1.5V,1.8V
F22	P50	IO_L10P_T1U_N6_QBC_AD4P_36	Bank36	1.2V,1.35V,1.5V,1.8V
F26	P48	IO_L11N_T1U_N9_GC_36	Bank36	1.2V,1.35V,1.5V,1.8V
F25	P47	IO_L11P_T1U_N8_GC_36	Bank36	1.2V,1.35V,1.5V,1.8V
F29	N49	IO_L12N_T1U_N11_GC_36	Bank36	1.2V,1.35V,1.5V,1.8V
F28	N48	IO_L12P_T1U_N10_GC_36	Bank36	1.2V,1.35V,1.5V,1.8V
G24	M49	IO_L13N_T2L_N1_GC_QBC_36	Bank36	1.2V,1.35V,1.5V,1.8V
G23	M48	IO_L13P_T2L_N0_GC_QBC_36	Bank36	1.2V,1.35V,1.5V,1.8V
G27	L50	IO_L14N_T2L_N3_GC_36	Bank36	1.2V,1.35V,1.5V,1.8V
G26	L49	IO_L14P_T2L_N2_GC_36	Bank36	1.2V,1.35V,1.5V,1.8V
G30	K50	IO_L15N_T2L_N5_AD11N_36	Bank36	1.2V,1.35V,1.5V,1.8V
G29	K49	IO_L15P_T2L_N4_AD11P_36	Bank36	1.2V,1.35V,1.5V,1.8V
H23	L47	IO_L16N_T2U_N7_QBC_AD3N_36	Bank36	1.2V,1.35V,1.5V,1.8V
H22	L46	IO_L16P_T2U_N6_QBC_AD3P_36	Bank36	1.2V,1.35V,1.5V,1.8V
H26	M47	IO_L17N_T2U_N9_AD10N_36	Bank36	1.2V,1.35V,1.5V,1.8V
H25	M46	IO_L17P_T2U_N8_AD10P_36	Bank36	1.2V,1.35V,1.5V,1.8V
H29	K48	IO_L18N_T2U_N11_AD2N_36	Bank36	1.2V,1.35V,1.5V,1.8V

J4 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
H28	K47	IO_L18P_T2U_N10_AD2P_36	Bank36	1.2V,1.35V,1.5V,1.8V
J21	H50	IO_L19N_T3L_N1_DBC_AD9N_36	Bank36	1.2V,1.35V,1.5V,1.8V
J20	J50	IO_L19P_T3L_N0_DBC_AD9P_36	Bank36	1.2V,1.35V,1.5V,1.8V
J24	G49	IO_L20N_T3L_N3_AD1N_36	Bank36	1.2V,1.35V,1.5V,1.8V
J23	H49	IO_L20P_T3L_N2_AD1P_36	Bank36	1.2V,1.35V,1.5V,1.8V
J27	G51	IO_L21N_T3L_N5_AD8N_36	Bank36	1.2V,1.35V,1.5V,1.8V
J26	H51	IO_L21P_T3L_N4_AD8P_36	Bank36	1.2V,1.35V,1.5V,1.8V
J30	G48	IO_L22N_T3U_N7_DBC_AD0N_36	Bank36	1.2V,1.35V,1.5V,1.8V
J29	H48	IO_L22P_T3U_N6_DBC_AD0P_36	Bank36	1.2V,1.35V,1.5V,1.8V
K20	J48	IO_L23N_T3U_N9_36	Bank36	1.2V,1.35V,1.5V,1.8V
K19	J47	IO_L23P_T3U_N8_36	Bank36	1.2V,1.35V,1.5V,1.8V
K23	G47	IO_L24N_T3U_N11_36	Bank36	1.2V,1.35V,1.5V,1.8V
K22	G46	IO_L24P_T3U_N10_36	Bank36	1.2V,1.35V,1.5V,1.8V

Table 5-8 Prodigy Connector – J5

J5 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	BY3	MGTYRXN0_220	Bank220	
A14	BY4	MGTYRXP0_220	Bank220	
A11	BW1	MGTYRXN1_220	Bank220	
A10	BW2	MGTYRXP1_220	Bank220	
A7	BV3	MGTYRXN2_220	Bank220	
A6	BV4	MGTYRXP2_220	Bank220	
A3	BU1	MGTYRXN3_220	Bank220	
A2	BU2	MGTYRXP3_220	Bank220	
B17	CC6	MGTYTXN0_220	Bank220	
B16	CC7	MGTYTXP0_220	Bank220	
B13	CB4	MGTYTXN1_220	Bank220	
B12	CB5	MGTYTXP1_220	Bank220	
B9	CA6	MGTYTXN2_220	Bank220	
B8	CA7	MGTYTXP2_220	Bank220	
B5	BW6	MGTYTXN3_220	Bank220	
B4	BW7	MGTYTXP3_220	Bank220	
A19	CB8	MGTREFCLK0N_220	Bank220	
A18	CB9	MGTREFCLK0P_220	Bank220	
B21	BY8	MGTREFCLK1N_220	Bank220	
B20	BY9	MGTREFCLK1P_220	Bank220	
C3	AV58	IO_L1N_T0L_N1_DBC_28	Bank28	1.2V,1.35V,1.5V,1.8V
C2	AU58	IO_L1P_T0L_N0_DBC_28	Bank28	1.2V,1.35V,1.5V,1.8V
C7	AT60	IO_L2N_T0L_N3_28	Bank28	1.2V,1.35V,1.5V,1.8V
C6	AR60	IO_L2P_T0L_N2_28	Bank28	1.2V,1.35V,1.5V,1.8V
C11	AU59	IO_L3N_T0L_N5_AD15N_28	Bank28	1.2V,1.35V,1.5V,1.8V
C10	AT59	IO_L3P_T0L_N4_AD15P_28	Bank28	1.2V,1.35V,1.5V,1.8V

J5 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D2	AV60	IO_L4N_T0U_N7_DBC_AD7N_28	Bank28	1.2V,1.35V,1.5V,1.8V
D1	AV59	IO_L4P_T0U_N6_DBC_AD7P_28	Bank28	1.2V,1.35V,1.5V,1.8V
D5	AR59	IO_L5N_T0U_N9_AD14N_28	Bank28	1.2V,1.35V,1.5V,1.8V
D4	AR58	IO_L5P_T0U_N8_AD14P_28	Bank28	1.2V,1.35V,1.5V,1.8V
D8	AU61	IO_L6N_T0U_N11_AD6N_28	Bank28	1.2V,1.35V,1.5V,1.8V
D7	AT61	IO_L6P_T0U_N10_AD6P_28	Bank28	1.2V,1.35V,1.5V,1.8V
E3	AP61	IO_L7N_T1L_N1_QBC_AD13N_28	Bank28	1.2V,1.35V,1.5V,1.8V
E2	AP60	IO_L7P_T1L_N0_QBC_AD13P_28	Bank28	1.2V,1.35V,1.5V,1.8V
E6	AT62	IO_L8N_T1L_N3_AD5N_28	Bank28	1.2V,1.35V,1.5V,1.8V
E5	AR62	IO_L8P_T1L_N2_AD5P_28	Bank28	1.2V,1.35V,1.5V,1.8V
E9	AR63	IO_L9N_T1L_N5_AD12N_28	Bank28	1.2V,1.35V,1.5V,1.8V
E8	AP62	IO_L9P_T1L_N4_AD12P_28	Bank28	1.2V,1.35V,1.5V,1.8V
F2	AP63	IO_L10N_T1U_N7_QBC_AD4N_28	Bank28	1.2V,1.35V,1.5V,1.8V
F1	AN63	IO_L10P_T1U_N6_QBC_AD4P_28	Bank28	1.2V,1.35V,1.5V,1.8V
F5	AN61	IO_L11N_T1U_N9_GC_28	Bank28	1.2V,1.35V,1.5V,1.8V
F4	AN60	IO_L11P_T1U_N8_GC_28	Bank28	1.2V,1.35V,1.5V,1.8V
F8	AM62	IO_L12N_T1U_N11_GC_28	Bank28	1.2V,1.35V,1.5V,1.8V
F7	AM61	IO_L12P_T1U_N10_GC_28	Bank28	1.2V,1.35V,1.5V,1.8V
G3	AL61	IO_L13N_T2L_N1_GC_QBC_28	Bank28	1.2V,1.35V,1.5V,1.8V
G2	AL60	IO_L13P_T2L_N0_GC_QBC_28	Bank28	1.2V,1.35V,1.5V,1.8V
G6	AL62	IO_L14N_T2L_N3_GC_28	Bank28	1.2V,1.35V,1.5V,1.8V
G5	AK62	IO_L14P_T2L_N2_GC_28	Bank28	1.2V,1.35V,1.5V,1.8V
G9	AJ63	IO_L15N_T2L_N5_AD11N_28	Bank28	1.2V,1.35V,1.5V,1.8V
G8	AH63	IO_L15P_T2L_N4_AD11P_28	Bank28	1.2V,1.35V,1.5V,1.8V
G12	AJ61	IO_L16N_T2U_N7_QBC_AD3N_28	Bank28	1.2V,1.35V,1.5V,1.8V
G11	AH61	IO_L16P_T2U_N6_QBC_AD3P_28	Bank28	1.2V,1.35V,1.5V,1.8V
H2	AK63	IO_L17N_T2U_N9_AD10N_28	Bank28	1.2V,1.35V,1.5V,1.8V
H1	AJ62	IO_L17P_T2U_N8_AD10P_28	Bank28	1.2V,1.35V,1.5V,1.8V
H5	AJ60	IO_L18N_T2U_N11_AD2N_28	Bank28	1.2V,1.35V,1.5V,1.8V
H4	AH60	IO_L18P_T2U_N10_AD2P_28	Bank28	1.2V,1.35V,1.5V,1.8V
H8	AP58	IO_L19N_T3L_N1_DBC_AD9N_28	Bank28	1.2V,1.35V,1.5V,1.8V
H7	AN58	IO_L19P_T3L_N0_DBC_AD9P_28	Bank28	1.2V,1.35V,1.5V,1.8V
J3	AL57	IO_L20N_T3L_N3_AD1N_28	Bank28	1.2V,1.35V,1.5V,1.8V
J2	AK57	IO_L20P_T3L_N2_AD1P_28	Bank28	1.2V,1.35V,1.5V,1.8V
J6	AN59	IO_L21N_T3L_N5_AD8N_28	Bank28	1.2V,1.35V,1.5V,1.8V
J5	AM59	IO_L21P_T3L_N4_AD8P_28	Bank28	1.2V,1.35V,1.5V,1.8V
J9	AK60	IO_L22N_T3U_N7_DBC_AD0N_28	Bank28	1.2V,1.35V,1.5V,1.8V
J8	AK59	IO_L22P_T3U_N6_DBC_AD0P_28	Bank28	1.2V,1.35V,1.5V,1.8V
K2	AM58	IO_L23N_T3U_N9_28	Bank28	1.2V,1.35V,1.5V,1.8V
K1	AM57	IO_L23P_T3U_N8_28	Bank28	1.2V,1.35V,1.5V,1.8V
K5	AK58	IO_L24N_T3U_N11_28	Bank28	1.2V,1.35V,1.5V,1.8V
K4	AJ58	IO_L24P_T3U_N10_28	Bank28	1.2V,1.35V,1.5V,1.8V
C15	AN56	IO_L1N_T0L_N1_DBC_29	Bank29	1.2V,1.35V,1.5V,1.8V

J5 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
C14	AN55	IO_L1P_T0L_N0_DBC_29	Bank29	1.2V,1.35V,1.5V,1.8V
C19	AL55	IO_L2N_T0L_N3_29	Bank29	1.2V,1.35V,1.5V,1.8V
C18	AL54	IO_L2P_T0L_N2_29	Bank29	1.2V,1.35V,1.5V,1.8V
C23	AN54	IO_L3N_T0L_N5_AD15N_29	Bank29	1.2V,1.35V,1.5V,1.8V
C22	AM54	IO_L3P_T0L_N4_AD15P_29	Bank29	1.2V,1.35V,1.5V,1.8V
D13	AK55	IO_L4N_T0U_N7_DBC_AD7N_29	Bank29	1.2V,1.35V,1.5V,1.8V
D12	AK54	IO_L4P_T0U_N6_DBC_AD7P_29	Bank29	1.2V,1.35V,1.5V,1.8V
D17	AM56	IO_L5N_T0U_N9_AD14N_29	Bank29	1.2V,1.35V,1.5V,1.8V
D16	AL56	IO_L5P_T0U_N8_AD14P_29	Bank29	1.2V,1.35V,1.5V,1.8V
D20	AJ56	IO_L6N_T0U_N11_AD6N_29	Bank29	1.2V,1.35V,1.5V,1.8V
D19	AJ55	IO_L6P_T0U_N10_AD6P_29	Bank29	1.2V,1.35V,1.5V,1.8V
E12	AN51	IO_L7N_T1L_N1_QBC_AD13N_29	Bank29	1.2V,1.35V,1.5V,1.8V
E11	AM51	IO_L7P_T1L_N0_QBC_AD13P_29	Bank29	1.2V,1.35V,1.5V,1.8V
E15	AJ53	IO_L8N_T1L_N3_AD5N_29	Bank29	1.2V,1.35V,1.5V,1.8V
E14	AJ52	IO_L8P_T1L_N2_AD5P_29	Bank29	1.2V,1.35V,1.5V,1.8V
E18	AN53	IO_L9N_T1L_N5_AD12N_29	Bank29	1.2V,1.35V,1.5V,1.8V
E17	AM53	IO_L9P_T1L_N4_AD12P_29	Bank29	1.2V,1.35V,1.5V,1.8V
F11	AJ51	IO_L10N_T1U_N7_QBC_AD4N_29	Bank29	1.2V,1.35V,1.5V,1.8V
F10	AJ50	IO_L10P_T1U_N6_QBC_AD4P_29	Bank29	1.2V,1.35V,1.5V,1.8V
F14	AK53	IO_L11N_T1U_N9_GC_29	Bank29	1.2V,1.35V,1.5V,1.8V
F13	AK52	IO_L11P_T1U_N8_GC_29	Bank29	1.2V,1.35V,1.5V,1.8V
F17	AL52	IO_L12N_T1U_N11_GC_29	Bank29	1.2V,1.35V,1.5V,1.8V
F16	AL51	IO_L12P_T1U_N10_GC_29	Bank29	1.2V,1.35V,1.5V,1.8V
G15	AL50	IO_L13N_T2L_N1_GC_QBC_29	Bank29	1.2V,1.35V,1.5V,1.8V
G14	AL49	IO_L13P_T2L_N0_GC_QBC_29	Bank29	1.2V,1.35V,1.5V,1.8V
G18	AK50	IO_L14N_T2L_N3_GC_29	Bank29	1.2V,1.35V,1.5V,1.8V
G17	AK49	IO_L14P_T2L_N2_GC_29	Bank29	1.2V,1.35V,1.5V,1.8V
G21	AN49	IO_L15N_T2L_N5_AD11N_29	Bank29	1.2V,1.35V,1.5V,1.8V
G20	AM49	IO_L15P_T2L_N4_AD11P_29	Bank29	1.2V,1.35V,1.5V,1.8V
H11	AK48	IO_L16N_T2U_N7_QBC_AD3N_29	Bank29	1.2V,1.35V,1.5V,1.8V
H10	AJ48	IO_L16P_T2U_N6_QBC_AD3P_29	Bank29	1.2V,1.35V,1.5V,1.8V
H14	AN48	IO_L17N_T2U_N9_AD10N_29	Bank29	1.2V,1.35V,1.5V,1.8V
H13	AM48	IO_L17P_T2U_N8_AD10P_29	Bank29	1.2V,1.35V,1.5V,1.8V
H17	AK47	IO_L18N_T2U_N11_AD2N_29	Bank29	1.2V,1.35V,1.5V,1.8V
H16	AJ47	IO_L18P_T2U_N10_AD2P_29	Bank29	1.2V,1.35V,1.5V,1.8V
H20	AM47	IO_L19N_T3L_N1_DBC_AD9N_29	Bank29	1.2V,1.35V,1.5V,1.8V
H19	AL47	IO_L19P_T3L_N0_DBC_AD9P_29	Bank29	1.2V,1.35V,1.5V,1.8V
J12	AM44	IO_L20N_T3L_N3_AD1N_29	Bank29	1.2V,1.35V,1.5V,1.8V
J11	AL44	IO_L20P_T3L_N2_AD1P_29	Bank29	1.2V,1.35V,1.5V,1.8V
J15	AN46	IO_L21N_T3L_N5_AD8N_29	Bank29	1.2V,1.35V,1.5V,1.8V
J14	AM46	IO_L21P_T3L_N4_AD8P_29	Bank29	1.2V,1.35V,1.5V,1.8V
J18	AK45	IO_L22N_T3U_N7_DBC_AD0N_29	Bank29	1.2V,1.35V,1.5V,1.8V
J17	AK44	IO_L22P_T3U_N6_DBC_AD0P_29	Bank29	1.2V,1.35V,1.5V,1.8V

J5 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
K11	AN45	IO_L23N_T3U_N9_29	Bank29	1.2V,1.35V,1.5V,1.8V
K10	AN44	IO_L23P_T3U_N8_29	Bank29	1.2V,1.35V,1.5V,1.8V
K14	AJ46	IO_L24N_T3U_N11_29	Bank29	1.2V,1.35V,1.5V,1.8V
K13	AJ45	IO_L24P_T3U_N10_29	Bank29	1.2V,1.35V,1.5V,1.8V
C27	AH56	IO_L1N_T0L_N1_DBC_30	Bank30	1.2V,1.35V,1.5V,1.8V
C26	AH55	IO_L1P_T0L_N0_DBC_30	Bank30	1.2V,1.35V,1.5V,1.8V
C30	AF57	IO_L2N_T0L_N3_30	Bank30	1.2V,1.35V,1.5V,1.8V
C29	AF56	IO_L2P_T0L_N2_30	Bank30	1.2V,1.35V,1.5V,1.8V
D25	AG57	IO_L3N_T0L_N5_AD15N_30	Bank30	1.2V,1.35V,1.5V,1.8V
D24	AG56	IO_L3P_T0L_N4_AD15P_30	Bank30	1.2V,1.35V,1.5V,1.8V
D28	AE55	IO_L4N_T0U_N7_DBC_AD7N_30	Bank30	1.2V,1.35V,1.5V,1.8V
D27	AE54	IO_L4P_T0U_N6_DBC_AD7P_30	Bank30	1.2V,1.35V,1.5V,1.8V
E21	AD57	IO_L5N_T0U_N9_AD14N_30	Bank30	1.2V,1.35V,1.5V,1.8V
E20	AE57	IO_L5P_T0U_N8_AD14P_30	Bank30	1.2V,1.35V,1.5V,1.8V
E24	AD56	IO_L6N_T0U_N11_AD6N_30	Bank30	1.2V,1.35V,1.5V,1.8V
E23	AD55	IO_L6P_T0U_N10_AD6P_30	Bank30	1.2V,1.35V,1.5V,1.8V
E27	AH54	IO_L7N_T1L_N1_QBC_AD13N_30	Bank30	1.2V,1.35V,1.5V,1.8V
E26	AH53	IO_L7P_T1L_N0_QBC_AD13P_30	Bank30	1.2V,1.35V,1.5V,1.8V
E30	AD53	IO_L8N_T1L_N3_AD5N_30	Bank30	1.2V,1.35V,1.5V,1.8V
E29	AD52	IO_L8P_T1L_N2_AD5P_30	Bank30	1.2V,1.35V,1.5V,1.8V
F20	AG54	IO_L9N_T1L_N5_AD12N_30	Bank30	1.2V,1.35V,1.5V,1.8V
F19	AG53	IO_L9P_T1L_N4_AD12P_30	Bank30	1.2V,1.35V,1.5V,1.8V
F23	AE53	IO_L10N_T1U_N7_QBC_AD4N_30	Bank30	1.2V,1.35V,1.5V,1.8V
F22	AE52	IO_L10P_T1U_N6_QBC_AD4P_30	Bank30	1.2V,1.35V,1.5V,1.8V
F26	AF52	IO_L11N_T1U_N9_GC_30	Bank30	1.2V,1.35V,1.5V,1.8V
F25	AF51	IO_L11P_T1U_N8_GC_30	Bank30	1.2V,1.35V,1.5V,1.8V
F29	AG52	IO_L12N_T1U_N11_GC_30	Bank30	1.2V,1.35V,1.5V,1.8V
F28	AG51	IO_L12P_T1U_N10_GC_30	Bank30	1.2V,1.35V,1.5V,1.8V
G24	AF50	IO_L13N_T2L_N1_GC_QBC_30	Bank30	1.2V,1.35V,1.5V,1.8V
G23	AF49	IO_L13P_T2L_N0_GC_QBC_30	Bank30	1.2V,1.35V,1.5V,1.8V
G27	AE50	IO_L14N_T2L_N3_GC_30	Bank30	1.2V,1.35V,1.5V,1.8V
G26	AE49	IO_L14P_T2L_N2_GC_30	Bank30	1.2V,1.35V,1.5V,1.8V
G30	AH51	IO_L15N_T2L_N5_AD11N_30	Bank30	1.2V,1.35V,1.5V,1.8V
G29	AH50	IO_L15P_T2L_N4_AD11P_30	Bank30	1.2V,1.35V,1.5V,1.8V
H23	AH49	IO_L16N_T2U_N7_QBC_AD3N_30	Bank30	1.2V,1.35V,1.5V,1.8V
H22	AH48	IO_L16P_T2U_N6_QBC_AD3P_30	Bank30	1.2V,1.35V,1.5V,1.8V
H26	AD51	IO_L17N_T2U_N9_AD10N_30	Bank30	1.2V,1.35V,1.5V,1.8V
H25	AD50	IO_L17P_T2U_N8_AD10P_30	Bank30	1.2V,1.35V,1.5V,1.8V
H29	AG49	IO_L18N_T2U_N11_AD2N_30	Bank30	1.2V,1.35V,1.5V,1.8V
H28	AG48	IO_L18P_T2U_N10_AD2P_30	Bank30	1.2V,1.35V,1.5V,1.8V
J21	AG47	IO_L19N_T3L_N1_DBC_AD9N_30	Bank30	1.2V,1.35V,1.5V,1.8V
J20	AG46	IO_L19P_T3L_N0_DBC_AD9P_30	Bank30	1.2V,1.35V,1.5V,1.8V
J24	AG44	IO_L20N_T3L_N3_AD1N_30	Bank30	1.2V,1.35V,1.5V,1.8V

J5 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
J23	AH44	IO_L20P_T3L_N2_AD1P_30	Bank30	1.2V,1.35V,1.5V,1.8V
J27	AF47	IO_L21N_T3L_N5_AD8N_30	Bank30	1.2V,1.35V,1.5V,1.8V
J26	AF46	IO_L21P_T3L_N4_AD8P_30	Bank30	1.2V,1.35V,1.5V,1.8V
J30	AE45	IO_L22N_T3U_N7_DBC_AD0N_30	Bank30	1.2V,1.35V,1.5V,1.8V
J29	AF45	IO_L22P_T3U_N6_DBC_AD0P_30	Bank30	1.2V,1.35V,1.5V,1.8V
K20	AE48	IO_L23N_T3U_N9_30	Bank30	1.2V,1.35V,1.5V,1.8V
K19	AE47	IO_L23P_T3U_N8_30	Bank30	1.2V,1.35V,1.5V,1.8V
K23	AD47	IO_L24N_T3U_N11_30	Bank30	1.2V,1.35V,1.5V,1.8V
K22	AD46	IO_L24P_T3U_N10_30	Bank30	1.2V,1.35V,1.5V,1.8V

Table 5-9 Prodigy Connector – J6

J6 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	BT3	MGTYRXN0_221	Bank221	
A14	BT4	MGTYRXP0_221	Bank221	
A11	BR1	MGTYRXN1_221	Bank221	
A10	BR2	MGTYRXP1_221	Bank221	
A7	BP3	MGTYRXN2_221	Bank221	
A6	BP4	MGTYRXP2_221	Bank221	
A3	BN1	MGTYRXN3_221	Bank221	
A2	BN2	MGTYRXP3_221	Bank221	
B17	BV8	MGTYTXN0_221	Bank221	
B16	BV9	MGTYTXP0_221	Bank221	
B13	BU6	MGTYTXN1_221	Bank221	
B12	BU7	MGTYTXP1_221	Bank221	
B9	BT8	MGTYTXN2_221	Bank221	
B8	BT9	MGTYTXP2_221	Bank221	
B5	BR6	MGTYTXN3_221	Bank221	
B4	BR7	MGTYTXP3_221	Bank221	
A19	BW10	MGTREFCLK0N_221	Bank221	
A18	BW11	MGTREFCLK0P_221	Bank221	
B21	BU10	MGTREFCLK1N_221	Bank221	
B20	BU11	MGTREFCLK1P_221	Bank221	
C3	CA60	IO_L1N_T0L_N1_DBC_22	Bank22	1.2V,1.35V,1.5V,1.8V
C2	CA59	IO_L1P_T0L_N0_DBC_22	Bank22	1.2V,1.35V,1.5V,1.8V
C7	CC58	IO_L2N_T0L_N3_22	Bank22	1.2V,1.35V,1.5V,1.8V
C6	CB58	IO_L2P_T0L_N2_22	Bank22	1.2V,1.35V,1.5V,1.8V
C11	CA61	IO_L3N_T0L_N5_AD15N_22	Bank22	1.2V,1.35V,1.5V,1.8V
C10	BY60	IO_L3P_T0L_N4_AD15P_22	Bank22	1.2V,1.35V,1.5V,1.8V
D2	CC59	IO_L4N_T0U_N7_DBC_AD7N_22	Bank22	1.2V,1.35V,1.5V,1.8V
D1	CB59	IO_L4P_T0U_N6_DBC_AD7P_22	Bank22	1.2V,1.35V,1.5V,1.8V
D5	BW63	IO_L5N_T0U_N9_AD14N_22	Bank22	1.2V,1.35V,1.5V,1.8V

J6 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D4	BW62	IO_L5P_T0U_N8_AD14P_22	Bank22	1.2V,1.35V,1.5V,1.8V
D8	BY59	IO_L6N_T0U_N11_AD6N_22	Bank22	1.2V,1.35V,1.5V,1.8V
D7	BY58	IO_L6P_T0U_N10_AD6P_22	Bank22	1.2V,1.35V,1.5V,1.8V
E3	BW58	IO_L7N_T1L_N1_QBC_AD13N_22	Bank22	1.2V,1.35V,1.5V,1.8V
E2	BV58	IO_L7P_T1L_N0_QBC_AD13P_22	Bank22	1.2V,1.35V,1.5V,1.8V
E6	BV59	IO_L8N_T1L_N3_AD5N_22	Bank22	1.2V,1.35V,1.5V,1.8V
E5	BU59	IO_L8P_T1L_N2_AD5P_22	Bank22	1.2V,1.35V,1.5V,1.8V
E9	BV63	IO_L9N_T1L_N5_AD12N_22	Bank22	1.2V,1.35V,1.5V,1.8V
E8	BU63	IO_L9P_T1L_N4_AD12P_22	Bank22	1.2V,1.35V,1.5V,1.8V
F2	BU62	IO_L10N_T1U_N7_QBC_AD4N_22	Bank22	1.2V,1.35V,1.5V,1.8V
F1	BT62	IO_L10P_T1U_N6_QBC_AD4P_22	Bank22	1.2V,1.35V,1.5V,1.8V
F5	BW60	IO_L11N_T1U_N9_GC_22	Bank22	1.2V,1.35V,1.5V,1.8V
F4	BV60	IO_L11P_T1U_N8_GC_22	Bank22	1.2V,1.35V,1.5V,1.8V
F8	BV61	IO_L12N_T1U_N11_GC_22	Bank22	1.2V,1.35V,1.5V,1.8V
F7	BU61	IO_L12P_T1U_N10_GC_22	Bank22	1.2V,1.35V,1.5V,1.8V
G3	BR60	IO_L13N_T2L_N1_GC_QBC_22	Bank22	1.2V,1.35V,1.5V,1.8V
G2	BP60	IO_L13P_T2L_N0_GC_QBC_22	Bank22	1.2V,1.35V,1.5V,1.8V
G6	BT61	IO_L14N_T2L_N3_GC_22	Bank22	1.2V,1.35V,1.5V,1.8V
G5	BT60	IO_L14P_T2L_N2_GC_22	Bank22	1.2V,1.35V,1.5V,1.8V
G9	BP63	IO_L15N_T2L_N5_AD11N_22	Bank22	1.2V,1.35V,1.5V,1.8V
G8	BP62	IO_L15P_T2L_N4_AD11P_22	Bank22	1.2V,1.35V,1.5V,1.8V
G12	BT59	IO_L16N_T2U_N7_QBC_AD3N_22	Bank22	1.2V,1.35V,1.5V,1.8V
G11	BR59	IO_L16P_T2U_N6_QBC_AD3P_22	Bank22	1.2V,1.35V,1.5V,1.8V
H2	BP61	IO_L17N_T2U_N9_AD10N_22	Bank22	1.2V,1.35V,1.5V,1.8V
H1	BN61	IO_L17P_T2U_N8_AD10P_22	Bank22	1.2V,1.35V,1.5V,1.8V
H5	BR63	IO_L18N_T2U_N11_AD2N_22	Bank22	1.2V,1.35V,1.5V,1.8V
H4	BR62	IO_L18P_T2U_N10_AD2P_22	Bank22	1.2V,1.35V,1.5V,1.8V
H8	BN60	IO_L19N_T3L_N1_DBC_AD9N_22	Bank22	1.2V,1.35V,1.5V,1.8V
H7	BN59	IO_L19P_T3L_N0_DBC_AD9P_22	Bank22	1.2V,1.35V,1.5V,1.8V
J3	BM62	IO_L20N_T3L_N3_AD1N_22	Bank22	1.2V,1.35V,1.5V,1.8V
J2	BL62	IO_L20P_T3L_N2_AD1P_22	Bank22	1.2V,1.35V,1.5V,1.8V
J6	BL60	IO_L21N_T3L_N5_AD8N_22	Bank22	1.2V,1.35V,1.5V,1.8V
J5	BK60	IO_L21P_T3L_N4_AD8P_22	Bank22	1.2V,1.35V,1.5V,1.8V
J9	BK63	IO_L22N_T3U_N7_DBC_AD0N_22	Bank22	1.2V,1.35V,1.5V,1.8V
J8	BK62	IO_L22P_T3U_N6_DBC_AD0P_22	Bank22	1.2V,1.35V,1.5V,1.8V
K2	BM59	IO_L23N_T3U_N9_22	Bank22	1.2V,1.35V,1.5V,1.8V
K1	BL59	IO_L23P_T3U_N8_22	Bank22	1.2V,1.35V,1.5V,1.8V
K5	BM61	IO_L24N_T3U_N11_22	Bank22	1.2V,1.35V,1.5V,1.8V
K4	BL61	IO_L24P_T3U_N10_22	Bank22	1.2V,1.35V,1.5V,1.8V
C15	BJ52	IO_L1N_T0L_N1_DBC_23	Bank23	1.2V,1.35V,1.5V,1.8V
C14	BJ51	IO_L1P_T0L_N0_DBC_23	Bank23	1.2V,1.35V,1.5V,1.8V
C19	BM52	IO_L2N_T0L_N3_23	Bank23	1.2V,1.35V,1.5V,1.8V
C18	BM51	IO_L2P_T0L_N2_23	Bank23	1.2V,1.35V,1.5V,1.8V

J6 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
C23	BK53	IO_L3N_T0L_N5_AD15N_23	Bank23	1.2V,1.35V,1.5V,1.8V
C22	BK52	IO_L3P_T0L_N4_AD15P_23	Bank23	1.2V,1.35V,1.5V,1.8V
D13	BL52	IO_L4N_T0U_N7_DBC_AD7N_23	Bank23	1.2V,1.35V,1.5V,1.8V
D12	BL51	IO_L4P_T0U_N6_DBC_AD7P_23	Bank23	1.2V,1.35V,1.5V,1.8V
D17	BM54	IO_L5N_T0U_N9_AD14N_23	Bank23	1.2V,1.35V,1.5V,1.8V
D16	BM53	IO_L5P_T0U_N8_AD14P_23	Bank23	1.2V,1.35V,1.5V,1.8V
D20	BL50	IO_L6N_T0U_N11_AD6N_23	Bank23	1.2V,1.35V,1.5V,1.8V
D19	BK50	IO_L6P_T0U_N10_AD6P_23	Bank23	1.2V,1.35V,1.5V,1.8V
E12	BN51	IO_L7N_T1L_N1_QBC_AD13N_23	Bank23	1.2V,1.35V,1.5V,1.8V
E11	BN50	IO_L7P_T1L_N0_QBC_AD13P_23	Bank23	1.2V,1.35V,1.5V,1.8V
E15	BR53	IO_L8N_T1L_N3_AD5N_23	Bank23	1.2V,1.35V,1.5V,1.8V
E14	BR52	IO_L8P_T1L_N2_AD5P_23	Bank23	1.2V,1.35V,1.5V,1.8V
E18	BT51	IO_L9N_T1L_N5_AD12N_23	Bank23	1.2V,1.35V,1.5V,1.8V
E17	BT50	IO_L9P_T1L_N4_AD12P_23	Bank23	1.2V,1.35V,1.5V,1.8V
F11	BR50	IO_L10N_T1U_N7_QBC_AD4N_23	Bank23	1.2V,1.35V,1.5V,1.8V
F10	BP50	IO_L10P_T1U_N6_QBC_AD4P_23	Bank23	1.2V,1.35V,1.5V,1.8V
F14	BN54	IO_L11N_T1U_N9_GC_23	Bank23	1.2V,1.35V,1.5V,1.8V
F13	BN53	IO_L11P_T1U_N8_GC_23	Bank23	1.2V,1.35V,1.5V,1.8V
F17	BP53	IO_L12N_T1U_N11_GC_23	Bank23	1.2V,1.35V,1.5V,1.8V
F16	BP52	IO_L12P_T1U_N10_GC_23	Bank23	1.2V,1.35V,1.5V,1.8V
G15	BP55	IO_L13N_T2L_N1_GC_QBC_23	Bank23	1.2V,1.35V,1.5V,1.8V
G14	BN55	IO_L13P_T2L_N0_GC_QBC_23	Bank23	1.2V,1.35V,1.5V,1.8V
G18	BP56	IO_L14N_T2L_N3_GC_23	Bank23	1.2V,1.35V,1.5V,1.8V
G17	BN56	IO_L14P_T2L_N2_GC_23	Bank23	1.2V,1.35V,1.5V,1.8V
G21	BR55	IO_L15N_T2L_N5_AD11N_23	Bank23	1.2V,1.35V,1.5V,1.8V
G20	BR54	IO_L15P_T2L_N4_AD11P_23	Bank23	1.2V,1.35V,1.5V,1.8V
H11	BP58	IO_L16N_T2U_N7_QBC_AD3N_23	Bank23	1.2V,1.35V,1.5V,1.8V
H10	BP57	IO_L16P_T2U_N6_QBC_AD3P_23	Bank23	1.2V,1.35V,1.5V,1.8V
H14	BR58	IO_L17N_T2U_N9_AD10N_23	Bank23	1.2V,1.35V,1.5V,1.8V
H13	BR57	IO_L17P_T2U_N8_AD10P_23	Bank23	1.2V,1.35V,1.5V,1.8V
H17	BN58	IO_L18N_T2U_N11_AD2N_23	Bank23	1.2V,1.35V,1.5V,1.8V
H16	BM58	IO_L18P_T2U_N10_AD2P_23	Bank23	1.2V,1.35V,1.5V,1.8V
H20	BL54	IO_L19N_T3L_N1_DBC_AD9N_23	Bank23	1.2V,1.35V,1.5V,1.8V
H19	BK54	IO_L19P_T3L_N0_DBC_AD9P_23	Bank23	1.2V,1.35V,1.5V,1.8V
J12	BM57	IO_L20N_T3L_N3_AD1N_23	Bank23	1.2V,1.35V,1.5V,1.8V
J11	BL57	IO_L20P_T3L_N2_AD1P_23	Bank23	1.2V,1.35V,1.5V,1.8V
J15	BL55	IO_L21N_T3L_N5_AD8N_23	Bank23	1.2V,1.35V,1.5V,1.8V
J14	BK55	IO_L21P_T3L_N4_AD8P_23	Bank23	1.2V,1.35V,1.5V,1.8V
J18	BK58	IO_L22N_T3U_N7_DBC_AD0N_23	Bank23	1.2V,1.35V,1.5V,1.8V
J17	BK57	IO_L22P_T3U_N6_DBC_AD0P_23	Bank23	1.2V,1.35V,1.5V,1.8V
K11	BJ56	IO_L23N_T3U_N9_23	Bank23	1.2V,1.35V,1.5V,1.8V
K10	BJ55	IO_L23P_T3U_N8_23	Bank23	1.2V,1.35V,1.5V,1.8V
K14	BJ58	IO_L24N_T3U_N11_23	Bank23	1.2V,1.35V,1.5V,1.8V

J6 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
K13	BJ57	IO_L24P_T3U_N10_23	Bank23	1.2V,1.35V,1.5V,1.8V
C27	BD48	IO_L1N_T0L_N1_DBC_24	Bank24	1.2V,1.35V,1.5V,1.8V
C26	BD47	IO_L1P_T0L_N0_DBC_24	Bank24	1.2V,1.35V,1.5V,1.8V
C30	BH46	IO_L2N_T0L_N3_24	Bank24	1.2V,1.35V,1.5V,1.8V
C29	BH45	IO_L2P_T0L_N2_24	Bank24	1.2V,1.35V,1.5V,1.8V
D25	BD46	IO_L3N_T0L_N5_AD15N_24	Bank24	1.2V,1.35V,1.5V,1.8V
D24	BD45	IO_L3P_T0L_N4_AD15P_24	Bank24	1.2V,1.35V,1.5V,1.8V
D28	BG47	IO_L4N_T0U_N7_DBC_AD7N_24	Bank24	1.2V,1.35V,1.5V,1.8V
D27	BG46	IO_L4P_T0U_N6_DBC_AD7P_24	Bank24	1.2V,1.35V,1.5V,1.8V
E21	BF45	IO_L5N_T0U_N9_AD14N_24	Bank24	1.2V,1.35V,1.5V,1.8V
E20	BE45	IO_L5P_T0U_N8_AD14P_24	Bank24	1.2V,1.35V,1.5V,1.8V
E24	BF47	IO_L6N_T0U_N11_AD6N_24	Bank24	1.2V,1.35V,1.5V,1.8V
E23	BF46	IO_L6P_T0U_N10_AD6P_24	Bank24	1.2V,1.35V,1.5V,1.8V
E27	BH51	IO_L7N_T1L_N1_QBC_AD13N_24	Bank24	1.2V,1.35V,1.5V,1.8V
E26	BH50	IO_L7P_T1L_N0_QBC_AD13P_24	Bank24	1.2V,1.35V,1.5V,1.8V
E30	BH48	IO_L8N_T1L_N3_AD5N_24	Bank24	1.2V,1.35V,1.5V,1.8V
E29	BG48	IO_L8P_T1L_N2_AD5P_24	Bank24	1.2V,1.35V,1.5V,1.8V
F20	BD51	IO_L9N_T1L_N5_AD12N_24	Bank24	1.2V,1.35V,1.5V,1.8V
F19	BD50	IO_L9P_T1L_N4_AD12P_24	Bank24	1.2V,1.35V,1.5V,1.8V
F23	BH49	IO_L10N_T1U_N7_QBC_AD4N_24	Bank24	1.2V,1.35V,1.5V,1.8V
F22	BG49	IO_L10P_T1U_N6_QBC_AD4P_24	Bank24	1.2V,1.35V,1.5V,1.8V
F26	BF50	IO_L11N_T1U_N9_GC_24	Bank24	1.2V,1.35V,1.5V,1.8V
F25	BE50	IO_L11P_T1U_N8_GC_24	Bank24	1.2V,1.35V,1.5V,1.8V
F29	BF49	IO_L12N_T1U_N11_GC_24	Bank24	1.2V,1.35V,1.5V,1.8V
F28	BE49	IO_L12P_T1U_N10_GC_24	Bank24	1.2V,1.35V,1.5V,1.8V
G24	BG52	IO_L13N_T2L_N1_GC_QBC_24	Bank24	1.2V,1.35V,1.5V,1.8V
G23	BF52	IO_L13P_T2L_N0_GC_QBC_24	Bank24	1.2V,1.35V,1.5V,1.8V
G27	BG51	IO_L14N_T2L_N3_GC_24	Bank24	1.2V,1.35V,1.5V,1.8V
G26	BF51	IO_L14P_T2L_N2_GC_24	Bank24	1.2V,1.35V,1.5V,1.8V
G30	BE52	IO_L15N_T2L_N5_AD11N_24	Bank24	1.2V,1.35V,1.5V,1.8V
G29	BD52	IO_L15P_T2L_N4_AD11P_24	Bank24	1.2V,1.35V,1.5V,1.8V
H23	BH53	IO_L16N_T2U_N7_QBC_AD3N_24	Bank24	1.2V,1.35V,1.5V,1.8V
H22	BG53	IO_L16P_T2U_N6_QBC_AD3P_24	Bank24	1.2V,1.35V,1.5V,1.8V
H26	BE53	IO_L17N_T2U_N9_AD10N_24	Bank24	1.2V,1.35V,1.5V,1.8V
H25	BD53	IO_L17P_T2U_N8_AD10P_24	Bank24	1.2V,1.35V,1.5V,1.8V
H29	BH54	IO_L18N_T2U_N11_AD2N_24	Bank24	1.2V,1.35V,1.5V,1.8V
H28	BG54	IO_L18P_T2U_N10_AD2P_24	Bank24	1.2V,1.35V,1.5V,1.8V
J21	BE55	IO_L19N_T3L_N1_DBC_AD9N_24	Bank24	1.2V,1.35V,1.5V,1.8V
J20	BE54	IO_L19P_T3L_N0_DBC_AD9P_24	Bank24	1.2V,1.35V,1.5V,1.8V
J24	BH56	IO_L20N_T3L_N3_AD1N_24	Bank24	1.2V,1.35V,1.5V,1.8V
J23	BG56	IO_L20P_T3L_N2_AD1P_24	Bank24	1.2V,1.35V,1.5V,1.8V
J27	BD56	IO_L21N_T3L_N5_AD8N_24	Bank24	1.2V,1.35V,1.5V,1.8V
J26	BD55	IO_L21P_T3L_N4_AD8P_24	Bank24	1.2V,1.35V,1.5V,1.8V

J6 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
J30	BG57	IO_L22N_T3U_N7_DBC_AD0N_24	Bank24	1.2V,1.35V,1.5V,1.8V
J29	BF57	IO_L22P_T3U_N6_DBC_AD0P_24	Bank24	1.2V,1.35V,1.5V,1.8V
K20	BE57	IO_L23N_T3U_N9_24	Bank24	1.2V,1.35V,1.5V,1.8V
K19	BD57	IO_L23P_T3U_N8_24	Bank24	1.2V,1.35V,1.5V,1.8V
K23	BF56	IO_L24N_T3U_N11_24	Bank24	1.2V,1.35V,1.5V,1.8V
K22	BF55	IO_L24P_T3U_N10_24	Bank24	1.2V,1.35V,1.5V,1.8V

Table 5-10 Prodigy Connector – J7

J7 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	BM3	MGTYRXN0_222	Bank222	
A14	BM4	MGTYRXP0_222	Bank222	
A11	BL1	MGTYRXN1_222	Bank222	
A10	BL2	MGTYRXP1_222	Bank222	
A7	BK3	MGTYRXN2_222	Bank222	
A6	BK4	MGTYRXP2_222	Bank222	
A3	BJ1	MGTYRXN3_222	Bank222	
A2	BJ2	MGTYRXP3_222	Bank222	
B17	BP8	MGTYTXN0_222	Bank222	
B16	BP9	MGTYTXP0_222	Bank222	
B13	BN6	MGTYTXN1_222	Bank222	
B12	BN7	MGTYTXP1_222	Bank222	
B9	BM8	MGTYTXN2_222	Bank222	
B8	BM9	MGTYTXP2_222	Bank222	
B5	BL6	MGTYTXN3_222	Bank222	
B4	BL7	MGTYTXP3_222	Bank222	
A19	BR10	MGTREFCLK0N_222	Bank222	
A18	BR11	MGTREFCLK0P_222	Bank222	
B21	BN10	MGTREFCLK1N_222	Bank222	
B20	BN11	MGTREFCLK1P_222	Bank222	
C3	BU28	IO_L1N_T0L_N1_DBC_63	Bank63	1.2V,1.35V,1.5V,1.8V
C2	BU29	IO_L1P_T0L_N0_DBC_63	Bank63	1.2V,1.35V,1.5V,1.8V
C7	BW27	IO_L2N_T0L_N3_63	Bank63	1.2V,1.35V,1.5V,1.8V
C6	BW28	IO_L2P_T0L_N2_63	Bank63	1.2V,1.35V,1.5V,1.8V
C11	BV28	IO_L3N_T0L_N5_AD15N_63	Bank63	1.2V,1.35V,1.5V,1.8V
C10	BV29	IO_L3P_T0L_N4_AD15P_63	Bank63	1.2V,1.35V,1.5V,1.8V
D2	BW25	IO_L4N_T0U_N7_DBC_AD7N_63	Bank63	1.2V,1.35V,1.5V,1.8V
D1	BW26	IO_L4P_T0U_N6_DBC_AD7P_63	Bank63	1.2V,1.35V,1.5V,1.8V
D5	BV25	IO_L5N_T0U_N9_AD14N_63	Bank63	1.2V,1.35V,1.5V,1.8V
D4	BV26	IO_L5P_T0U_N8_AD14P_63	Bank63	1.2V,1.35V,1.5V,1.8V
D8	BY27	IO_L6N_T0U_N11_AD6N_63	Bank63	1.2V,1.35V,1.5V,1.8V
D7	BY28	IO_L6P_T0U_N10_AD6P_63	Bank63	1.2V,1.35V,1.5V,1.8V
E3	BY24	IO_L7N_T1L_N1_QBC_AD13N_63	Bank63	1.2V,1.35V,1.5V,1.8V

J7 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
E2	BY25	IO_L7P_T1L_N0_QBC_AD13P_63	Bank63	1.2V,1.35V,1.5V,1.8V
E6	CA24	IO_L8N_T1L_N3_AD5N_63	Bank63	1.2V,1.35V,1.5V,1.8V
E5	CA25	IO_L8P_T1L_N2_AD5P_63	Bank63	1.2V,1.35V,1.5V,1.8V
E9	CC25	IO_L9N_T1L_N5_AD12N_63	Bank63	1.2V,1.35V,1.5V,1.8V
E8	CC26	IO_L9P_T1L_N4_AD12P_63	Bank63	1.2V,1.35V,1.5V,1.8V
F2	CC24	IO_L10N_T1U_N7_QBC_AD4N_63	Bank63	1.2V,1.35V,1.5V,1.8V
F1	CB24	IO_L10P_T1U_N6_QBC_AD4P_63	Bank63	1.2V,1.35V,1.5V,1.8V
F5	CA26	IO_L11N_T1U_N9_GC_63	Bank63	1.2V,1.35V,1.5V,1.8V
F4	CA27	IO_L11P_T1U_N8_GC_63	Bank63	1.2V,1.35V,1.5V,1.8V
F8	CB26	IO_L12N_T1U_N11_GC_63	Bank63	1.2V,1.35V,1.5V,1.8V
F7	CB27	IO_L12P_T1U_N10_GC_63	Bank63	1.2V,1.35V,1.5V,1.8V
G3	CB29	IO_L13N_T2L_N1_GC_QBC_63	Bank63	1.2V,1.35V,1.5V,1.8V
G2	CA29	IO_L13P_T2L_N0_GC_QBC_63	Bank63	1.2V,1.35V,1.5V,1.8V
G6	CA30	IO_L14N_T2L_N3_GC_63	Bank63	1.2V,1.35V,1.5V,1.8V
G5	CA31	IO_L14P_T2L_N2_GC_63	Bank63	1.2V,1.35V,1.5V,1.8V
G9	CC28	IO_L15N_T2L_N5_AD11N_63	Bank63	1.2V,1.35V,1.5V,1.8V
G8	CC29	IO_L15P_T2L_N4_AD11P_63	Bank63	1.2V,1.35V,1.5V,1.8V
G12	CB32	IO_L16N_T2U_N7_QBC_AD3N_63	Bank63	1.2V,1.35V,1.5V,1.8V
G11	CA32	IO_L16P_T2U_N6_QBC_AD3P_63	Bank63	1.2V,1.35V,1.5V,1.8V
H2	CC30	IO_L17N_T2U_N9_AD10N_63	Bank63	1.2V,1.35V,1.5V,1.8V
H1	CC31	IO_L17P_T2U_N8_AD10P_63	Bank63	1.2V,1.35V,1.5V,1.8V
H5	CC33	IO_L18N_T2U_N11_AD2N_63	Bank63	1.2V,1.35V,1.5V,1.8V
H4	CB33	IO_L18P_T2U_N10_AD2P_63	Bank63	1.2V,1.35V,1.5V,1.8V
H8	BY29	IO_L19N_T3L_N1_DBC_AD9N_63	Bank63	1.2V,1.35V,1.5V,1.8V
H7	BY30	IO_L19P_T3L_N0_DBC_AD9P_63	Bank63	1.2V,1.35V,1.5V,1.8V
J3	BW32	IO_L20N_T3L_N3_AD1N_63	Bank63	1.2V,1.35V,1.5V,1.8V
J2	BW33	IO_L20P_T3L_N2_AD1P_63	Bank63	1.2V,1.35V,1.5V,1.8V
J6	BW30	IO_L21N_T3L_N5_AD8N_63	Bank63	1.2V,1.35V,1.5V,1.8V
J5	BW31	IO_L21P_T3L_N4_AD8P_63	Bank63	1.2V,1.35V,1.5V,1.8V
J9	BY33	IO_L22N_T3U_N7_DBC_AD0N_63	Bank63	1.2V,1.35V,1.5V,1.8V
J8	BY34	IO_L22P_T3U_N6_DBC_AD0P_63	Bank63	1.2V,1.35V,1.5V,1.8V
K2	BV30	IO_L23N_T3U_N9_63	Bank63	1.2V,1.35V,1.5V,1.8V
K1	BV31	IO_L23P_T3U_N8_63	Bank63	1.2V,1.35V,1.5V,1.8V
K5	BV33	IO_L24N_T3U_N11_63	Bank63	1.2V,1.35V,1.5V,1.8V
K4	BV34	IO_L24P_T3U_N10_63	Bank63	1.2V,1.35V,1.5V,1.8V
C15	BR32	IO_L1N_T0L_N1_DBC_64	Bank64	1.2V,1.35V,1.5V,1.8V
C14	BR33	IO_L1P_T0L_N0_DBC_64	Bank64	1.2V,1.35V,1.5V,1.8V
C19	BU32	IO_L2N_T0L_N3_64	Bank64	1.2V,1.35V,1.5V,1.8V
C18	BT32	IO_L2P_T0L_N2_64	Bank64	1.2V,1.35V,1.5V,1.8V
C23	BT30	IO_L3N_T0L_N5_AD15N_64	Bank64	1.2V,1.35V,1.5V,1.8V
C22	BR30	IO_L3P_T0L_N4_AD15P_64	Bank64	1.2V,1.35V,1.5V,1.8V
D13	BU33	IO_L4N_T0U_N7_DBC_AD7N_64	Bank64	1.2V,1.35V,1.5V,1.8V
D12	BU34	IO_L4P_T0U_N6_DBC_AD7P_64	Bank64	1.2V,1.35V,1.5V,1.8V
D17	BU31	IO_L5N_T0U_N9_AD14N_64	Bank64	1.2V,1.35V,1.5V,1.8V

J7 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D16	BT31	IO_L5P_T0U_N8_AD14P_64	Bank64	1.2V,1.35V,1.5V,1.8V
D20	BT34	IO_L6N_T0U_N11_AD6N_64	Bank64	1.2V,1.35V,1.5V,1.8V
D19	BR34	IO_L6P_T0U_N10_AD6P_64	Bank64	1.2V,1.35V,1.5V,1.8V
E12	BP30	IO_L7N_T1L_N1_QBC_AD13N_64	Bank64	1.2V,1.35V,1.5V,1.8V
E11	BP31	IO_L7P_T1L_N0_QBC_AD13P_64	Bank64	1.2V,1.35V,1.5V,1.8V
E15	BN33	IO_L8N_T1L_N3_AD5N_64	Bank64	1.2V,1.35V,1.5V,1.8V
E14	BN34	IO_L8P_T1L_N2_AD5P_64	Bank64	1.2V,1.35V,1.5V,1.8V
E18	BN30	IO_L9N_T1L_N5_AD12N_64	Bank64	1.2V,1.35V,1.5V,1.8V
E17	BN31	IO_L9P_T1L_N4_AD12P_64	Bank64	1.2V,1.35V,1.5V,1.8V
F11	BM33	IO_L10N_T1U_N7_QBC_AD4N_64	Bank64	1.2V,1.35V,1.5V,1.8V
F10	BM34	IO_L10P_T1U_N6_QBC_AD4P_64	Bank64	1.2V,1.35V,1.5V,1.8V
F14	BM31	IO_L11N_T1U_N9_GC_64	Bank64	1.2V,1.35V,1.5V,1.8V
F13	BL31	IO_L11P_T1U_N8_GC_64	Bank64	1.2V,1.35V,1.5V,1.8V
F17	BM32	IO_L12N_T1U_N11_GC_64	Bank64	1.2V,1.35V,1.5V,1.8V
F16	BL32	IO_L12P_T1U_N10_GC_64	Bank64	1.2V,1.35V,1.5V,1.8V
G15	BK32	IO_L13N_T2L_N1_GC_QBC_64	Bank64	1.2V,1.35V,1.5V,1.8V
G14	BJ32	IO_L13P_T2L_N0_GC_QBC_64	Bank64	1.2V,1.35V,1.5V,1.8V
G18	BK33	IO_L14N_T2L_N3_GC_64	Bank64	1.2V,1.35V,1.5V,1.8V
G17	BJ33	IO_L14P_T2L_N2_GC_64	Bank64	1.2V,1.35V,1.5V,1.8V
G21	BJ30	IO_L15N_T2L_N5_AD11N_64	Bank64	1.2V,1.35V,1.5V,1.8V
G20	BJ31	IO_L15P_T2L_N4_AD11P_64	Bank64	1.2V,1.35V,1.5V,1.8V
H11	BH30	IO_L16N_T2U_N7_QBC_AD3N_64	Bank64	1.2V,1.35V,1.5V,1.8V
H10	BH31	IO_L16P_T2U_N6_QBC_AD3P_64	Bank64	1.2V,1.35V,1.5V,1.8V
H14	BL30	IO_L17N_T2U_N9_AD10N_64	Bank64	1.2V,1.35V,1.5V,1.8V
H13	BK30	IO_L17P_T2U_N8_AD10P_64	Bank64	1.2V,1.35V,1.5V,1.8V
H17	BL34	IO_L18N_T2U_N11_AD2N_64	Bank64	1.2V,1.35V,1.5V,1.8V
H16	BK34	IO_L18P_T2U_N10_AD2P_64	Bank64	1.2V,1.35V,1.5V,1.8V
H20	BG31	IO_L19N_T3L_N1_DBC_AD9N_64	Bank64	1.2V,1.35V,1.5V,1.8V
H19	BG32	IO_L19P_T3L_N0_DBC_AD9P_64	Bank64	1.2V,1.35V,1.5V,1.8V
J12	BE32	IO_L20N_T3L_N3_AD1N_64	Bank64	1.2V,1.35V,1.5V,1.8V
J11	BE33	IO_L20P_T3L_N2_AD1P_64	Bank64	1.2V,1.35V,1.5V,1.8V
J15	BF31	IO_L21N_T3L_N5_AD8N_64	Bank64	1.2V,1.35V,1.5V,1.8V
J14	BF32	IO_L21P_T3L_N4_AD8P_64	Bank64	1.2V,1.35V,1.5V,1.8V
J18	BG33	IO_L22N_T3U_N7_DBC_AD0N_64	Bank64	1.2V,1.35V,1.5V,1.8V
J17	BG34	IO_L22P_T3U_N6_DBC_AD0P_64	Bank64	1.2V,1.35V,1.5V,1.8V
K11	BE29	IO_L23N_T3U_N9_64	Bank64	1.2V,1.35V,1.5V,1.8V
K10	BE30	IO_L23P_T3U_N8_64	Bank64	1.2V,1.35V,1.5V,1.8V
K14	BF34	IO_L24N_T3U_N11_64	Bank64	1.2V,1.35V,1.5V,1.8V
K13	BE34	IO_L24P_T3U_N10_64	Bank64	1.2V,1.35V,1.5V,1.8V
C27	BJ36	IO_L1N_T0L_N1_DBC_66	Bank66	1.2V,1.35V,1.5V,1.8V
C26	BJ35	IO_L1P_T0L_N0_DBC_66	Bank66	1.2V,1.35V,1.5V,1.8V
C30	BF36	IO_L2N_T0L_N3_66	Bank66	1.2V,1.35V,1.5V,1.8V
C29	BF35	IO_L2P_T0L_N2_66	Bank66	1.2V,1.35V,1.5V,1.8V
D25	BF37	IO_L3N_T0L_N5_AD15N_66	Bank66	1.2V,1.35V,1.5V,1.8V

J7 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
D24	BE37	IO_L3P_T0L_N4_AD15P_66	Bank66	1.2V,1.35V,1.5V,1.8V
D28	BG37	IO_L4N_T0U_N7_DBC_AD7N_66	Bank66	1.2V,1.35V,1.5V,1.8V
D27	BG36	IO_L4P_T0U_N6_DBC_AD7P_66	Bank66	1.2V,1.35V,1.5V,1.8V
E21	BH38	IO_L5N_T0U_N9_AD14N_66	Bank66	1.2V,1.35V,1.5V,1.8V
E20	BG38	IO_L5P_T0U_N8_AD14P_66	Bank66	1.2V,1.35V,1.5V,1.8V
E24	BH36	IO_L6N_T0U_N11_AD6N_66	Bank66	1.2V,1.35V,1.5V,1.8V
E23	BH35	IO_L6P_T0U_N10_AD6P_66	Bank66	1.2V,1.35V,1.5V,1.8V
E27	BL35	IO_L7N_T1L_N1_QBC_AD13N_66	Bank66	1.2V,1.35V,1.5V,1.8V
E26	BK35	IO_L7P_T1L_N0_QBC_AD13P_66	Bank66	1.2V,1.35V,1.5V,1.8V
E30	BP36	IO_L8N_T1L_N3_AD5N_66	Bank66	1.2V,1.35V,1.5V,1.8V
E29	BP35	IO_L8P_T1L_N2_AD5P_66	Bank66	1.2V,1.35V,1.5V,1.8V
F20	BN36	IO_L9N_T1L_N5_AD12N_66	Bank66	1.2V,1.35V,1.5V,1.8V
F19	BN35	IO_L9P_T1L_N4_AD12P_66	Bank66	1.2V,1.35V,1.5V,1.8V
F23	BP38	IO_L10N_T1U_N7_QBC_AD4N_66	Bank66	1.2V,1.35V,1.5V,1.8V
F22	BP37	IO_L10P_T1U_N6_QBC_AD4P_66	Bank66	1.2V,1.35V,1.5V,1.8V
F26	BM37	IO_L11N_T1U_N9_GC_66	Bank66	1.2V,1.35V,1.5V,1.8V
F25	BM36	IO_L11P_T1U_N8_GC_66	Bank66	1.2V,1.35V,1.5V,1.8V
F29	BL37	IO_L12N_T1U_N11_GC_66	Bank66	1.2V,1.35V,1.5V,1.8V
F28	BL36	IO_L12P_T1U_N10_GC_66	Bank66	1.2V,1.35V,1.5V,1.8V
G24	BM39	IO_L13N_T2L_N1_GC_QBC_66	Bank66	1.2V,1.35V,1.5V,1.8V
G23	BM38	IO_L13P_T2L_N0_GC_QBC_66	Bank66	1.2V,1.35V,1.5V,1.8V
G27	BL40	IO_L14N_T2L_N3_GC_66	Bank66	1.2V,1.35V,1.5V,1.8V
G26	BL39	IO_L14P_T2L_N2_GC_66	Bank66	1.2V,1.35V,1.5V,1.8V
G30	BN39	IO_L15N_T2L_N5_AD11N_66	Bank66	1.2V,1.35V,1.5V,1.8V
G29	BN38	IO_L15P_T2L_N4_AD11P_66	Bank66	1.2V,1.35V,1.5V,1.8V
H23	BP41	IO_L16N_T2U_N7_QBC_AD3N_66	Bank66	1.2V,1.35V,1.5V,1.8V
H22	BN41	IO_L16P_T2U_N6_QBC_AD3P_66	Bank66	1.2V,1.35V,1.5V,1.8V
H26	BP40	IO_L17N_T2U_N9_AD10N_66	Bank66	1.2V,1.35V,1.5V,1.8V
H25	BN40	IO_L17P_T2U_N8_AD10P_66	Bank66	1.2V,1.35V,1.5V,1.8V
H29	BM41	IO_L18N_T2U_N11_AD2N_66	Bank66	1.2V,1.35V,1.5V,1.8V
H28	BL41	IO_L18P_T2U_N10_AD2P_66	Bank66	1.2V,1.35V,1.5V,1.8V
J21	BJ38	IO_L19N_T3L_N1_DBC_AD9N_66	Bank66	1.2V,1.35V,1.5V,1.8V
J20	BJ37	IO_L19P_T3L_N0_DBC_AD9P_66	Bank66	1.2V,1.35V,1.5V,1.8V
J24	BK40	IO_L20N_T3L_N3_AD1N_66	Bank66	1.2V,1.35V,1.5V,1.8V
J23	BK39	IO_L20P_T3L_N2_AD1P_66	Bank66	1.2V,1.35V,1.5V,1.8V
J27	BH39	IO_L21N_T3L_N5_AD8N_66	Bank66	1.2V,1.35V,1.5V,1.8V
J26	BG39	IO_L21P_T3L_N4_AD8P_66	Bank66	1.2V,1.35V,1.5V,1.8V
J30	BJ41	IO_L22N_T3U_N7_DBC_AD0N_66	Bank66	1.2V,1.35V,1.5V,1.8V
J29	BJ40	IO_L22P_T3U_N6_DBC_AD0P_66	Bank66	1.2V,1.35V,1.5V,1.8V
K20	BF40	IO_L23N_T3U_N9_66	Bank66	1.2V,1.35V,1.5V,1.8V
K19	BF39	IO_L23P_T3U_N8_66	Bank66	1.2V,1.35V,1.5V,1.8V
K23	BE40	IO_L24N_T3U_N11_66	Bank66	1.2V,1.35V,1.5V,1.8V
K22	BE39	IO_L24P_T3U_N10_66	Bank66	1.2V,1.35V,1.5V,1.8V

Table 5-11 Prodigy Connector – J8

J8 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
A15	BH3	MGTYRXN0_225	Bank225	
A14	BH4	MGTYRXP0_225	Bank225	
A11	BG1	MGTYRXN1_225	Bank225	
A10	BG2	MGTYRXP1_225	Bank225	
A7	BF3	MGTYRXN2_225	Bank225	
A6	BF4	MGTYRXP2_225	Bank225	
A3	BE1	MGTYRXN3_225	Bank225	
A2	BE2	MGTYRXP3_225	Bank225	
B17	BK8	MGTYTXN0_225	Bank225	
B16	BK9	MGTYTXP0_225	Bank225	
B13	BJ6	MGTYTXN1_225	Bank225	
B12	BJ7	MGTYTXP1_225	Bank225	
B9	BH8	MGTYTXN2_225	Bank225	
B8	BH9	MGTYTXP2_225	Bank225	
B5	BG6	MGTYTXN3_225	Bank225	
B4	BG7	MGTYTXP3_225	Bank225	
A19	BJ10	MGTREFCLK0N_225	Bank225	
A18	BJ11	MGTREFCLK0P_225	Bank225	
B21	BG10	MGTREFCLK1N_225	Bank225	
B20	BG11	MGTREFCLK1P_225	Bank225	
C3	BV15	IO_L1N_T0L_N1_DBC_60	Bank60	1.2V,1.35V,1.5V,1.8V
C2	BV16	IO_L1P_T0L_N0_DBC_60	Bank60	1.2V,1.35V,1.5V,1.8V
C7	BV18	IO_L2N_T0L_N3_60	Bank60	1.2V,1.35V,1.5V,1.8V
C6	BU18	IO_L2P_T0L_N2_60	Bank60	1.2V,1.35V,1.5V,1.8V
C11	BV13	IO_L3N_T0L_N5_AD15N_60	Bank60	1.2V,1.35V,1.5V,1.8V
C10	BV14	IO_L3P_T0L_N4_AD15P_60	Bank60	1.2V,1.35V,1.5V,1.8V
D2	BU17	IO_L4N_T0U_N7_DBC_AD7N_60	Bank60	1.2V,1.35V,1.5V,1.8V
D1	BT17	IO_L4P_T0U_N6_DBC_AD7P_60	Bank60	1.2V,1.35V,1.5V,1.8V
D5	BU13	IO_L5N_T0U_N9_AD14N_60	Bank60	1.2V,1.35V,1.5V,1.8V
D4	BU14	IO_L5P_T0U_N8_AD14P_60	Bank60	1.2V,1.35V,1.5V,1.8V
D8	BU16	IO_L6N_T0U_N11_AD6N_60	Bank60	1.2V,1.35V,1.5V,1.8V
D7	BT16	IO_L6P_T0U_N10_AD6P_60	Bank60	1.2V,1.35V,1.5V,1.8V
E3	BR17	IO_L7N_T1L_N1_QBC_AD13N_60	Bank60	1.2V,1.35V,1.5V,1.8V
E2	BP17	IO_L7P_T1L_N0_QBC_AD13P_60	Bank60	1.2V,1.35V,1.5V,1.8V
E6	BP18	IO_L8N_T1L_N3_AD5N_60	Bank60	1.2V,1.35V,1.5V,1.8V
E5	BN18	IO_L8P_T1L_N2_AD5P_60	Bank60	1.2V,1.35V,1.5V,1.8V
E9	BT14	IO_L9N_T1L_N5_AD12N_60	Bank60	1.2V,1.35V,1.5V,1.8V
E8	BT15	IO_L9P_T1L_N4_AD12P_60	Bank60	1.2V,1.35V,1.5V,1.8V
F2	BR13	IO_L10N_T1U_N7_QBC_AD4N_60	Bank60	1.2V,1.35V,1.5V,1.8V
F1	BP13	IO_L10P_T1U_N6_QBC_AD4P_60	Bank60	1.2V,1.35V,1.5V,1.8V
F5	BR14	IO_L11N_T1U_N9_GC_60	Bank60	1.2V,1.35V,1.5V,1.8V

J8 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
F4	BR15	IO_L11P_T1U_N8_GC_60	Bank60	1.2V,1.35V,1.5V,1.8V
F8	BP15	IO_L12N_T1U_N11_GC_60	Bank60	1.2V,1.35V,1.5V,1.8V
F7	BP16	IO_L12P_T1U_N10_GC_60	Bank60	1.2V,1.35V,1.5V,1.8V
G3	BN15	IO_L13N_T2L_N1_GC_QBC_60	Bank60	1.2V,1.35V,1.5V,1.8V
G2	BN16	IO_L13P_T2L_N0_GC_QBC_60	Bank60	1.2V,1.35V,1.5V,1.8V
G6	BM16	IO_L14N_T2L_N3_GC_60	Bank60	1.2V,1.35V,1.5V,1.8V
G5	BL16	IO_L14P_T2L_N2_GC_60	Bank60	1.2V,1.35V,1.5V,1.8V
G9	BL14	IO_L15N_T2L_N5_AD11N_60	Bank60	1.2V,1.35V,1.5V,1.8V
G8	BL15	IO_L15P_T2L_N4_AD11P_60	Bank60	1.2V,1.35V,1.5V,1.8V
G12	BN13	IO_L16N_T2U_N7_QBC_AD3N_60	Bank60	1.2V,1.35V,1.5V,1.8V
G11	BN14	IO_L16P_T2U_N6_QBC_AD3P_60	Bank60	1.2V,1.35V,1.5V,1.8V
H2	BM17	IO_L17N_T2U_N9_AD10N_60	Bank60	1.2V,1.35V,1.5V,1.8V
H1	BL17	IO_L17P_T2U_N8_AD10P_60	Bank60	1.2V,1.35V,1.5V,1.8V
H5	BM13	IO_L18N_T2U_N11_AD2N_60	Bank60	1.2V,1.35V,1.5V,1.8V
H4	BM14	IO_L18P_T2U_N10_AD2P_60	Bank60	1.2V,1.35V,1.5V,1.8V
H8	BK17	IO_L19N_T3L_N1_DBC_AD9N_60	Bank60	1.2V,1.35V,1.5V,1.8V
H7	BJ17	IO_L19P_T3L_N0_DBC_AD9P_60	Bank60	1.2V,1.35V,1.5V,1.8V
J3	BJ18	IO_L20N_T3L_N3_AD1N_60	Bank60	1.2V,1.35V,1.5V,1.8V
J2	BH18	IO_L20P_T3L_N2_AD1P_60	Bank60	1.2V,1.35V,1.5V,1.8V
J6	BJ16	IO_L21N_T3L_N5_AD8N_60	Bank60	1.2V,1.35V,1.5V,1.8V
J5	BH16	IO_L21P_T3L_N4_AD8P_60	Bank60	1.2V,1.35V,1.5V,1.8V
J9	BJ15	IO_L22N_T3U_N7_DBC_AD0N_60	Bank60	1.2V,1.35V,1.5V,1.8V
J8	BH15	IO_L22P_T3U_N6_DBC_AD0P_60	Bank60	1.2V,1.35V,1.5V,1.8V
K2	BK14	IO_L23N_T3U_N9_60	Bank60	1.2V,1.35V,1.5V,1.8V
K1	BK15	IO_L23P_T3U_N8_60	Bank60	1.2V,1.35V,1.5V,1.8V
K5	BK13	IO_L24N_T3U_N11_60	Bank60	1.2V,1.35V,1.5V,1.8V
K4	BJ13	IO_L24P_T3U_N10_60	Bank60	1.2V,1.35V,1.5V,1.8V
C15	BU21	IO_L1N_T0L_N1_DBC_61	Bank61	1.2V,1.35V,1.5V,1.8V
C14	BT22	IO_L1P_T0L_N0_DBC_61	Bank61	1.2V,1.35V,1.5V,1.8V
C19	BP21	IO_L2N_T0L_N3_61	Bank61	1.2V,1.35V,1.5V,1.8V
C18	BP22	IO_L2P_T0L_N2_61	Bank61	1.2V,1.35V,1.5V,1.8V
C23	BT20	IO_L3N_T0L_N5_AD15N_61	Bank61	1.2V,1.35V,1.5V,1.8V
C22	BT21	IO_L3P_T0L_N4_AD15P_61	Bank61	1.2V,1.35V,1.5V,1.8V
D13	BU22	IO_L4N_T0U_N7_DBC_AD7N_61	Bank61	1.2V,1.35V,1.5V,1.8V
D12	BU23	IO_L4P_T0U_N6_DBC_AD7P_61	Bank61	1.2V,1.35V,1.5V,1.8V
D17	BR19	IO_L5N_T0U_N9_AD14N_61	Bank61	1.2V,1.35V,1.5V,1.8V
D16	BR20	IO_L5P_T0U_N8_AD14P_61	Bank61	1.2V,1.35V,1.5V,1.8V
D20	BR22	IO_L6N_T0U_N11_AD6N_61	Bank61	1.2V,1.35V,1.5V,1.8V
D19	BR23	IO_L6P_T0U_N10_AD6P_61	Bank61	1.2V,1.35V,1.5V,1.8V
E12	BN19	IO_L7N_T1L_N1_QBC_AD13N_61	Bank61	1.2V,1.35V,1.5V,1.8V
E11	BM19	IO_L7P_T1L_N0_QBC_AD13P_61	Bank61	1.2V,1.35V,1.5V,1.8V
E15	BP23	IO_L8N_T1L_N3_AD5N_61	Bank61	1.2V,1.35V,1.5V,1.8V
E14	BN23	IO_L8P_T1L_N2_AD5P_61	Bank61	1.2V,1.35V,1.5V,1.8V

J8 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
E18	BL19	IO_L9N_T1L_N5_AD12N_61	Bank61	1.2V,1.35V,1.5V,1.8V
E17	BL20	IO_L9P_T1L_N4_AD12P_61	Bank61	1.2V,1.35V,1.5V,1.8V
F11	BN20	IO_L10N_T1U_N7_QBC_AD4N_61	Bank61	1.2V,1.35V,1.5V,1.8V
F10	BN21	IO_L10P_T1U_N6_QBC_AD4P_61	Bank61	1.2V,1.35V,1.5V,1.8V
F14	BM22	IO_L11N_T1U_N9_GC_61	Bank61	1.2V,1.35V,1.5V,1.8V
F13	BL22	IO_L11P_T1U_N8_GC_61	Bank61	1.2V,1.35V,1.5V,1.8V
F17	BM21	IO_L12N_T1U_N11_GC_61	Bank61	1.2V,1.35V,1.5V,1.8V
F16	BL21	IO_L12P_T1U_N10_GC_61	Bank61	1.2V,1.35V,1.5V,1.8V
G15	BJ21	IO_L13N_T2L_N1_GC_QBC_61	Bank61	1.2V,1.35V,1.5V,1.8V
G14	BH21	IO_L13P_T2L_N0_GC_QBC_61	Bank61	1.2V,1.35V,1.5V,1.8V
G18	BK22	IO_L14N_T2L_N3_GC_61	Bank61	1.2V,1.35V,1.5V,1.8V
G17	BJ22	IO_L14P_T2L_N2_GC_61	Bank61	1.2V,1.35V,1.5V,1.8V
G21	BJ23	IO_L15N_T2L_N5_AD11N_61	Bank61	1.2V,1.35V,1.5V,1.8V
G20	BH23	IO_L15P_T2L_N4_AD11P_61	Bank61	1.2V,1.35V,1.5V,1.8V
H11	BK23	IO_L16N_T2U_N7_QBC_AD3N_61	Bank61	1.2V,1.35V,1.5V,1.8V
H10	BK24	IO_L16P_T2U_N6_QBC_AD3P_61	Bank61	1.2V,1.35V,1.5V,1.8V
H14	BH19	IO_L17N_T2U_N9_AD10N_61	Bank61	1.2V,1.35V,1.5V,1.8V
H13	BH20	IO_L17P_T2U_N8_AD10P_61	Bank61	1.2V,1.35V,1.5V,1.8V
H17	BK19	IO_L18N_T2U_N11_AD2N_61	Bank61	1.2V,1.35V,1.5V,1.8V
H16	BK20	IO_L18P_T2U_N10_AD2P_61	Bank61	1.2V,1.35V,1.5V,1.8V
H20	BE22	IO_L19N_T3L_N1_DBC_AD9N_61	Bank61	1.2V,1.35V,1.5V,1.8V
H19	BE23	IO_L19P_T3L_N0_DBC_AD9P_61	Bank61	1.2V,1.35V,1.5V,1.8V
J12	BG21	IO_L20N_T3L_N3_AD1N_61	Bank61	1.2V,1.35V,1.5V,1.8V
J11	BG22	IO_L20P_T3L_N2_AD1P_61	Bank61	1.2V,1.35V,1.5V,1.8V
J15	BH24	IO_L21N_T3L_N5_AD8N_61	Bank61	1.2V,1.35V,1.5V,1.8V
J14	BG24	IO_L21P_T3L_N4_AD8P_61	Bank61	1.2V,1.35V,1.5V,1.8V
J18	BF20	IO_L22N_T3U_N7_DBC_AD0N_61	Bank61	1.2V,1.35V,1.5V,1.8V
J17	BE20	IO_L22P_T3U_N6_DBC_AD0P_61	Bank61	1.2V,1.35V,1.5V,1.8V
K11	BF24	IO_L23N_T3U_N9_61	Bank61	1.2V,1.35V,1.5V,1.8V
K10	BE24	IO_L23P_T3U_N8_61	Bank61	1.2V,1.35V,1.5V,1.8V
K14	BF21	IO_L24N_T3U_N11_61	Bank61	1.2V,1.35V,1.5V,1.8V
K13	BF22	IO_L24P_T3U_N10_61	Bank61	1.2V,1.35V,1.5V,1.8V
C27	BU24	IO_L1N_T0L_N1_DBC_62	Bank62	1.2V,1.35V,1.5V,1.8V
C26	BT24	IO_L1P_T0L_N0_DBC_62	Bank62	1.2V,1.35V,1.5V,1.8V
C30	BT29	IO_L2N_T0L_N3_62	Bank62	1.2V,1.35V,1.5V,1.8V
C29	BR29	IO_L2P_T0L_N2_62	Bank62	1.2V,1.35V,1.5V,1.8V
D25	BT25	IO_L3N_T0L_N5_AD15N_62	Bank62	1.2V,1.35V,1.5V,1.8V
D24	BT26	IO_L3P_T0L_N4_AD15P_62	Bank62	1.2V,1.35V,1.5V,1.8V
D28	BU26	IO_L4N_T0U_N7_DBC_AD7N_62	Bank62	1.2V,1.35V,1.5V,1.8V
D27	BT27	IO_L4P_T0U_N6_DBC_AD7P_62	Bank62	1.2V,1.35V,1.5V,1.8V
E21	BR24	IO_L5N_T0U_N9_AD14N_62	Bank62	1.2V,1.35V,1.5V,1.8V
E20	BR25	IO_L5P_T0U_N8_AD14P_62	Bank62	1.2V,1.35V,1.5V,1.8V
E24	BR27	IO_L6N_T0U_N11_AD6N_62	Bank62	1.2V,1.35V,1.5V,1.8V

J8 Pin No.	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
E23	BR28	IO_L6P_T0U_N10_AD6P_62	Bank62	1.2V,1.35V,1.5V,1.8V
E27	BN24	IO_L7N_T1L_N1_QBC_AD13N_62	Bank62	1.2V,1.35V,1.5V,1.8V
E26	BM24	IO_L7P_T1L_N0_QBC_AD13P_62	Bank62	1.2V,1.35V,1.5V,1.8V
E30	BN28	IO_L8N_T1L_N3_AD5N_62	Bank62	1.2V,1.35V,1.5V,1.8V
E29	BM28	IO_L8P_T1L_N2_AD5P_62	Bank62	1.2V,1.35V,1.5V,1.8V
F20	BP25	IO_L9N_T1L_N5_AD12N_62	Bank62	1.2V,1.35V,1.5V,1.8V
F19	BN25	IO_L9P_T1L_N4_AD12P_62	Bank62	1.2V,1.35V,1.5V,1.8V
F23	BN29	IO_L10N_T1U_N7_QBC_AD4N_62	Bank62	1.2V,1.35V,1.5V,1.8V
F22	BM29	IO_L10P_T1U_N6_QBC_AD4P_62	Bank62	1.2V,1.35V,1.5V,1.8V
F26	BM26	IO_L11N_T1U_N9_GC_62	Bank62	1.2V,1.35V,1.5V,1.8V
F25	BM27	IO_L11P_T1U_N8_GC_62	Bank62	1.2V,1.35V,1.5V,1.8V
F29	BP26	IO_L12N_T1U_N11_GC_62	Bank62	1.2V,1.35V,1.5V,1.8V
F28	BN26	IO_L12P_T1U_N10_GC_62	Bank62	1.2V,1.35V,1.5V,1.8V
G24	BK27	IO_L13N_T2L_N1_GC_QBC_62	Bank62	1.2V,1.35V,1.5V,1.8V
G23	BJ27	IO_L13P_T2L_N0_GC_QBC_62	Bank62	1.2V,1.35V,1.5V,1.8V
G27	BL26	IO_L14N_T2L_N3_GC_62	Bank62	1.2V,1.35V,1.5V,1.8V
G26	BL27	IO_L14P_T2L_N2_GC_62	Bank62	1.2V,1.35V,1.5V,1.8V
G30	BJ25	IO_L15N_T2L_N5_AD11N_62	Bank62	1.2V,1.35V,1.5V,1.8V
G29	BJ26	IO_L15P_T2L_N4_AD11P_62	Bank62	1.2V,1.35V,1.5V,1.8V
H23	BL25	IO_L16N_T2U_N7_QBC_AD3N_62	Bank62	1.2V,1.35V,1.5V,1.8V
H22	BK25	IO_L16P_T2U_N6_QBC_AD3P_62	Bank62	1.2V,1.35V,1.5V,1.8V
H26	BK28	IO_L17N_T2U_N9_AD10N_62	Bank62	1.2V,1.35V,1.5V,1.8V
H25	BJ28	IO_L17P_T2U_N8_AD10P_62	Bank62	1.2V,1.35V,1.5V,1.8V
H29	BL29	IO_L18N_T2U_N11_AD2N_62	Bank62	1.2V,1.35V,1.5V,1.8V
H28	BK29	IO_L18P_T2U_N10_AD2P_62	Bank62	1.2V,1.35V,1.5V,1.8V
J21	BG27	IO_L19N_T3L_N1_DBC_AD9N_62	Bank62	1.2V,1.35V,1.5V,1.8V
J20	BF27	IO_L19P_T3L_N0_DBC_AD9P_62	Bank62	1.2V,1.35V,1.5V,1.8V
J24	BH25	IO_L20N_T3L_N3_AD1N_62	Bank62	1.2V,1.35V,1.5V,1.8V
J23	BH26	IO_L20P_T3L_N2_AD1P_62	Bank62	1.2V,1.35V,1.5V,1.8V
J27	BE27	IO_L21N_T3L_N5_AD8N_62	Bank62	1.2V,1.35V,1.5V,1.8V
J26	BE28	IO_L21P_T3L_N4_AD8P_62	Bank62	1.2V,1.35V,1.5V,1.8V
J30	BG26	IO_L22N_T3U_N7_DBC_AD0N_62	Bank62	1.2V,1.35V,1.5V,1.8V
J29	BF26	IO_L22P_T3U_N6_DBC_AD0P_62	Bank62	1.2V,1.35V,1.5V,1.8V
K20	BF25	IO_L23N_T3U_N9_62	Bank62	1.2V,1.35V,1.5V,1.8V
K19	BE25	IO_L23P_T3U_N8_62	Bank62	1.2V,1.35V,1.5V,1.8V
K23	BG29	IO_L24N_T3U_N11_62	Bank62	1.2V,1.35V,1.5V,1.8V
K22	BF29	IO_L24P_T3U_N10_62	Bank62	1.2V,1.35V,1.5V,1.8V

5.4 DDR4 SODIMM I/O

There are two DDR4 SO-DIMM J11 and J12 on FPGA Module VU19P which are used to plug DDR4 memory modules into the SO-DIMM socket. It supports up to 72bit with ECC

16GB capacity DDR4 SO-DIMM memory module. Pin connections and functions are described in Table 5-14 and Table 5-15.

Figure 5-3 Two on-board vertical DDR4-SODIMM

Note: For the details of the physical size of two on-board vertical DDR4-SODIMM, please refer to the 3D drawing file from S2C FAE for technique support.

Table 5-12 DDR4 SODIMM – J11

J11 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
144	P1_DDR4_A0	AC46	IO_L24N_T3U_N11_32	Bank32	1.2V
133	P1_DDR4_A1	Y47	IO_L23N_T3U_N9_32	Bank32	1.2V
132	P1_DDR4_A2	Y45	IO_L22N_T3U_N7_DBC_AD0N_32	Bank32	1.2V
131	P1_DDR4_A3	AA46	IO_L20N_T3L_N3_AD1N_32	Bank32	1.2V
128	P1_DDR4_A4	W53	IO_L11N_T1U_N9_GC_32	Bank32	1.2V
126	P1_DDR4_A5	W52	IO_L11P_T1U_N8_GC_32	Bank32	1.2V
127	P1_DDR4_A6	Y49	IO_L16P_T2U_N6_QBC_AD3P_32	Bank32	1.2V
122	P1_DDR4_A7	AA49	IO_L18N_T2U_N11_AD2N_32	Bank32	1.2V
125	P1_DDR4_A8	Y50	IO_L16N_T2U_N7_QBC_AD3N_32	Bank32	1.2V
121	P1_DDR4_A9	AA47	IO_L23P_T3U_N8_32	Bank32	1.2V
146	P1_DDR4_A10	AC48	IO_L19P_T3L_N0_DBC_AD9P_32	Bank32	1.2V
120	P1_DDR4_A11	AA45	IO_L22P_T3U_N6_DBC_AD0P_32	Bank32	1.2V
119	P1_DDR4_A12	V51	IO_L17N_T2U_N9_AD10N_32	Bank32	1.2V
158	P1_DDR4_A13	AC51	IO_L15N_T2L_N5_AD11N_32	Bank32	1.2V
151	P1_DDR4_WE_N_A14	AB46	IO_L20P_T3L_N2_AD1P_32	Bank32	1.2V
156	P1_DDR4_CAS_N_A15	AC49	IO_L19N_T3L_N1_DBC_AD9N_32	Bank32	1.2V
152	P1_DDR4_RAS_N_A16	AC50	IO_L15P_T2L_N4_AD11P_32	Bank32	1.2V
114	P1_DDR4_ACT_N	AB49	IO_L18P_T2U_N10_AD2P_32	Bank32	1.2V
116	P1_DDR4_ALERT_N	AB48	IO_L21N_T3L_N5_AD8N_32	Bank32	1.2V
150	P1_DDR4_BA0	AB47	IO_L21P_T3L_N4_AD8P_32	Bank32	1.2V
145	P1_DDR4_BA1	Y54	IO_L7P_T1L_N0_QBC_AD13P_32	Bank32	1.2V
115	P1_DDR4_BG0	W51	IO_L17P_T2U_N8_AD10P_32	Bank32	1.2V

J11 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
113	P1_DDR4_BG1	W55	IO_L9P_T1L_N4_AD12P_32	Bank32	1.2V
139	P1_DDR4_CK0_C	AB52	IO_L13N_T2L_N1_GC_QBC_32	Bank32	1.2V
137	P1_DDR4_CK0_T	AB51	IO_L13P_T2L_N0_GC_QBC_32	Bank32	1.2V
140	P1_DDR4_CK1_C	AA52	IO_L14N_T2L_N3_GC_32	Bank32	1.2V
138	P1_DDR4_CK1_T	AA51	IO_L14P_T2L_N2_GC_32	Bank32	1.2V
109	P1_DDR4_CKE0	V53	IO_L10P_T1U_N6_QBC_AD4P_32	Bank32	1.2V
110	P1_DDR4_CKE1	AC45	IO_L24P_T3U_N10_32	Bank32	1.2V
149	P1_DDR4_CS0_N	W56	IO_L9N_T1L_N5_AD12N_32	Bank32	1.2V
157	P1_DDR4_CS1_N	V54	IO_L10N_T1U_N7_QBC_AD4N_32	Bank32	1.2V
8	P1_DDR4_DQ0	AG59	IO_L3N_T0L_N5_AD15N_31	Bank31	1.2V
7	P1_DDR4_DQ1	AF62	IO_L6P_T0U_N10_AD6P_31	Bank31	1.2V
20	P1_DDR4_DQ2	AG61	IO_L2P_T0L_N2_31	Bank31	1.2V
21	P1_DDR4_DQ3	AF59	IO_L5P_T0U_N8_AD14P_31	Bank31	1.2V
4	P1_DDR4_DQ4	AG58	IO_L3P_T0L_N4_AD15P_31	Bank31	1.2V
3	P1_DDR4_DQ5	AF61	IO_L2N_T0L_N3_31	Bank31	1.2V
16	P1_DDR4_DQ6	AF60	IO_L5N_T0U_N9_AD14N_31	Bank31	1.2V
17	P1_DDR4_DQ7	AE62	IO_L6N_T0U_N11_AD6N_31	Bank31	1.2V
12	P1_DDR4_DM0	AH58	IO_L1P_T0L_N0_DBC_31	Bank31	1.2V
11	P1_DDR4_DQS0_C	AG63	IO_L4N_T0U_N7_DBC_AD7N_31	Bank31	1.2V
13	P1_DDR4_DQS0_T	AG62	IO_L4P_T0U_N6_DBC_AD7P_31	Bank31	1.2V
28	P1_DDR4_DQ8	AC55	IO_L3P_T0L_N4_AD15P_32	Bank32	1.2V
29	P1_DDR4_DQ9	AB53	IO_L5P_T0U_N8_AD14P_32	Bank32	1.2V
41	P1_DDR4_DQ10	AA57	IO_L6N_T0U_N11_AD6N_32	Bank32	1.2V
42	P1_DDR4_DQ11	AB56	IO_L2P_T0L_N2_32	Bank32	1.2V
24	P1_DDR4_DQ12	AB54	IO_L5N_T0U_N9_AD14N_32	Bank32	1.2V
25	P1_DDR4_DQ13	AA56	IO_L6P_T0U_N10_AD6P_32	Bank32	1.2V
38	P1_DDR4_DQ14	AC56	IO_L3N_T0L_N5_AD15N_32	Bank32	1.2V
37	P1_DDR4_DQ15	AB57	IO_L2N_T0L_N3_32	Bank32	1.2V
33	P1_DDR4_DM1	AC53	IO_L1P_T0L_N0_DBC_32	Bank32	1.2V
32	P1_DDR4_DQS1_C	AA55	IO_L4N_T0U_N7_DBC_AD7N_32	Bank32	1.2V
34	P1_DDR4_DQS1_T	AA54	IO_L4P_T0U_N6_DBC_AD7P_32	Bank32	1.2V
50	P1_DDR4_DQ16	AB59	IO_L15N_T2L_N5_AD11N_31	Bank31	1.2V
49	P1_DDR4_DQ17	AA59	IO_L17P_T2U_N8_AD10P_31	Bank31	1.2V
62	P1_DDR4_DQ18	AA62	IO_L14N_T2L_N3_GC_31	Bank31	1.2V
63	P1_DDR4_DQ19	Y62	IO_L18P_T2U_N10_AD2P_31	Bank31	1.2V
46	P1_DDR4_DQ20	AA60	IO_L17N_T2U_N9_AD10N_31	Bank31	1.2V
45	P1_DDR4_DQ21	AB58	IO_L15P_T2L_N4_AD11P_31	Bank31	1.2V
58	P1_DDR4_DQ22	AA61	IO_L14P_T2L_N2_GC_31	Bank31	1.2V
59	P1_DDR4_DQ23	Y63	IO_L18N_T2U_N11_AD2N_31	Bank31	1.2V
54	P1_DDR4_DM2	AB61	IO_L13P_T2L_N0_GC_QBC_31	Bank31	1.2V
53	P1_DDR4_DQS2_C	Y60	IO_L16N_T2U_N7_QBC_AD3N_31	Bank31	1.2V
55	P1_DDR4_DQS2_T	Y59	IO_L16P_T2U_N6_QBC_AD3P_31	Bank31	1.2V
70	P1_DDR4_DQ24	T57	IO_L9N_T1L_N5_AD12N_33	Bank33	1.2V
71	P1_DDR4_DQ25	R55	IO_L12N_T1U_N11_GC_33	Bank33	1.2V

J11 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
83	P1_DDR4_DQ26	P55	IO_L11P_T1U_N8_GC_33	Bank33	1.2V
84	P1_DDR4_DQ27	R58	IO_L8N_T1L_N3_AD5N_33	Bank33	1.2V
66	P1_DDR4_DQ28	T56	IO_L9P_T1L_N4_AD12P_33	Bank33	1.2V
67	P1_DDR4_DQ29	P56	IO_L11N_T1U_N9_GC_33	Bank33	1.2V
79	P1_DDR4_DQ30	R54	IO_L12P_T1U_N10_GC_33	Bank33	1.2V
80	P1_DDR4_DQ31	R57	IO_L8P_T1L_N2_AD5P_33	Bank33	1.2V
75	P1_DDR4_DM3	U56	IO_L7P_T1L_N0_QBC_AD13P_33	Bank33	1.2V
74	P1_DDR4_DQS3_C	T55	IO_L10N_T1U_N7_QBC_AD4N_33	Bank33	1.2V
76	P1_DDR4_DQS3_T	T54	IO_L10P_T1U_N6_QBC_AD4P_33	Bank33	1.2V
174	P1_DDR4_DQ32	U63	IO_L23N_T3U_N9_31	Bank31	1.2V
173	P1_DDR4_DQ33	W62	IO_L21P_T3L_N4_AD8P_31	Bank31	1.2V
187	P1_DDR4_DQ34	W63	IO_L21N_T3L_N5_AD8N_31	Bank31	1.2V
186	P1_DDR4_DQ35	V59	IO_L20N_T3L_N3_AD1N_31	Bank31	1.2V
170	P1_DDR4_DQ36	V63	IO_L23P_T3U_N8_31	Bank31	1.2V
169	P1_DDR4_DQ37	V58	IO_L20P_T3L_N2_AD1P_31	Bank31	1.2V
183	P1_DDR4_DQ38	U61	IO_L24P_T3U_N10_31	Bank31	1.2V
182	P1_DDR4_DQ39	U62	IO_L24N_T3U_N11_31	Bank31	1.2V
178	P1_DDR4_DM4	W60	IO_L19P_T3L_N0_DBC_AD9P_31	Bank31	1.2V
177	P1_DDR4_DQS4_C	V61	IO_L22N_T3U_N7_DBC_AD0N_31	Bank31	1.2V
179	P1_DDR4_DQS4_T	V60	IO_L22P_T3U_N6_DBC_AD0P_31	Bank31	1.2V
195	P1_DDR4_DQ40	N56	IO_L6N_T0U_N11_AD6N_33	Bank33	1.2V
194	P1_DDR4_DQ41	N58	IO_L3P_T0L_N4_AD15P_33	Bank33	1.2V
207	P1_DDR4_DQ42	K57	IO_L2P_T0L_N2_33	Bank33	1.2V
208	P1_DDR4_DQ43	L57	IO_L5N_T0U_N9_AD14N_33	Bank33	1.2V
191	P1_DDR4_DQ44	M57	IO_L5P_T0U_N8_AD14P_33	Bank33	1.2V
190	P1_DDR4_DQ45	M58	IO_L3N_T0L_N5_AD15N_33	Bank33	1.2V
203	P1_DDR4_DQ46	N55	IO_L6P_T0U_N10_AD6P_33	Bank33	1.2V
204	P1_DDR4_DQ47	K58	IO_L2N_T0L_N3_33	Bank33	1.2V
199	P1_DDR4_DM5	P57	IO_L1P_T0L_N0_DBC_33	Bank33	1.2V
198	P1_DDR4_DQS5_C	L56	IO_L4N_T0U_N7_DBC_AD7N_33	Bank33	1.2V
200	P1_DDR4_DQS5_T	M56	IO_L4P_T0U_N6_DBC_AD7P_33	Bank33	1.2V
216	P1_DDR4_DQ48	K54	IO_L24N_T3U_N11_33	Bank33	1.2V
215	P1_DDR4_DQ49	J52	IO_L20N_T3L_N3_AD1N_33	Bank33	1.2V
228	P1_DDR4_DQ50	J51	IO_L20P_T3L_N2_AD1P_33	Bank33	1.2V
229	P1_DDR4_DQ51	M51	IO_L21P_T3L_N4_AD8P_33	Bank33	1.2V
211	P1_DDR4_DQ52	M52	IO_L21N_T3L_N5_AD8N_33	Bank33	1.2V
212	P1_DDR4_DQ53	L54	IO_L24P_T3U_N10_33	Bank33	1.2V
224	P1_DDR4_DQ54	L52	IO_L23N_T3U_N9_33	Bank33	1.2V
225	P1_DDR4_DQ55	L51	IO_L23P_T3U_N8_33	Bank33	1.2V
220	P1_DDR4_DM6	M53	IO_L19P_T3L_N0_DBC_AD9P_33	Bank33	1.2V
219	P1_DDR4_DQS6_C	K53	IO_L22N_T3U_N7_DBC_AD0N_33	Bank33	1.2V
221	P1_DDR4_DQS6_T	K52	IO_L22P_T3U_N6_DBC_AD0P_33	Bank33	1.2V
237	P1_DDR4_DQ56	P52	IO_L14P_T2L_N2_GC_33	Bank33	1.2V
236	P1_DDR4_DQ57	T51	IO_L17P_T2U_N8_AD10P_33	Bank33	1.2V

J11 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
249	P1_DDR4_DQ58	U53	IO_L15N_T2L_N5_AD11N_33	Bank33	1.2V
250	P1_DDR4_DQ59	U52	IO_L15P_T2L_N4_AD11P_33	Bank33	1.2V
232	P1_DDR4_DQ60	P51	IO_L18P_T2U_N10_AD2P_33	Bank33	1.2V
233	P1_DDR4_DQ61	P53	IO_L14N_T2L_N3_GC_33	Bank33	1.2V
245	P1_DDR4_DQ62	N51	IO_L18N_T2U_N11_AD2N_33	Bank33	1.2V
246	P1_DDR4_DQ63	T52	IO_L17N_T2U_N9_AD10N_33	Bank33	1.2V
241	P1_DDR4_DM7	R52	IO_L13P_T2L_N0_GC_QBC_33	Bank33	1.2V
240	P1_DDR4_DQS7_C	N54	IO_L16N_T2U_N7_QBC_AD3N_33	Bank33	1.2V
242	P1_DDR4_DQS7_T	N53	IO_L16P_T2U_N6_QBC_AD3P_33	Bank33	1.2V
92	P1_DDR4_DQ64	AD61	IO_L11N_T1U_N9_GC_31	Bank31	1.2V
91	P1_DDR4_DQ65	AD62	IO_L8P_T1L_N2_AD5P_31	Bank31	1.2V
101	P1_DDR4_DQ66	AC59	IO_L9N_T1L_N5_AD12N_31	Bank31	1.2V
105	P1_DDR4_DQ67	AC58	IO_L9P_T1L_N4_AD12P_31	Bank31	1.2V
88	P1_DDR4_DQ68	AD60	IO_L11P_T1U_N8_GC_31	Bank31	1.2V
87	P1_DDR4_DQ69	AC60	IO_L12P_T1U_N10_GC_31	Bank31	1.2V
100	P1_DDR4_DQ70	AD63	IO_L8N_T1L_N3_AD5N_31	Bank31	1.2V
104	P1_DDR4_DQ71	AC61	IO_L12N_T1U_N11_GC_31	Bank31	1.2V
96	P1_DDR4_DM8	AE59	IO_L7P_T1L_N0_QBC_AD13P_31	Bank31	1.2V
95	P1_DDR4_DQS8_C	AB63	IO_L10N_T1U_N7_QBC_AD4N_31	Bank31	1.2V
97	P1_DDR4_DQS8_T	AC63	IO_L10P_T1U_N6_QBC_AD4P_31	Bank31	1.2V
134	P1_DDR4_EVENT_N	U58	IO_T1U_N12_33	Bank33	1.2V
155	P1_DDR4_ODT0	V56	IO_L8N_T1L_N3_AD5N_32	Bank32	1.2V
161	P1_DDR4_ODT1	V55	IO_L8P_T1L_N2_AD5P_32	Bank32	1.2V
143	P1_DDR4_PARITY	Y55	IO_L7N_T1L_N1_QBC_AD13N_32	Bank32	1.2V
108	P1_DDR4_RESET_N	Y48	IO_T3U_N12_32	Bank32	1.2V
253	P1_DDR4_SCL	K55	IO_T3U_N12_33	Bank33	1.2V
254	P1_DDR4_SDA	U54	IO_T2U_N12_33	Bank33	1.2V

Table 5-13 DDR4 SODIMM – J12

J12 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
144	P2_DDR4_A0	AV56	IO_L22P_T3U_N6_DBC_AD0P_26	Bank26	1.2V
133	P2_DDR4_A1	BA57	IO_L24N_T3U_N11_26	Bank26	1.2V
132	P2_DDR4_A2	AW58	IO_L20N_T3L_N3_AD1N_26	Bank26	1.2V
131	P2_DDR4_A3	BA56	IO_L19N_T3L_N1_DBC_AD9N_26	Bank26	1.2V
128	P2_DDR4_A4	AW56	IO_L22N_T3U_N7_DBC_AD0N_26	Bank26	1.2V
126	P2_DDR4_A5	AY57	IO_L24P_T3U_N10_26	Bank26	1.2V
127	P2_DDR4_A6	BB57	IO_L23N_T3U_N9_26	Bank26	1.2V
122	P2_DDR4_A7	AY55	IO_T3U_N12_26	Bank26	1.2V
125	P2_DDR4_A8	BB56	IO_L23P_T3U_N8_26	Bank26	1.2V
121	P2_DDR4_A9	BC56	IO_L21N_T3L_N5_AD8N_26	Bank26	1.2V
146	P2_DDR4_A10	AW57	IO_L20P_T3L_N2_AD1P_26	Bank26	1.2V
120	P2_DDR4_A11	BB54	IO_L17P_T2U_N8_AD10P_26	Bank26	1.2V

J12 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
119	P2_DDR4_A12	BC55	IO_L21P_T3L_N4_AD8P_26	Bank26	1.2V
158	P2_DDR4_A13	AW50	IO_L7P_T1L_N0_QBC_AD13P_26	Bank26	1.2V
151	P2_DDR4_WE_N_A14	AW52	IO_L18P_T2U_N10_AD2P_26	Bank26	1.2V
156	P2_DDR4_CAS_N_A15	AW51	IO_L7N_T1L_N1_QBC_AD13N_26	Bank26	1.2V
152	P2_DDR4_RAS_N_A16	BA51	IO_L11P_T1U_N8_GC_26	Bank26	1.2V
114	P2_DDR4_ACT_N	BC50	IO_L10P_T1U_N6_QBC_AD4P_26	Bank26	1.2V
116	P2_DDR4_ALERT_N	BB51	IO_L11N_T1U_N9_GC_26	Bank26	1.2V
150	P2_DDR4_BA0	BA49	IO_L8P_T1L_N2_AD5P_26	Bank26	1.2V
145	P2_DDR4_BA1	BA54	IO_L15N_T2L_N5_AD11N_26	Bank26	1.2V
115	P2_DDR4_BG0	BC53	IO_L16N_T2U_N7_QBC_AD3N_26	Bank26	1.2V
113	P2_DDR4_BG1	BC54	IO_L17N_T2U_N9_AD10N_26	Bank26	1.2V
139	P2_DDR4_CK0_C	BB52	IO_L13N_T2L_N1_GC_QBC_26	Bank26	1.2V
137	P2_DDR4_CK0_T	BA52	IO_L13P_T2L_N0_GC_QBC_26	Bank26	1.2V
140	P2_DDR4_CK1_C	AY53	IO_L14N_T2L_N3_GC_26	Bank26	1.2V
138	P2_DDR4_CK1_T	AY52	IO_L14P_T2L_N2_GC_26	Bank26	1.2V
109	P2_DDR4_CKE0	BB53	IO_L16P_T2U_N6_QBC_AD3P_26	Bank26	1.2V
110	P2_DDR4_CKE1	BC49	IO_L9N_T1L_N5_AD12N_26	Bank26	1.2V
149	P2_DDR4_CS0_N	BA55	IO_L19P_T3L_N0_DBC_AD9P_26	Bank26	1.2V
157	P2_DDR4_CS1_N	BC51	IO_L10N_T1U_N7_QBC_AD4N_26	Bank26	1.2V
8	P2_DDR4_DQ0	BE60	IO_L12P_T1U_N10_GC_25	Bank25	1.2V
7	P2_DDR4_DQ1	BF59	IO_L11N_T1U_N9_GC_25	Bank25	1.2V
20	P2_DDR4_DQ2	BE62	IO_L8N_T1L_N3_AD5N_25	Bank25	1.2V
21	P2_DDR4_DQ3	BD63	IO_L9P_T1L_N4_AD12P_25	Bank25	1.2V
4	P2_DDR4_DQ4	BF60	IO_L12N_T1U_N11_GC_25	Bank25	1.2V
3	P2_DDR4_DQ5	BE59	IO_L11P_T1U_N8_GC_25	Bank25	1.2V
16	P2_DDR4_DQ6	BE63	IO_L9N_T1L_N5_AD12N_25	Bank25	1.2V
17	P2_DDR4_DQ7	BD62	IO_L8P_T1L_N2_AD5P_25	Bank25	1.2V
12	P2_DDR4_DM0	BF61	IO_L7P_T1L_N0_QBC_AD13P_25	Bank25	1.2V
28	P2_DDR4_DQ8	BJ60	IO_L5N_T0U_N9_AD14N_25	Bank25	1.2V
29	P2_DDR4_DQ9	BJ63	IO_L6N_T0U_N11_AD6N_25	Bank25	1.2V
41	P2_DDR4_DQ10	BH61	IO_L2P_T0L_N2_25	Bank25	1.2V
42	P2_DDR4_DQ11	BJ61	IO_L2N_T0L_N3_25	Bank25	1.2V
24	P2_DDR4_DQ12	BH59	IO_L3N_T0L_N5_AD15N_25	Bank25	1.2V
25	P2_DDR4_DQ13	BG59	IO_L3P_T0L_N4_AD15P_25	Bank25	1.2V
38	P2_DDR4_DQ14	BJ62	IO_L6P_T0U_N10_AD6P_25	Bank25	1.2V
37	P2_DDR4_DQ15	BH60	IO_L5P_T0U_N8_AD14P_25	Bank25	1.2V
33	P2_DDR4_DM1	BG58	IO_L1P_T0L_N0_DBC_25	Bank25	1.2V
50	P2_DDR4_DQ16	BC59	IO_L17N_T2U_N9_AD10N_25	Bank25	1.2V
49	P2_DDR4_DQ17	BD60	IO_L14N_T2L_N3_GC_25	Bank25	1.2V
62	P2_DDR4_DQ18	BC63	IO_L15N_T2L_N5_AD11N_25	Bank25	1.2V
63	P2_DDR4_DQ19	BA62	IO_L18P_T2U_N10_AD2P_25	Bank25	1.2V
46	P2_DDR4_DQ20	BC58	IO_L17P_T2U_N8_AD10P_25	Bank25	1.2V
45	P2_DDR4_DQ21	BB63	IO_L15P_T2L_N4_AD11P_25	Bank25	1.2V

J12 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
58	P2_DDR4_DQ22	BC60	IO_L14P_T2L_N2_GC_25	Bank25	1.2V
59	P2_DDR4_DQ23	BB62	IO_L18N_T2U_N11_AD2N_25	Bank25	1.2V
54	P2_DDR4_DM2	BC61	IO_L13P_T2L_N0_GC_QBC_25	Bank25	1.2V
70	P2_DDR4_DQ24	AT52	IO_L11N_T1U_N9_GC_27	Bank27	1.2V
71	P2_DDR4_DQ25	AT51	IO_L11P_T1U_N8_GC_27	Bank27	1.2V
83	P2_DDR4_DQ26	AR52	IO_L12P_T1U_N10_GC_27	Bank27	1.2V
84	P2_DDR4_DQ27	AP53	IO_L8N_T1L_N3_AD5N_27	Bank27	1.2V
66	P2_DDR4_DQ28	AU52	IO_L9N_T1L_N5_AD12N_27	Bank27	1.2V
67	P2_DDR4_DQ29	AU51	IO_L9P_T1L_N4_AD12P_27	Bank27	1.2V
79	P2_DDR4_DQ30	AR53	IO_L12N_T1U_N11_GC_27	Bank27	1.2V
80	P2_DDR4_DQ31	AP52	IO_L8P_T1L_N2_AD5P_27	Bank27	1.2V
75	P2_DDR4_DM3	AU53	IO_L7P_T1L_N0_QBC_AD13P_27	Bank27	1.2V
174	P2_DDR4_DQ32	AW62	IO_L20P_T3L_N2_AD1P_25	Bank25	1.2V
173	P2_DDR4_DQ33	AY59	IO_L23P_T3U_N8_25	Bank25	1.2V
187	P2_DDR4_DQ34	AY60	IO_L21N_T3L_N5_AD8N_25	Bank25	1.2V
186	P2_DDR4_DQ35	AV63	IO_L24P_T3U_N10_25	Bank25	1.2V
170	P2_DDR4_DQ36	AY62	IO_L20N_T3L_N3_AD1N_25	Bank25	1.2V
169	P2_DDR4_DQ37	BA59	IO_L23N_T3U_N9_25	Bank25	1.2V
183	P2_DDR4_DQ38	AW60	IO_L21P_T3L_N4_AD8P_25	Bank25	1.2V
182	P2_DDR4_DQ39	AW63	IO_L24N_T3U_N11_25	Bank25	1.2V
178	P2_DDR4_DM4	BA60	IO_L19P_T3L_N0_DBC_AD9P_25	Bank25	1.2V
195	P2_DDR4_DQ40	AU46	IO_L21P_T3L_N4_AD8P_27	Bank27	1.2V
194	P2_DDR4_DQ41	AP46	IO_L24N_T3U_N11_27	Bank27	1.2V
207	P2_DDR4_DQ42	AT45	IO_L20N_T3L_N3_AD1N_27	Bank27	1.2V
208	P2_DDR4_DQ43	AT44	IO_L20P_T3L_N2_AD1P_27	Bank27	1.2V
191	P2_DDR4_DQ44	AU47	IO_L21N_T3L_N5_AD8N_27	Bank27	1.2V
190	P2_DDR4_DQ45	AP45	IO_L24P_T3U_N10_27	Bank27	1.2V
203	P2_DDR4_DQ46	AV45	IO_L23P_T3U_N8_27	Bank27	1.2V
204	P2_DDR4_DQ47	AV46	IO_L23N_T3U_N9_27	Bank27	1.2V
199	P2_DDR4_DM5	AR47	IO_L19P_T3L_N0_DBC_AD9P_27	Bank27	1.2V
216	P2_DDR4_DQ48	AP55	IO_L3P_T0L_N4_AD15P_27	Bank27	1.2V
215	P2_DDR4_DQ49	AU56	IO_L2P_T0L_N2_27	Bank27	1.2V
228	P2_DDR4_DQ50	AT54	IO_L6P_T0U_N10_AD6P_27	Bank27	1.2V
229	P2_DDR4_DQ51	AR54	IO_L5P_T0U_N8_AD14P_27	Bank27	1.2V
211	P2_DDR4_DQ52	AU57	IO_L2N_T0L_N3_27	Bank27	1.2V
212	P2_DDR4_DQ53	AR55	IO_L5N_T0U_N9_AD14N_27	Bank27	1.2V
224	P2_DDR4_DQ54	AT55	IO_L6N_T0U_N11_AD6N_27	Bank27	1.2V
225	P2_DDR4_DQ55	AP56	IO_L3N_T0L_N5_AD15N_27	Bank27	1.2V
220	P2_DDR4_DM6	AV54	IO_L1P_T0L_N0_DBC_27	Bank27	1.2V
237	P2_DDR4_DQ56	AW48	IO_L5P_T0U_N8_AD14P_26	Bank26	1.2V
236	P2_DDR4_DQ57	AW47	IO_L3N_T0L_N5_AD15N_26	Bank26	1.2V
249	P2_DDR4_DQ58	BB46	IO_L2N_T0L_N3_26	Bank26	1.2V
250	P2_DDR4_DQ59	BA46	IO_L2P_T0L_N2_26	Bank26	1.2V

J12 Pin No.	Net Name	FPGA Pin No.	FPGA Pin Description	FPGA Bank	IO Voltage
232	P2_DDR4_DQ60	AW46	IO_L3P_T0L_N4_AD15P_26	Bank26	1.2V
233	P2_DDR4_DQ61	AY48	IO_L5N_T0U_N9_AD14N_26	Bank26	1.2V
245	P2_DDR4_DQ62	AW45	IO_L6P_T0U_N10_AD6P_26	Bank26	1.2V
246	P2_DDR4_DQ63	AY45	IO_L6N_T0U_N11_AD6N_26	Bank26	1.2V
241	P2_DDR4_DM7	BB47	IO_L1P_T0L_N0_DBC_26	Bank26	1.2V
92	P2_DDR4_DQ64	AV51	IO_L15N_T2L_N5_AD11N_27	Bank27	1.2V
91	P2_DDR4_DQ65	AR49	IO_L14P_T2L_N2_GC_27	Bank27	1.2V
101	P2_DDR4_DQ66	AP47	IO_L18P_T2U_N10_AD2P_27	Bank27	1.2V
105	P2_DDR4_DQ67	AV49	IO_L17N_T2U_N9_AD10N_27	Bank27	1.2V
88	P2_DDR4_DQ68	AV50	IO_L15P_T2L_N4_AD11P_27	Bank27	1.2V
87	P2_DDR4_DQ69	AP48	IO_L18N_T2U_N11_AD2N_27	Bank27	1.2V
100	P2_DDR4_DQ70	AU49	IO_L17P_T2U_N8_AD10P_27	Bank27	1.2V
104	P2_DDR4_DQ71	AR50	IO_L14N_T2L_N3_GC_27	Bank27	1.2V
96	P2_DDR4_DM8	AT49	IO_L13P_T2L_N0_GC_QBC_27	Bank27	1.2V
11	P2_DDR4_DQS0_C	BE58	IO_L10N_T1U_N7_QBC_AD4N_25	Bank25	1.2V
13	P2_DDR4_DQS0_T	BD58	IO_L10P_T1U_N6_QBC_AD4P_25	Bank25	1.2V
32	P2_DDR4_DQS1_C	BG62	IO_L4N_T0U_N7_DBC_AD7N_25	Bank25	1.2V
34	P2_DDR4_DQS1_T	BG61	IO_L4P_T0U_N6_DBC_AD7P_25	Bank25	1.2V
53	P2_DDR4_DQS2_C	BB59	IO_L16N_T2U_N7_QBC_AD3N_25	Bank25	1.2V
55	P2_DDR4_DQS2_T	BB58	IO_L16P_T2U_N6_QBC_AD3P_25	Bank25	1.2V
74	P2_DDR4_DQS3_C	AP51	IO_L10N_T1U_N7_QBC_AD4N_27	Bank27	1.2V
76	P2_DDR4_DQS3_T	AP50	IO_L10P_T1U_N6_QBC_AD4P_27	Bank27	1.2V
177	P2_DDR4_DQS4_C	AW61	IO_L22N_T3U_N7_DBC_AD0N_25	Bank25	1.2V
179	P2_DDR4_DQS4_T	AV61	IO_L22P_T3U_N6_DBC_AD0P_25	Bank25	1.2V
198	P2_DDR4_DQS5_C	AR45	IO_L22N_T3U_N7_DBC_AD0N_27	Bank27	1.2V
200	P2_DDR4_DQS5_T	AR44	IO_L22P_T3U_N6_DBC_AD0P_27	Bank27	1.2V
219	P2_DDR4_DQS6_C	AT57	IO_L4N_T0U_N7_DBC_AD7N_27	Bank27	1.2V
221	P2_DDR4_DQS6_T	AT56	IO_L4P_T0U_N6_DBC_AD7P_27	Bank27	1.2V
240	P2_DDR4_DQS7_C	BA47	IO_L4N_T0U_N7_DBC_AD7N_26	Bank26	1.2V
242	P2_DDR4_DQS7_T	AY47	IO_L4P_T0U_N6_DBC_AD7P_26	Bank26	1.2V
95	P2_DDR4_DQS8_C	AV48	IO_L16N_T2U_N7_QBC_AD3N_27	Bank27	1.2V
97	P2_DDR4_DQS8_T	AU48	IO_L16P_T2U_N6_QBC_AD3P_27	Bank27	1.2V
134	P2_DDR4_EVENT_N	AU54	IO_T1U_N12_27	Bank27	1.2V
155	P2_DDR4_ODT0	AW53	IO_L18N_T2U_N11_AD2N_26	Bank26	1.2V
161	P2_DDR4_ODT1	BB49	IO_L8N_T1L_N3_AD5N_26	Bank26	1.2V
143	P2_DDR4_PARITY	AY54	IO_L15P_T2L_N4_AD11P_26	Bank26	1.2V
108	P2_DDR4_RESET_N	BC48	IO_L9P_T1L_N4_AD12P_26	Bank26	1.2V
253	P2_DDR4_SCL	AU44	IO_T3U_N12_27	Bank27	1.2V
254	P2_DDR4_SDA	AR48	IO_T2U_N12_27	Bank27	1.2V

5.5 Global Reset

Single VU19P Logic System provides two global resets from SC Clock Module Type D. The SC Clock Module Type D occupies one SC connector and should be mounted on PCM VU19PS to use as external clock input, external reset input and clock output.

SC Clock Module Type D provides:

5	Pairs of LVDS clock inputs on MMCX
1	Single-ended OSC socket
2	Reset inputs through MMCX
3	Pairs of LVDS clock outputs on MMCX

In addition to 2 MMCX resets on SC Clock Module Type D, the PCM VU19PS also provides three global resets from on board push buttons and two global resets from Player Pro runtime software as global reset source. All these reset sources are "AND" together.

Table 5-14 Global Reset Pin Out

Global Reset	Clock source	FPGA Pin No.	FPGA Bank	I/O Voltage
GRST1	P_JS1.4 or P_SW4 or PPro runtime	CA39	Bank65	1.8V
GRST2	P_JS1.8 or P_SW5 or PPro runtime	BY53	Bank21	1.8V
GRST3	P_SW6	E47	Bank37	1.8V

Note: All Global Resets are low active.

5.6 Micro SD Card Configuration Address Settings

Single VU19P Logic System provides 16 sets of Micro SD Card download configuration address. When user inserts the programmed Micro SD card into Micro SD card slot **P_J5 on** PCM VU19PS, it will automatically load FPGA image from one of the 16 SD Card configuration addresses into FPGA Module VU19P according to the Switch P_S3.1, P_S3.2, P_S3.3 and P_S3.4 settings on PCM VU19PS.

Note: Push button **P_SW3** reconfigures the FPGA through Micro SD card.

Table 5-15 Micro SD Card download settings

Switch				Configuration Address	Description
P_S3.4	P_S3.3	P_S3.2	P_S3.1		
ON	ON	ON	ON	Suit0	load FPGA image from Micro SD Card configuration Suit0
ON	ON	ON	OFF	Suit1	load FPGA image from Micro SD Card configuration Suit1
ON	ON	OFF	ON	Suit2	load FPGA image from Micro SD Card configuration Suit2

ON	ON	OFF	OFF	Suit3	load FPGA image from Micro SD Card configuration Suit3
ON	OFF	ON	ON	Suit4	load FPGA image from Micro SD Card configuration Suit4
ON	OFF	ON	OFF	Suit5	load FPGA image from Micro SD Card configuration Suit5
ON	OFF	OFF	ON	Suit6	load FPGA image from Micro SD Card configuration Suit6
ON	OFF	OFF	OFF	Suit7	load FPGA image from Micro SD Card configuration Suit7
OFF	ON	ON	ON	Suit8	load FPGA image from Micro SD Card configuration Suit8
OFF	ON	ON	OFF	Suit9	load FPGA image from Micro SD Card configuration Suit9
OFF	ON	OFF	ON	Suit10	load FPGA image from Micro SD Card configuration Suit10
OFF	ON	OFF	OFF	Suit11	load FPGA image from Micro SD Card configuration Suit11
OFF	OFF	ON	ON	Suit12	load FPGA image from Micro SD Card configuration Suit12
OFF	OFF	ON	OFF	Suit13	load FPGA image from Micro SD Card configuration Suit13
OFF	OFF	OFF	ON	Suit14	load FPGA image from Micro SD Card configuration Suit14
OFF	OFF	OFF	OFF	Suit15	load FPGA image from Micro SD Card configuration Suit15

Note: The default setting of P_S3.1, P_S3.2, P_S3.3 and P_S3.4 is "ON ON ON ON" which means load FPGA image from Micro SD Card configuration Suit0

5.7 User I/O

FPGA Module VU19P has user I/Os for user debugging that includes: 2x push buttons, 3x LEDs, 1x 4-position DIP Switch, and 8x GPIOs. Pin connections and functions are described in Table 5-16.

Table 5-16 User I/O

Net Name	FPGA Pin No.	FPGA Bank	User I/O Pin	I/O Voltage	Function
GPIO1	AC13	Bank93	**SW2**	3.3V	**Push button** (input signal) Push = L Normal = H
GPIO2	AC14	Bank93	**SW3**	3.3V	
GPIO3	U13	Bank98	**S2.1**	3.3V	**Toggle switch** (input signal) ON = L OFF = H
GPIO4	U14	Bank98	**S2.2**	3.3V	
GPIO5	V13	Bank98	**S2.3**	3.3V	
GPIO6	V14	Bank98	**S2.4**	3.3V	
GPIO7	AD15	Bank93	**LED35**	3.3V	**LED** (output signal) H = LED ON L = LED OFF
GPIO8	AD16	Bank93	**LED36**	3.3V	
GPIO9	AD17	Bank93	**LED37**	3.3V	
GPIO10	V16	Bank98	J16.1	3.3V	GPIO signals
GPIO11	W15	Bank98	J16.2	3.3V	
GPIO12	W16	Bank98	J16.3	3.3V	
GPIO13	Y14	Bank98	J16.4	3.3V	
GPIO14	Y15	Bank98	J16.6	3.3V	
GPIO15	AA14	Bank98	J16.7	3.3V	
GPIO16	AA15	Bank98	J16.8	3.3V	

Net Name	FPGA Pin No.	FPGA Bank	User I/O Pin	I/O Voltage	Function
GPIO17	AA16	Bank98	J16.9	3.3V	
GND			J16.5		
GND			J16.10	----	

5.8 Dedicated TDM Circuitry

Single VU19P has dedicated circuitry on FPGA Module VU19P for LVDS TDM. The push button SW1 is used as reset signal for LVDS TDM. The oscillator X1 fixed to 200MHz frequency on board is used as reference clock. The LED2 is used as TDM training successful indication.

Table 5-17 Dedicated TDM Circuitry

Net Name	FPGA Pin No.	FPGA Bank	Peripheral	I/O Voltage	Function
TDM_RESET	AC15	Bank98	SW1	3.3V	**Push button:** Push = L Normal = H
TDM_DONE	AC16	Bank98	LED2	3.3	**LED:** H = LED ON L = LED OFF
TDM_CLKP	BW37	Bank65	X2	1.8V	**Frequency:** 200MHz
TDM_CLKN	BY37	Bank65	X2	1.8V	

5.9 UART IOs

Single VU19P has two UART interface. Pin connections and functions are described in Table 5-18.

Table 5-18 UART I/O

Net Name	UART Pin Header	FPGA Pin No.	FPGA Bank	I/O Voltage
TXD1	J19.1	AD13	Bank93	3.3V
RXD1	J19.2	AE13	Bank93	3.3V
TXD2	J19.4	AE14	Bank93	3.3V
RXD2	J19.5	AE15	Bank93	3.3V
GND	J19.3			
GND	J19.6			

5.10 Virtual IOs

6 Appendix 2: Mating Connectors and Cables

This section provides information on Prodigy Logic System-compatible connectors and cables. You can either directly purchase these parts from the vendor or contact S2C sales on how to order them.

6.1 EXT Clock MMCX

You could input 3 pairs of clocks through standard MMCX connectors (JG1-JG6).

You could output 3 pairs of clocks through standard MMCX connectors (JG7-JG12).

You could input 3 resets through standard MMCX connectors (JG13-JG15).

6.2 External I/O

Prodigy connector uses Samtec SEAF 300-pin connectors, which provide 72 LVDS pairs or 144 single-ended general purpose I/O, 4 Gigabit Transceivers, 3.3V and VCCIO to daughter cards. These connectors allow you to connect Prodigy Logic System to other hardware in two ways: (i) directly mount a target board onto Prodigy Logic System, (ii) connect a target board and Prodigy Logic System by Prodigy cable.

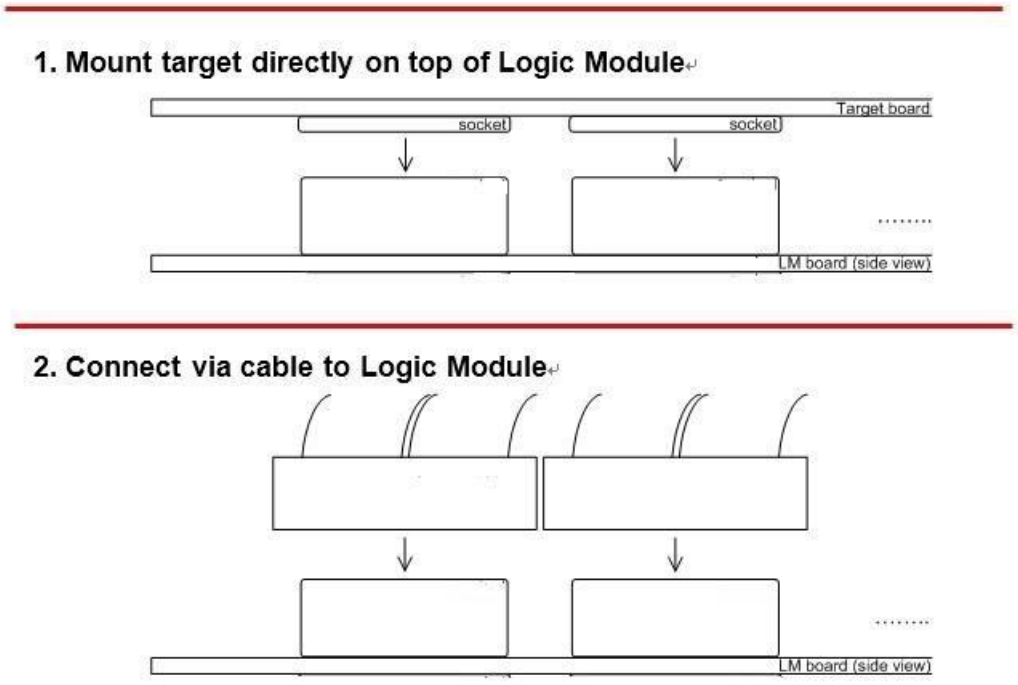

Figure 6-1 Board Connection Methods

All Prodigy connectors keep the same relative spacing between each other. If your target board requires mounting on multiple Prodigy connectors, the spatial relationship among the connectors is as follows:

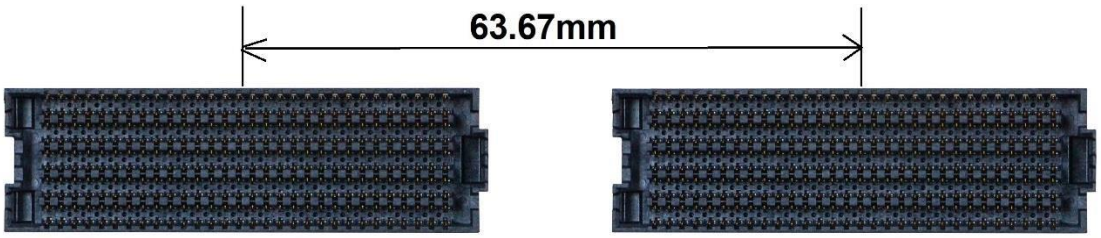

Figure 6-2 Prodigy Connector Spacing

The specifications of the components needed to mate the Prodigy connectors are as follows:

Top side	Socket connector
Manufacturer	Samtec
Part Number	SEAF-30-06.5-S-10-2-A-K-TR
Mates With	SEAM-30-02.0-S-10-2-A-K-TR or SEAM-30-11.0-S-10-2-A-K-TR

The specification of SEAF-30-06.5-S-10-2-A-K-TR is shown on Figure 6-3.

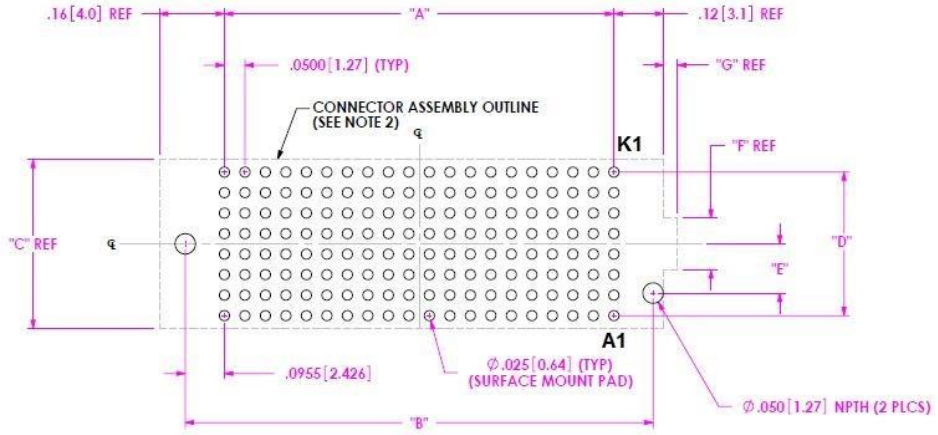

TABLE 1

No. OF POS	"A"	"B"
-10	.450 [11.430]	.641 [16.28]
-15	.700 [17.780]	.891 [22.63]
-19	.900 [22.860]	1.091 [27.71]
-20	.950 [24.130]	1.141 [28.96]
-25	1.200 [30.480]	1.391 [35.33]
-30	1.450 [36.830]	1.641 [41.68]
-40	1.950 [49.530]	2.141 [54.38]
-50	2.450 [62.230]	2.641 [67.06]

TABLE 2

ROW	"C"	"D"	"E"	"F"	"G"
-04	.22 [5.6]	.150 [3.81]	.079 [2.01]	.13 [3.2]	.05 [1.3]
-05	.32 [8.2]	.200 [5.08]	.120 [3.05]	.22 [5.7]	.03 [0.8]
-06	.32 [8.2]	.250 [6.35]	.120 [3.05]	.22 [5.7]	.03 [0.8]
-08	.42 [10.7]	.350 [8.89]	.120 [3.05]	.13 [3.2]	.03 [0.8]
-10	.52 [13.2]	.450 [11.43]	.120 [3.05]	.22 [5.7]	.03 [0.8]

Figure 6-3 SEAF-30-06.5-S-10-2-A-K-TR specification

The specification of SEAM-30-02.0-S-10-2-A-K-TR or SEAM-30-11.0-S-10-2-A-K-TR is shown on Figure 6-4.

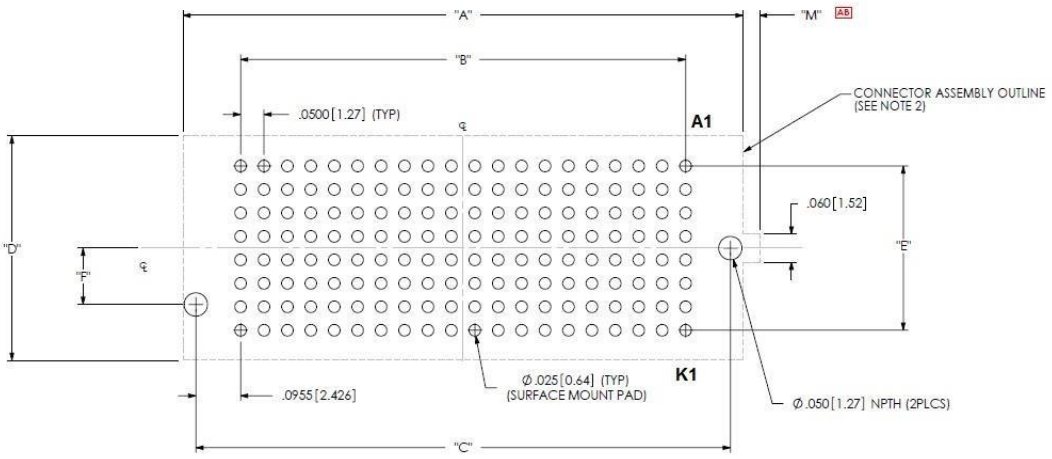

TABLE 1

No. OF POS	"A"	"B"	"C"
-10	.696 [17.68]	.450 [11.430]	.641 [16.28]
-15	.946 [24.03]	.700 [17.780]	.891 [22.63]
-19	1.146 [29.11]	.900 [22.860]	1.091 [27.71]
-20	1.196 [30.38]	.950 [24.130]	1.141 [28.98]
-25	1.446 [36.73]	1.200 [30.480]	1.391 [35.33]
-30	1.696 [43.08]	1.450 [36.830]	1.641 [41.68]
-40	2.196 [55.78]	1.950 [49.530]	2.141 [54.38]
-50	2.696 [68.48]	2.450 [62.230]	2.641 [67.08]

TABLE 2

ROW	LEAD STYLE	"D"	"E"	"F"	"M" AB
-04	-02.0, -03.0 & -03.5	.278 [7.06]	.150 [3.81]	.079 [2.01]	.063 [1.60]
	-07.0, -09.0, & -11.0	.328 [8.33]	.150 [3.81]	.079 [2.01]	.063 [1.60]
-05	-02.0, -03.0, -03.5, -05.5	.378 [9.60]	.200 [5.08]	.120 [3.05]	.035 [0.89]
-06	-02.0, -03.0, -03.5, -05.5	.378 [9.60]	.250 [6.35]	.120 [3.05]	.035 [0.89]
	-06.0, -07.0, 09.0, -11.0	.428 [10.87]	.250 [6.35]	.120 [3.05]	.035 [0.89]
-08	-02.0, -03.0 & -03.5	.478 [12.14]	.350 [8.89]	.120 [3.05]	.035 [0.89]
	06.5, -07.0, -09.0, & -11.0	.528 [13.41]	.350 [8.89]	.120 [3.05]	.035 [0.89]
-10	-02.0, -03.0 & -03.5	.578 [14.68]	.450 [11.43]	.120 [3.05]	.035 [0.89]
	06.5, -07.0, -09.0, & -11.0	.628 [15.95]	.450 [11.43]	.120 [3.05]	.035 [0.89]

Figure 6-4 SEAM-30-02.0-S-10-2-A-K-TR specification

Prodigy GT connector uses Samtec SEAF 120-pin connectors, which provide 8 Gigabit Transceivers, 16 GPIOs and 3.3V to daughter cards. These connectors allow you to directly mount a target board onto Prodigy Logic System.

All Prodigy GT connectors keep the same relative spacing between each other. If your target board requires mounting on multiple Prodigy GT connectors, the spatial relationship among the connectors is as follows:

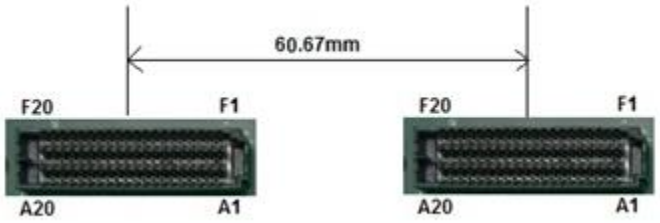

Figure 6-5 Prodigy GT Connector Spacing

The specifications of the components needed to mate the Prodigy connectors are as follows:

Top side	Socket connector
Manufacturer	Samtec
Part Number	SEAF-20-06.5-S-06-2-A-K-TR
Mates With	SEAM-20-02.0-S-06-2-A-K-TR or SEAM-20-11.0-S-06-2-A-K-TR

The specification of SEAF-20-06.5-S-06-2-A-K-TR is shown on Figure 6-6.

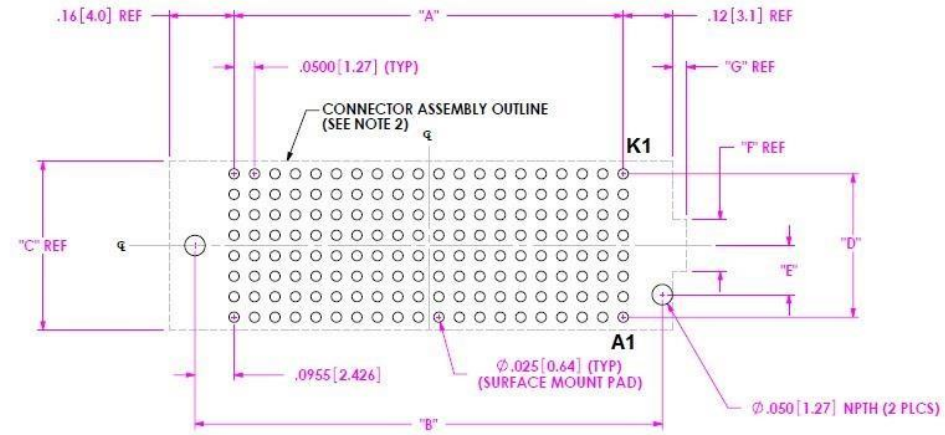

TABLE 1		
No. OF POS	"A"	"B"
-10	450 [11.430]	.641 [16.28]
-15	700 [17.780]	.891 [22.63]
-19	.900 [22.860]	1.091 [27.71]
-20	.950 [24.130]	1.141 [28.98]
-25	1.200 [30.480]	1.391 [35.33]
-30	1.450 [36.830]	1.641 [41.68]
-40	1.950 [49.530]	2.141 [54.38]
-50	2.450 [62.230]	2.641 [67.08]

TABLE 2					
ROW	"C"	"D"	"E"	"F"	"G"
-04	.22 [5.6]	.150 [3.81]	.079 [2.01]	.13 [3.2]	.05 [1.3]
-05	.32 [8.2]	.200 [5.08]	.120 [3.05]	.22 [5.7]	.03 [0.8]
-06	.32 [8.2]	.250 [6.35]	.120 [3.05]	.22 [5.7]	.03 [0.8]
-08	.42 [10.7]	.350 [8.89]	.120 [3.05]	.13 [3.2]	.03 [0.8]
-10	.52 [13.2]	.450 [11.43]	.120 [3.05]	.22 [5.7]	.03 [0.8]

Figure 6-6 SEAF-20-06.5-S-06-2-A-K-TR specification

The specification of SEAM-20-02.0-S-06-2-A-K-TR or SEAM-20-11.0-S-06-2-A-K-TR is shown on Figure 6-7.

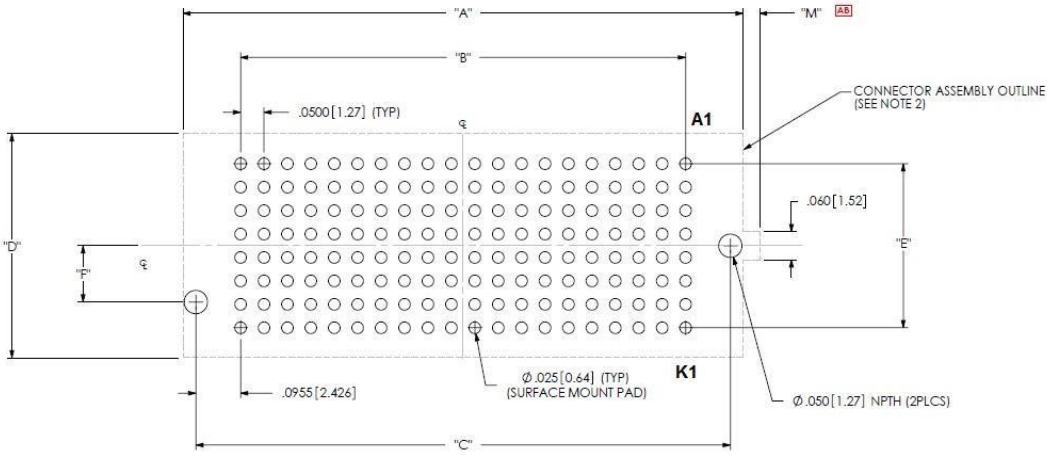

TABLE 1			
No. OF POS	"A"	"B"	"C"
-10	.696 [17.68]	.450 [11.430]	.641 [16.28]
-15	.946 [24.03]	.700 [17.780]	.891 [22.63]
-19	1.146 [29.11]	.900 [22.860]	1.091 [27.71]
-20	1.196 [30.38]	.950 [24.130]	1.141 [28.98]
-25	1.446 [36.73]	1.200 [30.480]	1.391 [35.33]
-30	1.696 [43.08]	1.450 [36.830]	1.641 [41.68]
-40	2.196 [55.78]	1.950 [49.530]	2.141 [54.38]
-50	2.696 [68.48]	2.450 [62.230]	2.641 [67.08]

TABLE 2					
ROW	LEAD STYLE	"D"	"E"	"F"	"M" AB
-04	-02.0, -03.0 & -03.5	.278 [7.06]	.150 [3.81]	.079 [2.01]	.063 [1.60]
	-07.0, -09.0, & -11.0	.328 [8.33]	.150 [3.81]	.079 [2.01]	.063 [1.60]
-05	-02.0, -03.0, -03.5, -05.5	.378 [9.60]	.200 [5.08]	.120 [3.05]	.035 [0.89]
-06	-02.0, -03.0, -03.5, -05.5	.378 [9.60]	.250 [6.35]	.120 [3.05]	.035 [0.89]
	-06.0, -07.0, 09.0, -11.0	.428 [10.87]	.250 [6.35]	.120 [3.05]	.035 [0.89]
-08	-02.0, -03.0 & -03.5	.478 [12.14]	.350 [8.89]	.120 [3.05]	.035 [0.89]
	06.5, -07.0, -09.0, & -11.0	.528 [13.41]	.350 [8.89]	.120 [3.05]	.035 [0.89]
-10	-02.0, -03.0 & -03.5	.578 [14.68]	.450 [11.43]	.120 [3.05]	.035 [0.89]
	06.5, -07.0, -09.0, & -11.0	.628 [15.95]	.450 [11.43]	.120 [3.05]	.035 [0.89]

Figure 6-7 SEAM-20-02.0-S-06-2-A-K-TR specification

7 Appendix 3: Pin-outs / Board dimensions

This appendix presents the following collected information:

- JTAG signal pinout
- Prodigy Connector (300-pin) pinouts
- Prodigy GT (120-pin) pinouts
- FPGA Module board dimensions

Table 7-1 JTAG Signal and Pin Number

JTAG Signal & Pin Num						
2. VREF	4.TMS	6.TCK	8.TDO	10.TDI	12.NC	14.NC
1. GND	3. GND	5. GND	7. GND	9. GND	11. GND	13. GND

Table 7-2 Prodigy Connector Pinouts (Samtec **300-pin** SEAF)

	K	J	H	G	F	E	D	C	B	A
1	LA22_P	GND	LA16_P	GND	LA09_P	GND	LA03_P	GND	PRSNT	GND
2	LA22_N	LA19_P	LA16_N	LA12_P	LA09_N	LA06_P	LA03_N	LA00_P	GND	DP3_M2C_P
3	GND	LA19_N	GND	LA12_N	GND	LA06_N	GND	LA00_N	GND	DP3_M2C_N
4	LA23_P	GND	LA17_P	GND	LA10_P	GND	LA04_P	GND	DP3_C2M_P	GND
5	LA23_N	LA20_P	LA17_N	LA13_P	LA10_N	LA07_P	LA04_N	GND	DP3_C2M_N	GND
6	GND	LA20_N	GND	LA13_N	GND	LA07_N	GND	LA01_P	GND	DP2_M2C_P
7	RES	GND	LA18_P	GND	LA11_P	GND	LA05_P	LA01_N	GND	DP2_M2C_N
8	RES	LA21_P	LA18_N	LA14_P	LA11_N	LA08_P	LA05_N	GND	DP2_C2M_P	GND
9	GND	LA21_N	GND	LA14_N	GND	LA08_N	GND	GND	DP2_C2M_N	GND
10	LB22_P	GND	LB15_P	GND	LB09_P	GND	GND	LA02_P	GND	DP1_M2C_P
11	LB22_N	LB19_P	LB15_N	LA15_P	LB09_N	LB06_P	GND	LA02_N	GND	DP1_M2C_N
12	GND	LB19_N	GND	LA15_N	GND	LB06_N	LB03_P	GND	DP1_C2M_P	GND
13	LB23_P	GND	LB16_P	GND	LB10_P	GND	LB03_N	GND	DP1_C2M_N	GND
14	LB23_N	LB20_P	LB16_N	LB12_P	LB10_N	LB07_P	GND	LB00_P	GND	DP0_M2C_P
15	GND	LB20_N	GND	LB12_N	GND	LB07_N	GND	LB00_N	GND	DP0_M2C_N
16	RES	GND	LB17_P	GND	LB11_P	GND	LB04_P	GND	DP0_C2M_P	GND
17	RES	LB21_P	LB17_N	LB13_P	LB11_N	LB08_P	LB04_N	GND	DP0_C2M_N	GND
18	GND	LB21_N	GND	LB13_N	GND	LB08_N	GND	LB01_P	GND	REFCLK0_P
19	LC22_P	GND	LB18_P	GND	LC08_P	GND	LB05_P	LB01_N	GND	REFCLK0_N
20	LC22_N	LC18_P	LB18_N	LB14_P	LC08_N	LC04_P	LB05_N	GND	REFCLK1_P	GND
21	GND	LC18_N	GND	LB14_N	GND	LC04_N	GND	GND	REFCLK1_N	GND
22	LC23_P	GND	LC15_P	GND	LC09_P	GND	GND	LB02_P	GND	SCL
23	LC23_N	LC19_P	LC15_N	LC12_P	LC09_N	LC05_P	GND	LB02_N	TMS	SDA
24	GND	LC19_N	GND	LC12_N	GND	LC05_N	LC02_P	GND	TCK	GA0
25	RES	GND	LC16_P	GND	LC10_P	GND	LC02_N	GND	TDO	GA1
26	RES	LC20_P	LC16_N	LC13_P	LC10_N	LC06_P	GND	LC00_P	TDI	GA2
27	GND	LC20_N	GND	LC13_N	GND	LC06_N	LC03_P	LC00_N	GND	GND
28	RES	GND	LC17_P	GND	LC11_P	GND	LC03_N	GND	VCCIO	VCC3V3
29	RES	LC21_P	LC17_N	LC14_P	LC11_N	LC07_P	GND	LC01_P	VCCIO	VCC3V3
30	GND	LC21_N	GND	LC14_N	GND	LC07_N	GND	LC01_N	VCCIO	VCC3V3

User should refer to "S2C Prodigy Logic System Daughter Board Design Guide" to know the definitions of pin PRSNT, SCL, SDA, GA[0:2] , RESERVED[0:12] on Prodigy connector if they plan to make their own Prodigy daughter cards.

Table 7-3 Prodigy GT Connector Pinouts (Samtec **120-pin** SEAF)

	F	E	D	C	B	A
1	VCC3V3	VCC3V3	VCC3V3	VCC3V3	GND	GND
2	LA00_P	LA00_N	GND	GND	DP7_M2C_P	DP7_M2C_N
3	GND	GND	DP7_C2M_P	DP7_C2M_N	GND	GND
4	LA01_P	LA01_N	GND	GND	DP6_M2C_P	DP6_M2C_N
5	GND	GND	DP6_C2M_P	DP6_C2M_N	GND	GND
6	LA02_P	LA02_N	GND	GND	DP5_M2C_P	DP5_M2C_N
7	GND	GND	DP5_C2M_P	DP5_C2M_N	GND	GND
8	TMS	TCK	GND	GND	DP4_M2C_P	DP4_M2C_N
9	GND	GND	DP4_C2M_P	DP4_C2M_N	GND	GND
10	TDO	TDI	GND	GND	DP3_M2C_P	DP3_M2C_N
11	GND	GND	DP3_C2M_P	DP3_C2M_N	GND	GND
12	LA03_P	LA03_N	GND	GND	DP2_M2C_P	DP2_M2C_N
13	GND	GND	DP2_C2M_P	DP2_C2M_N	GND	GND
14	LA04_P	LA04_N	GND	GND	DP1_M2C_P	DP1_M2C_N
15	GND	GND	DP1_C2M_P	DP1_C2M_N	GND	GND
16	LA05_P	LA05_N	GND	GND	DP0_M2C_P	DP0_M2C_N
17	GND	GND	DP0_C2M_P	DP0_C2M_N	GND	GND
18	LA06_P	LA06_N	GND	GND	REFCLK0_P	REFCLK0_N
19	GND	GND	REFCLK1_P	REFCLK1_N	SDA	SCL
20	LA07_P	LA07_N	PRSNT	GA0	GA1	GA2

7.1 FPGA Module: Board Dimension

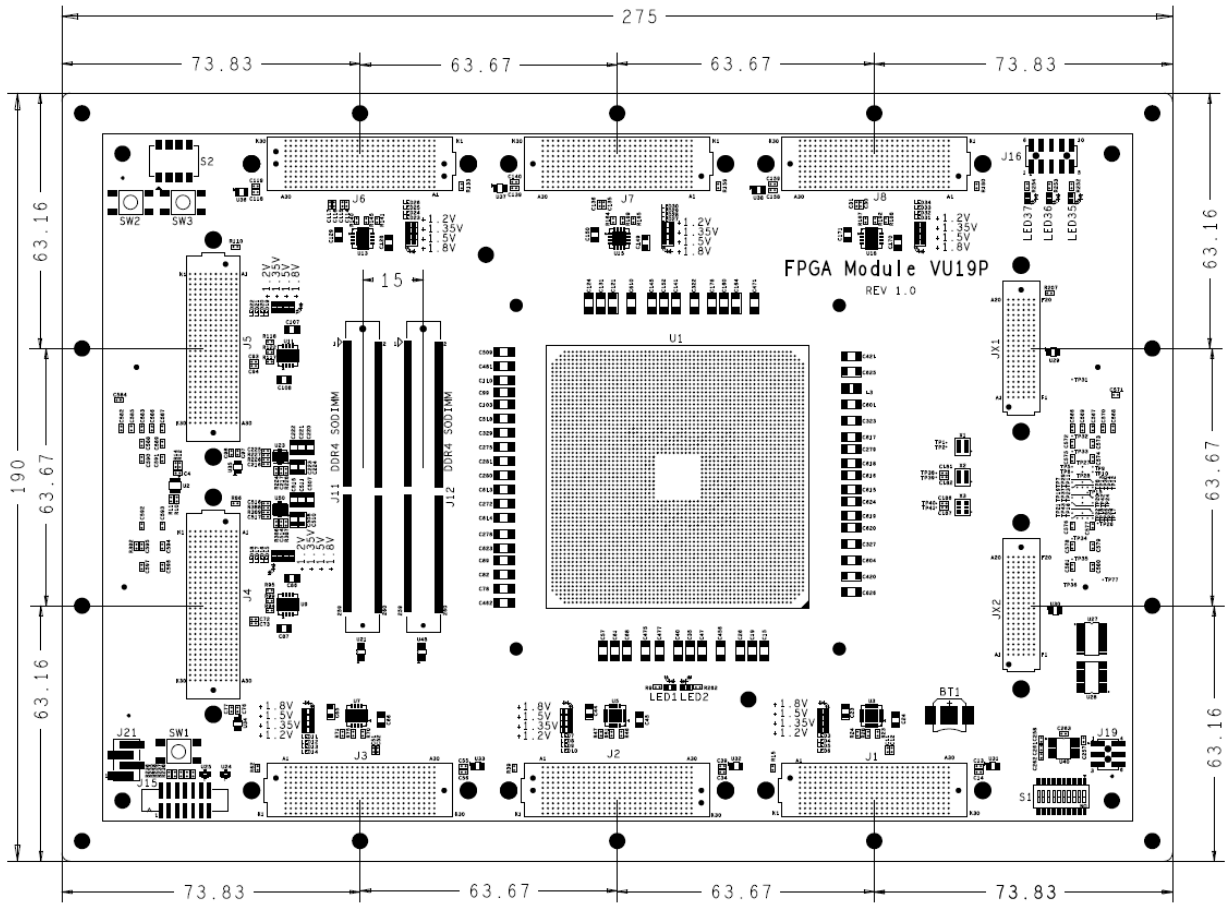

Figure 7-1 FPGA Module VU19P Board Dimension

8 Care and Handling

Important: The VU19P Chassis System does *not* contain any user-serviceable components. Do not attempt to access any internal components or disassemble the system.

DISASSEMBLY WILL VOID WARRANTY

8.1 Safety Precautions

Please take the following safety precautions in the care and handling of your Prodigy Logic System:

- Prodigy Logic System supports only 12V DC power inputs, through the ATX 8-Pin CPU power connector. Applying any voltage above 12V may damage your Prodigy Logic System.
- Before powering up the Prodigy Logic System, you MUST install and use the fans which are included in the package to cool the FPGA devices on the Prodigy Logic System.
- If you use OSC1 for clock inputs, please ensure that the oscillators are inserted with the right directions before powering up the Prodigy Logic System.
- If the statuses of LED are not consistent with the LED default statuses described in the reference manual when you power on Prodigy Logic System, please power down Prodigy Logic System immediately to prevent further damage caused by possible power shorting.
- Do not plug or unplug the following components when Prodigy Logic System is powered on:
    - Intel Altera JTAG cable
    - Oscillators in the OSC socket
    - Prodigy LS connectors
    - SODIMM socket
- Do not adjust any of the switches on Prodigy Logic System when it is powered on.
- If the daughter/mother boards that connect to Prodigy Logic Systems use different power source with Prodigy logic modules, the correct power on sequence is:
    - Connect your mother/daughter boards with Prodigy Logic System when all of them are powered off
    - Power on Prodigy Logic System
    - Download Prodigy Logic System FPGA
    - Power on daughter/mother board
- And the correct power off sequence is:
    - Power off daughter/mother board
    - Power off Prodigy LS
- All Prodigy LS FPGA I/O are directly drawn out to optimize application flexibility and performance, and thus do NOT have any protection. As such, any voltage above 1.8V or logic short may lead to permanent FPGA I/O pin damage. Do not connect Prodigy Logic System's I/Os to any target device with a voltage above 1.8V. Also make sure that all I/O connectors are securely connected before powering on.
- When using PGT connector on Prodigy LS, please make sure the interface on daughter card matches with PGT I/O requirement.

- There are 16 common I/Os in each PGT connector. The common I/Os support up to 1.8V. Refer To 'Prodigy LS Hardware Reference Manual' for pin information.
- When probing Prodigy Logic System I/Os with a logic analyzer or an oscilloscope, make sure that the probing tool does not touch adjacent pins, which may cause a short circuit, and that the test equipment has the same ground as that of Prodigy Logic System.
- Do not place Prodigy Logic System on any electrical conducting surface.
- Make sure that you work in an anti-static environment and observe all necessary antistatic handling precautions before unpacking and operating Prodigy Logic System.
- Pressure and/or shaking may damage Prodigy Logic System. High temperatures, high voltages, moisture, dust, static, and magnetization should also be avoided.
- Prodigy Logic System should not be cleaned with or come into contact with any liquids.

8.2 Electrostatic Handling Considerations

- Prodigy Logic System is packaged in antistatic or conductive containers. Before taking it out of its container, make sure the module is in a static-free workstation (location).
- Prodigy Logic System must remain in its protective packaging unless it is being used in a static-free location. Transport the module only in its original container to avoid any potential damage to the pins.
- Before removing Prodigy Logic System from its packaging, place the package on a grounded bench top, ensure a wrist strap is snugly worn around your wrist and is properly plugged into the ground receptacle, and then ground your hands by placing them in contact with the conductive bench top.
- A conductive shoe strap with conductive tiles or mats may be used instead of the wrist strap.
- Once you leave the workstation, you must still follow the previous procedures when you return to work with the module at the static-free location.
- Do not place Prodigy Logic System in contact with plastic snow polystyrene foam, Styrofoam peanuts, or other high-dielectric materials, unless these materials have been treated with an antistatic agent (treated materials appear pink and generate less than 100V).
- Do not transport Prodigy Logic System or store it in trays, tote boxes, vials, or other containers made of untreated plastic, unless it is protected within its original packaging.

NOTE: Please save the original packaging for future shipment needs.

9 Help and Support

Check with your local sales representative about local support services. For a list of local offices see the Contact Us link on our Web site:
http://www.s2cinc.com/AboutS2C/ContactUs.htm
Additionally, you can contact our technical support via email at **support@s2cinc.com**.

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