Cortex®-M0 DesignStart™ Design Kit (AT510)

r1p0-00rel0

Release Note

Cortex-M0 DesignStart Design Kit Release Note

Proprietary notice

Document confidentiality status

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Product status

The information in this document is for a product at Full Release status.

Web address

http://www.arm.com

Feedback

ARM limited welcomes feedback on both the product, and the documentation.

Support for the Cortex-M0 DesignStart Design Kit

Support is not provided with the Cortex-M0 DesignStart Design Kit. However, if you have a question you can post it on the ARM forums at http://forums.arm.com.

Feedback on this document

If you have any comments about this document, please send email to errata@arm.com giving:

- The document title
- The document's number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

ARM Internal Document Reference

ARM-EPM-091340 0.12

Contents

1 PRODUCT DELIVERABLES

1.1 Product Release Status

This is the full release of the ARM Cortex-M0 DesignStart Design Kit at revision r1p0. These deliverables are released under the terms of the agreement between ARM and each licensee (the "Agreement"). Use by recipient of the deliverables is subject to the terms and conditions of the Agreement.

NOTE:

- These deliverables may only be used as described in the terms of your legal agreement.

1.2 About the ARM Cortex-M0 DesignStart Design Kit

The Cortex-M0 DesignStart Design Kit is intended for system Verilog design and simulation of a prototype SoC based on the Cortex-M0 DesignStart processor.

The DesignStart Design Kit has:

- An ARM Cortex-M0 DesignStart processor.
- An example system-level design for the ARM Cortex-M0 processor.
- Reusable AMBA components for system-level development.

The Cortex-M0 DesignStart processor is a fixed configuration of the Cortex-M0 processor, enabling low cost easy access to Cortex-M0 processor technology by offering a subset of the full product.

The Cortex-M0 DesignStart processor is delivered as a preconfigured and obfuscated, but synthesizable, Verilog version of the full Cortex-M0 processor and is intended for integration and simulation purposes. It does not have debug capability (as this is not used in RTL simulation) and is not intended for production silicon.

A Cortex-M0 DesignStart FPGA Prototyping Kit is also available for system prototyping with the ARM Versatile™ Express Cortex-M Prototyping System (http://www.arm.com/products/tools/development-boards/versatile-express/cortex-m-prototyping-system.php)

The Cortex-M0 DesignStart FPGA Prototyping Kit includes an encrypted FPGA image of the Cortex-M0 DesignStart processor as well as a customizable AHB subsystem. Unlike the Cortex-M0 DesignStart processor of the DesignStart Design Kit, the encrypted image of the Cortex-M0 DesignStart processor contains debug logic that supports software development and debug on the ARM MPS2 board.

In addition, the AHB subsystem delivered with the FPGA prototyping kit is modifiable, allowing the user to customize logic surrounding the DesignStart processor. This customization process relies on technology supplied by Altera's Quartus FPGA design tool called partial reconfiguration. There are tool requirements for usage of the partial reconfiguration feature. These requirements are explained in the *MPS2 license request* instruction document (http://www.arm.com/files/pdf/MPS2_PR_licence_request.pdf).

In order to enable the partial reconfiguration feature, an additional license is required to the basic Quartus Prime subscription edition license. If you do not have the partial reconfiguration feature enabled in your existing license then please contact mps-support@arm.com to request one.

1.3 ARM Part Numbers for this product

The files are delivered through ARM's IP delivery server (http://connect.arm.com).

The following table lists the ARM part numbers for the individual deliverables that form part of the delivery.

Table *1.3-1*: ARM part numbers for release AT510-BU-98000

Product code	Description	Version
AT510-DC-80001	Cortex-M0 DesignStart Design Kit Release Note – PDF System format	r1p0-00rel0
AT510-DC-80002	Cortex-M0 DesignStart RTL Testbench User Guide	r1p0-00rel0
AT510-MN-80001	Synthesizable RTL – Verilog	r1p0-00rel0

2 INSTALLATION

2.1 Introduction

The Cortex-M0 DesignStart Design Kit intellectual property (IP) deliverables are provided as a single zipped tar file. The following instructions cover Unix-like operating systems only.

2.1.1 Unpacking the shipment

The Cortex-M0 DesignStart Design Kit is distributed as a single zipped tar file bundle containing three sub-deliverables, AT510-DC-80001 (this release note), AT510-DC-80002 (the *Cortex-M0 DesignStart RTL Testbench User Guide*) and AT510-MN-80001 (the synthesizable Verilog and test-bench). Download the zipped tar file and unpack it using the GNU gtar utility command:

```
% gtar xzvf AT510-BU-98000-r1p0-00rel0.tgz
```

The content of the zipped tar file is described in section 1.2 of *the Cortex-M0 DesignStart RTL Testbench User Guide*.

Once unpacked, the deliverables are ready to use.

3 TOOLS

This release of the Cortex-M0 DesignStart Design Kit supports Linux and Unix for the simulation process and the synthesis process. If you use Keil MDK-ARM for software development, you can install the design kit in a location that is accessible from Linux, Unix, and Windows. Do this using one of the following procedures:

- Install the design kit on a network drive that:
  - A Linux or Unix terminal can access.
  - Is mapped to a network drive on a Windows machine.

- Use a personal computer to do the following:
  - Install virtualization software and install a guest Operating System (OS).
  - Set up a shared folder to access the design kit through the host OS.
  - Install the design kit in the shared folder.

Then compile the software with Keil MDK-ARM in the Windows environment, and run the simulations in the Linux or Unix environment. To run the design kit on other operating systems, modify the makefiles to meet your specific requirements.

This release of Cortex-M0 DesignStart Design Kit has been developed with the following tools:

- Mentor Questasim 10.3b
- Cadence Incisive 10.20.010
- Synopsys VCS 2011.12
- RVCT 5.06.21
- Synopsys DC 2013.03-SP5
- Synopsys Formality 2013.03-SP5

4 KNOWN ISSUES AND LIMITATIONS

Please refer to section 1.3 of the *ARM Cortex-M0 DesignStart RTL Testbench User Guide*.

5 DIFFERENCES FROM PREVIOUS RELEASE

5.1 Differences from release r0p0-00rel0

The following table compares supported features on Cortex-M0 DesignStart Design Kit r1p0 from Cortex-M0 DesignStart Processor r0p0:

Table 4.1-1: Comparison between Cortex-M0 DesignStart processor r0p0 and Cortex-M0 DesignStart Design Kit r1p0

	Cortex-M0 DesignStart processor r0p0	Cortex-M0 DesignStart Design Kit r1p0
ARMv6-M compatible	Yes	Yes
Deliverable	Obfuscated, flattened, gate-level Verilog	Obfuscated, flattened, gate-level Verilog
Configuration options	No	No
Interrupt lines	16	32
Multiplier	slow	fast
Debug	No	No
Low power mode support and WIC	No	No
Example sub-system	No	Includes example system design as well as some AHB peripherals

6 BENEFITS OF THE FULL CORTEX-M0 PROCESSOR

The Cortex-M0 DesignStart processor is not intended for production system on chips. As such, the full Cortex-M0 processor provides additional capabilities above that of the Cortex-M0 DesignStart processor. These are:

6.1 Low power optimizations

The full Cortex-M0 processor is designed for deployment in a multi-power domain system to maximize static power efficiency, featuring a minimal *Wake-up Interrupt Controller* (WIC). It also makes extensive use of architectural clock gating to minimize dynamic power. For simplicity these are amongst the technologies not included in the Cortex-M0 DesignStart processor.

6.2 Debug support

The full Cortex-M0 processor supports the use of an external hardware debugger to facilitate the development of applications. Connection is possible via either Serial-Wire or JTAG interfaces and provides a host of debug functionality. Both connections provide the ability to access all AHB-Lite connected slaves, including RAM, whilst the processor is running, as well as providing full halting-mode debug. Halting-mode debug allows all processor registers to be examined and modified, and can be configured to provide up to four hardware breakpoints and two hardware watchpoints. Unlimited software breakpoints are possible via the BKPT instruction. The Cortex-M0 DesignStart processor implementation does not provide any debug capabilities. For information on Debug support, see *Cortex-M0 DesignStart FPGA Testbench User Guide*

6.3 Hardware multiplier options

The ARMv6-M architecture provides a MULS instruction capable of performing a 32-bitx32-bit multiply, generating a 32-bit result. The full Cortex-M0 processor product allows implementation time selection between a fast single-cycle implementation and a low-area 32-cycle implementation. The Cortex-M0 DesignStart processor only provides the single-cycle option.

6.4 Jitter-free interrupt handling

The full Cortex-M0 processor provides the capability to optionally regulate the time between an interrupt-signal being asserted and having the associated exception handler being entered, thus providing zero-jitter interrupt entry. The Cortex-M0 DesignStart processor always handles interrupts as fast as possible.

6.5 Migrating to the Full Cortex-M0 Processor

The Cortex-M0 DesignStart processor is derived from the full ARM Cortex-M0 AT510-MN-22100-r0p0-03rel1 deliverable. The DesignStart version of the ARM Cortex-M0 processor offers a preconfigured subset of the features, interfaces, capabilities, power-domains, documentation and synthesis support of the full ARM Cortex-M0 processor. Licensees of the full Cortex-M0 processor have access to the plain-text Verilog RTL with the ability to configure the processor via Verilog parameters. Licensees wishing to mirror the parameters used for the DesignStart Cortex-M0 processor should set the RAR and SYST parameters to 1, the NUMIRQ parameter to 32 and set all other parameters to zero. The full Cortex-M0 processor includes additional ports, not present in the Cortex-M0 DesignStart processor. The full Cortex-M0 processor can be configured to match the Cortex-M0 DesignStart processor by assigning **SCLK** from **HCLK**, tying **SLEEPHOLDREQn** HIGH, and tying all other unused inputs LOW.

7 SUPPORT AND MAINTENANCE

Support is not provided with the Cortex-M0 DesignStart Design Kit. However, if you have a question you can post it on the ARM forums at http://forums.arm.com.