**Midterm – 600pts total**

1. Compare and contrast (tell me why) verifying at the block level vs system level in terms of:
   1. Control – 10pts
   2. Ease of debug – 10pts
   3. Simulation performance – 10pts
   4. Testbench complexity – 10pts
2. Create a 4-bit 2-state variable called addr. Generate a random number between 0 and 15 inclusive and assign it to addr. 10pts
3. Create a 4-bit 4-state variable called addr. Generate a random number between 0 and 5 inclusive and assign it to addr. 10pts
4. What aspects of a design should be randomized? Why? 20pts
5. What is the initial value of a 4-state logic type? 10pts
6. What is the initial value of a 2-state logic type? 10pts
7. Given the following declarations:

byte my\_byte;

integer my\_integer = 32’b0000\_1111\_xxxx\_zzzz;

int my\_int = my\_integer;

1. What is the range of my\_byte? Why? 10pts
2. What is the final value of my\_int? Why? 10pts
3. Declare an array of size 7x128 (7-bit word, 128 words). 10pts
4. For the array just declared what happens if a write to location 129 is attempted? 10pts
5. For the array just declared what happens if a read to location 129 is attempted? What is returned? 10pts
6. Answer the following array questions: 10pts each
   1. Declare a 2-dimensional array of size 8x3 (8-bit words by 3 words) of type bit called my\_mem. Initialize all locations to 8’hA5
   2. Declare a 2-dimensional array of size 4x4 (4-bit words by 4 words) of type logic called my\_logicmem. Initialize my\_logicmem[0]=0, my\_logicmem[1]=1, my\_logicmem[2]=2, my\_logicmem[3]=3
   3. Declare a 4-bit variable of type logic called my\_logic. Initialize my\_logic to 4’hF
   4. What is the value of my\_mem after the following assignment: my\_mem[2] = my\_logicmem[4]; Why?
   5. What is the value of my\_logic after the following assignment: my\_logic = my\_logicmem[4]; Why?
   6. What is the value of my\_logicmem after the following assignment: my\_logicmem[3] = my\_mem[3]; Why?
   7. What is the value of my\_mem after the following assignment: my\_mem[3] = my\_logic; Why?
7. Declare an associative array to hold the reset value of configuration registers. The index of the associative array is the name of the configuration register. Initialize the associative array according to the following table: 10pts

|  |  |  |
| --- | --- | --- |
| **Register** | **Width** | **Reset Value** |
| adc0\_reg | [15:0] | 16'hFFFF |
| analog\_test | [15:0] | 16'hABCD |
| digital\_test | [15:0] | 16'h0 |
| digital\_config | [15:0] | 16'h1 |

* 1. Print out only the reset value of the analog test register. 10pts

1. Given the following array declaration

shortint byte\_array[6]=`{0, 127, -128, 1, -1, 0};

what will be displayed by:

1. $display("%p", byte\_array.min); 10pts
2. $display("%p", byte\_array.max); 10pts
3. $display("%p", byte\_array.unique); 10pts
4. $display("%p”, byte\_array.find with (item > 0)); 10pts
5. $display("%p", byte\_array.find\_index with (item <0)); 10pts
6. byte\_array.sort; $display("%p”, byte\_array); 10pts
7. Suppose you are modeling a 4GB memory array that you expect to write only occasionally. What would be an appropriate storage type? Why? 10pts
8. What signals in your testbench should be of type 2-state to minimize memory usage? Why? 10pts
9. What signals in your testbench should be of type 4-state to minimize memory usage? Why? 10pts
10. Should an array of 16-bit values be modeled as an unpacked or packed array to minimize memory usage? Why? 10pts
11. Answer the following questions regarding strings.
    1. Create a variable of type string and assign to it “UCCS Engineering” 10pts
    2. Append to the end of the string “ 2009” 10pts
    3. Display the string. 10pts
12. Given the following packet structure:



* 1. Define a user defined 7-bit type. 10pts
  2. Encapsulate the fields of the packet in a structure using your new type. 10pts
  3. Instantiate the structure and assign the header to 7’h5A; 10pts

1. Why would a function be defined in an interface? 10pts
2. If the function in an interface performed non-synthesizable operations like $display how can a DUT that uses this interface be synthesizable? 10pts
3. Given the following array:

shortint shortint\_array[1023:0];

1. Create a function that prints out the last element of the array. Pass the array by reference. 10pts
2. Call the function and pass in the values by name not position. 10pts
3. For the following interface:

interface reg\_if(input bit clk);

bit write, bit [15:0] data\_in, bit [7:0] address, logic [15:0] data\_out;

modport slave (input clk, write, data\_in, address, output data\_out);

endinterface

1. Develop a clocking block called cb that: 10pts
2. is sensitive to the positive edge of clock
3. all I/O are synchronous to the clock
4. Expand the interface to create a modport for the testbench that uses the clocking block. 10pts
5. Complete the following timing diagram assuming the interface is instantiated as reg\_bus. 20pts



1. Define a class in a package that has the following characteristics: 50pts
   1. Member variables of 8-bit logic type called *header,* of 16-bit logic type called *payload*, and of 8-bit logic type called *parity,* and a static integer called *error.*
   2. A function that calculates the parity by the following diagram. Each parity bit is determined by the calculating the XOR of the rows above it. For example, parity[0]=payload[0]^payload[8]^header[0]



* 1. A custom constructor that by default initializes the *header* to 8’hA5 and the *payload* to all F’s. Values for header and payload can also be initialized through arguments passed into the constructor. The custom constructor calls the function in b. to compute the correct parity.
  2. A function that prints all the member variables of an object.

1. Design a program using the package defined in question 22) that completes the following tasks: 40pts
   1. Initialize member variable *error* through the class prior to construction.
   2. Create 2 objects. The first object will be created using the default values and the second object will be created with header = 8’h3C and payload=16’h1234 passed to the constructor by name not position.
   3. Call the print function from 22d. for each object.
   4. Explicitly deallocate the 2nd object.
2. When is a SystemVerilog construct expected to be synthesizable? Why? 10pts
3. When is verification of a design complete? Why? 20pts