**Chapter 1, Verification Guidelines homework**

The purpose of this homework is to:

1. Practice writing a test plan
2. Practice writing a test-bench
3. Become comfortable with the Questa verification environment

Create a test plan and self-checking test-bench for the ALU we went over in class. The ALU design will be provided and has the following characteristics.

1. Reset which resets C to 0.
2. 4-bit signed inputs, A and B
3. 5-bit registered signed output C
4. 4 op-codes
   1. add
   2. sub
   3. bitwise invert input A
   4. reduction OR input B
5. Assume the following encoding of the opcodes.

|  |  |
| --- | --- |
| **Opcode** | **Encoding** |
| add | 2’b00 |
| sub | 2’b01 |
| bitwise invert input A | 2’b10 |
| reduction OR input B | 2’b11 |

You must use questasim and your testbench must be self checking. Cut and paste the transcript window into your HW submission. It should look something like:

# // QuestaSim 6.6b May 21 2010 Linux 2.6.27.45-0.1-default

# //

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# //

# do run.do

# vsim ALU\_4\_bit\_tb

# Loading sv\_std.std

# Refreshing /home/UFP/gtumbush/4280/HW1/work.ALU\_4\_bit\_tb

# Loading work.ALU\_4\_bit\_tb

# Refreshing /home/UFP/gtumbush/4280/HW1/work.ALU\_4\_bit

# Loading work.ALU\_4\_bit

# .main\_pane.wave.interior.cs.body.pw.wf

# 4600: At end of test error count is 0

Deliverables:

1. Test plan for ALU
2. Code for ALU testbench
3. Copy of transcript window