

Base Address	31	...	24	23	...	16	15	...	8	7	6	5	4	3	2	1	0	Register name
0xFFED000	Unused																E	ICDDCR
0xFFED100	Set-enable bits																	ICDISER <sub>n</sub>
0xFFED180	Clear-enable bits																	ICDICER <sub>n</sub>
0xFFED400	Priority, offset 3				Priority, offset 2				Priority, offset 1				Priority, offset 0				ICDIPR <sub>n</sub>	
0xFFED800	CPUs, offset 3				CPUs, offset 2				CPUs, offset 1				CPUs, offset 0				ICDIPT <sub>R</sub> <sub>n</sub>	
0xFFEDC00	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	ICDICFR <sub>n</sub>	