| 31 | | | 24 | 23 | | | 16 | 15 | | • • | 8 | 7 6 | 5 4 | 3 2 | 1 0 | Register name |
|--------------------|-------------------|---|---|---|--|---|---|--|--|--|---|--|--|--|---|--|
| Unused | | | | | | | | | | | | | | | ICDDCR | |
| | Set-enable bits | | | | | | | | | | | | | | | ICDISERn |
| | Set-enable bits | | | | | | | | | | | | | | | |
| | Clear-enable bits | | | | | | | | | | | | | | | ICDICERn |
| | Clear-enable bits | | | | | | | | | | | | | | | |
| Priority, offset 3 | | | | Priority, offset 2 | | | | Priority, offset 1 | | | | Priority, offset 0 | | | | ICDIPRn |
| Priority, offset 3 | | | Priority, offset 2 | | | | Priority, offset 1 | | | | Priority, offset 0 | | | | | |
| CPUs, offset 3 | | | | CPUs, offset 2 | | | | CPUs, offset 1 | | | | CPUs, offset 0 | | | | ICDIPTRn |
| CPUs, offset 3 | | | | CPUs, offset 2 | | | | CPUs, offset 1 | | | | CPUs, offset 0 | | | | |
| F15 | F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | ICDICFRn |
| F15 | F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | |
| | Pri Pri Cl F15 | Priority, Priority, CPUs, CPUs, F15 F14 | Priority, offse Priority, offse CPUs, offse CPUs, offse F15 F14 F13 | Priority, offset 3 Priority, offset 3 CPUs, offset 3 CPUs, offset 3 F15 F14 F13 F12 | Priority, offset 3 Pri Priority, offset 3 Pri CPUs, offset 3 CPUs, | Priority, offset 3 Priority, Priority, offset 3 Priority, CPUs, offset 3 CPUs, CPUs, offset 3 CPUs, F15 F14 F13 F12 F11 F10 | Se Se Cle Cle Cle Priority, offset 3 Priority, offset Priority, offset 3 Priority, offset CPUs, offset 3 CPUs, offset CPUs, offset 3 CPUs, offset F15 F14 F13 F12 F11 F10 F9 | Set-ena Set-ena Clear-en Clear-en Priority, offset 3 Priority, offset 2 Priority, offset 3 Priority, offset 2 CPUs, offset 3 CPUs, offset 2 CPUs, offset 3 CPUs, offset 2 F15 F14 F13 F12 F11 F10 F9 F8 | Unused Set-enable by Set-enable by Clear-enable by Clear-enable Clear-enable Priority, offset 3 Priority, offset 2 Priority, offset 3 Priority, offset 2 Priority, offset 3 CPUs, offset 2 CPUs, offset 3 CPUs, offset | Unused Set-enable bits Set-enable bits Clear-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, Priority, offset 3 Priority, offset 2 Priority, CPUs, offset 3 CPUs, offset 2 CPUs, CPUs, offset 3 CPUs, offset 2 CPUs, F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 | Unused Set-enable bits Set-enable bits Clear-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, offset Priority, offset 3 Priority, offset 2 Priority, offset CPUs, offset 3 CPUs, offset 2 CPUs, offset CPUs, offset 3 CPUs, offset 2 CPUs, offset CPUs, offset 3 CPUs, offset 2 CPUs, offset F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 | Unused Set-enable bits Set-enable bits Clear-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 3 Priority, offset 2 Priority, offset 1 CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 F4 | Unused Set-enable bits Set-enable bits Clear-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 3 CPUs, offset 2 CPUs, offset 1 CI CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CI F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 F4 F3 | Unused Set-enable bits Set-enable bits Clear-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, The priority of the priorit | Unused Set-enable bits Clear-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, offset CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, offset CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, offset F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 F4 F3 F2 F1 | Unused Set-enable bits Set-enable bits Clear-enable bits Clear-enable bits Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 0 Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 0 Priority, offset 3 Priority, offset 2 Priority, offset 1 Priority, offset 0 CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, offset 0 CPUs, offset 3 CPUs, offset 2 CPUs, offset 1 CPUs, offset 0 F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 F4 F3 F2 F1 F0 |