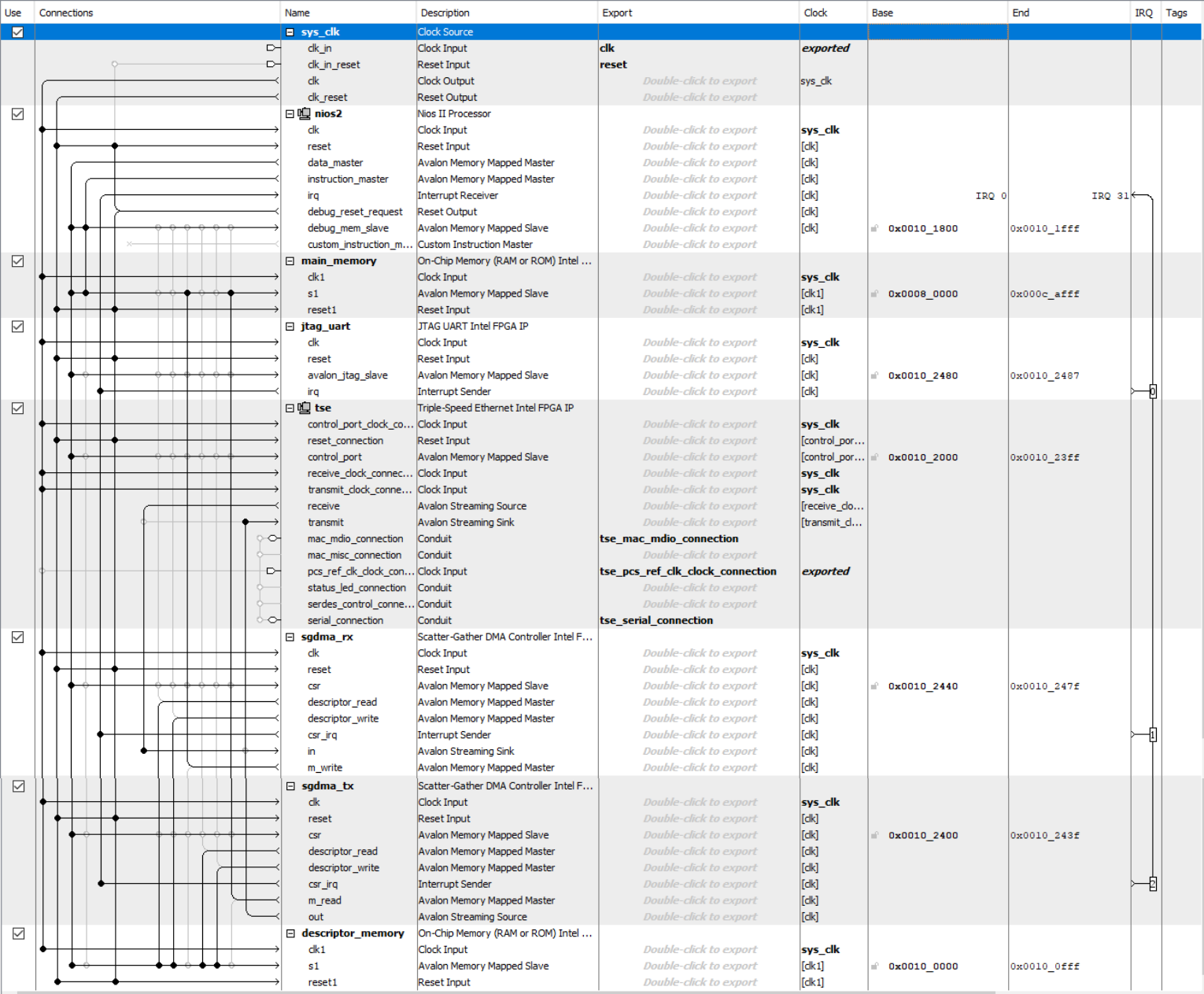

| Use | Name | Description | Export | Clock | Base | End | IRQ | Tags |
|---|---|---|---|---|---|---|---|---|
| ☑ | **sys_clk** | Clock Source | | | | | | |
| | clk_in | Clock Input | **clk** | ***exported*** | | | | |
| | clk_in_reset | Reset Input | **reset** | | | | | |
| | clk | Clock Output | *Double-click to export* | sys_clk | | | | |
| | clk_reset | Reset Output | *Double-click to export* | | | | | |
| ☑ | **nios2** | Nios II Processor | | | | | | |
| | clk | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | reset | Reset Input | *Double-click to export* | [clk] | | | | |
| | data_master | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | instruction_master | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | irq | Interrupt Receiver | *Double-click to export* | [clk] | | | IRQ 0 | IRQ 31 |
| | debug_reset_request | Reset Output | *Double-click to export* | [clk] | | | | |
| | debug_mem_slave | Avalon Memory Mapped Slave | *Double-click to export* | [clk] | 0x0010_1800 | 0x0010_1fff | | |
| | custom_instruction_m... | Custom Instruction Master | *Double-click to export* | | | | | |
| ☑ | **main_memory** | On-Chip Memory (RAM or ROM) Intel ... | | | | | | |
| | clk1 | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | s1 | Avalon Memory Mapped Slave | *Double-click to export* | [clk1] | 0x0008_0000 | 0x000c_afff | | |
| | reset1 | Reset Input | *Double-click to export* | [clk1] | | | | |
| ☑ | **jtag_uart** | JTAG UART Intel FPGA IP | | | | | | |
| | clk | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | reset | Reset Input | *Double-click to export* | [clk] | | | | |
| | avalon_jtag_slave | Avalon Memory Mapped Slave | *Double-click to export* | [clk] | 0x0010_2480 | 0x0010_2487 | | |
| | irq | Interrupt Sender | *Double-click to export* | [clk] | | | | 0 |
| ☑ | **tse** | Triple-Speed Ethernet Intel FPGA IP | | | | | | |
| | control_port_clock_co... | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | reset_connection | Reset Input | *Double-click to export* | [control_por... | | | | |
| | control_port | Avalon Memory Mapped Slave | *Double-click to export* | [control_por... | 0x0010_2000 | 0x0010_23ff | | |
| | receive_clock_connec... | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | transmit_clock_conne... | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | receive | Avalon Streaming Source | *Double-click to export* | [receive_do... | | | | |
| | transmit | Avalon Streaming Sink | *Double-click to export* | [transmit_d... | | | | |
| | mac_mdio_connection | Conduit | **tse_mac_mdio_connection** | | | | | |
| | mac_misc_connection | Conduit | *Double-click to export* | | | | | |
| | pcs_ref_clk_clock_con... | Clock Input | **tse_pcs_ref_clk_clock_connection** | ***exported*** | | | | |
| | status_led_connection | Conduit | *Double-click to export* | | | | | |
| | serdes_control_conne... | Conduit | *Double-click to export* | | | | | |
| | serial_connection | Conduit | **tse_serial_connection** | | | | | |
| ☑ | **sgdma_rx** | Scatter-Gather DMA Controller Intel F... | | | | | | |
| | clk | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | reset | Reset Input | *Double-click to export* | [clk] | | | | |
| | csr | Avalon Memory Mapped Slave | *Double-click to export* | [clk] | 0x0010_2440 | 0x0010_247f | | |
| | descriptor_read | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | descriptor_write | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | csr_irq | Interrupt Sender | *Double-click to export* | [clk] | | | | 1 |
| | in | Avalon Streaming Sink | *Double-click to export* | [clk] | | | | |
| | m_write | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| ☑ | **sgdma_tx** | Scatter-Gather DMA Controller Intel F... | | | | | | |
| | clk | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | reset | Reset Input | *Double-click to export* | [clk] | | | | |
| | csr | Avalon Memory Mapped Slave | *Double-click to export* | [clk] | 0x0010_2400 | 0x0010_243f | | |
| | descriptor_read | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | descriptor_write | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | csr_irq | Interrupt Sender | *Double-click to export* | [clk] | | | | 2 |
| | m_read | Avalon Memory Mapped Master | *Double-click to export* | [clk] | | | | |
| | out | Avalon Streaming Source | *Double-click to export* | [clk] | | | | |
| ☑ | **descriptor_memory** | On-Chip Memory (RAM or ROM) Intel ... | | | | | | |
| | clk1 | Clock Input | *Double-click to export* | **sys_clk** | | | | |
| | s1 | Avalon Memory Mapped Slave | *Double-click to export* | [clk1] | 0x0010_0000 | 0x0010_0fff | | |
| | reset1 | Reset Input | *Double-click to export* | [clk1] | | | | |