FPGA TECH SOLUTION

SOLUTION AHEAD

SPARTAN6 STARTER KIT

Campus FPGA Kit User Manual

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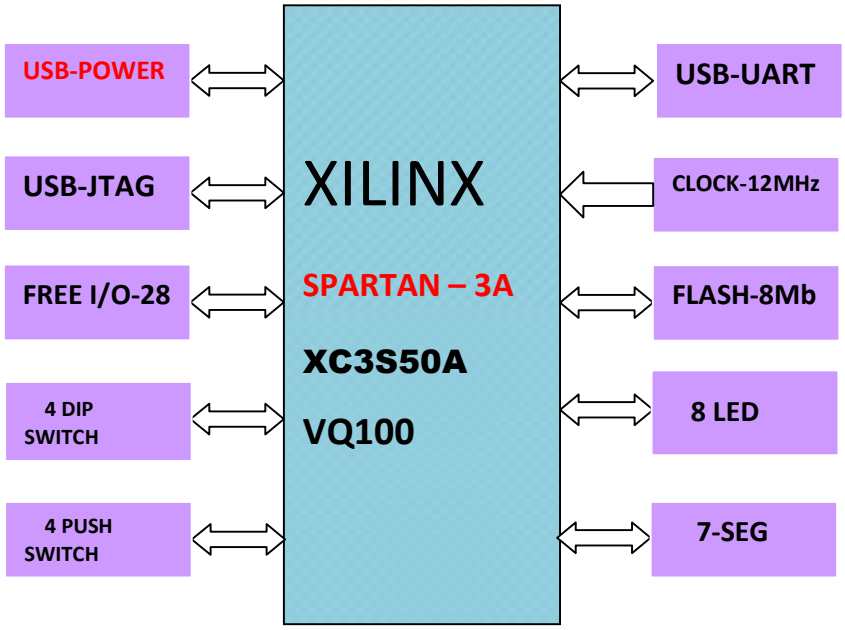
Key Features:

- **Spartan6-XC3S50A_VQ100 FPGA**
  - **Up to 82 user-I/O pins**
  - **VQ-100 package**

Key components:

- **XC3S50A_VQ00**
- **OSCILLATOR – 12MHz**
- **FLASH – M25P80**
- **USB Power**
- **On board USB Jtag**
- **USB to serial**
- **8 LED**
- **4 DIP SWITCHS**
- **4 PUSH BUTTONS**
- **28 user I/O**
- **4 seven-Seg**



BOARD POWERING

The **CAMPUS FPGA** can work on USB power you can also connect external 5VDc. supply. When **JP2** jumper is placed in 2 & 3 power is used from USB connector. When **JP2** jumper is placed in 1 & 2 power is used from external power adaptor

LED's and DIP Switches Interface

The **CAMPUS FPGA** board has 8 individual LED & 4 DIP switches. A LED is assigned to each I/O to indicate its data status when I/O is configured as output. DIP switch is used to provide digital input (i.e. logic 0 and logic 1).

Pin Assignment (UCF Location) for IOs:

Slide Switch	XC6SLX9	Active
SW0	P20	LOW
SW1	P19	LOW
SW2	P41	LOW
SW3	P44	LOW

LED	XC6SLX9	Active
TL1	P33	HIGH
TL2	P34	HIGH
TL3	P35	HIGH
TL4	P36	HIGH
TL5	P37	HIGH
TL6	P40	HIGH
TL7	P49	HIGH
TL8	P50	HIGH

Seven segments Interface

The **CAMPUS FPGA** board includes 3 common anode seven segment displays

seven segments	XC6SLX9
SIG_A	P15
SIG_B	P16
SIG_C	P28
SIG_D	P52
SIG_E	P56
SIG_F	P59
SIG_G	P57
SIG_PD	P32
SEL_DISP1	P31
SEL_DISP2	P30
SEL_DISP3	P29

Pushbuttons Interface

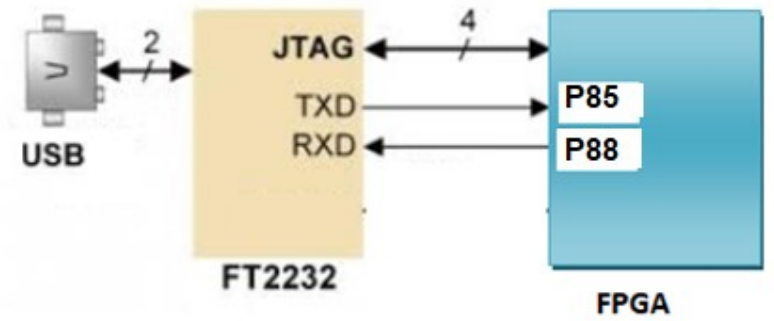
The **CAMPUS FPGA** board has 4 individual pushbuttons for input purpose. The pushbuttons are read as 0 when pushed. They are read as 1 in normal (Unpressed) condition. Pushbuttons are labeled as SW1 TO SW4.

Pin Assignment (UCF Location) for Pushbuttons:

Signal Name	XC6SLX9	Active
SW1	P39	**LOW**
SW2	P24	**LOW**
SW3	P7	**LOW**
SW4	P21	**LOW**

USB Interface

The **CAMPUS FPGA** board have USB interface using device FT2232HL from FTDI. This act as USB to UART converter so that Communication with FPGA can accomplished by USB port.



Pin Assignment (UCF Location) for USB interface:

Signal Name	XC6SLX9
USB_Rx	P88
USB_TX	P85

Clock Sources

The **CAMPUS FPGA** supports clock input sources which are listed below.
The board includes an on-board 12 MHz clock oscillator

Signal Name	XC6SLX9
Clock 12Mhz	P86

FREE INPUT OUTPUT

The **CAMPUS FPGA** board has seven free input output connectors. Each connector have 8 input output pins, 3.3V Dc pin and GND pin.

J6	FPGA
1	3.3V
2	89
3	90
4	93
5	94
6	98
7	99
8	3
9	4
10	5
11	6
12	9
13	10
14	12
15	13
16	GND

J5	FPGA
1	3.3V
2	85
3	84
4	83
5	78
6	77
7	73
8	72
9	71
10	70
11	65
12	64
13	62
14	61
15	60
16	GND