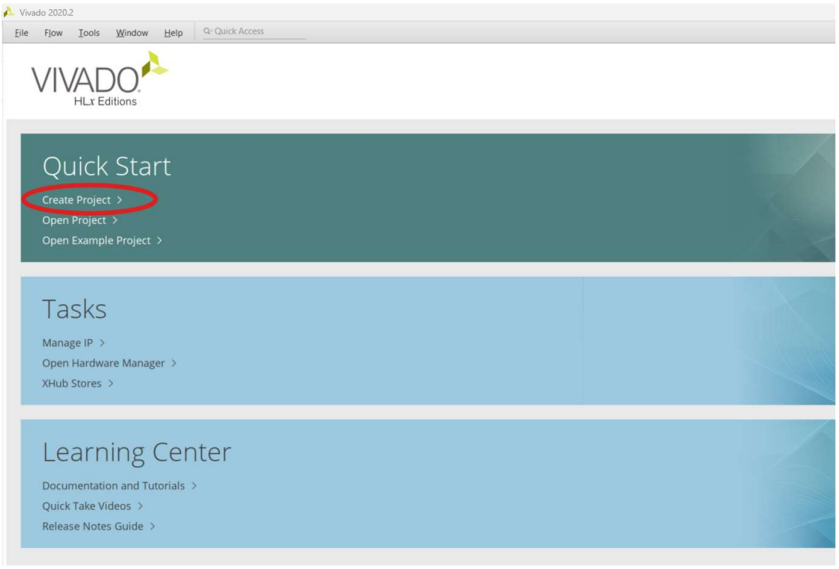
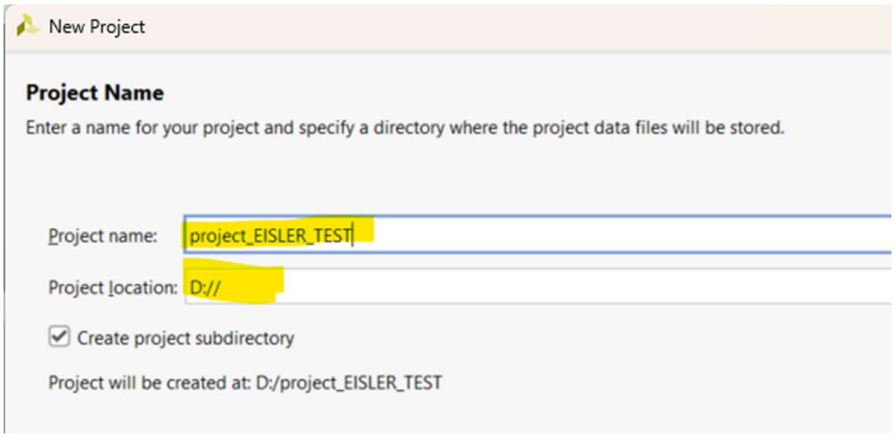
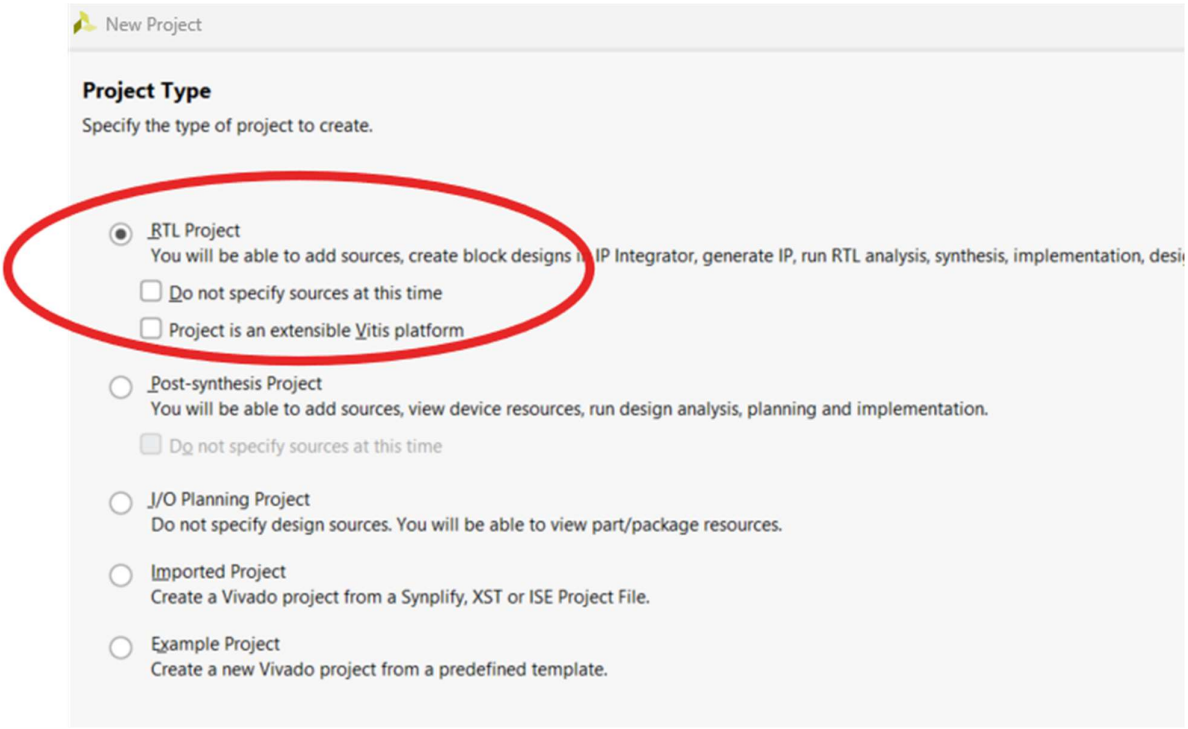
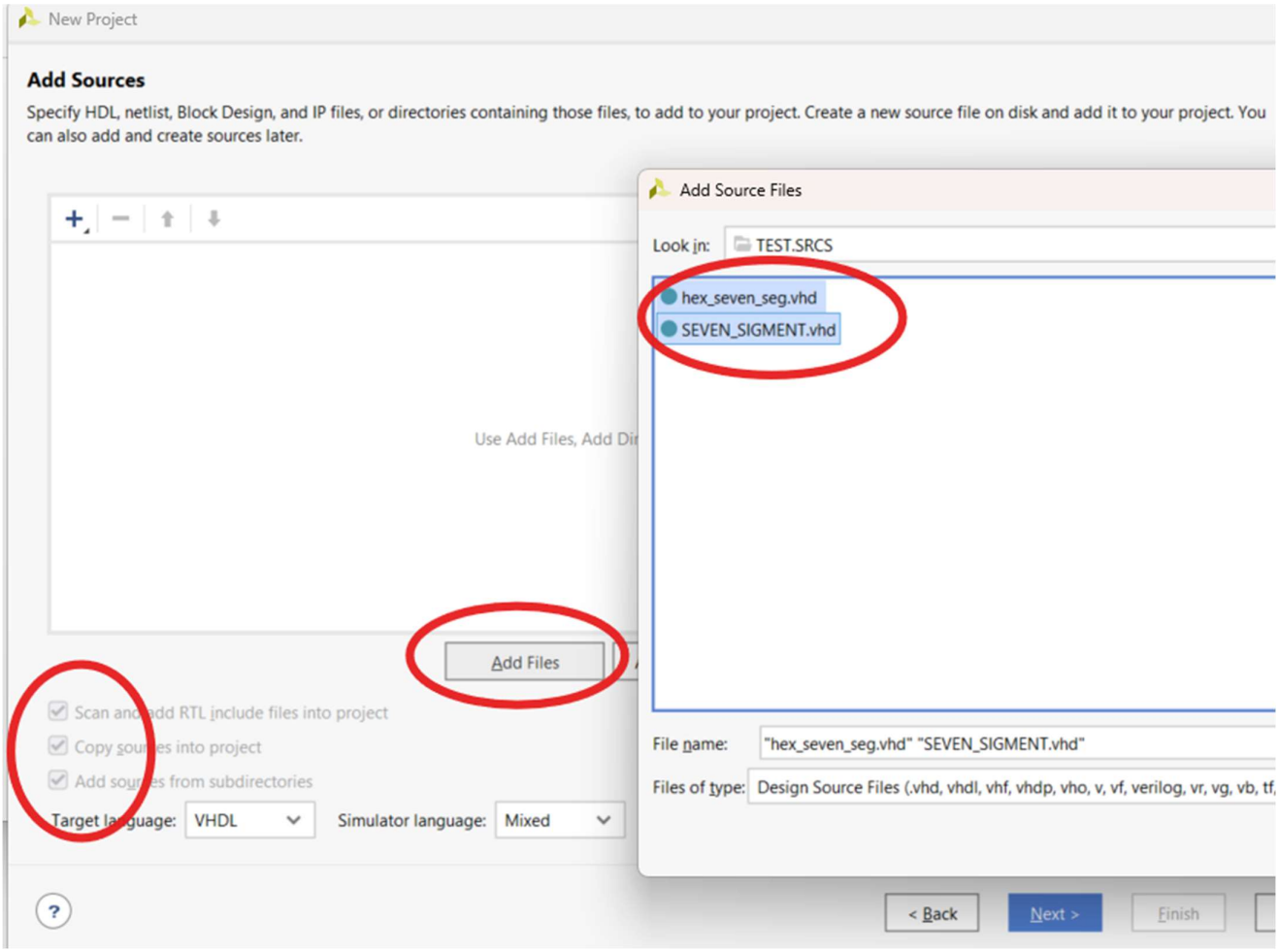
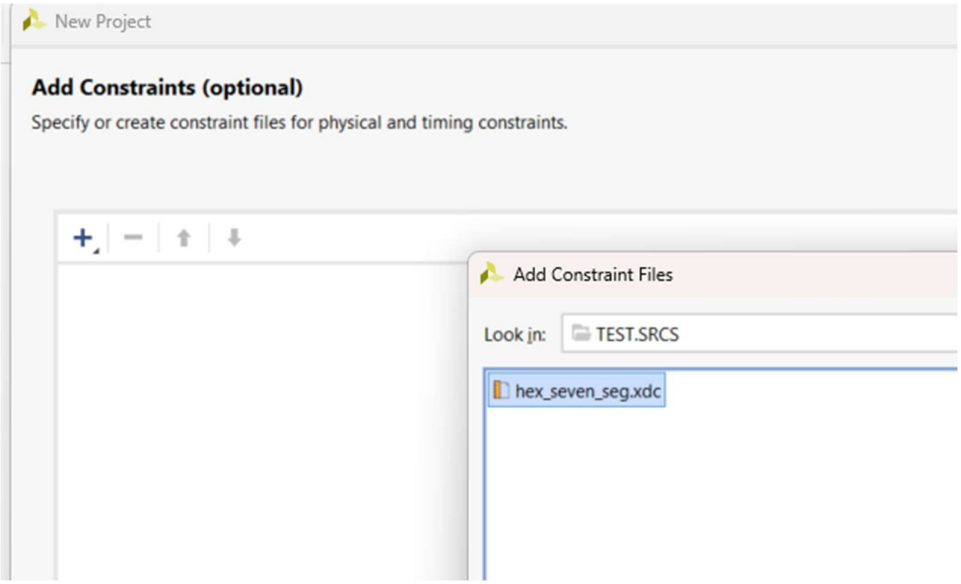
Getting started with Vivado design suite for EISLER Artix-7 FPGA Board


Vivado 2020.2
File Flow Tools Window Help
Quick Access
VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide

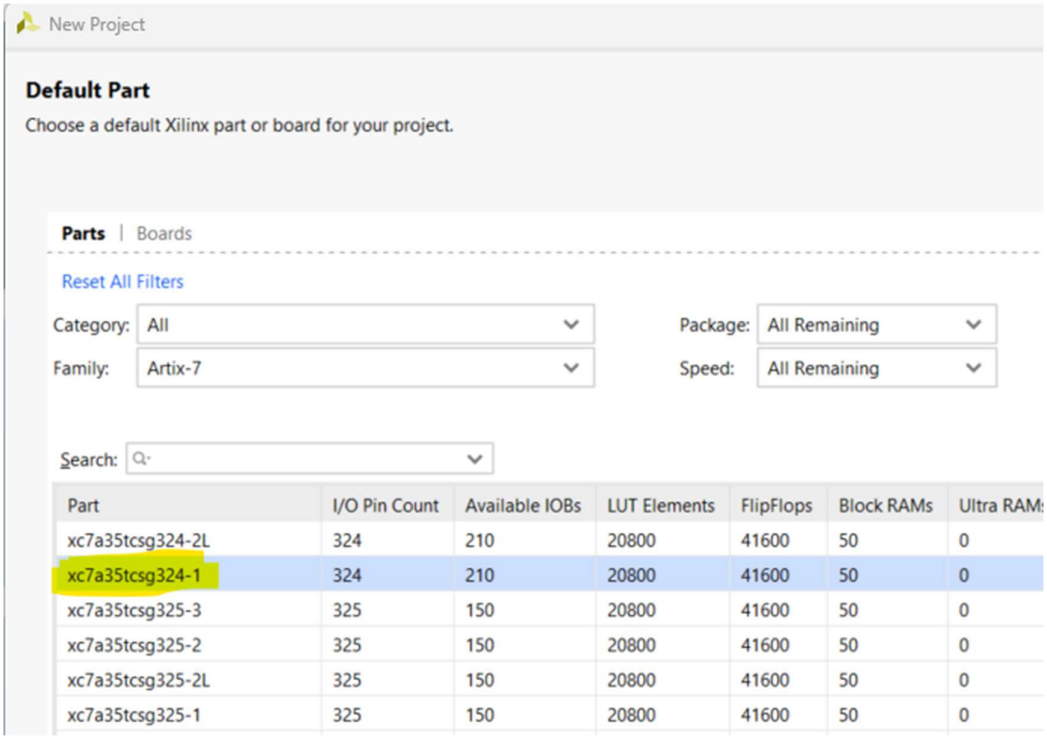

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
project_EISLER_TEST
Project location:
D:/
Create project subdirectory
Project will be created at: D:/project_EISLER_TEST


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, desi
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.

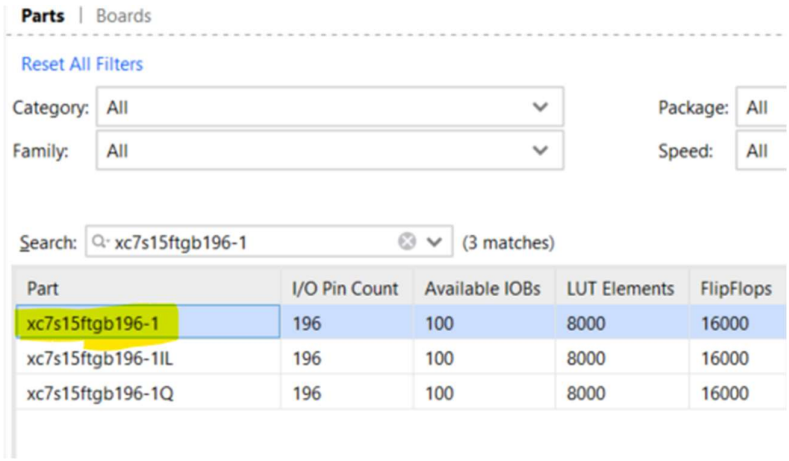

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Di
Add Files
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: Mixed
Add Source Files
Look in: TEST.SRCS
hex_seven_seg.vhd
SEVEN_SIGMENT.vhd
File name: "hex_seven_seg.vhd" "SEVEN_SIGMENT.vhd"
Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verilog, vr, vg, vb, tf,
< Back
Next >
Finish

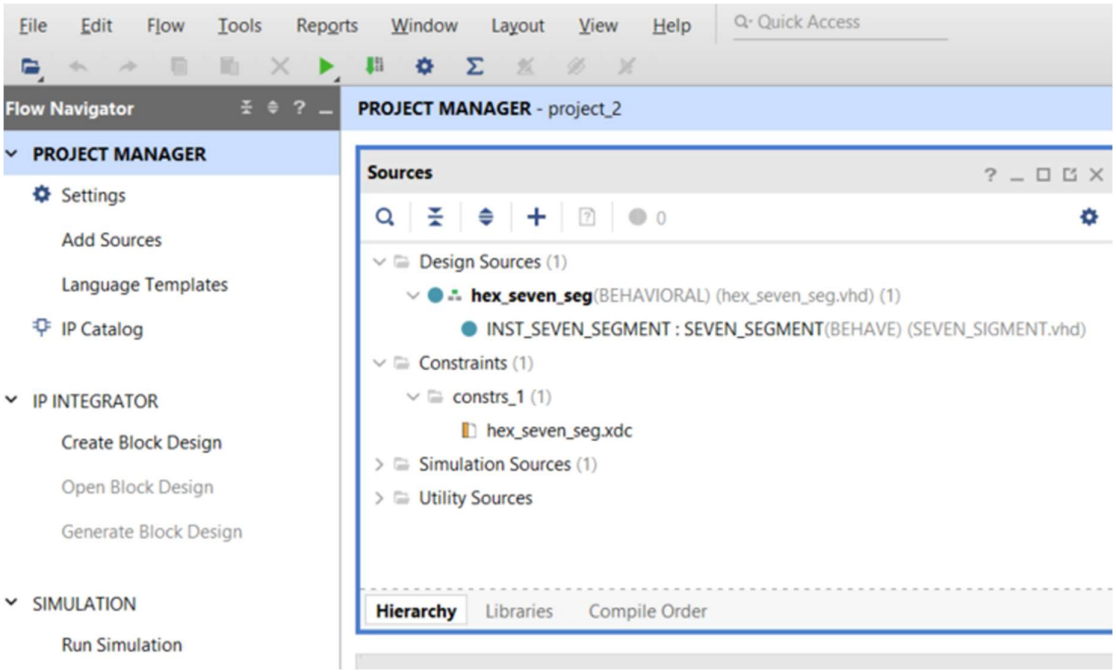


FOR EISLER ARTIX 7 FPGA BOARD



FOR PINE SPARTAN7 FPGA BOARD


Parts | Boards
Reset All Filters
Category: All
Family: All
Package: All
Speed: All
Search: xc7s15ftgb196-1
(3 matches)
Part
I/O Pin Count
Available IOBs
LUT Elements
FlipFlops
xc7s15ftgb196-1
196
100
8000
16000
xc7s15ftgb196-1IL
196
100
8000
16000
xc7s15ftgb196-1Q
196
100
8000
16000


File
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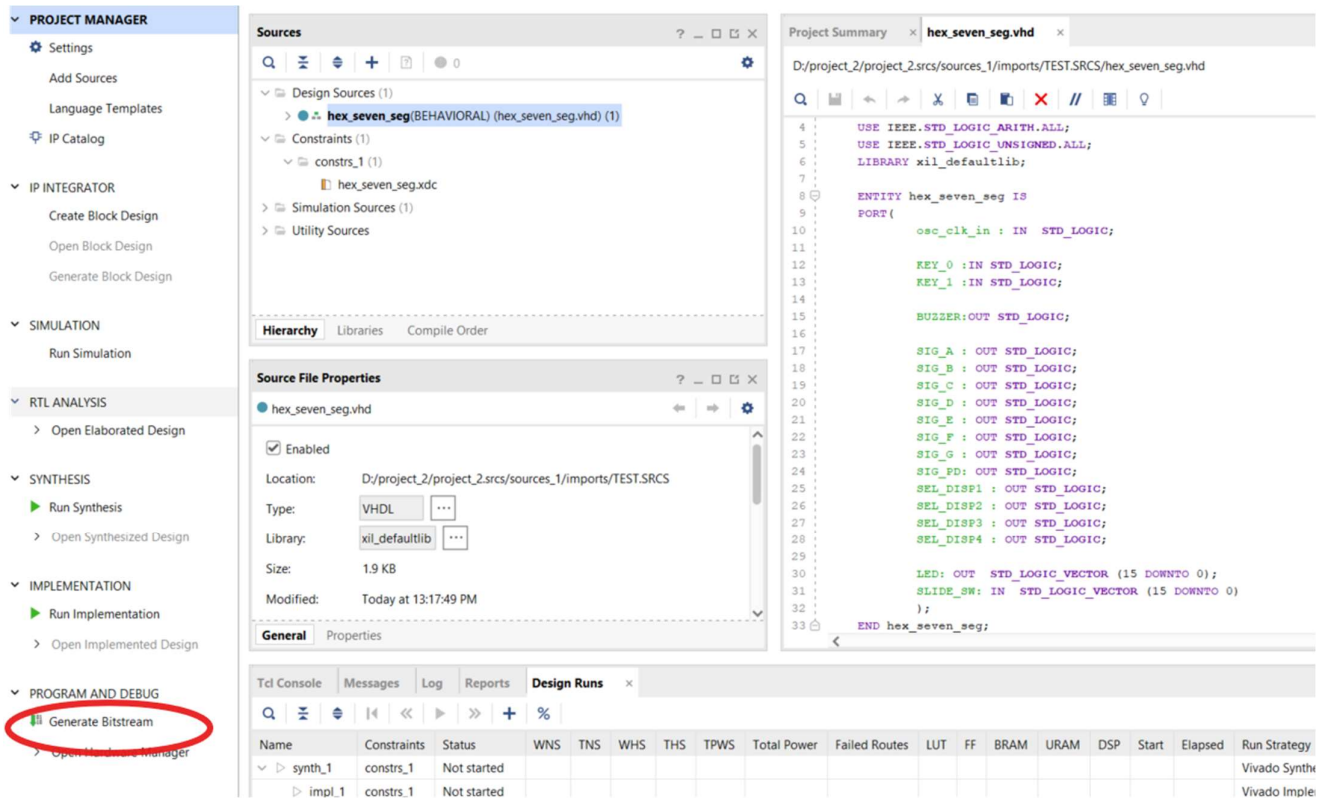
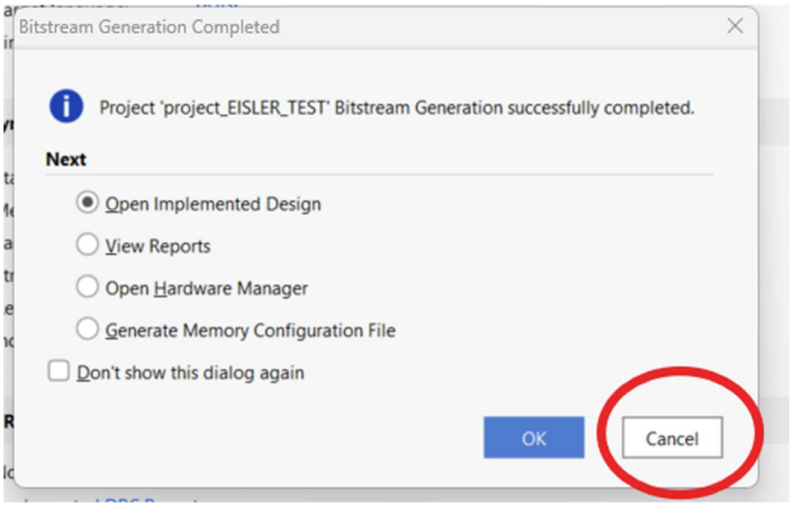
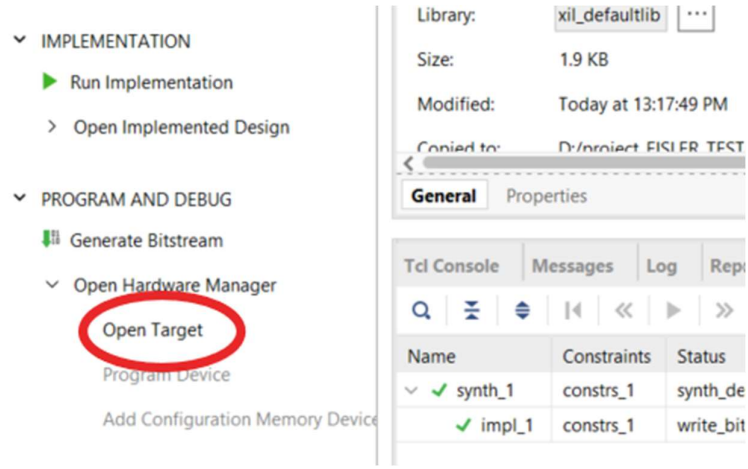
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
PROJECT MANAGER - project_2
Sources
Design Sources (1)
hex_seven_seg(BEHAVIORAL) (hex_seven_seg.vhd) (1)
INST_SEVEN_SEGMENT : SEVEN_SEGMENT(BEHAVE) (SEVEN_SIGMENT.vhd)
Constraints (1)
constrs_1 (1)
hex_seven_seg.xdc
Simulation Sources (1)
Utility Sources
Hierarchy
Libraries
Compile Order

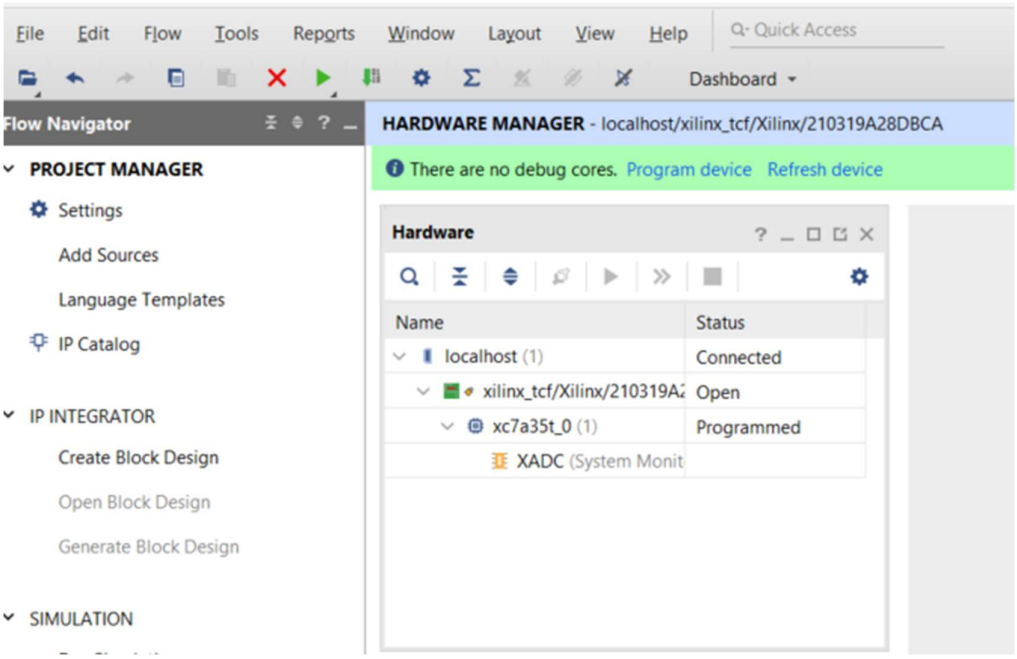




Open Hardware Manager

Make sure board is powered on & USB connector is connected to computer properly


IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Device
Library:
xil_defaultlib
Size:
1.9 KB
Modified:
Today at 13:17:49 PM
General
Properties
Tcl Console
Messages
Log
Name
Constraints
Status
synth_1
constrs_1
synth_de
impl_1
constrs_1
write_bit


File
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PROJECT MANAGER
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Language Templates
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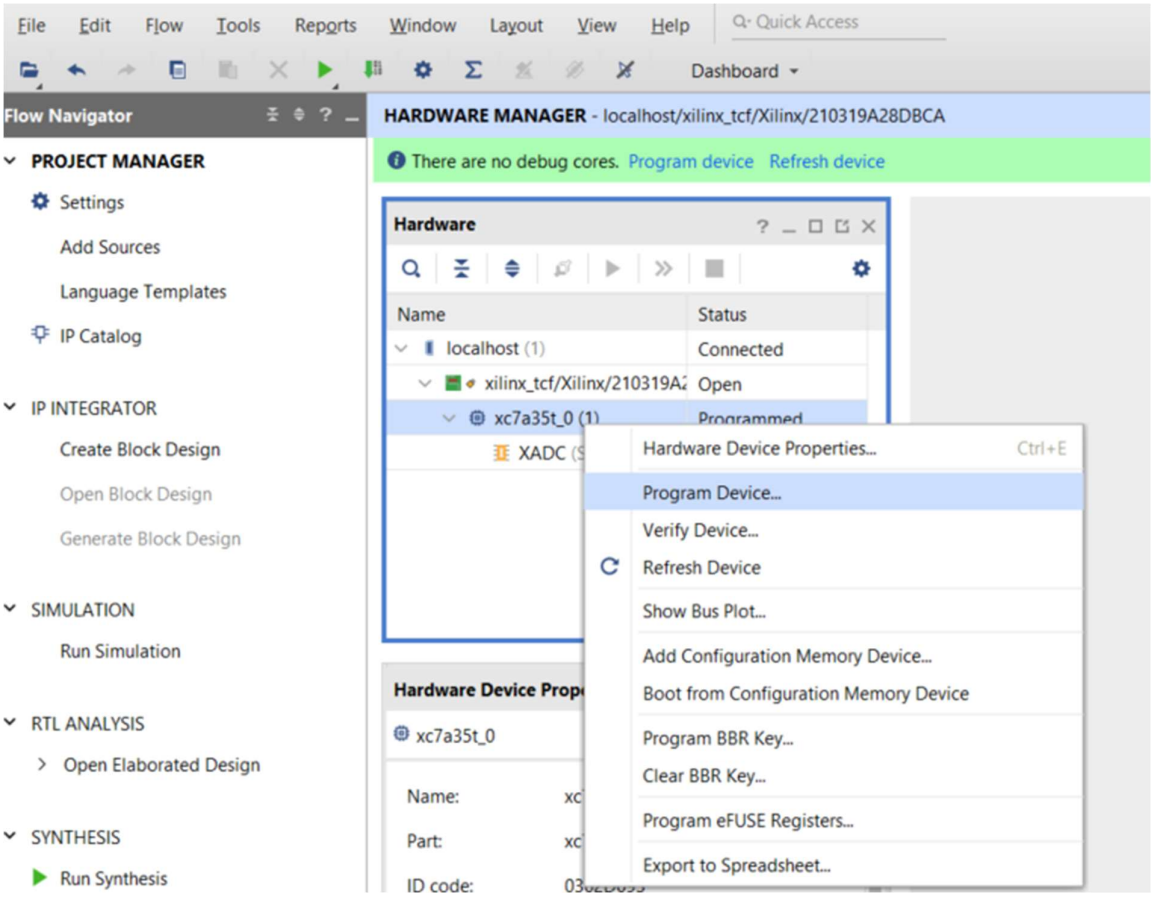
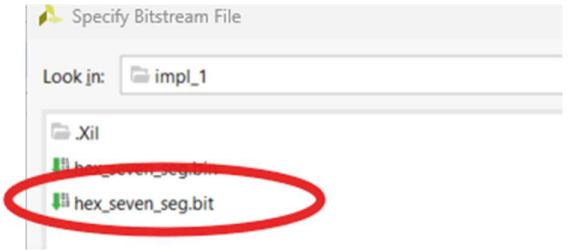
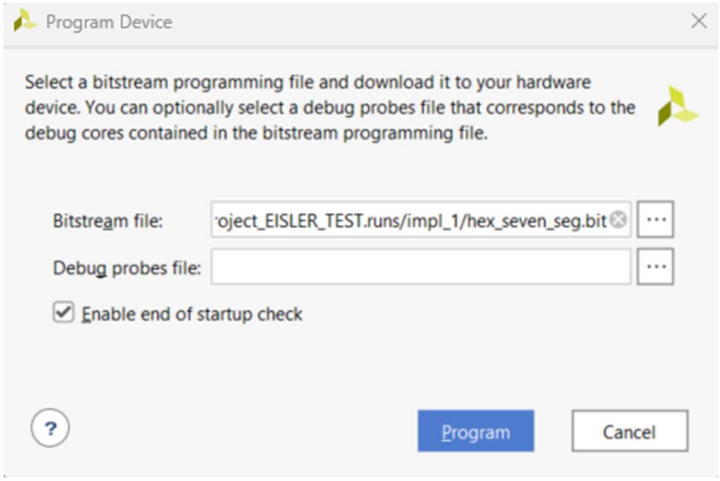
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/210319A28DBCA
There are no debug cores. Program device
Refresh device
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Xilinx/210319A
Open
xc7a35t_0 (1)
Programmed
XADC (System Monit



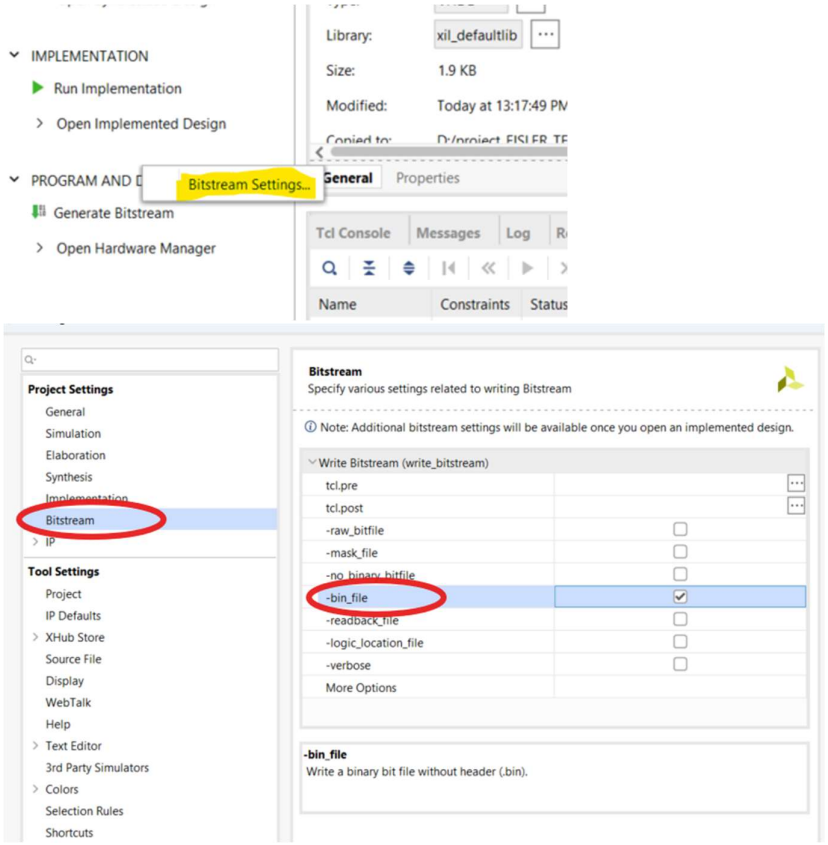
In runs/impl/ folder

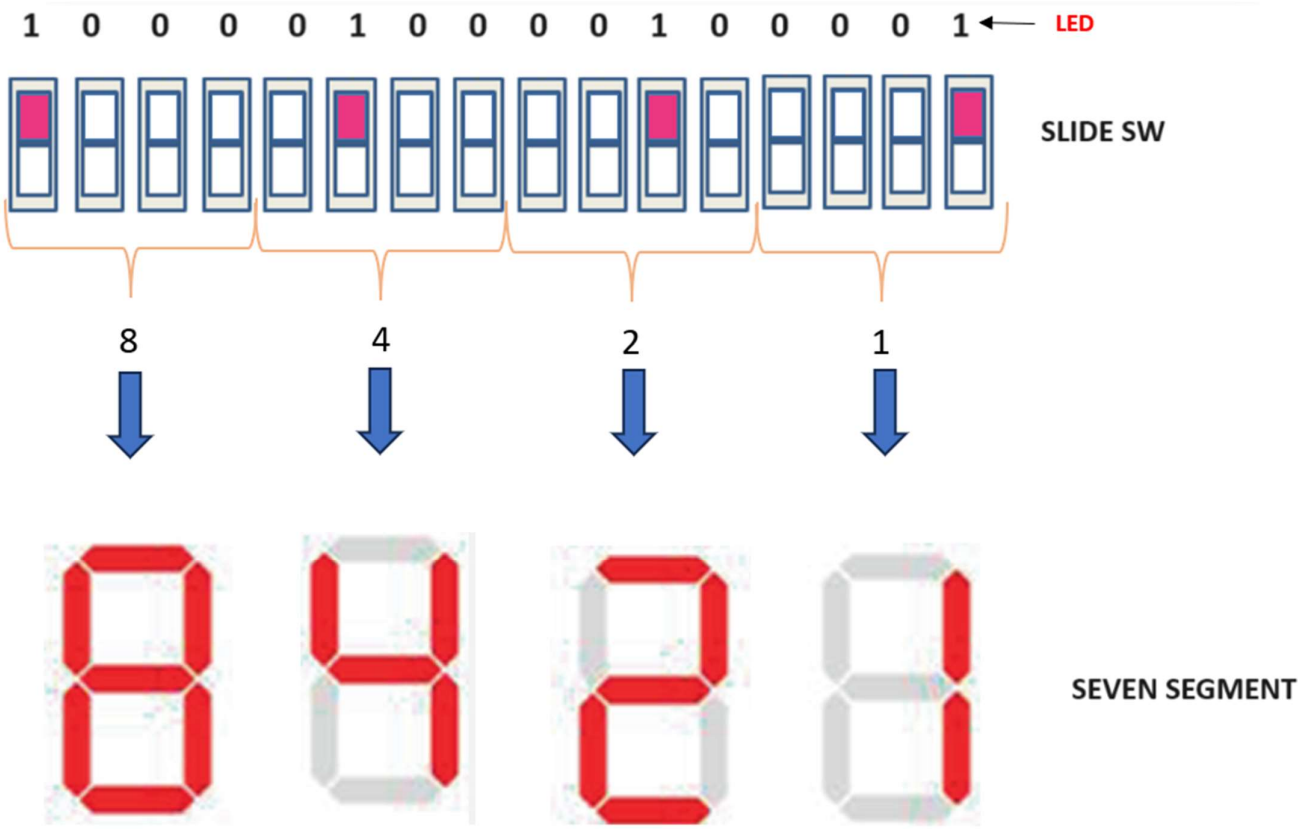




Now check output on board

How To program flash attached to FPGA




1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1
LED
SLIDE SW
8
4
2
1
SEVEN SEGMENT