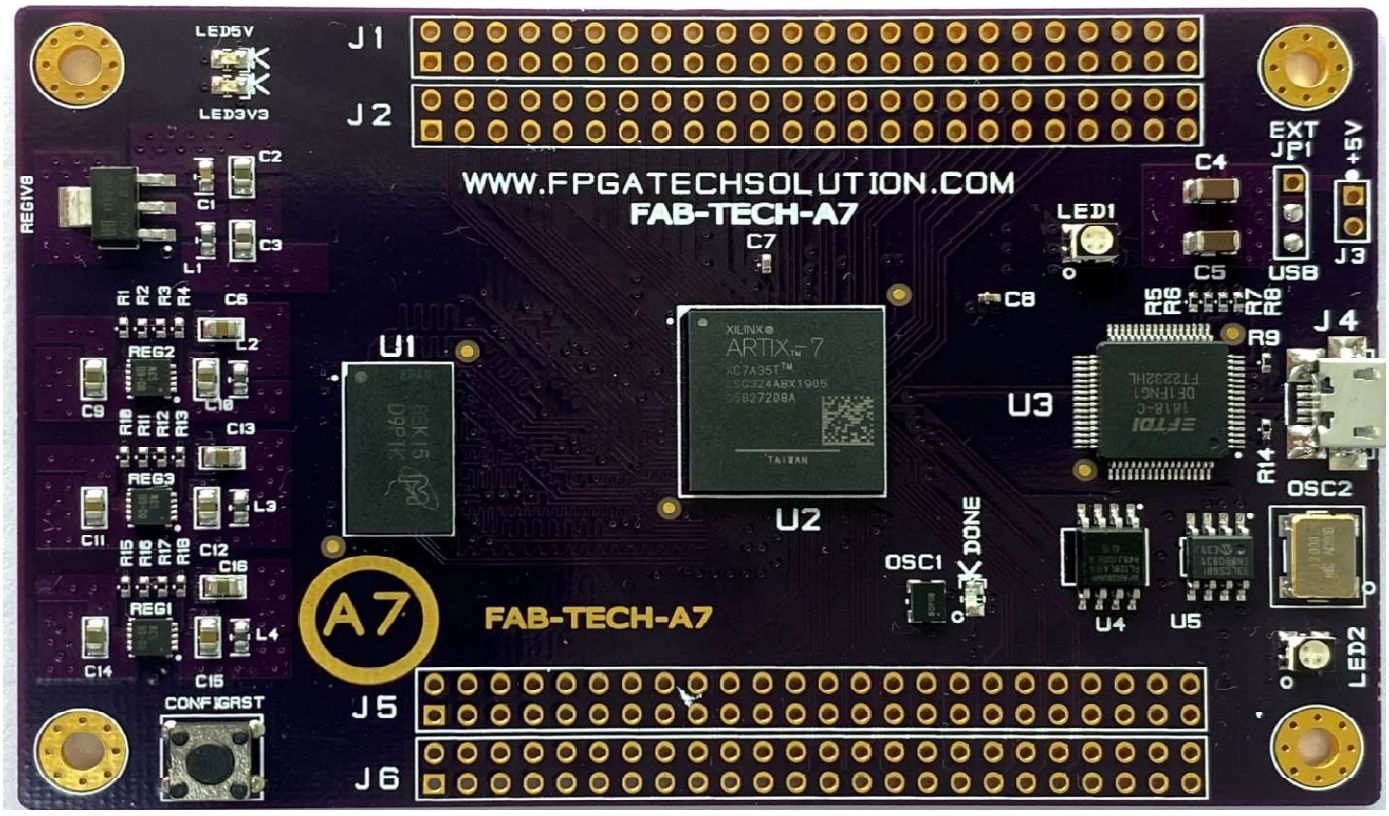
# Fabulous Technology ARTIX 7 FPGA

FPGA TECH SOLUTION

SOLUTION AHEAD



# Introduction

**Fab-Tech-A7 is an easy to use FPGA Development board featuring Artix 7 FPGA (XC7A35T – CFG324 package) with FTDI's FT2232H Dual-Channel USB device, which support Xilinx Vivado, SDK & Vitis to program FPGA. It is specially designed for the development and integration of FPGA based accelerated features to other designs. This board works with USB power however provision is given for external 5V power supply**

**Note: This FPGA Development board is fully compatible with Vivado, EDK, SDK, Vitis, System Generator and ChipscopePro Tools at ease with on-board USB JTAG Interface.**

# Features

- **Device: Xilinx Artix 7 FPGA (XC7A35T- CFG324)**
- **DDR3: 2Gb DDR3 (MT41J128M16JT-125 or equivalent)**
- **SPI FLASH 128Mb(S25FL128L) for FPGA configuration storage and custom user data storage FPGA configuration via JTAG and USB**
- **100MHz CMOS oscillator**
- **2 RGB LED**
- **Maximum 142 IOs for user-defined purposes(71 Differential Pairs)**
- **High-Speed USB 2.0 interface for On-board flash programming. FT2232H Channel Ais dedicated for JTAG Programming. Channel B can be used as USB to serial convertor**
- **Built-in programming interface. No expensive JTAG adapters needed for programming the board**

# Applications

- **Product Prototype Development**
- **Development and testing of custom embedded processors**
- **Signal Processing**
- **Communication devices development**
- **Educational tool for Schools and Universities**

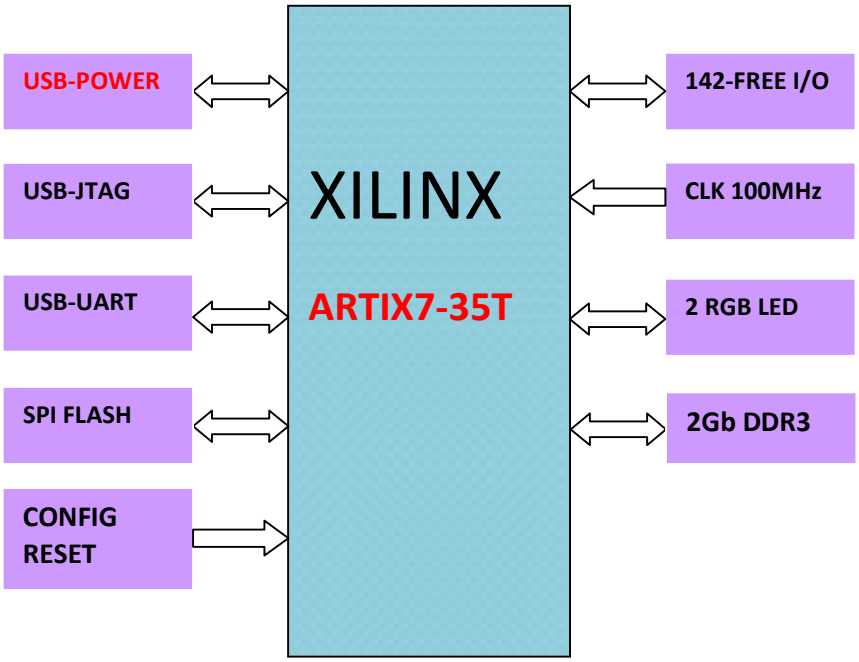
**Board Features:**

**Artix7- XC7A15T/35T/75T/50T/100T**

- **Up to 142 user-I/O pins**
- **CSG-324 package**

## Key components:

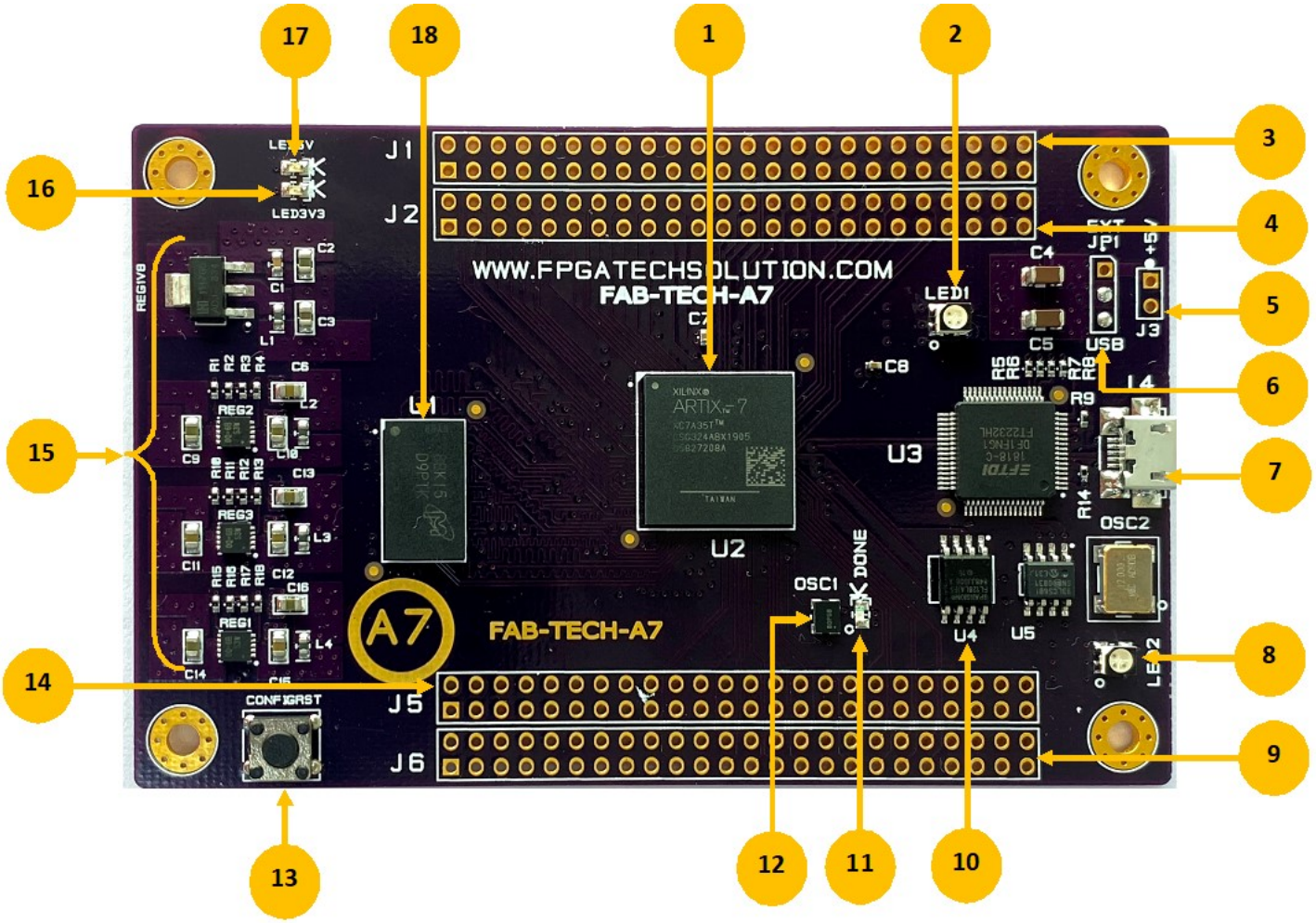
- **Artix7- XC7A35T**
- **2Gb DDR3**
- **OSCILLATOR – 100MHz**
- **SPI FLASH 128Mb**
- **USB POWER**
- **On board USB JTAG**
- **USB to SERIAL**
- **2 RGB – LED**
- **Size 87mm X 105mm**




**Note: This FPGA Development board is fully compatible with Vivado, EDK, SDK, Vitis, System Generator and ChipscopePro Tools at ease with on-board USB JTAG Interface.**

**On request this board can be available with following FPGA**

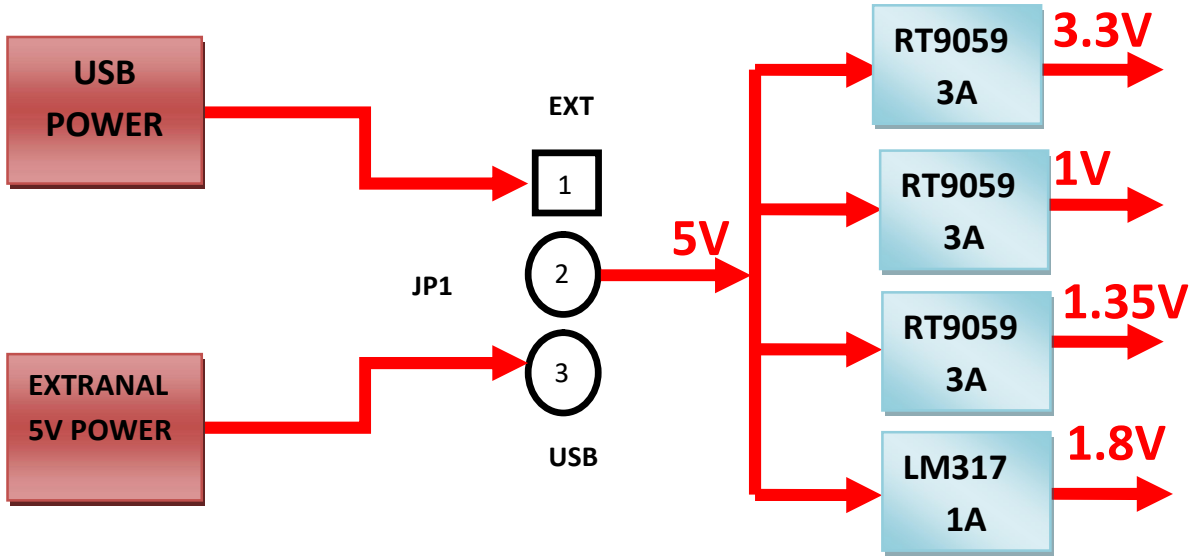
**XC7A15T-1CSG324C**
**XC7A35T-1CSG324C**
**XC7A75T-1CSG324C**
**XC7A100T-1CSG324C**

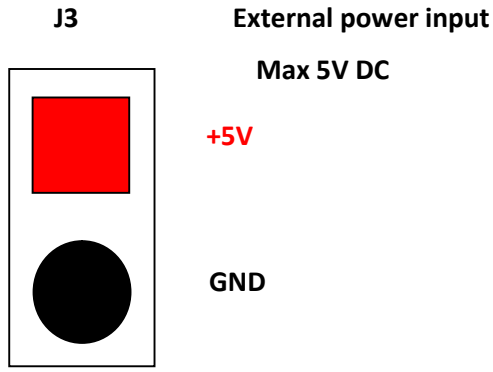



| Callout | Description | Callout | Description |
|---|---|---|---|
| 1 | Artix FPGA | 10 | SPI Flash |
| 2 | User Tri color LEDs | 11 | FPGA programming DONE LED |
| 3 | User GPIO header | 12 | 100Mhz Oscillator |
| 4 | User GPIO header | 13 | FPGA Configuration reset button |
| 5 | Power jack (for optional ext. supply) | 14 | User GPIO header |
| 6 | Power select jumper (Ext. supply / USB) | 15 | Power supply Circuit |
| 7 | Shared USB JTAG / UART port | 16 | Power supply LED for 3.3V |
| 8 | User Tri color LEDs | 17 | Power supply LED for 5V |
| 9 | User GPIO header | 18 | DDR3 memory |

## BOARD POWERING

The FAB-TECH-A7 uses +5V power supply to function properly. By default the board is configured to use +5V supply from USB, So an external +5V power is not required unless USB port is unable to supply enough current. In most cases USB ports are capable of providing enough current for the module. Current requirement for this board largely depends on your application. Please consult FPGA data sheet for more details on power requirements. If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly as shown below When JP1 jumper is placed towards USB as shown in below image power is used from USB connector & when JP1 jumper is placed towards power connector power is used from external connector

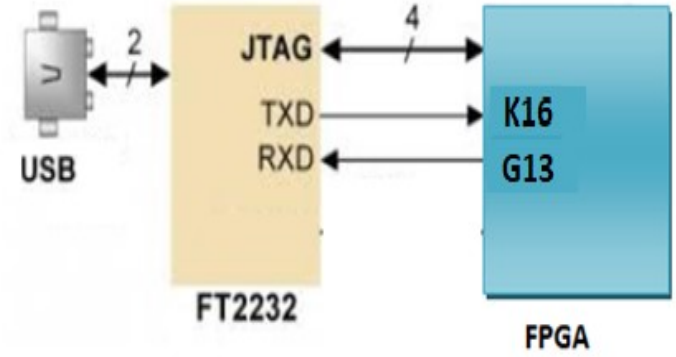


# JTAG Configuration

The Xilinx tools typically communicate with FPGAs using the Test Access Port and Boundary-Scan Architecture, commonly referred to as JTAG. During JTAG programming, a .bit file is transferred from the PC to the FPGA using the onboard USB-JTAG circuitry . You can perform JTAG programming any time after the Board has been powered on, regardless of whether the mode pin. If the FPGA is already configured, then the existing configuration is overwritten with the bitstream being transmitted over JTAG. For this board by default mode pin are fixed to use FPGA from being configured from Quad-SPI Flash until a JTAG programming occurs.

Programming the board with an uncompressed bitstream using the on-board USB-JTAG circuitry usually takes around 6 seconds. JTAG programming can be done using the hardware manager in Vivado or the iMPACT tool included with ISE.

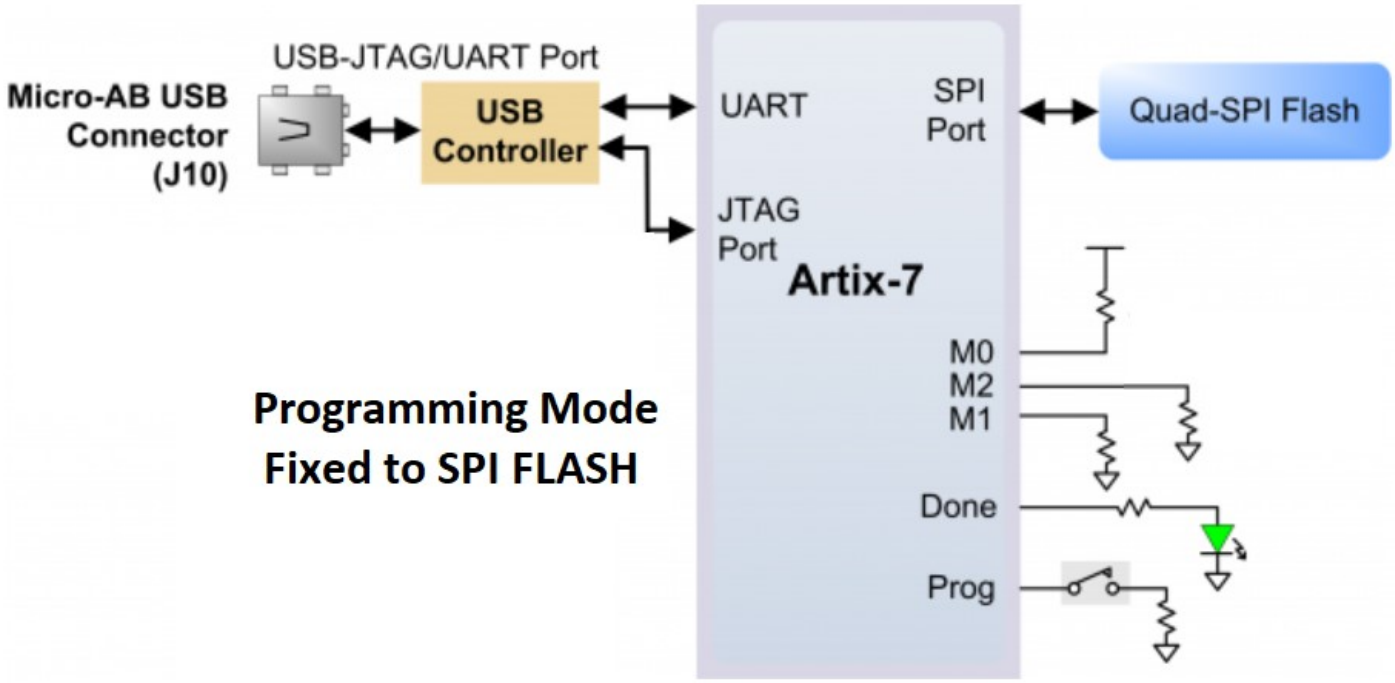


# Quad-SPI Configuration

Since the FPGA's memory on the Fab-Tech-A7 is volatile, it relies on the Quad-SPI flash memory to store the configuration between power cycles. This configuration mode is called Master SPI. The blank FPGA takes the role of master and reads the configuration file out of the flash device upon power-up. To that effect, a configuration file needs to be downloaded first to the flash. When programming a nonvolatile flash device, a bitstream file is transferred to the flash in a two-step process. First, the FPGA is programmed with a circuit that can program flash devices, and then data is transferred to the flash device via the FPGA circuit (this complexity is hidden from the user by the Xilinx tools). This is called indirect programming. After the flash device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the mode pins. Programming files stored in the flash device will remain until they are overwritten, regardless of power-cycle events.

Programming the flash can take as long as four to five minutes, which is mostly due to the lengthy erase process inherent to the memory technology. Once written however, FPGA configuration can be very fast—less than a second. Bitstream compression, SPI bus width, and configuration rate are factors controlled by the Xilinx tools that can affect configuration speed. This board supports x1, x2, and x4 bus widths and data rates of up to 50 MHz for Quad-SPI programming.

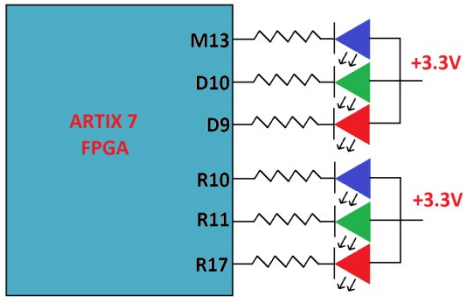
Quad-SPI programming can be done using the hardware manager in Vivado or with the iMPACT tool included with ISE.



## LED's Interface

**FAB-TECH-A7** board contains two tri-color LEDs. Each tri-color LED has three input signals that drive the cathodes of three smaller internal LEDs: one red, one blue, and one green. Driving the signal corresponding to one of these colors high will illuminate the internal LED. The input signals are driven by the FPGA which inverts the signals. Therefore, to light up the tri-color LED, the corresponding signals need to be driven low. The tri-color LED will emit a color dependent on the combination of internal LEDs that are currently being illuminated. For example, if the red and blue signals are driven high and green is driven low, the tri-color LED will emit a purple color.

we strongly recommends the use of pulse-width modulation (PWM) when driving the tri-color LEDs. Driving any of the inputs to a steady logic '1' will result in the LED being illuminated at an uncomfortably bright level. You can avoid this by ensuring that none of the tri-color signals are driven with more than a 50% duty cycle. Using PWM also greatly expands the potential color palette of the tri-color led. Individually adjusting the duty cycle of each color between 50% and 0% causes the different colors to be illuminated at different intensities, allowing virtually any color to be displayed.



# Oscillators/Clocks

**FAB-TECH-A7** board includes a single 100 MHz crystal oscillator connected to pin P17 (P17 is a MRCC input on bank 14). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100 MHz input clock. For a full description of these rules and of the capabilities of the Artix-7 clocking resources, refer to the “7 Series FPGAs Clocking Resources User Guide” available from Xilinx.

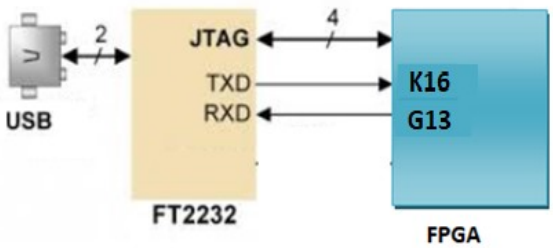
Xilinx offers the Clocking Wizard IP core to help users generate the different clocks required for a specific design. This wizard will properly instantiate the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy-to-use wrapper component around these clocking resources that can be inserted into the user’s design. The clocking wizard can be accessed from within the Project Navigator or Core Generator tools.

## USB-UART Bridge (Serial Port)

The **FAB-TECH-A7** includes an FTDI FT2232HL USB-UART bridge that allows you use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the “Virtual Com Port” or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the K16 and G13 FPGA pins.

The FT2232HL is also used as the controller for the USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the Arty to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable.

The connections between the FT2232HL and the Artix-7 are shown in Figure



# Memory

The **FAB-TECH-A7** board contains two external memories: a 2Gb DDR3 SDRAM and a 128Mb (16MB) non-volatile serial Flash device. The DDR3L module is connected to the FPGA using the industry standard interface. The serial Flash is on a dedicated quad-mode (x4) SPI bus. The connections and pin assignments between the FPGA and external memories are shown below.

## DDR3L

The **FAB-TECH-A7** includes one MT41K128M16JT-125 memory component, creating a single rank, 16-bit wide interface. It is routed to a 1.35V-powered HR (High Range) FPGA bank with 50 ohm controlled single-ended trace impedance. 50 ohm internal terminations in the FPGA are used to match the trace characteristics. Similarly, on the memory side, on-die terminations (ODT) are used for impedance matching.

For proper operation of the memory, a memory controller and physical layer (PHY) interface needs to be included in the FPGA design. The easiest way to accomplish this on the Fab-Tech-A7 is to use the Xilinx 7-series memory interface solutions core generated by the MIG (Memory Interface Generator) Wizard. Depending on the tool used (ISE, EDK or Vivado), the MIG Wizard can generate a native FIFO-style or an AXI4 interface to connect to user logic. This workflow allows the customization of several DDR parameters optimized for the particular application. Table 2 below lists the MIG Wizard settings optimized for the **FAB-TECH-A7**.

| DDR3L settings for FAB-TECH-A7 | |
|---|---|
| **Setting** | **Value** |
| Memory type | DDR3 SDRAM |
| Max. clock period | 3000ps (667Mbps data rate) |
| Memory part | MT41K128M16JT-125 |
| Memory Voltage | 1.35V |
| Data width | 16 |
| Data mask | Enabled |
| Recommended Input Clock Period | 6000 ps (166.667 MHz) |
| Output Driver Impedance Control | RZQ/6 |
| Controller Chip Select pin | Enabled |
| Rtt (nominal) – On-die termination | RZQ/6 |
| Internal Vref | Enabled |
| Internal termination impedance | 50ohms |

The MIG Wizard will require the fixed pin-out of the memory signals to be entered and validated before generating the IP core. For your convenience, an importable UCF file is provided on the **FAB-TECH-A7** resource center to speed up this process. It is included in the “MIG Project” design resource download. This download also includes a .prj file that can be imported into the wizard to automatically configure it with the options found in Table 2.

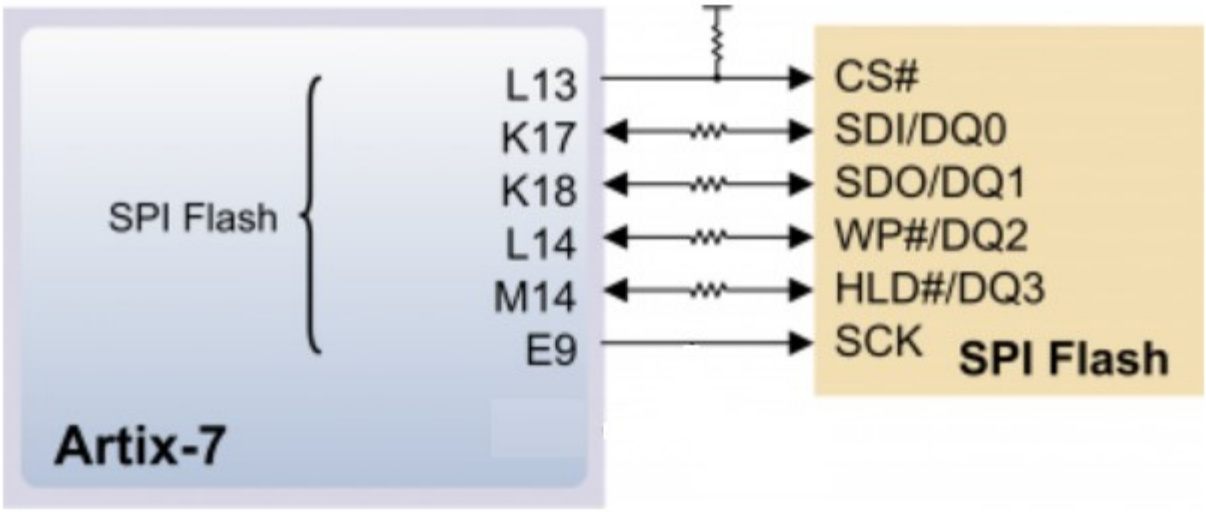
For more details on the Xilinx MIG, refer to the 7 Series FPGAs Memory Interface Solutions User Guide (ug586).

### Quad-SPI Flash

FPGA configuration files can be written to the Quad-SPI Flash S25FL128L ,and setting the mode jumper will cause the FPGA to automatically read a configuration from this device at power on. An Artix-7 35T configuration file requires 17,536,096 bits of memory, leaving about 87% of the flash device (or ~14MB) available for user data. A common use for this extra memory is to store Microblaze programs too big to fit in the onboard Block memory (typically 128 KB). These programs are then loaded and executed using a smaller bootloader program that can fit in the block memory. It is possible to automatically generate this bootloader, roll it into a single file (called an .mcs file) that also contains the bitstream and your custom Microblaze application, and program this file into SPI Flash using Xilinx SDK and Vivado. Xilinx Answer Record 63605 explains how to do this.

The contents of the memory can be manipulated by issuing certain commands on the SPI bus. The implementation of this protocol is outside the scope of this document. All signals in the SPI bus are general-purpose user I/O pins after FPGA configuration. On other boards, SCK is an exception because it remains a dedicated pin even after configuration, however, on Fab-Tech-A7 the SCK signal is routed to an additional general purpose pin that can be accessed after configuration (see Figure below). This allows access to this pin without having to instantiate the special FPGA primitive called STARTUPE2.

Xilinx's AXI Quad SPI core can be used to read/write the flash in a Microblaze design. Refer to Xilinx's product guide for this core to learn more about using it.



## FREE INPUT OUTPUT

The **FAB-TECH-A7** board has total 140 user I/O placed four input output connectors.

**All pin can work with maximum 3.3V DC**

# GPIO connector J1 48 pin connection as follows

| J1 | | | | | |
|---|---|---|---|---|---|
| 1 | 5V | 5V | 2 | 5V | 5V |
| 3 | LVDS_IO_P_1 | K2 | 4 | LVDS_IO_N_1 | K1 |
| 5 | LVDS_IO_P_2 | J3 | 6 | LVDS_IO_N_2 | J2 |
| 7 | LVDS_IO_P_3 | H2 | 8 | LVDS_IO_N_3 | G2 |
| 9 | LVDS_IO_P_4 | J4 | 10 | LVDS_IO_N_4 | H4 |
| 11 | LVDS_IO_P_5 | H6 | 12 | LVDS_IO_N_5 | H5 |
| 13 | LVDS_IO_P_6 | G4 | 14 | LVDS_IO_N_6 | G3 |
| 15 | LVDS_IO_P_7 | F4 | 16 | LVDS_IO_N_7 | F3 |
| 17 | LVDS_IO_P_8 | E3 | 18 | LVDS_IO_N_8 | D3 |
| 19 | LVDS_IO_P_9 | E6 | 20 | LVDS_IO_N_9 | E5 |
| 21 | GND | GND | 22 | GND | GND |
| 23 | LVDS_IO_P_10 | D5 | 24 | LVDS_IO_N_10 | D4 |
| 25 | LVDS_IO_P_11 | A13 | 26 | LVDS_IO_N_11 | A14 |
| 27 | LVDS_IO_P_12 | C4 | 28 | LVDS_IO_N_12 | B4 |
| 29 | LVDS_IO_P_13 | C6 | 30 | LVDS_IO_N_13 | C5 |
| 31 | GND | GND | 32 | GND | GND |
| 33 | LVDS_IO_P_14 | B7 | 34 | LVDS_IO_N_14 | B6 |
| 35 | LVDS_IO_P_15 | D8 | 36 | LVDS_IO_N_15 | C7 |
| 37 | LVDS_IO_P_16 | G6 | 38 | LVDS_IO_N_16 | F6 |
| 39 | LVDS_IO_P_17 | E7 | 40 | LVDS_IO_N_17 | D7 |
| 41 | GND | | 42 | GND | |
| 43 | LVDS_IO_P_66 | C9 | 44 | LVDS_IO_N_66 | B9 |
| 45 | LVDS_IO_P_67 | D12 | 46 | LVDS_IO_N_67 | D13 |
| 47 | 3.3V | 3.3V | 48 | 3.3V | 3.3V |

# GPIO connector J5 48 pin connection as follows

| J5 | | | | | |
|---|---|---|---|---|---|
| 1 | 5V | 5V | 2 | 5V | 5V |
| 3 | LVDS_IO_P_18 | T9 | 4 | LVDS_IO_N_18 | T10 |
| 5 | LVDS_IO_P_19 | T11 | 6 | LVDS_IO_N_19 | U11 |
| 7 | LVDS_IO_P_20 | T13 | 8 | LVDS_IO_N_20 | U13 |
| 9 | LVDS_IO_P_21 | P15 | 10 | LVDS_IO_N_21 | R15 |
| 11 | LVDS_IO_P_22 | R16 | 12 | LVDS_IO_N_22 | T16 |
| 13 | LVDS_IO_P_23 | N15 | 14 | LVDS_IO_N_23 | N16 |
| 15 | LVDS_IO_P_24 | M16 | 16 | LVDS_IO_N_24 | M17 |
| 17 | LVDS_IO_P_25 | K13 | 18 | LVDS_IO_N_25 | J13 |
| 19 | LVDS_IO_P_26 | J14 | 20 | LVDS_IO_N_26 | H15 |
| 21 | GND | | 22 | GND | |
| 23 | LVDS_IO_P_27 | H17 | 24 | LVDS_IO_N_27 | G17 |
| 25 | LVDS_IO_P_28 | F15 | 26 | LVDS_IO_N_28 | F16 |
| 27 | LVDS_IO_P_29 | E17 | 28 | LVDS_IO_N_29 | D17 |
| 29 | LVDS_IO_P_30 | C16 | 30 | LVDS_IO_N_30 | C17 |
| 31 | GND | GND | 32 | GND | GND |
| 33 | LVDS_IO_P_31 | D15 | 34 | LVDS_IO_N_31 | C15 |
| 35 | LVDS_IO_P_32 | D14 | 36 | LVDS_IO_N_32 | C14 |
| 37 | LVDS_IO_P_33 | B13 | 38 | LVDS_IO_N_33 | B14 |
| 39 | LVDS_IO_P_34 | C12 | 40 | LVDS_IO_N_34 | B12 |
| 41 | GND | GND | 42 | GND | GND |
| 43 | NC | NC | 44 | NC | NC |
| 45 | NC | NC | 46 | NC | NC |
| 47 | 3.3V | 3.3V | 48 | 3.3V | 3.3V |

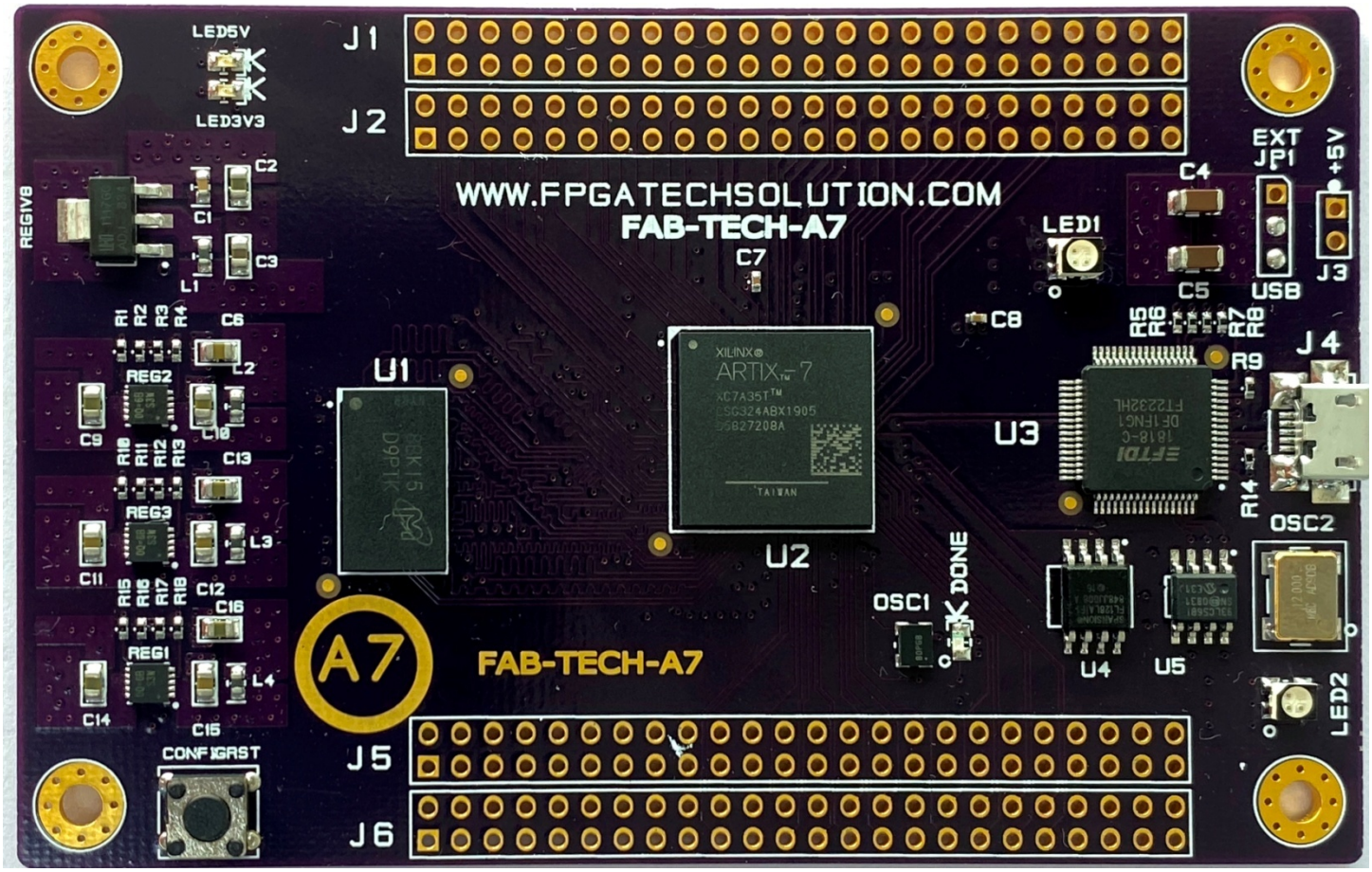
# GPIO connector J6 48 pin connection as follows

| J6 | | | | | |
|---|---|---|---|---|---|
| 1 | 5V | 5V | 2 | 5V | 5V |
| 3 | LVDS_IO_P_35 | F13 | 4 | LVDS_IO_N_35 | F14 |
| 5 | LVDS_IO_P_36 | T14 | 6 | LVDS_IO_N_36 | T15 |
| 7 | LVDS_IO_P_37 | R12 | 8 | LVDS_IO_N_37 | R13 |
| 9 | LVDS_IO_P_38 | N14 | 10 | LVDS_IO_N_38 | P14 |
| 11 | LVDS_IO_P_39 | K15 | 12 | LVDS_IO_N_39 | J15 |
| 13 | LVDS_IO_P_40 | H14 | 14 | LVDS_IO_N_40 | G14 |
| 15 | LVDS_IO_P_41 | H16 | 16 | LVDS_IO_N_41 | G16 |
| 17 | LVDS_IO_P_42 | E15 | 18 | LVDS_IO_N_42 | E16 |
| 19 | LVDS_IO_P_43 | V10 | 20 | LVDS_IO_N_43 | V11 |
| 21 | GND | GND | 22 | GND | GND |
| 23 | LVDS_IO_P_44 | U12 | 24 | LVDS_IO_N_44 | V12 |
| 25 | LVDS_IO_P_45 | U14 | 26 | LVDS_IO_N_45 | V14 |
| 27 | LVDS_IO_P_46 | V15 | 28 | LVDS_IO_N_46 | V16 |
| 29 | LVDS_IO_P_47 | U16 | 30 | LVDS_IO_N_47 | V17 |
| 31 | GND | GND | 32 | GND | GND |
| 33 | LVDS_IO_P_48 | U17 | 34 | LVDS_IO_N_48 | U18 |
| 35 | LVDS_IO_P_49 | R18 | 36 | LVDS_IO_N_49 | T18 |
| 37 | LVDS_IO_P_50 | N17 | 38 | LVDS_IO_N_50 | P18 |
| 39 | LVDS_IO_P_51 | L18 | 40 | LVDS_IO_N_51 | M18 |
| 41 | GND | GND | 42 | GND | GND |
| 43 | LVDS_IO_P_71 | C11 | 44 | LVDS_IO_N_71 | C10 |
| 45 | NC | NC | 46 | NC | NC |
| 47 | 3.3V | 3.3V | 48 | 3.3V | 3.3V |

# GPIO connector J2 48 pin connection as follows

| J2 | | | | | |
|---|---|---|---|---|---|
| 1 | 5V | 5V | 2 | 5V | 5V |
| 3 | LVDS_IO_P_52 | H1 | 4 | LVDS_IO_N_52 | G1 |
| 5 | LVDS_IO_P_53 | F1 | 6 | LVDS_IO_N_53 | E1 |
| 7 | LVDS_IO_P_54 | E2 | 8 | LVDS_IO_N_54 | D2 |
| 9 | LVDS_IO_P_55 | C2 | 10 | LVDS_IO_N_55 | C1 |
| 11 | LVDS_IO_P_56 | B1 | 12 | LVDS_IO_N_56 | A1 |
| 13 | LVDS_IO_P_57 | B3 | 14 | LVDS_IO_N_57 | B2 |
| 15 | LVDS_IO_P_58 | A4 | 16 | LVDS_IO_N_58 | A3 |
| 17 | LVDS_IO_P_59 | A6 | 18 | LVDS_IO_N_59 | A5 |
| 19 | LVDS_IO_P_60 | B8 | 20 | LVDS_IO_N_60 | A8 |
| 21 | GND | | 22 | GND | |
| 23 | LVDS_IO_P_61 | A10 | 24 | LVDS_IO_N_61 | A9 |
| 25 | LVDS_IO_P_62 | B11 | 26 | LVDS_IO_N_62 | A11 |
| 27 | LVDS_IO_P_63 | A15 | 28 | LVDS_IO_N_63 | A16 |
| 29 | LVDS_IO_P_64 | B16 | 30 | LVDS_IO_N_64 | B17 |
| 31 | GND | GND | 32 | GND | GND |
| 33 | LVDS_IO_P_65 | B18 | 34 | LVDS_IO_N_65 | A18 |
| 35 | LVDS_IO_P_68 | E18 | 36 | LVDS_IO_N_66 | D18 |
| 37 | LVDS_IO_P_69 | G18 | 38 | LVDS_IO_N_67 | F18 |
| 39 | LVDS_IO_P_70 | J17 | 40 | LVDS_IO_N_68 | J18 |
| 41 | GND | GND | 42 | GND | GND |
| 43 | NC | NC | 44 | NC | NC |
| 45 | NC | NC | 46 | NC | NC |
| 47 | 3.3V | 3.3V | 48 | 3.3V | 3.3V |

**Note: All pin with this color are XADC pins**


LED5V
LED3V3
J1
J2
WWW.FPGATECHSOLUTION.COM
FAB-TECH-A7
EXT
JP1
+5V
J3
USB
LED1
C4
C5
C7
C8
U1
U2
U3
J4
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OSC2
OSC1
DONE
U4
U5
LED2
REGIV8
REG2
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C6
C9
C10
C11
C12
C13
C14
C15
C16
CONFIGRST
J5
J6
A7
FAB-TECH-A7