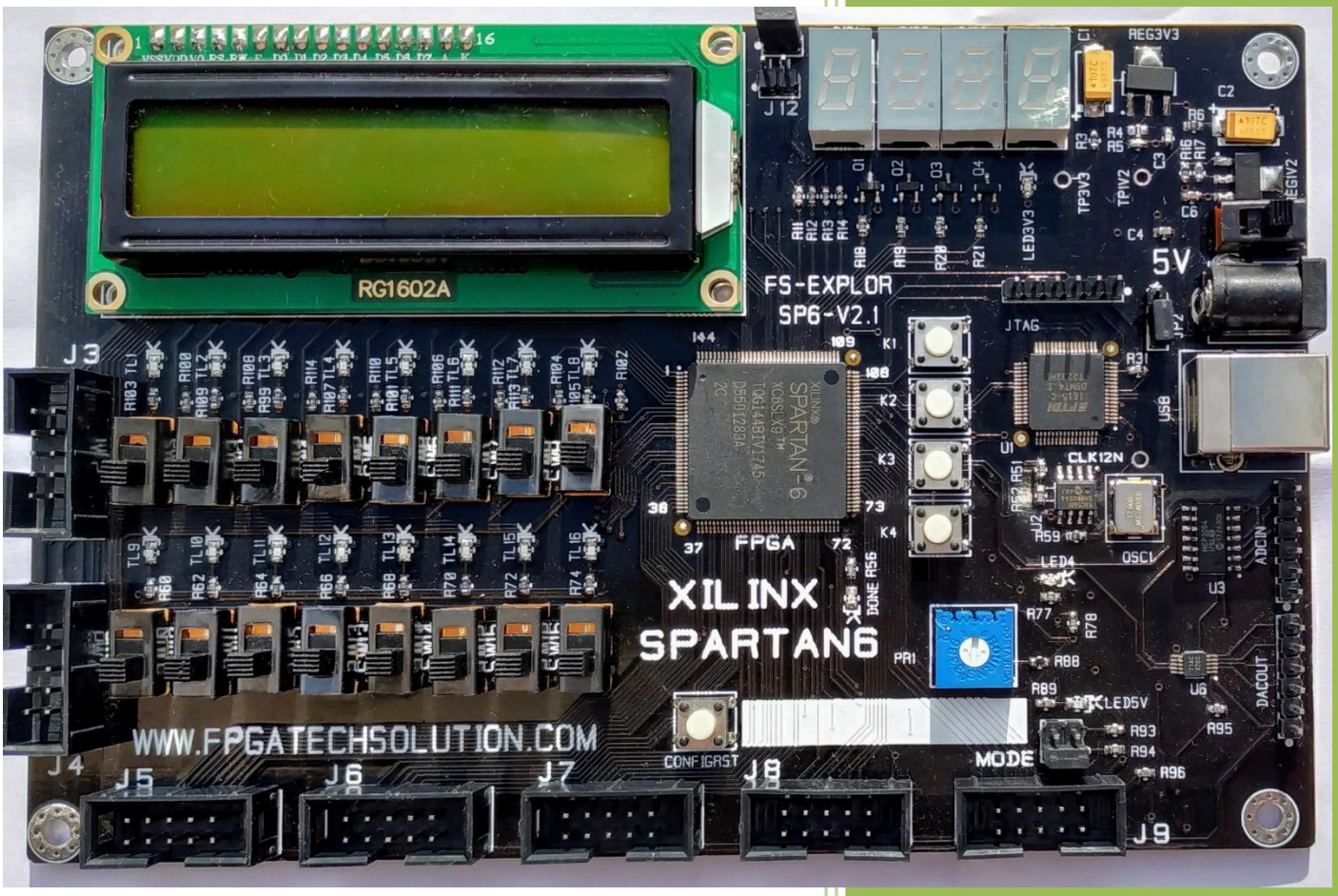
FPGA TECH SOLUTION

SOLUTION AHEAD

FS -EXPLOR SP6-V2.1

VLSI Development Board User Manual



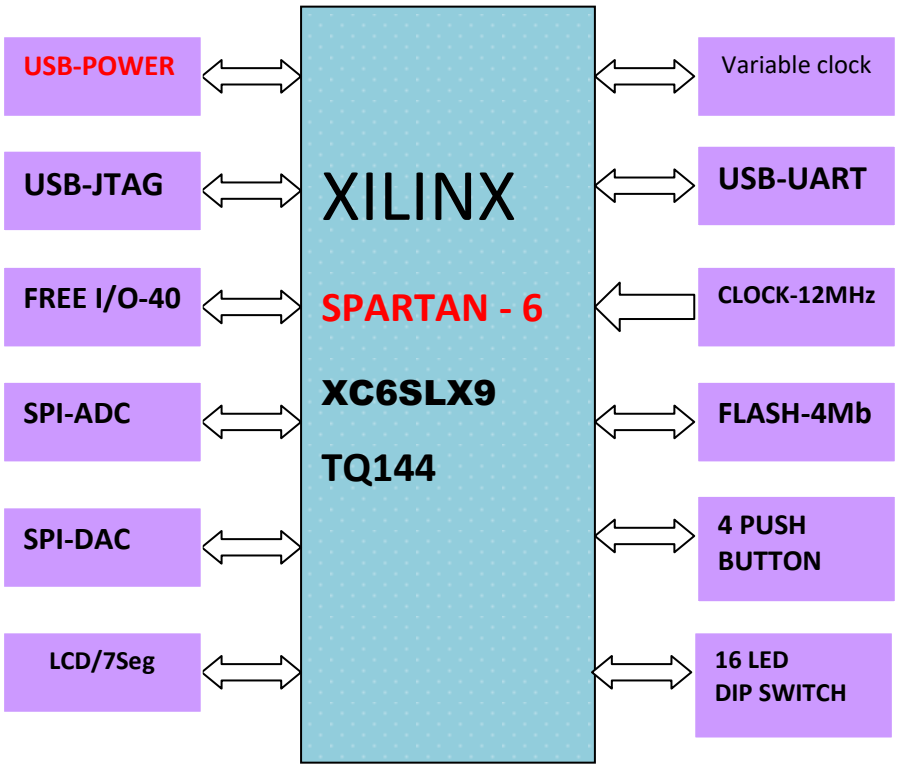
info@fpgatechsolution.com
Mobile: 9665889991
WWW.FPGASOLUTION.COM

Key Features:

- Spartan6-XC6SLX9_TQ144FPGA
- Up to 102 user-I/O pins
- TQ-144 package

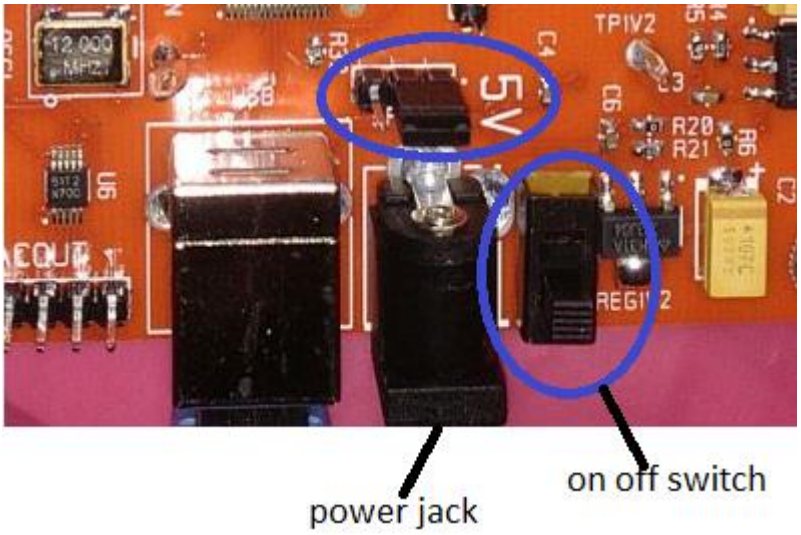
Key components:

- XC6SLX9_TQ144
- OSCILLATOR – 12MHz
- FLASH – M25P40
- USB Power
- On board USB Jtag
- USB to serial
- 10bit SPI ADC
- 8bit SPI DAC
- 16LED & DIP switch
- 4 PUSH BUTTONS
- 56 user I/O
- LCD 16By2& 7-Se
- Variable clock



BOARD POWERING

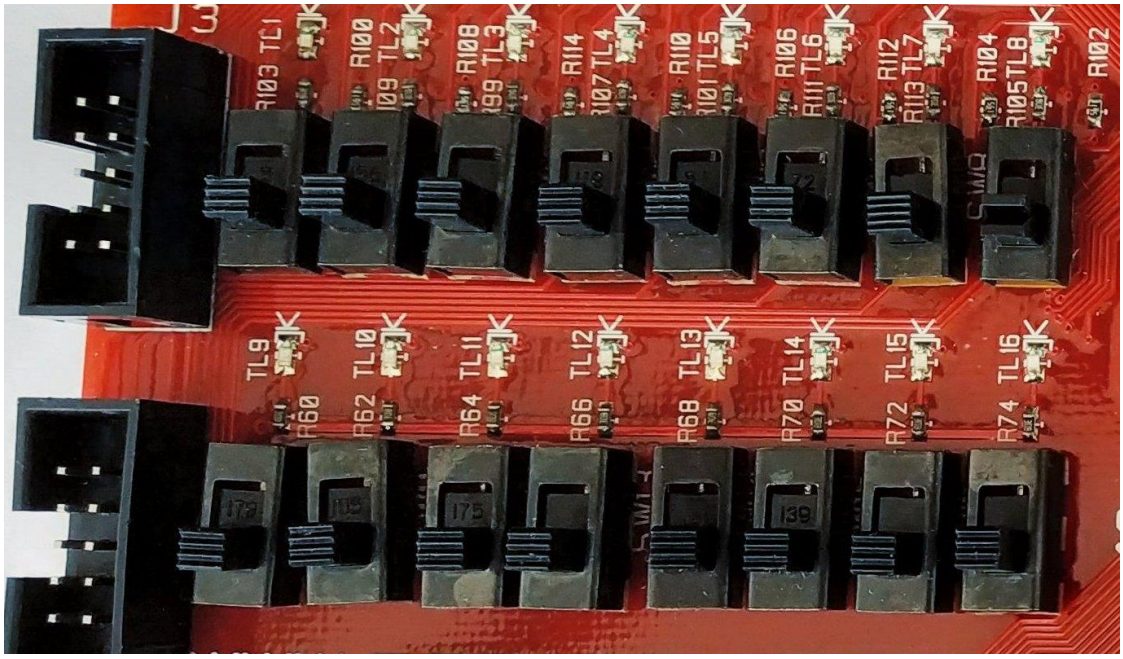
TheFS-EXPLOR-SP6-V2 board can work on USB power or external 5VDc supply. When **JP2** jumper is placed in 2 & 3 power is used from USB connector. When **JP2** jumper is placed in 1 & 2 power is used from external 5VDc supply



LED's and DIP Switches Interface

The FS-EXPLOR-SP6-V2 Board has 16 individual bidirectional I/O's. Each I/O is connected with a surface-mount LED and a DIP switch. A LED is assigned to each I/O to indicate its data status when I/O is configured as input. DIP switch is used to provide digital input (i.e. logic 0 and logic 1) to the FPGA.

The LED can display the output data value of I/O by configuring it as output and keeping its corresponding DIP switch at 0 positions



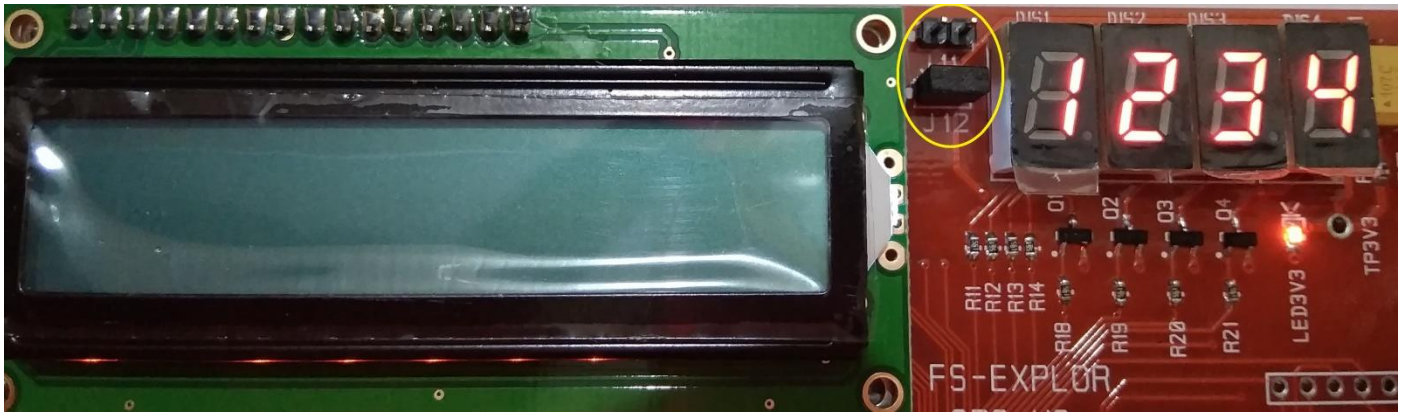
.

Pin Assignment (UCF Location) for IOs:

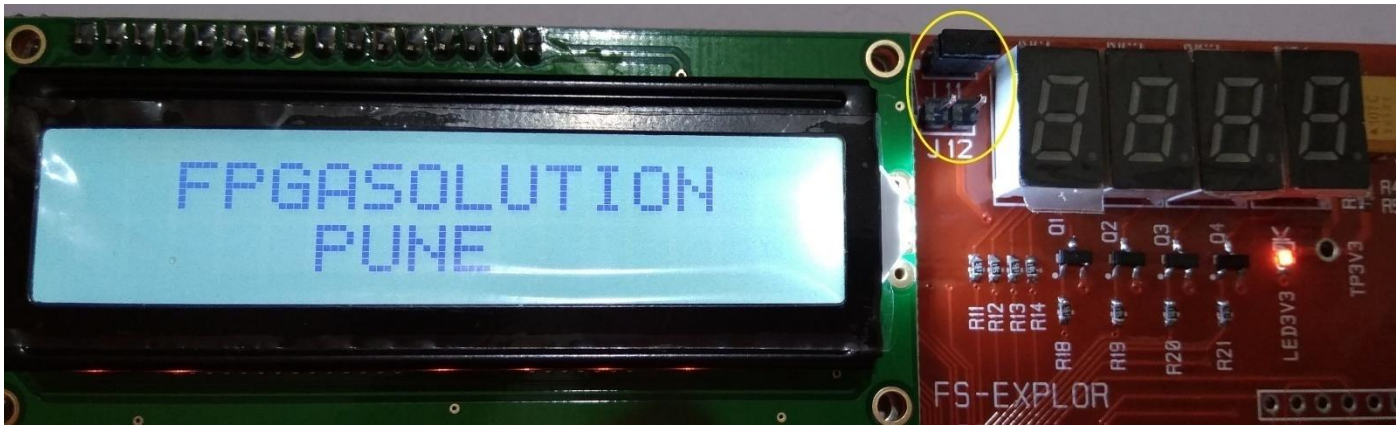
NET dip_led<0> LOC = P139 ; NET dip_led<8> LOC = P14;
NET dip_led<1> LOC = P141 ; NET dip_led<9> LOC = P15;
NET dip_led<2> LOC = P143 ; NET dip_led<10> LOC = P16;
NET dip_led<3> LOC = P1 ; NET dip_led<11> LOC = P17;
NET dip_led<4> LOC = P5 ; NET dip_led<12> LOC = P21;
NET dip_led<5> LOC = P7 ; NET dip_led<13> LOC = P22;
NET dip_led<6> LOC = P9 ; NET dip_led<14> LOC = P23;
NET dip_led<7> LOC = P11 ; NET dip_led<15> LOC = P29;

LCD Interface

The FS-EXPLOR-SP6-V2 board has 4 seven segment multiplexed with LCD, using JP12 & JP11 jumper user can decided LCD is to be power on OR seven segment. When you want to use seven segments connect jumper to J12 as shown below



When you want to use LCD connect jumper to J11 as shown below

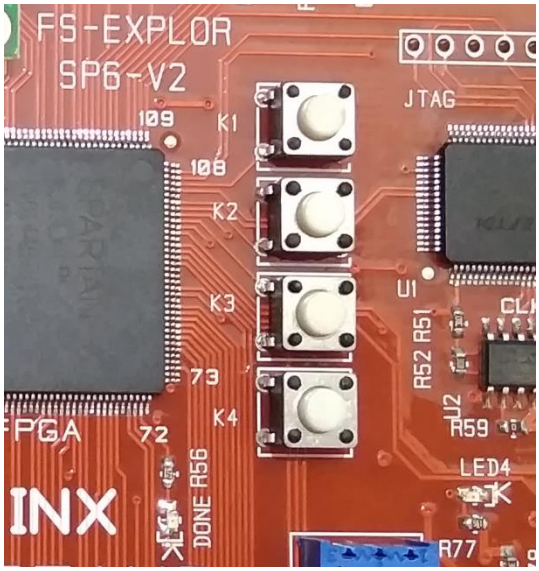


. **Pin Assignment (UCF Location) for IOs:**

```
NET SIG_A          LOC = P119;   NET DATA_BUS(0) LOC = P116;
NET SIG_B          LOC = P118;   NET DATA_BUS(1) LOC = P117;
NET SIG_C          LOC = P117;   NET DATA_BUS(2) LOC = P118;
NET SIG_D          LOC = P120;   NET DATA_BUS(3) LOC = P119;
NET SIG_E          LOC = P121;   NET DATA_BUS(4) LOC = P120;
NET SIG_F          LOC = P124;   NET DATA_BUS(5) LOC = P121;
NET SIG_G          LOC = P123;   NET DATA_BUS(6) LOC = P123;
NET SIG_PD         LOC = P116;   NET DATA_BUS(7) LOC = P124;
NET SEL_DISP1      LOC = P115;   NET LCD_e       LOC = P115;
NET SEL_DISP2      LOC = P114;   NET LCD_rs      LOC = P114;
NET SEL_DISP3      LOC = P112;
NET SEL_DISP4      LOC = P111;
```

Pushbuttons Interface

The FS-EXPLOR-SP6-V2board has 4 individual pushbuttons for input purpose. The pushbuttons are read as 1 when pushed. They are read as 0 in normal (unpressed) condition. Pushbuttons are labeled as SW1 TO SW4.



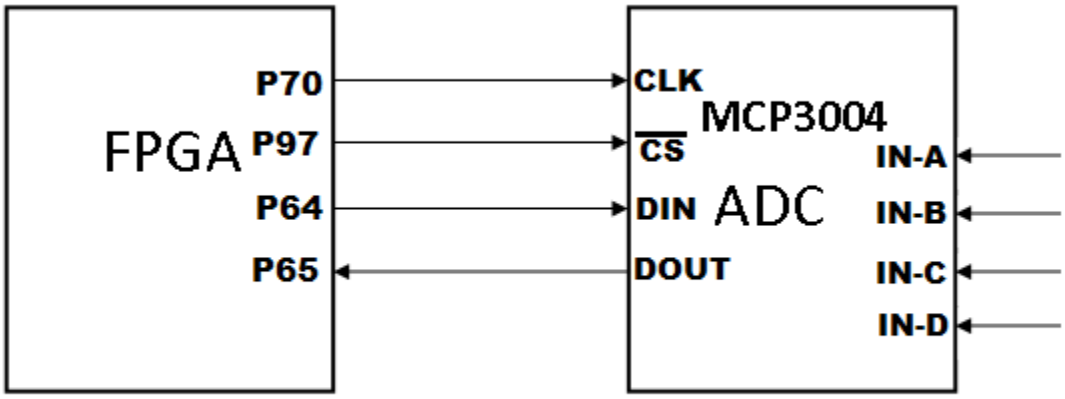
Signal Name	XC6SLX9	Active
SW1	P105	**HIGH**
SW2	P101	**HIGH**
SW3	P99	**HIGH**
SW4	P74	**HIGH**

Pin Assignment (UCF Location) for Pushbuttons:

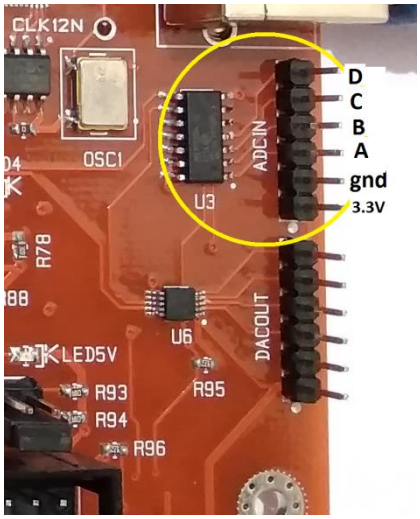
```
NET sw1  LOC = P105 ;
NET sw2  LOC = P101 ;
NET sw3  LOC = P99  ;
NET sw4  LOC = P74  ;
```

ADC Interface

The FS-EXPLOR-SP6-V2board includes anADC MCP3004. The ADC has 4 analog input channels. The channels are selected by setting the address pins of ADC. The analog input to all channels is given by external circuit through relimate pins. The other controlling signals of ADC are interfaced with FPGA board as shown in following figure. VREF is connected to 3.3V, so analog voltage input rang of all channel is 0 to 3.3V.



Interfacing of ADC with FPGA



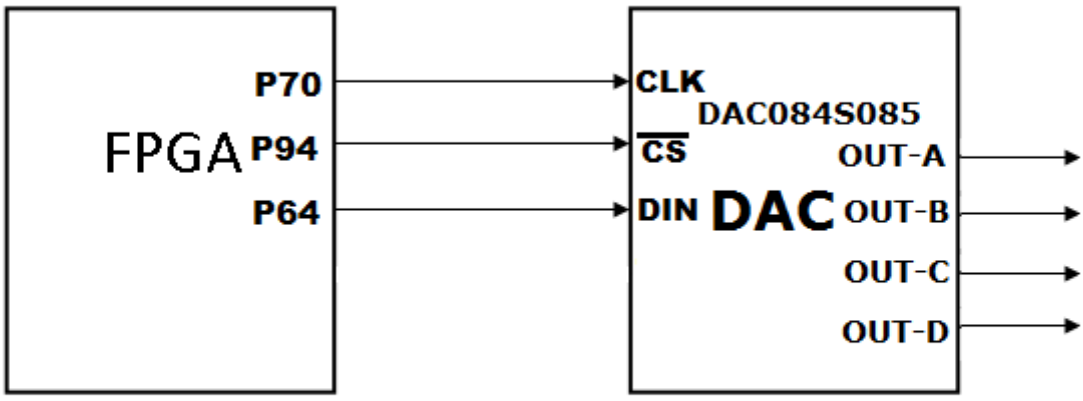
Signal Name	XC6SLX9
clk	P70
cs_adc	P97
adc_in	P65
adc_out	P64

Pin assignment (UCF Location) for ADC:

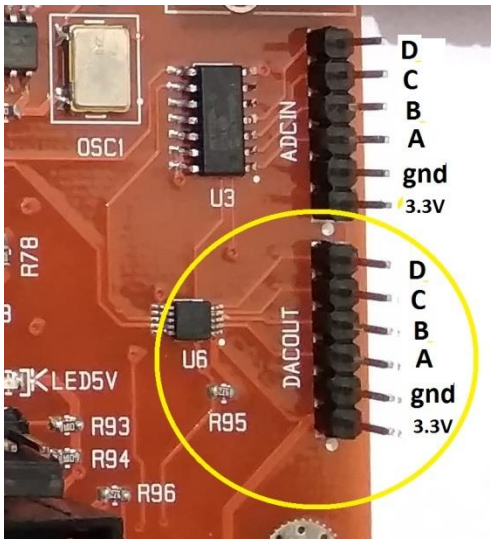
```
NET "clk"        LOC = P70;
NET "cs_adc"   LOC = P97;
NET "adc_in"    LOC = p65;
NET "adc_out" LOC = P64;
```

DAC Interface

The FS-EXPLOR-SP6-V2board includes 8-bit 4 channels, digital-to-analog converter (DACs) DAC084S085. DAC allows easy interface to most popular microprocessor buses and output ports. DAC works on 3.3V. The following figure shows the interfacing diagram of DAC with FPGA Board. VREF is connected to 3.3V, so analog voltage output rang of all channel is 0 to 3.3V.



Interfacing of DAC with FPGA



Signal Name	XC6SLX9
CS_DAC	P94
CLK	P70
MOSI	P64

Pin Assignment (UCF Location) DAC084S085:

```
NET "CS_DAC" LOC = P94;
NET "CLK"    LOC = P70;
NET "MOSI"   LOC = P64;
```

USB Interface

The FS-EXPLOR-SP6-V2board have USB interface using device FT2232HL from FTDI. This acts as a Jtag and USB to UART converter, so that Communication with FPGA can accomplish by USB port.

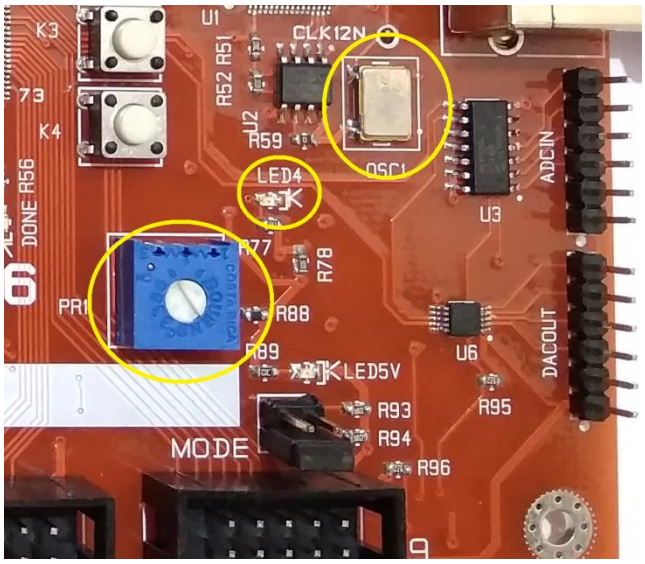
Signal Name	XC6SLX9
USB_TX	P102
USB_RX	P104

Pin Assignment (UCF Location) for USB interface:

NET "USB_TX" LOC = P102;
NET "USB_RX" LOC = P104;

Clock Sources

The FS-EXPLOR-SP6-V2 supports clock input sources which are listed below.
The board includes an on-board 12 MHz clock oscillator. This board also has a variable clock frequency generator. You can very frequency by using PR1 pot, LED4 will show variable clock.



Signal Name	XC6SLX9
Clock 12Mhz	P95
Variable clock	P87

Pin Assignment (UCF Location) for clock:

```
NET CLK_12MHZ   LOC = P95  ;
NET CLK_555     LOC = P87  ;
```

FREE INPUT OUTPUT

The FS-EXPLOR SP6-V2board has seven free input output connectors. Each connector have 8 input output pins, 3.3V Dc pin and GND pin.

Name	Signal Name	XCS6LX9-TQG144		Name	Signal Name	XCS6LX9-TQG144
J3	J3_1	P126		J5	J5_1	P26
	J3_2	P127			J5_2	P24
	J3_3	P131			J5_3	P30
	J3_4	P132			J5_4	P27
	J3_5	P133			J5_5	P33
	J3_6	P134			J5_6	P32
	J3_7	P137			J5_7	P35
	J3_8	P138			J5_8	P34
	J3_9	**GND**			J5_9	**GND**
	J3_10	**+3.3V**			J5_10	**+3.3V**
J4	J4_1	P140		J6	J6_1	P41
	J4_2	P142			J6_2	P40
	J4_3	P144			J6_3	P44
	J4_4	P2			J6_4	P43
	J4_5	P6			J6_5	P46
	J4_6	P8			J6_6	P45
	J4_7	P10			J6_7	P48
	J4_8	P12			J6_8	P47
	J4_9	**GND**			J9_9	**GND**
	J5_10	**+3.3V**			J6_10	**+3.3V**
Name	**Signal Name**	**XCS6LX9-TQG144**		**Name**	**Signal Name**	**XCS6LX9-TQG144**
J7	J7_1	P51		J8	J8_1	P62
	J7_2	P50			J8_2	P66
	J7_3	P56			J8_3	P75
	J7_4	P55			J8_4	P78
	J7_5	P58			J8_5	P80
	J7_6	P57			J8_6	P79
	J7_7	P61			J8_7	P82
	J7_8	P59			J8_8	P81
	J7_9	**GND**			J8_9	**GND**
	J7_10	**+3.3V**			J8_10	**+3.3V**

Name	Signal Name	XCS6LX9-TQG144
J9	J9_1	P83
	J9_2	P84
	J9_3	P85
	J9_4	P88
	J9_5	P92
	J9_6	P93
	J9_7	P98
	J9_8	P100
	J9_9	**GND**
	J9_10	**+3.3V**

All Source code can be download from link given below

https://github.com/fpgatechsolution/FS-EXPLOR-SP6-V2