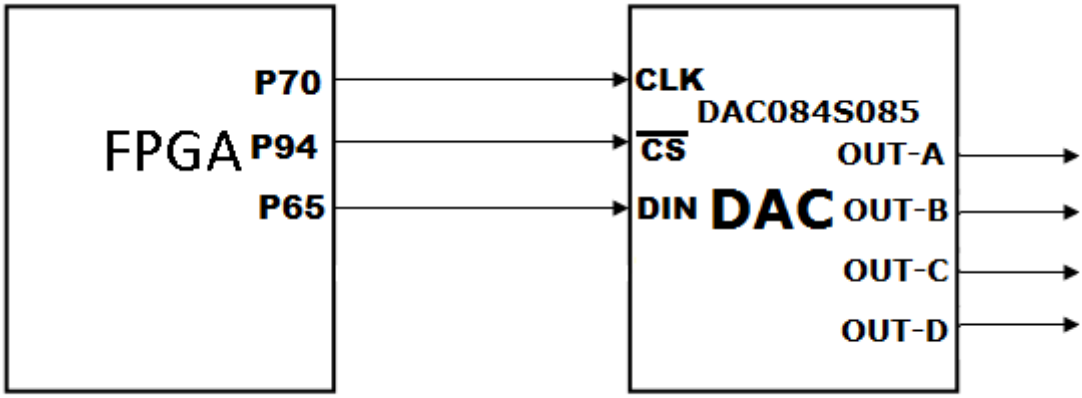
HOW TO TESE DAC

DAC Interface

The **FS-EXPLOR SP6-V2** board includes 8-bit 4 channels, digital-to-analog converter (DACs) DAC084S085. DAC allows easy interface to most popular microprocessor buses and output ports. DAC works on 3.3V. The following figure shows the interfacing diagram of DAC with FPGA Board. VREF is connected to 3.3V, so analog voltage output rang of all channel is 0 to 3.3V.



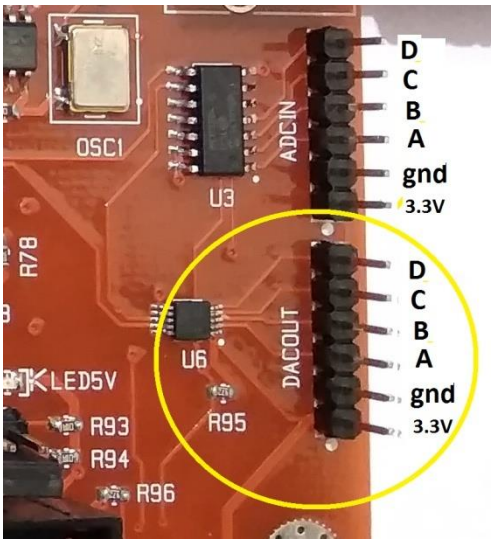
Interfacing of DAC with FPGA

Pin Assignment (UCF Location) DAC084S085:

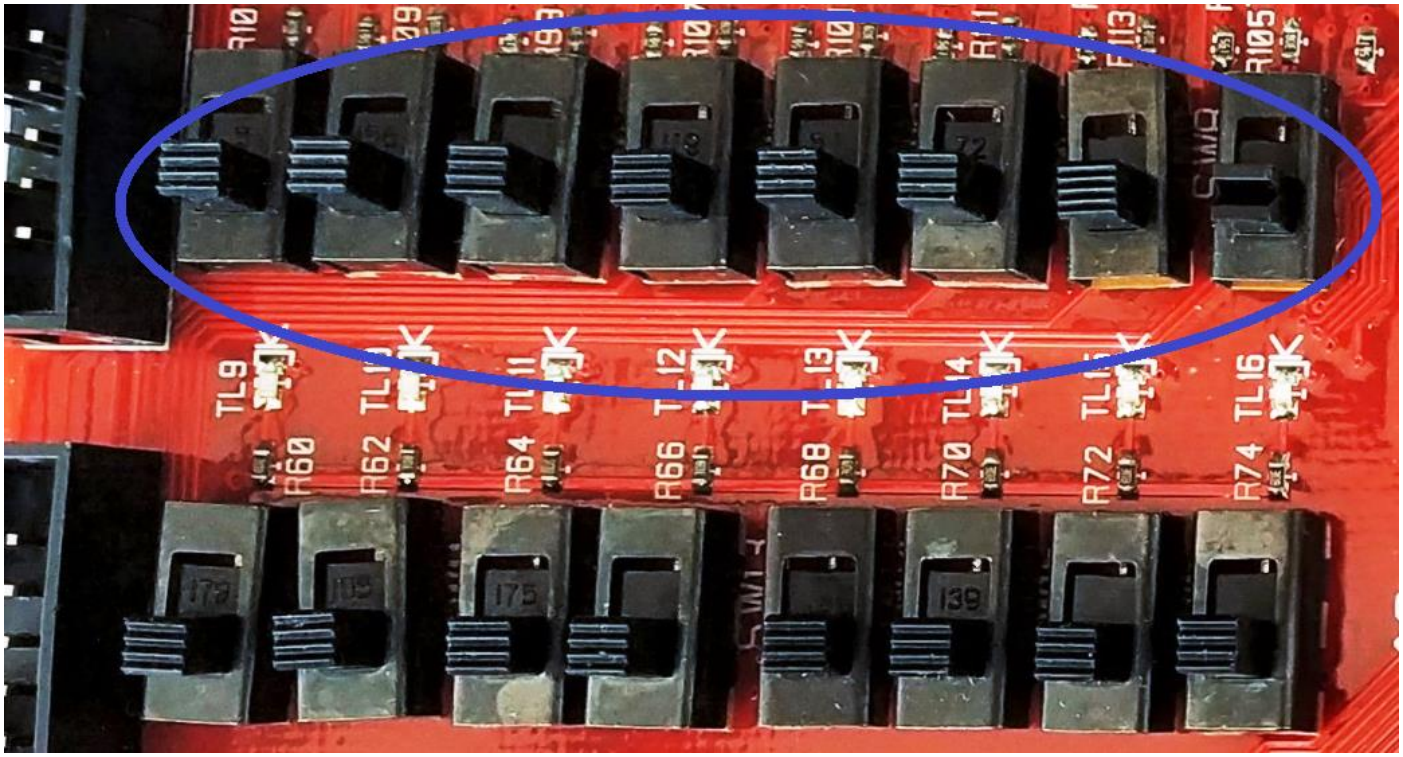
Signal Name	LX9
CS	P94
CLK	P70
DIN	P65

Follow the following steps

Power on kit connect usb cable and configure FPGA with dac_test.bit

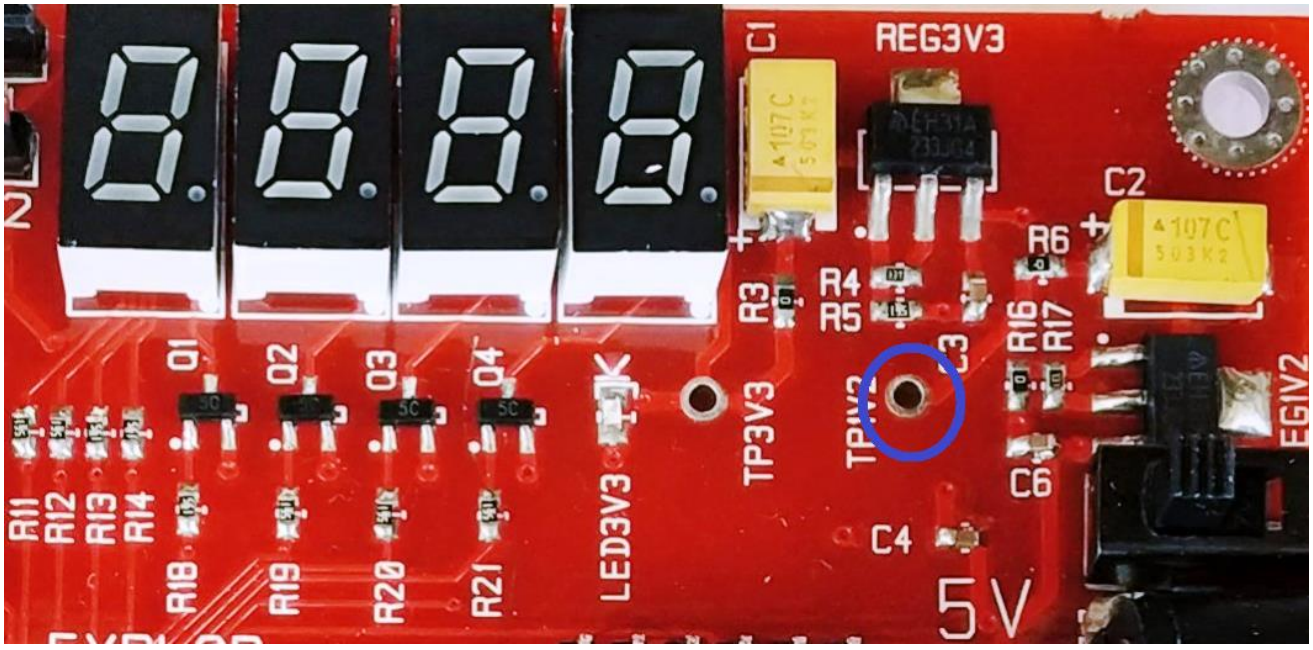


Now carefully check output voltage on any analog output pin (out-A) with respect or dip switches below LCD, channel can be select by sw9 & sw10



Calculations for DAC output

DAC is 8bit, Vref is 3.3V for more accuracy check Vref as shown below



Now suppose Vref is 3.3V

As 8bit DAC max count is 255

Voltage for one steep = Vref / 255

Voltage for one steep = 0.01294

Now the see count that display on 7-seg or LCD as shown below

Now out voltage at out-A =0.01294 X count on LCD

LCD & Seven Segment Interface

The **FS-EXPLOR SP6-V1**board has 4seven segment multiplexed with LCD, using JP1 jumper user can decided LCD is to be power on OR seven segment.

LCD	seven segment	XC6SLX9
LCD_D3	SIG_A	P119
LCD_D2	SIG_B	P118
LCD_D1	SIG_C	P117
LCD_D4	SIG_D	P120
LCD_D5	SIG_E	P121
LCD_D7	SIG_F	P124
LCD_D6	SIG_G	P123
LCD_D0	SIG_PD	P116
LCD_RS	SEL_DISP1	P115
	SEL_DISP2	P114
LCD_EN	SEL_DISP3	P112
	SEL_DISP4	P111

As LCD and seven segment is multiplexed we have make a provision in VHDL code as, when switch marked red is ON then LCD will work &when switch marked red is OFF then seven segment will work