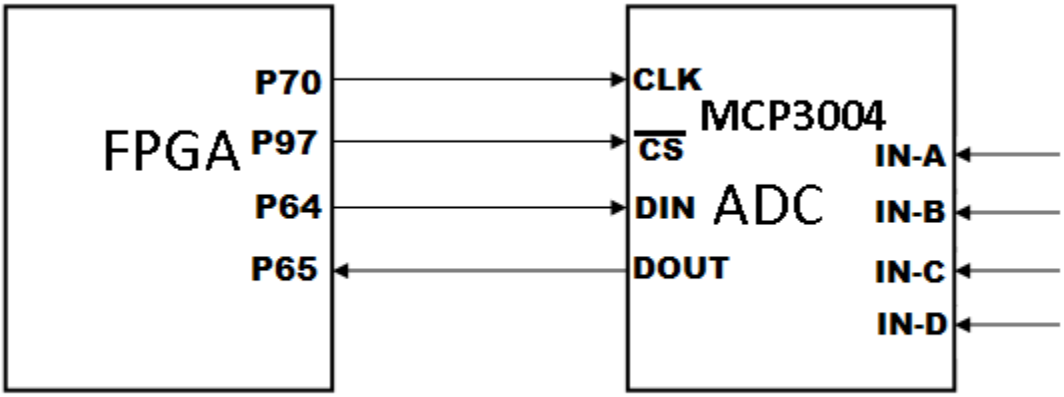
HOW TO TESE ADC

ADC Interface

The **FS-EXPLOR SP6-V2** board includes an ADC MCP3004. The ADC has 4 analog input channels. The channels are selected by setting the address pins of ADC. The analog input to all channels is given by external circuit through relimate pins. The other controlling signals of ADC are interfaced with FPGA board as shown in following figure. VREF is connected to 3.3V, **so analog voltage input rang of all channel is 0 to 3.3V.**



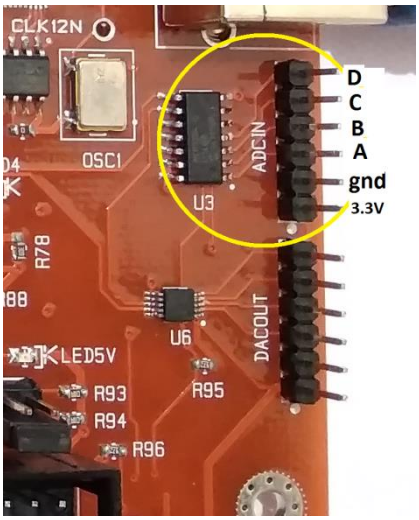
Interfacing of ADC with FPGA

Pin assignment (UCF Location) for ADC:

Signal Name	LX 9
CLK	P70
CS	P97
DIN	P65
DOUT	P64

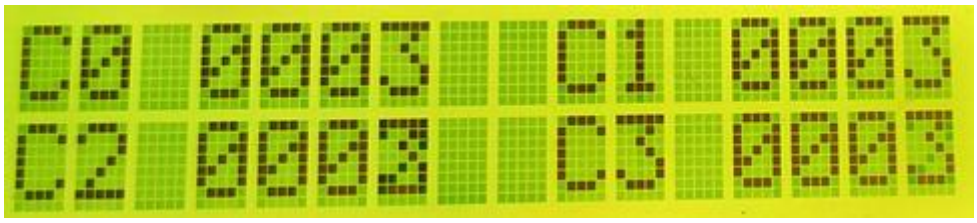
Follow the following steps

Power on kit connect usb cable and configure FPGA with adc_test.bit



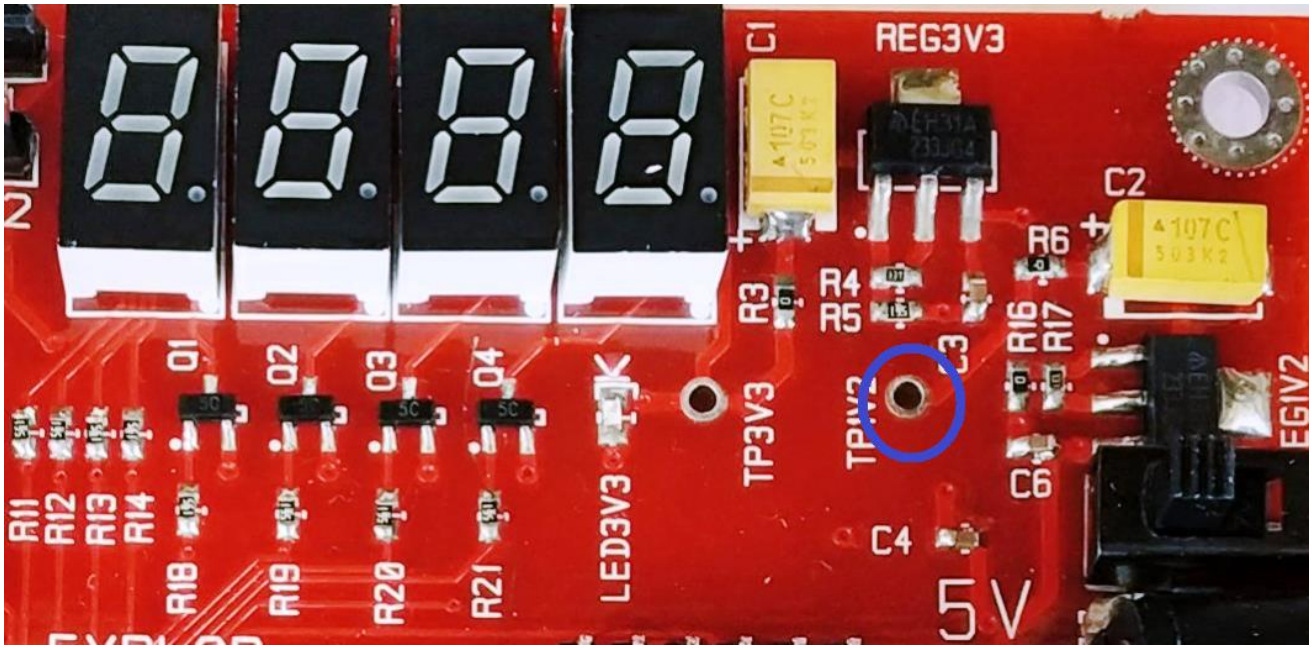
Now carefully apply voltage to Ain-D and see output count on LCD

please do not apply voltage more than 3.3v



Calculations for ADC output

ADC is 10bit, Vref is 3.3V for more accuracy check Vref as shown below



Now suppose Vref is 3.3V

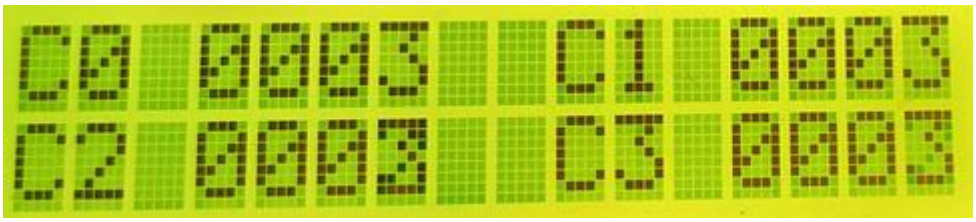
As 10bit ADC max count is 1023

Voltage for one steep = Vref / 1023

Voltage for one steep = 0.00322

Now the see count that display on 7-seg or LCD as shown below

Input voltage at Ain-D =0.00322 X count on LCD



LCD & Seven Segment Interface

The **FS-EXPLOR SP6-V2** board has 4seven segment multiplexed with LCD, using JP1 jumper user can decided LCD is to be power on OR seven segment.

LCD	seven segment	XC6SLX9
LCD_D3	SIG_A	P119
LCD_D2	SIG_B	P118
LCD_D1	SIG_C	P117
LCD_D4	SIG_D	P120
LCD_D5	SIG_E	P121
LCD_D7	SIG_F	P124
LCD_D6	SIG_G	P123
LCD_D0	SIG_PD	P116
LCD_RS	SEL_DISP1	P115
	SEL_DISP2	P114
LCD_EN	SEL_DISP3	P112
	SEL_DISP4	P111

As LCD and seven segment is multiplexed we have make a provision in VHDL code as, when switch marked red is ON then LCD will work & when switch marked red is OFF then seven segment will work