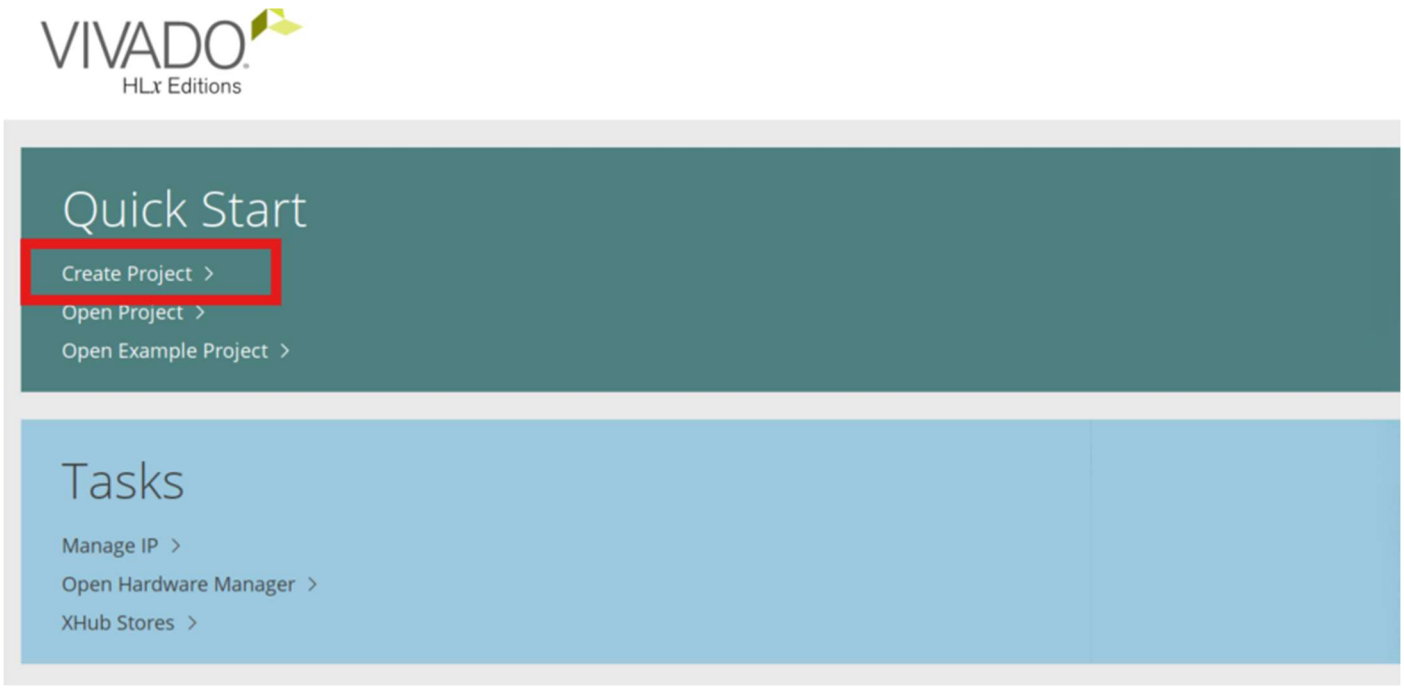
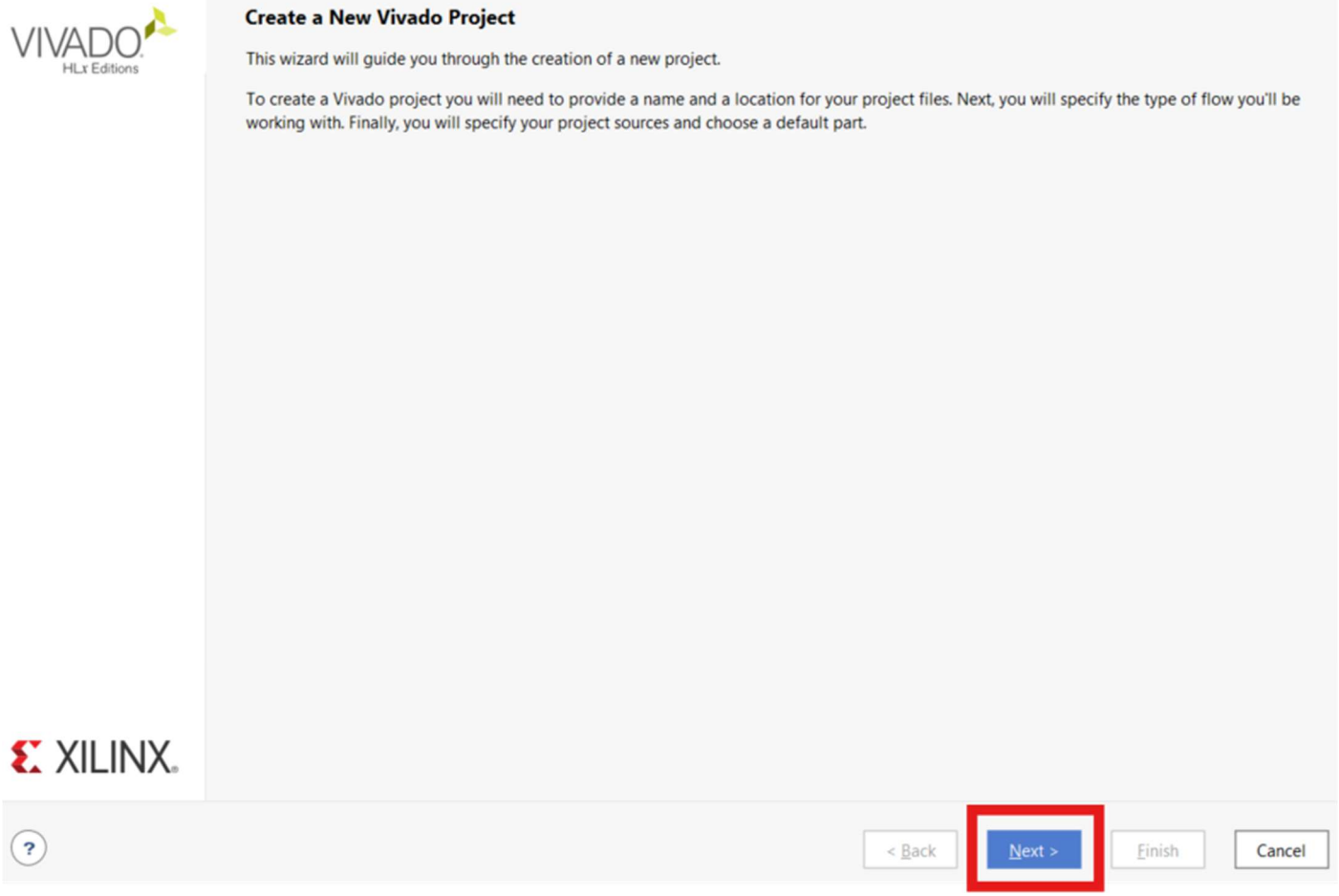
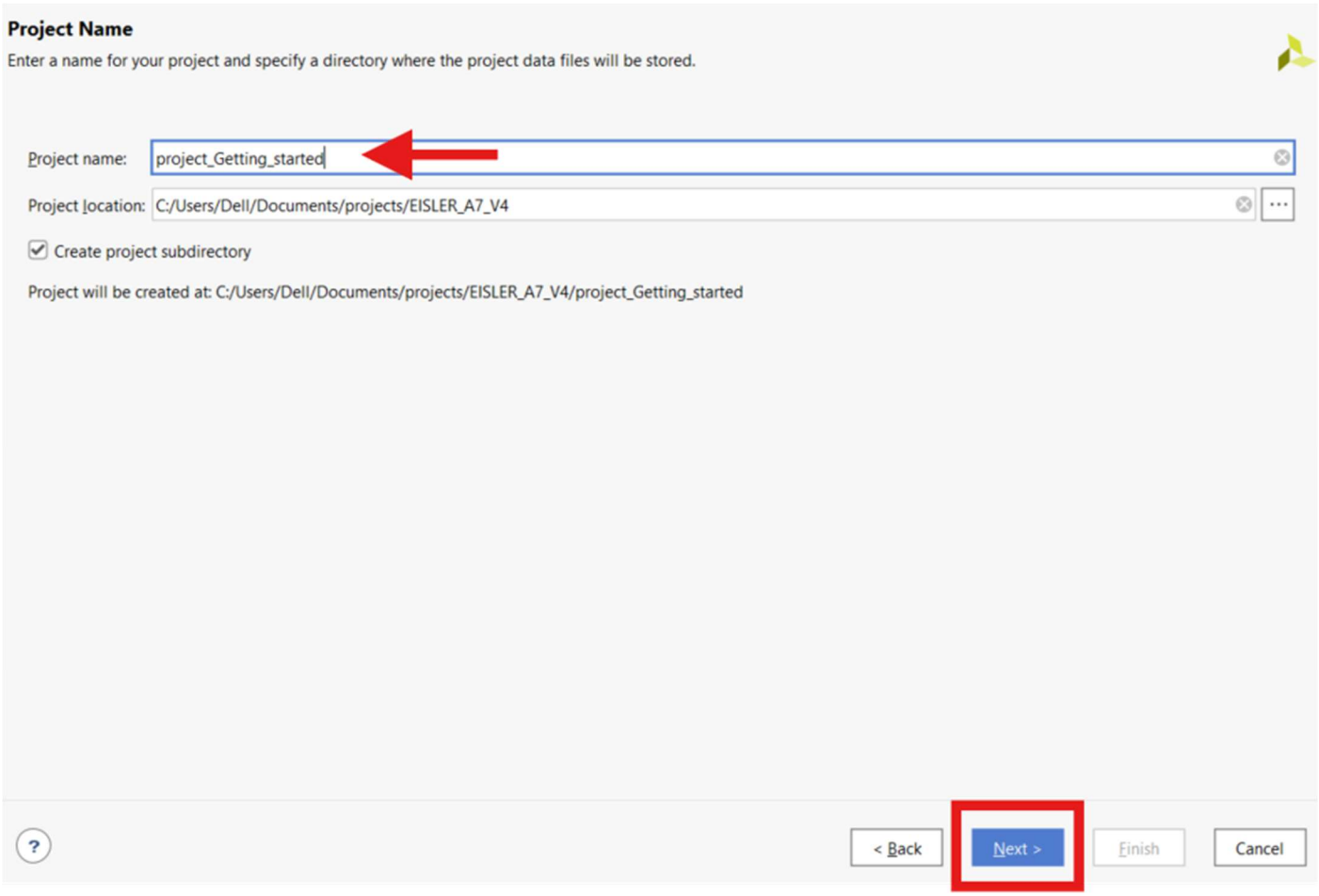
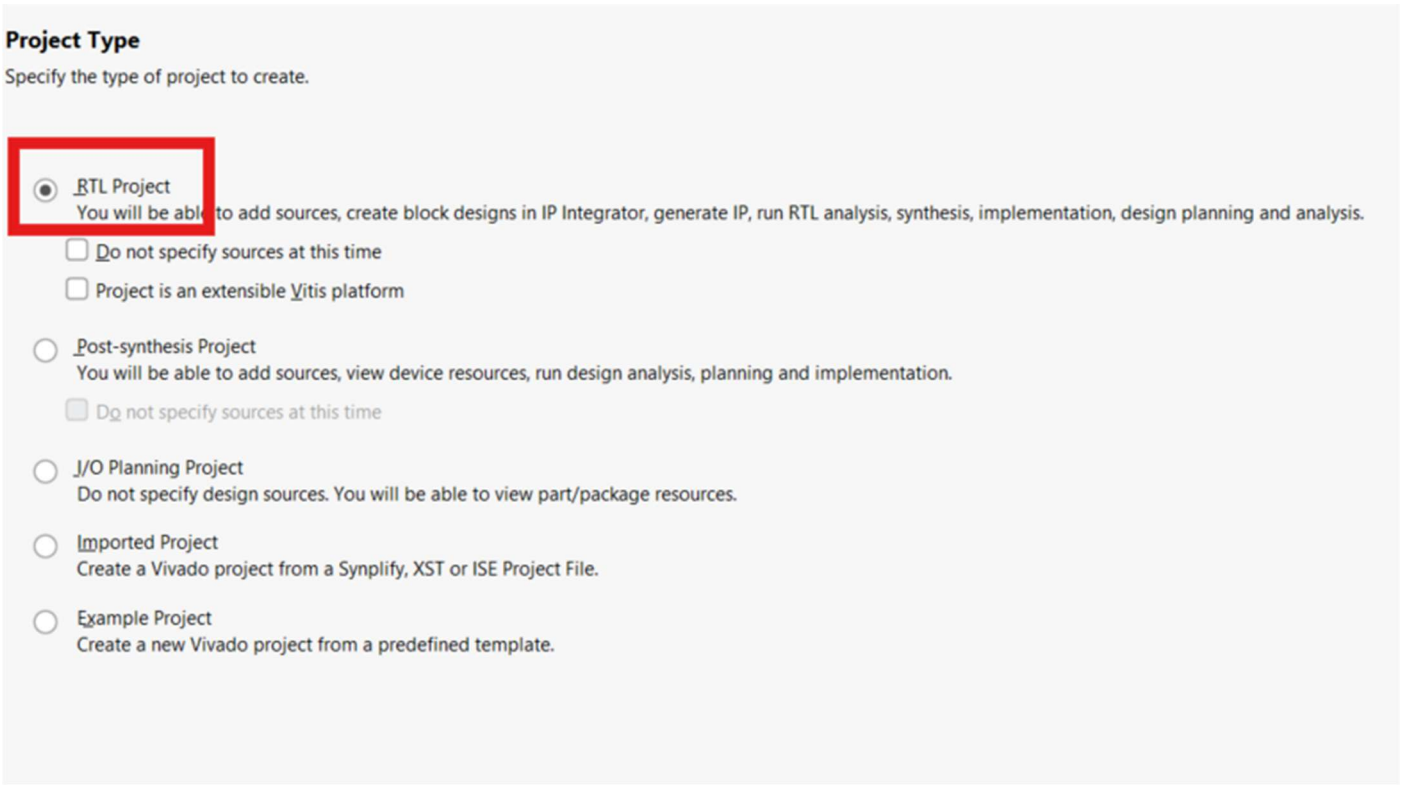
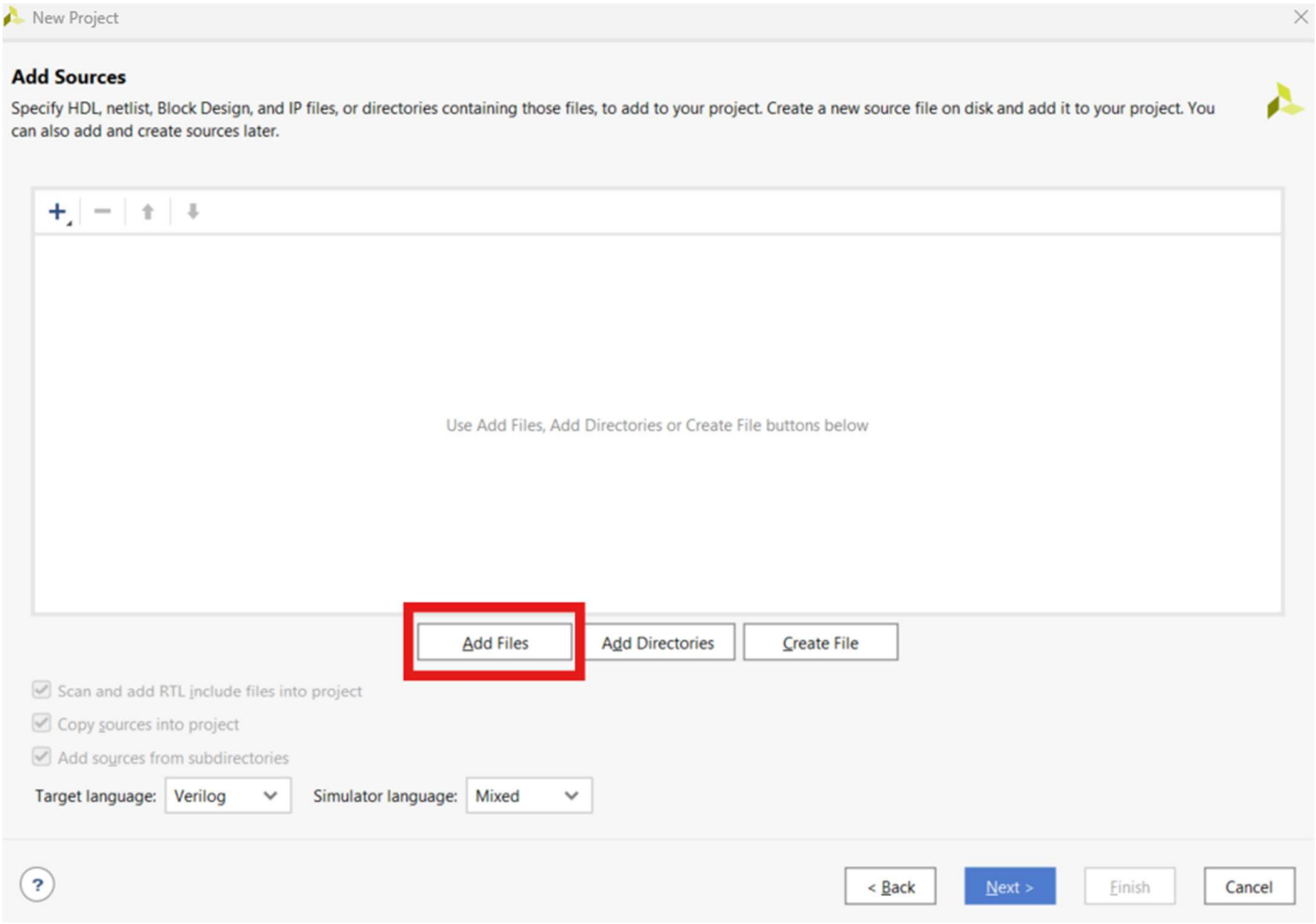
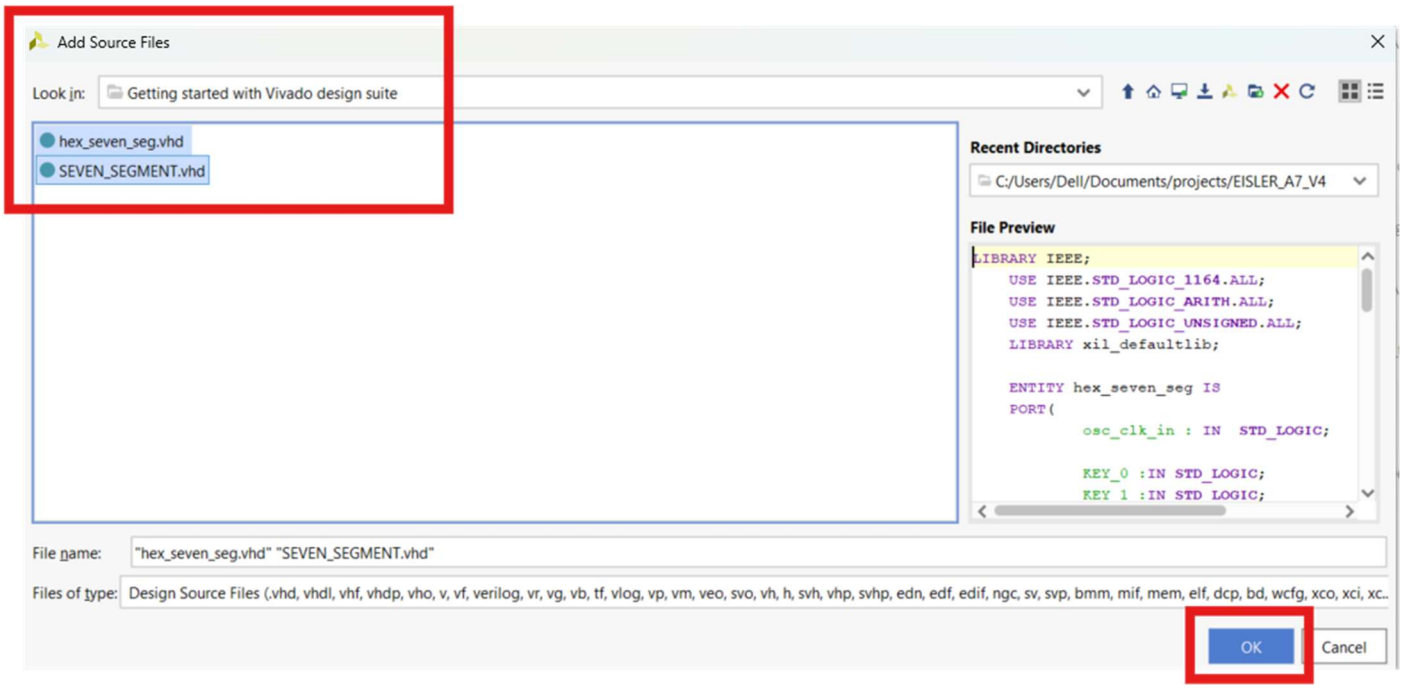

VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores

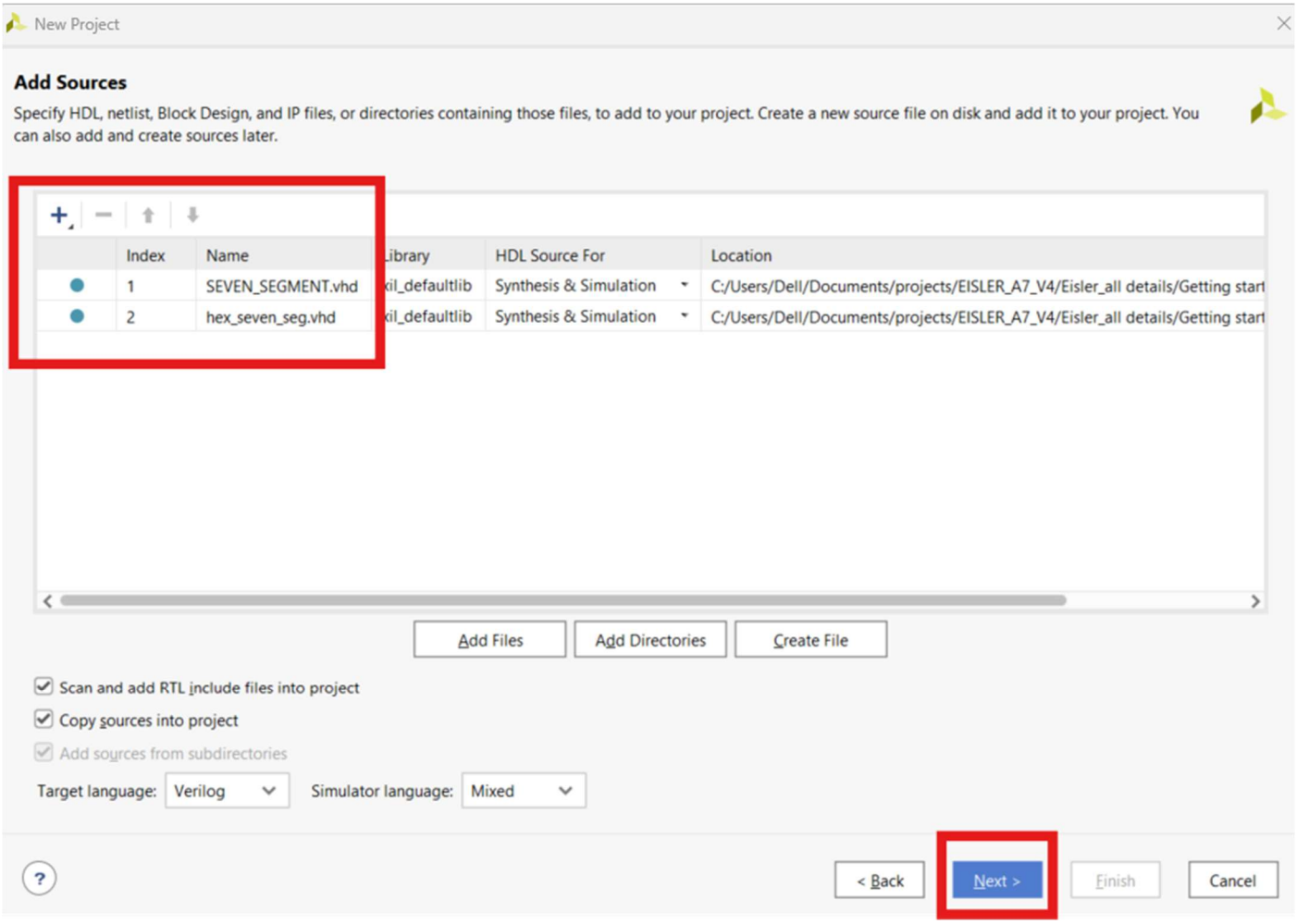

VIVADO
HLx Editions
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
XILINX
?
< Back
Next >
Finish
Cancel

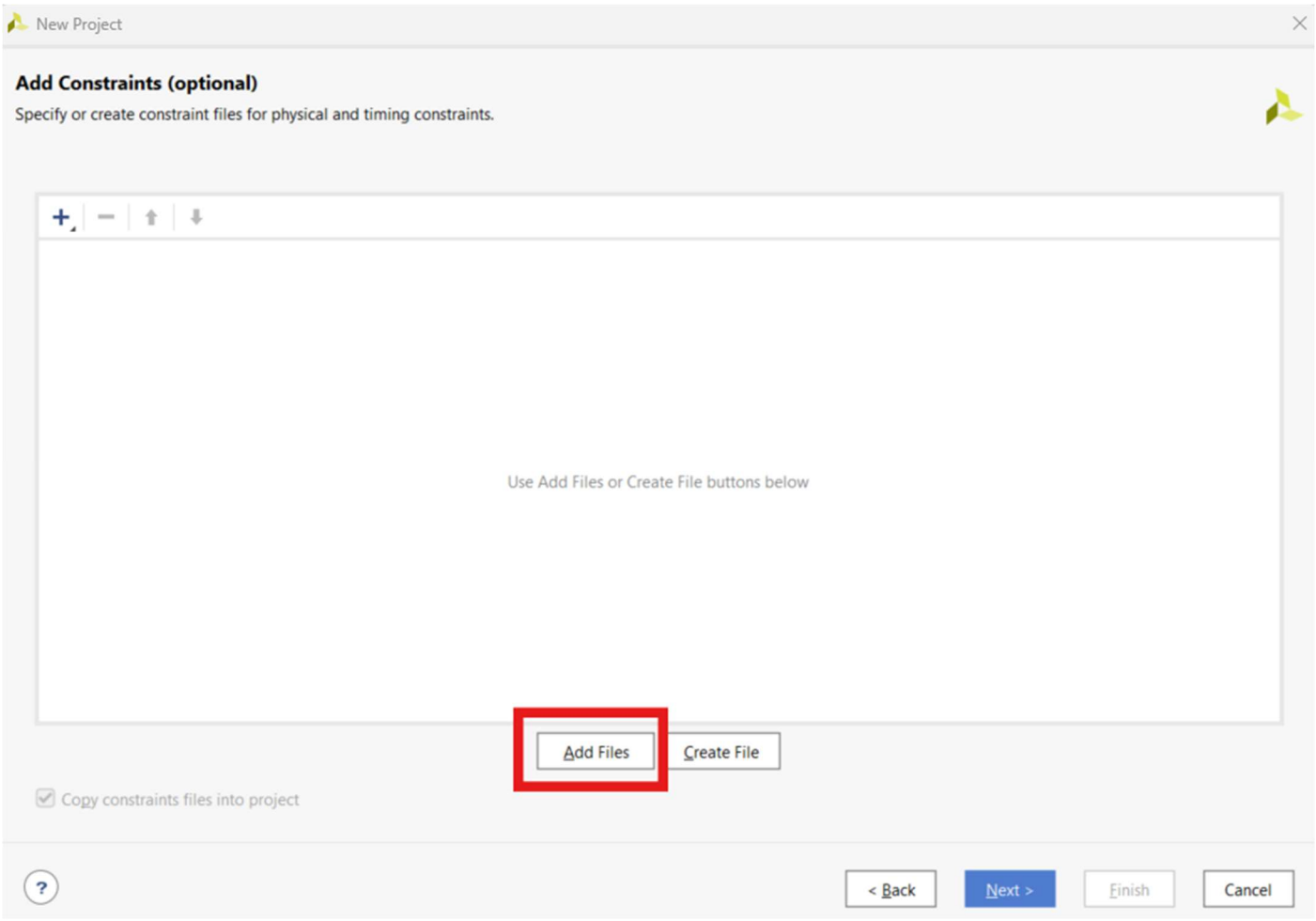

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: project_Getting_started
Project location: C:/Users/Dell/Documents/projects/EISLER_A7_V4
Create project subdirectory
Project will be created at: C:/Users/Dell/Documents/projects/EISLER_A7_V4/project_Getting_started
?
< Back
Next >
Finish
Cancel

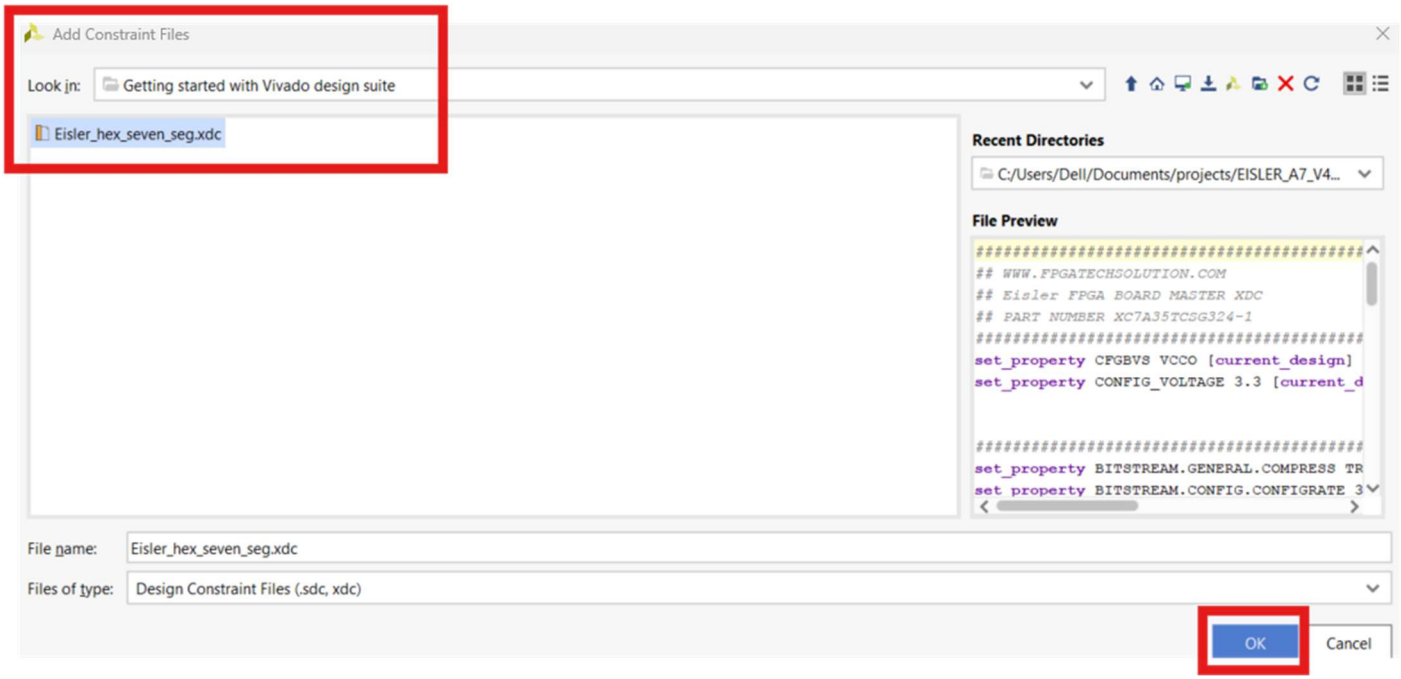

Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.

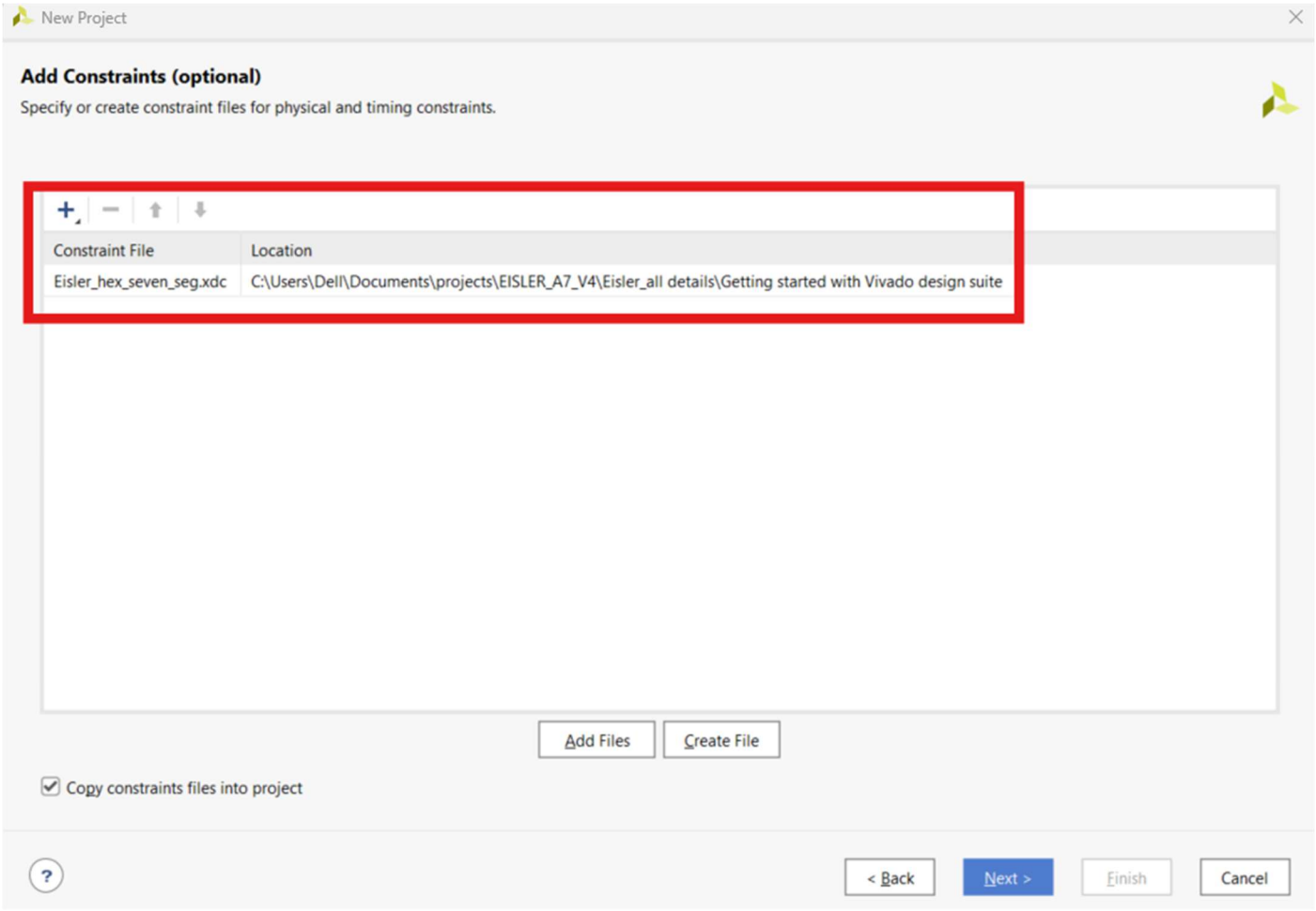

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: Verilog
Simulator language: Mixed
< Back
Next >
Finish
Cancel

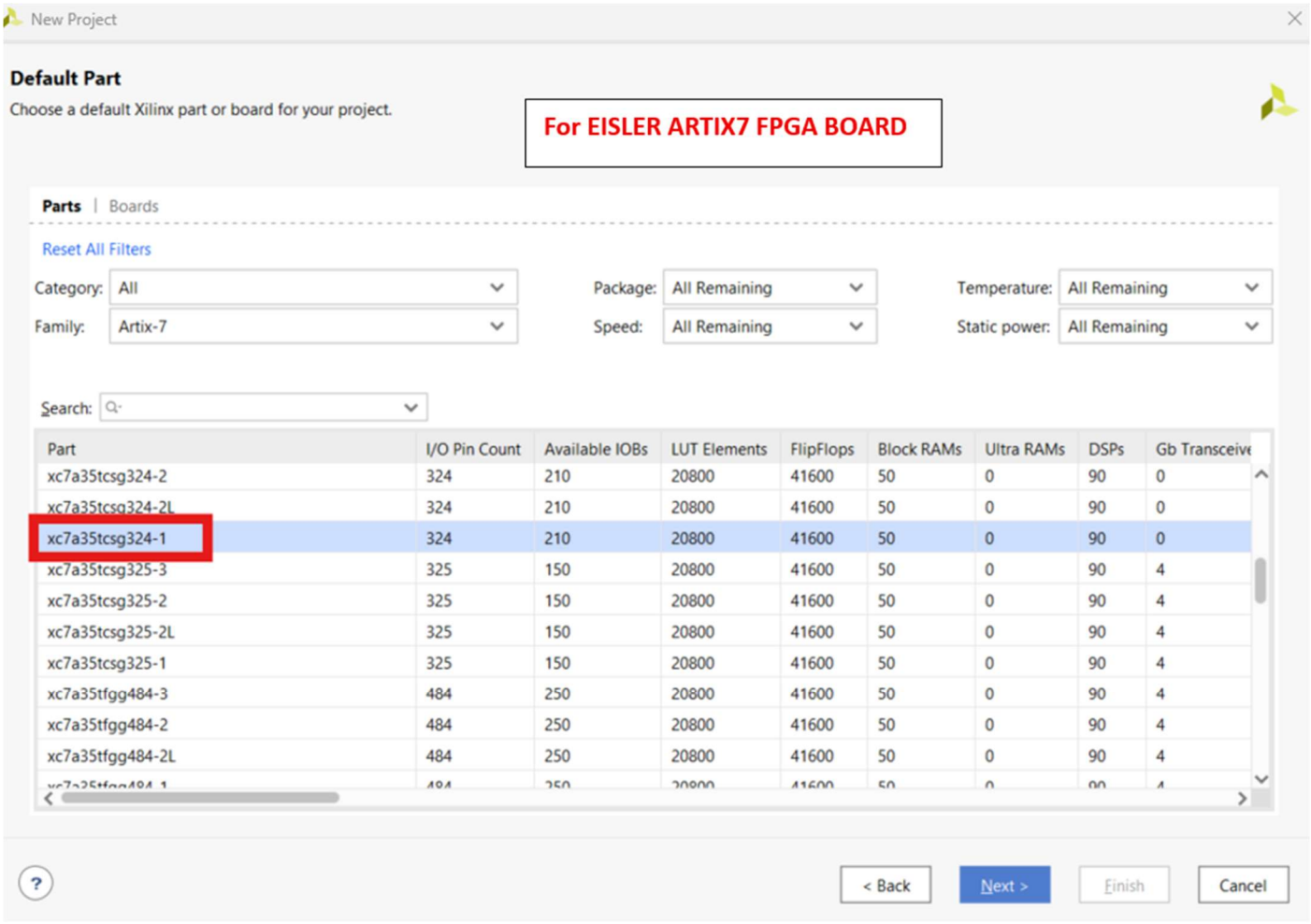

Add Source Files
Look in: Getting started with Vivado design suite
hex_seven_seg.vhd
SEVEN_SEGMENT.vhd
Recent Directories
C:/Users/Dell/Documents/projects/EISLER_A7_V4
File Preview
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
LIBRARY xil_defaultlib;
ENTITY hex_seven_seg IS
PORT(
osc_clk_in : IN STD_LOGIC;
KEY_0 :IN STD_LOGIC;
KEY_1 :IN STD_LOGIC;
File name: "hex_seven_seg.vhd" "SEVEN_SEGMENT.vhd"
Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verilog, vr, vg, vb, tf, vlog, vp, vm, veo, svo, vh, h, svh, vhp, svhp, edn, edf, edif, ngc, sv, svp, bmm, mif, mem, elf, dcp, bd, wcfg, xco, xci, xc..
OK
Cancel

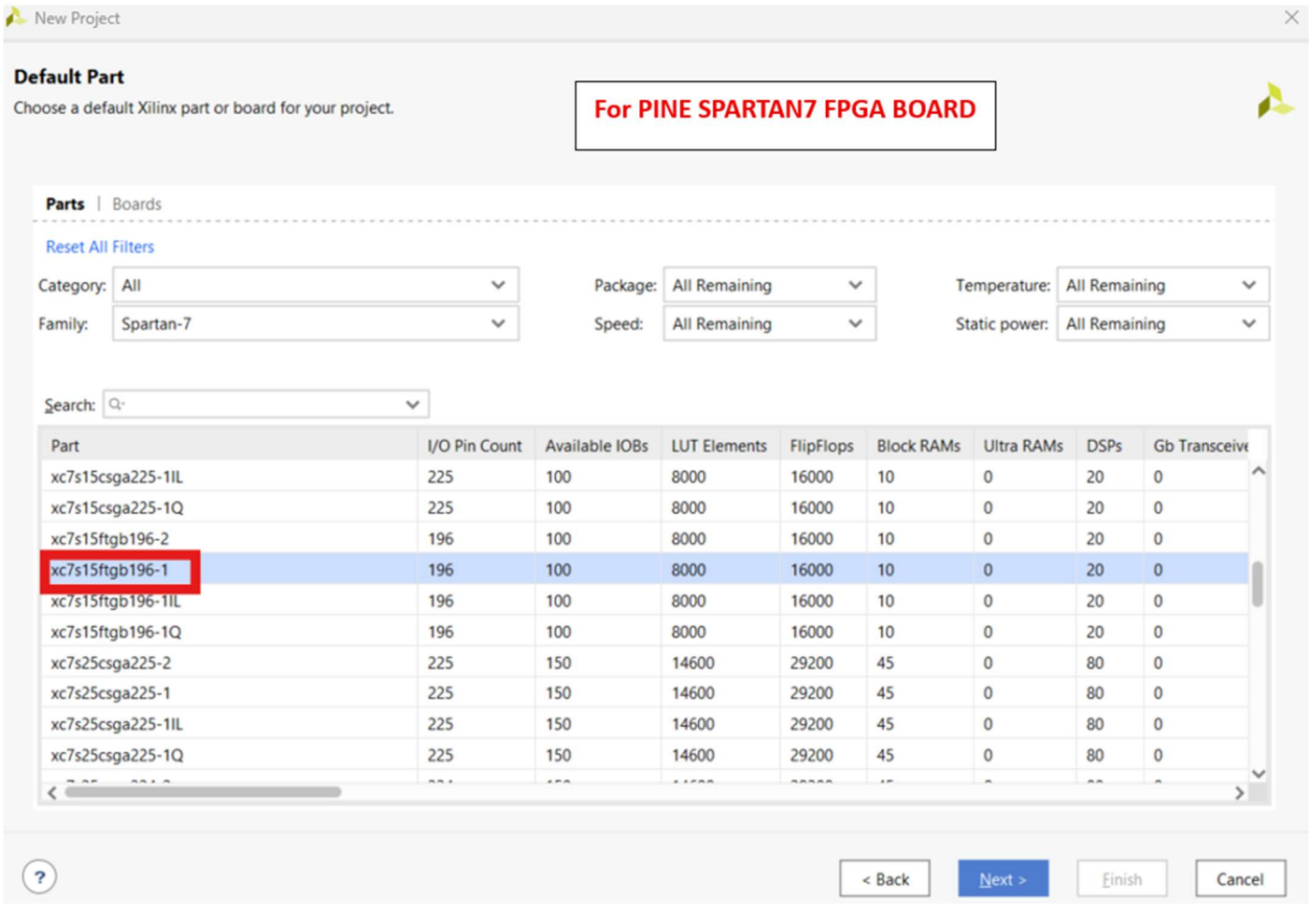

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Index
Name
Library
HDL Source For
Location
1
SEVEN_SEGMENT.vhd
xil_defaultlib
Synthesis & Simulation
C:/Users/Dell/Documents/projects/EISLER_A7_V4/Eisler_all details/Getting start
2
hex_seven_seg.vhd
xil_defaultlib
Synthesis & Simulation
C:/Users/Dell/Documents/projects/EISLER_A7_V4/Eisler_all details/Getting start
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language:
Verilog
Simulator language:
Mixed
< Back
Next >
Finish
Cancel

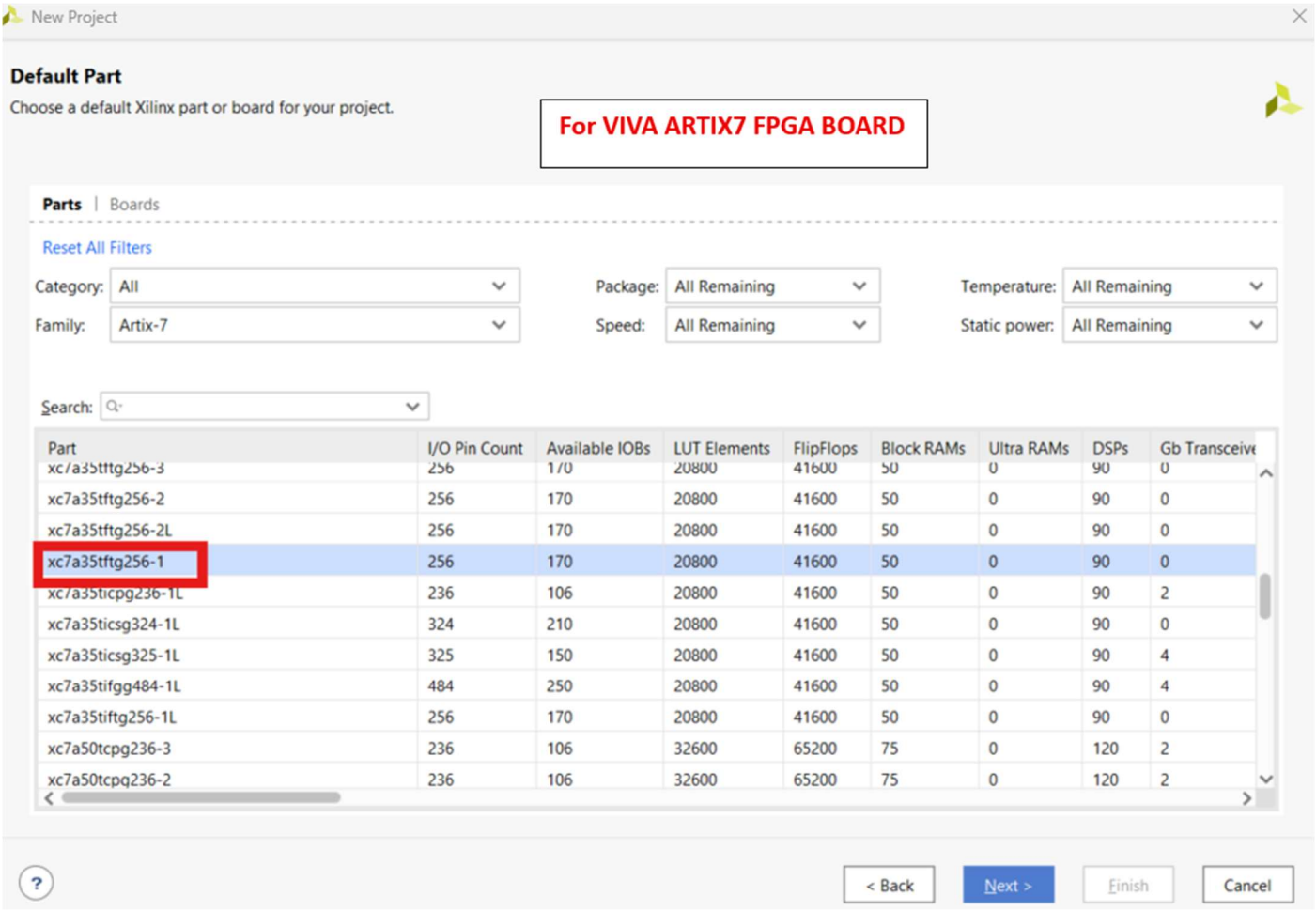

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

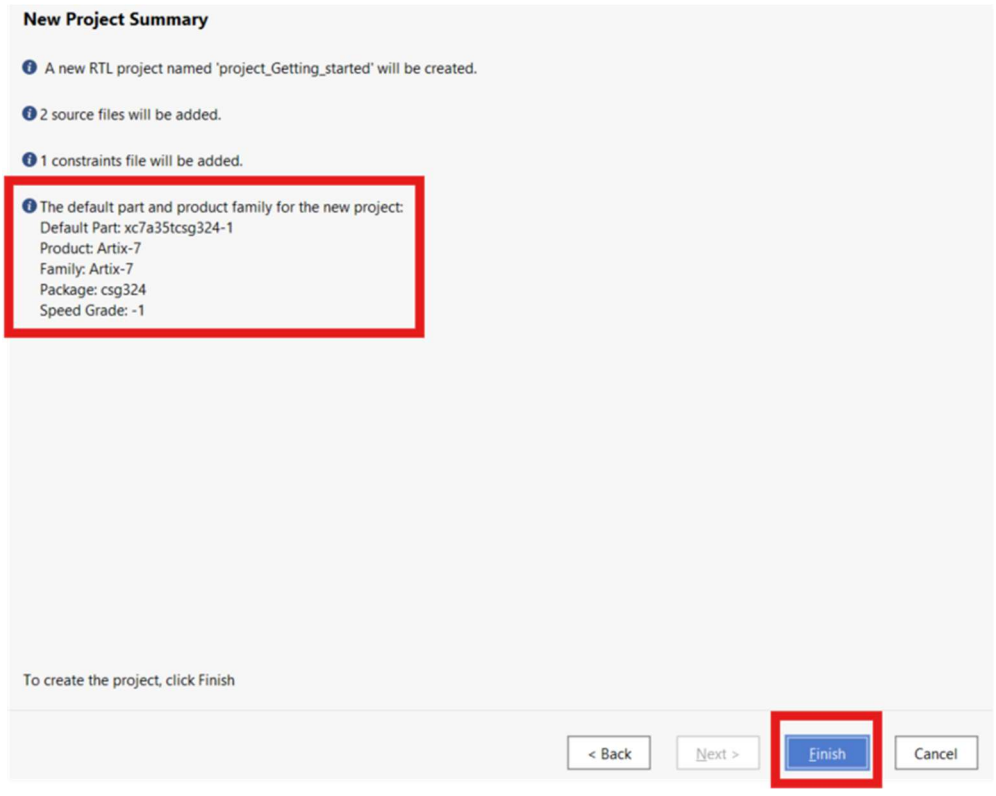

Add Constraint Files
Look in:
Getting started with Vivado design suite
Eisler_hex_seven_seg.xdc
Recent Directories
C:/Users/Dell/Documents/projects/EISLER_A7_V4...
File Preview
WWW.FPGATECHSOLUTION.COM
Eisler FPGA BOARD MASTER XDC
PART NUMBER XC7A35TCSG324-1
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_d
set_property BITSTREAM.GENERAL.COMPRESS TR
set_property BITSTREAM.CONFIG.CONFIGRATE 3
File name:
Eisler_hex_seven_seg.xdc
Files of type:
Design Constraint Files (.sdc, xdc)
OK
Cancel

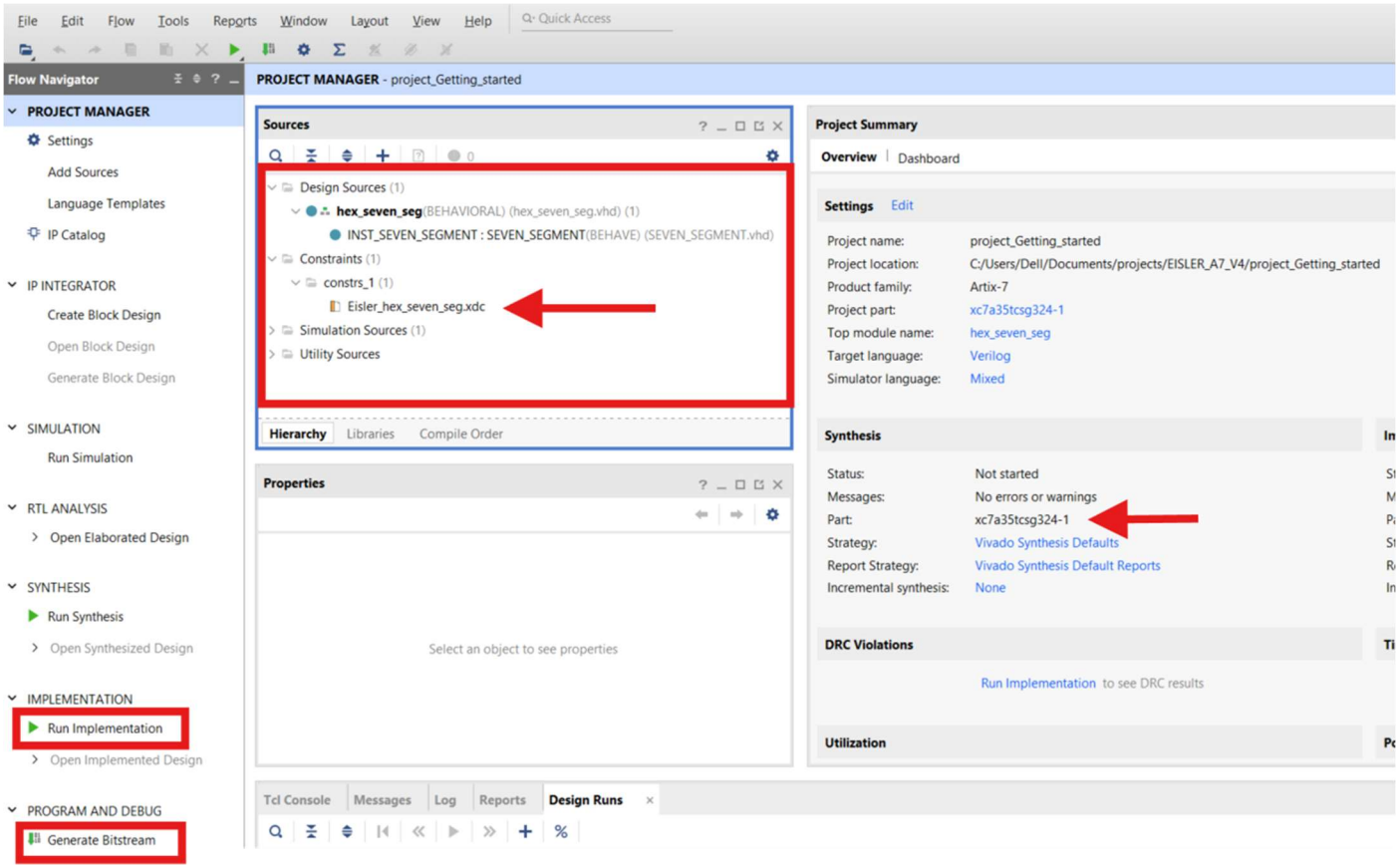

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Constraint File
Location
Eisler_hex_seven_seg.xdc
C:\Users\Dell\Documents\projects\EISLER_A7_V4\Eisler_all details\Getting started with Vivado design suite
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

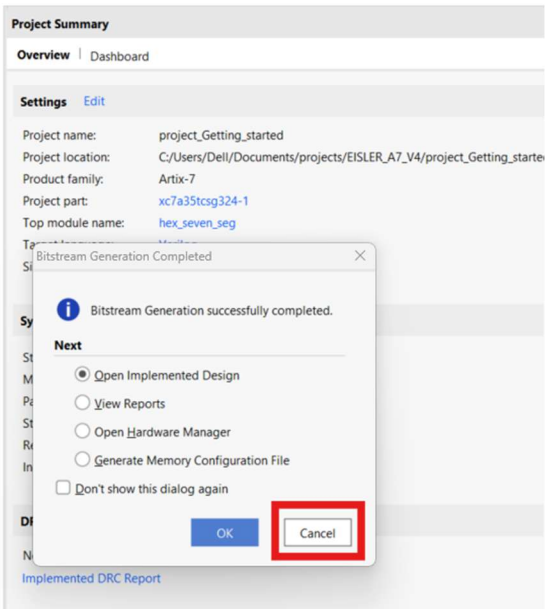

New Project
Default Part
Choose a default Xilinx part or board for your project.
For EISLER ARTIX7 FPGA BOARD
Parts | Boards
Reset All Filters
Category: All
Family: Artix-7
Package: All Remaining
Speed: All Remaining
Temperature: All Remaining
Static power: All Remaining
Search:
Part | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra RAMs | DSPs | Gb Transceiv
xc7a35tcsg324-2 | 324 | 210 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35tcsg324-2L | 324 | 210 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35tcsg324-1 | 324 | 210 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35tcsg325-3 | 325 | 150 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tcsg325-2 | 325 | 150 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tcsg325-2L | 325 | 150 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tcsg325-1 | 325 | 150 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tfgg484-3 | 484 | 250 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tfgg484-2 | 484 | 250 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tfgg484-2L | 484 | 250 | 20800 | 41600 | 50 | 0 | 90 | 4
< Back
Next >
Finish
Cancel

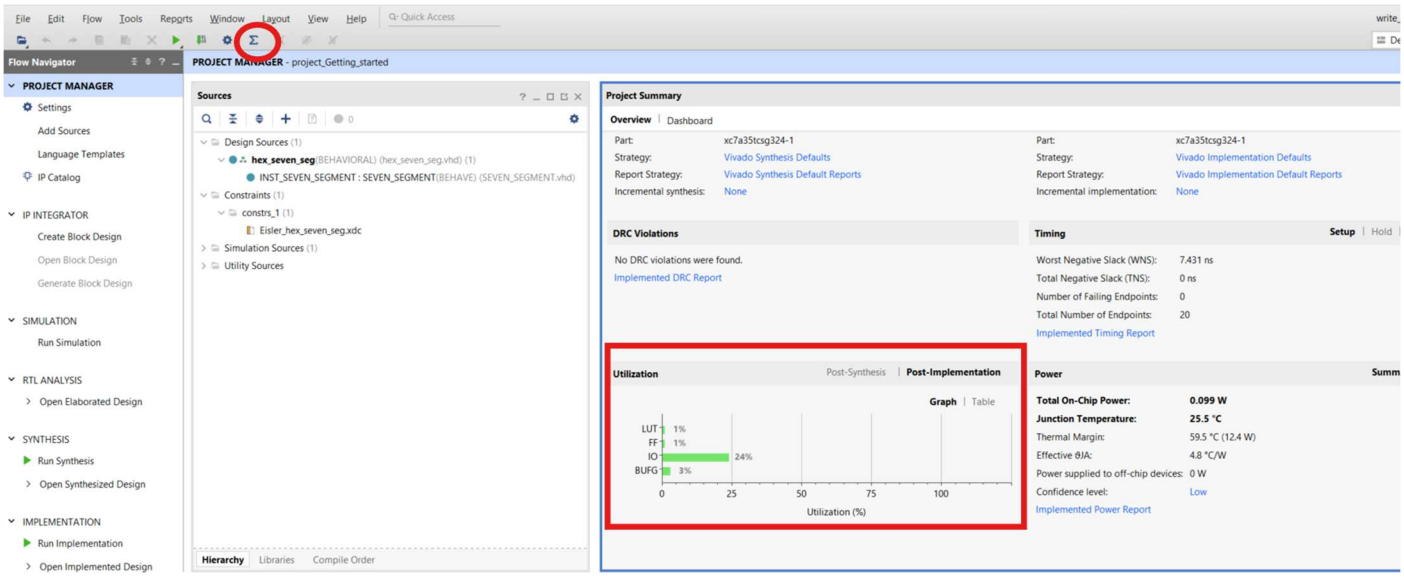

New Project
Default Part
Choose a default Xilinx part or board for your project.
For PINE SPARTAN7 FPGA BOARD
Parts | Boards
Reset All Filters
Category: All
Family: Spartan-7
Package: All Remaining
Speed: All Remaining
Temperature: All Remaining
Static power: All Remaining
Search:
Part | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra RAMs | DSPs | Gb Transceiv
xc7s15csga225-1IL | 225 | 100 | 8000 | 16000 | 10 | 0 | 20 | 0
xc7s15csga225-1Q | 225 | 100 | 8000 | 16000 | 10 | 0 | 20 | 0
xc7s15ftgb196-2 | 196 | 100 | 8000 | 16000 | 10 | 0 | 20 | 0
xc7s15ftgb196-1 | 196 | 100 | 8000 | 16000 | 10 | 0 | 20 | 0
xc7s15ftgb196-1IL | 196 | 100 | 8000 | 16000 | 10 | 0 | 20 | 0
xc7s15ftgb196-1Q | 196 | 100 | 8000 | 16000 | 10 | 0 | 20 | 0
xc7s25csga225-2 | 225 | 150 | 14600 | 29200 | 45 | 0 | 80 | 0
xc7s25csga225-1 | 225 | 150 | 14600 | 29200 | 45 | 0 | 80 | 0
xc7s25csga225-1IL | 225 | 150 | 14600 | 29200 | 45 | 0 | 80 | 0
xc7s25csga225-1Q | 225 | 150 | 14600 | 29200 | 45 | 0 | 80 | 0
< Back
Next >
Finish
Cancel

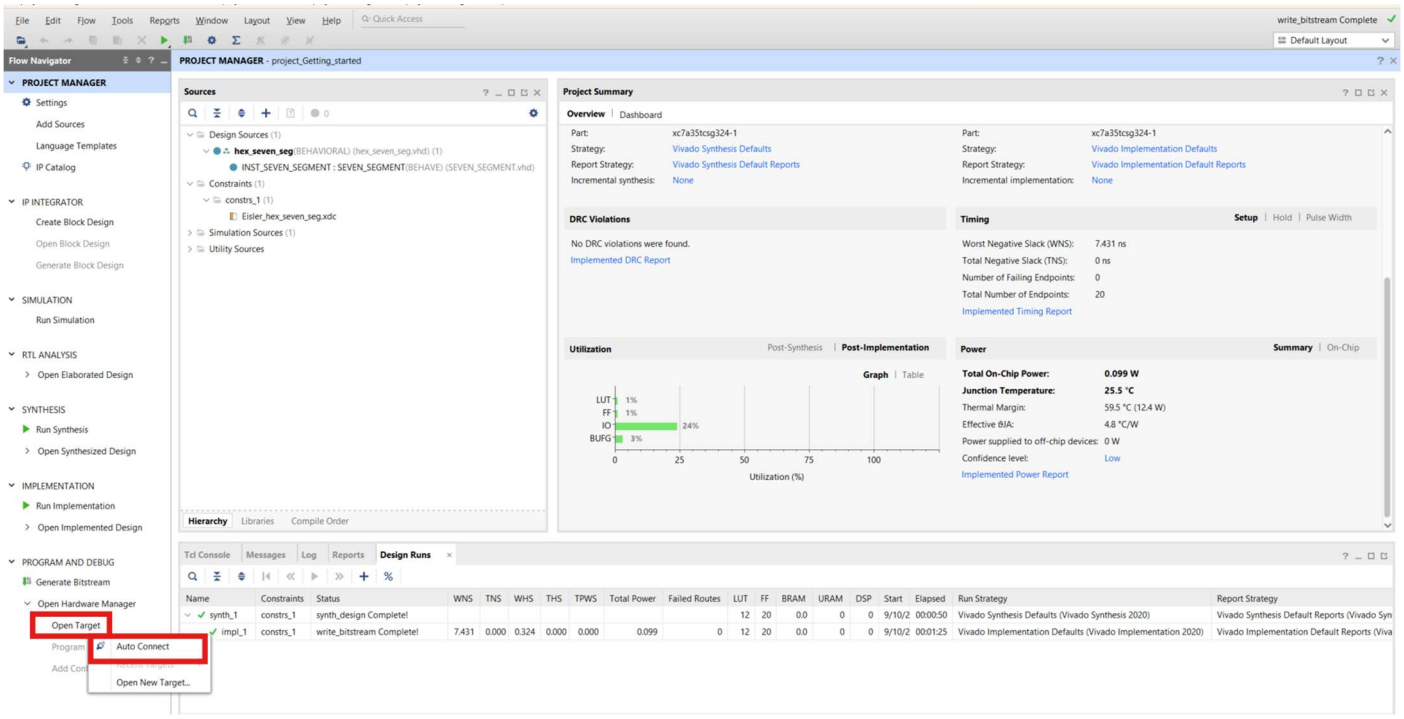

New Project
Default Part
Choose a default Xilinx part or board for your project.
For VIVA ARTIX7 FPGA BOARD
Parts | Boards
Reset All Filters
Category: All
Package: All Remaining
Temperature: All Remaining
Family: Artix-7
Speed: All Remaining
Static power: All Remaining
Search:
Part | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra RAMs | DSPs | Gb Transceiv
xc7a35tftg256-3 | 256 | 170 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35tftg256-2 | 256 | 170 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35tftg256-2L | 256 | 170 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35tftg256-1 | 256 | 170 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35ticpg236-1L | 236 | 106 | 20800 | 41600 | 50 | 0 | 90 | 2
xc7a35ticsg324-1L | 324 | 210 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a35ticsg325-1L | 325 | 150 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tifgg484-1L | 484 | 250 | 20800 | 41600 | 50 | 0 | 90 | 4
xc7a35tiftg256-1L | 256 | 170 | 20800 | 41600 | 50 | 0 | 90 | 0
xc7a50tcpg236-3 | 236 | 106 | 32600 | 65200 | 75 | 0 | 120 | 2
xc7a50tcpg236-2 | 236 | 106 | 32600 | 65200 | 75 | 0 | 120 | 2
< Back
Next >
Finish
Cancel


New Project Summary
A new RTL project named 'project_Getting_started' will be created.
2 source files will be added.
1 constraints file will be added.
The default part and product family for the new project:
Default Part: xc7a35tcsg324-1
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1
To create the project, click Finish
< Back
Next >
Finish
Cancel


File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER - project_Getting_started
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Sources
Design Sources (1)
hex_seven_seg(BEHAVIORAL) (hex_seven_seg.vhd) (1)
INST_SEVEN_SEGMENT : SEVEN_SEGMENT(BEHAVE) (SEVEN_SEGMENT.vhd)
Constraints (1)
constrs_1 (1)
Eisler_hex_seven_seg.xdc
Simulation Sources (1)
Utility Sources
Hierarchy Libraries Compile Order
Properties
Select an object to see properties
Project Summary
Overview Dashboard
Settings Edit
Project name: project_Getting_started
Project location: C:/Users/Dell/Documents/projects/EISLER_A7_V4/project_Getting_started
Product family: Artix-7
Project part: xc7a35tcsg324-1
Top module name: hex_seven_seg
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Not started
Messages: No errors or warnings
Part: xc7a35tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
DRC Violations
Run Implementation to see DRC results
Utilization
Tcl Console Messages Log Reports Design Runs

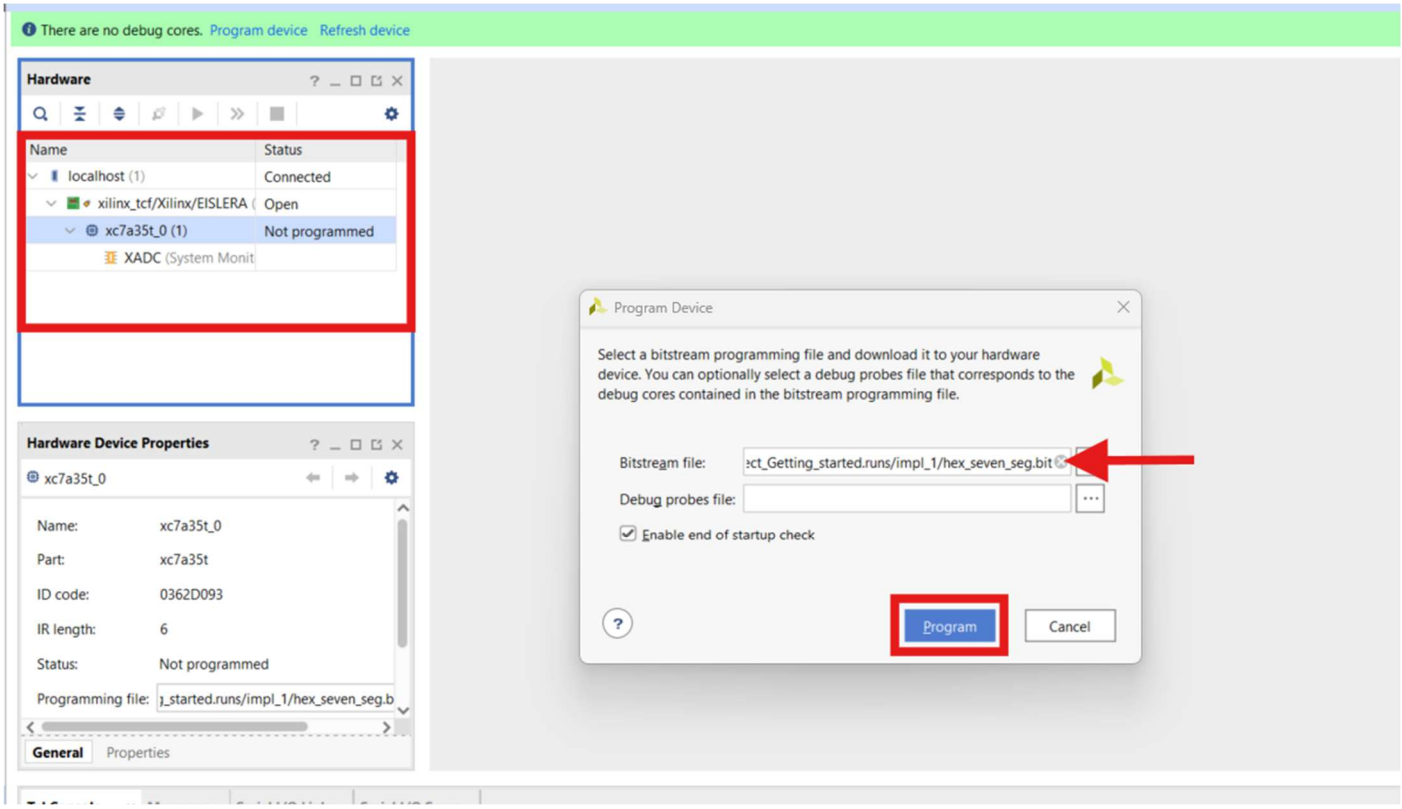

Project Summary
Overview Dashboard
Settings Edit
Project name: project_Getting_started
Project location: C:/Users/Dell/Documents/projects/EISLER_A7_V4/project_Getting_starte
Product family: Artix-7
Project part: xc7a35tcsg324-1
Top module name: hex_seven_seg
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel
Implemented DRC Report


File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER - project_Getting_started
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Sources
Design Sources (1)
hex_seven_seg(BEHAVIORAL) (hex_seven_seg.vhd) (1)
INST_SEVEN_SEGMENT : SEVEN_SEGMENT(BEHAVE) (SEVEN_SEGMENT.vhd)
Constraints (1)
constrs_1 (1)
Eisler_hex_seven_seg.xdc
Simulation Sources (1)
Utility Sources
Hierarchy Libraries Compile Order
Project Summary
Overview | Dashboard
Part: xc7a35tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Part: xc7a35tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
No DRC violations were found.
Implemented DRC Report
Timing Setup | Hold
Worst Negative Slack (WNS): 7.431 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 20
Implemented Timing Report
Utilization Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
FF 1%
IO 24%
BUFG 3%
0 25 50 75 100
Utilization (%)
Power
Total On-Chip Power: 0.099 W
Junction Temperature: 25.5 °C
Thermal Margin: 59.5 °C (12.4 W)
Effective θJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report

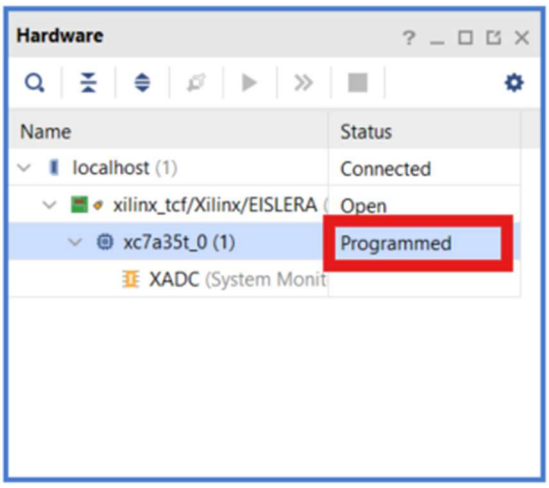

File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
PROJECT MANAGER - project_Getting_started
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Auto Connect
Open New Target...
Sources
Design Sources (1)
hex_seven_seg(BEHAVIORAL) (hex_seven_seg.vhd) (1)
INST_SEVEN_SEGMENT : SEVEN_SEGMENT(BEHAVE) (SEVEN_SEGMENT.vhd)
Constraints (1)
constrs_1 (1)
Eisler_hex_seven_seg.xdc
Simulation Sources (1)
Utility Sources
Hierarchy Libraries Compile Order
Project Summary
Overview | Dashboard
Part: xc7a35tcsg324-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Part: xc7a35tcsg324-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
No DRC violations were found.
Implemented DRC Report
Timing Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 7.431 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 20
Implemented Timing Report
Utilization Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
FF 1%
IO 24%
BUFG 3%
0 25 50 75 100
Utilization (%)
Power Summary | On-Chip
Total On-Chip Power: 0.099 W
Junction Temperature: 25.5 °C
Thermal Margin: 59.5 °C (12.4 W)
Effective θJA: 4.8 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy
synth_1 constrs_1 synth_design Complete! 12 20 0.0 0 0 9/10/2 00:00:50 Vivado Synthesis Defaults (Vivado Synthesis 2020) Vivado Synthesis Default Reports (Vivado Syn
impl_1 constrs_1 write_bitstream Complete! 7.431 0.000 0.324 0.000 0.000 0.099 0 12 20 0.0 0 0 9/10/2 00:01:25 Vivado Implementation Defaults (Vivado Implementation 2020) Vivado Implementation Default Reports (Viva

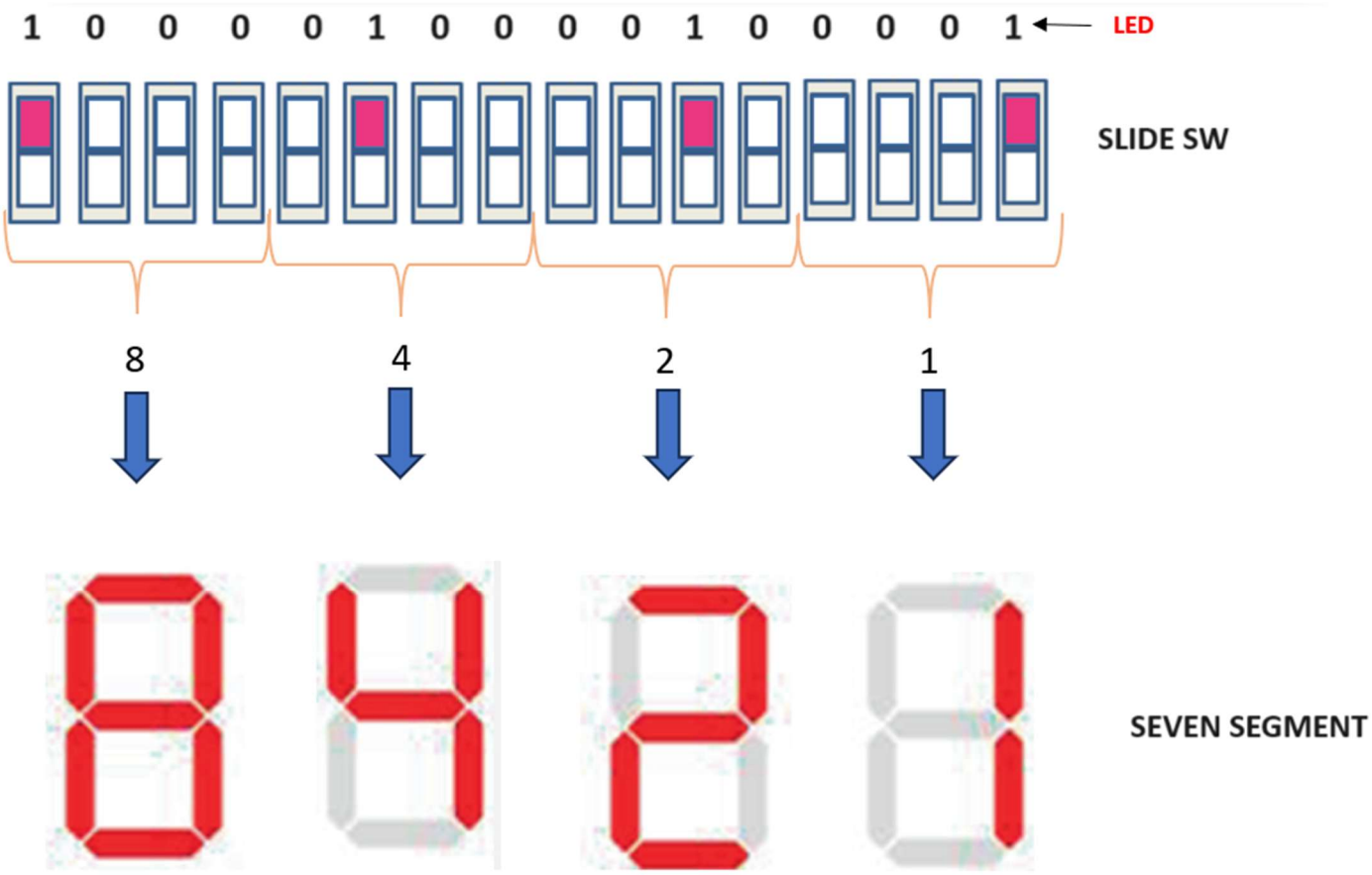
Open Hardware Manager

Make sure board is powered on & USB connector is connected to computer properly



Now check output on board




1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1
LED
SLIDE SW
8
4
2
1
SEVEN SEGMENT