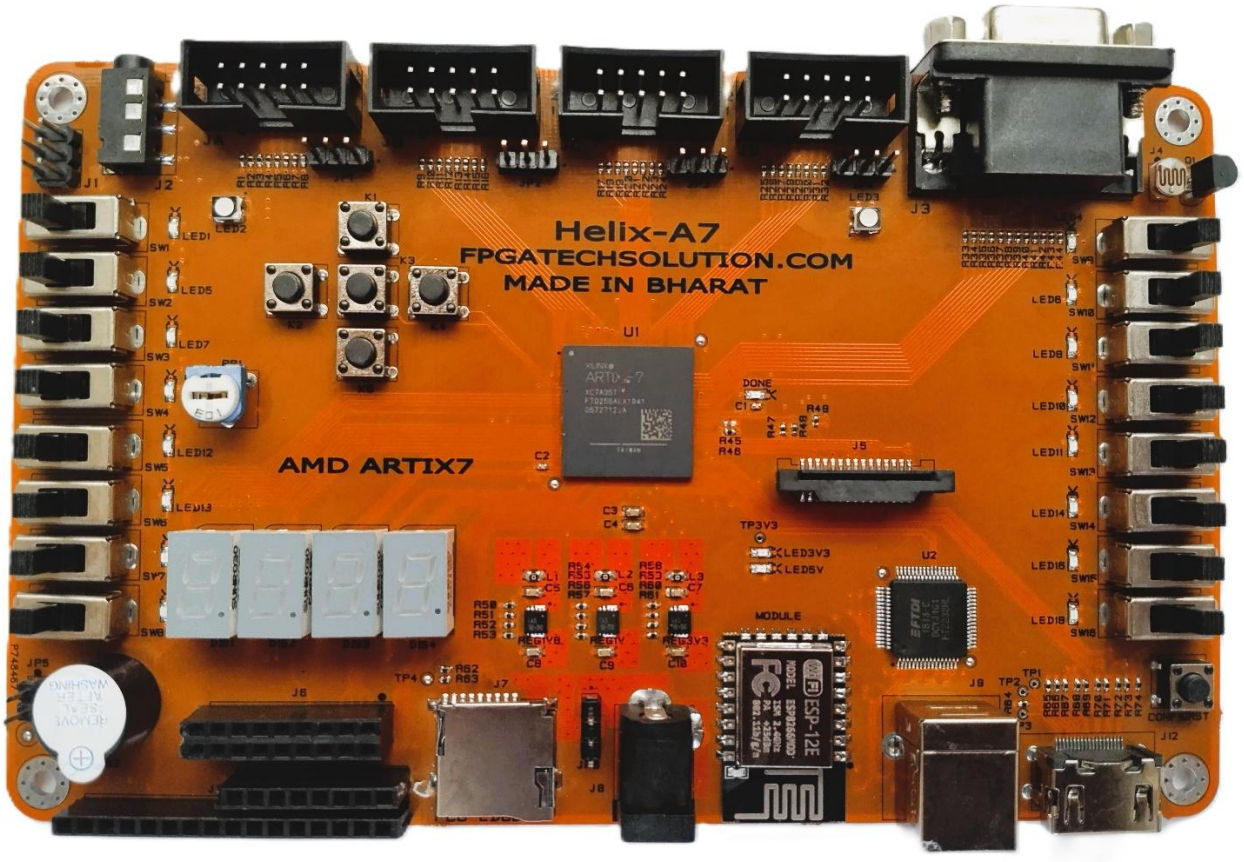
MANUAL EISLER A7

FPGA TECH SOLUTION

...SOLUTION AHEAD



Introduction

The HELIX ARTIX7 FPGA board is a complete, ready-to-use digital circuit development platform based on the latest Artix7 Field Programmable Gate Array (FPGA) from Xilinx. With its high-capacity FPGA (Xilinx part number **XC7A35TFTG256-1**), low overall cost, and collection of USB, VGA, and other ports, the HELIX ARTIX7 FPGA can host designs ranging from introductory combinational circuits to complex sequential circuits like embedded processors and controllers. It includes enough switches, LEDs and other I/O devices to allow a large number designs to be completed without the need for any additional hardware, and enough uncommitted FPGA I/O pins to allow designs to be expanded using PMODs or other custom boards and circuits.

The HELIX ARTIX7 FPGA board has on board USB JTAG which support Vivado & vitis.

No need to purchases license, works 100% fine with webpack license

Applications

- Product Prototype Development
- Development and testing of custom embedded processors
- Signal Processing
- Communication devices development
- Educational tool for Schools and Universities

Features

The Artix-7FPGA is optimized for high performance logic, and offers more capacity, higher performance, and more resources than earlier designs. Artix-7 XC7A35TFTG256-1 features include:

- 12,800 logic cells in 5000 slices (each slice contains four 6-input LUTs and 8 flip-flops);
- 360 Kbits of fast block RAM;
- Two clock management tiles, each with a phase-locked loop (PLL);
- 20 DSP slices;
- Internal clock speeds exceeding 450MHz;

The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 also offers an improved collection of ports and peripherals, including:

- OSCILLATOR – 100MHz
- QFLASH –32Mb
- MIPI CSI camera connector
- LM35 temperature sensor connected to XADC pin
- LDR connected to XADC pin
- POT connected to XADC pin
- 16 user switches
- 16 user LEDs
- 5 user pushbuttons
- 100MHz clock
- 4-digit 7-segment display
- 4 PMOD (support digilent PMOD)
- Buzzer
- HDMI
- 8Bit SPI DAC
- SD CARD
- Audio 3.5mm Jack
- 2RGB LED
- 12bit VGA output
- USB-UART Bridge
- USB-JTAG port for FPGA programming and communication (support Vivado)

Add on modules (extra cost) compatible with HELIX ARTIX7 FPGA BOARD Artix7 FPGA A7 are available as follows

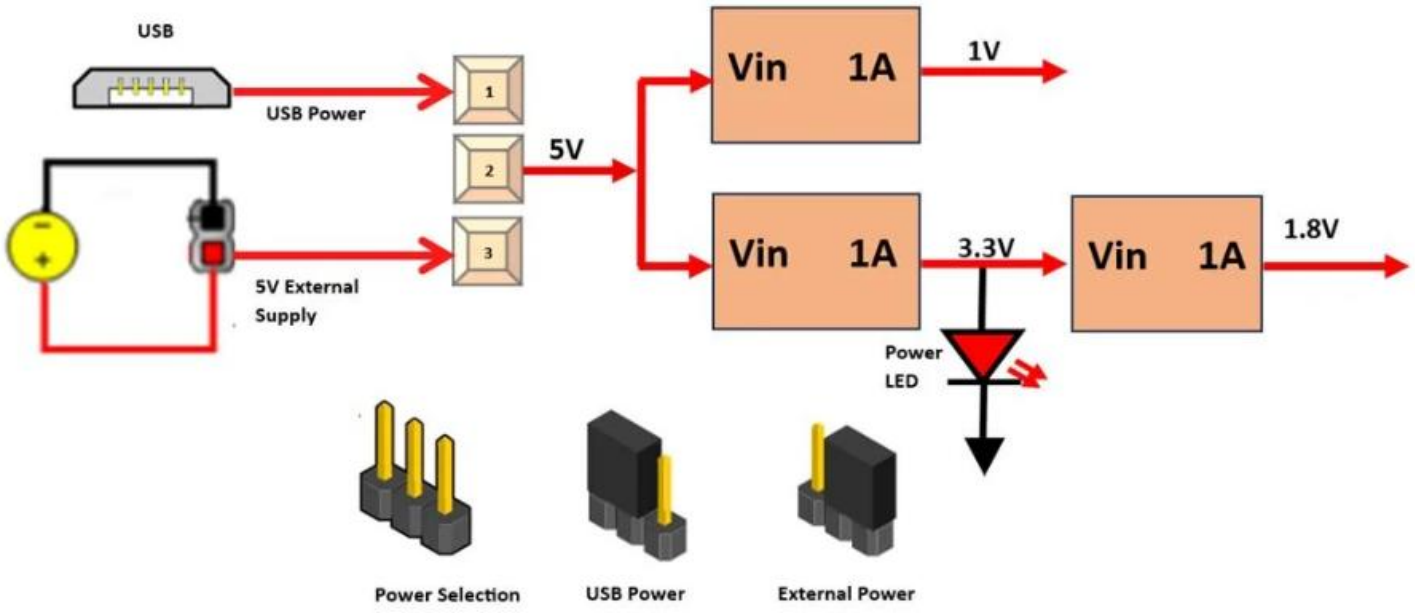
4X4 Matrix keyboard
OV7670VGA camera
TFT display
WIFI module
Bluetooth module
OLED display
wooden box

Software--The first Vivado Design Suite Exclusive: **(Recommended Vivado 19.1 OR 20.2)**

The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 works with Xilinx's new high-performance Vivado ® Design Suite. Vivado includes many new tools and design flows that facilitate and enhance the latest design methods. It runs faster, allows better use of FPGA resources, and allows designers to focus their time evaluating design alternatives. The System Edition includes an on-chip logic analyzer, high-level synthesis tool, and other cutting-edge tools, and the free "WebPACK" version allows HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 designs to be created at no additional cost.

BOARD POWERING

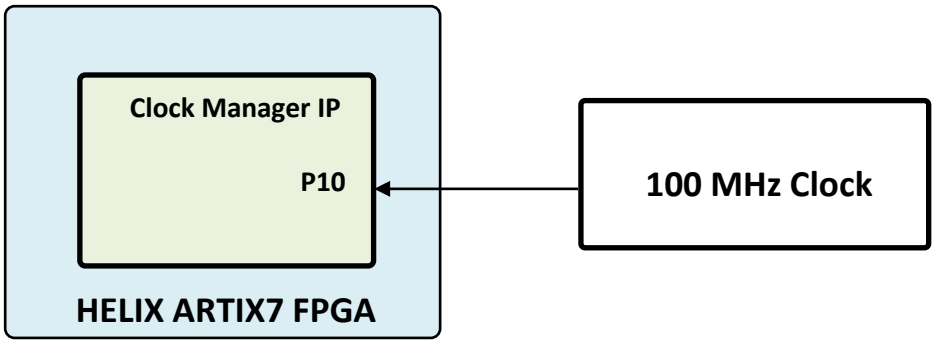
The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 uses +5V power supply to function properly. By default the board is configured to use +5V supply from USB. So an external +5V power is not required unless USB port is unable to supply enough current. In most cases USB ports are capable of providing enough current for the module. Current requirement for this board largely depends on your application. Please consult FPGA data sheet for more details on power requirements. If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly as shown below When JP6 jumper is placed towards USB as shown in below image power is used from USB connector & when JP6 jumper is placed towards power connector power is used from external connector



Oscillators/ Clocks

The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 board includes a single 100MHz oscillator connected to pin P10 (P10 is a MRCC input on bank 14). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100MHz input clock. For a full description of these rules and of the capabilities of the Artix-7clocking resources, refer to the “7 Series FPGAs Clocking Resources User Guide” available from

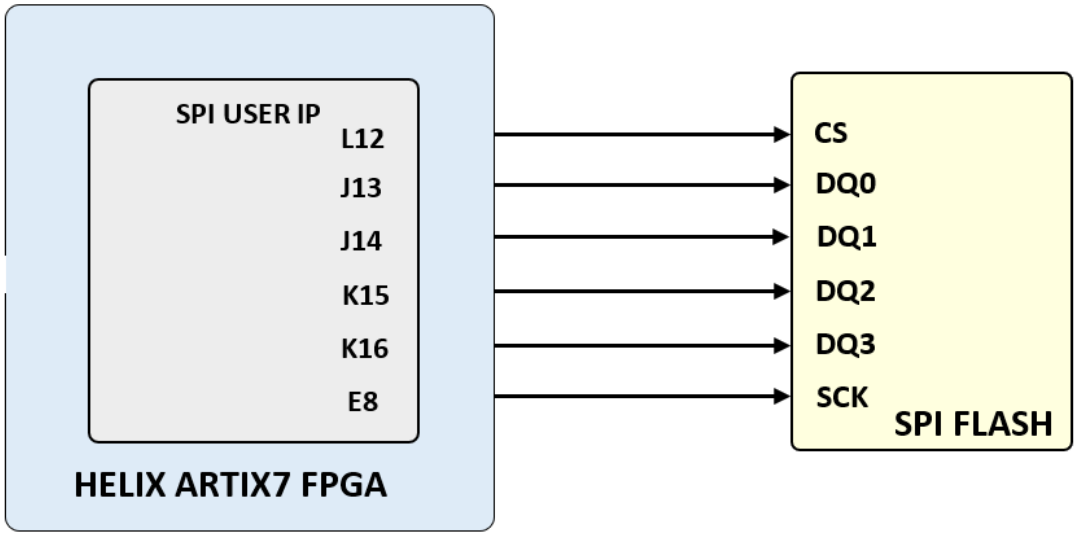
Xilinx http://www.xilinx.com/support/documentation/user_guides/ug472_7Series_Clocking.pdf.



Xilinx offers the Clocking Wizard IP core to help users generate the different clocks required for a specific design. This wizard properly instantiates the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy to use wrapper component around these clocking resources that can be inserted into the user’s design. The Clocking Wizard can be accessed from within IP Catalog, which can be found under the Project Manager section of the Flow Navigator in Vivado.

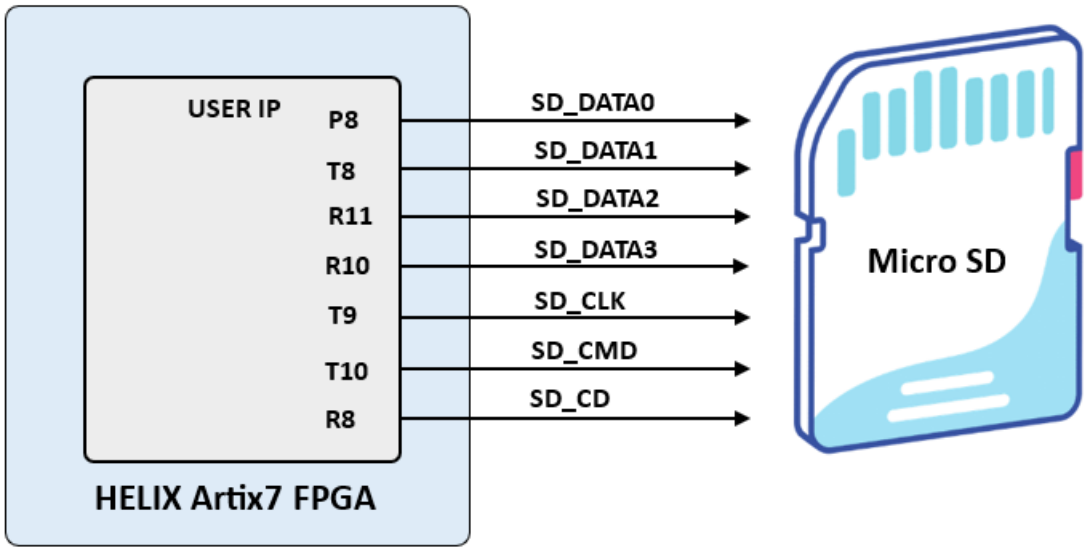
SPI FLASH

The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 board contains a 32Mbit non-volatile serial Flash device, which is attached to the Spartan 7 FPGA using a dedicated quad-mode (x4) SPI bus. The connections and pin assignments between the FPGA and the serial flash device are shown the below figure



HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 have been loaded with a Flash device from Maronix (part number MX25L3233FM1I-08G).FPGA configuration files can be written to the Quad SPI Flash, and mode settings are available to cause the FPGA to automatically read a configuration from this device at power on. An FPGA configuration file requires just over one Mbytes of memory, leaving approximately 98% of the flash device available for user data.

SD Card

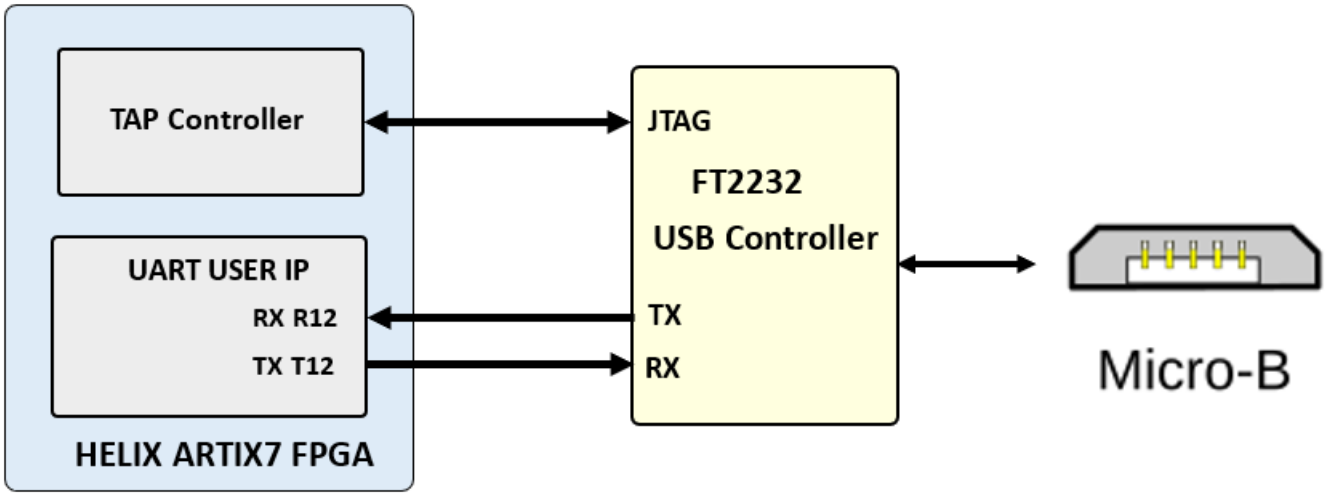


USB-UART Bridge (Serial Port)

The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 includes an FTDI FT2232HL

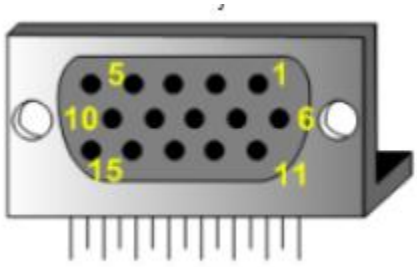
http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232H.pdf USB-UART bridge (attached to connector J9) that allows you to use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the “Virtual Com Port” or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on FPGA pins.

The FT2232HL is also used as the controller for the USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable. The connections between the FT2232H and the Artix-7 are shown in the below figure.

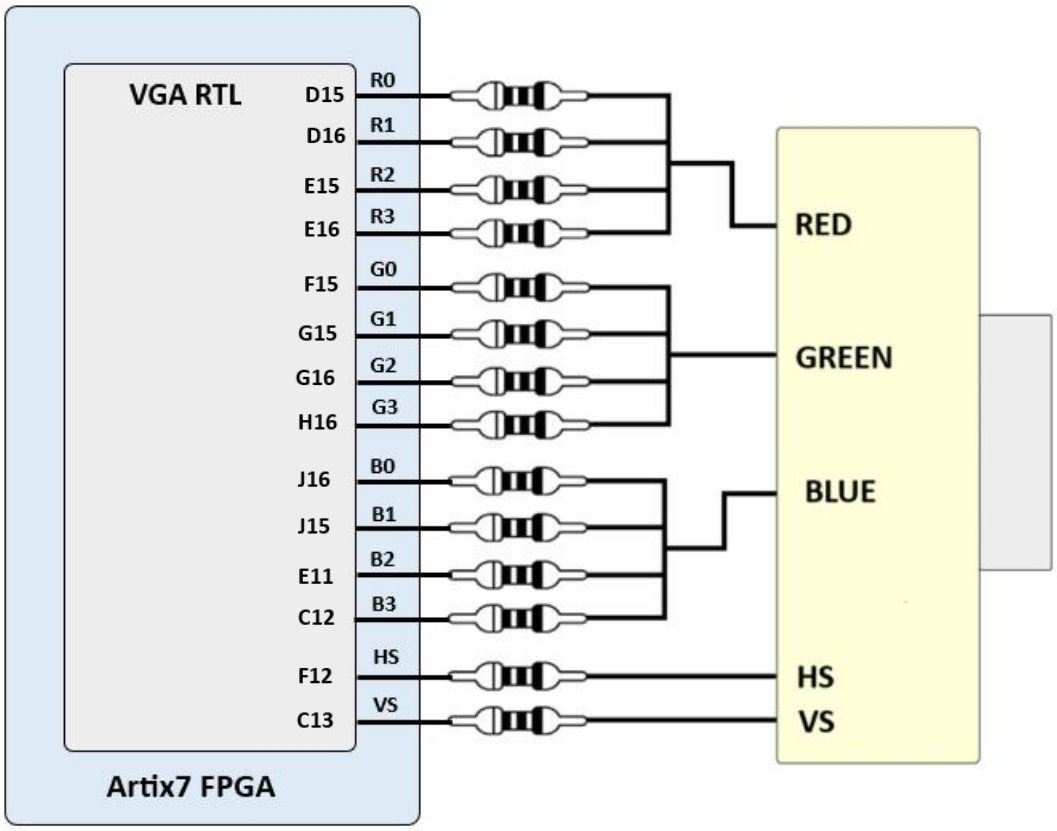


VGA Port

The HELIX ARTIX7 FPGA board uses 5 FPGA signals to create a VGA port with 1 bits-per-color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 82-ohm termination resistance of the VGA display to create 16 signal levels each on the red, green, and blue VGA signals.



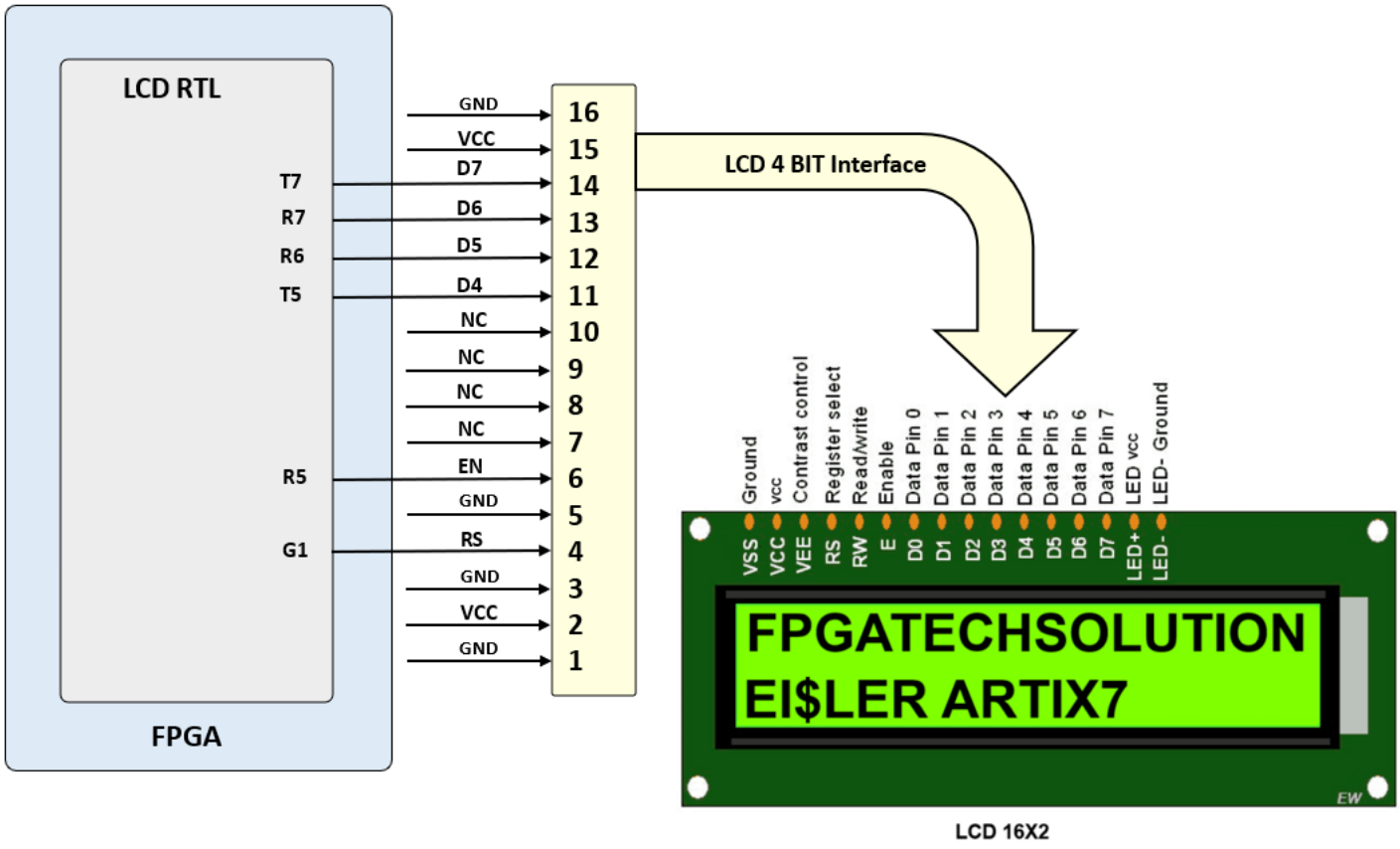
Pin 1: Red	Pin 5: GND
Pin 2: Grn	Pin 6: Red GND
Pin 3: Blue	Pin 7: Grn GND
Pin 13: HS	Pin 8: Blu GND
Pin 14: VS	Pin 10: Sync GND



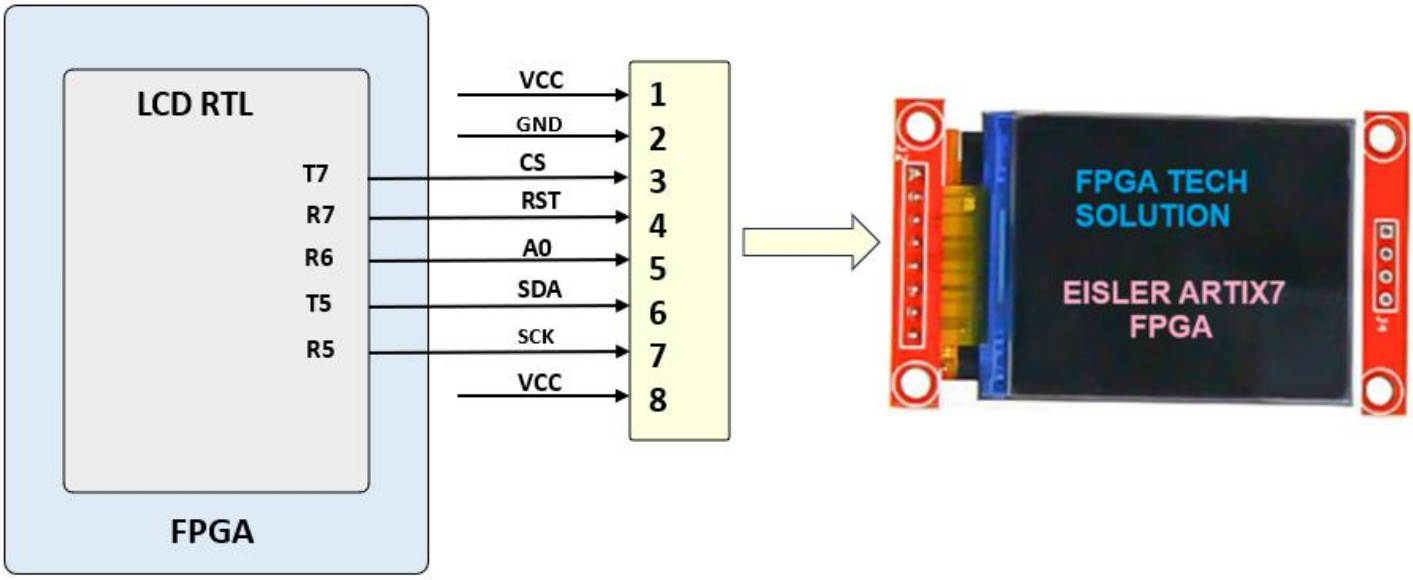
This circuit, shown in the above diagram, , produces video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 4096 different colors can be displayed, one for each unique 3-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

LCD Interface

The HELIX ARTIX7 FPGA board includes LCD16BY2 can be connected as show in following fig.
LCD16BY2 is connected with 4bit interface mode
Note: Either TFT LCD or 16BY2 LCD can be used at a time



LCD 16X2

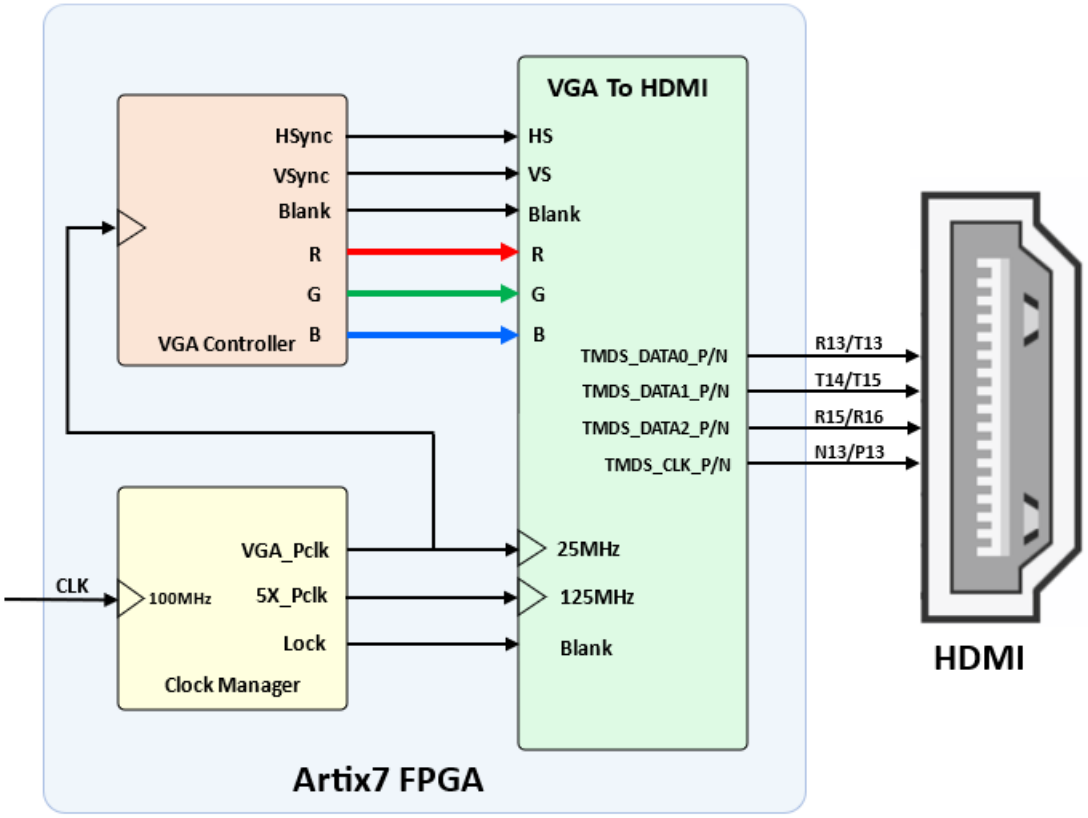


HDMI Interface

To interface an FPGA with HDMI, you need to understand both the FPGA architecture and the HDMI standard. HDMI transmits high-quality digital video and creating a proper interface involves generating the correct signals and protocols on the FPGA side.

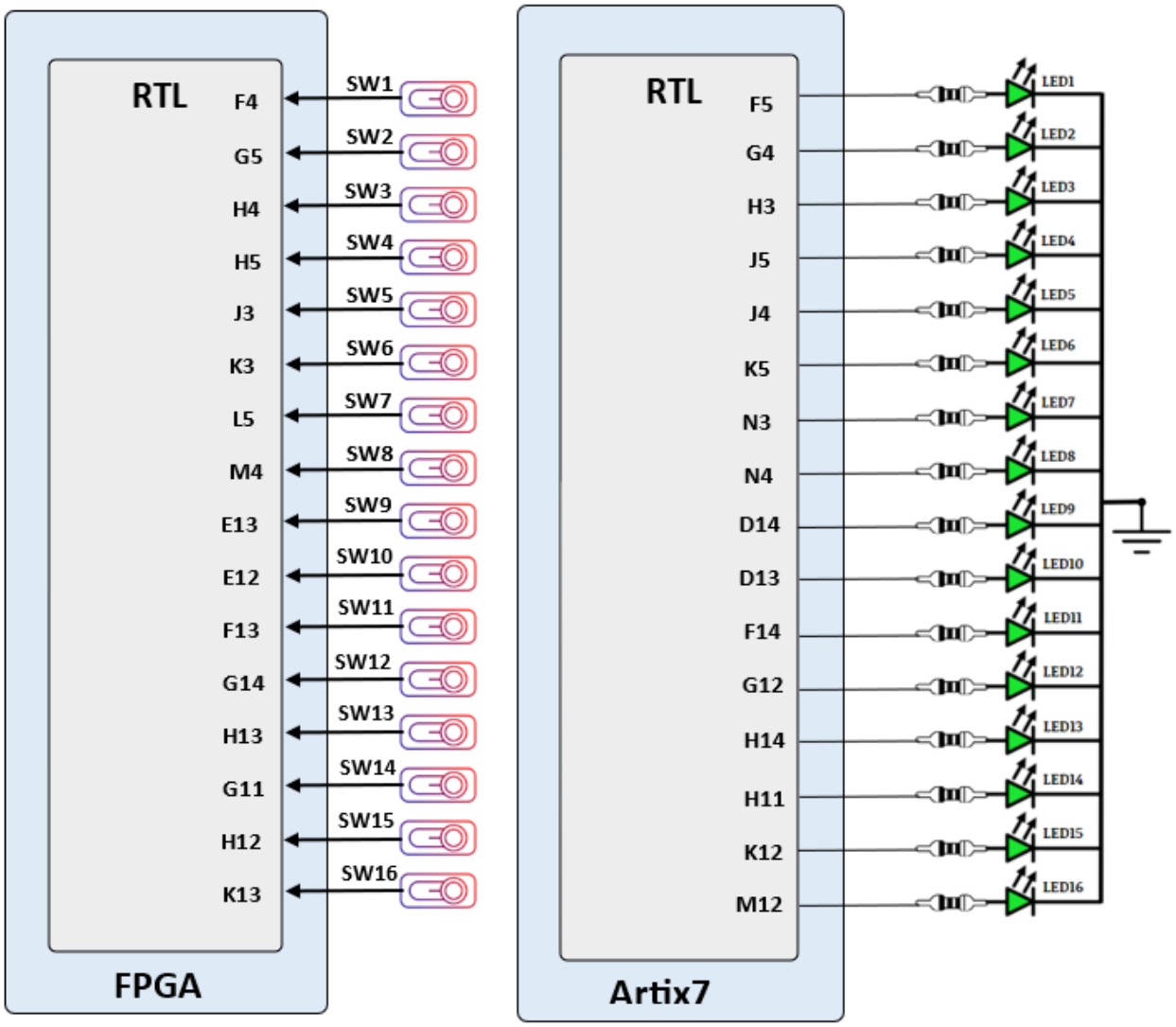
Key Components of an FPGA HDMI Interface:

1. **TMDS Encoding (Transition-Minimized Differential Signalling)**: HDMI uses TMDS to transmit video data. The TMDS encoding must be implemented in the FPGA, as HDMI expects this kind of signalling. This can be done using dedicated IP cores or by writing custom Verilog/VHDL code.
2. **Clock Signals**: HDMI requires specific clock signals to be transmitted along with the video data. The pixel clock is derived from the resolution and frame rate of the video. For example:
   - 640x480 @ 60Hz typically uses a 25.175 MHz clock.
   - 1920x1080 @ 60Hz uses a 148.5 MHz clock. Some FPGAs have dedicated PLL (Phase-Locked Loops) to generate these clock signals accurately.
3. **HDMI Video Data**: The video data (RGB or YCbCr) is packed into specific formats for HDMI transmission. Typically, a 24-bit (8-bit per channel) color depth is used for standard HDMI video. The data is sent at a specific rate depending on the resolution and refresh rate.



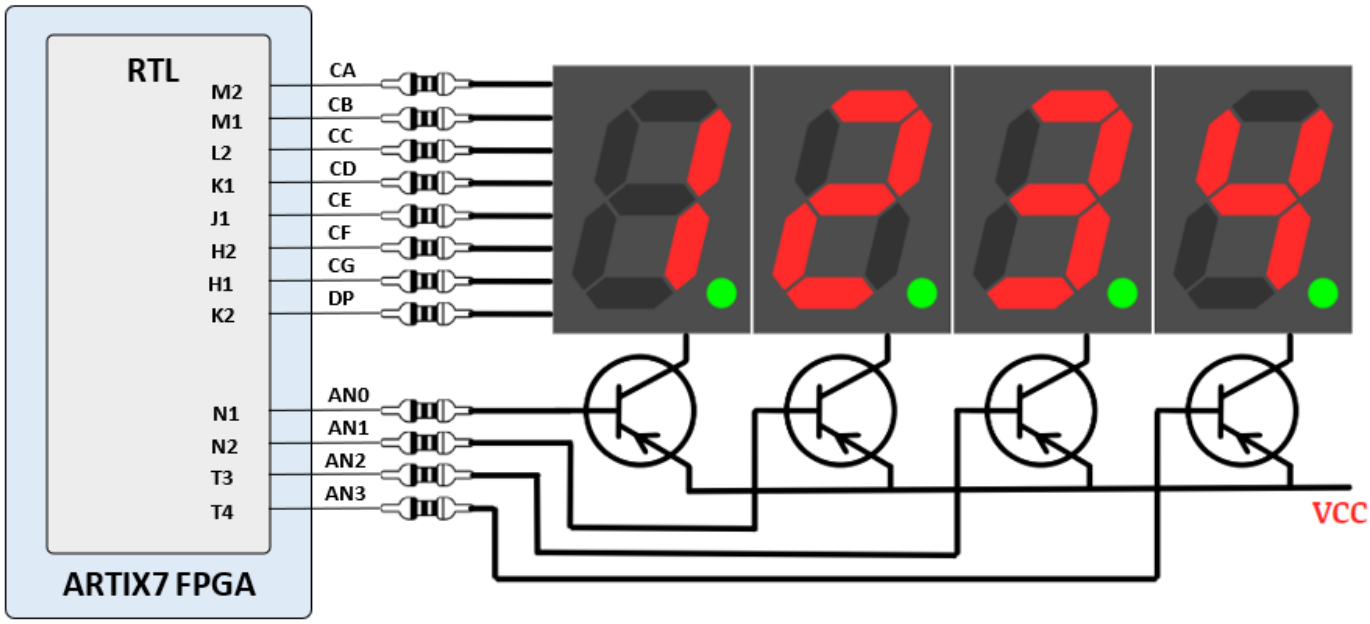
Basic I/O

The HELIX ARTIX7 FPGA BOARD ARTIX7 FPGA A7 board includes sixteen slide switches, four push buttons, sixteen individual LEDs, and a four-digit seven-segment display, as shown in the below diagram. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The four pushbuttons are “momentary” switches that normally generate a high output when they are at rest, and a low output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.



Seven Segment

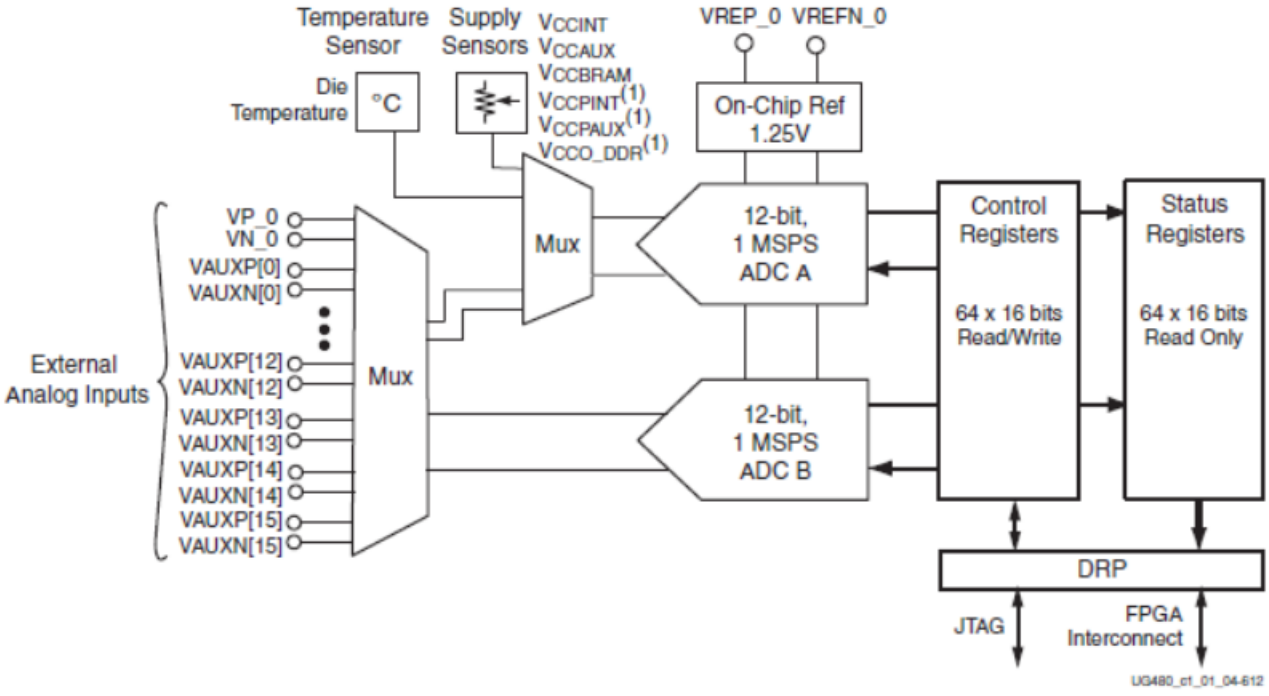
The HELIX ARTIX7 FPGA board includes 4 common Anode seven segment display as show in following fig.



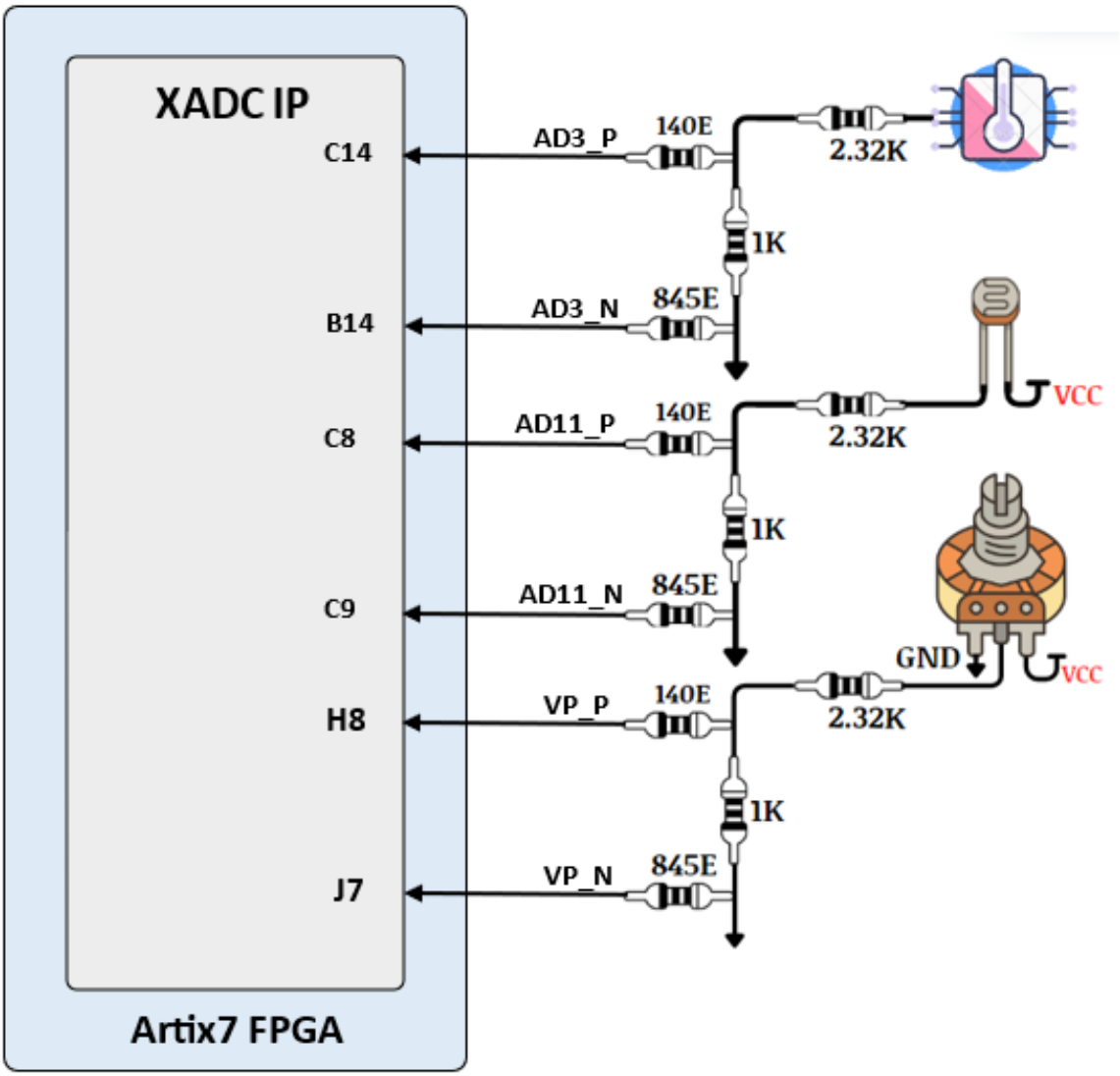
XADC

The Artix 7 FPGA chip used on the HELIX FPGA board is designed with the user in mind to provide high volume processing power for a relatively low cost. It has many powerful features including an on-board Analog-to-Digital converter (ADC) called the “XADC” available on 7 series FPGA devices provided by Xilinx. It is a dual 12-bit, 1 Mega sample per second (MSPS) ADC used to accommodate sampling for up to 17 auxiliary signals as well as including on-chip sensors for temperature and power monitoring.

The XADC supports a wide range of operating modes such as single channel, sequenced channel, dual ADC simultaneous sequence, or one-pass sequence channel sampling; event driven or continuous sampling operation; unipolar, differential, or bipolar signal sampling; etc… The XADC can also be configured to power down its individual ADCs, rearrange the order of sampling when running in a sequenced channel operation, enable averaging of samples to reduce noise, set alarms for user defined voltage and temperature tolerance violations for on-chip sensors, etc… The image below shows the block diagram of the XADC as found in the datasheet for the device as provided by Xilinx. You can download the datasheets for the XADC by clinking on the button below.



On HELIX FPGA board temperature sensor is connected with AD3_P/AD3_N channel, LDR(light dependent resistor) is connected with AD11_P/AD11_N channel and variable resistor (POT) is connected with VP_P/VP_N channel of artix7 FPGA is shown in following fig.



PMOD Ports

We have a large collection of PMOD (Peripheral Module) accessory boards that can attach to the expansion ports to add ready-made functions such as A/D's, D/A's, motor drivers, sensors, displays, and many other functions. These ports can be used as simple expansion ports, since all of the pin-outs correspond to pins on the FPGA.

The PMOD ports are arranged in a 2×5 right-angle, and are 100-mil female connectors that mate with standard 2×10 pin headers. Each 10-pin PMOD ports provides 3.3V VCC signals (pins 9), Ground signals (pins 10), and eight logic signals. Pin assignments for the PMOD I/O connected to the FPGA are shown in the below table.

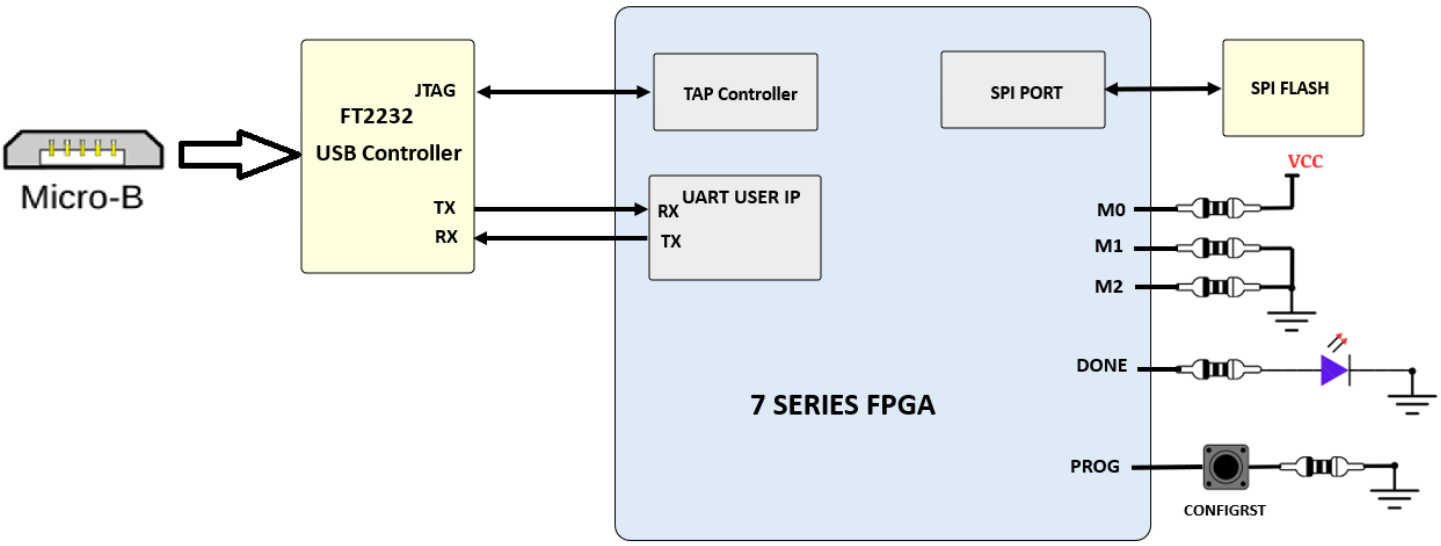
Warning: ***Since the PMOD pins are connected to Artix-7FPGA pins using a 3.3V logic standard, care should be taken not to drive these pins over 3.4V.***

PMOD JA	PMOD JB	PMOD JC	PMOD JD
JA_1: E2	JB_1: B3	JC_1: B1	JD_1: C3
JA_2: D1	JB_2: A4	JC_2: C4	JD_2: C2
JA_3: C1	JB_3: A6	JC_3: C6	JD_3: D4
JA_4: B1	JB_4: B7	JC_4: E6	JD_4: C4
JA_5: A2	JB_5: B2	JC_5: A1	JD_5: B4
JA_6: B14	JB_6: A3	JC_6: B4	JD_6: A3
JA_7: C14	JB_7: A5	JC_7: C5	JD_7: B6
JA_8: F14	JB_8: B6	JC_8: E5	JD_8: B5

FPGA Configuration

After power-on, the FPGA must be configured (or programmed) before it can perform any functions. You can configure the FPGA in one of the following ways:

1. A PC can use the USB-JTAG circuitry to program the FPGA any time the power is on.
2. A file stored in the non-volatile serial (SPI) flash device can be transferred to the FPGA using the SPI port.

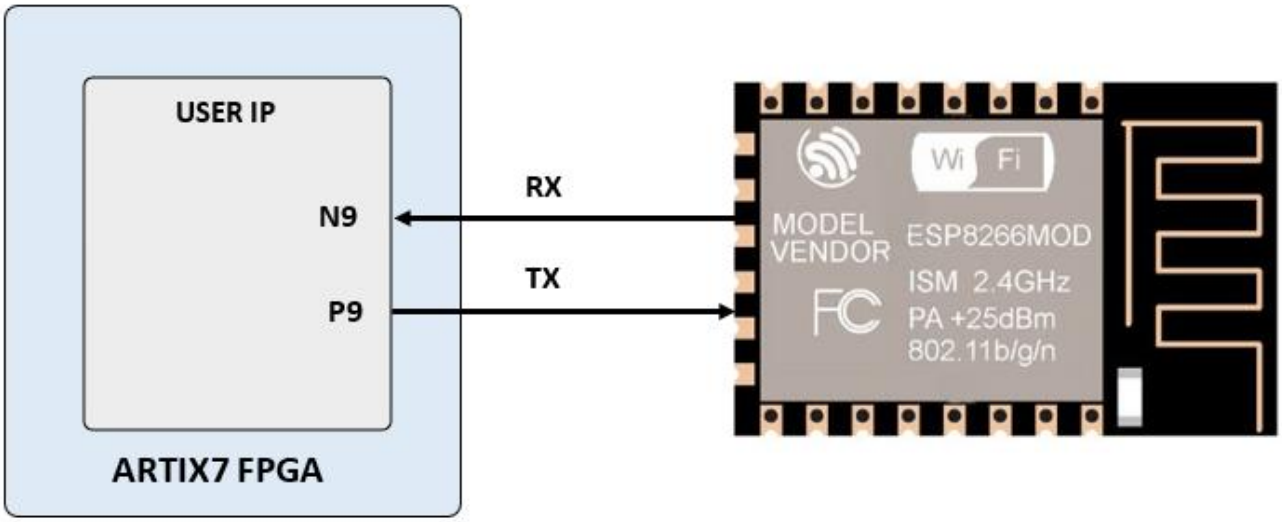


Above fig shows the different options available for configuring the FPGA. By default, on power on FPGA will be programmed by the Quad-SPI flash if it's programed with correct .bin file.

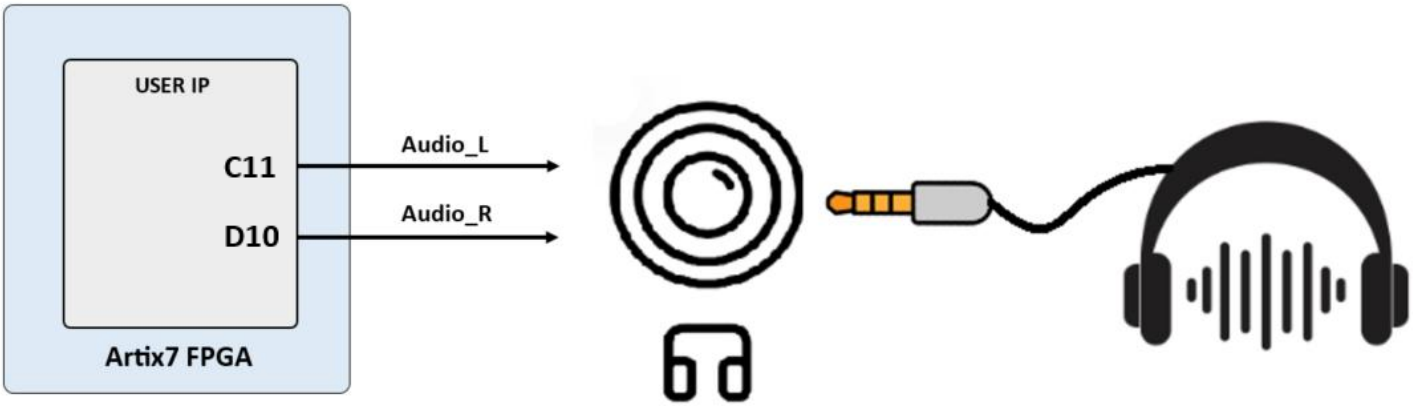
Bitstreams are stored in volatile memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

After being successfully programmed, the FPGA will cause the "DONE" LED to illuminate. Pressing the "PROG" button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from SPI flash, as we have fixed master spi mode.

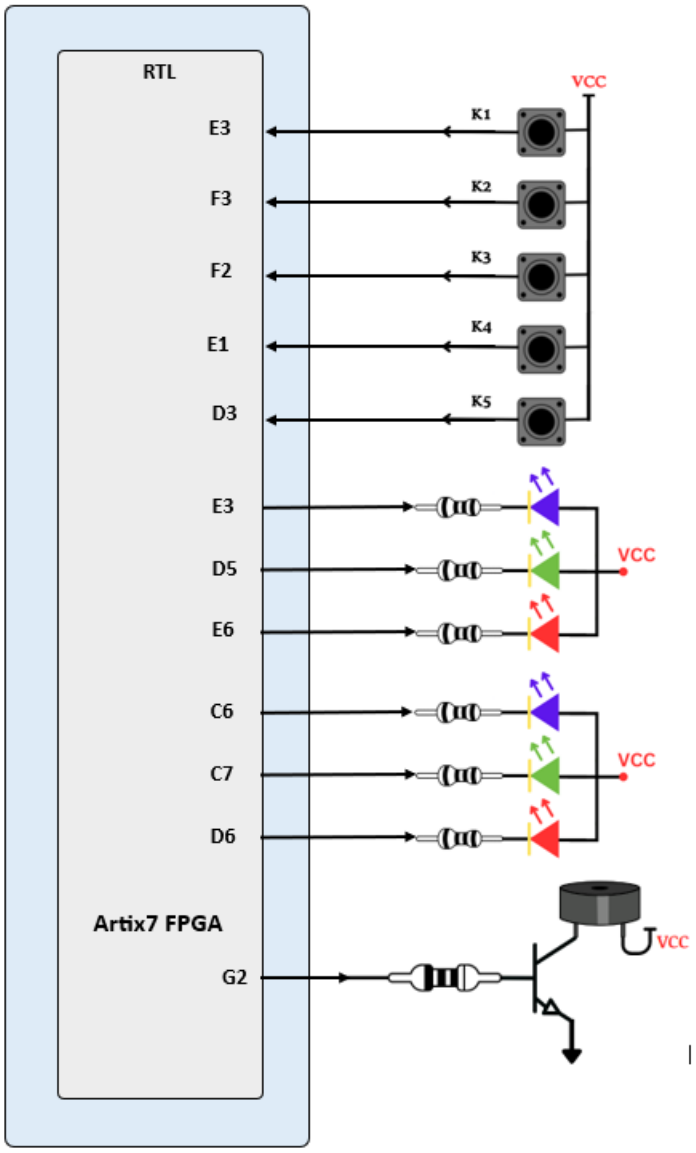
WIFI interface



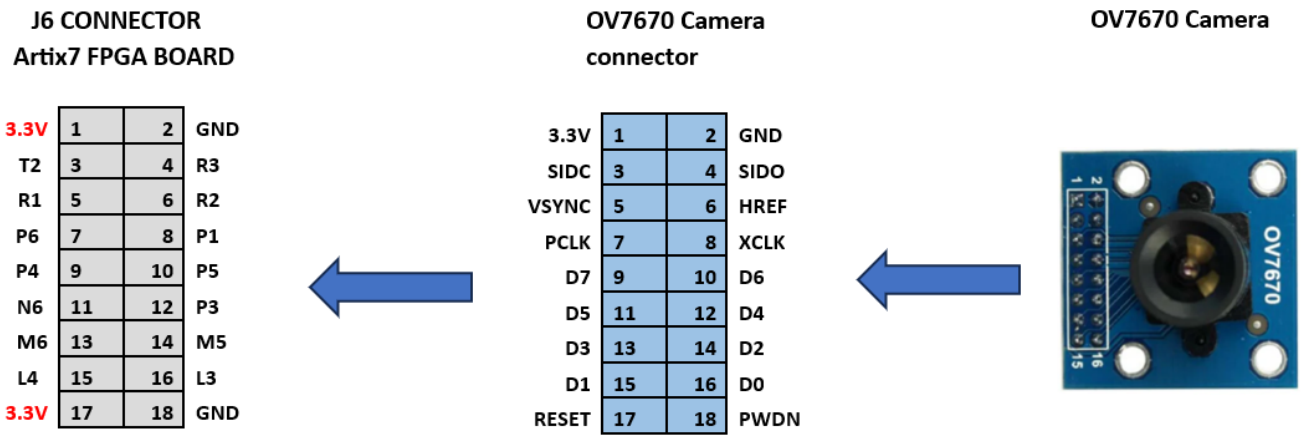
Audio interface



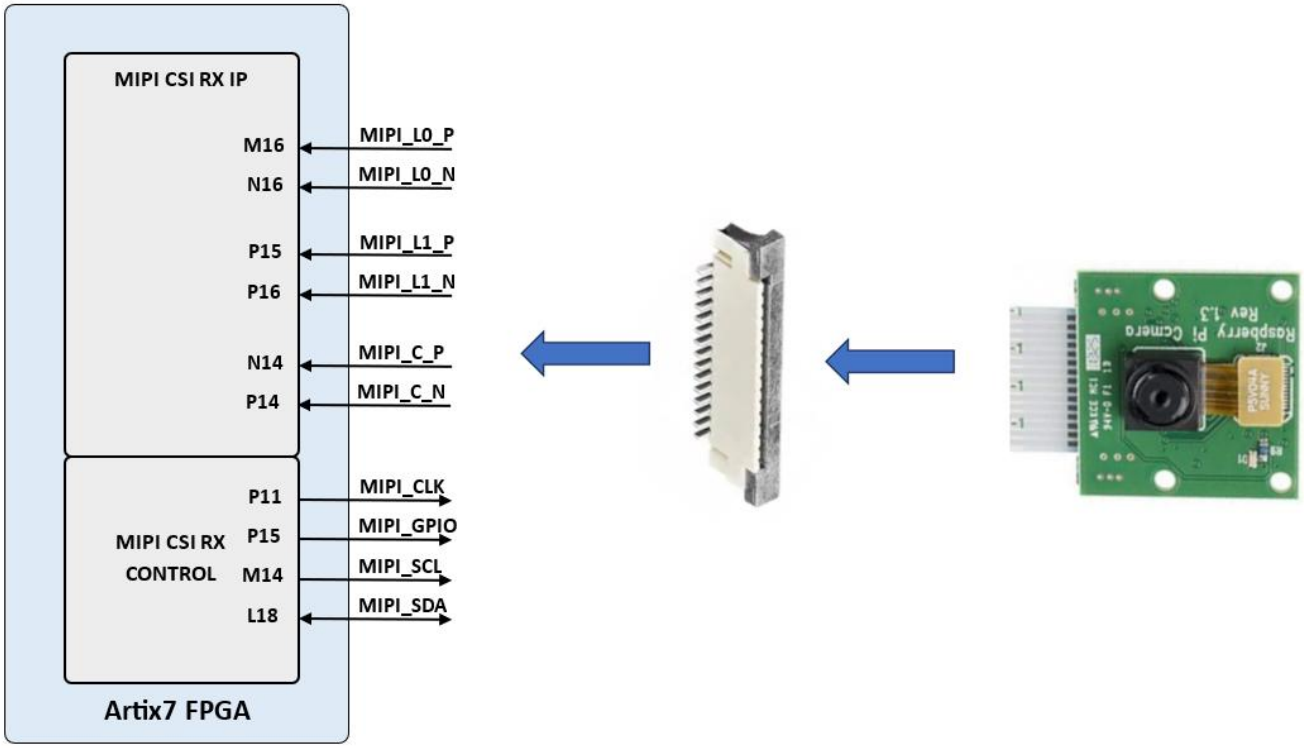
Push Button, Buzzer & RGB LED



OV7670 Camera interface



Raspberry pi MIPI-CSI camera




Raspberry Pi Camera
Rev 1.3

Install a camera module

To install a camera module, connect its flex ribbon cable into the camera connector. Follow these steps:

1. Gently lift up the connector latch. See Figure 3.
2. Insert the camera ribbon cable. Ensure that the connectors at the bottom of the ribbon cable are facing the contacts in the connector. See Figure 4.
3. Gently push the connector latch back into place. This may require two fingers, each at one end of the latch. Do not use excessive force.

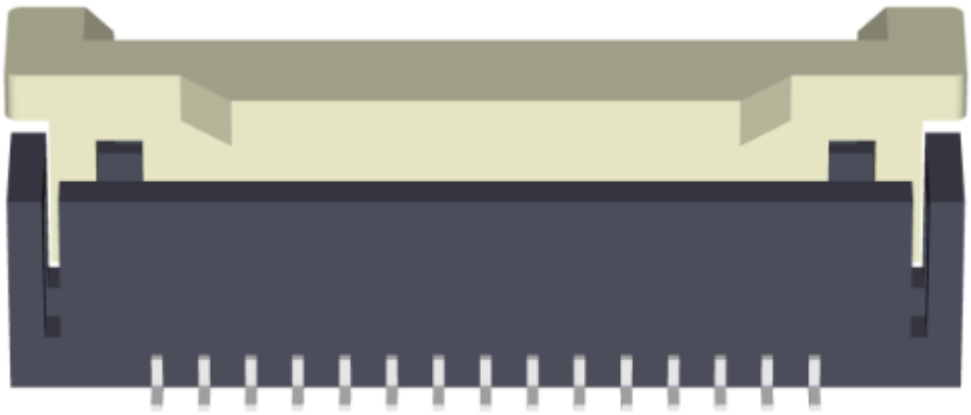


Figure 3. Gently lift the connector latch

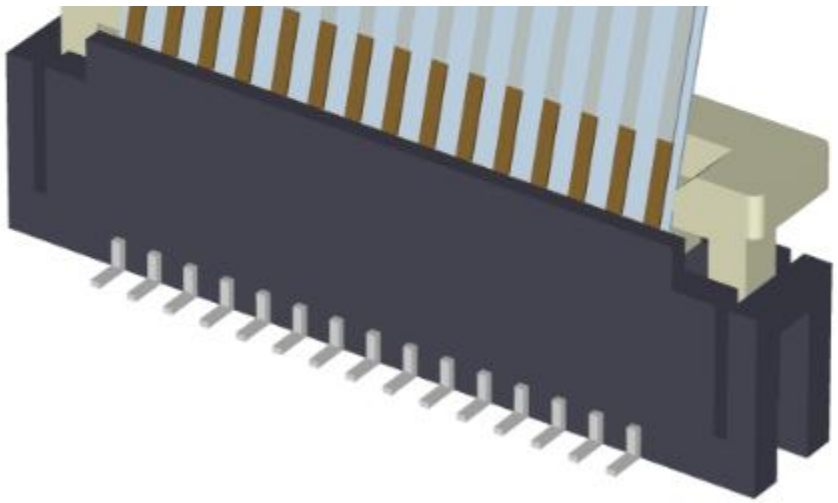


Figure 4. Installing a camera module to the CSI connector