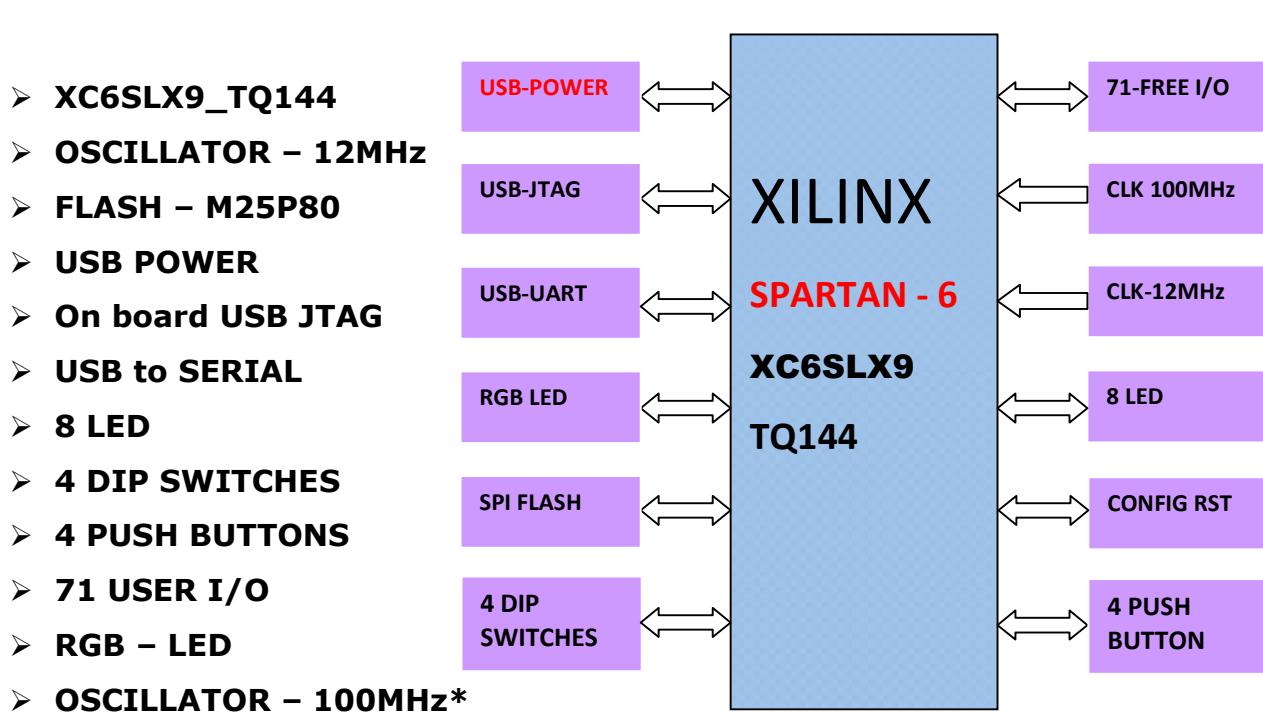


# Critical Design document for Spartan6 mini

## 1) Introduction of Spartan6 mini



Above block diagram shows all available blocks available in spartan6 mini board, Spartan6 mini board has advance Spartan6 FPGA (XC6SLX9-2tqg144), with onboard USB JTAG & USB to UART which support Xilinx IMPACT for programing

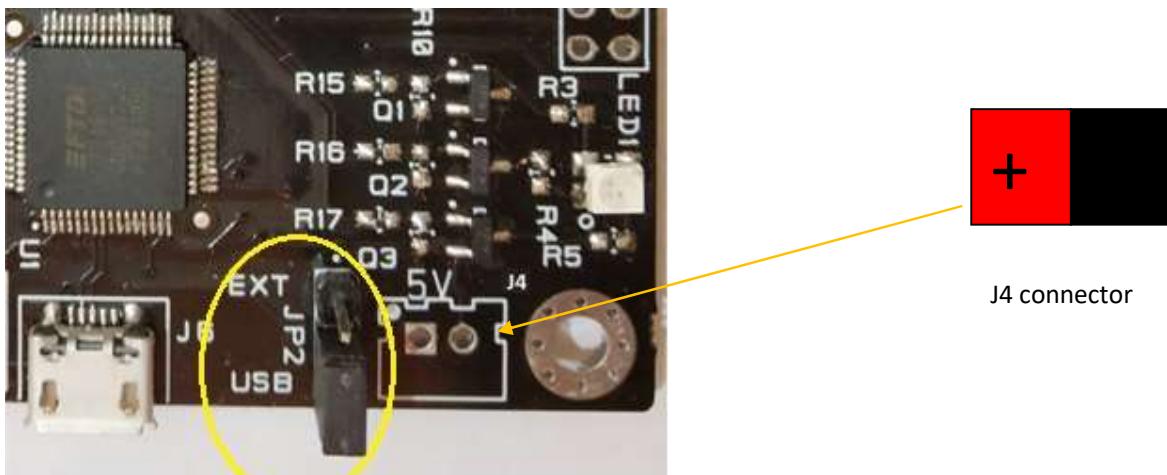
## 2) Description & Technical Specification

**Mini\_sp6** is low cost & easy to use FPGA Development board with Xilinx Spartan-6 FPGA.

**Mini\_sp6** is specially designed for experimenting and learning system design with FPGAs.

This development board designed with Xilinx XC6SLX9 TQG144 FPGA with maximum 71 user IOs. The USB 2.0 interface provides fast and easy configuration download to FPGA and on-board SPI flash.

The **MINI-SP6-FPGA** board can work on USB power; you can also connect external 5VDC supply. When **JP2** jumper is placed towards **USB** as shown in below image power is used from USB connector & when **JP2** jumper is placed towards **EXT** power is used from J4 connector (J4 is optional)



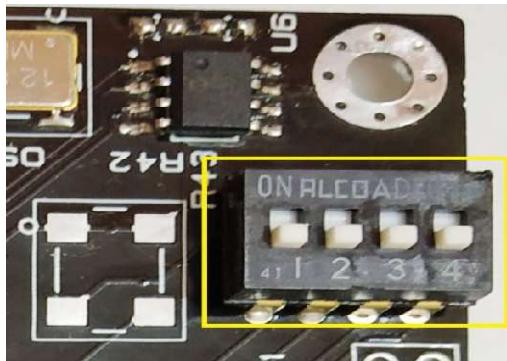
**Note: Max power input (J4 connector) 5V to 5.2V**

**Max input Voltage on all IO is 3V to 3.4V**

## DIP Switches Interface

The **MINI-SP6-FPGA** board has 4 push buttons & 4 DIP switch. Switches are used to provide digital input (i.e. logic 0 and logic 1).

### Pin Assignment (UCF Location):



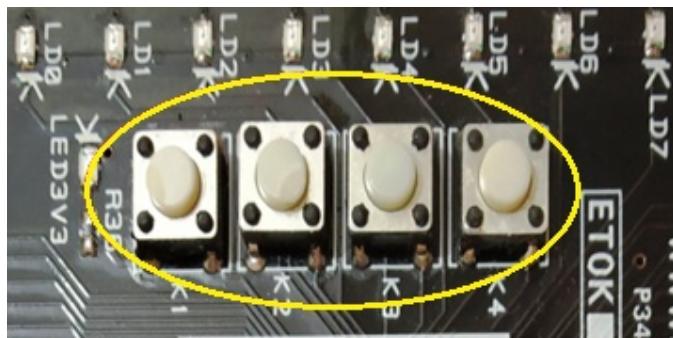
Slide Switch	XC6SLX9	Active
DIP_SW_1	P80	HIGH
DIP_SW_2	P81	HIGH
DIP_SW_3	P82	HIGH
DIP_SW_4	P83	HIGH

```
NET DIP_SW_1 LOC = P80 | IOSTANDARD = LVCMOS33;  
NET DIP_SW_2 LOC = P81 | IOSTANDARD = LVCMOS33;  
NET DIP_SW_3 LOC = P82 | IOSTANDARD = LVCMOS33;  
NET DIP_SW_4 LOC = P83 | IOSTANDARD = LVCMOS33;
```

## PUSH Button Interface

The **MINI-SP6-FPGA** board has 4 push buttons & 4 DIP switch. Switches are used to provide digital input (i.e. logic 0 and logic 1).

### Pin Assignment (UCF Location):



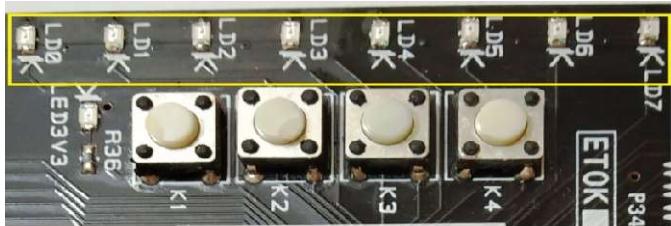
Slide Switch	XC6SLX9	Active
SW1	P17	HIGH
SW2	P14	HIGH
SW3	P10	HIGH
SW4	P7	HIGH

```
NET PUSH_BTN_1 LOC = P17 | IOSTANDARD = LVCMOS33;  
NET PUSH_BTN_2 LOC = P14 | IOSTANDARD = LVCMOS33;  
NET PUSH_BTN_3 LOC = P10 | IOSTANDARD = LVCMOS33;  
NET PUSH_BTN_4 LOC = P7 | IOSTANDARD = LVCMOS33;
```

## LED's Interface

The **MINI-SP6-FPGA** board has 8 individual LED, A LED is assigned to each I/O to indicate its data status when I/O is configured as output. DIP switch is used to provide digital input (i.e. logic 0 and logic 1).

### Pin Assignment (UCF Location):



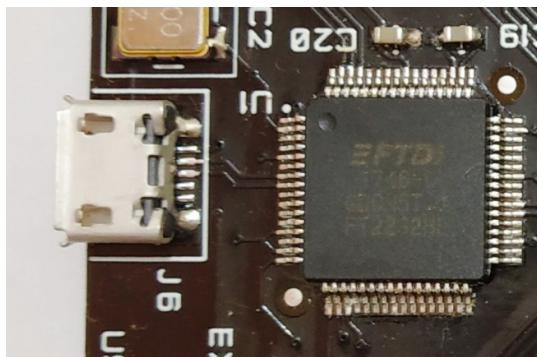
LED	XC6SLX9	Active
TL0	P16	HIGH
TL1	P15	HIGH
TL2	P12	HIGH
TL3	P11	HIGH
TL4	P9	HIGH
TL5	P8	HIGH
TL6	P6	HIGH
TL7	P5	HIGH

```
NET TL<0> loc=p16 | IOSTANDARD = LVCMOS33;  
NET TL<1> loc=p15 | IOSTANDARD = LVCMOS33;  
NET TL<2> loc=p12 | IOSTANDARD = LVCMOS33;  
NET TL<3> loc=p11 | IOSTANDARD = LVCMOS33;  
NET TL<4> loc=p9 | IOSTANDARD = LVCMOS33;  
NET TL<5> loc=p8 | IOSTANDARD = LVCMOS33;  
NET TL<6> loc=p6 | IOSTANDARD = LVCMOS33;  
NET TL<7> loc=p5 | IOSTANDARD = LVCMOS33;
```

## USB Interface

The **MINI-SP6-FPGA** board have USB interface using device FT2232HL from FTDI. This act as USB to UART converter so that Communication with FPGA can accomplished by USB port.

### Pin Assignment (UCF Location):



<b>Signal Name</b>	<b>XC6SLX9</b>
<b>USB_Rx</b>	<b>P88</b>
<b>USB_Tx</b>	<b>P85</b>

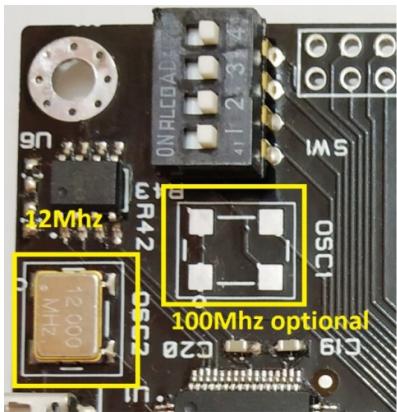
```
NET USB_UART_RX LOC = P88 | IOSTANDARD = LVCMOS33;  
NET USB_UART_TX LOC = P85 | IOSTANDARD = LVCMOS33;
```

## Clock Sources

The **MINI-SP6-FPGA** supports clock input sources which are listed below.

*The board includes an on-board 12 MHz clock oscillator & 100 MHz clock oscillator (optional)*

### Pin Assignment (UCF Location):



Signal Name	XC6SLX9
Clock 12Mhz	P87
Clock 100Mhz	P84

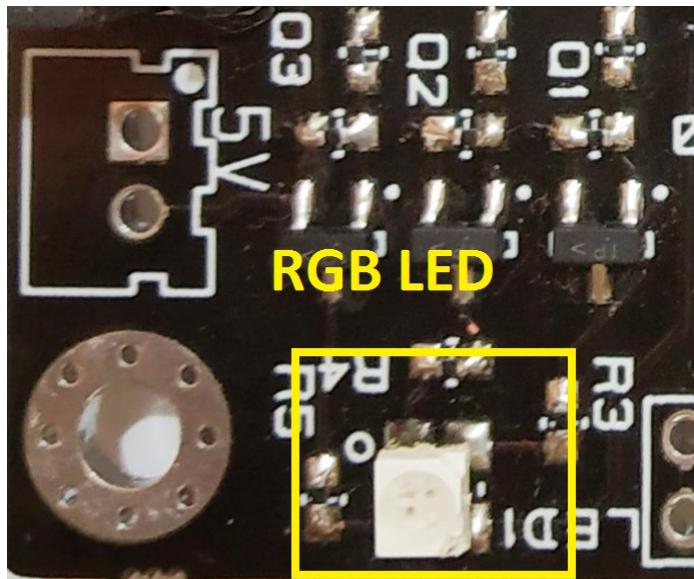
**NET CLOCK\_12MHZ LOC = P87 | IOSTANDARD = LVCMOS33;**

**NET CLOCK\_100MHZ LOC = P84 | IOSTANDARD = LVCMOS33;**

## **RGB-LED**

The **MINI-SP6-FPGA** has a **RGB LED**

**Pin Assignment (UCF Location):**



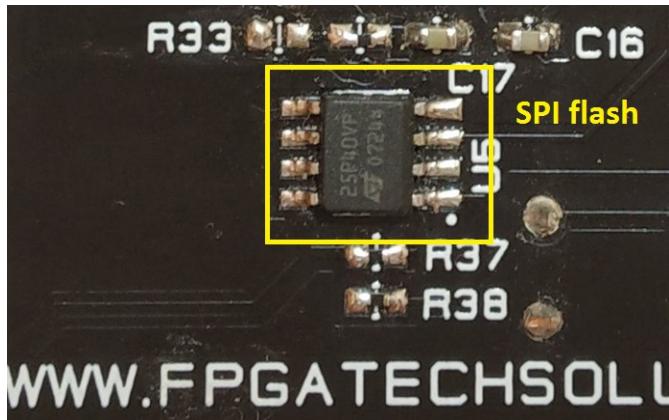
Signal Name	XC6SLX9
R	P93
G	P94
B	P95

```
NET LED_RED LOC = p95 | IOSTANDARD = LVCMOS33;  
NET LED_GREEN LOC = p94 | IOSTANDARD = LVCMOS33;  
NET LED_BLUE LOC = p93 | IOSTANDARD = LVCMOS33;
```

## Flash interface

The **MINI-SP6-FPGA** has a **SPI flash** interfaced with **FPGA**

**Pin Assignment (UCF Location):**



<b>Slide Switch</b>	<b>XC6SLX9</b>
<b>FLASH_CS</b>	<b>P38</b>
<b>MOSI</b>	<b>P64</b>
<b>MISO</b>	<b>P65</b>
<b>SPI_CLK</b>	<b>P70</b>

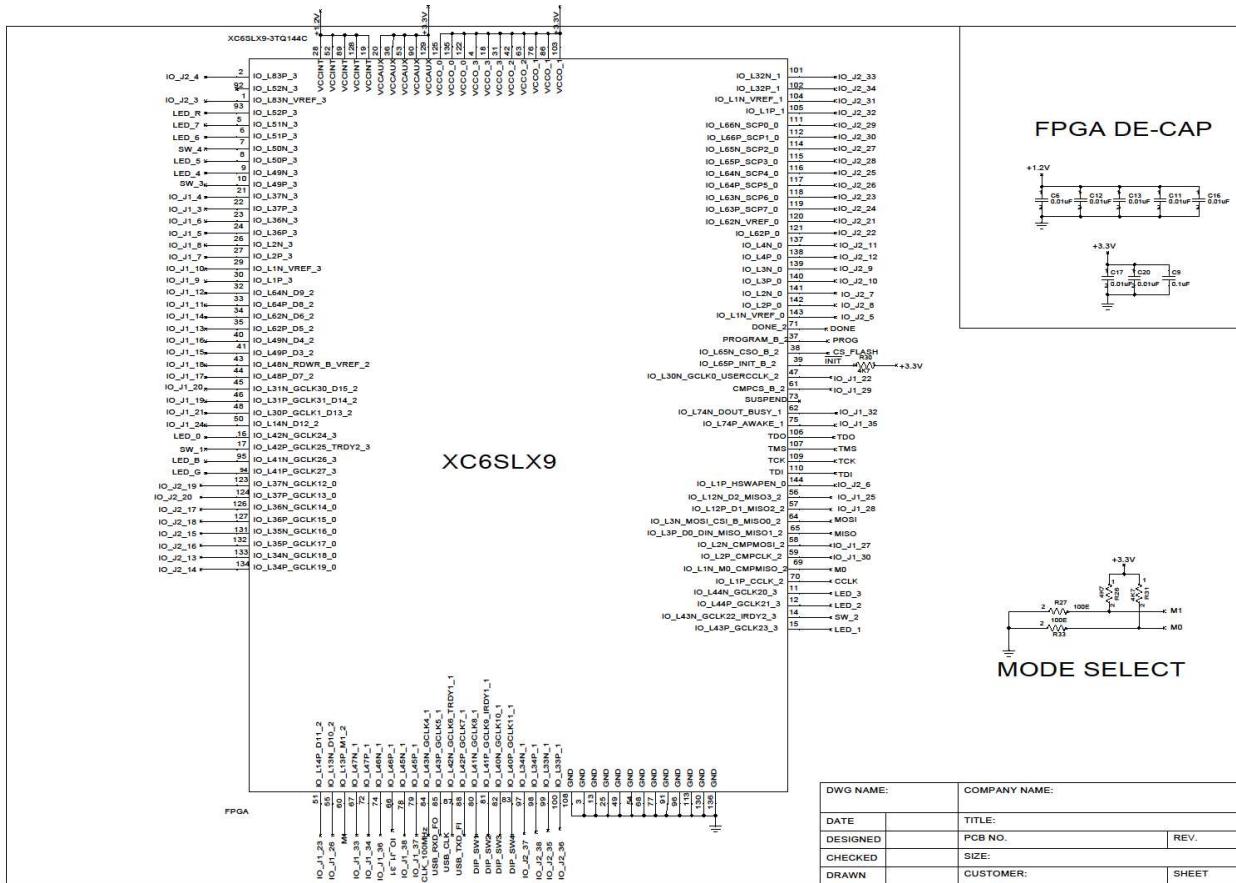
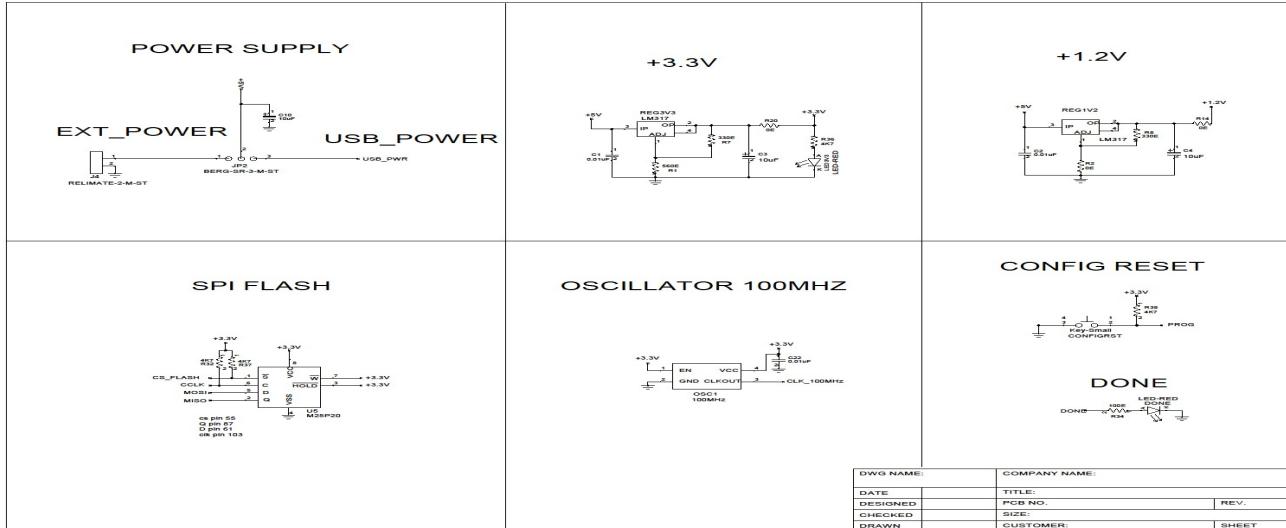
**NET FLASH\_CS LOC = P38 | IOSTANDARD = LVCMOS33;**

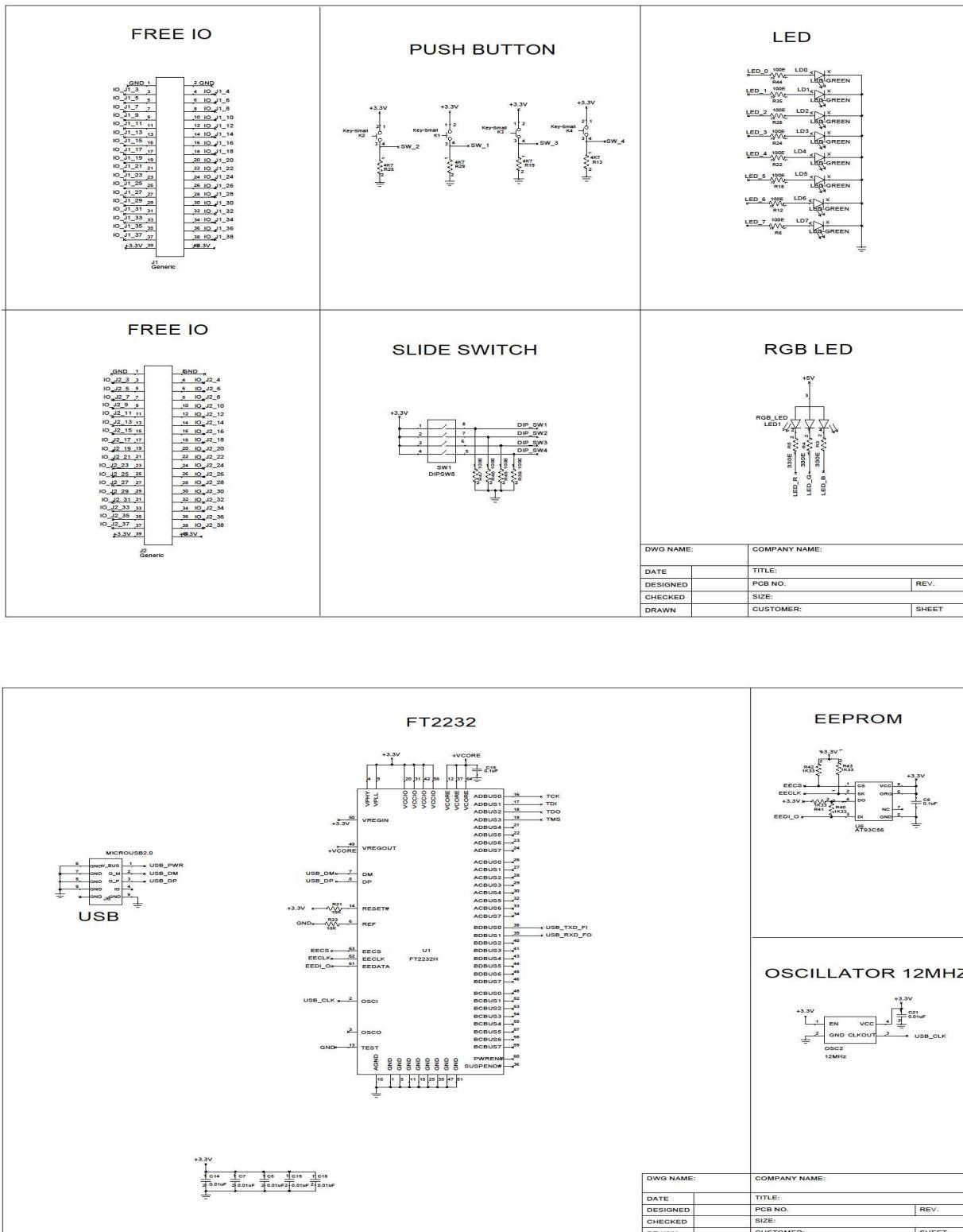
**NET FLASH\_MOSI LOC = P64 | IOSTANDARD = LVCMOS33;**

**NET FLASH\_MISO LOC = P65 | IOSTANDARD = LVCMOS33;**

**NET FLASH\_CLK LOC = P70 | IOSTANDARD = LVCMOS33;**

### **3) Schematic**

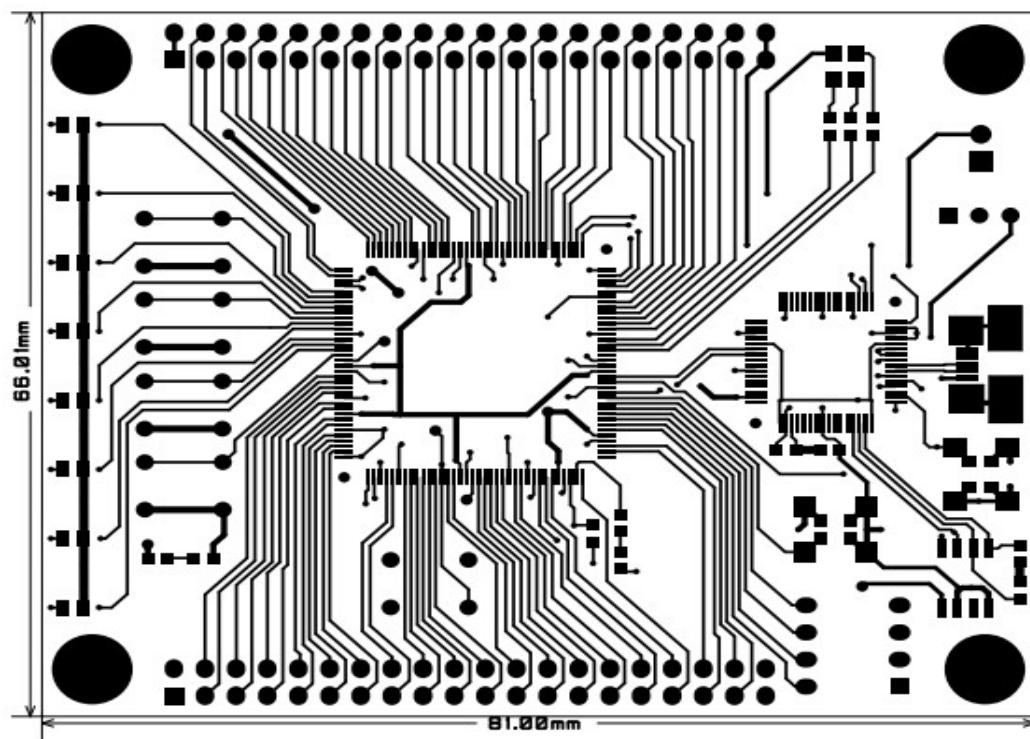
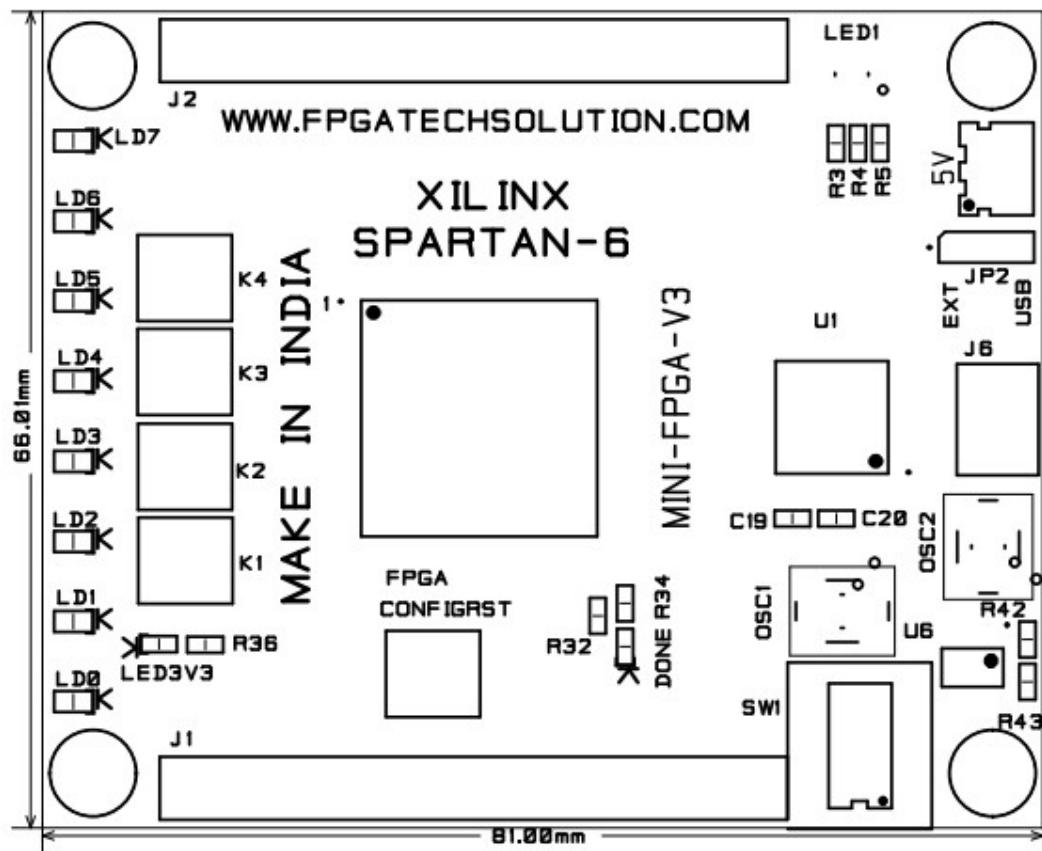


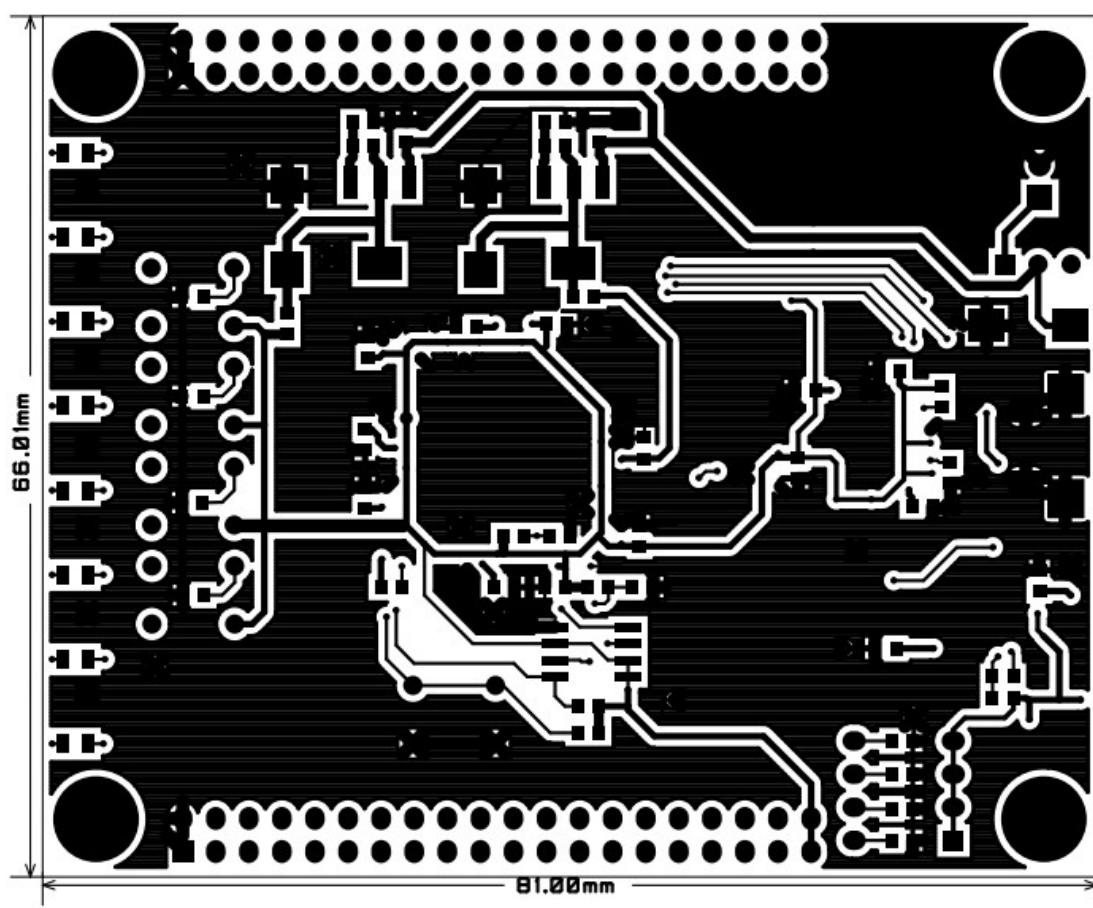
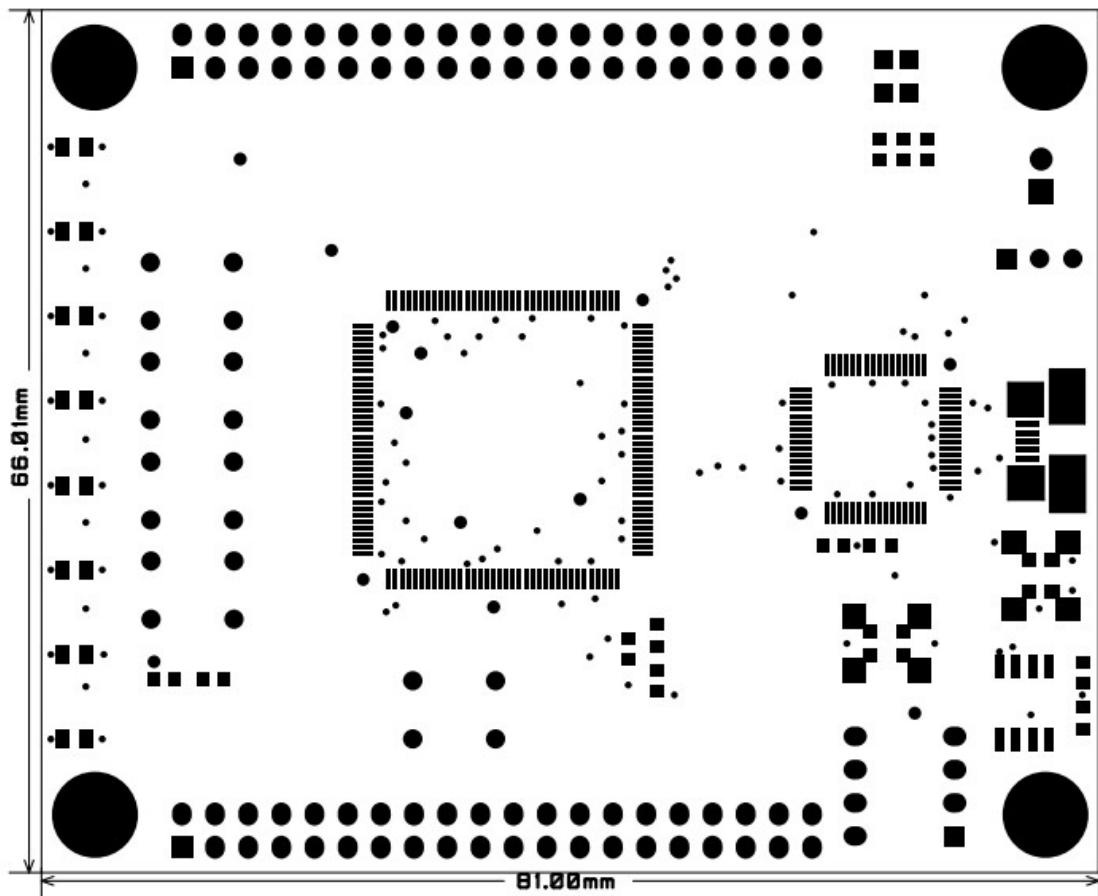


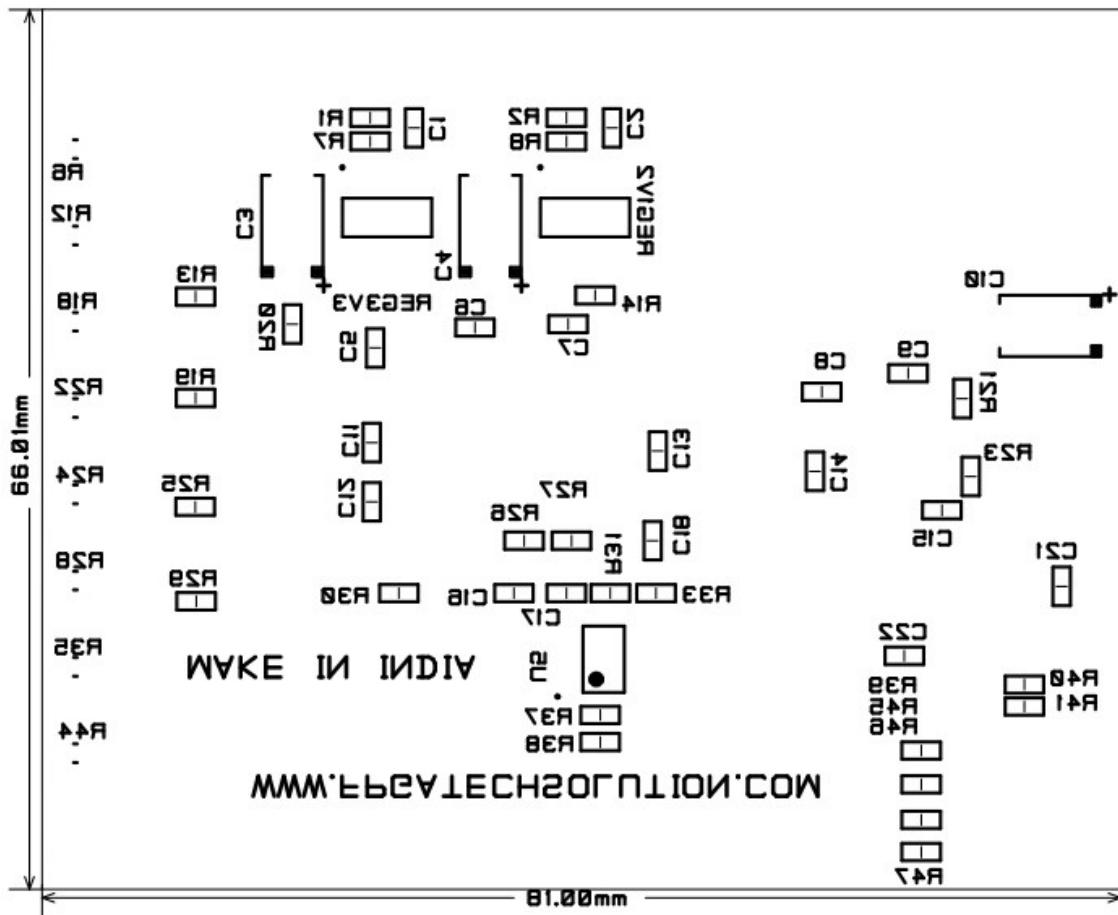
## 4) BOM

PCB NAME:- MINI SP6					
Sr.	Description	Part No	PACKAGE	Ident No.	Qty
1	M25P16-VMN8T (NUMONYX)	M25P16-VMW8G	S08	U5	1 NO
2	LM317sot223	LM317MSTT3G	SOT223	REG1V2,REG3V3	2 NO
3	FT2232H	FT2232HL	LQFP64	U1	1 NO
4	XC8SLX9-2TQFP144C	XC8SLX9-2TQG144C	PQG208	FPGA	1 NO
5	AT83C56B	B3LC56B-VSN	S08	U6	1 NO
6	oscilator 12 MHZ (7MM BY 5MM)	MCSJK-3N-12.00-3.3-50-B	SMD	OSC2	1 NO
7	oscilator 100 MHZ (7MM BY 5MM)	MCSJK-3N-100.00-3.3-50-B	SMD	OSC1	1 NO
8	100uf/6vCASED(7.30mm L X 4.30mm W X 3.10mm H)	TAJD107K016RNJ	SMD CAP	C3,C4,C10	3 NO
9	RGBLED	LM1-TPP1-01		LED1	1 NO
10	DIPSW8	MCNDS-04V	TH. HOLE	SW1	1 NO
11	MICROUSB2	10103594-0001LF		J8	1 NO
12	2 pin rellimate	B2B-XH-A (LF)(SN)	TH. HOLE	J4	2 NO
13	SWITCH 4PIN	1825910-6	TH. HOLE	CONFIGRESET,J1,J2,J3,J4	5 NO
14	BERGE STRIP MALE (2.54MM)3 PIN(STRAIGHT)	83-15402	PITCH-2.54 MM	JP2	1 NO
15	LED SMD RED	KPT-1608EC	SMD-0603	DONE,DED3V3	3 NO
16	LED SMD BLUE	150060BS75000	SMD-0603	LD0 TO LD7	8 NO
17	0 OHM	RC0603FR-070RL	SMD-0603	R2,R14,R20	3 NO
18	10K	0603SAJ0103T5E	SMD-0603	R21,R23,R41,R42,R43	5 NO
19	2K	RC0603FR-072KL	SMD-0603	R40	1 NO
20	4.7 K OHM	WR06X472JTL	SMD-0603	R13,R19,R25,R26,R29,R30, R31,R32,R36,R37,R38 R27,R33,R34,R39,R45,	11 NO
21	100 OHM		SMD-0603	R46,R47	7 NO
22	330 OHM	RC0603FR-07330RL	SMD-0603	R3,R4,R5,R7,R8	5 NO
23	560 OHM	RC0603FR-07560RL	SMD-0603	R1,R6,R9,R10,R11,R12,R15, R16,R17,R18,R22,R24	15 NO
24	0.1UF	CC0603KRX7R9BB104	SMD-0603	C1,C2,C5,C6,C7,C8,C9,C11, C12,C13,C14,C15,C16,C17, C18,C19,C20,C21,C22	19 NO
25	BERGE STRIP MALE (2.54MM) 40X2	77313-802-40LF	TH. HOLE	J1,J2	2

## 5) Layout







## 6) Software Required

**For this spartan6 mini board we need Xilinx ISE 41.7,  
using this only we can program FPGA & FLASH**

### How to download & install ISE

Please click on following link

<https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive-ise.html>

you will see following

Solutions Products Support

 XILINX

## Version

2020.1

2019.2

2019.1

2018.3

Vivado Archive

**ISE Archive**

CAE Vendor Libraries

Archive

We strongly recommend using the latest releases available.

14x

14.7 Windows 10

14.7

### Multi-File Download: ISE Design - 14.7 Full Product Installation

#### **Last Updated October 2013**

As of October 2013, ISE has moved into the sustaining phase of its product life cycle, and there are no more planned ISE releases.

ISE supports the following devices families and their previous generations: Spartan-6, Virtex-6, and Coolrunner. For more information, visit the [ISE Design Suite](#)

Xilinx recommends [Vivado Design Suite](#) for new design starts with Virtex-7, Kintex-7, Artix-7, and Zynq-7000.

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MD5 SUM Value : e8065b2ffb411bb74ae32efa475f9817

 [Full Installer for Windows 7/XP/Server \(TAR/GZIP - 6.18 GB\)](#)

MD5 SUM Value : 94f40553a93dfbeca642503e2721b270

**Even you are using windows 10 download this file only this work properly**



←



## Welcome

We are glad you've chosen Xilinx as your platform development partner. This program will install ISE design environment, Software development kit or Lab tools.

You will need to have administrator privileges in order to install this software on Windows operating systems.

For the product you select to install, we recommend that you identify a directory that does not contain an older installation of the same product version.

**Note - To reduce installation time, we recommend that you disable any anti-virus software before continuing.**

### ISE 14.7 Installer

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- Select Installation Options
- Select Destination Directory
- Installation

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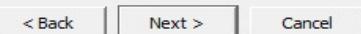
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The Xilinx Embedded Development Kit (EDK) is a suite of software and other technology that enables Licensee to design a complete embedded processor system for use in a Xilinx Device. EDK includes, among other components, (a) the Xilinx Platform Studio (XPS), which is the development environment, or GUI, used for designing the hardware portion of an embedded processor system; and (b) the Xilinx Software Development Kit (SDK), which is an integrated development environment, complementary to XPS, that is used to create and verify C/C++ embedded software applications. SDK is also made available separately from EDK.

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**Select Products to Install**

- Edition List
  - ISE WebPACK
  - ISE Design Suite Logic Edition
  - ISE Design Suite Embedded Edition
  - ISE Design Suite DSP Edition
  - ISE Design Suite System Edition
  - Lab Tools - Standalone Installation

Disk Space Required : 17480 MB

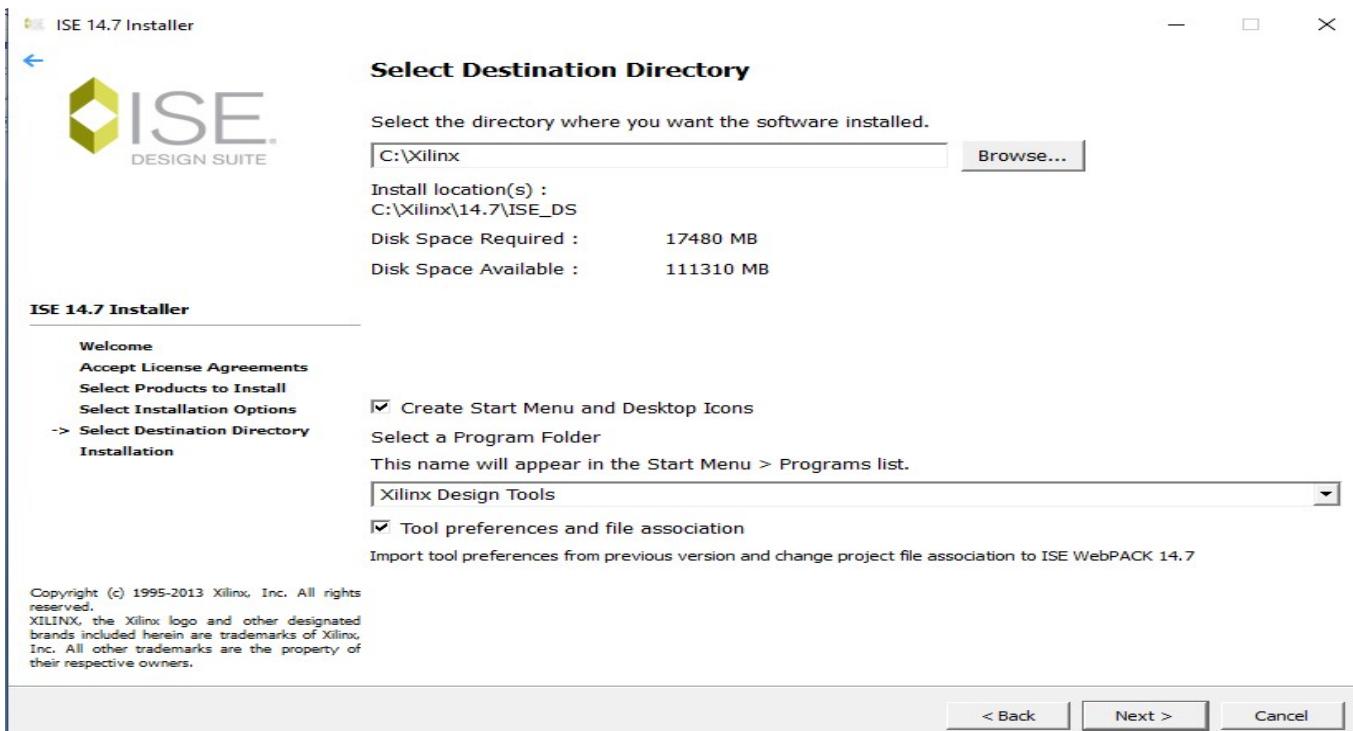
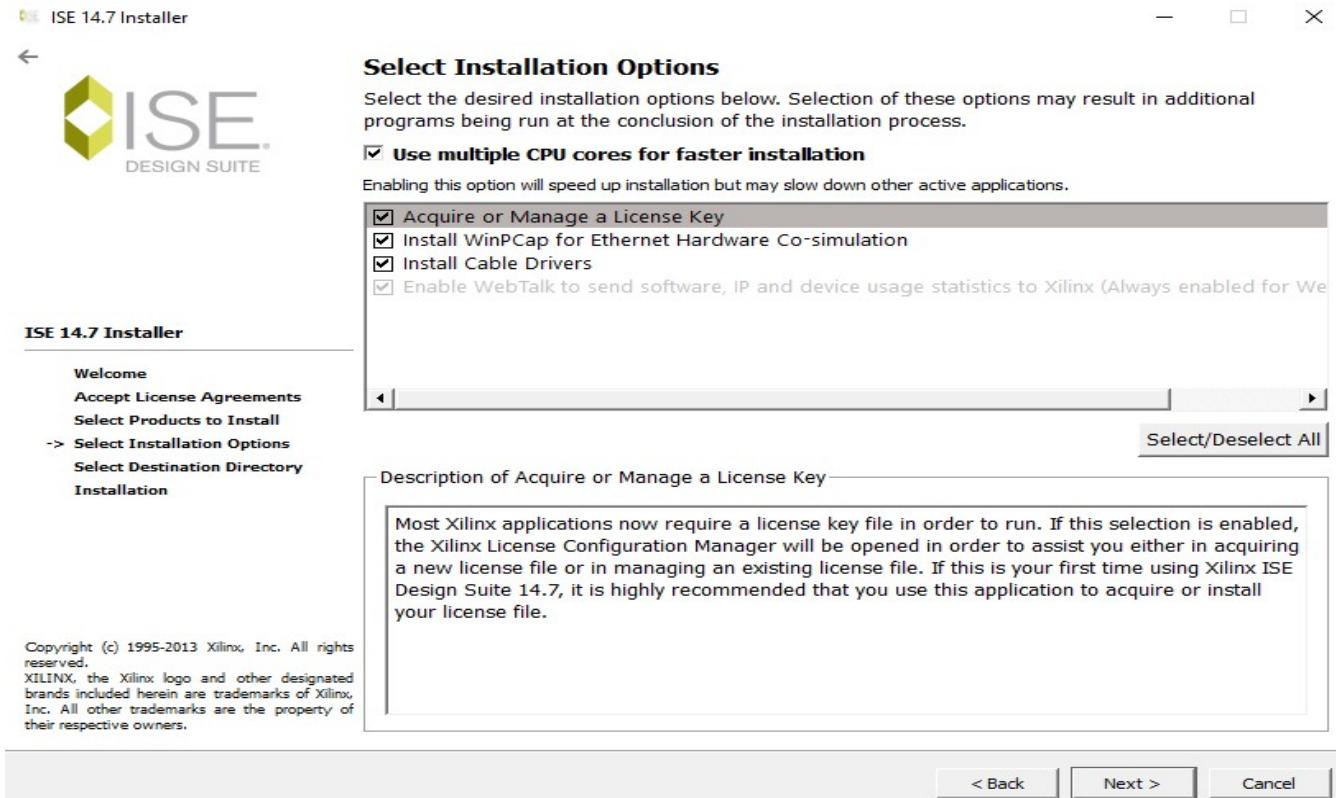
**Description of ISE WebPACK**

ISE WebPACK contains the most important tools you need for designing CPLDs and small to medium-sized FPGAs. Includes: ISE Design Tools (w/reduced device support), PlanAhead, Connectivity DSP IP, ChipScope Pro and The Embedded Development Kit will also be installed with WebPACK but are licensed separately (not included in a WebPACK license file).

&lt; Back

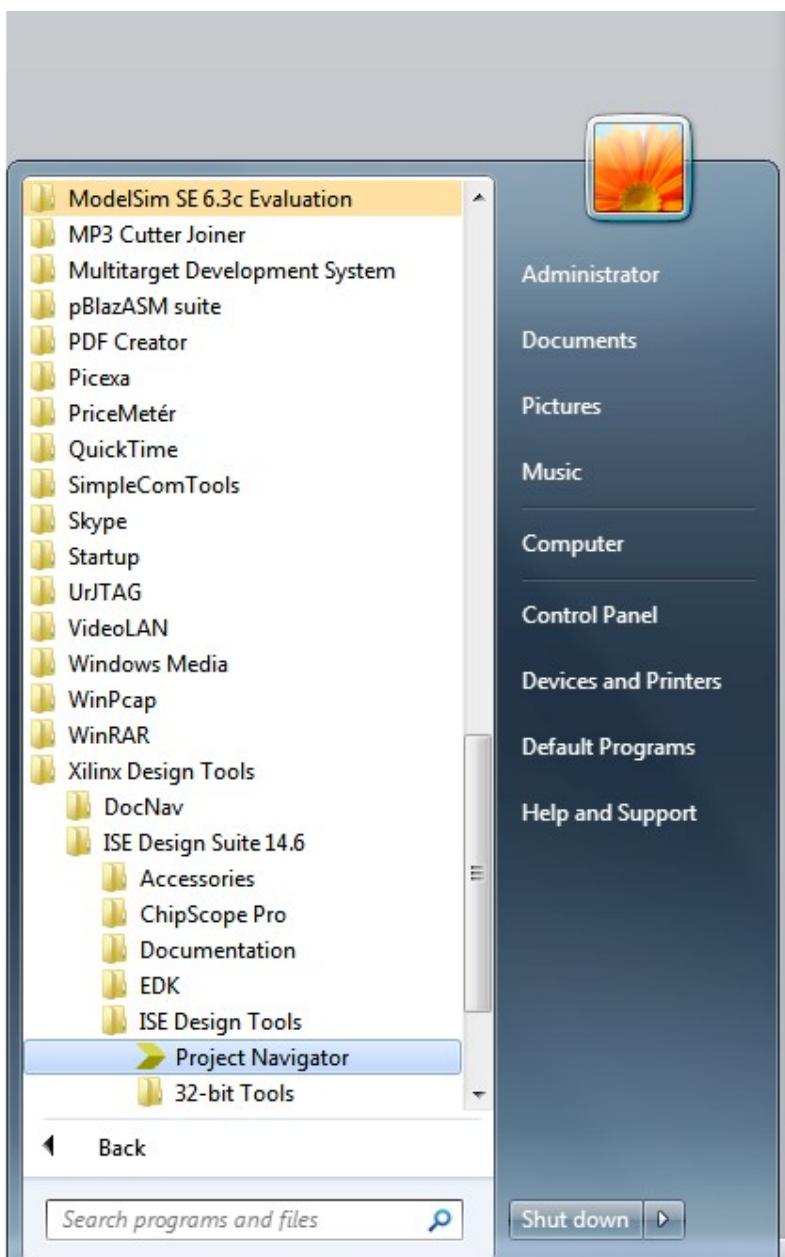
Next &gt;

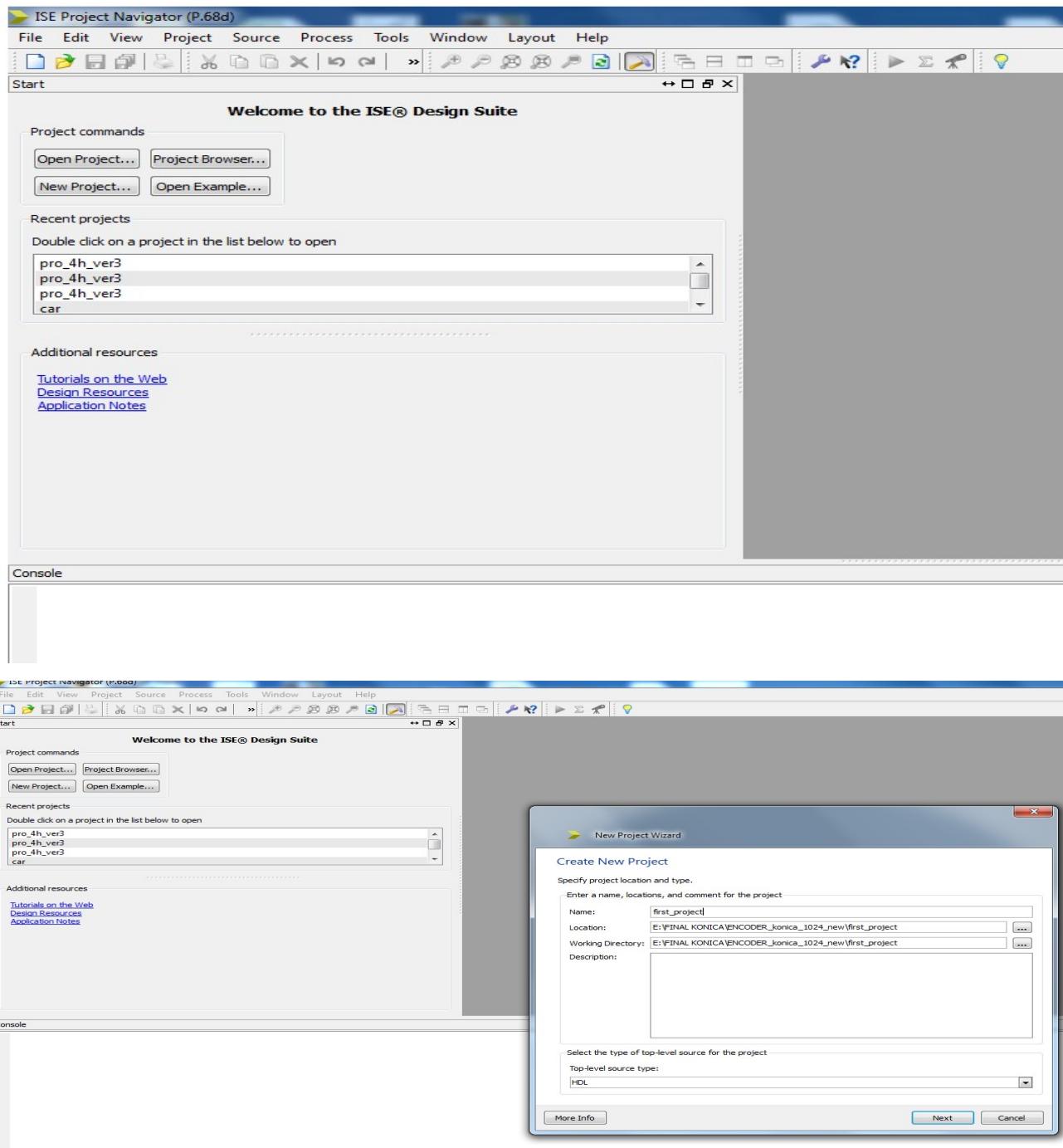
Cancel

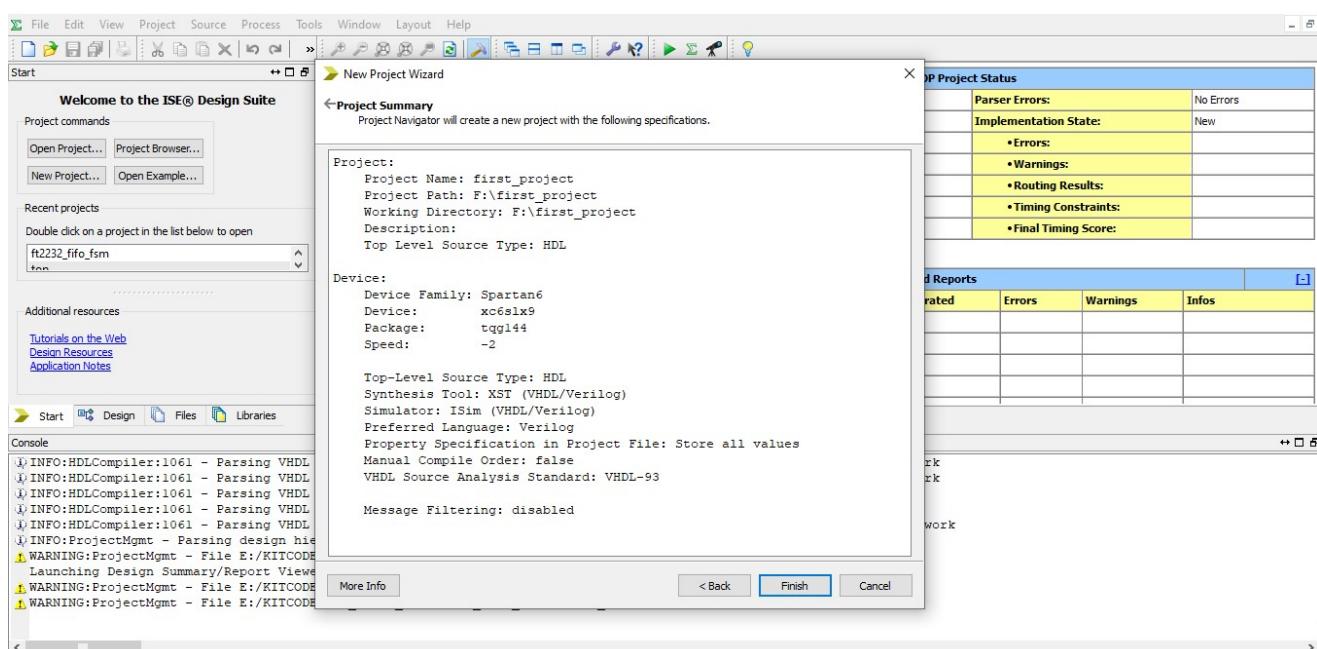
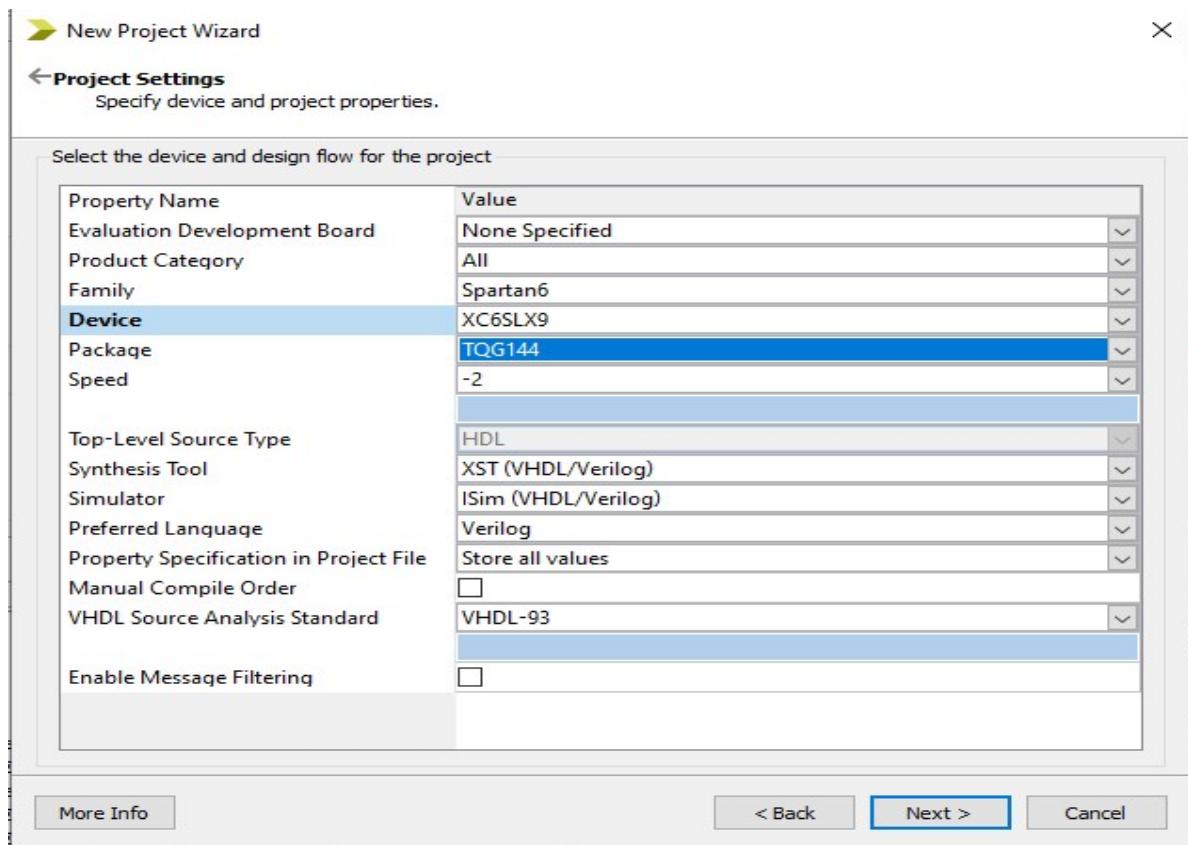


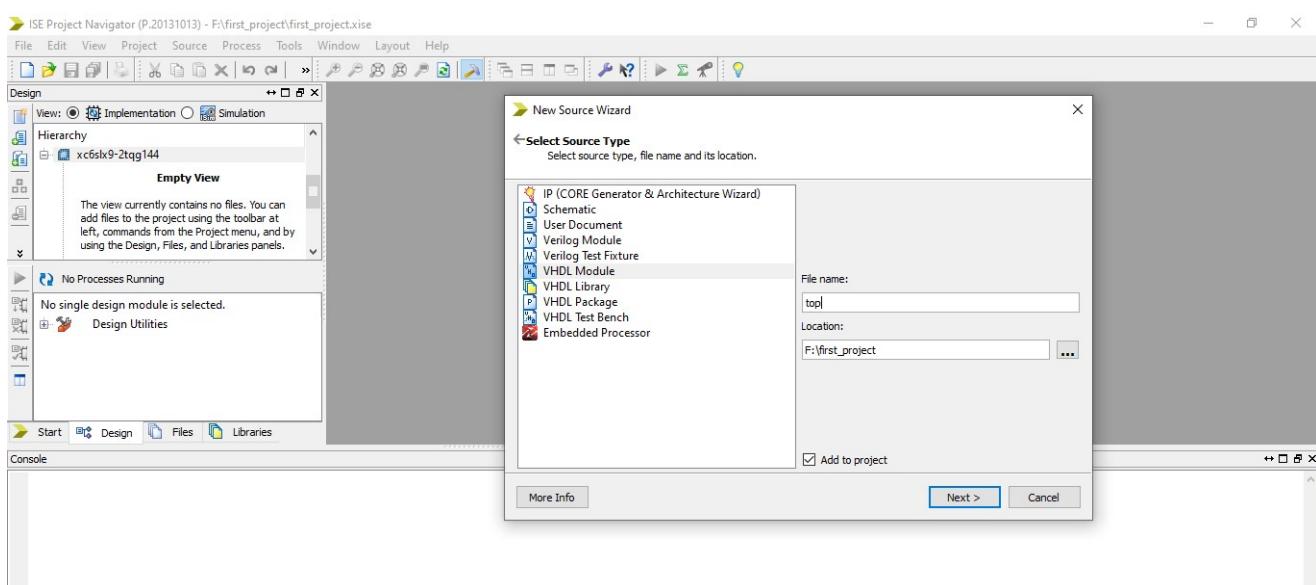
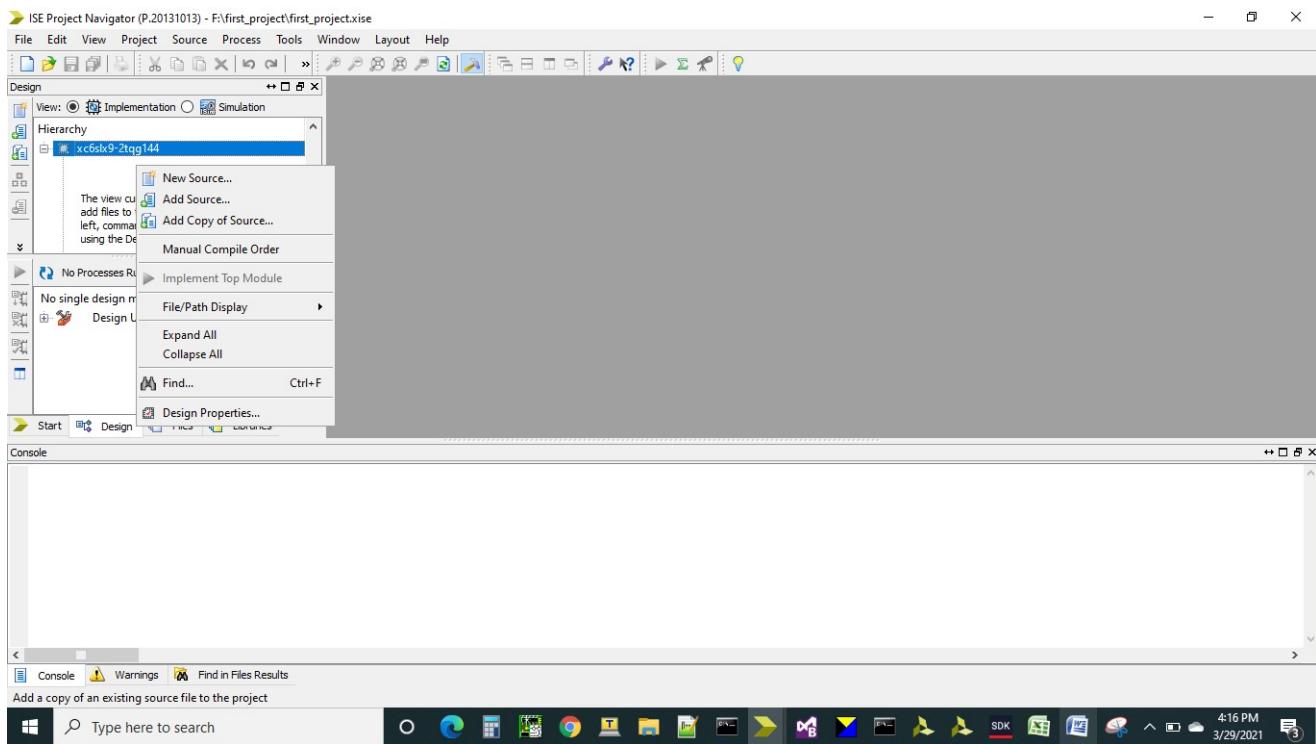
## 7) Getting Started

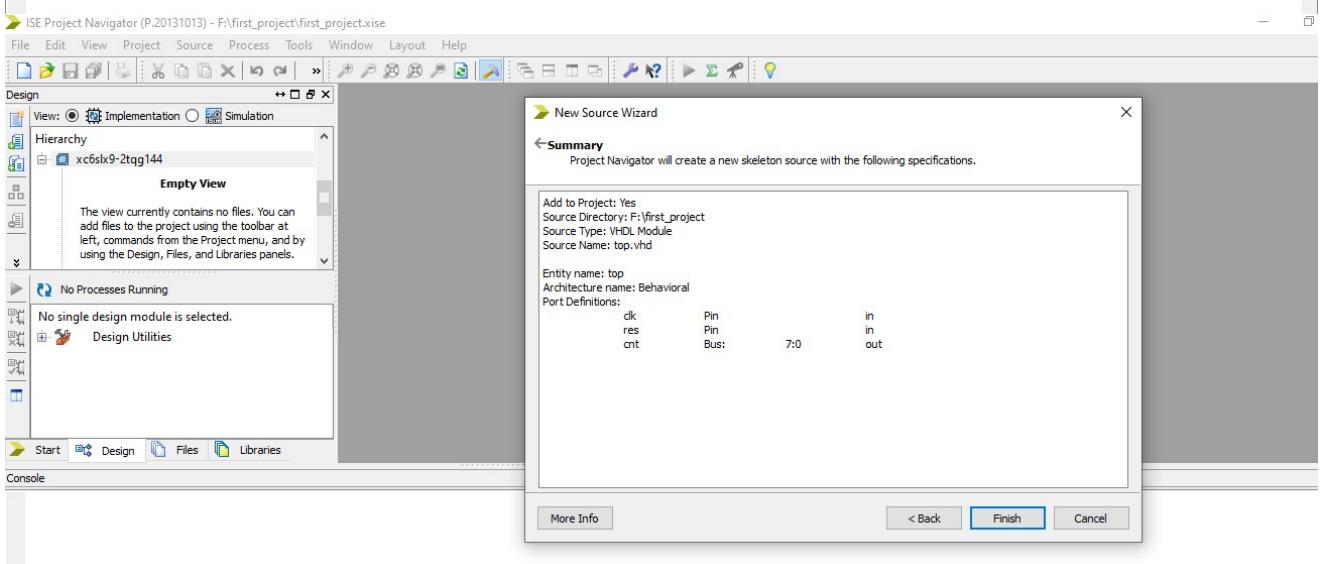
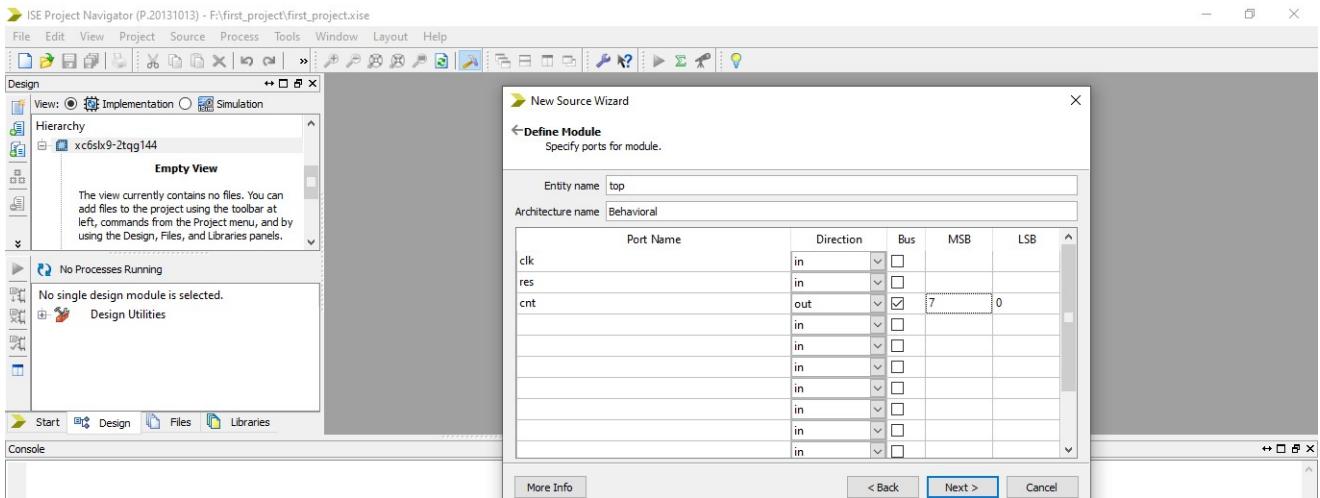
Please use following steps to create project in ISE







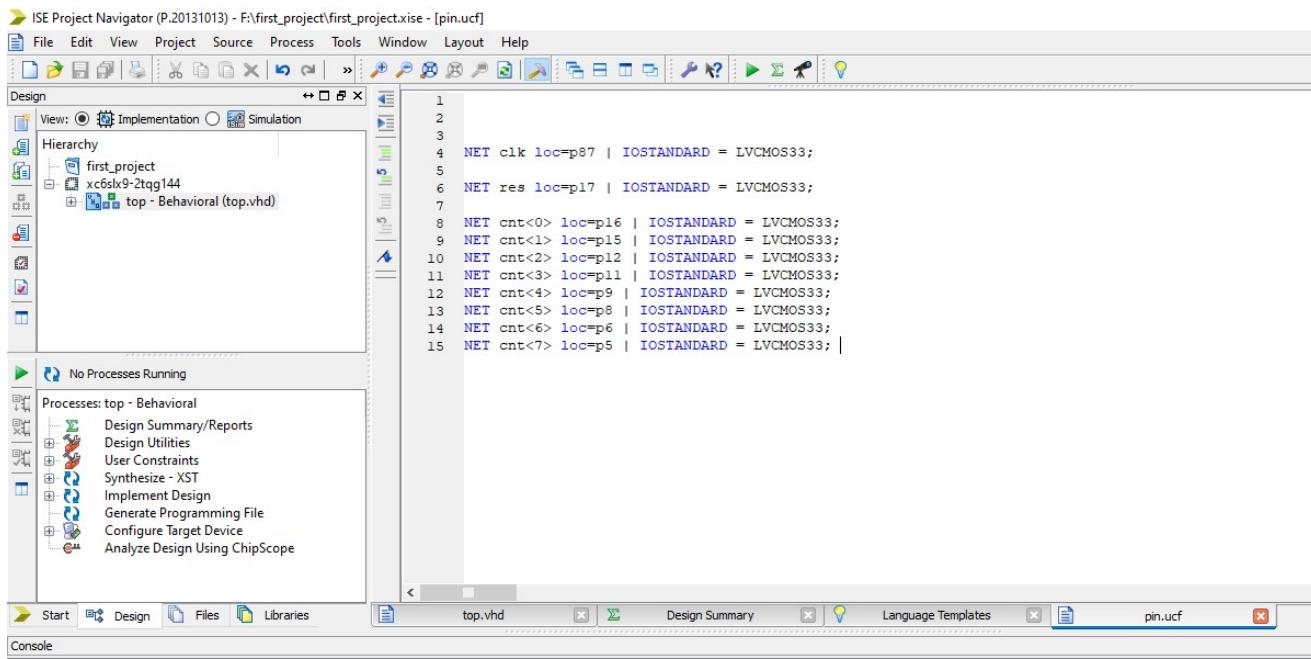
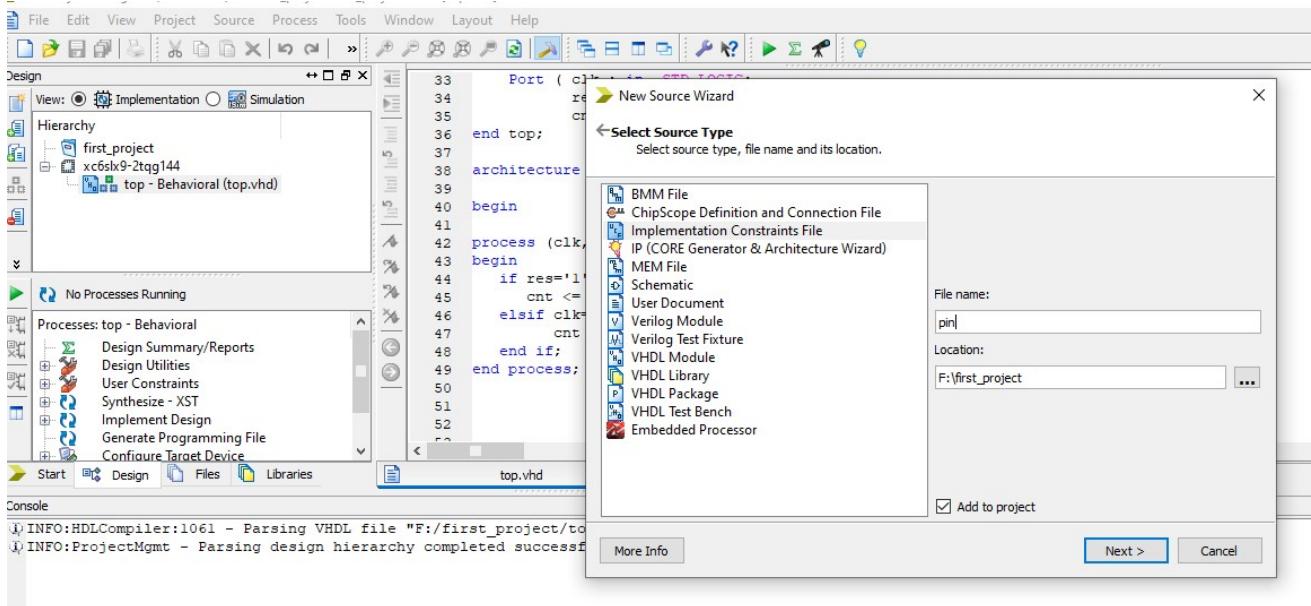




```

29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity top is
33     Port ( clk : in STD_LOGIC;
34             res : in STD_LOGIC;
35             cnt : out STD_LOGIC_VECTOR (7 downto 0));
36 end top;
37
38 architecture Behavioral of top is
39
40 begin
41
42 process (clk, res)
43 begin
44     if res='1' then
45         cnt <= (others => '0');
46     elsif clk='1' and clk'event then
47         cnt <= cnt + 1;
48     end if;
49 end process;
50
51
52
53
54 end Behavioral;
55

```



ISE Project Navigator (P.20131013) - F:\first\_project\first\_project.xise - [top.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- first\_project
  - xc6slx9-2tqg144
    - top - Behavioral (top.vhd)

Running: Synthesis

Processes: top - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
  - Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

```
1 LIBRARY IEEE;
2 USE IEEE.STD.LOGIC_1164.ALL;
3 USE IEEE.STD.LOGIC_ARITH.ALL;
4 USE IEEE.STD.LOGIC_UNSIGNED.ALL;
5 USE IEEE.NUMERIC_STD.ALL;
6
7 entity top is
8     Port ( clk : in STD_LOGIC;
9             res : in STD_LOGIC;
10            cnt : out STD_LOGIC_VECTOR (7 downto 0));
11 end top;
12
13 architecture Behavioral of top is
14
15 begin
16
17 process (clk, res)
18 begin
19     if res='1' then
20         cnt <= (others => '0');
21     elsif clk='1' and clk'event then
22         cnt <= cnt + 1;
23     end if;
24 end process;
25
26
27
28
```

tnn.vhd Design Summary (running) Language Templates

ISE Project Navigator (P.20131013) - F:\first\_project\first\_project.xise - [top.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- first\_project
  - xc6slx9-2tqg144
    - top - Behavioral (top.vhd)

No Processes Running

Processes: top - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
  - Generate Programming File
  - Configure Target Device
    - Generate Target PROM/ACE File
    - Manage Configuration Project (iMPACT)
    - Analyze Design Using ChipScope

```
2 USE IEEE.STD.LOGIC_1164.ALL;
3 USE IEEE.STD.LOGIC_ARITH.ALL;
4 USE IEEE.STD.LOGIC_UNSIGNED.ALL;
5 USE IEEE.NUMERIC_STD.ALL;
6
7 entity top is
8     Port ( clk : in STD_LOGIC;
9             res : in STD_LOGIC;
10            cnt : out STD_LOGIC_VECTOR (7 downto 0));
11 end top;
12
13 architecture Behavioral of top is
14
15 signal counter:STD_LOGIC_VECTOR (7 downto 0);
16 begin
17
18 process (clk, res)
19 begin
20     if res='1' then
21         cnt <= (others => '0');
22     elsif clk='1' and clk'event then
23         counter <= counter + 1;
24     end if;
25
26
27     cnt<=counter;
28
29
```

top.vhd Design Summary (Programming File Generated) Language Templates pin.ucf

