

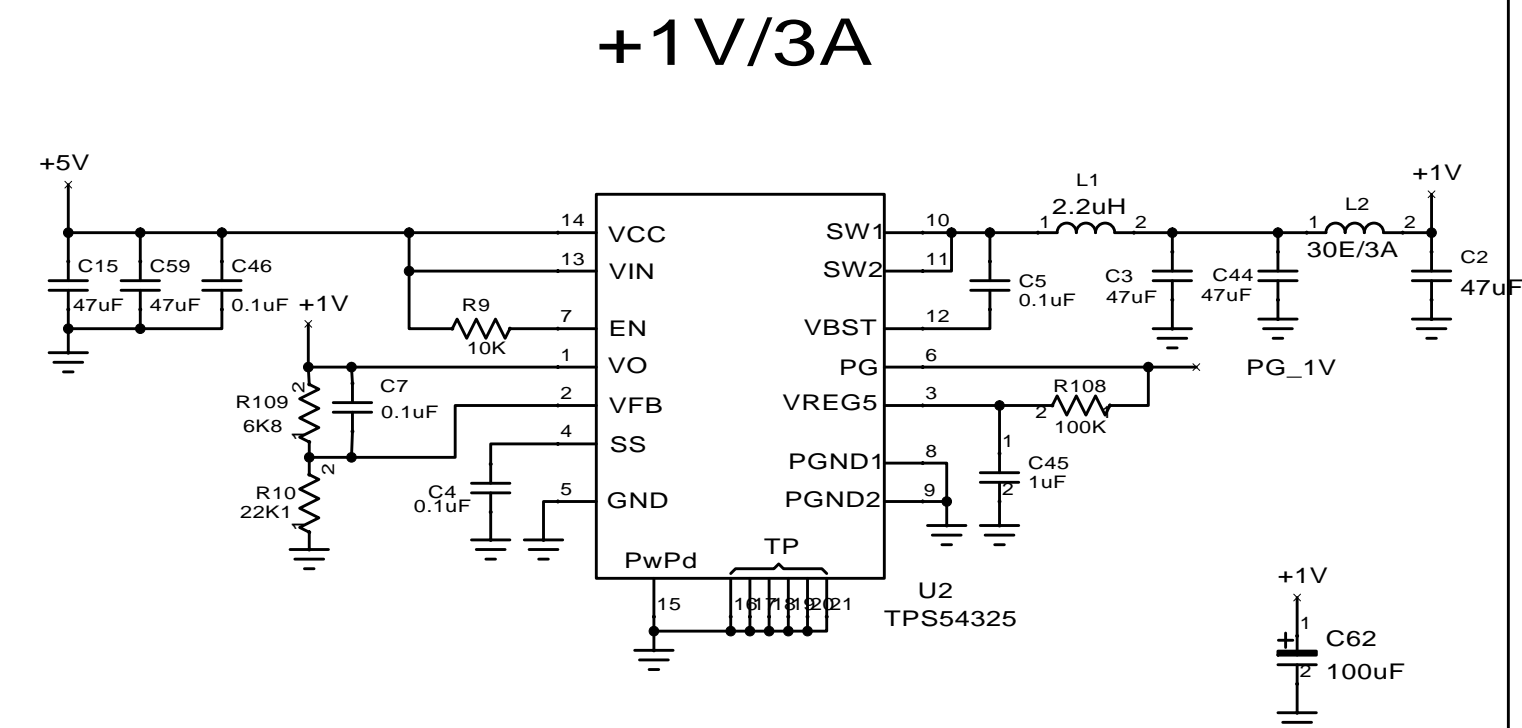
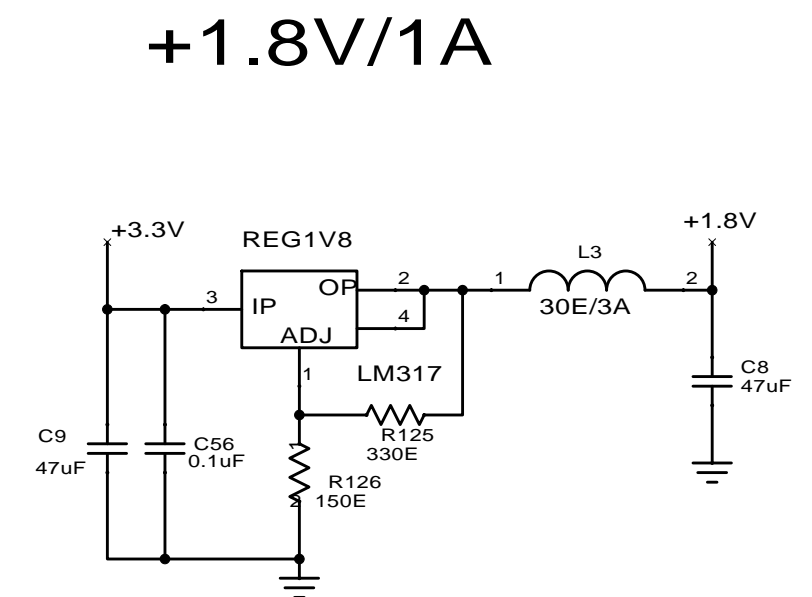
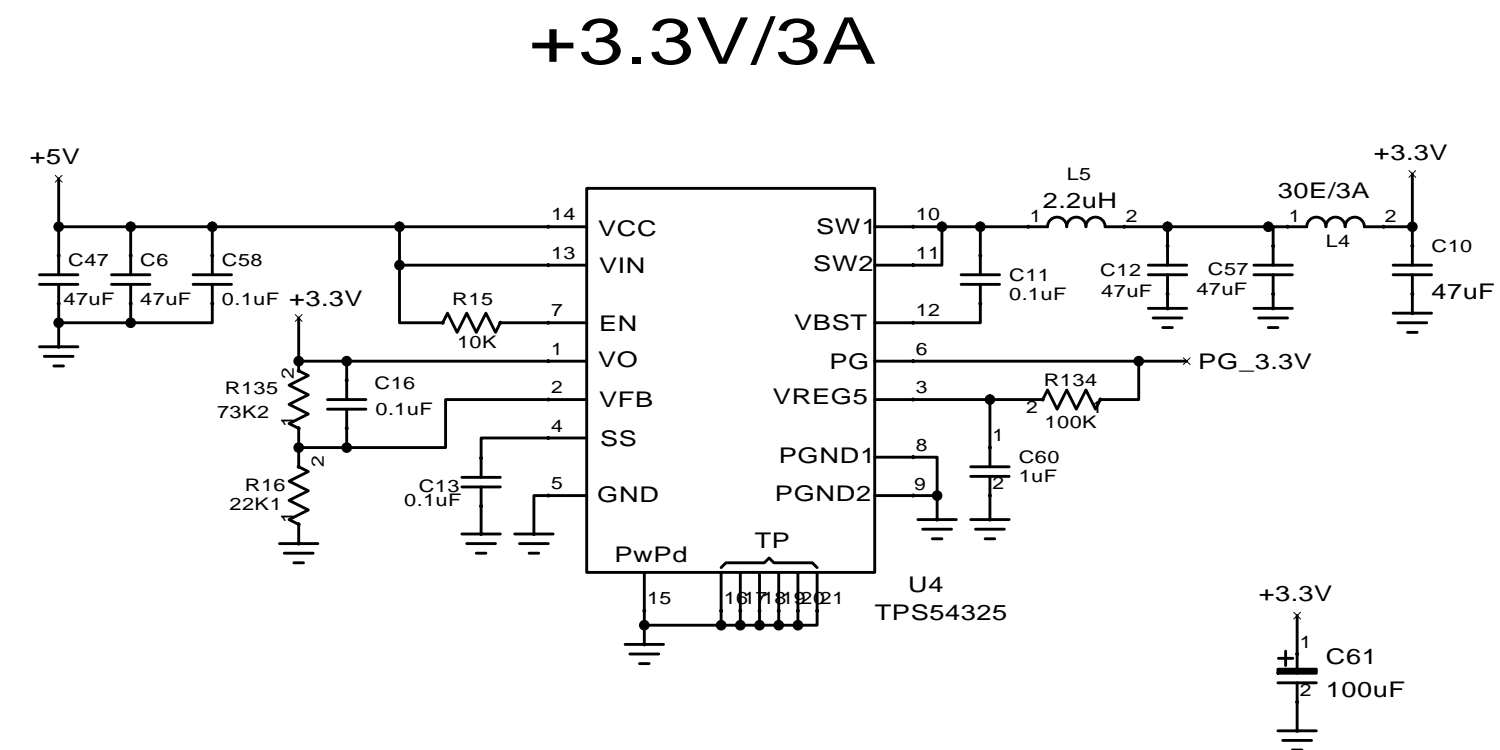
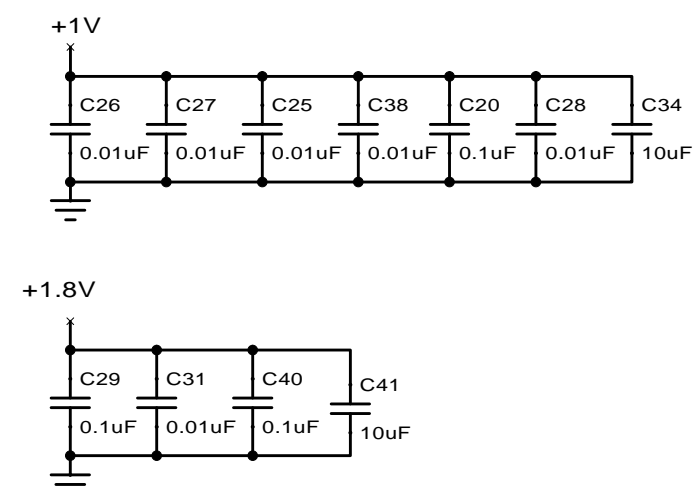
BERG-SR-2-M-ST

BERG-SR-3-M-ST

JP1

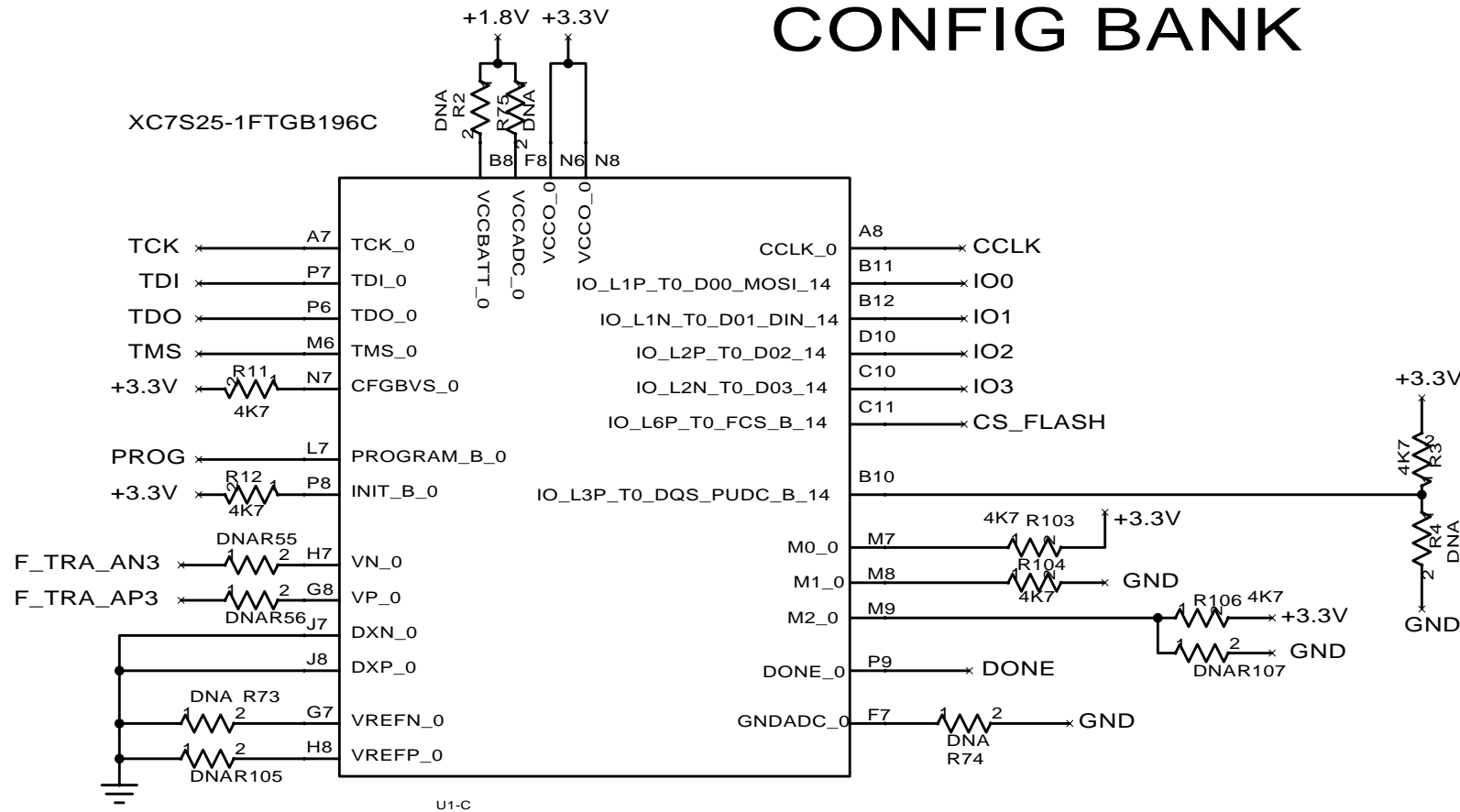
USB_PWR

+5V

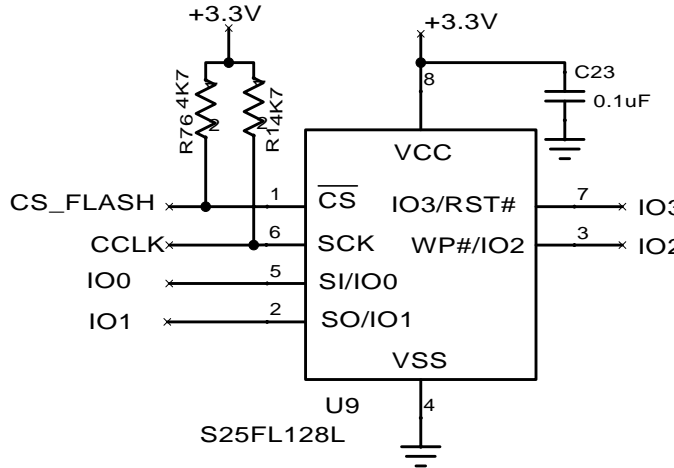
[illegible]
$$\begin{array}{l} \otimes^1 E^1_{\text{FIDUCIAL}} \\ \otimes^1 E^2_{\text{FIDUCIAL}} \\ \otimes^1 E^3_{\text{FIDUCIAL}} \\ \otimes^1 E^4_{\text{FIDUCIAL}} \\ \otimes^1 E^5_{\text{FIDUCIAL}} \\ \otimes^1 E^6_{\text{FIDUCIAL}} \end{array}$$


DWG NAME: PINE SPARTAN7		COMPANY NAME: FPGATECHSOLUTION	
DATE	15/11/2020	TITLE: PINE SPARTAN7	
DESIGNED		PCB NO. PINE_S7	REV.
CHECKED		SIZE: 82mm X 128mm	
DRAWN		CUSTOMER:	SHEET

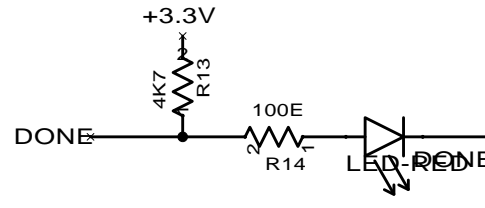
CONFIG BANK



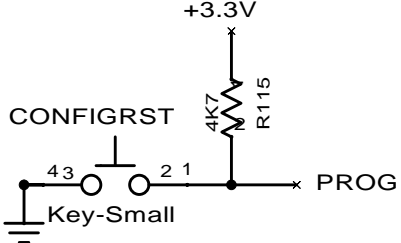
S25FL128L
FLASH



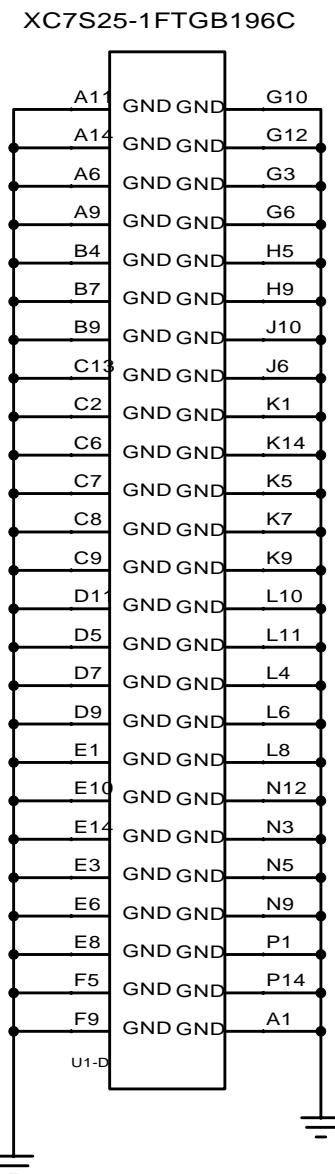
DONE LED



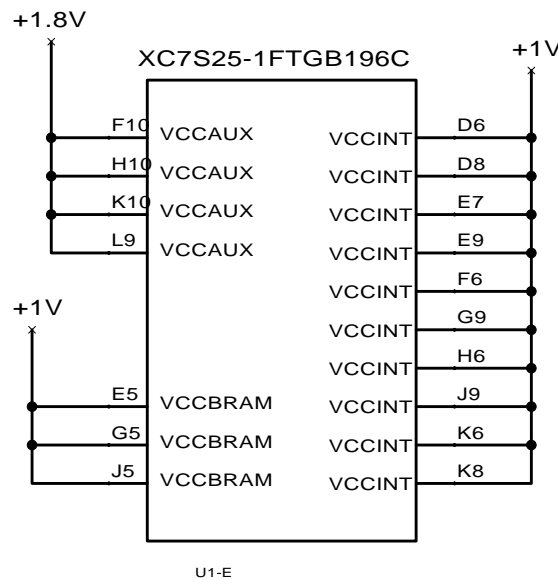
CONFIG RESET



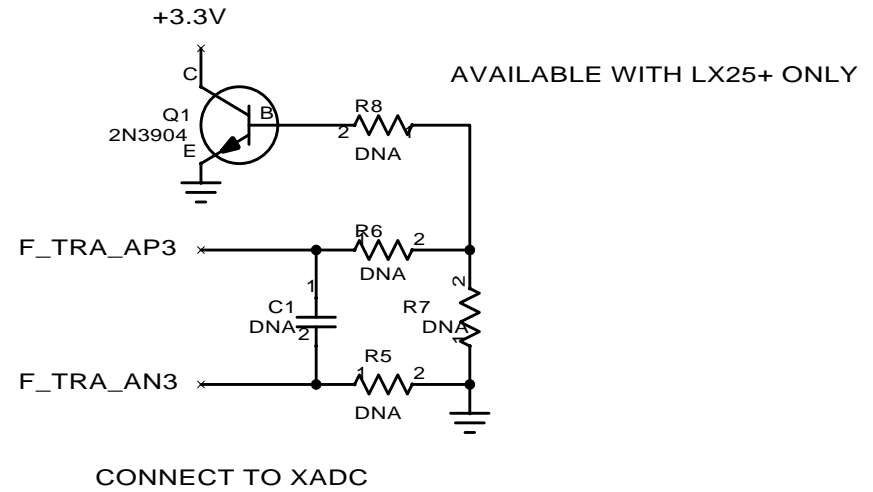
GND BANK



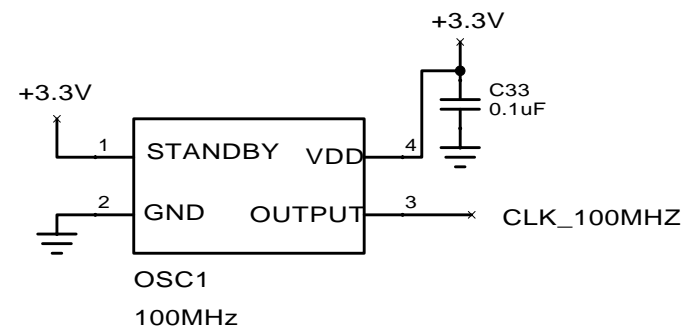
POWER BANK



LM35

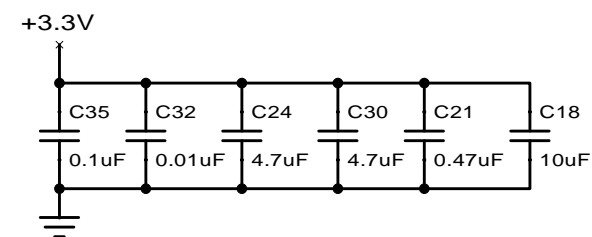
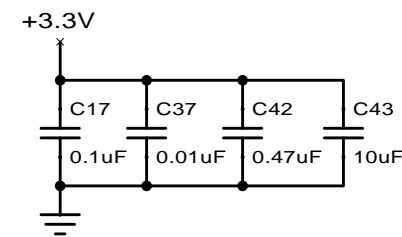
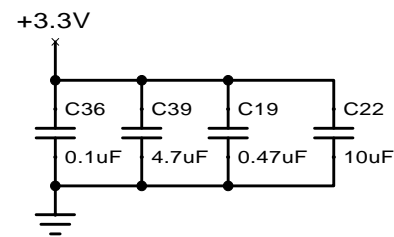
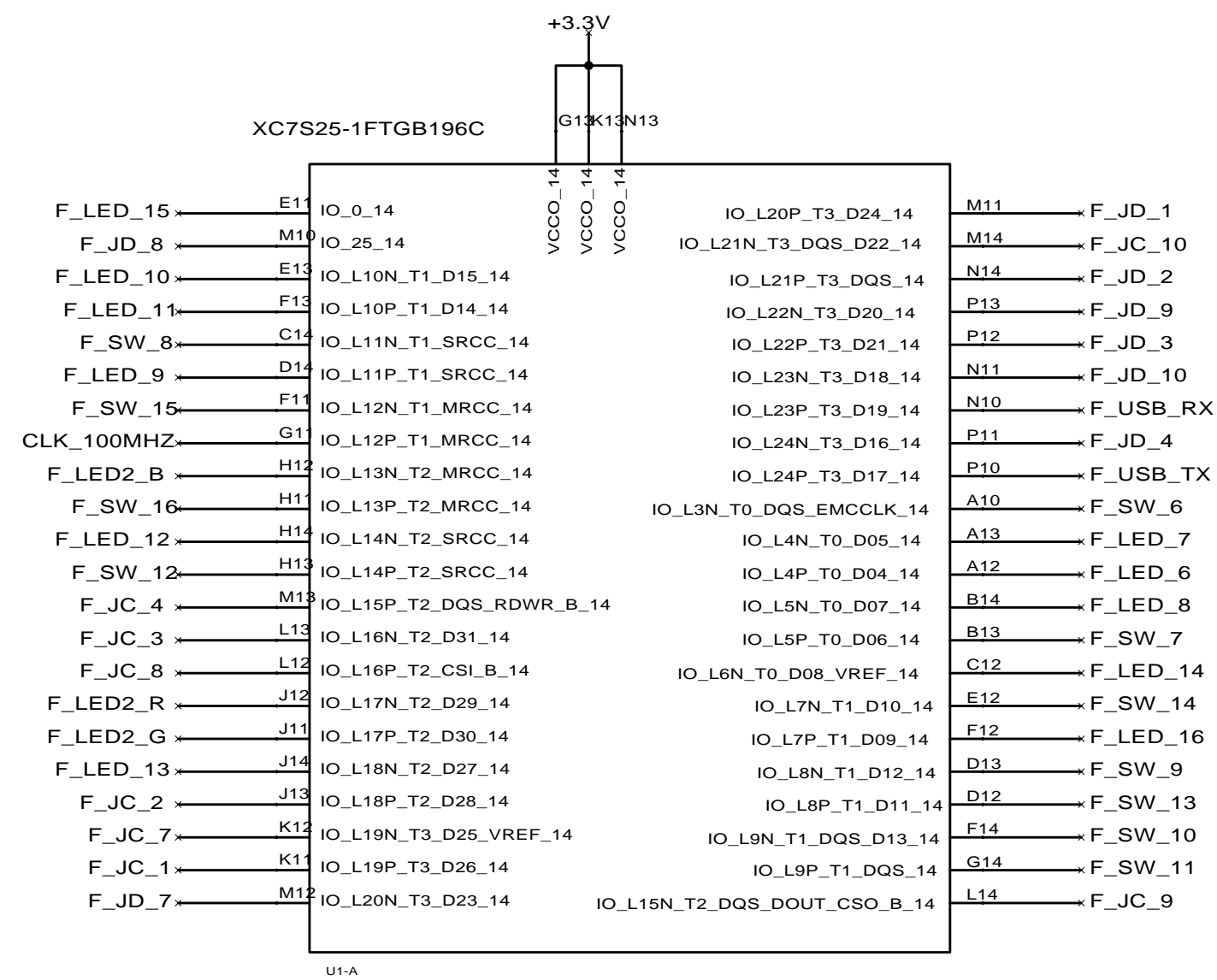


OSCILLATOR

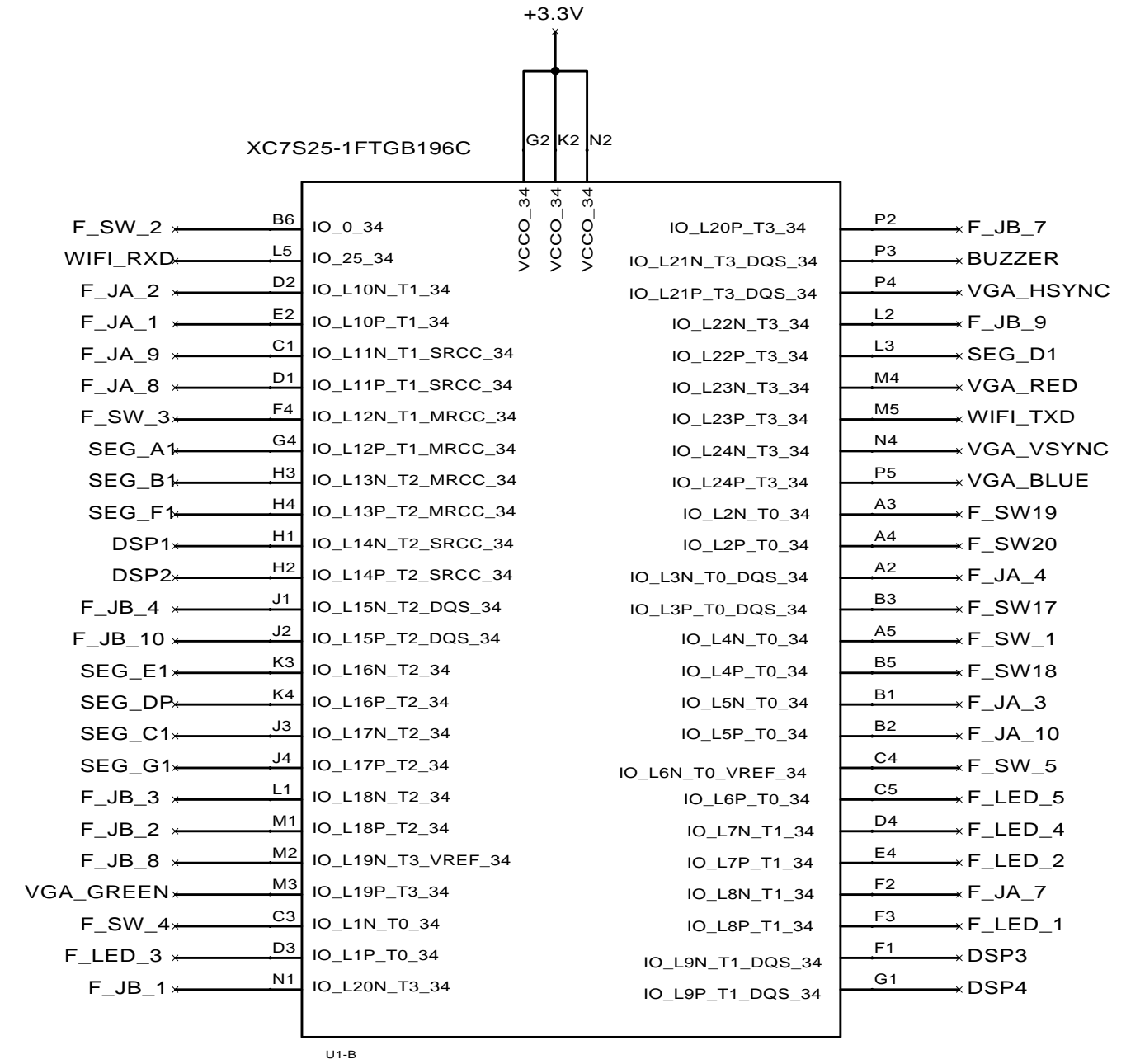


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CHECKED		SIZE: 82mm X 128mm	
DRAWN		CUSTOMER:	SHEET

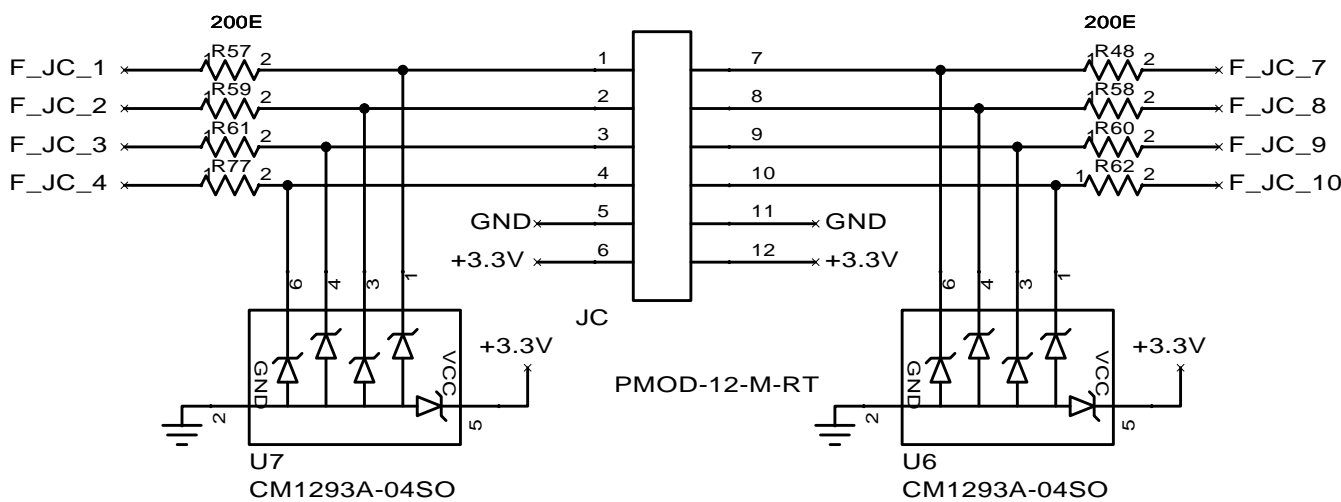
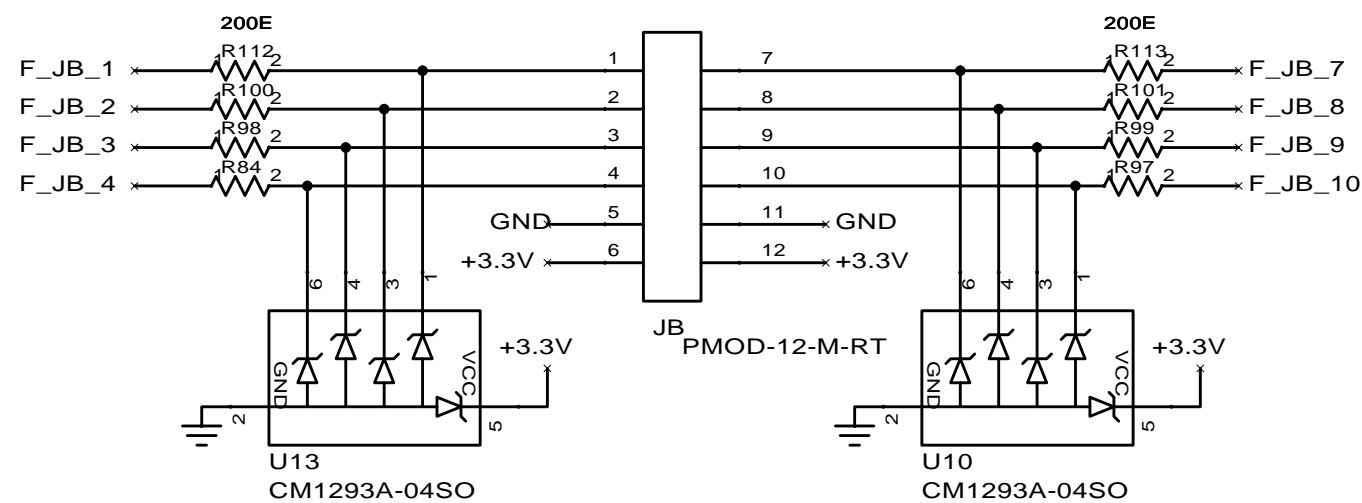
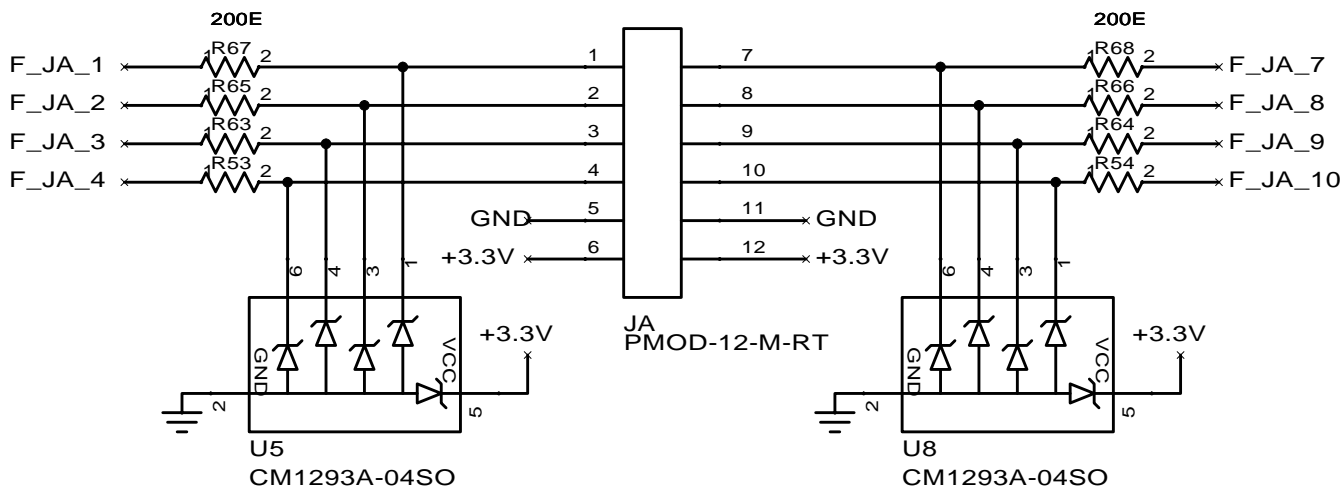
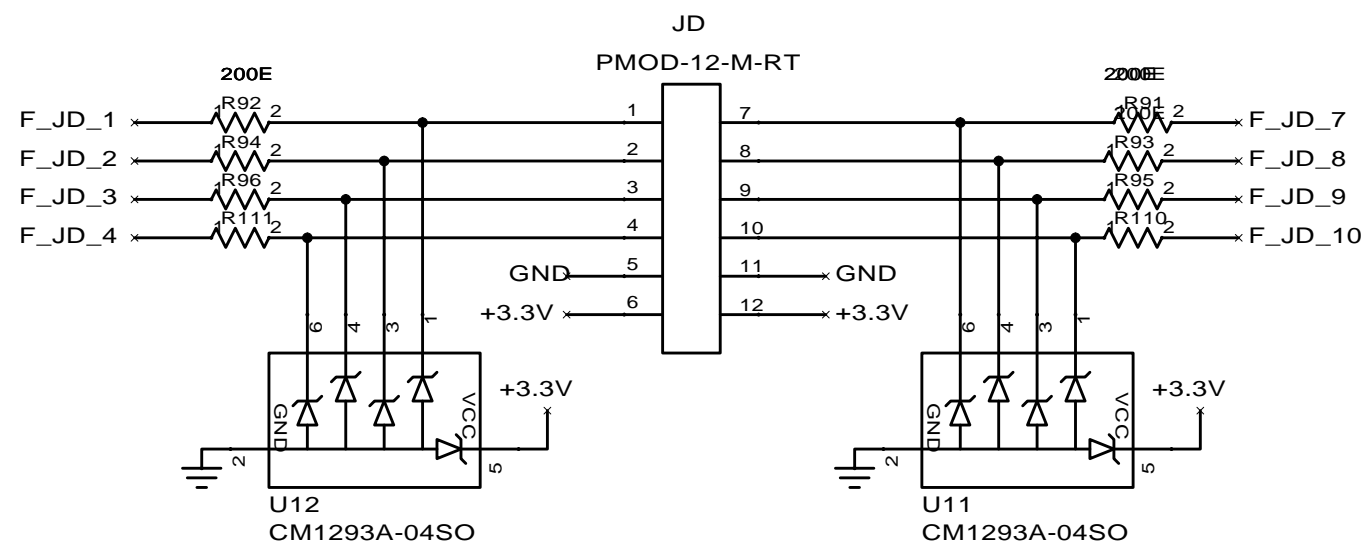
BANK 14



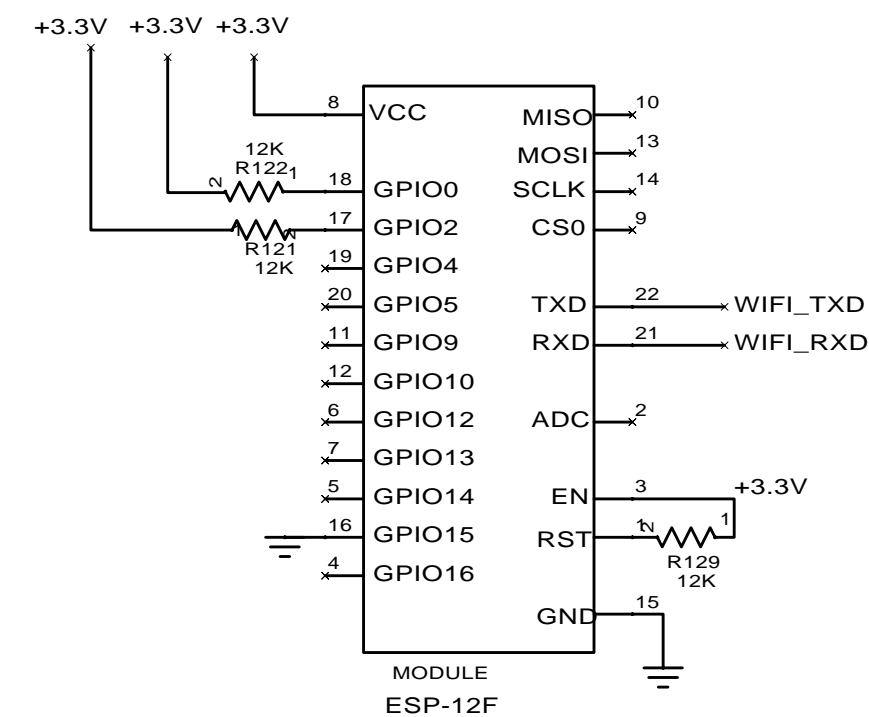
BANK 34



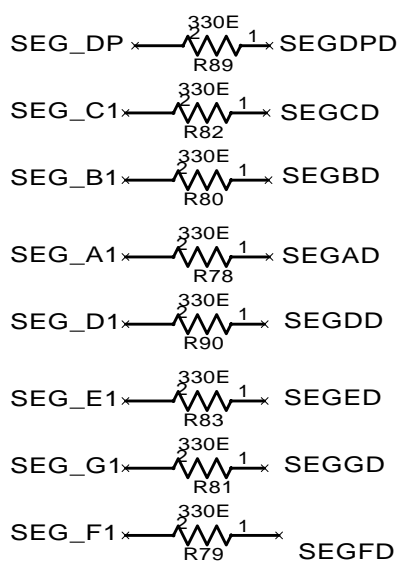
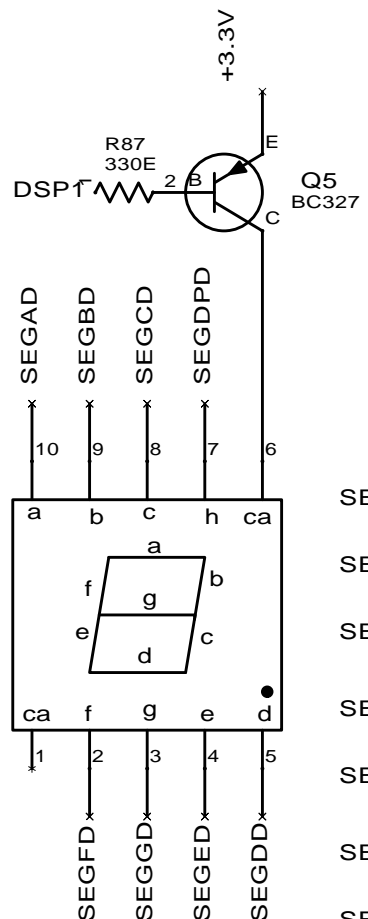
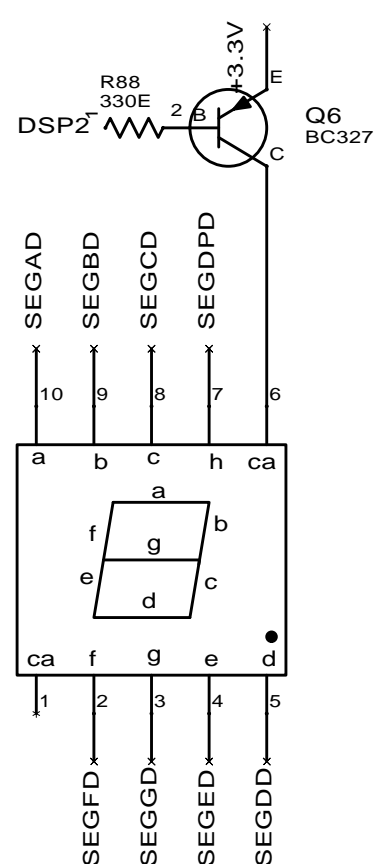
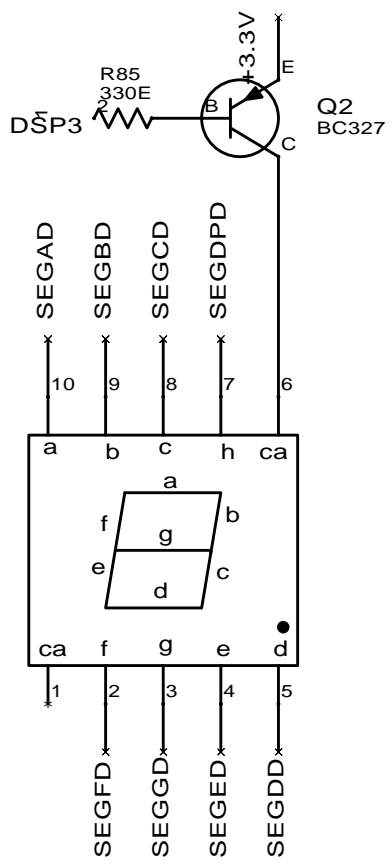
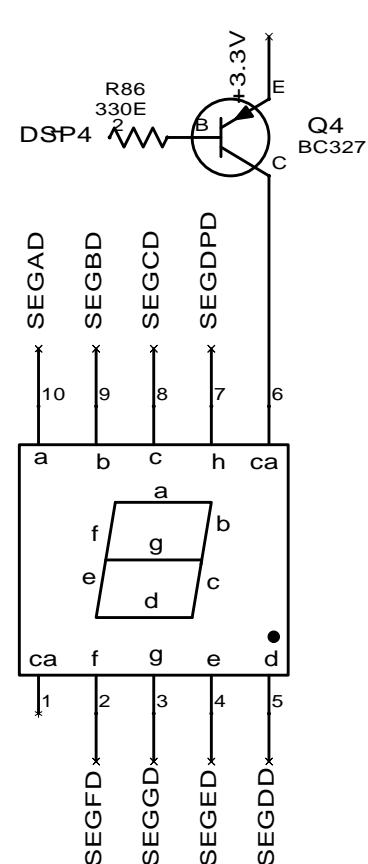
DWG NAME: PINE SPARTAN7		COMPANY NAME: FPGATECHSOLUTION	
DATE	15/11/2020	TITLE: PINE SPARTAN7	
DESIGNED		PCB NO. PINE_S7	REV.
CHECKED		SIZE: 82mm X 128mm	
DRAWN		CUSTOMER:	SHEET



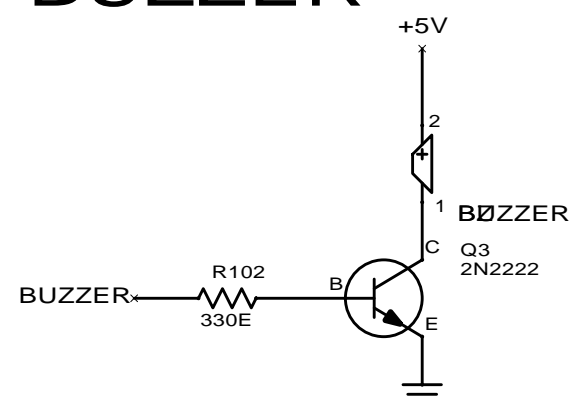
WIFI ESP-12E



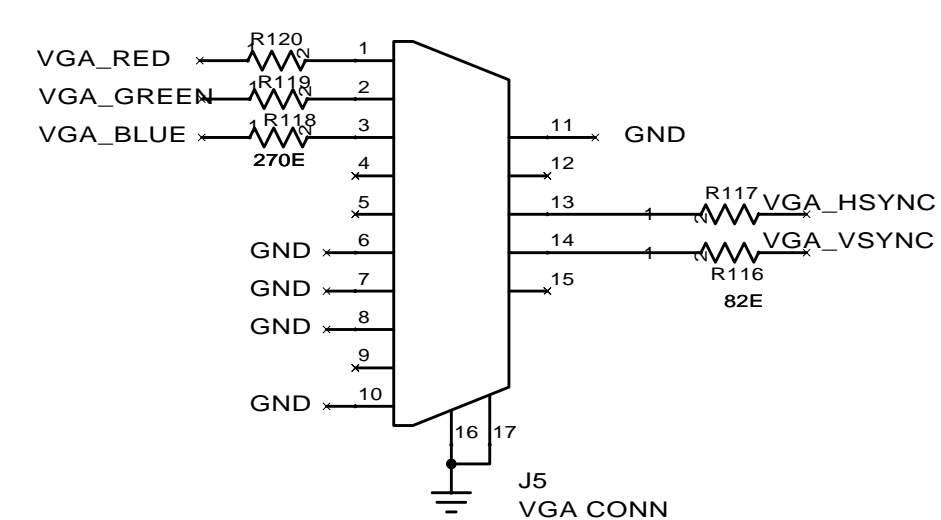
DISPLAY



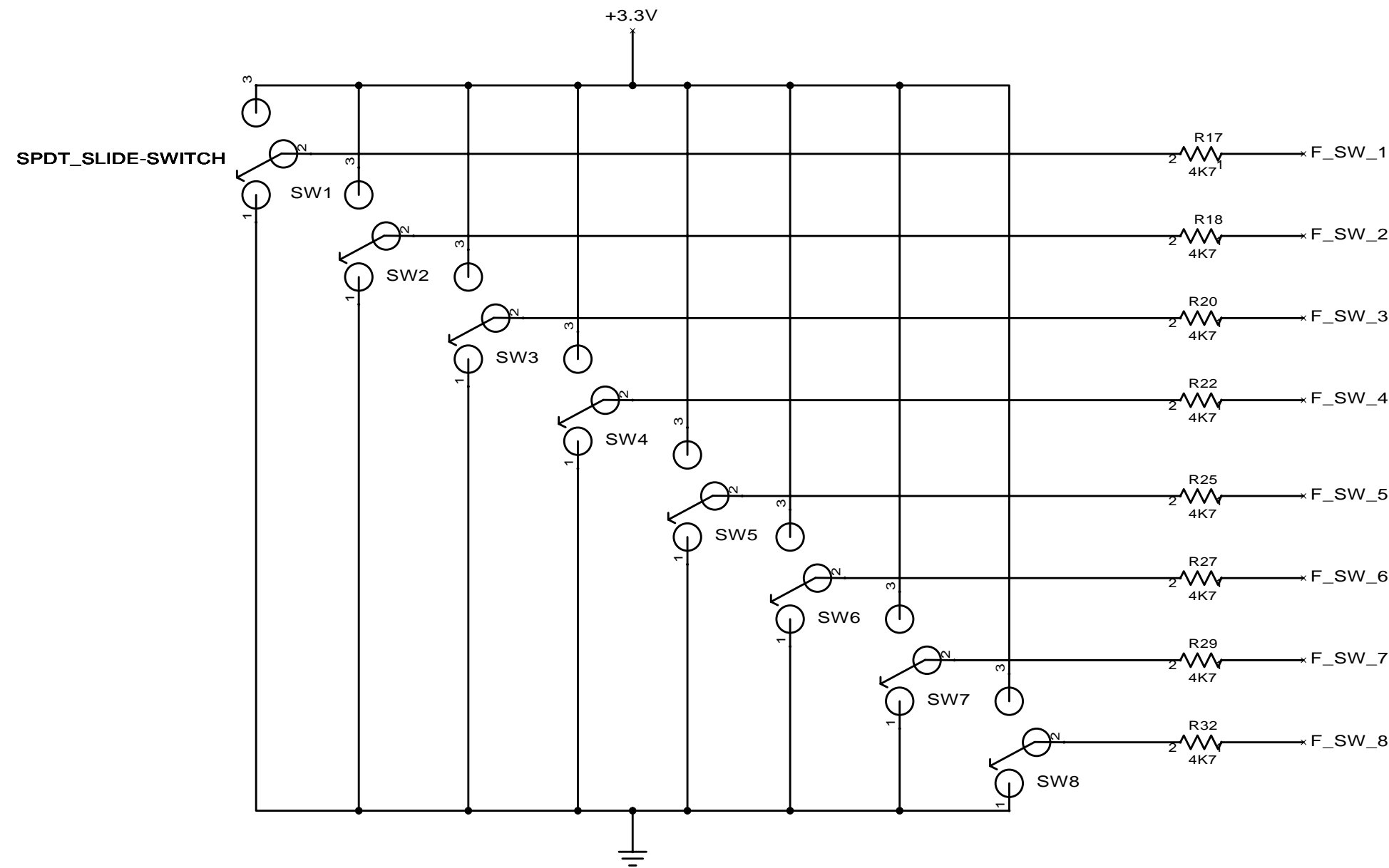
BUZZER



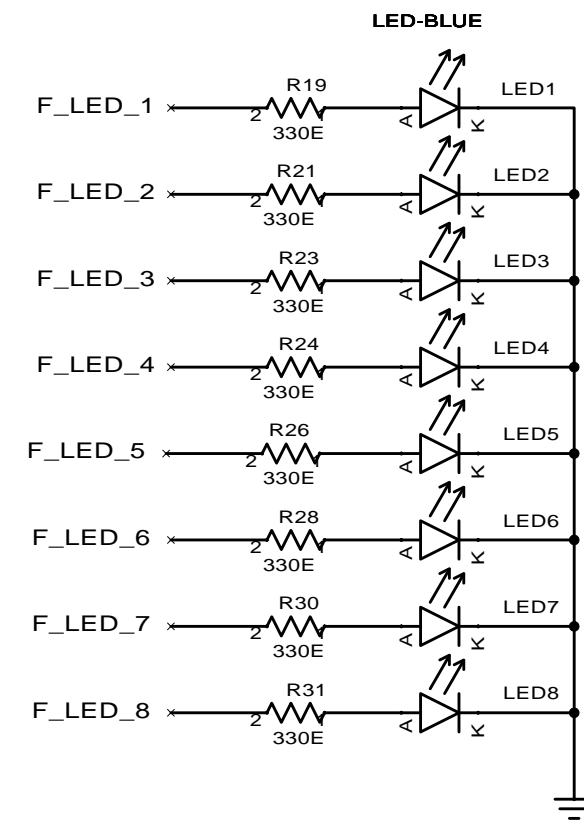
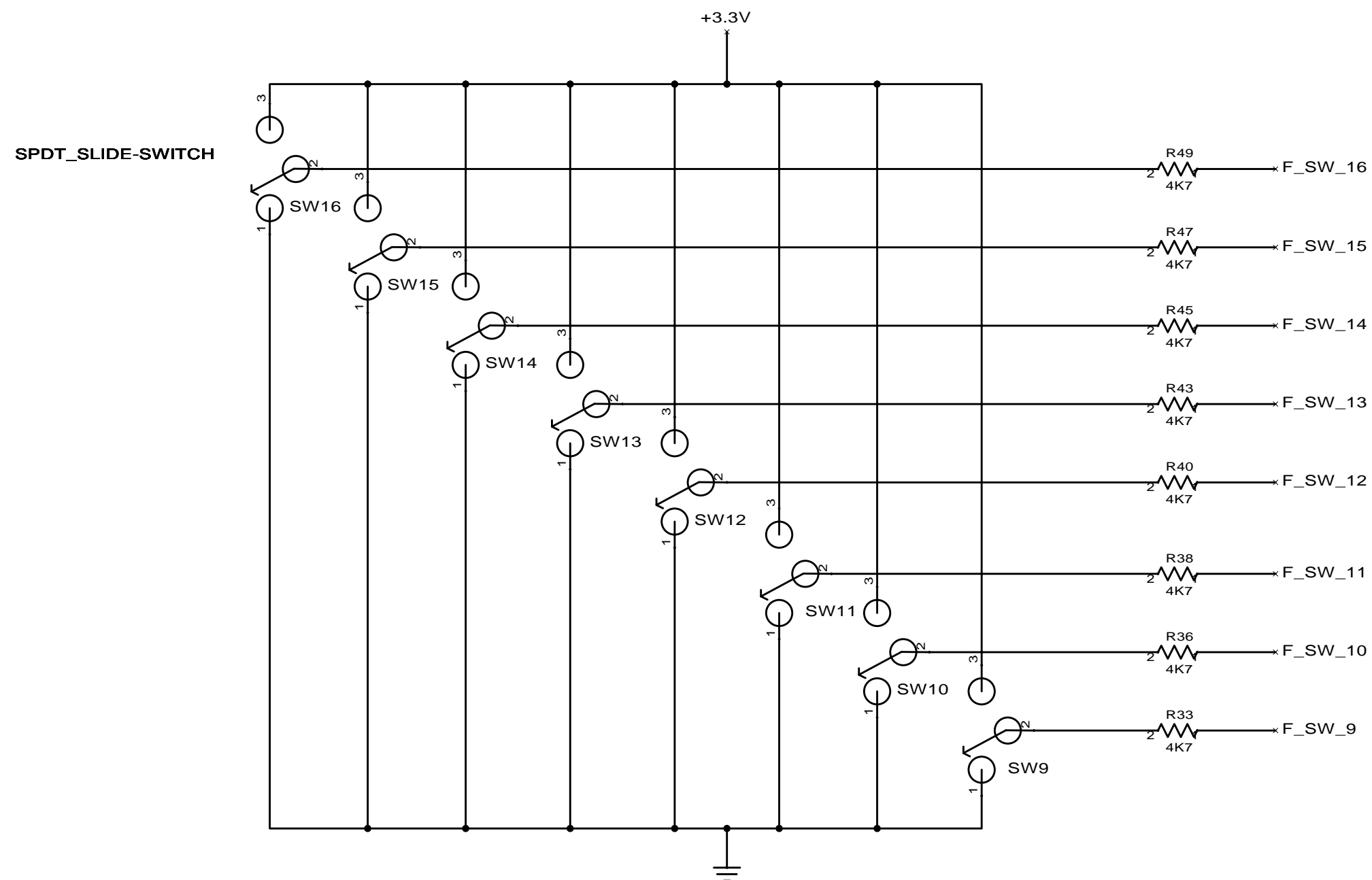
VGA



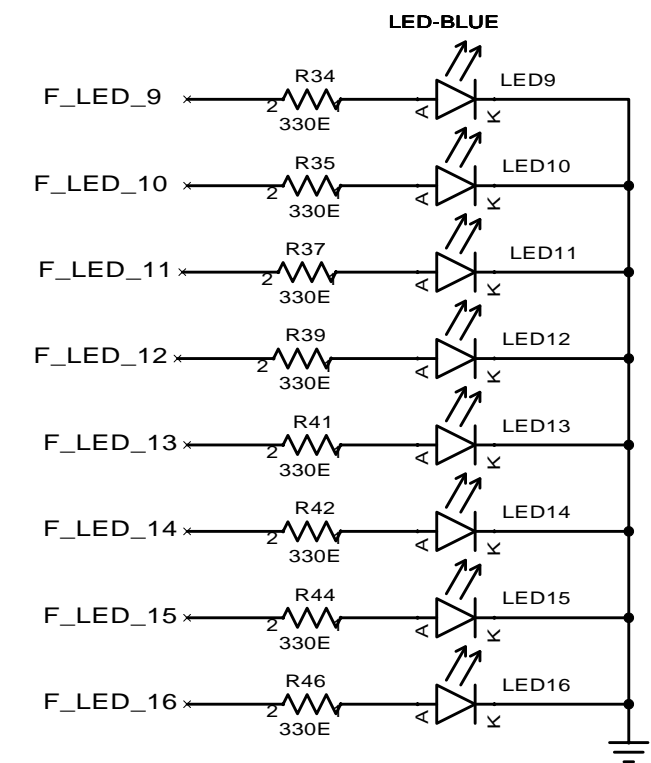
DWG NAME: PINE SPARTAN7		COMPANY NAME: FPGATECHSOLUTION	
DATE	15/11/2020	TITLE: PINE SPARTAN7	
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CHECKED		SIZE: 82mm X 128mm	
DRAWN		CUSTOMER:	SHEET



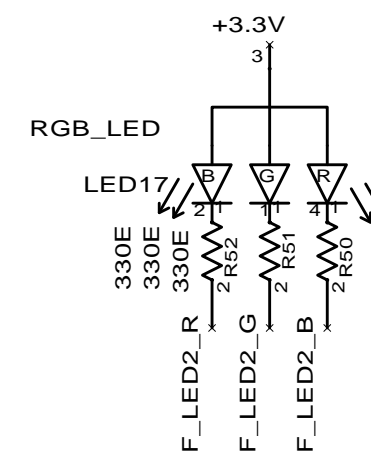
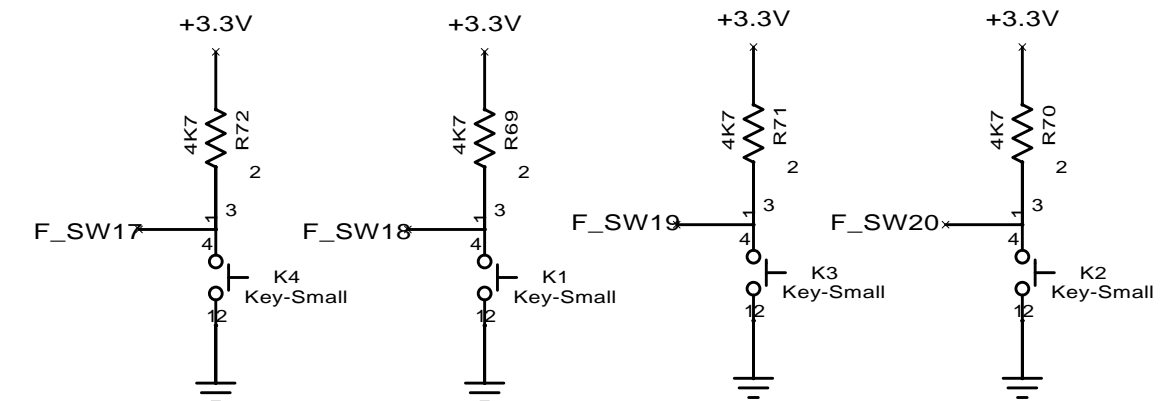
SLIDE SWITCH



LED



PUSH BTN



RGB LED

DWG NAME: PINE SPARTAN7		COMPANY NAME: FPGATECHSOLUTION	
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DRAWN		CUSTOMER:	SHEET