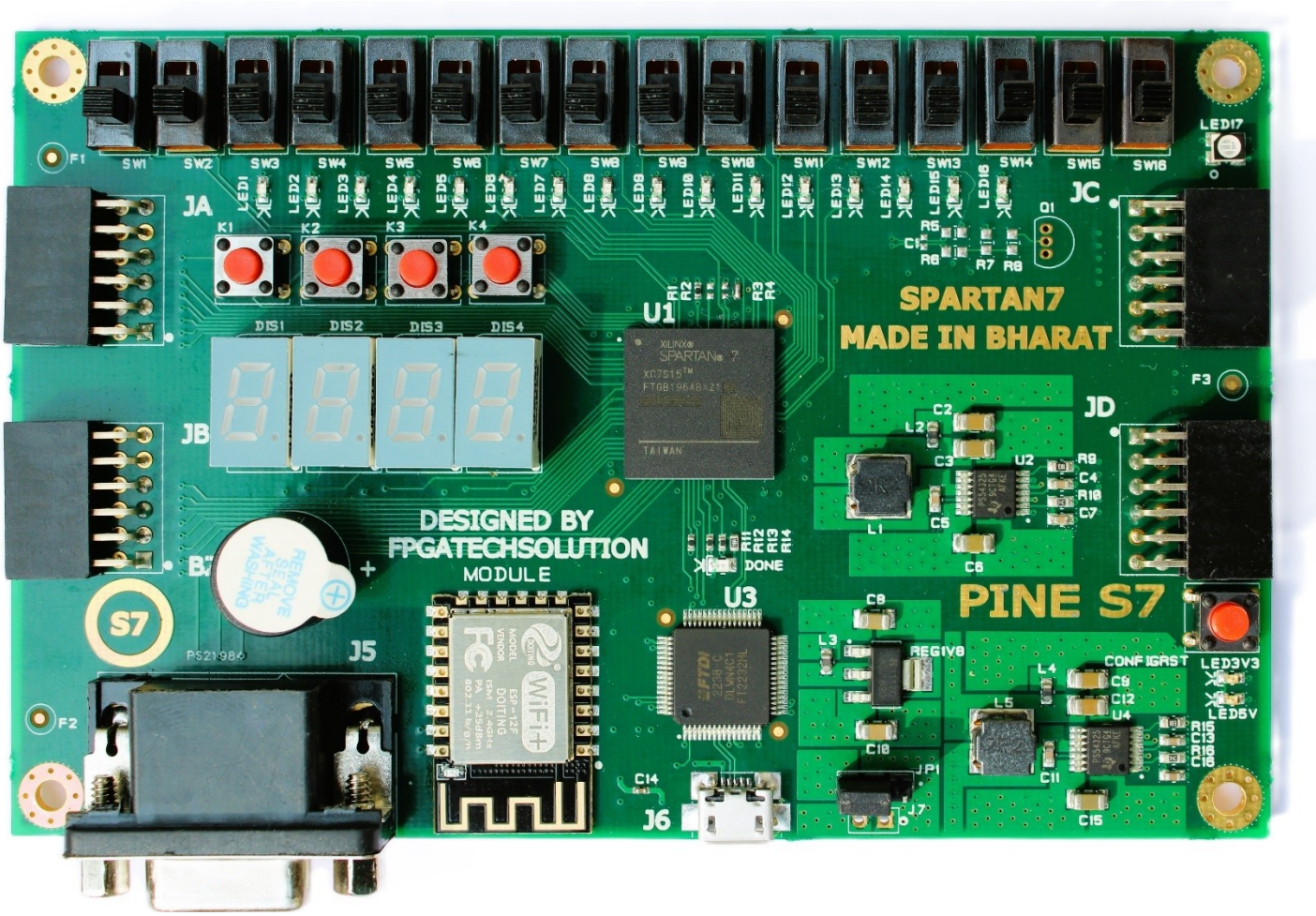
FPGA TECH SOLUTION

...SOLUTION AHEAD



lick here to download schematic & source code for PINS S7.

Introduction

The PINE-S7 board is a complete, ready-to-use digital circuit development platform based on the latest Spartan7 Field Programmable Gate Array (FPGA) from Xilinx. With its high-capacity FPGA (Xilinx part number XC7S15FTGB196-1), low overall cost, and collection of USB, VGA, and other ports, the PINE-S7 can host designs ranging from introductory combinational circuits to complex sequential circuits like embedded processors and controllers. It includes enough switches, LEDs and other I/O devices to allow a large number designs to be completed without the need for any additional hardware, and enough uncommitted FPGA I/O pins to allow designs to be expanded using Pmods or other custom boards and circuits.
The PINE-S7 board has on board USB JTAG which support Vivado & vitis.

Note: on request this board can be available with **XC7S25FTGB196-1** OR **XC7S50FTGB196-1**

Applications

- Product Prototype Development
- Development and testing of custom embedded processors
- Signal Processing
- Communication devices development
- Educational tool for Schools and Universities

Features

The Spartan-7 FPGA is optimized for high performance logic, and offers more capacity, higher performance, and more resources than earlier designs. Spartan-7 XC7S15FTGB196-1 features include:

- 12,800 logic cells in 5000 slices (each slice contains four 6-input LUTs and 8 flip-flops);
- 360 Kbits of fast block RAM;
- Two clock management tiles, each with a phase-locked loop (PLL);
- 20 DSP slices;
- Internal clock speeds exceeding 450MHz;

The PINE-S7 also offers an improved collection of ports and peripherals, including:

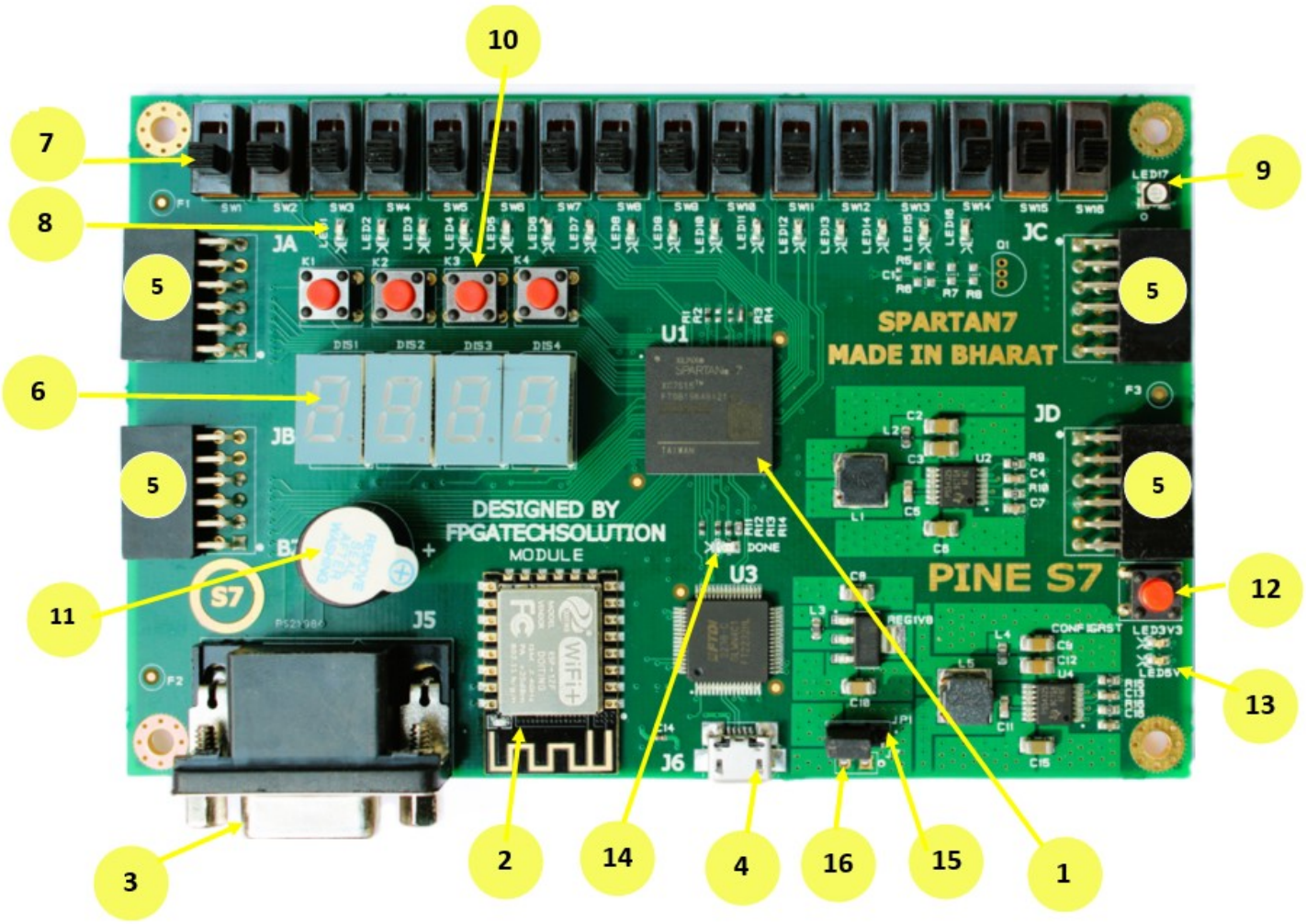
- 16 user switches
- 16 user LEDs
- 4 user pushbuttons
- 100MHz clock
- 4-digit 7-segment display
- Four Pmod ports (32GPIO)
- ESP-12E WiFi
- Buzzer
- RGB LED
- VGA output
- USB-UART Bridge
- Serial Flash
- USB-JTAG port for FPGA programming and communication (support Vivado)

Add on module available:

- 16By2LCD
- 4X4 matrix keypad
- OV7670 Camera module
- 4 user pushbuttons
- 4 channel ADC & DAC

Software--The first Vivado Design Suite Exclusive: **(Recommended Vivado 19.1)**

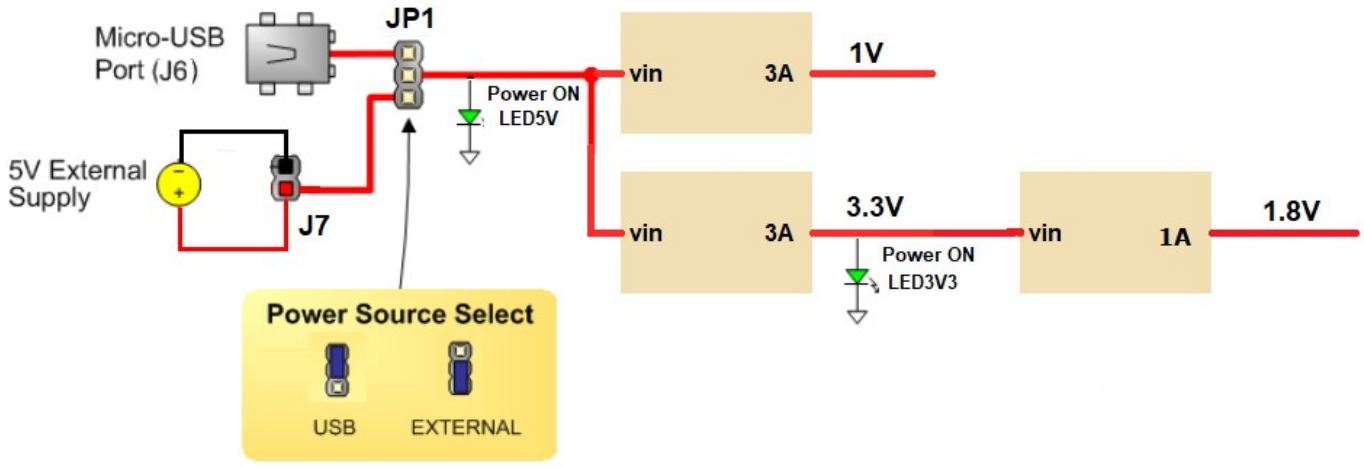
The PINE-S7 works with Xilinx's new high-performance Vivado ® Design Suite. Vivado includes many new tools and design flows that facilitate and enhance the latest design methods. It runs faster, allows better use of FPGA resources, and allows designers to focus their time evaluating design alternatives. The System Edition includes an on-chip logic analyzer, high-level synthesis tool, and other cutting-edge tools, and the free "**WebPACK**" version allows PINE-S7 designs to be created at no additional cost.



Sr. No.	component description	Sr. No.	component description
1	SPARTAN 7 FPGA	9	RGB LED
2	ESP-12E Wi-Fi module	10	Pushbuttons (4)
3	VGA	11	Buzzer
4	USB JTAG/UART	12	Configuration Reset
5	Pmod Connector (4)	13	Power LED
6	Seven Segments (4)	14	Configuration Done LED
7	Slide Switches (16)	15	Power selection Jumper
8	LEDs (16)	16	External Power connector

BOARD POWERING

The PINE-S7 uses +5V power supply to function properly. By default, the board is configured to use +5V supply from USB. External +5V power is not required unless USB port is unable to supply enough current. In most cases USB ports are capable of providing enough current for the module. Current requirement for this board largely depends on your application. Please consult FPGA data sheet for more details on power requirements. If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly as shown below When JP1 jumper is placed towards USB as shown in below image power is used from USB connector & when JP1 jumper is placed towards power connector power is used from external connector

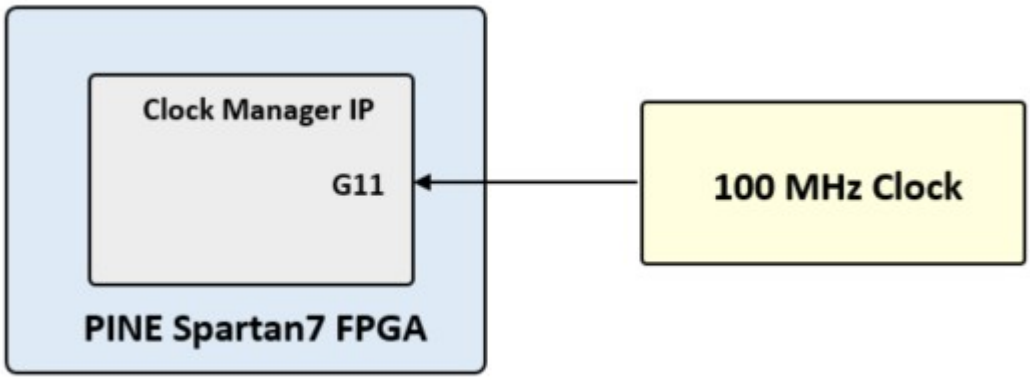


Oscillators/ Clocks

The PINE-S7 board includes a single 100MHz oscillator connected to pin G11 (G11 is a MRCC input on bank 14). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100MHz input clock. For a full description of these rules and of the capabilities of the Spartan-7 clocking resources, refer to the “7 Series FPGAs Clocking Resources User Guide” available from

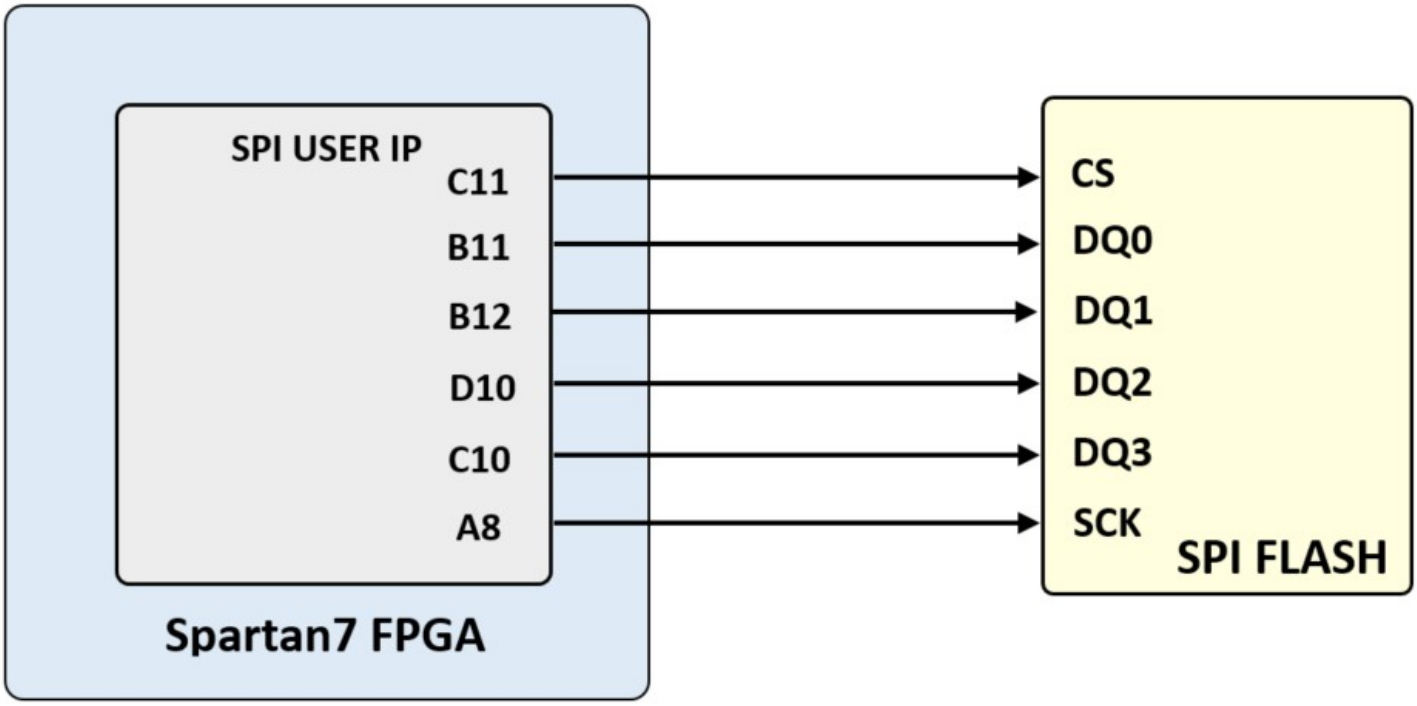
Xilinx http://www.xilinx.com/support/documentation/user_guides/ug472_7Series_Clocking.pdf.

Xilinx offers the Clocking Wizard IP core to help users generate the different clocks required for a specific design. This wizard properly instantiates the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy to use wrapper component around these clocking resources that can be inserted into the user’s design. The Clocking Wizard can be accessed from within IP Catalog, which can be found under the Project Manager section of the Flow Navigator in Vivado.



SPI FLASH

The PINE-S7 board contains a 128Mbit non-volatile serial Flash device, which is attached to the Spartan 7 FPGA using a dedicated quad-mode (x4) SPI bus. The connections and pin assignments between the FPGA and the serial flash device are shown the below figure



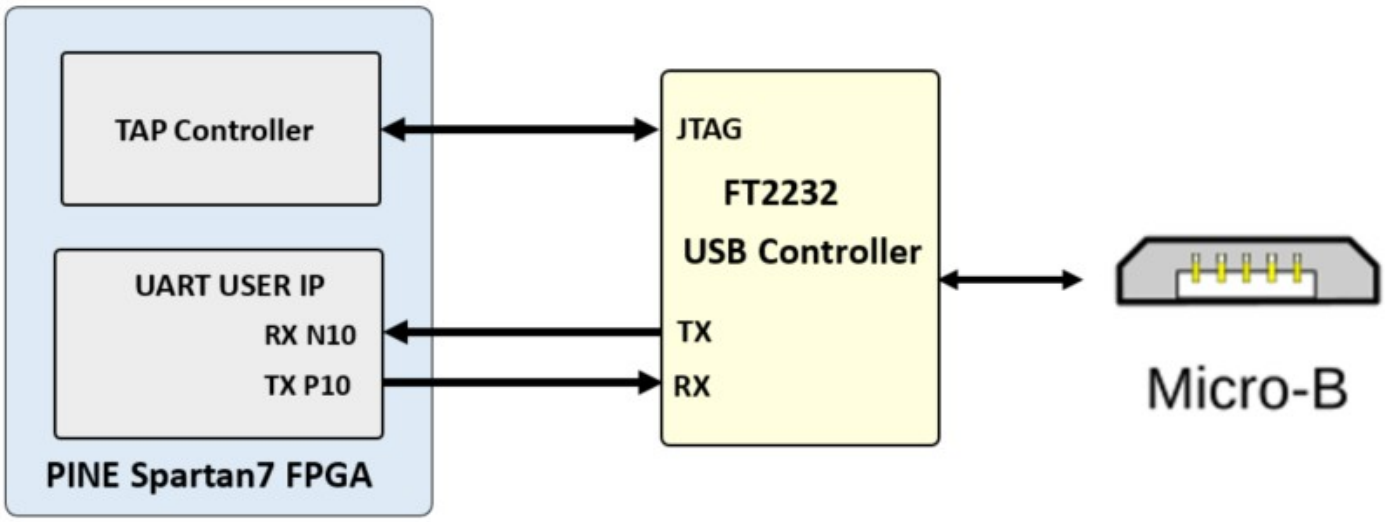
PINE-S7 have been loaded with a Flash device from Cypress (part number S25FL128).FPGA configuration files can be written to the Quad SPI Flash, and mode settings are available to cause the FPGA to automatically read a configuration from this device at power on. An FPGA configuration file requires just over one Mbytes of memory, leaving approximately 98% of the flash device available for user data.

USB-UART Bridge (Serial Port)

The PINE-S7 includes an FTDI FT2232HL

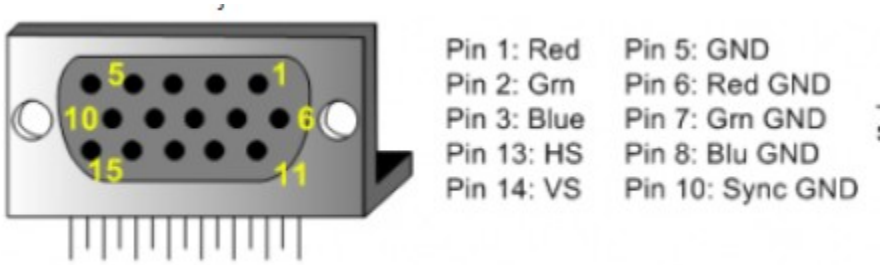
http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232H.pdf USB-UART bridge (attached to connector J6) that allows you to use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the “Virtual Com Port” or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the M5 and L5 FPGA pins.

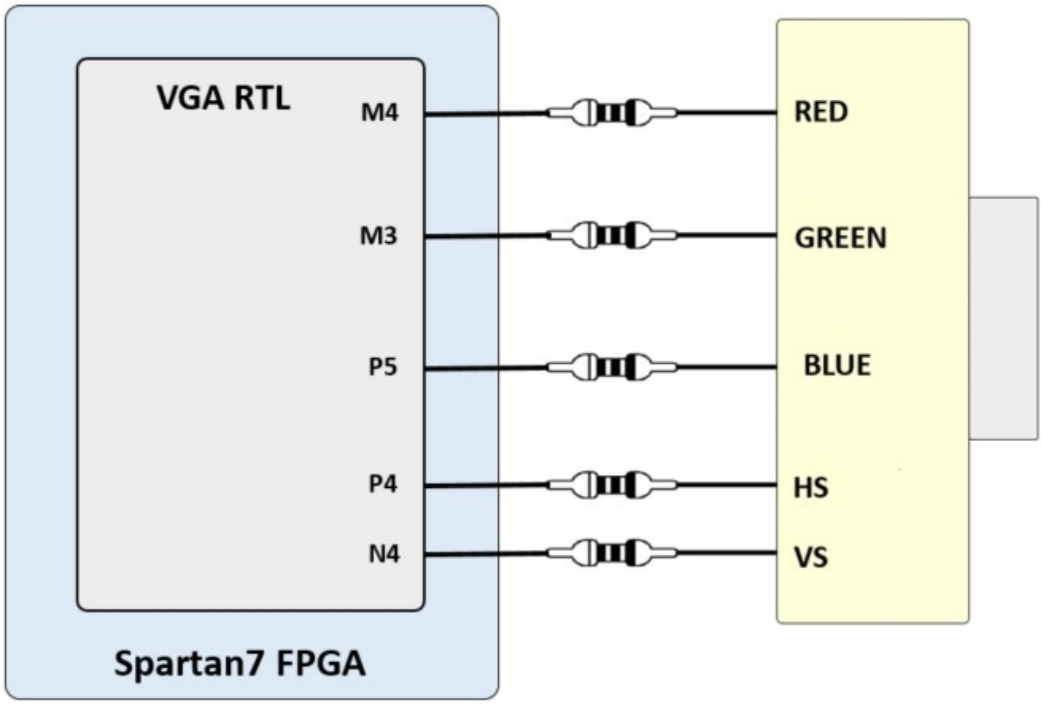
The FT2232HL is also used as the controller for the USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the PINE-S7 to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable. The connections between the FT2232HQ and the Artix-7 are shown in the below figure.



VGA Port

The PINE-S7 board uses 5 FPGA signals to create a VGA port with 1 bits-per-color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 82-ohm termination resistance of the VGA display to create 16 signal levels each on the red, green, and blue VGA signals.

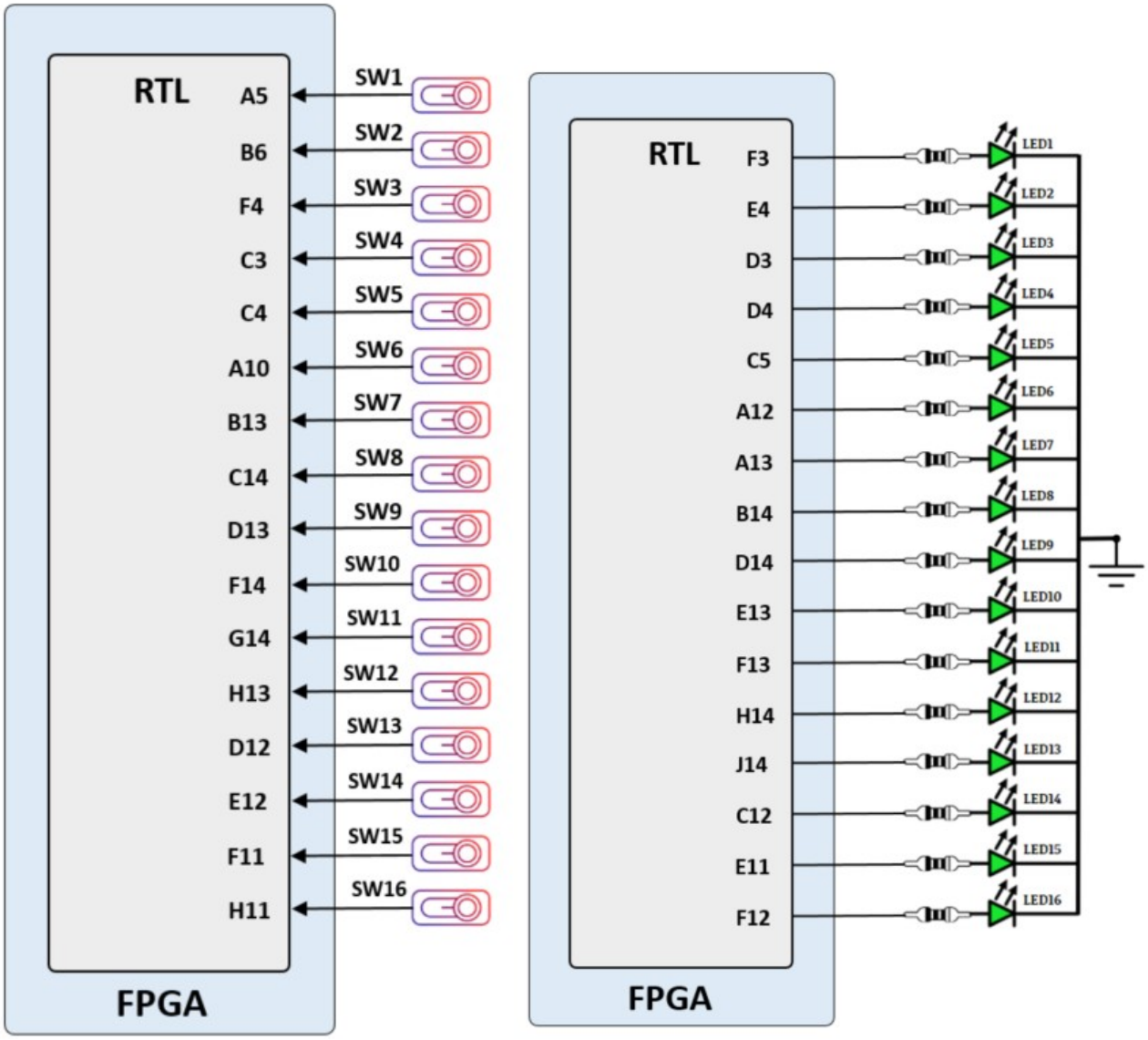




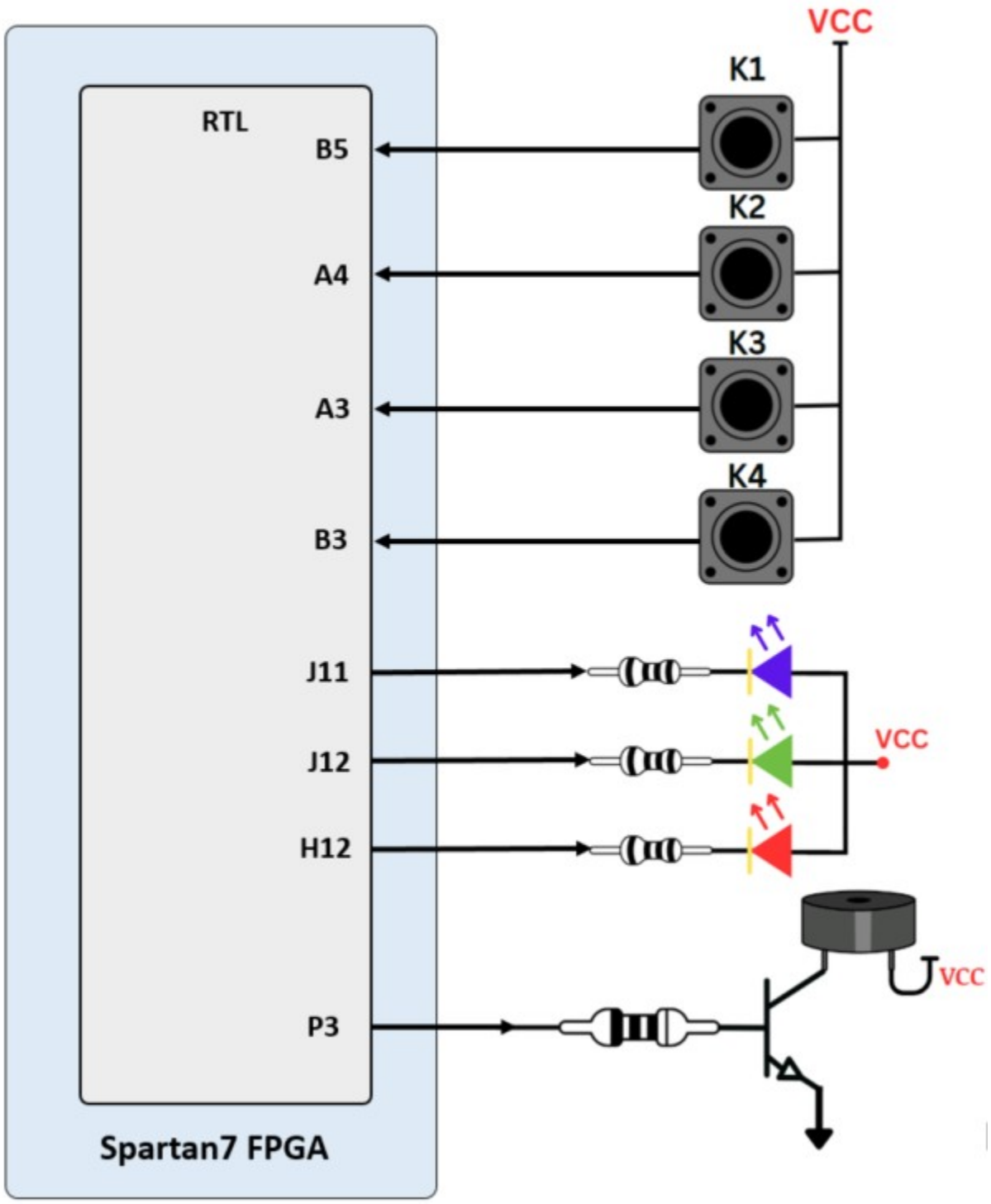
This circuit, shown in the above diagram, , produces video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 4096 different colors can be displayed, one for each unique 3-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

Basic I/O

The PINE-S7 board includes sixteen slide switches, four push buttons, sixteen individual LEDs, and a four-digit seven-segment display, as shown in the below diagram. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The four pushbuttons are “momentary” switches that normally generate a high output when they are at rest, and a low output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

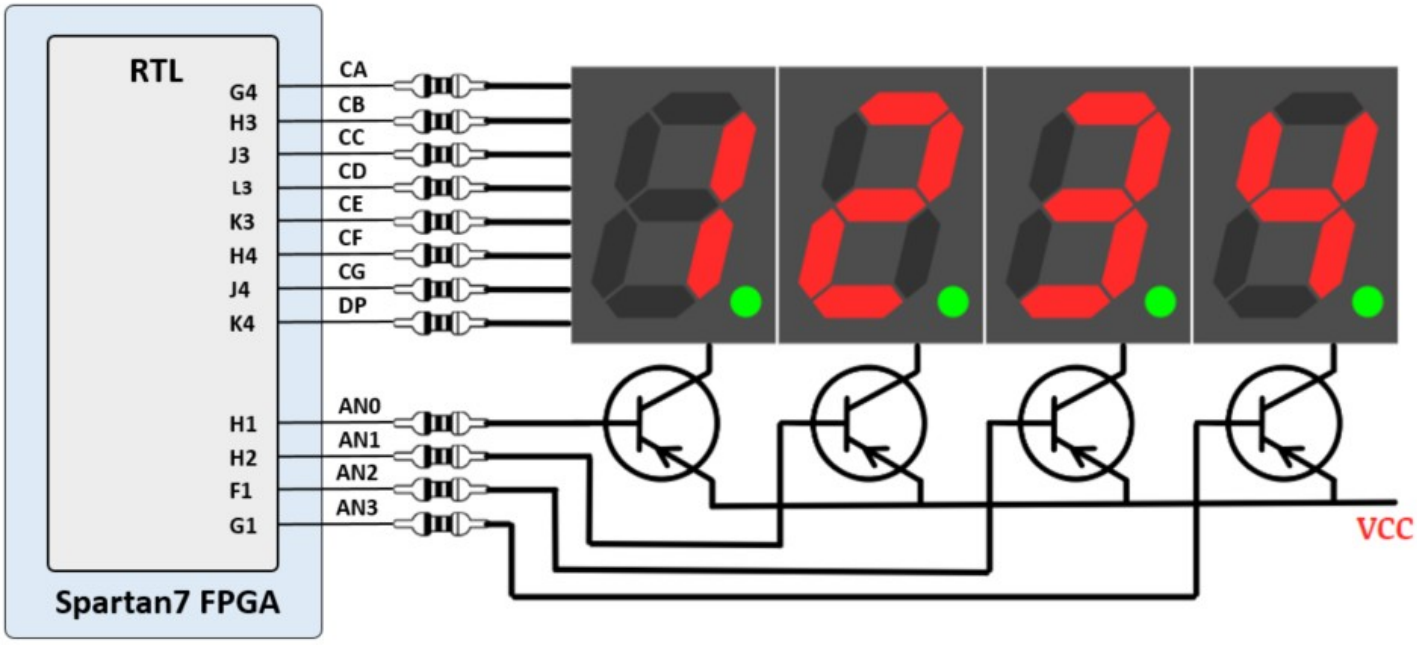


Push Button, Buzzer & RGB LED

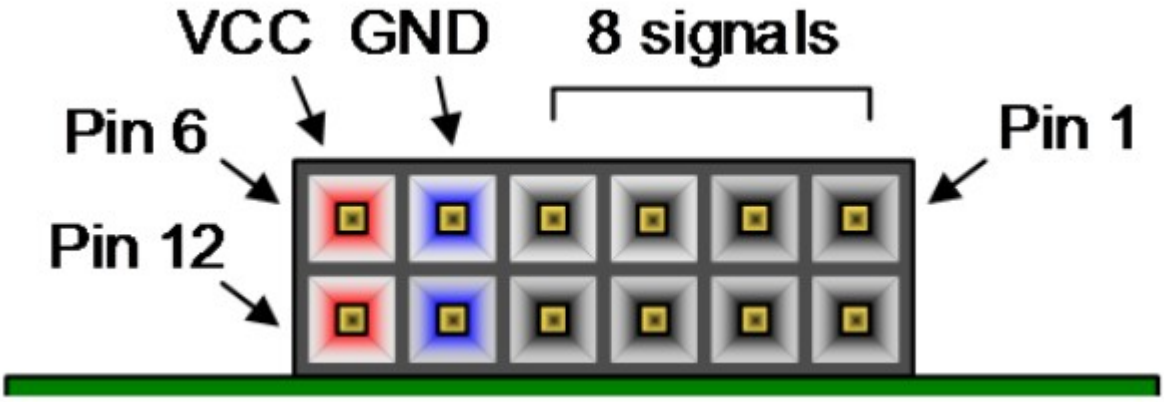


Seven Segment

The PINE Spartan7 FPGA board includes 4 common Anode seven segment display as show in following fig.



Pmod Ports



We have a large collection of Pmod (Peripheral Module) accessory boards that can attach to the expansion ports to add ready-made functions such as A/D's, D/A's, motor drivers, sensors, displays, and many other functions. These ports can be used as simple expansion ports, since all of the pin-outs correspond to pins on the FPGA.

The Pmod ports are arranged in a 2×6 right-angle, and are 100-mil female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod ports provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals. Pin assignments for the Pmod I/O connected to the FPGA are shown in the below table

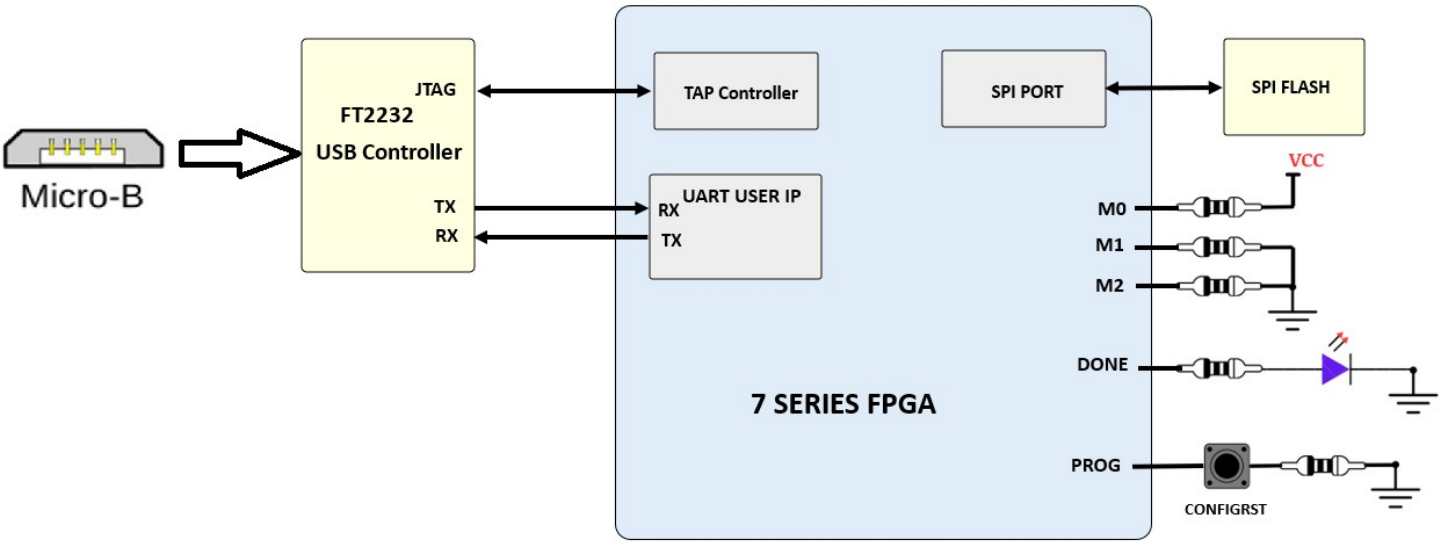
Warning: ***Since the Pmod pins are connected to Spartan-7 FPGA pins using a 3.3V logic standard, care should be taken not to drive these pins over 3.4V.***

Pmod JA	Pmod JB	Pmod JC	Pmod JD
JA1 :E2	JB1 :N1	JC1 :K11	JD1 :M11
JA2 :D2	JB2 :M1	JC2 :J13	JD2 :N14
JA3 :B1	JB3 :L1	JC3 :L13	JD3 :P12
JA4 :A2	JB4 :J1	JC4 :M13	JD4 :P11
JA7 :F2	JB7 :P2	JC7 :K12	JD7 :M12
JA8 :D1	JB8 :M2	JC8 :L12	JD8 :M10
JA9 :C1	JB9 :L2	JC9 :L14	JD9 :P13
JA10:B2	JB10:J2	JC10:M14	JD10:N11

FPGA Configuration

After power-on, the FPGA must be configured (or programmed) before it can perform any functions. You can configure the FPGA in one of the following ways:

1. A PC can use the USB-JTAG circuitry (port J15) to program the FPGA any time the power is on.
2. A file stored in the non-volatile serial (SPI) flash device can be transferred to the FPGA using the SPI port.



Above fig shows the different options available for configuring the FPGA. By default, on power on FPGA will be programmed by the Quad-SPI flash if it's programed with correct .bin file.

Bitstreams are stored in volatile memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

After being successfully programmed, the FPGA will cause the "DONE" LED to illuminate. Pressing the "PROG" button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from SPI flash, as we have fixed master spi mode.