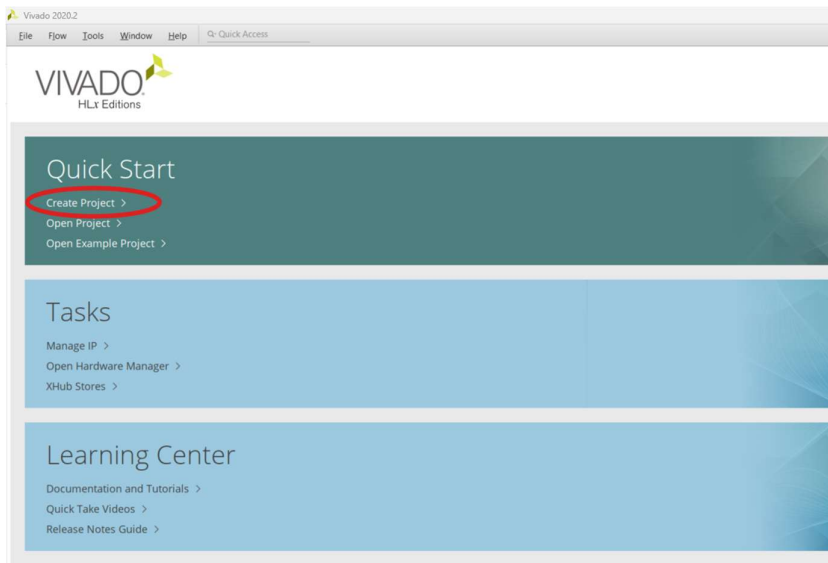



Getting started with Vivado design suite for PINE SPARTAN-7 FPGA Board



 **New Project**

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at: D:/project_EISLER_TEST

Project Type

Specify the type of project to create.

- ☒ **RTL Project**
You will be able to add sources, create block designs in the IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design.
- ☐ Do not specify sources at this time
- ☐ Project is an extensible Vitis platform
- ☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
- ☐ Do not specify sources at this time
- ☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- ☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- ☐ **Example Project**
Create a new Vivado project from a predefined template.

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.



Use Add Files, Add Directory

Add Files

- ☒ Scan and add RTL include files into project
- ☒ Copy sources into project
- ☒ Add sources from subdirectories

Target language: VHDL

Simulator language: Mixed

**Add Source Files**

Look in: TEST.SRCS

hex_seven_seg.vhd
SEVEN_SIGMENT.vhd

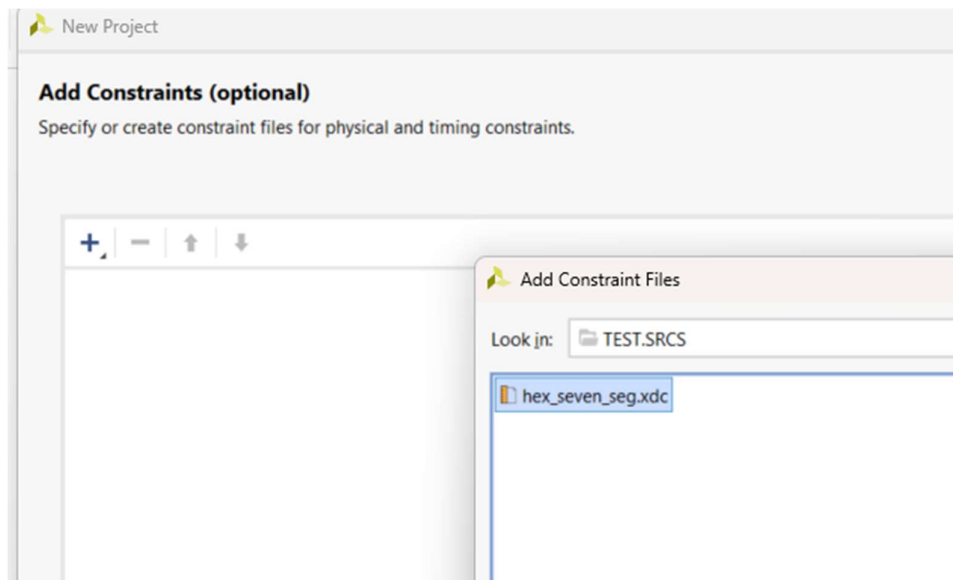
File name: "hex_seven_seg.vhd" "SEVEN_SIGMENT.vhd"

Files of type: Design Source Files (.vhd, vhdI, vhf, vhdP, vho, v, vf, verilog, vr, vg, vb, tf, t

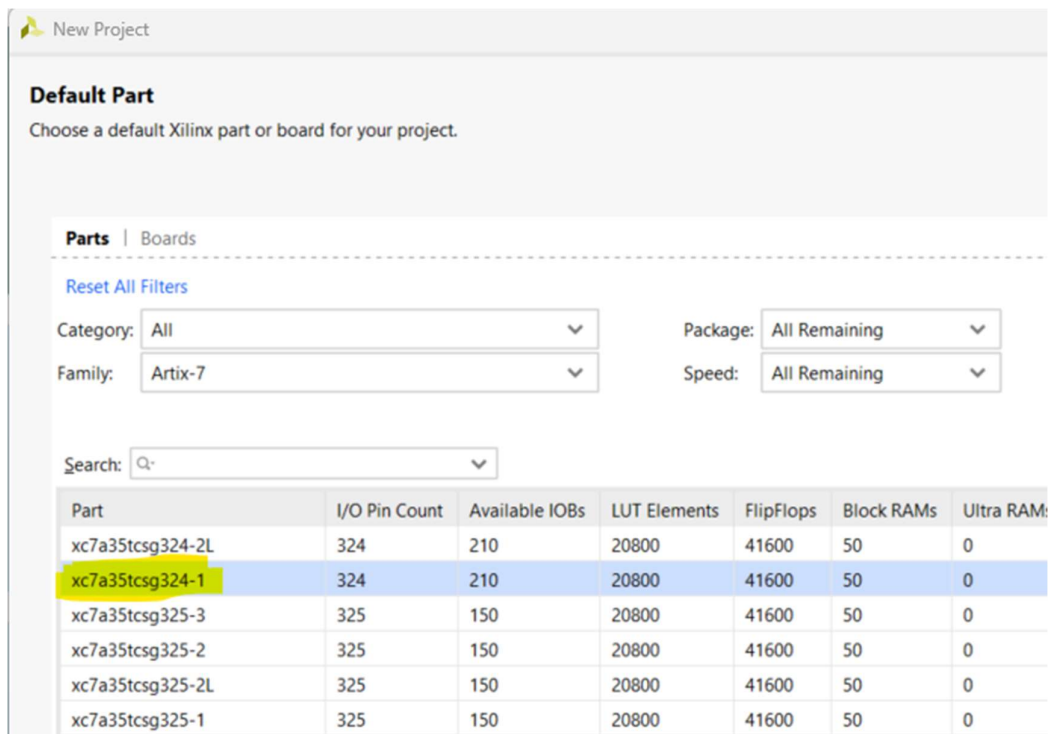
< Back

Next >

Finish



FOR EISLER ARTIX 7 FPGA BOARD



FOR PINE SPARTAN7 FPGA BOARD

[Reset All Filters](#)

Category:

Family:

Package:

Speed:

Search: (3 matches)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops
xc7s15ftgb196-1	196	100	8000	16000
xc7s15ftgb196-1IL	196	100	8000	16000
xc7s15ftgb196-1Q	196	100	8000	16000

FileEditFlowToolsReportsWindowLayoutViewHelp

Q Quick Access

Flow Navigator

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

PROJECT MANAGER - project_2

Sources

Design Sources (1)

hex_seven_seg(BEHAVIORAL) (hex_seven_seg.vhd) (1)

INST_SEVEN_SEGMENT : SEVEN_SEGMENT(BEHAVE) (SEVEN_SIGMENT.vhd)

Constraints (1)

constrs_1 (1)

hex_seven_seg.xdc

Simulation Sources (1)

Utility Sources

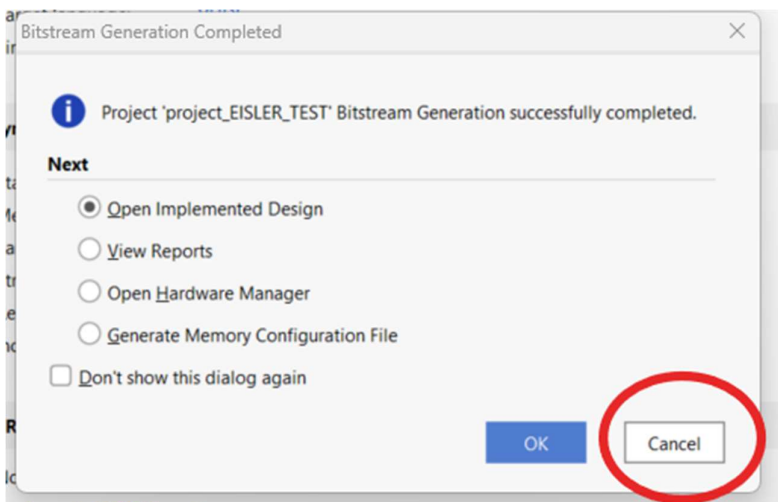
Hierarchy

Libraries

Compile Order

The screenshot displays the Xilinx Vivado IDE interface. On the left, the **PROJECT MANAGER** pane shows the project hierarchy. The **Sources** window lists the design sources, including **hex_seven_seg(BEHAVIORAL) (hex_seven_seg.vhd) (1)**. The **Source File Properties** window for **hex_seven_seg.vhd** shows it is enabled, located at **D:/project_2/project_2_srcs/sources_1/imports/TEST.SRCS**, with a type of **VHDL** and a library of **xil_defaultlib**. The **hex_seven_seg.vhd** code is shown in the editor, defining a 7-segment display driver. The **Design Runs** table at the bottom indicates that the synthesis and implementation runs have not yet started.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis
impl_1	constrs_1	Not started															Vivado Implementation



Open Hardware Manager

Make sure board is powered on & USB connector is connected to computer properly

- ▼ IMPLEMENTATION
 - ▶ Run Implementation
 - > Open Implemented Design

- ▼ PROGRAM AND DEBUG
 - Generate Bitstream
 - ▼ Open Hardware Manager
 - Open Target**
 - Program Device
 - Add Configuration Memory Device

Library: xil_defaultlib ...

Size: 1.9 KB

Modified: Today at 13:17:49 PM

Copied to: D:/project_FISLER_TEST

General Properties

Tcl Console Messages Log Rep

Name Constraints Status

✓ synth_1	constrs_1	synth_de
✓ impl_1	constrs_1	write_bit

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access

Flow Navigator

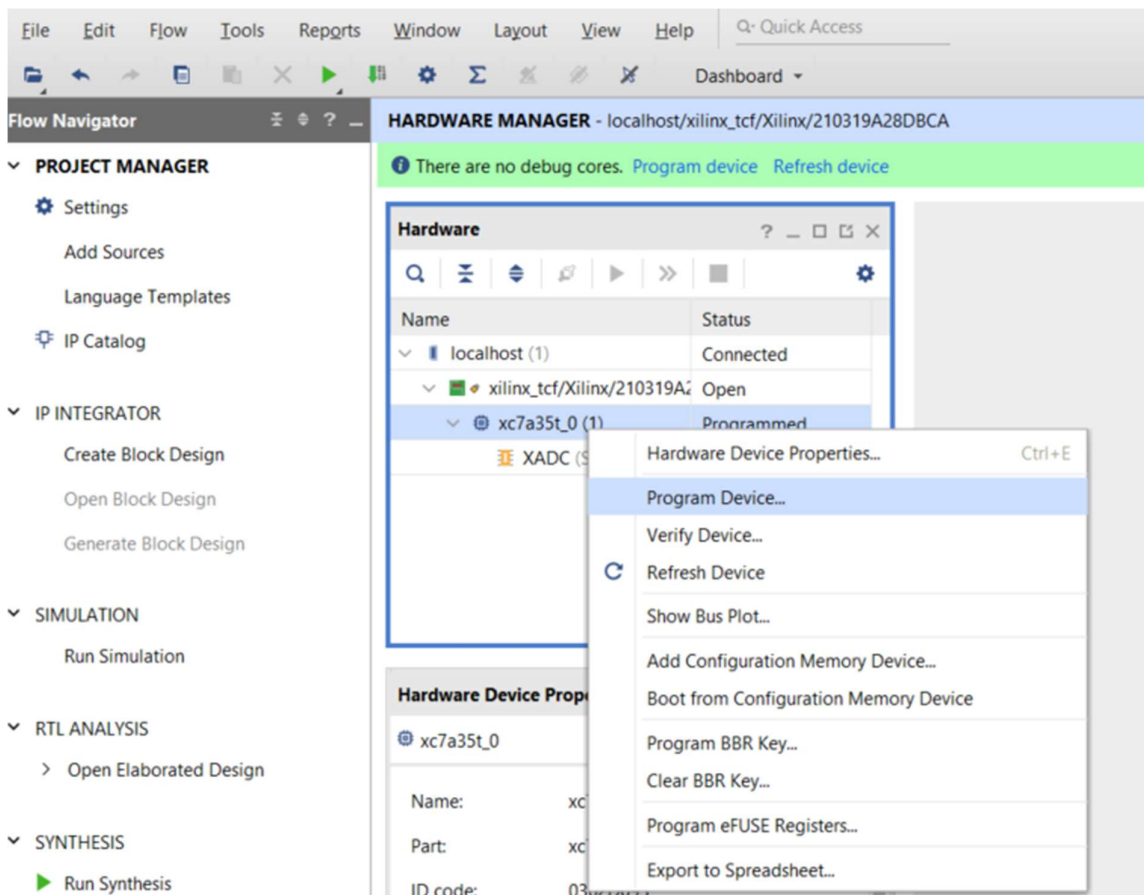
- ▼ PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- ▼ IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- ▼ SIMULATION

HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/210319A28DBCA

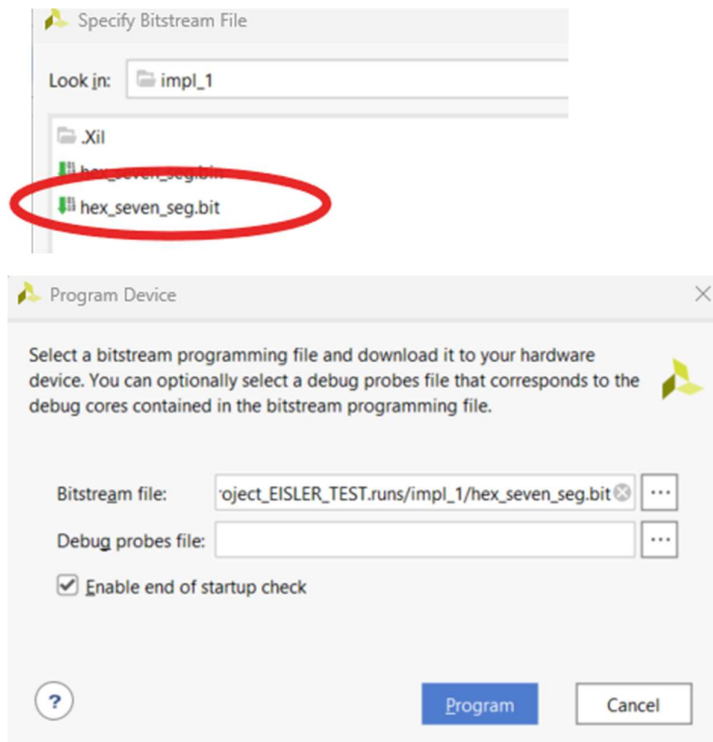
There are no debug cores. [Program device](#) [Refresh device](#)

Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/210319A2	Open
xc7a35t_0 (1)	Programmed
XADC (System Monit	



In runs/impl/ folder



Now check output on board

How To program flash attached to FPGA

The screenshot displays the Xilinx IDE interface. On the left, the 'IMPLEMENTATION' tab is active, showing options like 'Run Implementation' and 'Open Implemented Design'. Below it, the 'PROGRAM AND CONFIGURE' tab is selected, with 'Generate Bitstream' and 'Open Hardware Manager' visible. A yellow box highlights the 'Bitstream Settings...' button. The main window shows the 'Bitstream' settings panel, which is titled 'Specify various settings related to writing Bitstream'. A note states: 'Additional bitstream settings will be available once you open an implemented design.' Under the 'Write Bitstream (write_bitstream)' section, a table lists various options. The '-bin_file' option is highlighted with a red circle and has its checkbox checked. Below the table, the '-bin_file' section is expanded, showing the description: 'Write a binary bit file without header (.bin).'

Library: xil_defaultlib
Size: 1.9 KB
Modified: Today at 13:17:49 PM
Copied to: D:/project FISI ER TE

General Properties

Tcl Console Messages Log Run

Name Constraints Status

Project Settings

- General
- Simulation
- Elaboration
- Synthesis
- Implementation
- Bitstream**
- IP

Tool Settings

- Project
- IP Defaults
- XHub Store
- Source File
- Display
- WebTalk
- Help
- Text Editor
- 3rd Party Simulators
- Colors
- Selection Rules
- Shortcuts

Bitstream
Specify various settings related to writing Bitstream

Note: Additional bitstream settings will be available once you open an implemented design.

Write Bitstream (write_bitstream)

tcl.pre		...
tcl.post		...
-raw_bitfile	<input type="checkbox"/>	
-mask_file	<input type="checkbox"/>	
-no_binary_bitfile	<input type="checkbox"/>	
-bin_file	<input checked="" type="checkbox"/>	
-readback_file	<input type="checkbox"/>	
-logic_location_file	<input type="checkbox"/>	
-verbose	<input type="checkbox"/>	
More Options		

-bin_file
Write a binary bit file without header (.bin).

