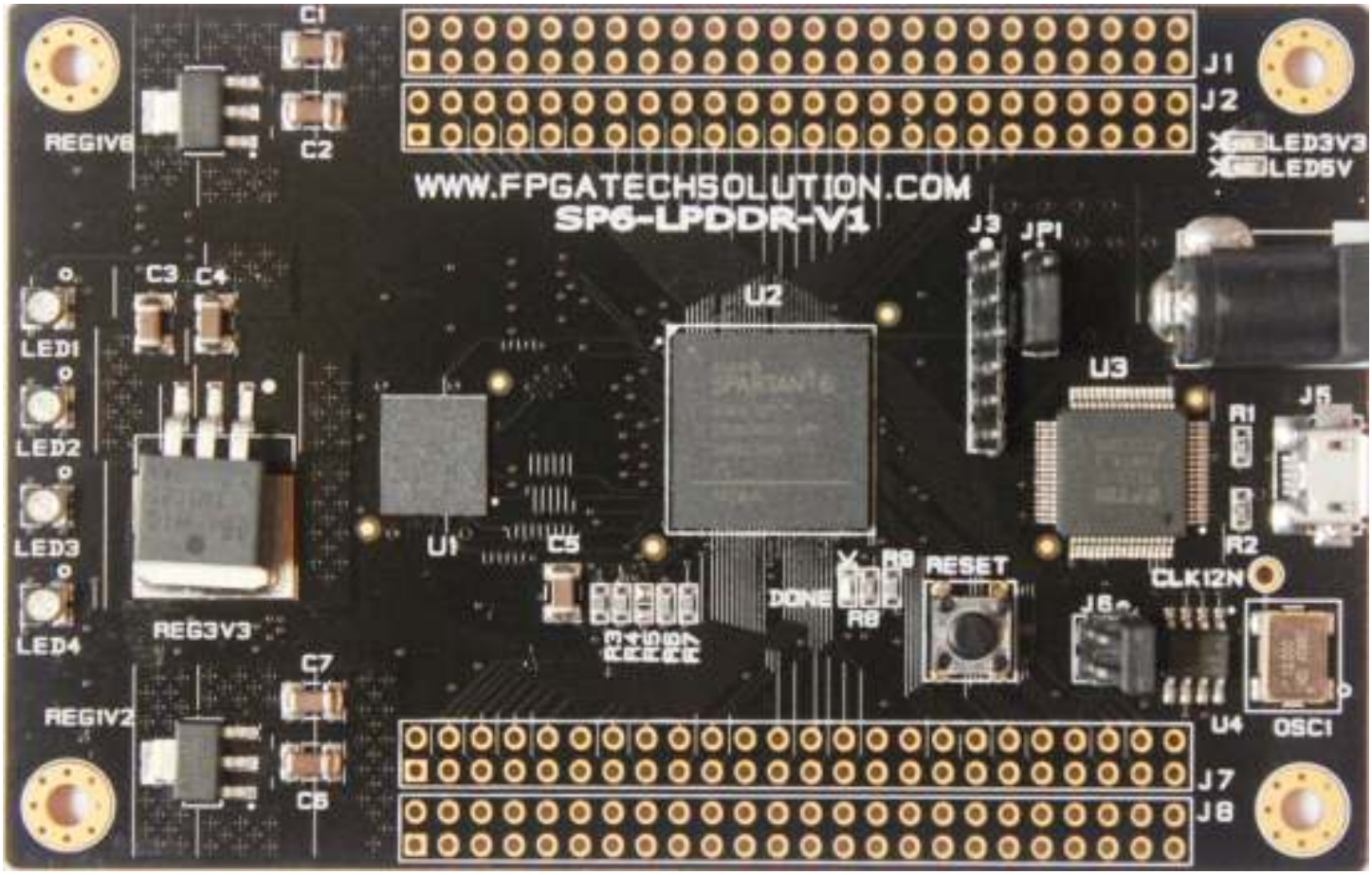
MANUAL SP6-LPDDR-V1

FPGA TECH SOLUTION

SOLUTION AHEAD



Introduction

SP6-LPDDR-V1 is an easy to use FPGA Development board featuring advance Xilinx Spartan-6 FPGA. This board is specially designed for experimenting and learning system design with FPGAs. This development board features Xilinx XC6SLX series FPGA with FTDI's FT2232HL Dual-Channel USB device. The high speed USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. No programmer or special downloader cable is needed to download the bit stream to the board.

Applications

- Product Prototype Development
- Development and testing of custom embedded processors
- Signal Processing
- Communication devices development
- Educational tool for Schools and Universities

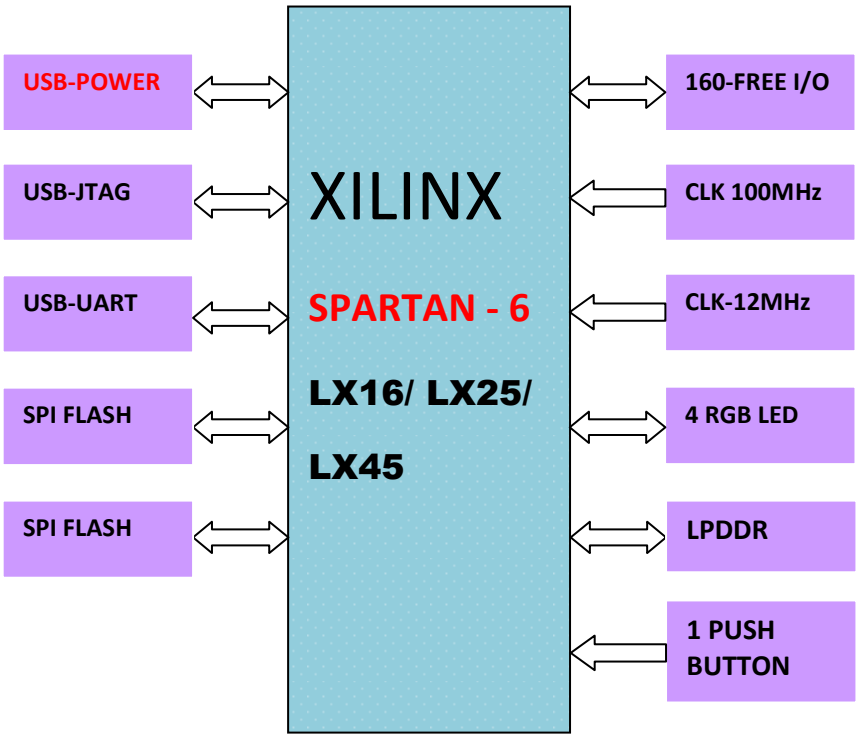
Key Features:

Spartan6-XC6SLX16/LX25/LX45

- **Up to 151 user-I/O pins**
- **CSG-324 package**

Key components:

- **Spartan6 FPGA**
- **LPDDR MT46H32M16LFBF**
- **OSCILLATOR – 12MHz**
- **OSCILLATOR – 100MHz**
- **FLASH – M25P80**
- **USB POWER**
- **On board USB JTAG**
- **USB to SERIAL / 8bit FIFO**
- **3 RGB – LED**
- **1 PUSH BUTTONS**
- **Size 87mm X 105mm**

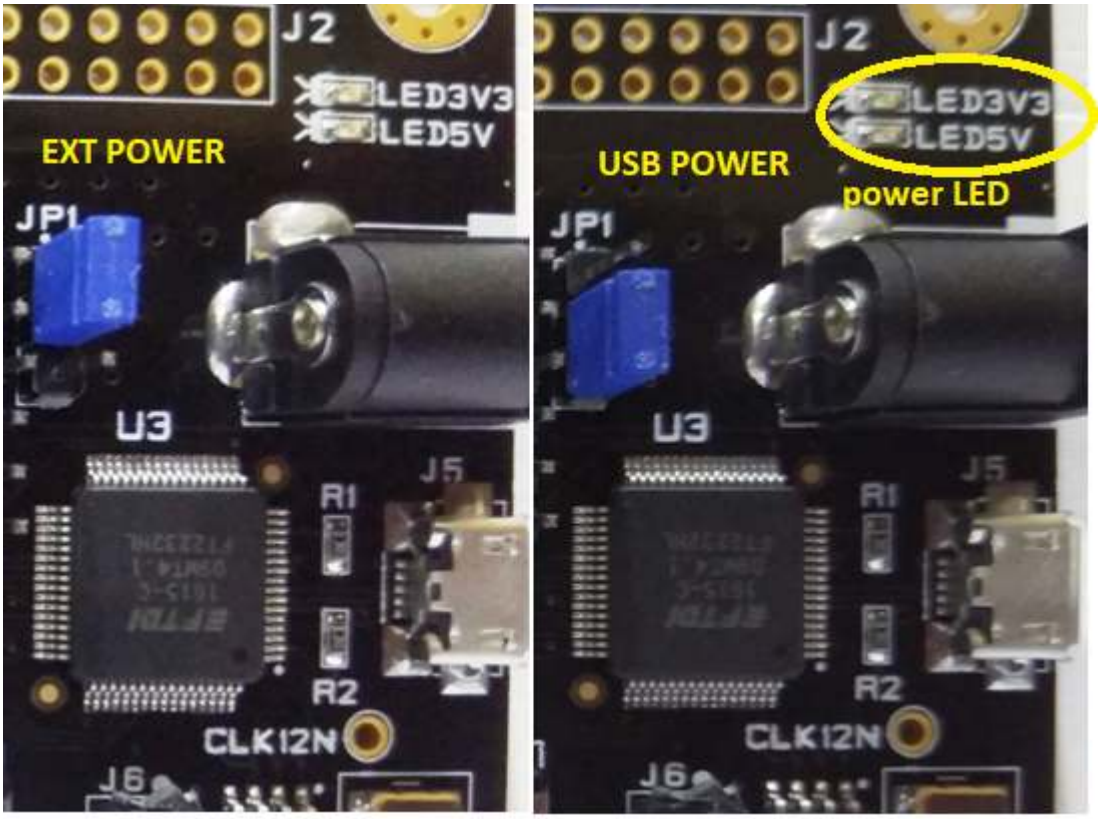


Note:

Max 151 user IO for LX16 FPGA
Max 145 user IO for LX25 FPGA
Max 137 user IO for LX45 FPGA
16Mb SPI flash is with LX45 only

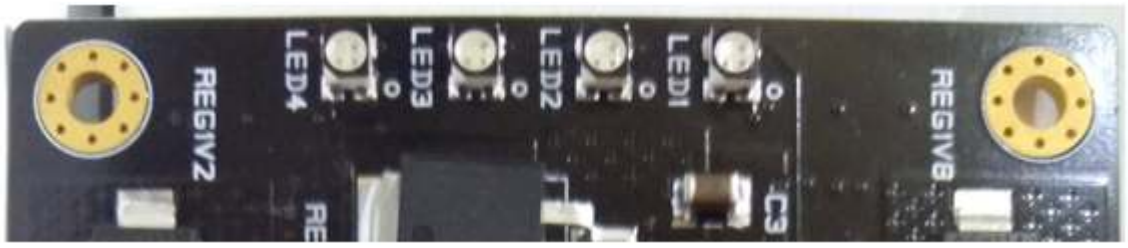
BOARD POWERING

The SP6-LPDDR-V1 uses +5V power supply to function properly. By default the board is configured to use +5V supply from USB. So an external +5V power is not required unless USB port is unable to supply enough current. In most cases USB ports are capable of providing enough current for the module. Current requirement for this board largely depends on your application. Please consult FPGA data sheet for more details on power requirements. If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly as shown below When JP1 jumper is placed towards USB as shown in below image power is used from USB connector & when JP1 jumper is placed towards power connector power is used from external connector



LED's Interface

The **SP6-LPDDR-V1** board has 3 individual RGB LED & 1 bicolor LED, A LED is assigned to each I/O to indicate its data status when I/O is configured as output.

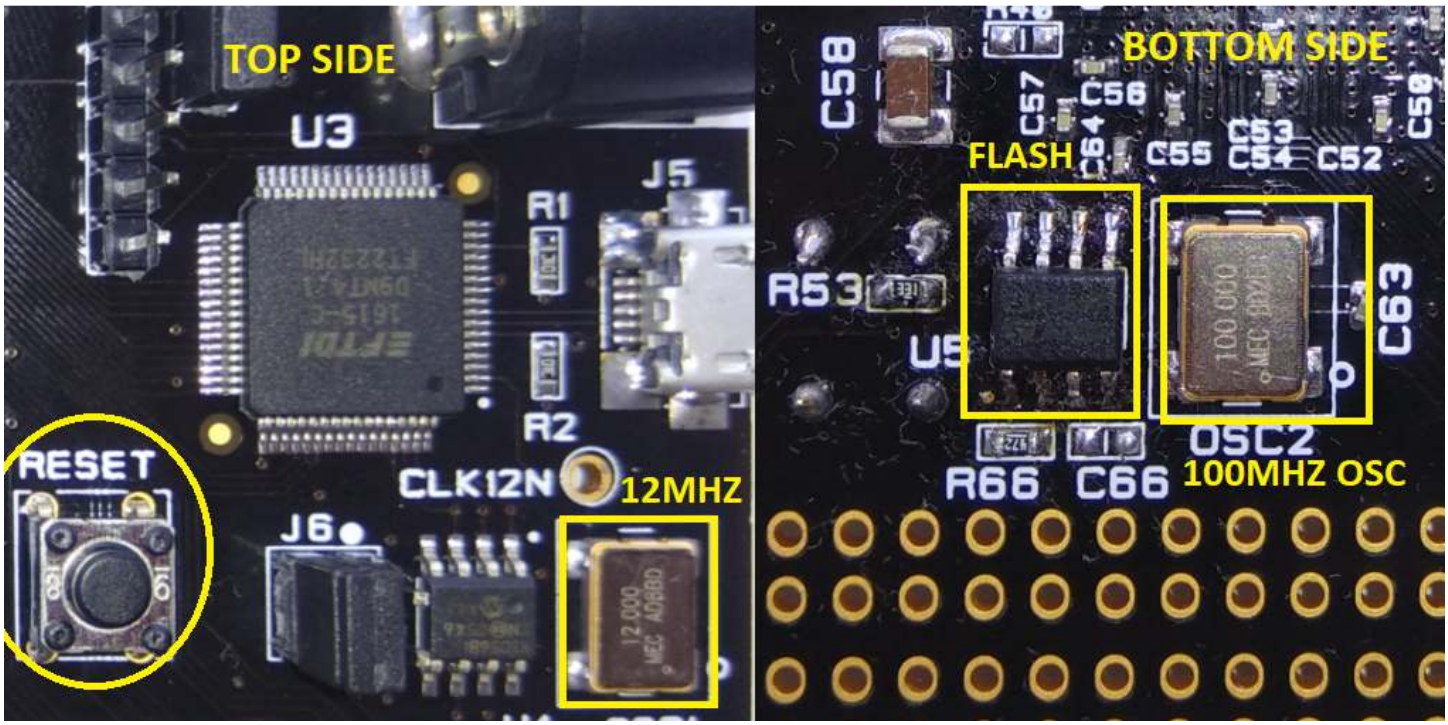


Pin Assignment (UCF Location):

```
NET "LED1_R"  LOC = L6  | IOSTANDARD = MOBILE_DDR;
NET "LED1_G"  LOC = M5 | IOSTANDARD = MOBILE_DDR;
NET "LED1_B"  LOC = P1  | IOSTANDARD = MOBILE_DDR;
NET "LED2_R"  LOC = E4  | IOSTANDARD = MOBILE_DDR;
NET "LED2_G"  LOC = C2  | IOSTANDARD = MOBILE_DDR ;
NET "LED2_B"  LOC = C1  | IOSTANDARD = MOBILE_DDR ;
NET "LED3_R"  LOC = P4  | IOSTANDARD = MOBILE_DDR;
NET "LED3_G"  LOC = P3  | IOSTANDARD = MOBILE_DDR ;
NET "LED3_B"  LOC = N3  | IOSTANDARD = MOBILE_DDR ;
NET "LED4_G"  LOC = P16  | IOSTANDARD = LVTTL;
NET "LED4_B" LOC = P15  | IOSTANDARD = LVTTL;
```

Clock Sources

The **SP6-LPDDR-V1** has clock input sources which are listed below.
The board includes an on-board 100MHz & 12MHz clock oscillator, 12MHz is on top side of PCB & 100MHz is on bottom side of PCB

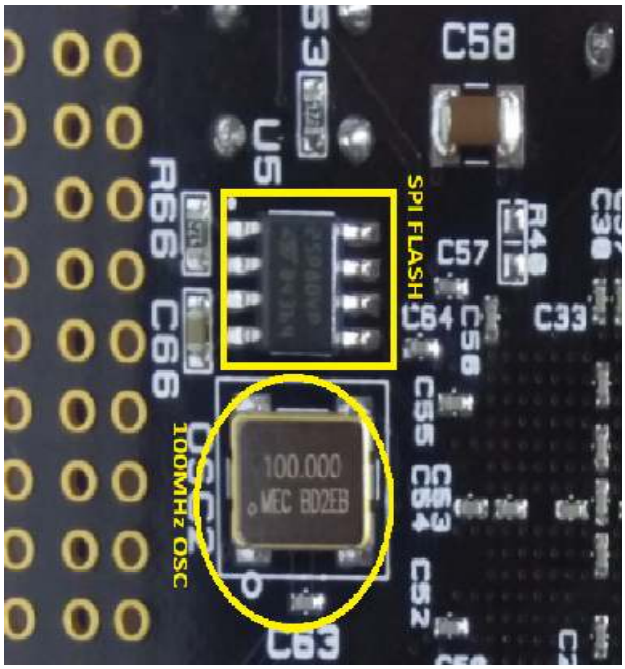


Pin Assignment (UCF Location):

```
NET "CLK_100MHZ" LOC = V10    | IOSTANDARD = LVTTL;
NET "CLK_12MHZ"   LOC  = H17   | IOSTANDARD = LVTTL;
NET "RESET"          LOC = U16    | IOSTANDARD = LVTTL;
```

SPI FLASH

The **SP6-LPDDR-V1** has on board spi flash Located at on bottom side of PCB
LX16 & lx25 fpga will have M25P80 flash and lx45 will have M25P16 flash

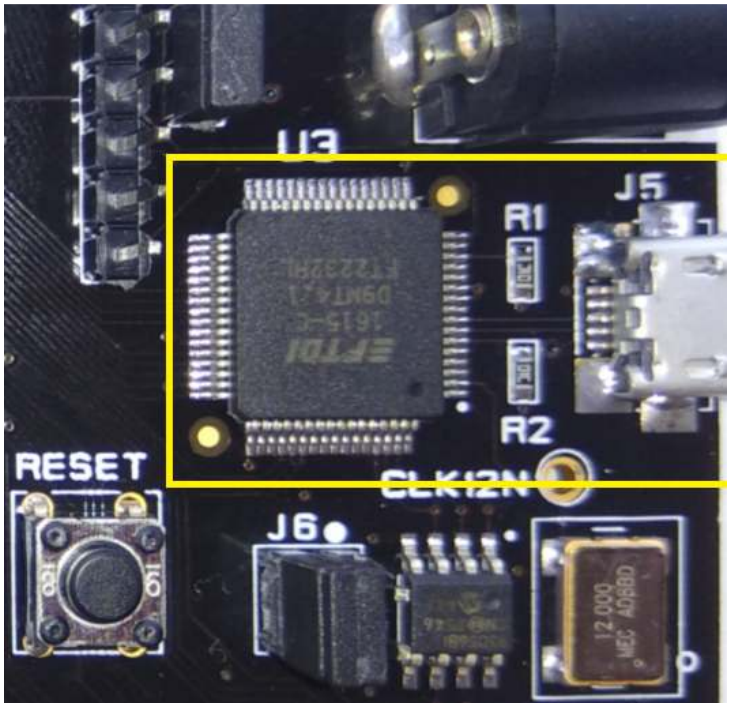


Pin Assignment (UCF Location):

```
NET "FLASH_CLOCK" LOC =R15 | IOSTANDARD = LVTTL ;
NET "FLASH_CS"    LOC =V3      | IOSTANDARD = LVTTL ;
NET "FLASH_MISO"  LOC =R13  | IOSTANDARD = LVTTL ;
NET "FLASH_MOSI"  LOC =T13  | IOSTANDARD = LVTTL ;
```

USB INTERFACE

The **SP6-LPDDR-V1** has advance High Speed USB 2.0 interface, FT2232H Channel A is dedicated for FPGA & SPI Flash Programming. Channel B can be used for custom applications like UART, 8bit FIFO

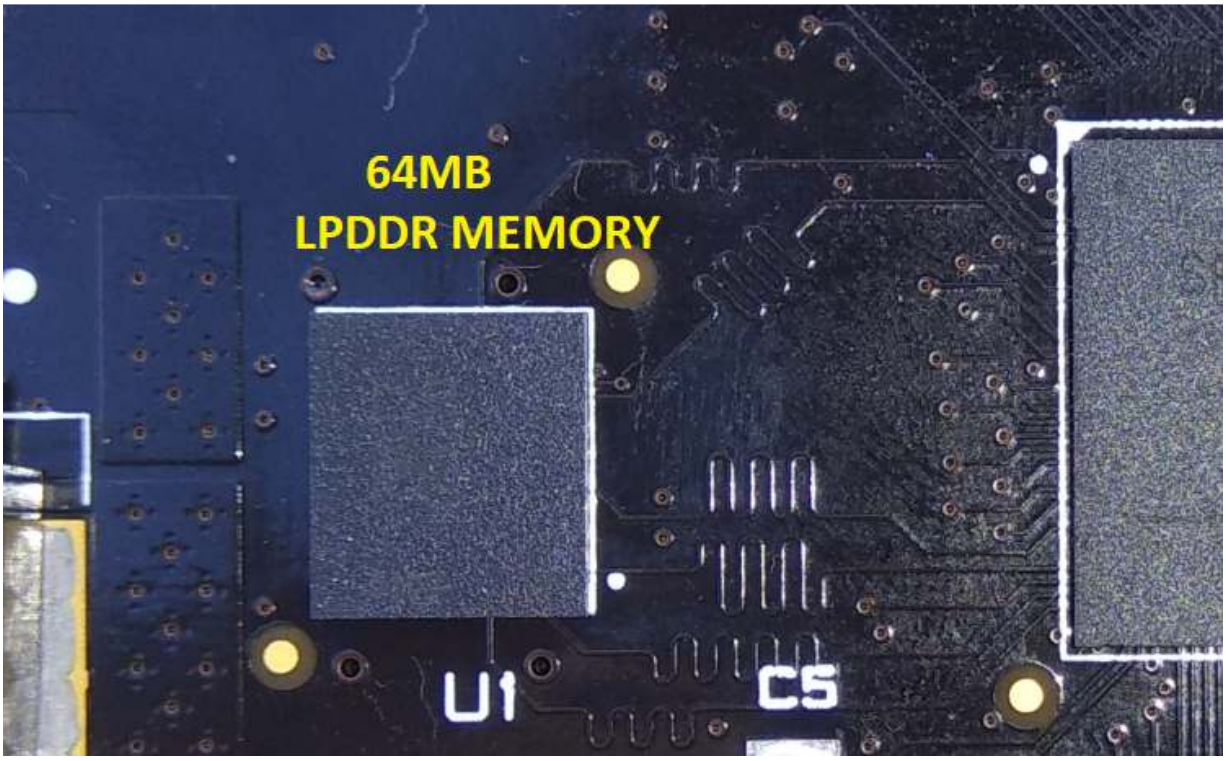


Pin connection of LPDDR & FPGA given below

```
NET "USB_DATA[0]" LOC =C17 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[1]" LOC =C18 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[2]" LOC =D17 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[3]" LOC =D18 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[4]" LOC =E16 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[5]" LOC =E18 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[6]" LOC =F17 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_DATA[7]" LOC =F18 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_WR"      LOC =K17 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_RD"      LOC =K18 | IOSTANDARD = LVTTL | SLEW = FAST | DRIVE = 8 ;
NET "USB_RXF"     LOC =H18 | IOSTANDARD = LVTTL| SLEW = FAST | DRIVE = 8  ;
NET "USB_TXE"     LOC =J18 | IOSTANDARD = LVTTL| SLEW = FAST | DRIVE = 8  ;
```

LPDDR INTERFACE

The **SP6-LPDDR-V1** has advance High Speed 64MB LPDDR memory **MT46H32M16LFBF**



Pin connection of LPDDR & FPGA given below

```
NET  "MCB_DDR3_DRAM_ADDR[0]" LOC = "J7"  | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[1]" LOC = "J6"  | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[2]" LOC = "H5" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[3]" LOC = "L7"  | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[4]" LOC = "F3"  | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[5]" LOC = "H4" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[6]" LOC = "H3" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[7]" LOC = "H6" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[8]" LOC = "D2" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[9]" LOC = "D1" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[10]"LOC = "F4" | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[11]"LOC = "D3"| IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_ADDR[12]"LOC = "G6"| IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_DQ[0]"   LOC = "L2"   | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_DQ[1]"   LOC = "L1"  | IOSTANDARD = MOBILE_DDR;
NET  "MCB_DDR3_DRAM_DQ[2]"   LOC = "K2"  | IOSTANDARD = MOBILE_DDR;
```

```
NET "MCB_DDR3_DRAM_DQ[3]"   LOC = "K1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[4]"   LOC = "H2"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[5]"   LOC = "H1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[6]"   LOC = "J3"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[7]"   LOC = "J1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[8]"   LOC = "M3"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[9]"   LOC = "M1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[10]"  LOC = "N2"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[11]"  LOC = "N1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[12]"  LOC = "T2"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[13]"  LOC = "T1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[14]"  LOC = "U2"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQ[15]"  LOC = "U1"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_BA[0]"   LOC = "F2"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_BA[1]"   LOC = "F1"  | IOSTANDARD = MOBILE_DDR;

NET "MCB_DDR3_DRAM_RAS_N"   LOC = "L5"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_CAS_N"   LOC = "K5"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_WE_N"    LOC = "E3"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_CLK"     LOC = "G3"  | IOSTANDARD = DIFF_MOBILE_DDR;
NET "MCB_DDR3_DRAM_CLK_N"   LOC = "G1" | IOSTANDARD = DIFF_MOBILE_DDR;
NET "MCB_DDR3_DRAM_CKE"     LOC = "H7"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_LDM"     LOC = "K3"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_DQS"     LOC = "L4"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_UDM"     LOC = "K4"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_DRAM_UDQS"    LOC = "P2"  | IOSTANDARD = MOBILE_DDR;
NET "MCB_DDR3_RZQ"          LOC = "N4"  | IOSTANDARD = MOBILE_DDR;
NET "CALIB_DONE"    LOC = "K13"  | IOSTANDARD = LVCMOS33;
NET "ERROR"         LOC = "K12"  | IOSTANDARD = LVCMOS33;
```

FREE INPUT OUTPUT

The **SP6-LPDDR-V1** board has max 151 user I/O placed four input output connectors.

All pin can work with maximum 3.3V DC

Max 151 user IO for LX16 FPGA
Max 145 user IO for LX25 FPGA
Max 137 user IO for LX45 FPGA

Pin connection of J1 & FPGA given below

J1					
J1_1	**5V**		J1_25	J1_IO_N_<11>	F9
J1_2	**5V**		J1_26	J1_IO_P_<11>	G9
J1_3	J1_IO_N_<1>	C6	J1_27	J1_IO_N_<12>	F10
J1_4	J1_IO_P_<1>	D6	J1_28	J1_IO_P_<12>	G11
J1_5	J1_IO_N_<2>	C8	J1_29	J1_IO_N_<13>	E11
J1_6	J1_IO_P_<2>	D8	J1_30	J1_IO_P_<13>	F11
J1_7	J1_IO_N_<3>	C9	J1_31	**GND**	
J1_8	J1_IO_P_<3>	D9	J1_32	**GND**	
J1_9	J1_IO_N_<4>	C11	J1_33	J1_IO_N_<14>	F16
J1_10	J1_IO_P_<4>	D11	J1_34	J1_IO_P_<14>	F15
J1_11	J1_EXTRA_IO_<1>	V16	J1_35	J1_IO_N_<15>	G18
J1_12	J1_EXTRA_IO_<2>	C4	J1_36	J1_IO_P_<15>	G16
J1_13	J1_IO_N_<5>	C12	J1_37	J1_IO_N_<16>	H16
J1_14	J1_IO_P_<6>	D12	J1_38	J1_IO_P_<16>	H15
J1_15	J1_IO_N_<6>	C14	J1_39	J1_IO_N_<17>	E12
J1_16	J1_IO_P_<7>	D14	J1_40	J1_IO_P_<17>	F12
J1_17	J1_IO_N_<7>	E6	J1_41	**GND**	
J1_18	J1_IO_P_<8>	F7	J1_42	**GND**	
J1_19	J1_IO_N_<8>	E8	J1_43	J1_IO_N_<18>	E13
J1_20	J1_IO_P_<9>	E7	J1_44	J1_IO_P_<18>	F13
J1_21	**GND**		J1_45	J1_IO_N_<19>	G14
J1_22	**GND**		J1_46	J1_IO_P_<19>	F14
J1_23	J1_IO_N_<10>	F8	J1_47	**3.3V**	
J1_24	J1_IO_P_<10>	G8	J1_48	**3.3V**	

Pin connection of J2 & FPGA given below

J2					
J2_1	**5V**		J2_25	J2_IO_N_<11>	A11
J2_2	**5V**		J2_26	J2_IO_P_<11>	B11
J2_3	J2_IO_N_<1>	A2	J2_27	J2_IO_N_<12>	A12
J2_4	J2_IO_P_<1>	B2	J2_28	J2_IO_P_<12>	B12
J2_5	J2_IO_N_<2>	A3	J2_29	J2_IO_N_<13>	A13
J2_6	J2_IO_P_<2>	B3	J2_30	J2_IO_P_<13>	C13
J2_7	J2_IO_N_<3>	A4	J2_31	**GND**	
J2_8	J2_IO_P_<3>	B4	J2_32	**GND**	
J2_9	J2_IO_N_<4>	A5	J2_33	J2_IO_N_<14>	A14
J2_10	J2_IO_P_<4>	C5	J2_34	J2_IO_P_<14>	B14
J2_11	J2_EXTRA_IO_<1>	P12	J2_35	J2_IO_N_<15>	A15
J2_12	J2_EXTRA_IO_<2>	J16	J2_36	J2_IO_P_<15>	C15
J2_13	J2_IO_N_<6>	A6	J2_37	J2_IO_N_<16>	A16
J2_14	J2_IO_P_<6>	B6	J2_38	J2_IO_P_<16>	B16
J2_15	J2_IO_N_<7>	A7	J2_39	J2_IO_N_<17>	K16
J2_16	J2_IO_P_<7>	C7	J2_40	J2_IO_P_<17>	K15
J2_17	J2_IO_N_<8>	A8	J2_41	**GND**	
J2_18	J2_IO_P_<8>	B8	J2_42	**GND**	
J2_19	J2_IO_N_<9>	A9	J2_43	J2_IO_N_<18>	L16
J2_20	J2_IO_P_<9>	B9	J2_44	J2_IO_P_<18>	L15
J2_21	**GND**		J2_45	J2_IO_N_<19>	N16
J2_22	**GND**		J2_46	J2_IO_P_<19>	N15
J2_23	J2_IO_N_<10>	A10	J2_47	**3.3V**	
J2_24	J2_IO_P_<10>	C10	J2_48	**3.3V**	

Pin connection of J7 & FPGA given below

J7					
J7_1	**3.3V**		J7_25	J7_IO_N_<10>	V14
J7_2	**3.3V**		J7_26	J7_IO_P_<10>	T14
J7_3	J7_IO_N_<1>	V4	J7_27	J7_IO_N_<11>	V15
J7_4	J7_IO_P_<1>	T4	J7_28	J7_IO_P_<11>	U15
J7_5	J7_IO_N_<2>	V5	J7_29	J7_IO_N_<12>	N11
J7_6	J7_IO_P_<2>	U5	J7_30	J7_IO_P_<12>	M11
J7_7	J7_IO_N_<3>	V6	J7_31	**GND**	
J7_8	J7_IO_P_<3>	T6	J7_32	**GND**	
J7_9	J7_IO_N_<4>	V7	J7_33	J7_IO_N_<13>	U18
J7_10	J7_IO_P_<4>	U7	J7_34	J7_IO_P_<13>	U17
J7_11	J7_EXTRA_IO_<1>	R5	J7_35	J7_IO_N_<14>	T18
J7_12	INT	U3	J7_36	J7_IO_P_<14>	T17
J7_13	J7_IO_N_<5>	V8	J7_37	J7_IO_N_<15>	P18
J7_14	J7_IO_P_<5>	U8	J7_38	J7_IO_P_<15>	P17
J7_15	J7_IO_N_<6>	V9	J7_39	J7_IO_N_<16>	N18
J7_16	J7_IO_P_<6>	T9	J7_40	J7_IO_P_<16>	N17
J7_17	J7_IO_N_<7>	V11	J7_41	**GND**	
J7_18	J7_IO_P_<7>	U11	J7_42	**GND**	
J7_19	J7_IO_N_<8>	V12	J7_43	J7_IO_N_<17>	M18
J7_20	J7_IO_P_<8>	T12	J7_44	J7_IO_P_<17>	M16
J7_21	**GND**		J7_45	J7_IO_N_<18>	L18
J7_22	**GND**		J7_46	J7_IO_P_<18>	L17
J7_23	J7_IO_N_<9>	V13	J7_47	**3.3V**	
J7_24	J7_IO_P_<9>	U13	J7_48	**3.3V**	

Pin connection of J8 & FPGA given below

J8					
J8_1	**3.3V**		J8_25	J8_IO_N_<11>	N9
J8_2	**3.3V**		J8_26	J8_IO_P_<11>	M10
J8_3	J8_IO_N_<1>	T3	J8_27	J8_IO_N_<12>	P11
J8_4	J8_IO_P_<1>	R3	J8_28	J8_IO_P_<12>	N10
J8_5	J8_IO_N_<2>	T7	J8_29	J8_IO_N_<13>	L13
J8_6	J8_IO_P_<2>	R7	J8_30	J8_IO_P_<13>	L12
J8_7	J8_IO_N_<3>	T8	J8_31	**GND**	
J8_8	J8_IO_P_<3>	R8	J8_32	**GND**	
J8_9	J8_IO_N_<4>	T10	J8_33	J8_IO_N_<14>	N14
J8_10	J8_IO_P_<4>	R10	J8_34	J8_IO_P_<14>	M14
J8_11	J8_EXTRA_IO_<1>	U10	J8_35	J8_IO_N_<15>	M13
J8_12	PROG	V2	J8_36	J8_IO_P_<15>	L14
J8_13	J8_IO_N_<6>	T11	J8_37	J8_IO_N_<16>	K13
J8_14	J8_IO_P_<6>	R11	J8_38	J8_IO_P_<16>	K12
J8_15	J8_IO_N_<7>	P6	J8_39	J8_IO_N_<17>	K14
J8_16	J8_IO_P_<7>	N5	J8_40	J8_IO_P_<17>	J13
J8_17	J8_IO_N_<8>	P7	J8_41	**GND**	
J8_18	J8_IO_P_<8>	N6	J8_42	**GND**	
J8_19	J8_IO_N_<9>	P8	J8_43	J8_IO_N_<18>	H14
J8_20	J8_IO_P_<9>	N7	J8_44	J8_IO_P_<18>	H13
J8_21	**GND**		J8_45	J8_IO_N_<19>	G13
J8_22	**GND**		J8_46	J8_IO_P_<19>	H12
J8_23	J8_IO_N_<10>	N8	J8_47	**3.3V**	
J8_24	J8_IO_P_<10>	M8	J8_48	**3.3V**	

Following pins are not available for LX45 FPGA

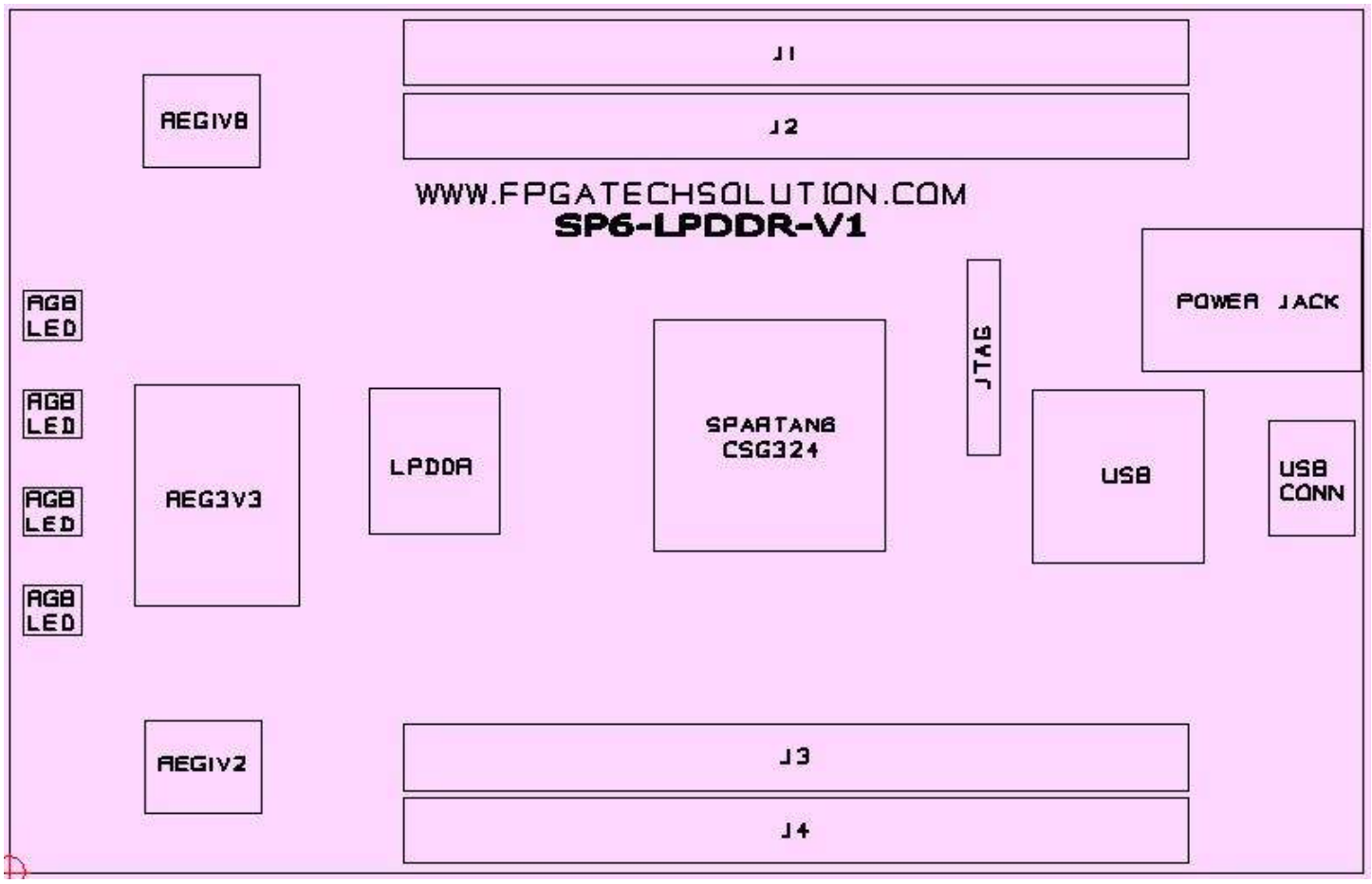
Hence Max 137 user IO for LX45 FPGA

J1_13	LX45	C12
J1_14	LX45	D12
J1_17	LX45	E6
J1_18	LX45	F7
J1_19	LX45	E8
J1_20	LX45	E7
J1_23	LX45	F8
J1_24	LX45	G8
J1_27	LX45	F10
J1_28	LX45	G11
J1_29	LX45	E11
J1_30	LX45	F11
J1_39	LX45	E12
J1_40	LX45	F12

Following pins are not available for LX25 FPGA

Max 145 user IO for LX25 FPGA

J1_17	LX25	E6
J1_18	LX25	F7
J1_19	LX25	E8
J1_20	LX25	E7
J1_23	LX25	F8
J1_24	LX25	G8



All sources code can be download from following link

https://github.com/fpgatechsolution/Spartan6_LPDDR