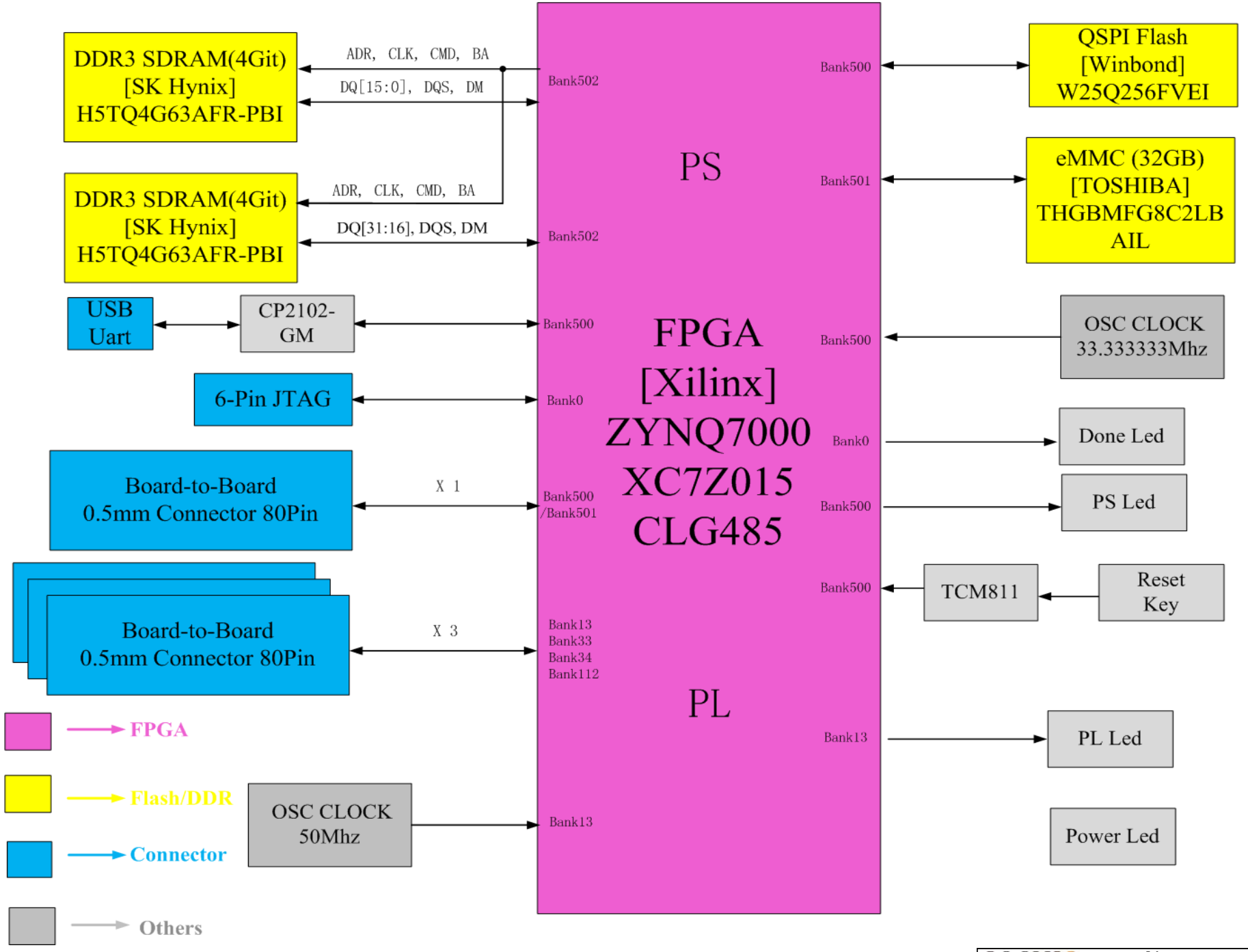

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Title	AC7015 BLOCK DIGRAM
Size	
Document Number	AC7015核心板 Schematics
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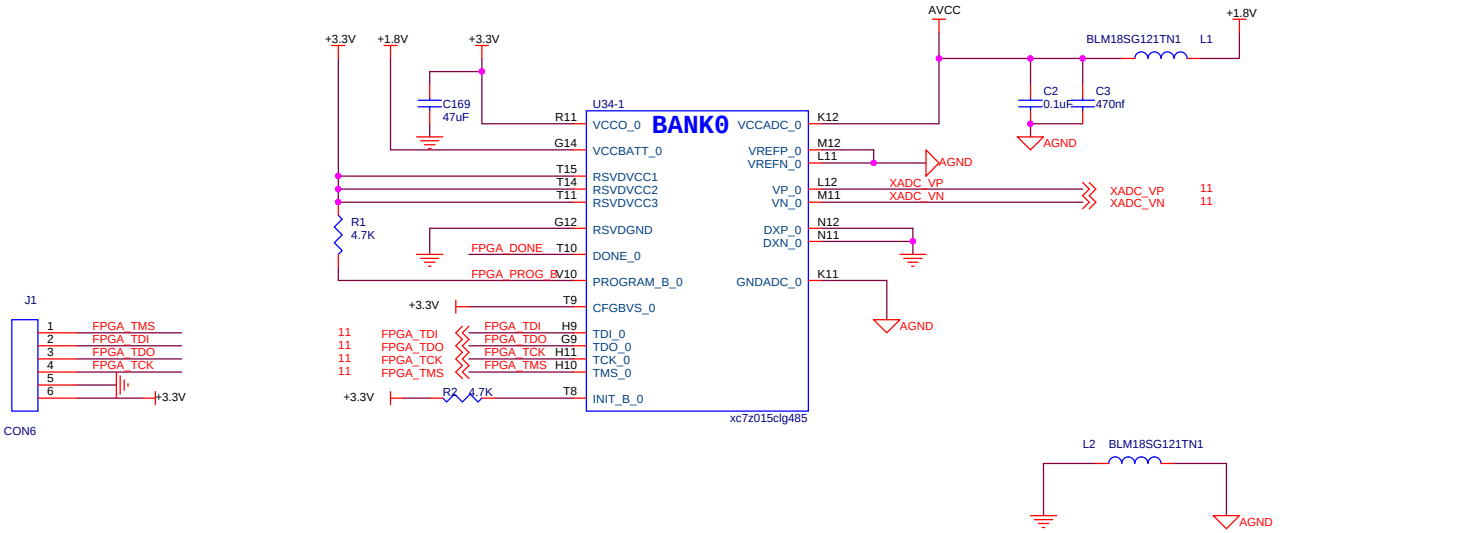

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Title	AC7015 Bank0
Size	Document Number: AC7015核心板 Schematics — Rev: 1.0
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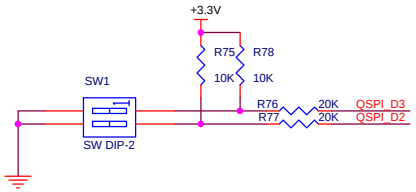
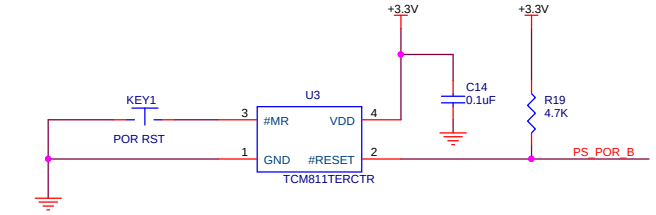
BOOT OPTION

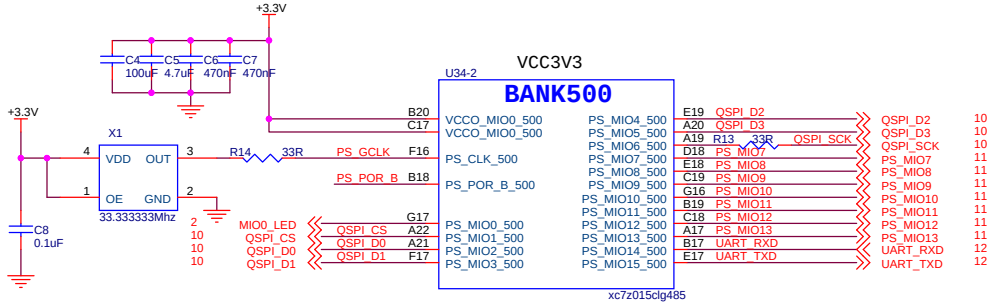
MIO[8] =1 ----MIO bank1 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V

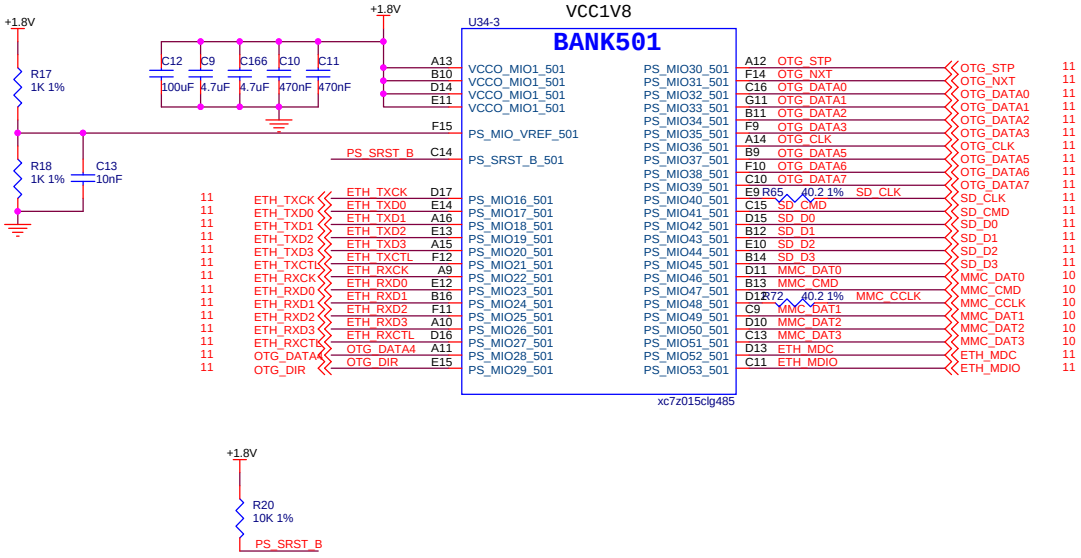


Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET







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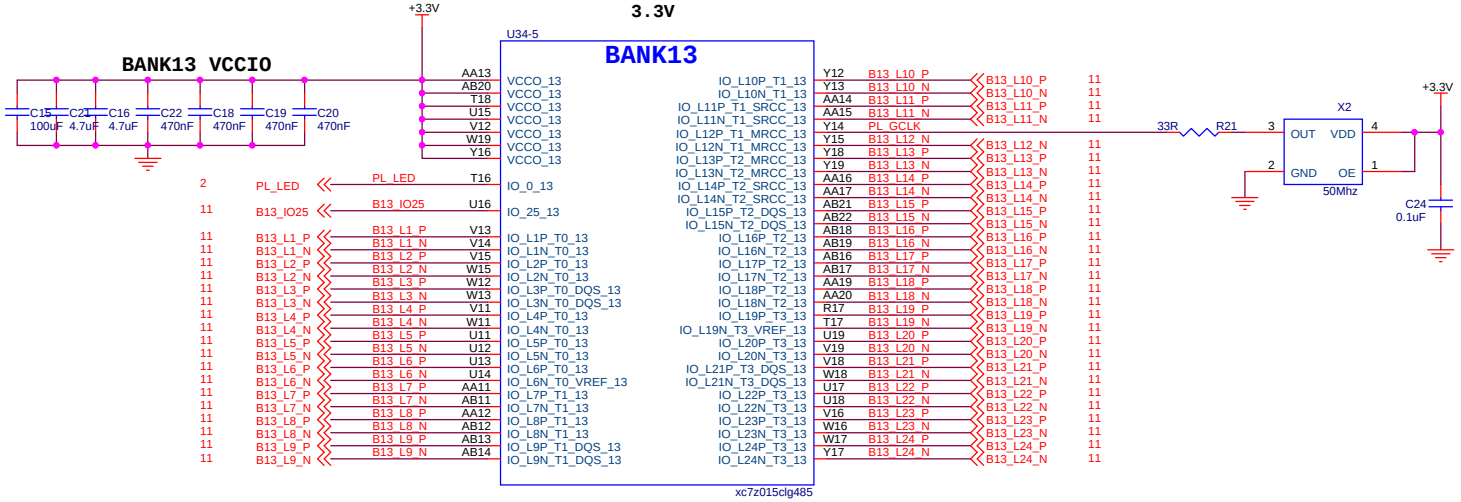
ALINX	www.alinx.com	
Title	AC7015 Bank500 & 501	
Size	Document Number: AC7015核心板 Schematics	Rev: 1.0
Date: Thursday, September 26, 2019	Sheet 3 of 12	



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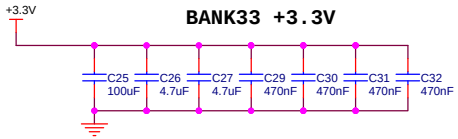
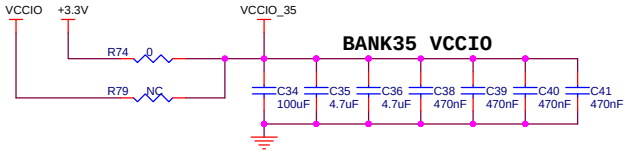
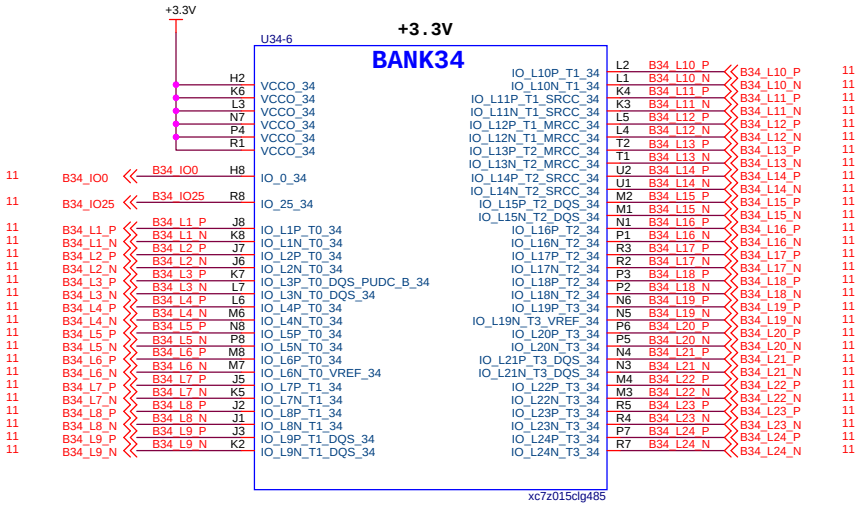
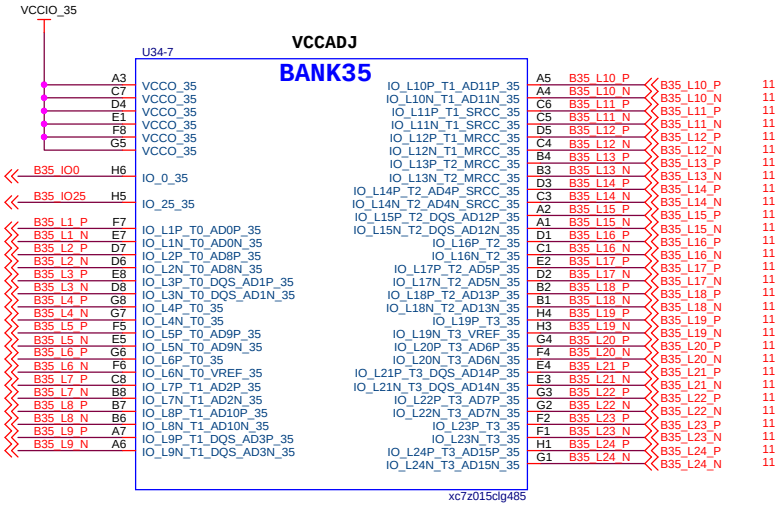
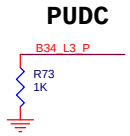
Title	AC7015 Bank13	
Size	Document Number: AC7015核心板 Schematics	Rev: 1.0
Date: Thursday, September 26, 2019	Sheet 4 of 12	











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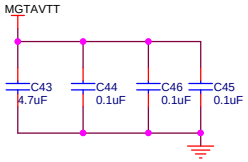
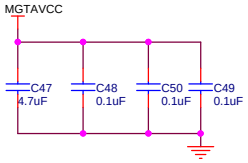
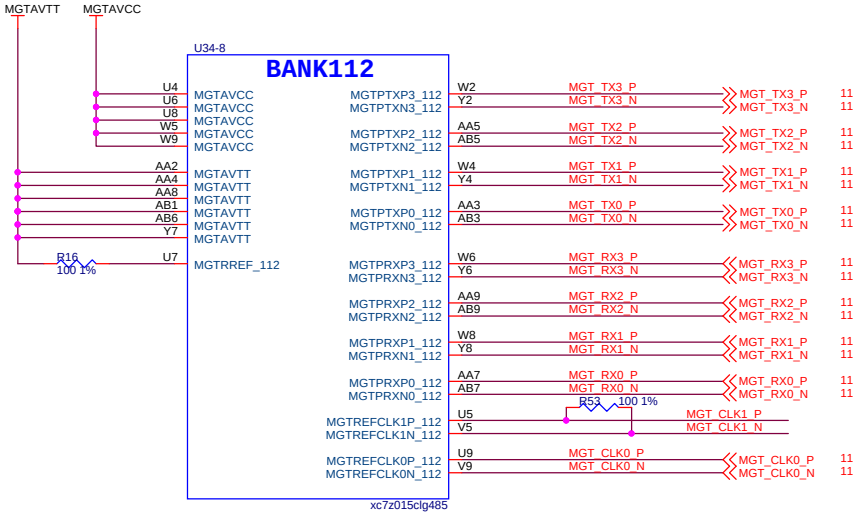
Title: AC7015 Bank34 & 35		
Size	Document Number: AC7015核心板 Schematics	Rev: 1.0
Date: Thursday, September 26, 2019	Sheet 5 of 12	

MGTAVTT 4.7uF(1) 0.1uF(2)



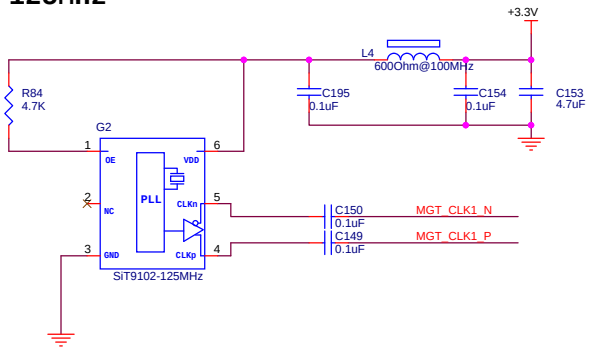
MGTAVCC 4.7uF(1) 0.1uF(2)



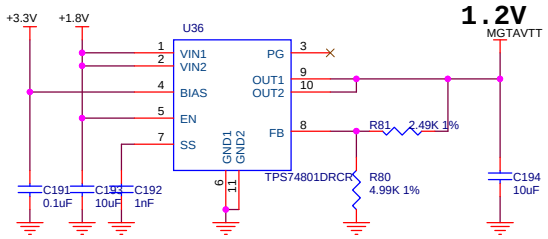


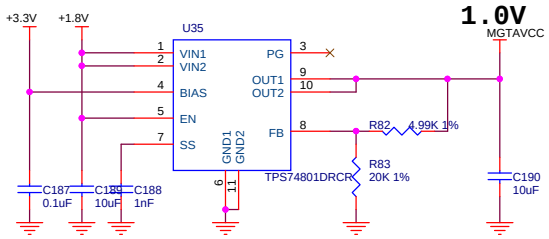
GTP CLOCK

125MHz



POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)





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Size	Document Number: AC7015核心板 Schematics	Rev: 1.0
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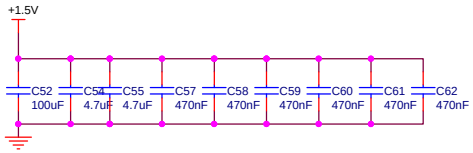

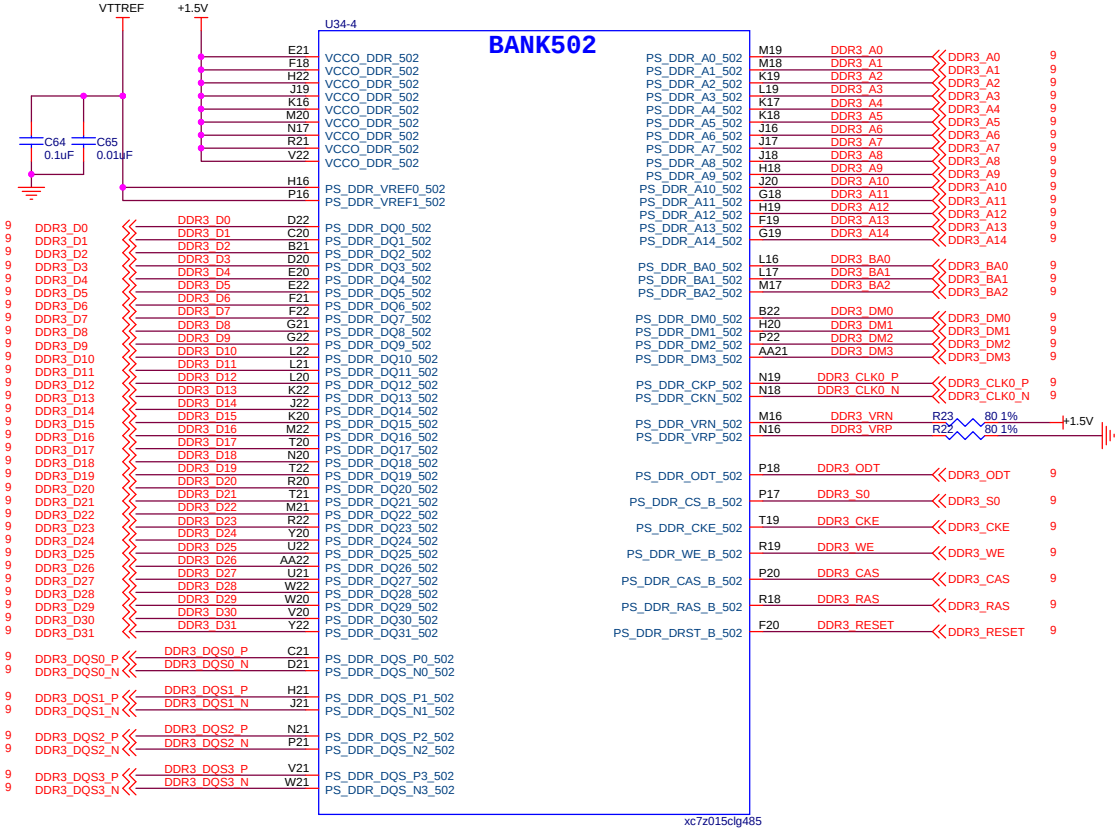

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Title: AC7015 Bank502

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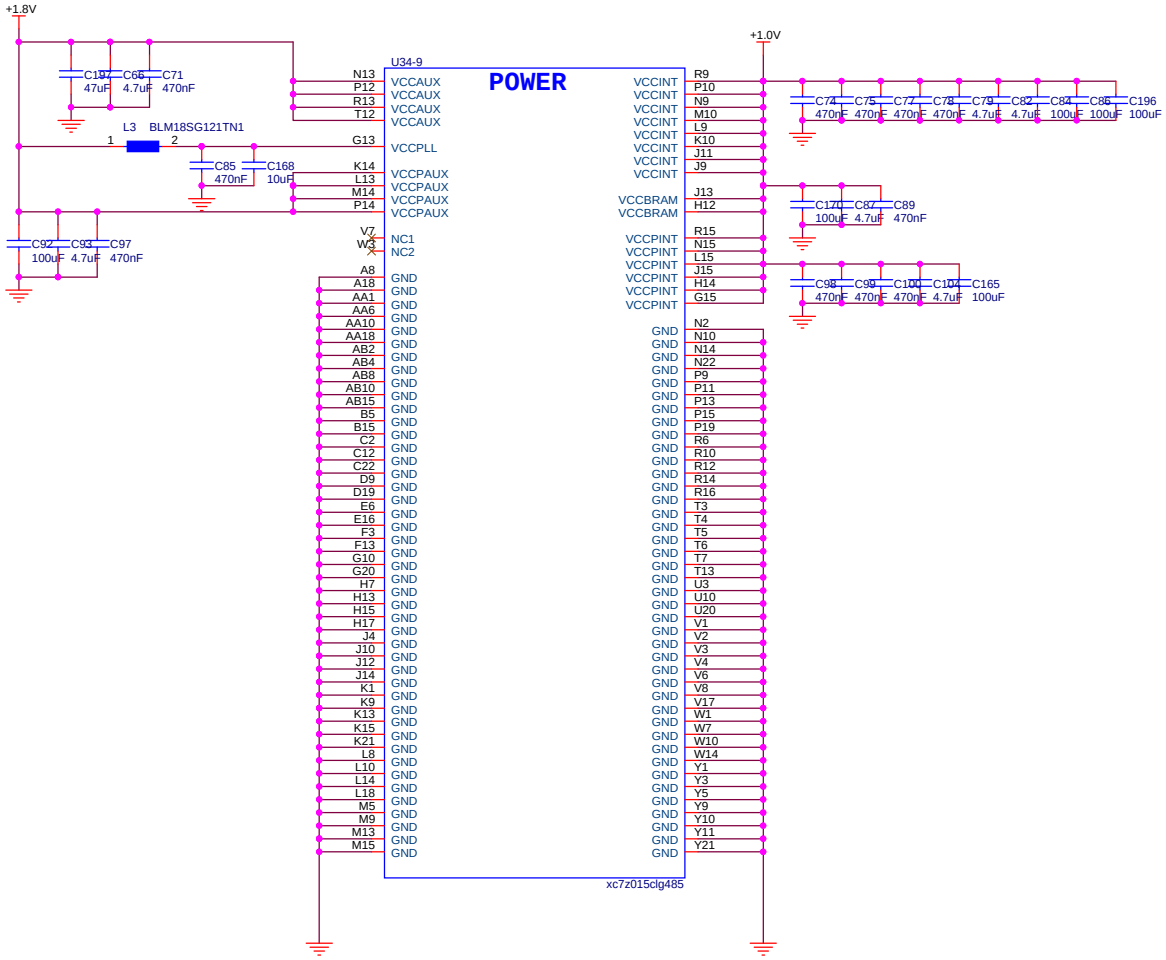

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Size	Document Number: AC7015核心板 Schematics	Rev: 1.0
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为了PCB走线方便，DDR3数据线组内（DQS除外）可以任意交换。
XILINX 的UG933文档的PAGE66有以下说明：

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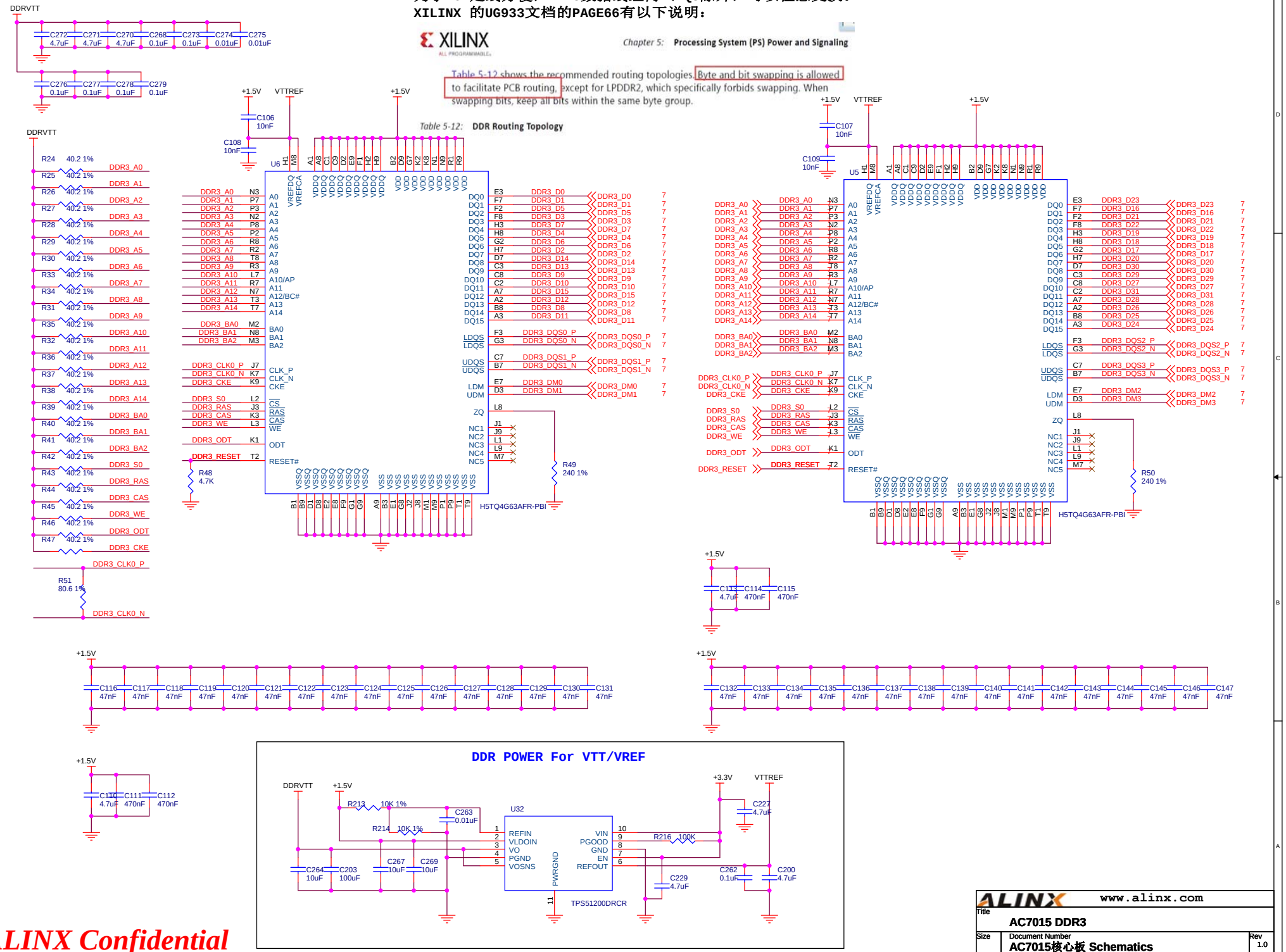
ALL PROGRAMMABLE.

Chapter 5: **Processing System (PS) Power and Signaling**

Table 5-12 shows the recommended routing topologies. Byte and bit swapping is allowed to facilitate PCB routing, except for LPDDR2, which specifically forbids swapping. When swapping bits, keep all bits within the same byte group.

Table 5-12: **DDR Routing Topology**



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Title	AC7015 DDR3
Size	Document Number: AC7015核心板 Schematics; Rev: 1.0
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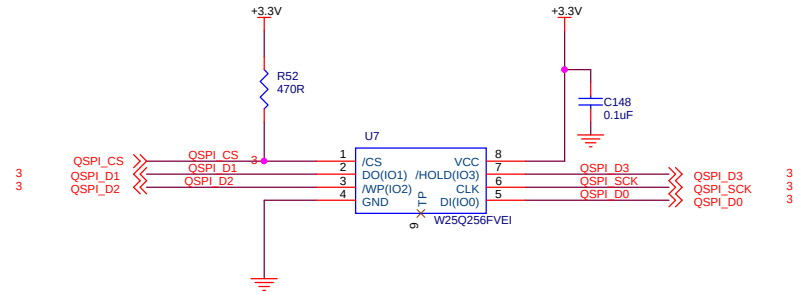

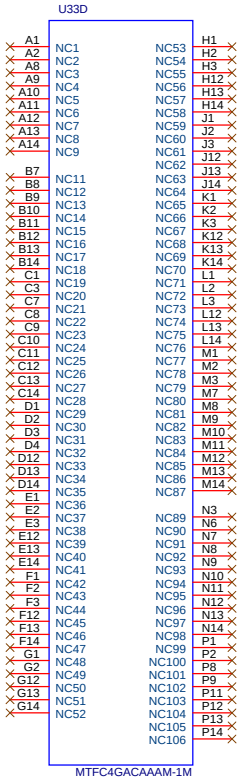

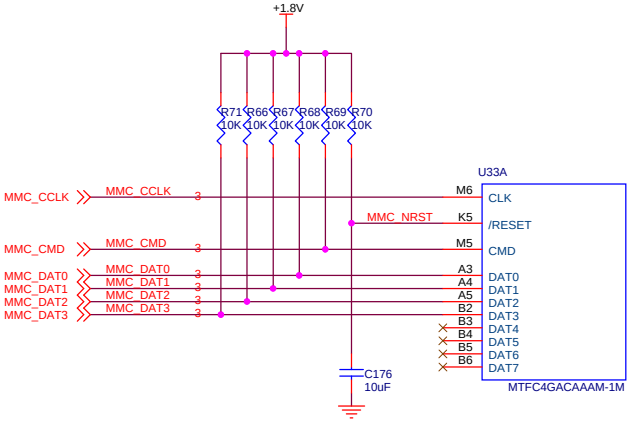

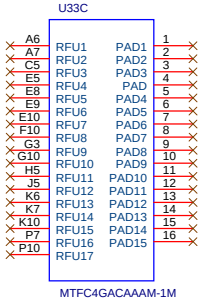

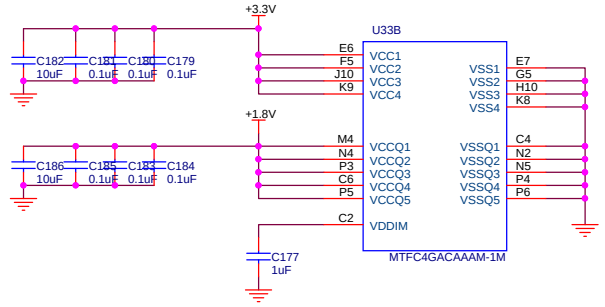

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Title: AC7015 QSPI FLASH		
Size	Document Number: AC7015核心板 Schematics	Rev: 1.0
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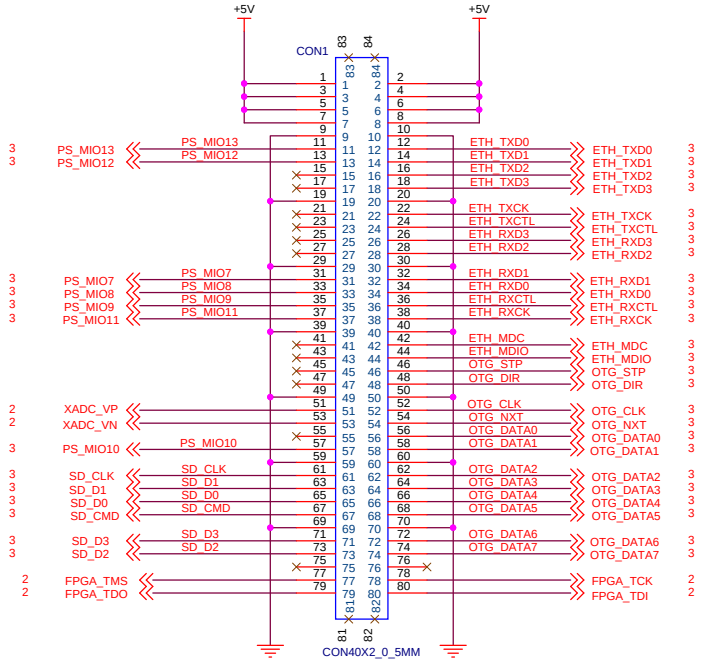
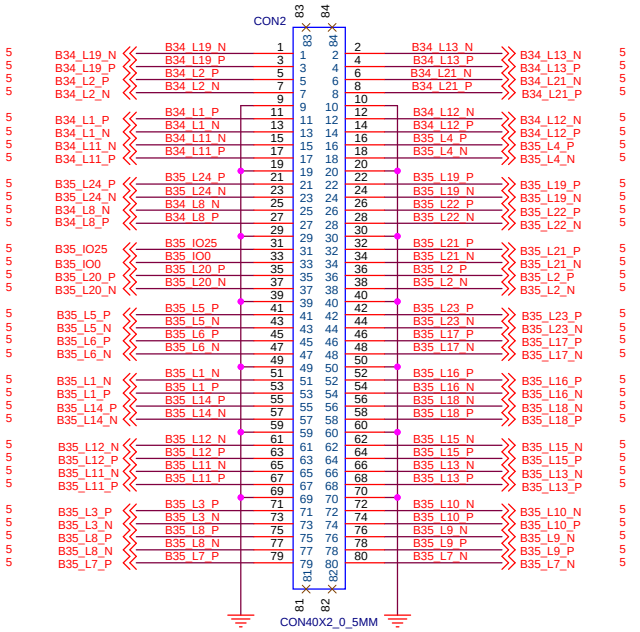
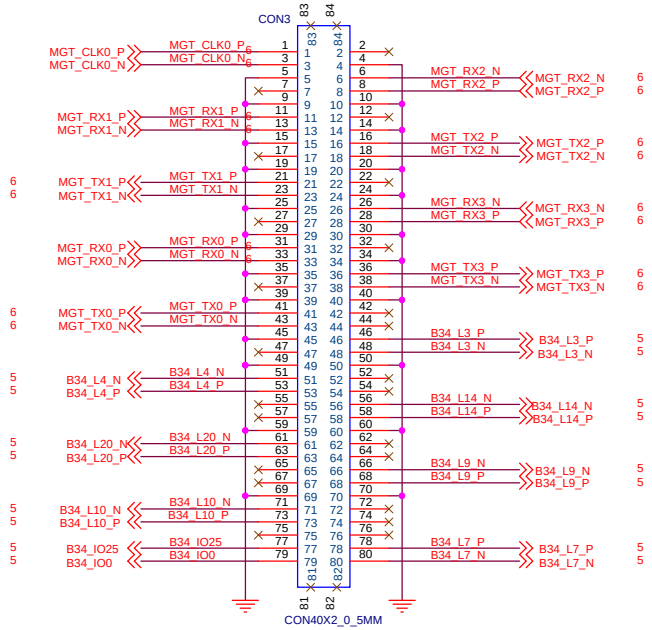
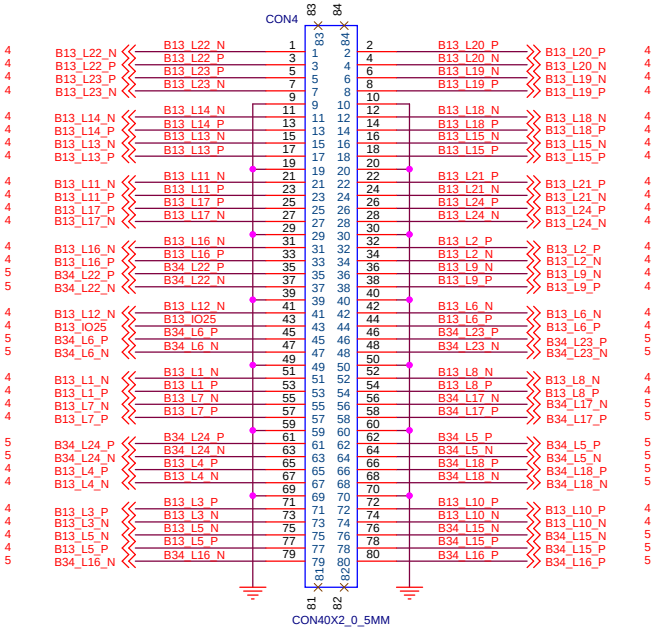
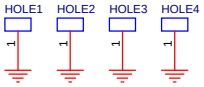








BANK35 IO Voltage is adjustable



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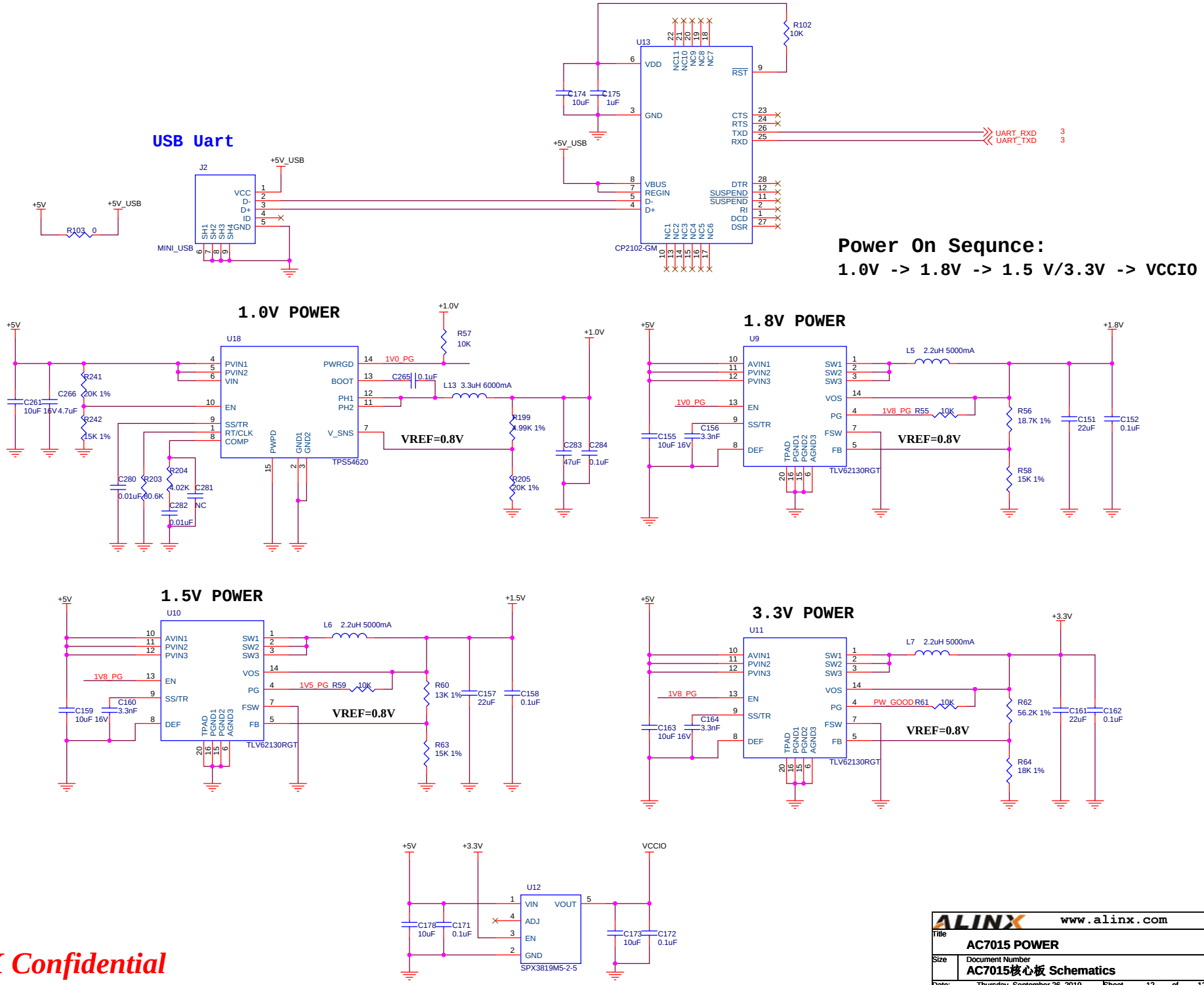
USB Uart
J2
MINI_USB
R103 0
+5V
+5V_USB
U13
CP2102-GM
VDD
GND
VBUS
REGIN
D-
D+
RST
CTS
RTS
TXD
RXD
DTR
SUSPEND
RI
DCD
DSR
R102 10K
C174 10uF
C175 1uF
UART_RXD
UART_TXD
Power On Sequnce:
1.0V -> 1.8V -> 1.5 V/3.3V -> VCCIO
1.0V POWER
U18
TPS54620
PVIN1
PVIN2
VIN
EN
SS/TR
RT/CLK
COMP
PWRGD
BOOT
PH1
PH2
V_SNS
PWPD
GND1
GND2
1V0_PG
VREF=0.8V
R57 10K
R241 20K 1%
R242 15K 1%
R199 4.99K 1%
R205 20K 1%
L13 3.3uH 6000mA
1.8V POWER
U9
TLV62130RGT
AVIN1
PVIN2
PVIN3
SW1
SW2
SW3
VOS
PG
FSW
FB
TPAD
PGND1
PGND2
AGND3
L5 2.2uH 5000mA
R56 18.7K 1%
R58 15K 1%
R55 10K
1.5V POWER
U10
L6 2.2uH 5000mA
1V8_PG
1V5_PG
R59 10K
R60 13K 1%
R63 15K 1%
C157 22uF
C158 0.1uF
3.3V POWER
U11
L7 2.2uH 5000mA
PW_GOOD
R61 10K
R62 56.2K 1%
R64 18K 1%
U12
SPX3819M5-2-5
VIN
VOUT
ADJ
EN
GND
VCCIO
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AC7015 POWER
AC7015核心板 Schematics
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