ZYNQ7000 FPGA Development Board AC7015 System on Module

Version Record

Version	Date	Release By	Description
Rev 1.0	2020-06-29	Rachel Zhou	First Release

Tabel of Contents

Part 1: AC7015 Core Board Introduction

The AC7015 (core board model, the same below) core board is an FPGA development board based on the Zynq chip XC7Z015-2CLG485I of the XILINX ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The ZYNQ FPGA chip contains a wide range of programmable logic cells, DSP and internal RAM.

The core board uses two SK Hynix DDR3 chips (H5TQ4G63AFR-PBI), each with a DDR capacity of 4Gbit; two DDR chips form a 32-bit data bus width, and the read and write data clock frequency between ZYNQ FPGA and DDR3 is up to 533Mhz; such a configuration can meet the system's high bandwidth data processing needs

In order to connect to the expansion board, the four board-to-board connectors of the core board extend the USB interface of the PS side, the Gigabit Ethernet interface, the SD card interface and other remaining MIO ports. Extend ZynQ's 4-pair high-speed transceiver GTP interface. Almost all IO ports (84) of BANK13, BAN34 and BANK35 on the PL side, the level of IO of BANK35 can be modified by replacing the LDO chip on the core board to meet the requirements of users with different level interfaces. For users who need a lot of IOs, this core board will be a good choice. Moreover, the IOs connection part, the routing between the ZYNQ FPGA chip and the interface is equal length and differential processing. The core board size is only 60*60 (mm), which is very suitable for secondary development.

Figure 1-1: AC7015 Core board Front View

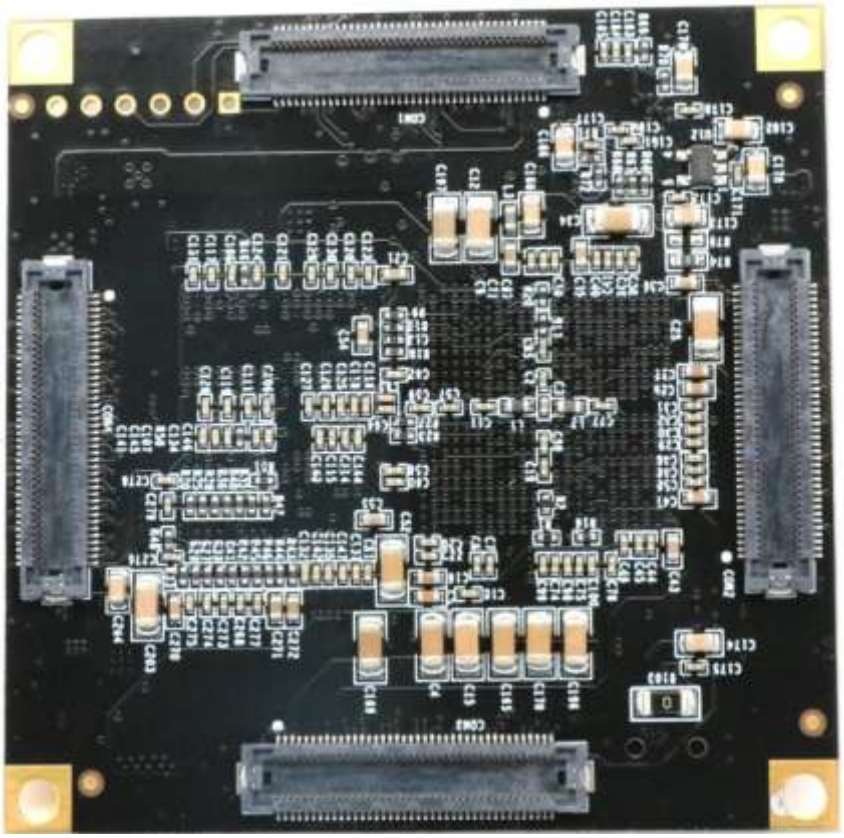

Figure 1-2: AC7015 Core Board Rear View

Part 2: ZYNQ Chip

The development board uses Xilinx's Zynq7000 series chip, model XC7Z015-2CLG485I. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power up or reset. Figure 2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

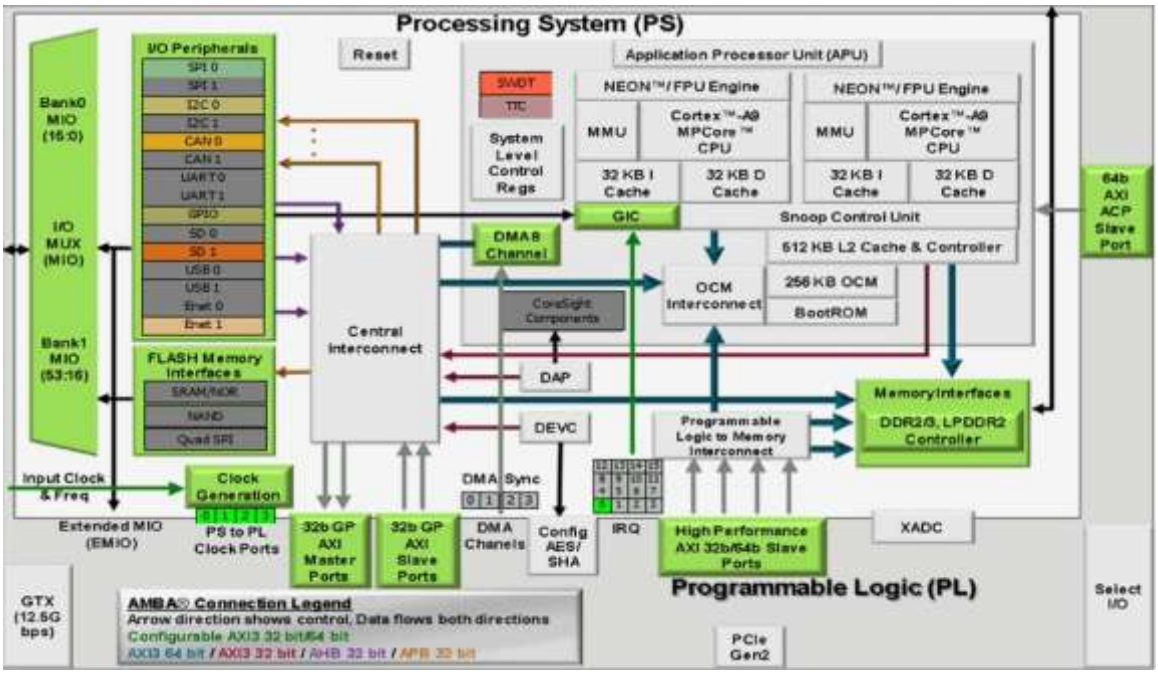

Figure 2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 1GHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3

interface

- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 groups of 32bit GPIO, 54 (32+22) as PS system IO, 64 connected to PL
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- LogicCells: 85K
- Look-up-tables (LUTs):53,200
- Flip-flops:106,400
- 18x25MACCs：220;
- BlockRAM：4.9Mb
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z015-2CLG485I chip speed grade is -2, industrial grade, package is BGA484, pin pitch is 0.8mm, the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2

Figure 2-2: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-3: TheXC7Z020 chip used on the Core Board

Part 3: DDR3 DRAM

The AC7015 core board is equipped with two SK Hynix DDR3 SDRAM chips (1GB total), model H5TQ4G63AFR-PBI. The bus width of DDR3 SDRAM is 32 bits in total. DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 3-1

Bit Number	Chip Model	Capacity	Factory
U5,U6	H5TQ4G63AFR-PBI	256M x 16bit	SK Hynix

Table 3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 3-1:

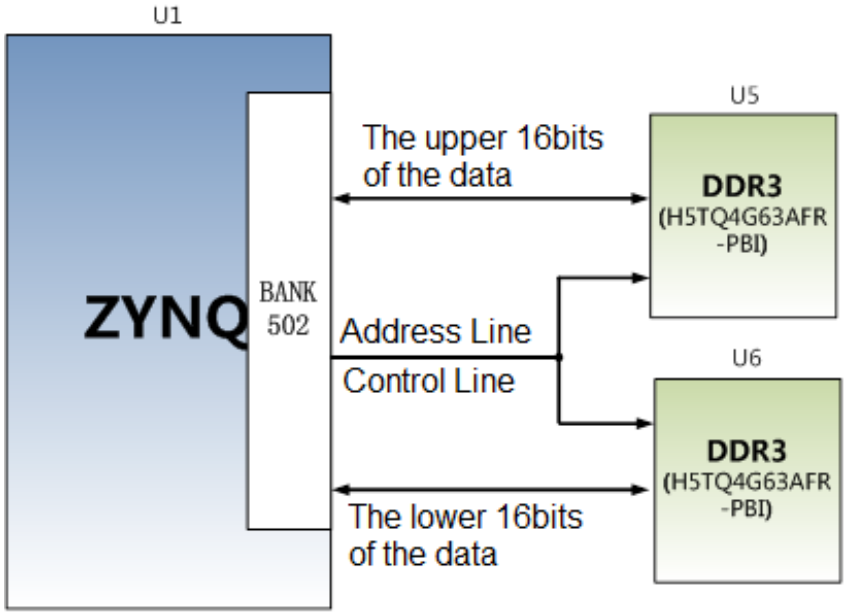

Figure 3-1: The Schematic part of DDR3 DRAM

Figure 3-2: DDR3 DRAM on the Core Board

DDR3 DRAM Pin Assignment

Signal Name	ZYNQ Pin Name	Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C21
DDR3_DQS0_N	PS_DDR_DQS_N0_502	D21
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H21
DDR3_DQS1_N	PS_DDR_DQS_N1_502	J21
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N21
DDR3_DQS2_N	PS_DDR_DQS_N2_502	P21

DDR3_DQS3_P	PS_DDR_DQS_P3_502	V21
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W21
DDR3_D0	PS_DDR_DQ0_502	D12
DDR3_D1	PS_DDR_DQ1_502	C20
DDR3_D2	PS_DDR_DQ2_502	B21
DDR3_D3	PS_DDR_DQ3_502	D20
DDR3_D4	PS_DDR_DQ4_502	E20
DDR3_D5	PS_DDR_DQ5_502	E22
DDR3_D6	PS_DDR_DQ6_502	F21
DDR3_D7	PS_DDR_DQ7_502	F22
DDR3_D8	PS_DDR_DQ8_502	G21
DDR3_D9	PS_DDR_DQ9_502	G22
DDR3_D10	PS_DDR_DQ10_502	L22
DDR3_D11	PS_DDR_DQ11_502	L21
DDR3_D12	PS_DDR_DQ12_502	L20
DDR3_D13	PS_DDR_DQ13_502	K22
DDR3_D14	PS_DDR_DQ14_502	J22
DDR3_D15	PS_DDR_DQ15_502	K20
DDR3_D16	PS_DDR_DQ16_502	M22
DDR3_D17	PS_DDR_DQ17_502	T20
DDR3_D18	PS_DDR_DQ18_502	N20
DDR3_D19	PS_DDR_DQ19_502	T22
DDR3_D20	PS_DDR_DQ20_502	R20
DDR3_D21	PS_DDR_DQ21_502	T21
DDR3_D22	PS_DDR_DQ22_502	M21
DDR3_D23	PS_DDR_DQ23_502	R22
DDR3_D24	PS_DDR_DQ24_502	A20
DDR3_D25	PS_DDR_DQ25_502	U22
DDR3_D26	PS_DDR_DQ26_502	AA22
DDR3_D27	PS_DDR_DQ27_502	U21
DDR3_D28	PS_DDR_DQ28_502	W22
DDR3_D29	PS_DDR_DQ29_502	W20
DDR3_D30	PS_DDR_DQ30_502	V20
DDR3_D31	PS_DDR_DQ31_502	Y22
DDR3_DM0	PS_DDR_DM0_502	B22
DDR3_DM1	PS_DDR_DM1_502	H20
DDR3_DM2	PS_DDR_DM2_502	P22
DDR3_DM3	PS_DDR_DM3_502	AA21
DDR3_A0	PS_DDR_A0_502	M19
DDR3_A1	PS_DDR_A1_502	M18
DDR3_A2	PS_DDR_A2_502	K19
DDR3_A3	PS_DDR_A3_502	L19
DDR3_A4	PS_DDR_A4_502	K17
DDR3_A5	PS_DDR_A5_502	K18
DDR3_A6	PS_DDR_A6_502	J16
DDR3_A7	PS_DDR_A7_502	J17
DDR3_A8	PS_DDR_A8_502	J18
DDR3_A9	PS_DDR_A9_502	H18
DDR3_A10	PS_DDR_A10_502	J20
DDR3_A11	PS_DDR_A11_502	G18
DDR3_A12	PS_DDR_A12_502	H19
DDR3_A13	PS_DDR_A13_502	F19
DDR3_A14	PS_DDR_A14_502	G19

DDR3_BA0	PS_DDR_BA0_502	L16
DDR3_BA1	PS_DDR_BA1_502	L17
DDR3_BA2	PS_DDR_BA2_502	M17
DDR3_S0	PS_DDR_CS_B_502	P17
DDR3_RAS	PS_DDR_RAS_B_502	R18
DDR3_CAS	PS_DDR_CAS_B_502	P20
DDR3_WE	PS_DDR_WE_B_502	R19
DDR3_ODT	PS_DDR_ODT_502	P18
DDR3_RESET	PS_DDR_DRST_B_502	F20
DDR3_CLK0_P	PS_DDR_CKP_502	N19
DDR3_CLK0_N	PS_DDR_CKN_502	N18
DDR3_CKE	PS_DDR_CKE_502	T19

Table 3-2: DDR3 DRAM Pin Assignment

Part 4: QSPI Flash

The core board is equipped with a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U7	W25Q256FVEI	32M Byte	Winbond

Table 4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 4-1 shows the QSPI Flash in the schematic.

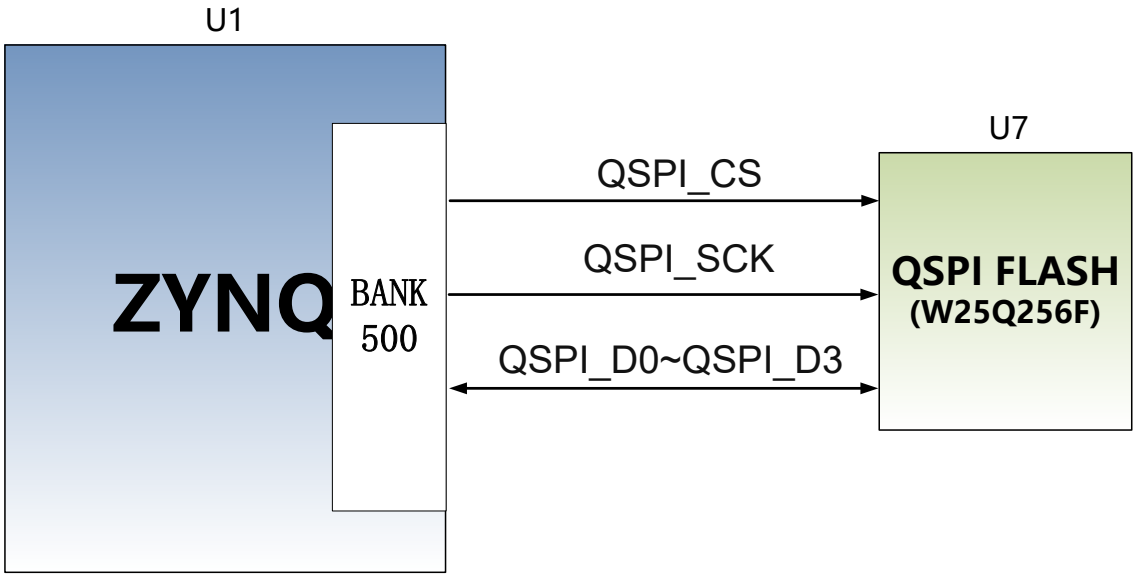

Figure 4-1: QSPI Flash in the schematic

Figure 4-2: QSPI Flash on the Core Board

Pin Assignment of QSPI Flash

Signal Name	ZYNQ Pin Name	Pin Number
QSPI_SCK	PS_MIO6_500	A19
QSPI_CS	PS_MIO1_500	A22
QSPI_D0	PS_MIO2_500	A21
QSPI_D1	PS_MIO3_500	F17
QSPI_D2	PS_MIO4_500	E19
QSPI_D3	PS_MIO5_500	A20

Table 4-2: Pin Assignment of QSPI FLASH

Part 5: eMMC Flash

The core board is equipped with a large capacity 8GB eMMC FLASH chip,

model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM-based applications, system files, and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 5-1：

Position	Model	Capacity	Factory
U33	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 5-1: eMMC FLASH Specification

eMMC FLASH is connected to the GPIO port of the BANK501 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 5-1 shows the eMMC Flash in the schematic.

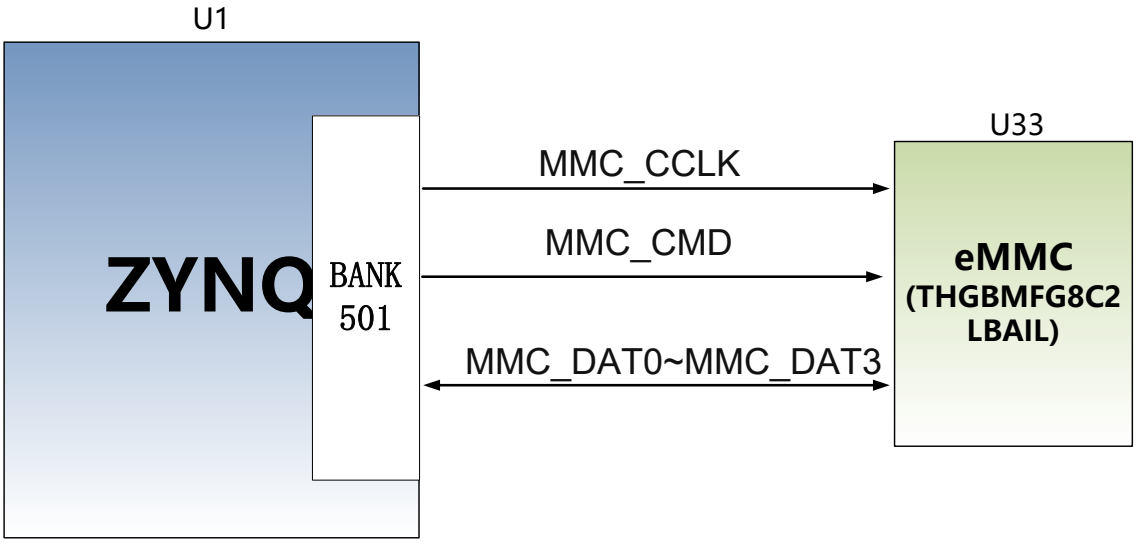

Figure 5-1: eMMC Flash in the Schematic

Figure 5-2: eMMC Flash on the Core Board

Pin Assignment of eMMC Flash

Signal Name	ZYNQ Pin Name	Pin Number
MMC_CCLK	PS_MIO48_501	D12
MMC_CMD	PS_MIO47_501	B13
MMC_D0	PS_MIO46_501	D11
MMC_D1	PS_MIO49_501	C9
MMC_D2	PS_MIO50_501	D10
MMC_D3	PS_MIO51_501	C13

Table 5-2: Pin Assignment of eMMC FLASH

Part 6: Clock configuration

AC7015 core board provides active clock for PS system, PL logic part and GTP transceiver respectively, so that PS system, PL logic and GTP transceiver can work independently. The PS and PL terminals use a single-ended crystal, and the GTP terminal uses a differential crystal.

PS system clock source

The ZYNQ chip provides a 33.333 MHz clock input to the PS section through the X1 crystal on the development board. The input of the clock is connected to the pins of PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 6-1:

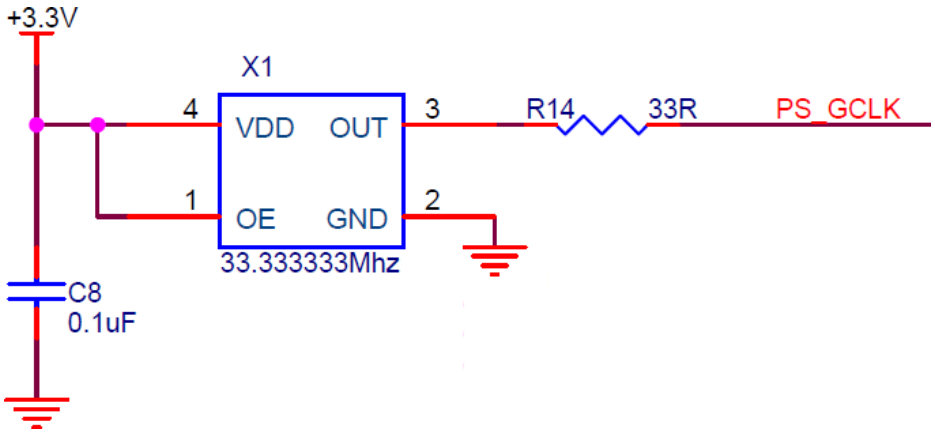

Figure 6-1: Active crystal oscillator to the PS section

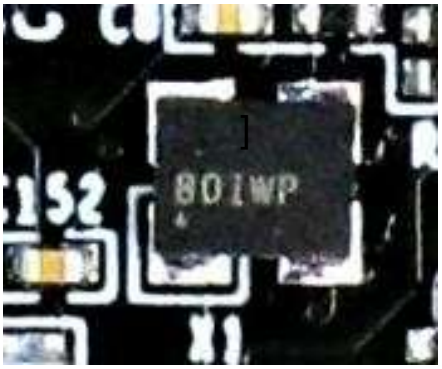

Figure 6-2: 33.333Mhz active Crystal Oscillator on the Core Board

PS Clock pin assignment:

Signal Name	ZYNQ Pin
PS_GCLK	F16

Table 6-1: PS Clock pin assignment

PL system clock source

The AC7015 core board provides a single-ended 125MHz PL system clock source with 3.3V power supply. The crystal output is connected to the global clock (MRCC) of the FPGA BANK13, which can be used to drive user logic within the FPGA. The schematic diagram of the clock source is shown in Figure 6-3:

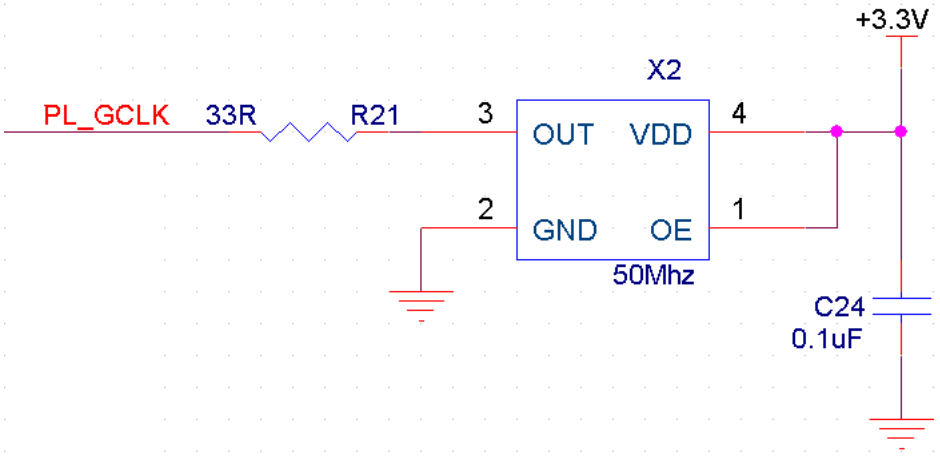

Figure 6-3: PL system clock source

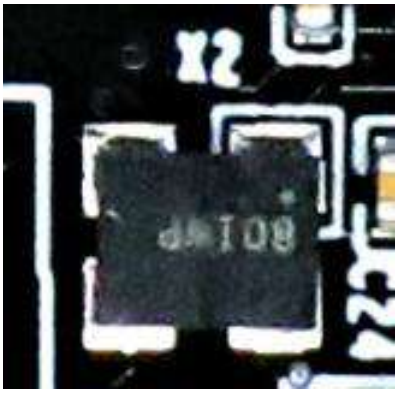

Figure 6-4: 50 Mhz oscillator on the Core Board

PL Clock pin assignment:

Signal Name	ZYNQ Pin
PL_GCLK	Y14

Table 6-2: PL Clock pin assignment

GTP differential clock

The AC7015 core board provides a differential 125MHz GTP reference clock. The differential LVDS clock output is connected to the reference clock of BANK112. This 125Mhz clock can be used as the reference clock for fiber optic data communication on the carrier board. The schematic diagram of the clock source is shown in Figure 6-5

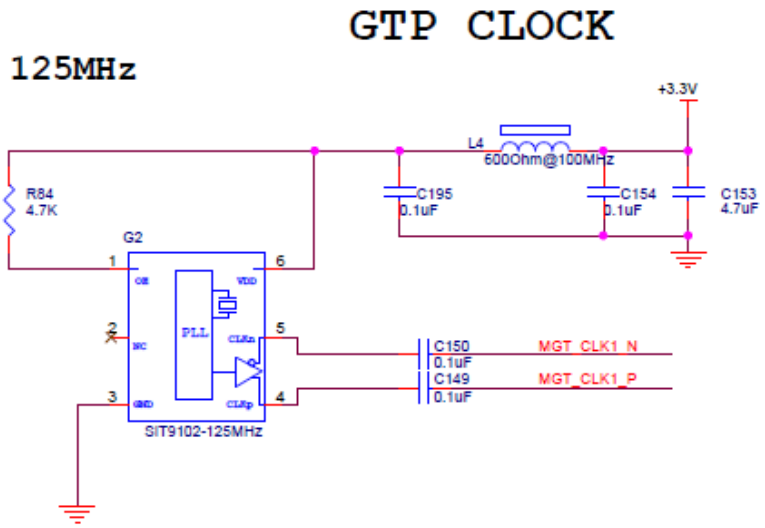

Figure 6-5: GTP Reference Clock

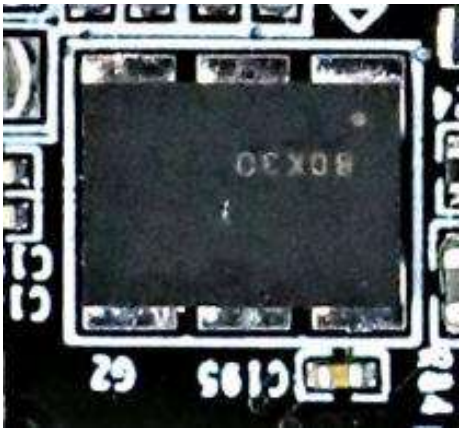

Figure 6-6: 125Mhz oscillator on the Core Board

GTP Clock pin assignment:

Signal Name	ZYNQ Pin
MGT_CLK1_P	U5
MGT_CLK1_N	V5

Part 7: USB to Serial Port

For the AC7015 core board to work and debug separately, we have a Uart to USB interface for the core board. Used for separate power supply and debugging of the core board. The conversion chip uses the USB-UART chip of Silicon Labs

CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

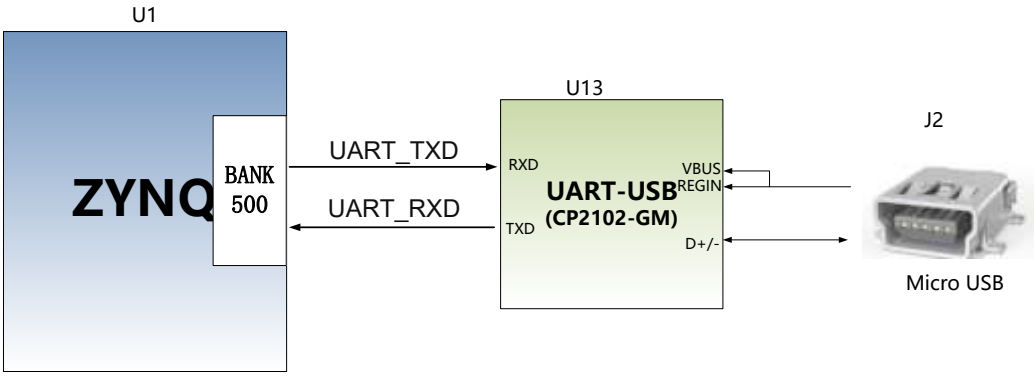

Figure 7-1: USB to Serial Port

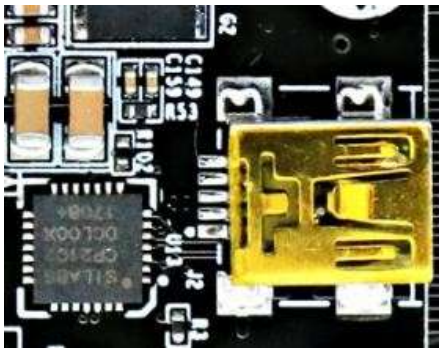

Figure 7-2: USB to Serial Port on the Core Board

Uart Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Explain
UART_RXD	PS_MIO14_500	B17	Uart data Input
UART_TXD	PS_MIO15_500	E17	Uart data Output

Table 7-1: Uart Pin Assignment

Part 8: LED Light

There are 4 red LED lights on the AC7015 core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), two are the user LED lights (LED1~LED2). When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will

illuminate. Two user LED lights are connected to the MIO of the PS, one is connected to the IO of the PL, the user can control the lighting and off by the program, when the IO voltage connected to the user LED light is high, the user LED light is off, when the connection IO voltage is low, the user LED will be illuminated. The schematic diagram of the LED light hardware connection is shown in Figure 8-1:

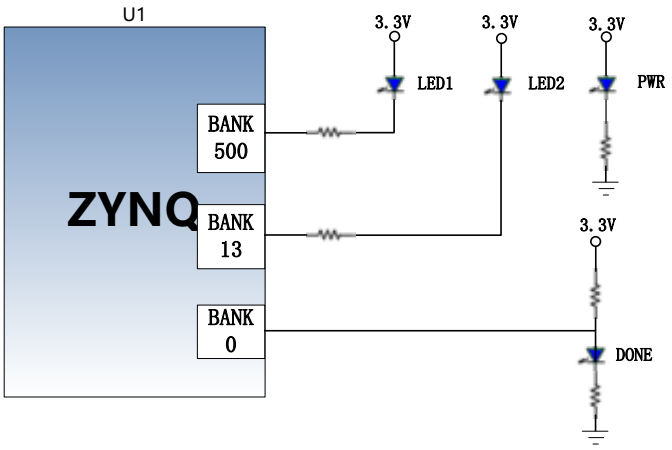

Figure 8-1: The schematic diagram of the LED light hardware connection

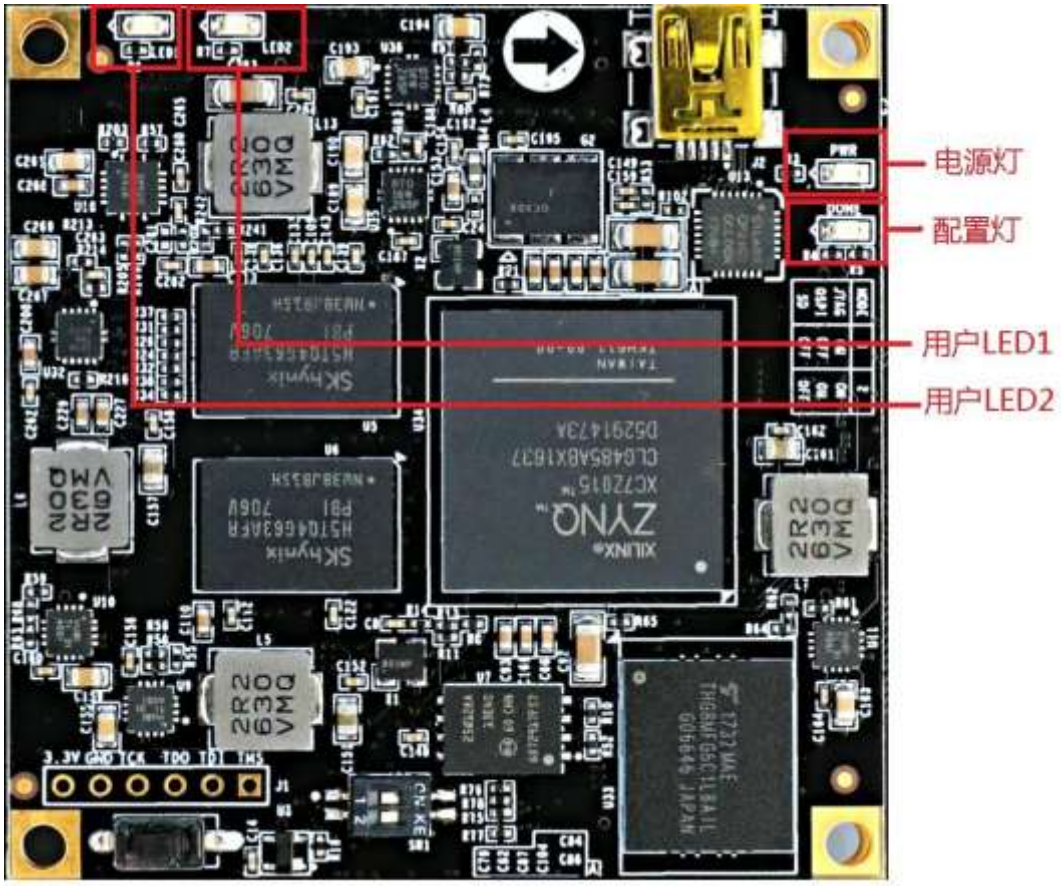

Figure 8-2: LED light on the Core Board

LED Pin Assignment:

Signal Name	ZYNQ Pin Name	ZNYQ Pin Number	Description
MIO0_LE	PS_MIO0_500	G17	User LED1
PL_LED	IO_0_13	T16	User LED2

Table 8-1: LED Pin Assignment

Part 9: Reset Button

The AC7015 has a reset button RESET and circuitry on the core board. The reset signal is connected to the PS reset pin of the ZYNQ chip. The reset button can be used by the user to reset the ZYNQ system. When the reset button is pressed, the reset chip will generate a low level reset signal to the ZYNQ chip. The schematic diagram of the reset button and reset chip connection is shown in Figure 9-1:

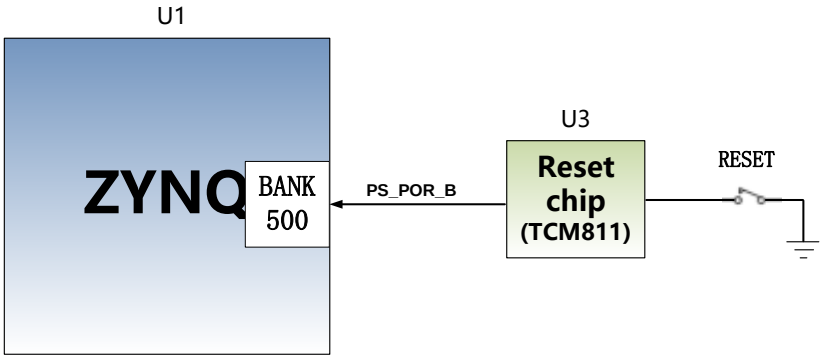

Figure 9-1: Reset button connection diagram

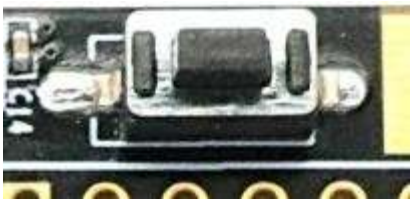

Figure 9-2: Reset button on the Core Board

Reset Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B_500	B18	Reset Key

Table 9-1: Reset Pin Assignment

Part 10: JTAG Interface

The JTAG test socket J1 is reserved on the AC7015 core board for separate JTAG download and debugging of the core board. Figure 2-10-1 is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK, GND. , +3.3V these six signals.

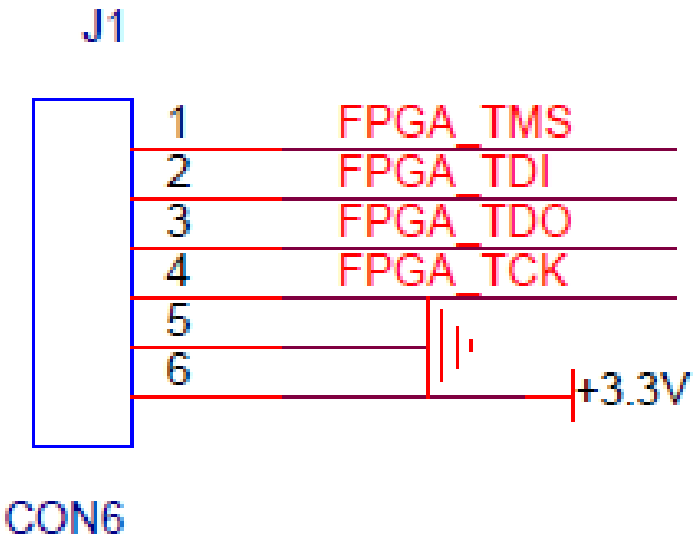

Figure 10-1: JTAG interface part of the core board schematic

The JTAG interface J1 on the core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connection to debug on the core board, you need to solder a 6-pin single-row pin header. Figure 10-2 shows the physical map of the JTAG interface on the development board.

Figure 10-2: JTAG interface on the core board

Part 11: DIP switch configuration

The AC7015 has a 2-digit DIP switch SW1 on the core board to configure the ZYNQ system's startup mode. The AC7015 system development platform supports three startup modes. The three startup modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the XC7Z015 chip is powered up, it will detect the level of the MIO port (MIO5 and MIO4) to determine which startup mode. Users can select different startup modes through the DIP switch SW1 on the core board. The SW1 startup mode configuration is shown in Table 11-1

SW1	Position（1，2）	MIO5,MIO4 Level	Startup mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 11-1: The SW1 Startup Mode Configuration

Part 12: Power

The AC7021 core board is powered by DC5V. It is powered by the Mini USB interface when it is used alone. It is powered by the extension board when the backplane is connected. Please be careful not to supply power to the Mini USB and the extension board at the same time to avoid damage. The power supply design on the core board is shown in Figure 12-1.

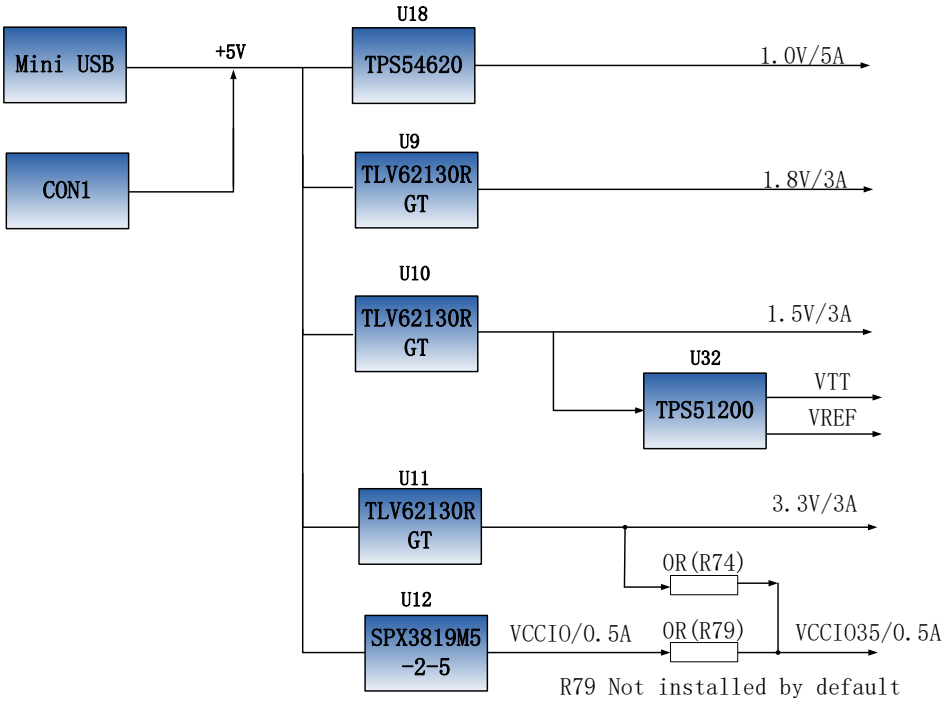

Figure 12-1: The Power Supply Design on the Core Board

The development board is powered by +5V, and is converted into +1.0V, +1.8V, +1.5V, +3.3V four-way power supply through four-way DC/DC power supply core TPS54620TLV62130RGT. The output current of +1.0V can be as high as 5A, and the other three output current are 3A. The VCCIO 2.5V power supply is generated by one LDO SPX3819M5-2-5. The VCCIO 2.5V power supply is mainly reserved for the BANK power supply of the BANK35 of the FPGA. The user can select the power supply of BANK35 through two 0 ohm resistors (R74, R79). By default, the R74 on the development board is installed, and the resistor of R79 is not installed, so the power supply of BANK35 is +3.3V. The user can replace the resistor so that the IO of the BANK35 outputs a voltage standard of 2.5V. 1.5V generates the VTT and VREF voltages required by DDR3 through TI's TPS51200. The functions of each power distribution are shown in the following Table 12-1:

Power	Function
+1.0V	ZYNQ PS and PL section Core Voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage, BANK501 IO voltage, eMMC
+3.3V	ZCNQ Bank0, Bank500, Bank13, Bank35 VCCIO, QSIP FLASH,

	Clock Crystal
+1.5V	DDR3, ZYNQ Bank501
VREF,VTT(+0.75V)	DDR3
VCCIO(+2.5V)	Reserved for ZYNQ Bank33,Bank 34

Table 12-1: The Functions of Each Power Distribution

Because the power supply of ZYNQ FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO). The circuit design ensures the normal operation of the chip. The power supply on the core board detailed as Figure 12-2 below:

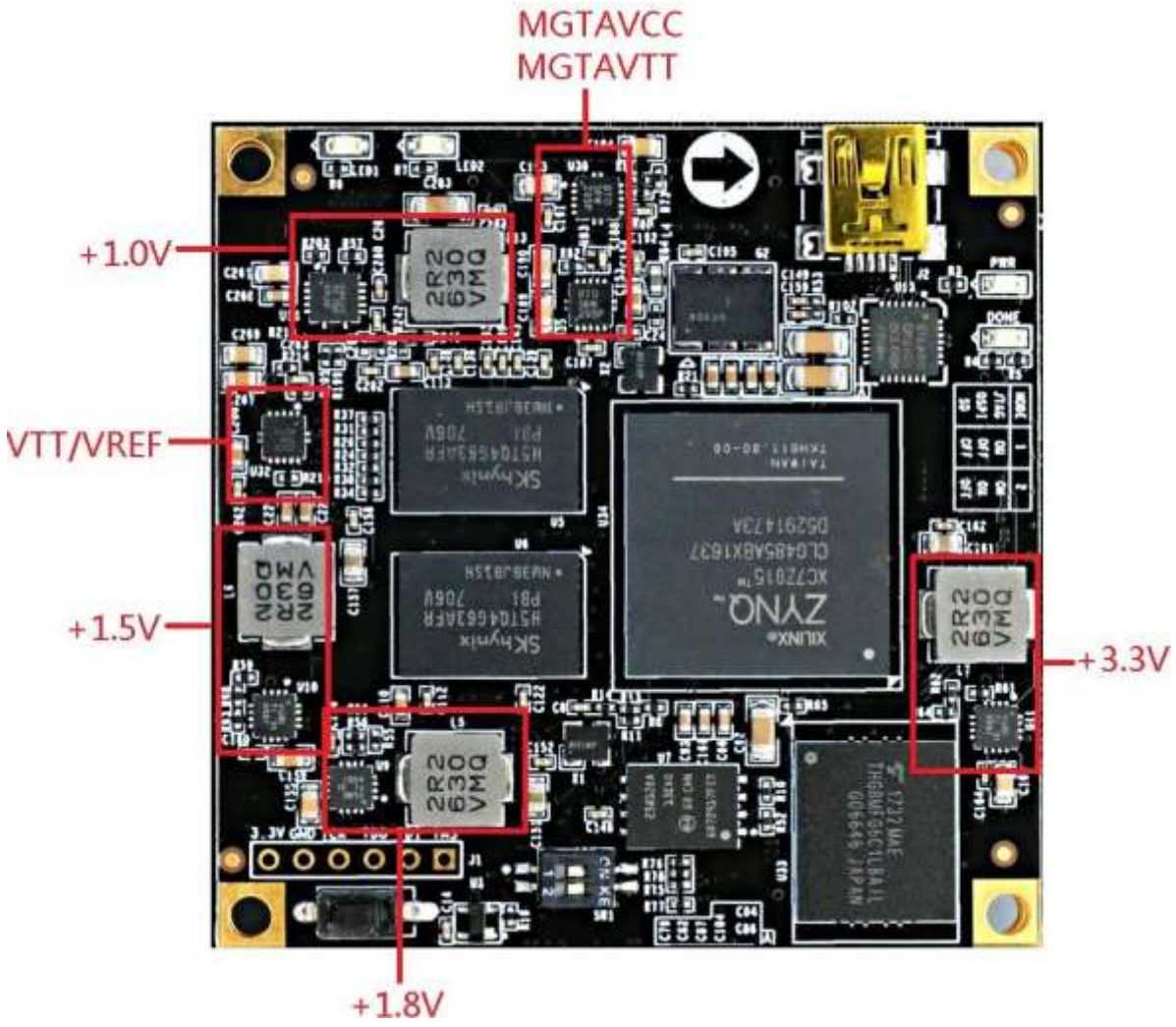

Figure 12-2: The Power Supply on the Core Board

Part 13: Structure diagram

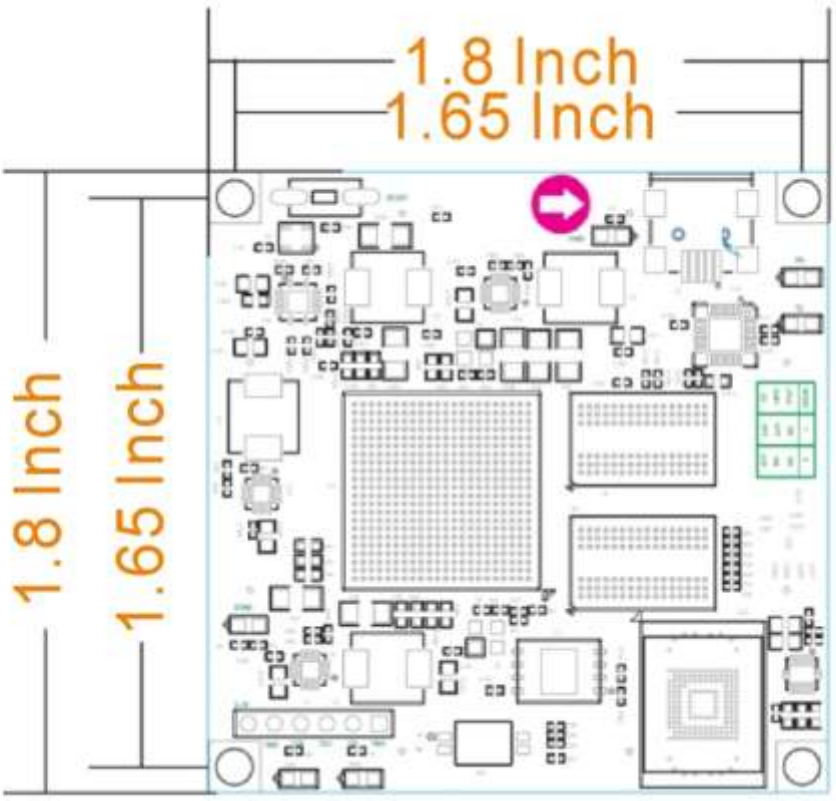

Figure 13-1: The Structure diagram (Top View)

Part 14: Connector pin definition

The core board expands four high-speed expansion ports, and uses four 80-pin inter-board connectors (CON1~CON4) to connect with the expansion board. The PIN pitch of the connector is 0.5mm. Among them, CON1 is connected to the power input, the MIO signal of the PS and the JTAG signal, and CON2~CON4 are connected to the IOs signals of BANK13, BANK34, BANK35 of PL and GTP transceiver signal. The IOs levels of BANK35 can be changed by changing the level of the LDO chip (U12) on the board. The default is 3.3V.

Pin assignments detailed as Table 14-1, Table 14-2, Table 14-3, Table 14-4

CON1 Pin	Signal Name	ZYNQ Pin Name	CON1 Pin	Signal Name	ZYNQ Pin Name
1	+5V	-	2	+5V	-
3	+5V	-	4	+5V	-
5	+5V	-	6	+5V	-
7	+5V	-	8	+5V	-
9	GND	-	10	GND	-
11	PS_MIO13	A17	12	ETH_TXD0	E14
13	PS_MIO12	C18	14	ETH_TXD1	A16
15	-	-	16	ETH_TXD2	E13
17	-	-	18	ETH_TXD3	A15
19	GND	-	20	GND	-
21	-	-	22	ETH_TXCK	D17
23	-	-	24	ETH_TXCTL	F12
25	-	-	26	ETH_RXD3	A10
27	-	-	28	ETH_RXD2	F11
29	GND	-	30	GND	-
31	PS_MIO7	D18	32	ETH_RXD1	B16
33	PS_MIO8	E18	34	ETH_RXD0	E12
35	PS_MIO9	C19	36	ETH_RXCTL	D16
37	PS_MIO11	B19	38	ETH_RXCK	A9
39	GND	-	40	GND	-
41	-	-	42	ETH_MDC	D13
43	-	-	44	ETH_MDIO	C11
45	-	-	46	OTG_STP	A12
47	-	-	48	OTG_DIR	E15
49	GND	-	50	GND	-
51	XADC_VP	L12	52	OTG_CLK	A14
53	XADC_VN	M11	54	OTG_NXT	F14
55	-	-	56	OTG_DATA0	C16

57	PS_MIO10	G16	58	OTG_DATA1	G11
59	GND	-	60	GND	-
61	SD_CLK	E9	62	OTG_DATA2	B11
63	SD_D1	B12	64	OTG_DATA3	F9
65	SD_D0	D15	66	OTG_DATA4	A11
67	SD_CMD	C15	68	OTG_DATA5	B9
69	GND	-	70	GND	-
71	SD_D3	B14	72	OTG_DATA6	F10
73	SD_D2	E10	74	OTG_DATA7	C10
75	-	-	76	-	-
77	FPGA_TMS	H10	78	FPGA_TCK	H11
79	FPGA_TDO	G9	80	FPGA_TDI	H9

Table 2-14-1: Pin Assignment of CON1

CON2 Pin	Signal Name	ZYNQ Pin Name	CON2 Pin	Signal Name	ZYNQ Pin Name
1	B34_L19_N	N5	2	B34_L13_N	T1
3	B34_L19_P	N6	4	B34_L13_P	T2
5	B34_L2_P	J7	6	B34_L21_N	N3
7	B34_L2_N	J6	8	B34_L21_P	N4
9	GND	-	10	GND	-
11	B34_L1_P	J8	12	B34_L12_N	L4
13	B34_L1_N	K8	14	B34_L12_P	L5
15	B34_L11_N	K3	16	B35_L4_P	G8
17	B34_L11_P	K4	18	B35_L4_N	G7
19	GND	-	20	GND	-
21	B35_L24_P	H1	22	B35_L19_P	H4
23	B35_L24_N	G1	24	B35_L19_N	H3
25	B34_L8_N	J1	26	B35_L22_P	G3
27	B34_L8_P	J2	28	B35_L22_N	G2
29	GND	-	30	GND	-
31	B35_IO25	H5	32	B35_L21_P	E4

33	B35_IO0	H6	34	B35_L21_N	E3
35	B35_L20_P	G4	36	B35_L2_P	D7
37	B35_L20_N	F4	38	B35_L2_N	D6
39	GND	-	40	GND	-
41	B35_L5_P	F5	42	B35_L23_P	F2
43	B35_L5_N	E5	44	B35_L23_N	F1
45	B35_L6_P	G6	46	B35_L17_P	E2
47	B35_L6_N	F6	48	B35_L17_N	D2
49	GND	-	50	GND	-
51	B35_L1_N	E7	52	B35_L16_P	D1
53	B35_L1_P	F7	54	B35_L16_N	C1
55	B35_L14_P	D3	56	B35_L18_N	B1
57	B35_L14_N	C3	58	B35_L18_P	B2
59	GND	-	60	GND	-
61	B35_L12_N	C4	62	B35_L15_N	A1
63	B35_L12_P	D5	64	B35_L15_P	A2
65	B35_L11_N	C5	66	B35_L13_N	B3
67	B35_L11_P	C6	68	B35_L13_P	B4
69	GND	-	70	GND	-
71	B35_L3_P	E8	72	B35_L10_N	A4
73	B35_L3_N	D8	74	B35_L10_P	A5
75	B35_L8_P	B7	76	B35_L9_N	A6
77	B35_L8_N	B6	78	B35_L9_P	A7
79	B35_L7_P	C8	80	B35_L7_N	B8

Table 2-14-2: Pin Assignment of CON2

CON3 Pin	Signal Name	ZYNQ Pin Name	CON3 Pin	Signal Name	ZYNQ Pin Name
1	MGT_CLK0_P	U9	2	-	-
3	MGT_CLK0_N	V9	4	GND	-
5	GND	-	6	MGT_RX2_ N	AB9
7	-	-	8	MGT_RX2_p	AA9

9	GND	-	10	GND	-
11	MGT_RX1_P	W8	12	-	-
13	MGT_RX1_N	Y8	14	GND	-
15	GND	-	16	MGT_TX2_P	AA5
17	-	-	18	MGT_TX2_N	AB5
19	GND	-	20	GND	-
21	MGT_TX1_P	W4	22	-	-
23	MGT_TX1_N	Y4	24	GND	-
25	GND	-	26	MGT_RX3_N	Y6
27	-	-	28	MGT_RX3_P	W6
29	GND	-	30	GND	-
31	MGT_RX0_P	AA7	32	-	-
33	MGT_RX0_N	AB7	34	GND	-
35	GND	-	36	MGT_TX3_P	W2
37	-	-	38	MGT_TX3_N	Y2
39	GND	-	40	GND	-
41	MGT_TX0_P	AA3	42	-	-
43	MGT_TX0_N	AB3	44	-	-
45	GND		46	B34_L3_P	K7
47	-		48	B34_L3_N	L7
49	GND	-	50	GND	-
51	B34_L4_N	M6	52	-	-
53	B34_L4_P	L6	54	-	-
55	-	-	56	B34_L14_N	U1
57	-	-	58	B34_L14_P	U2
59	GND	-	60	GND	-
61	B34_L20_N	P5	62	-	
63	B34_L20_P	P6	64	-	
65	-	-	66	B34_L9_N	J3
67	-	-	68	B34_L9_P	K2
69	GND	-	70	GND	-
71	B34_L10_N	L1	72	-	-

73	B34_L10_P	L2	74	-	-
75	-	-	76	-	-
77	B34_IO25	R8	78	B34_L7_P	J5
79	B34_IO0	H8	80	B34_L7_N	K5

Table 2-14-3: Pin Assignment of CON3

CON4 Pin	Signal Name	ZYNQ Pin Name	CON4 Pin	Signal Name	ZYNQ Pin Name
1	B13_L22_N	U18	2	B13_L20_P	U19
3	B13_L22_P	U17	4	B13_L20_N	V19
5	B13_L23_P	V16	6	B13_L19_N	T17
7	B13_L23_N	W16	8	B13_L19_P	R17
9	GND	-	10	GND	-
11	B13_L14_N	AA17	12	B13_L18_N	AA20
13	B13_L14_P	AA16	14	B13_L18_P	AA19
15	B13_L13_N	Y19	16	B13_L15_N	AB22
17	B13_L13_P	Y18	18	B13_L15_P	AB21
19	GND	-	20	GND	-
21	B13_L11_N	AA15	22	B13_L21_P	V18
23	B13_L11_P	AA14	24	B13_L21_N	W18
25	B13_L17_P	AB16	26	B13_L24_P	W17
27	B13_L17_N	AB17	28	B13_L24_N	Y17
29	GND	-	30	GND	-
31	B13_L16_N	AB19	32	B13_L2_P	V15
33	B13_L16_P	AB18	34	B13_L2_N	W15
35	B34_L22_P	M4	36	B13_L9_N	AB14
37	B34_L22_N	M3	38	B13_L9_P	AB13
39	GND	-	40	GND	-
41	B13_L12_N	Y15	42	B13_L6_N	U14
43	B13_IO25	U16	44	B13_L6_P	U13
45	B34_L6_P	M8	46	B34_L23_P	R5
47	B34_L6_N	M7	48	B34_L23_N	R4

49	GND	-	50	GND	-
51	B13_L1_N	V14	52	B13_L8_N	AB12
53	B13_L1_P	V13	54	B13_L8_P	AA12
55	B13_L7_N	AB11	56	B34_L17_N	R2
57	B13_L7_P	AA11	58	B34_L17_P	R3
59	GND	-	60	GND	-
61	B34_L24_P	P7	62	B34_L5_P	N8
63	B34_L24_N	R7	64	B34_L5_N	P8
65	B13_L4_P	V11	66	B34_L18_P	P3
67	B13_L4_N	W11	68	B34_L18_N	P2
69	GND	-	70	GND	-
71	B13_L3_P	W12	72	B13_L10_P	Y12
73	B13_L3_N	W13	74	B13_L10_N	Y13
75	B13_L5_N	U12	76	B34_L15_N	M1
77	B13_L5_P	U11	78	B34_L15_P	M2
79	B34_L16_N	P1	80	B34_L16_P	N1

Table 2-14-4: Pin Assignment of CON4