ZYNQ7000 FPGA Development Board AC7021BB System on Module

Version Record

Version	Date	Release By	Description
Rev 1.0	2020-06-29	Rachel Zhou	First Release

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Part 1: AC7021B Core Board Introduction

The AC7021B (core board model, the same below) core board is an FPGA development board based on the Zynq chip XC7Z020-2CLG484I of the XILINX ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The ZYNQ FPGA chip contains a wide range of programmable logic cells, DSP and internal RAM.

The core board uses two SK Hynix DDR3 chips (H5TQ4G63AFR-PBI), each with a 4Gbit DDR capacity; two DDR chips form a 32-bit data bus width, and the read and write data clock frequency between ZYNQ FPGA and DDR3 is up to 533Mhz; such a configuration can meet the system's high bandwidth data processing needs

In order to connect to the carrier board, the four board-to-board connectors of the core board extend the USB interface of the PS side, the Gigabit Ethernet interface, the SD card interface and other remaining MIO ports. As well as almost all IO ports (198) of BANK13, BANK33, BAN34 and BANK35 on the PL side, the level of IO of BANK33 and BANK34 can be modified by replacing the LDO chip on the core board to meet the requirements of users with different level interfaces. For users who need a lot of IOs, this core board will be a good choice. Moreover, the IOs connection part, the routing between the ZYNQ FPGA chip and the interface is equal length and differential processing. The core board size is only 2.36 inch* 2.36 inch, which is very suitable for secondary development.

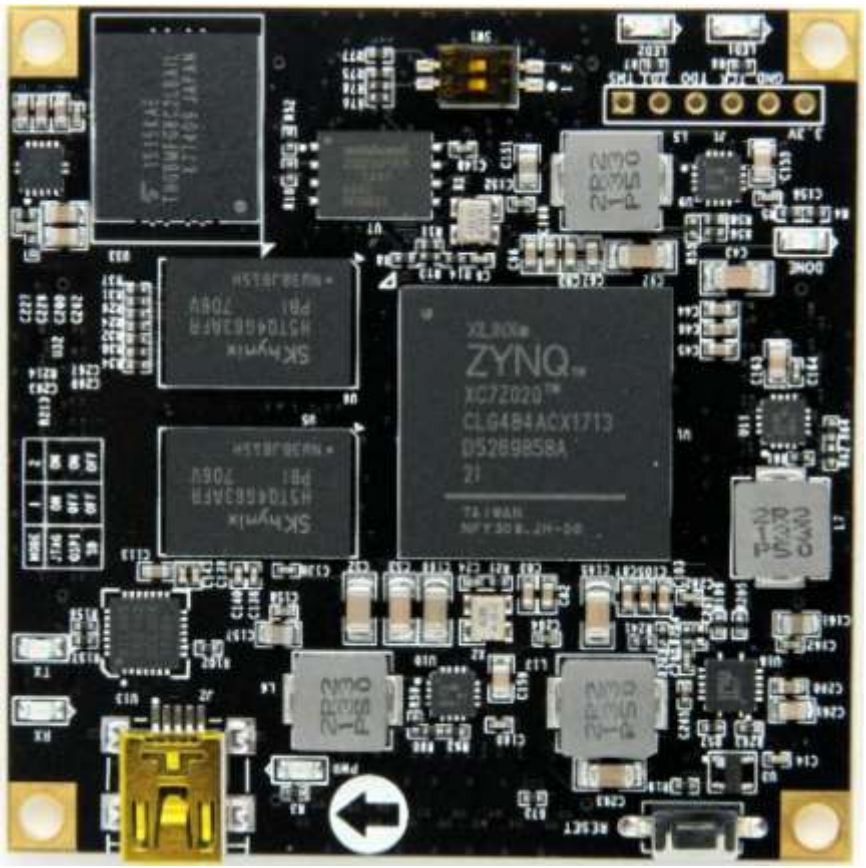

Figure 1-1: AC7021BCore board Front View

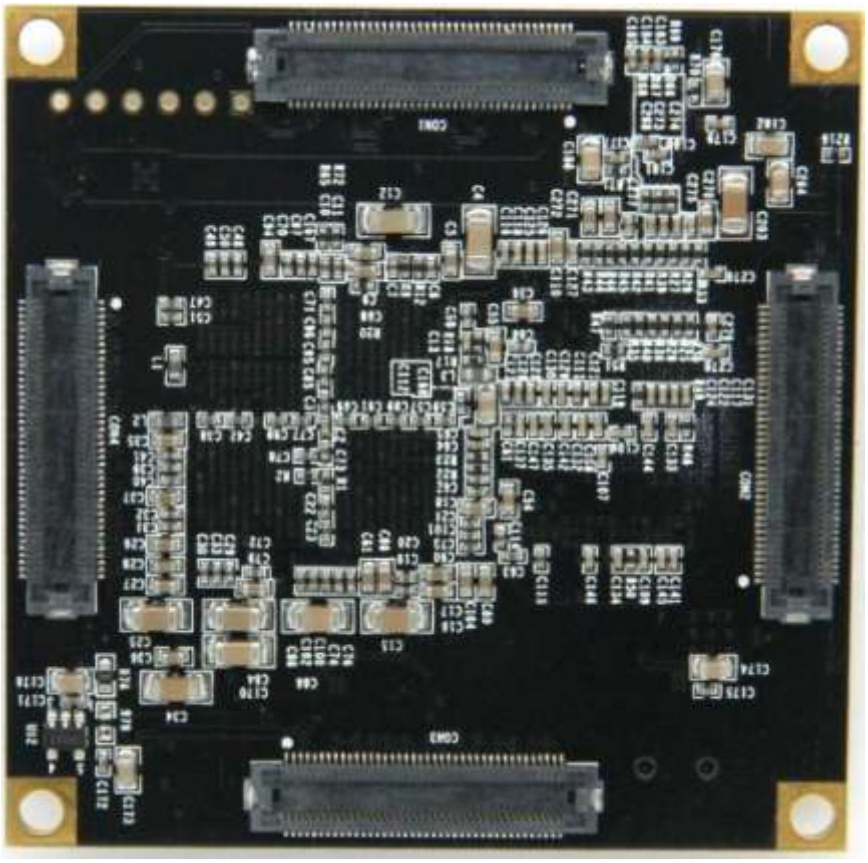

Figure 1-2:AC7021B core board rear view

Part 2: ZYQN Chip

The development board uses Xilinx's Zynq7000 series chip, model XC7Z020-2CLG484I. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO, etc. The PS can operate independently and start up at power up or reset. Figure 2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

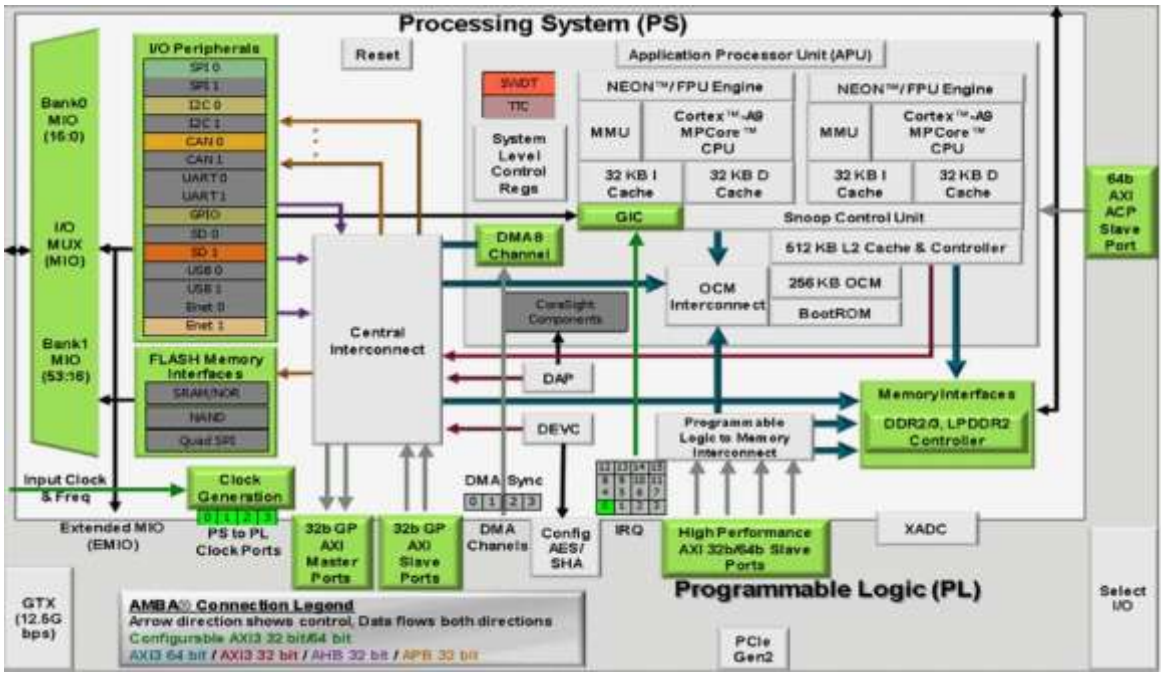

Figure 2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 1GHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII,

SGMII interface

- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 groups of 32bit GPIO, 54 (32+22) as PS system IO, 64 connected to PL
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- LogicCells: 85K
- Look-up-tables (LUTs):53,200
- Flip-flops:106,400
- 18x25MACCs：220;
- BlockRAM：4.9Mb
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z020-2CLG484I chip speed grade is -2, industrial grade, package is BGA484, pin pitch is 0.024 inch, the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2

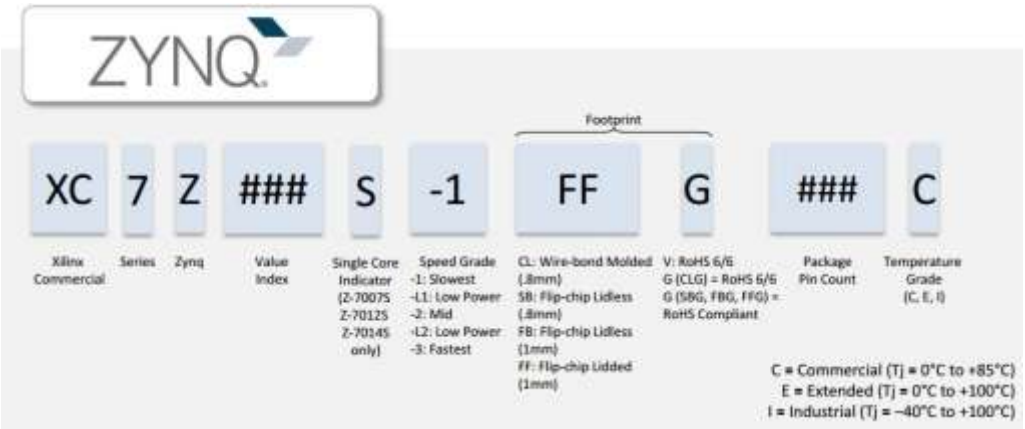

Figure 2-2: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-3: TheXC7Z020 chip used on the Core Board

Part 3 DDR3 DRAM

The AC7021B core board is equipped with two SK Hynix DDR3 SDRAM chips (1GB total), model H5TQ4G63AFR-PBI. The bus width of DDR3 SDRAM is 32 bits in total. DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 3-1

Bit Number	Chip Model	Capacity	Factory
U5,U6	H5TQ4G63AFR-PBI	256M x 16bit	SK Hynix

Table 3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 3-1:

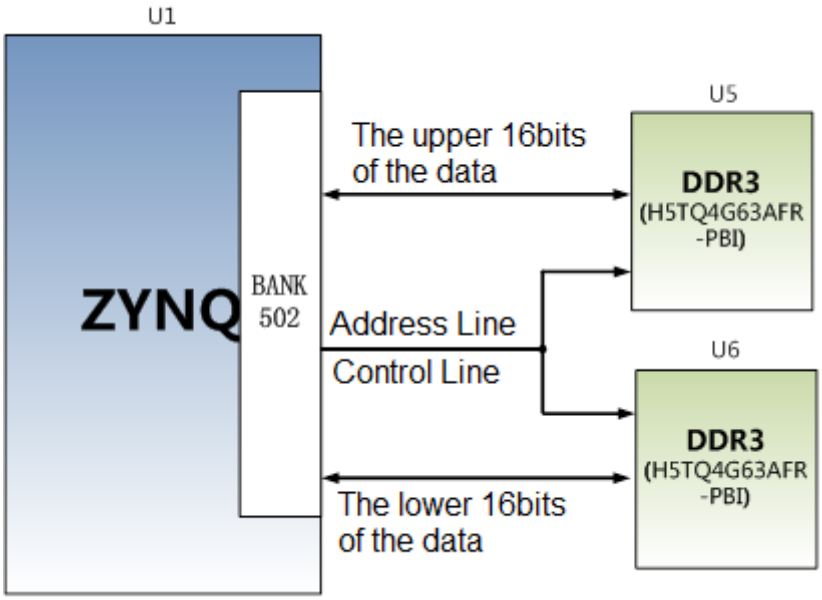

Figure 3-1: The Schematic part of DDR3 DRAM

Figure 3-2: DDR3 DRAM on the Core Board

DDR3 DRAM Pin Assignment

Signal Name	ZYNQ Pin Name	Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	D2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	J2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	P2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	V2
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W2
DDR3_D0	PS_DDR_DQ0_502	D1
DDR3_D1	PS_DDR_DQ1_502	C3
DDR3_D2	PS_DDR_DQ2_502	B2
DDR3_D3	PS_DDR_DQ3_502	D3
DDR3_D4	PS_DDR_DQ4_502	E3
DDR3_D5	PS_DDR_DQ5_502	E1
DDR3_D6	PS_DDR_DQ6_502	F2
DDR3_D7	PS_DDR_DQ7_502	F1
DDR3_D8	PS_DDR_DQ8_502	G2
DDR3_D9	PS_DDR_DQ9_502	G1
DDR3_D10	PS_DDR_DQ10_502	L1
DDR3_D11	PS_DDR_DQ11_502	L2
DDR3_D12	PS_DDR_DQ12_502	L3
DDR3_D13	PS_DDR_DQ13_502	K1
DDR3_D14	PS_DDR_DQ14_502	J1
DDR3_D15	PS_DDR_DQ15_502	K3
DDR3_D16	PS_DDR_DQ16_502	M1
DDR3_D17	PS_DDR_DQ17_502	T3
DDR3_D18	PS_DDR_DQ18_502	N3
DDR3_D19	PS_DDR_DQ19_502	T1
DDR3_D20	PS_DDR_DQ20_502	R3
DDR3_D21	PS_DDR_DQ21_502	T2
DDR3_D22	PS_DDR_DQ22_502	M2
DDR3_D23	PS_DDR_DQ23_502	R1
DDR3_D24	PS_DDR_DQ24_502	AA3
DDR3_D25	PS_DDR_DQ25_502	U1
DDR3_D26	PS_DDR_DQ26_502	AA1
DDR3_D27	PS_DDR_DQ27_502	U2
DDR3_D28	PS_DDR_DQ28_502	W1
DDR3_D29	PS_DDR_DQ29_502	Y3
DDR3_D30	PS_DDR_DQ30_502	W3
DDR3_D31	PS_DDR_DQ31_502	Y1
DDR3_DM0	PS_DDR_DM0_502	B1
DDR3_DM1	PS_DDR_DM1_502	H3
DDR3_DM2	PS_DDR_DM2_502	P1
DDR3_DM3	PS_DDR_DM3_502	AA2
DDR3_A0	PS_DDR_A0_502	M4
DDR3_A1	PS_DDR_A1_502	M5
DDR3_A2	PS_DDR_A2_502	K4
DDR3_A3	PS_DDR_A3_502	L4
DDR3_A4	PS_DDR_A4_502	K6
DDR3_A5	PS_DDR_A5_502	K5
DDR3_A6	PS_DDR_A6_502	J7
DDR3_A7	PS_DDR_A7_502	J6
DDR3_A8	PS_DDR_A8_502	J5

DDR3_A9	PS_DDR_A9_502	H5
DDR3_A10	PS_DDR_A10_502	J3
DDR3_A11	PS_DDR_A11_502	G5
DDR3_A12	PS_DDR_A12_502	H4
DDR3_A13	PS_DDR_A13_502	F4
DDR3_A14	PS_DDR_A14_502	G4
DDR3_BA0	PS_DDR_BA0_502	L7
DDR3_BA1	PS_DDR_BA1_502	L6
DDR3_BA2	PS_DDR_BA2_502	M6
DDR3_S0	PS_DDR_CS_B_502	P6
DDR3_RAS	PS_DDR_RAS_B_502	R5
DDR3_CAS	PS_DDR_CAS_B_502	P3
DDR3_WE	PS_DDR_WE_B_502	R4
DDR3_ODT	PS_DDR_ODT_502	P5
DDR3_RESET	PS_DDR_DRST_B_502	F3
DDR3_CLK0_P	PS_DDR_CKP_502	N4
DDR3_CLK0_N	PS_DDR_CKN_502	N5
DDR3_CKE	PS_DDR_CKE_502	V3

Table 3-2: DDR3 DRAM Pin Assignment

Part 4 QSPI Flash

The core board is equipped with a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U7	W25Q256FVEI	32M Byte	Winbond

Table 4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 4-1 shows the QSPI Flash in the schematic.

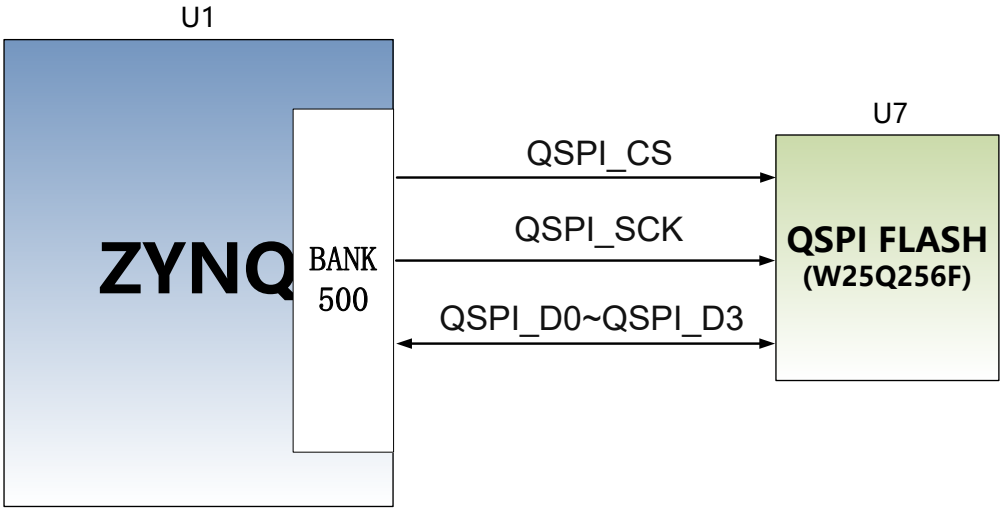

Figure 4-1: QSPI Flash in the schematic

Figure 4-2: QSPI Flash on the Core Board

Pin Assignment of QSPI Flash

Signal Name	ZYNQ Pin Name	Pin Number
QSPI_SCK	PS_MIO6_500	A4
QSPI_CS	PS_MIO1_500	A1
QSPI_D0	PS_MIO2_500	A2
QSPI_D1	PS_MIO3_500	F6
QSPI_D2	PS_MIO4_500	E4
QSPI_D3	PS_MIO5_500	A3

Table 4-2: Pin Assignment of QSPI FLASH

Part 5: eMMC Flash

The core board is equipped with a large capacity 32GB eMMC FLASH chip, model THGBMFG8C2LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the

eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM-based applications, system files, and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 5-1：

Position	Model	Capacity	Factory
U33	THGBMFG8C2LBAIL	32G Byte	TOSHIBA

Table 5-1: eMMC FLASH Specification

eMMC FLASH is connected to the GPIO port of the BANK501 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 5-1 shows the eMMC Flash in the schematic.

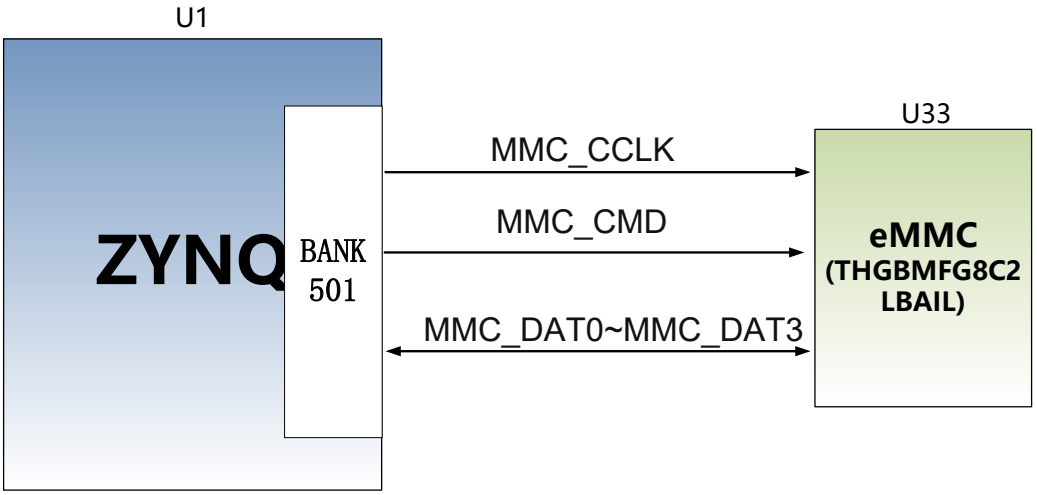

Figure 5-1: eMMC Flash in the Schematic

Figure 5-2: eMMC Flash on the Core Board

Pin Assignment of eMMC Flash

Signal Name	ZYNQ Pin Name	Pin Number
MMC_CCLK	PS_MIO48_501	D11
MMC_CMD	PS_MIO47_501	B10
MMC_D0	PS_MIO46_501	D12
MMC_D1	PS_MIO49_501	C14
MMC_D2	PS_MIO50_501	D13
MMC_D3	PS_MIO51_501	C10

Table 5-2: Pin Assignment of eMMC FLASH

Part 6: Clock configuration

The AC7021B core board provides active clocks for the PS system and the PL logic sections, respectively, so that the PS system and the PL logic can work independently.

PS system clock source

The ZYNQ chip provides a 33.333 MHz clock input to the PS section through the X1 crystal on the development board. The input of the clock is connected to the pins of PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 6-1:

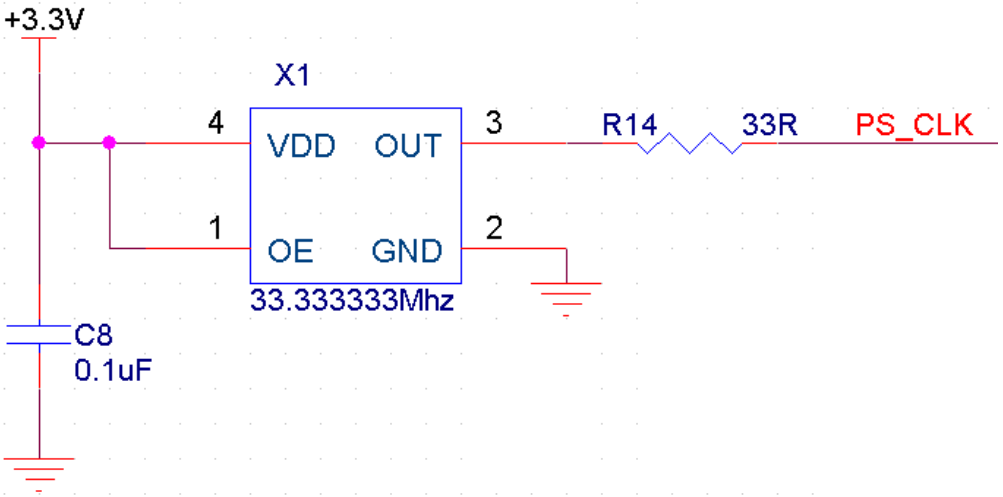

Figure 6-1: Active crystal oscillator to the PS section

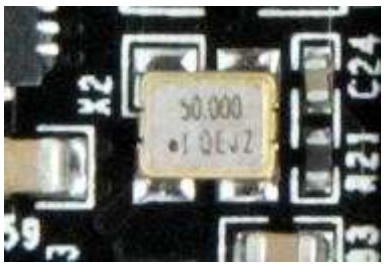

Figure 6-2: 33.333Mhz active Crystal Oscillator on the Core Board

PS Clock pin assignment:

Signal Name	Pin
PS_CLK_500	F7

Table 6-1: PS Clock pin assignment

PL system clock source

The AC7021B core board provides a single-ended 50MHz PL system clock source with 3.3V power supply. The crystal output is connected to the global clock (MRCC) of the FPGA BANK13, which can be used to drive user logic within the FPGA. The schematic diagram of the clock source is shown in Figure 6-3:

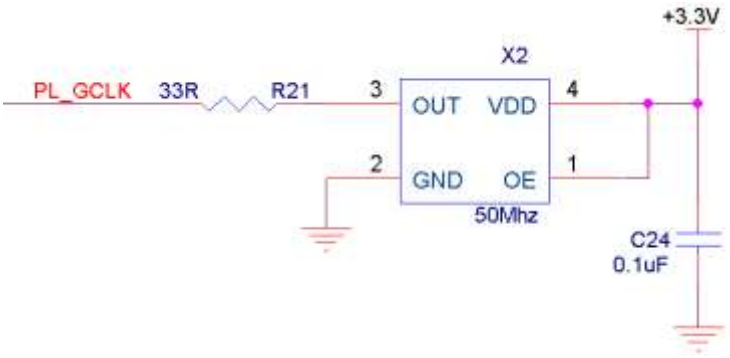

Figure 6-3: PL system clock source

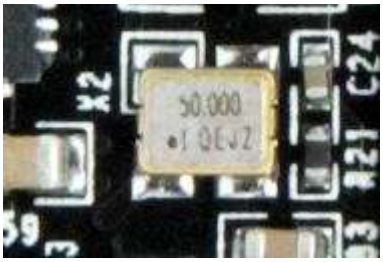

Figure 6-4: 50Mhz active crystal oscillator on the Core Board

PL Clock pin assignment:

Signal Name	Pin
PL_GCLK	Y9

Table 6-2: PL Clock pin assignment

Part 7: USB to serial port

For the AC7021B core board to work and debug separately, we have a Uart to USB interface for the core board. Used for separate power supply and debugging of the core board. The conversion chip uses the USB-UART chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

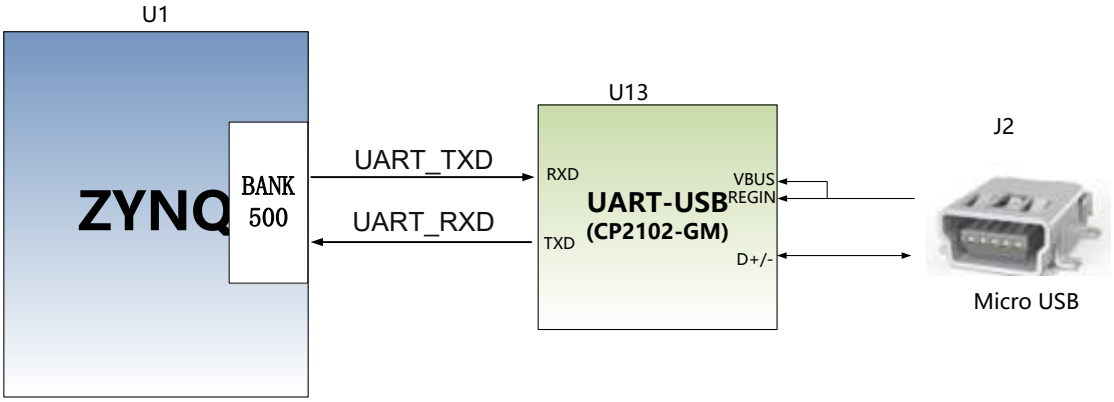

Figure 7-1: USB to Serial Port

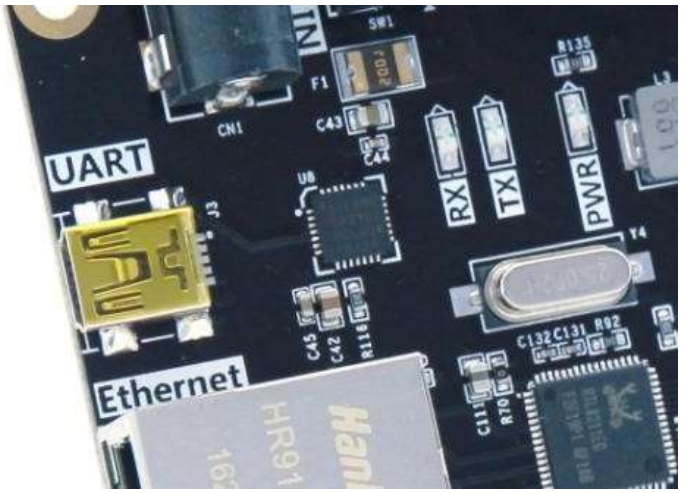

Figure 7-2: USB to Serial Port on the Core Board

At the same time, two LED indicators are set on the serial port signal, and the LEDs on the PCB are printed as RX and TX LEDs (D5 and D6). The RX and TX LEDs indicate whether the serial port has data received or sent, as shown in the Figure 7-3 below.

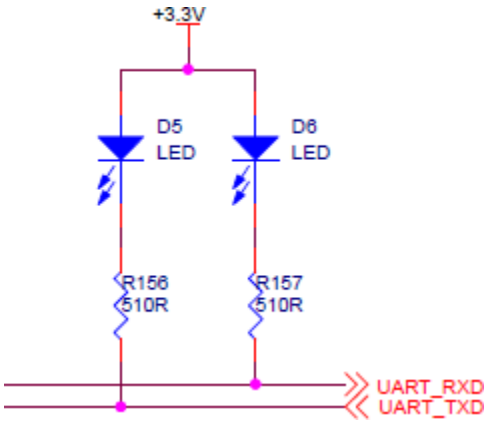

Figure 7-3: USB to serial port signal indicator

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO14_500	B6	Uart data output
UART_TXD	PS_MIO15_500	E6	Uart data input

Table 7-1: Uart Pin Assignment

Part8: LED

There are 6 red LED lights on the AC7021B core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), two are

the user LED lights (LED1~LED2), and the other two are the UART transmit and receive indicators (TX, RX). When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. Two user LED lights are connected to the MIO of the PS, one is connected to the IO of the PL, the user can control the lighting and off by the program, when the IO voltage connected to the user LED light is high, the user LED light is off. When the connection IO voltage is low, the user LED will be illuminated. The schematic diagram of the LED light hardware connection is shown in Figure 8-1:

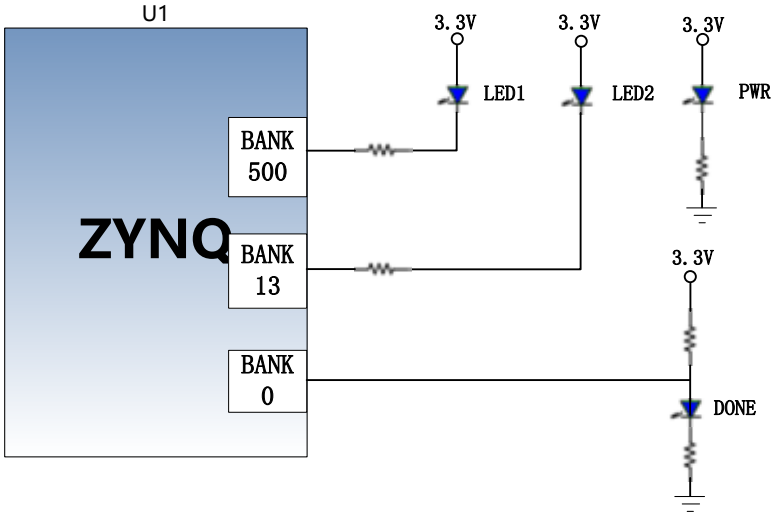

Figure 8-1: The schematic diagram of the LED light hardware connection

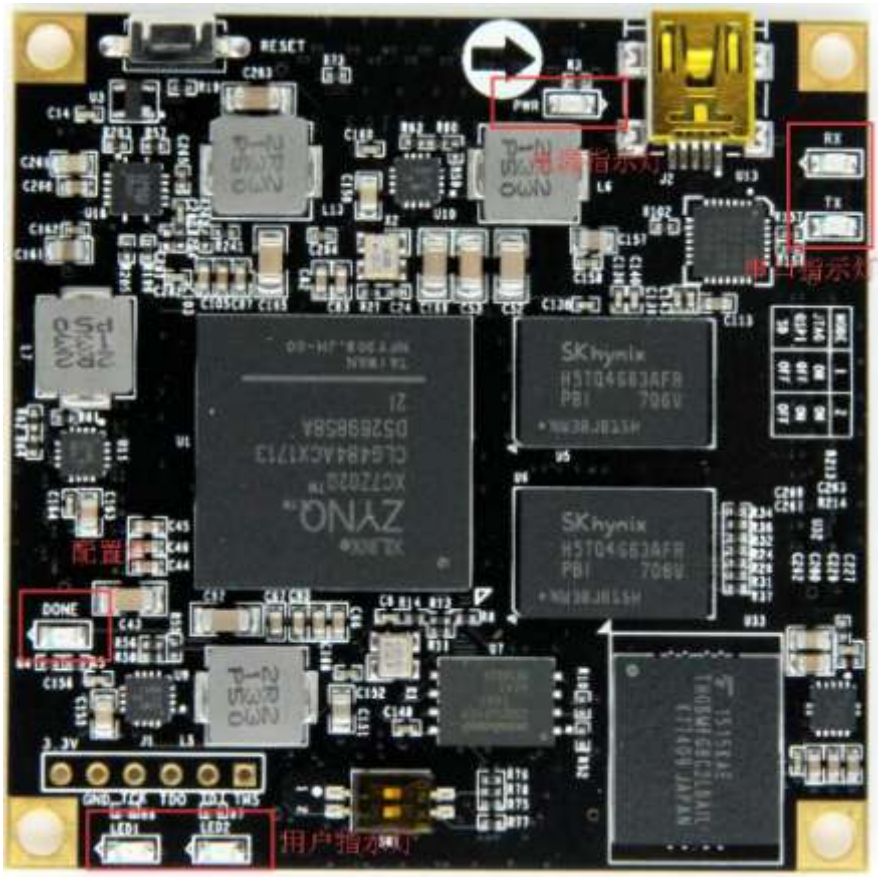

Figure 8-2: The LEDs on the Core Board

LED Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
MIO0_LED	PS_MIO0_500	G6	User LED1
PL_LED	IO_0_13	R7	User LED2

Table 8-1: LED Pin Assignment

Part 9: Reset button

The AC7021B has a reset button RESET and circuitry on the core board. The reset signal is connected to the PS reset pin of the ZYNQ chip. The reset button can be used by the user to reset the ZYNQ system. When the reset button is pressed, the reset chip will generate a low level reset signal to the ZYNQ chip. The schematic diagram of the reset button and reset chip connection is shown in Figure 9-1:

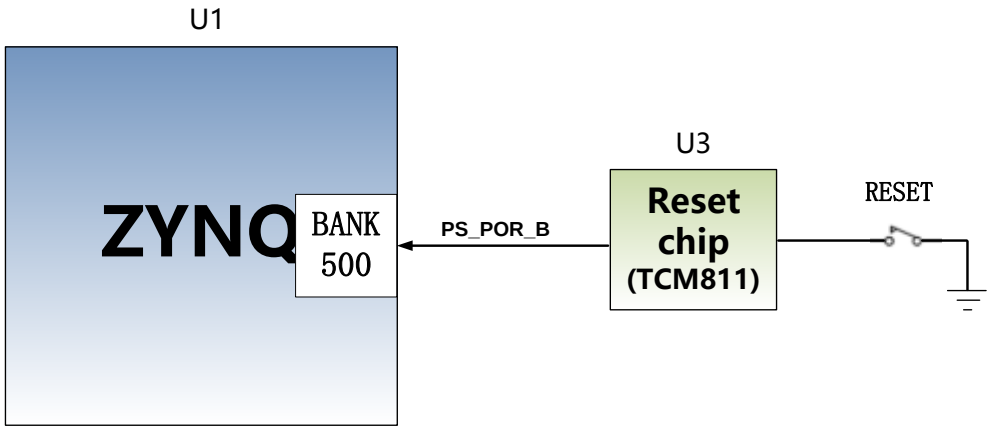

Figure 9-1: Reset button connection diagram

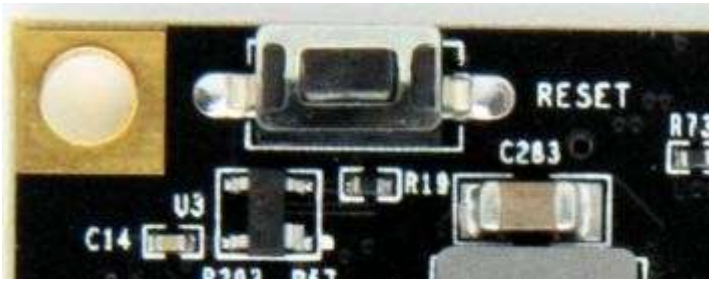

Figure 9-2: Reset Button on the Core Board

Reset Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PS_POR_B	PS_POR_B_500	B5	Reset Key

Table 9-1: Reset Pin Assignment

Part 10: JTAGE Interface

The JTAG test socket J1 is reserved on the AC7021B core board for separate JTAG download and debugging of the core board. Figure 10-1 is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK, GND. , +3.3V these six signals.

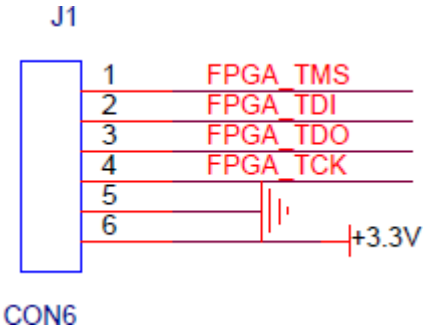

Figure 10-1: JTAG interface part of the core board schematic

The JTAG interface J1 on the core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connection to debug on the core board, you need to solder a 6-pin single-row pin header. Figure 10-2 shows the physical map of the JTAG interface on the development board.

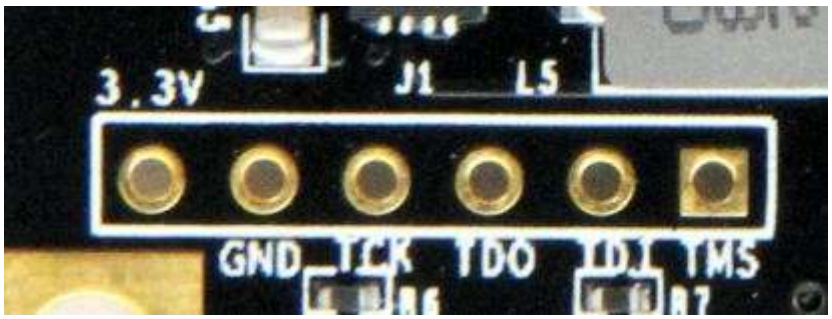

Figure 10-2: JTAG interface on the core board

Part 11: DIP switch configuration

The AC7021B has a 2-digit DIP switch SW1 on the core board to configure the ZYNQ system's startup mode. The AC7021B system development platform supports three startup modes. The three startup modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the XC7Z020 chip is powered up, it will detect the level of the MIO port (MIO5 and MIO4) to determine which startup mode. Users can select different startup modes through the DIP switch SW1 on the core board. The SW1 startup mode configuration is shown in Table 11-1

SW1	Position（1，2）	MIO5,MIO4 Level	Startup mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 11-1: The SW1 Startup Mode Configuration

Part 12: Power

The AC7021B core board is powered by DC5V. It is powered by the Mini USB interface when it is used alone. It is powered by the extension board when the backplane is connected. Please be careful not to supply power to the Mini

USB and the extension board at the same time to avoid damage. The power supply design on the core board is shown in Figure 12-1.

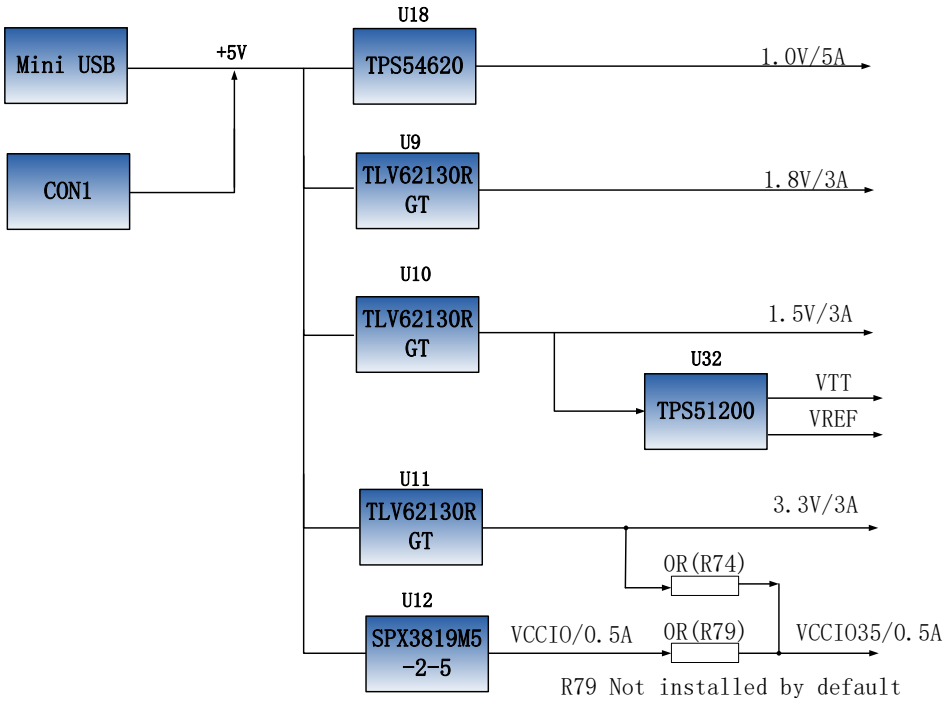

Figure 12-1: The Power Supply Design on the Core Board

The development board is powered by +5V, and is converted into +1.0V, +1.8V, +1.5V, +3.3V four-way power supply through four-way DC/DC power supply core TPS54620TLV62130RGT. The output current of +1.0V can be as high as 5A, and the other three output current are 3A. The VCCIO 2.5V power supply is generated by one LDO SPX3819M5-2-5. The VCCIO 2.5V power supply is mainly reserved for the BANK power supply of the BANK33 of the FPGA. The user can select the power supply of BANK33 and BANK34 through two 0 ohm resistors (R74, R79). By default, the R74 on the development board is installed, and the resistor of R79 is not installed, so the power supply of BANK33 and BANK34 is +3.3V. The user can replace the resistor so that the IO of the BANK33, 34 outputs a voltage standard of 2.5V. 1.5V generates the VTT and VREF voltages required by DDR3 through TI's TPS51200. The functions of each power distribution are shown in the following Table 12-1:

Power	Function
+1.0V	ZYNQ PS and PL section core voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage, BANK501 IO voltage, eMMC
+3.3V	ZCNQ Bank0, Bank500, Bank13, Bank35, VCCIO,QSIP FLASH, Clock Crystal
+1.5V	DDR3, ZYNQ Bank501
VREF,VTT（+0.75V	DDR3
VCCIO(+2.5V)	Reserved for ZYNQ Bank33,Bank 34

Table 12-1: The Functions of Each Power Distribution

Because the power supply of ZYNQ FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO). The circuit design ensures the normal operation of the chip. The power supply on the core board detailed as Figure 12-2 below

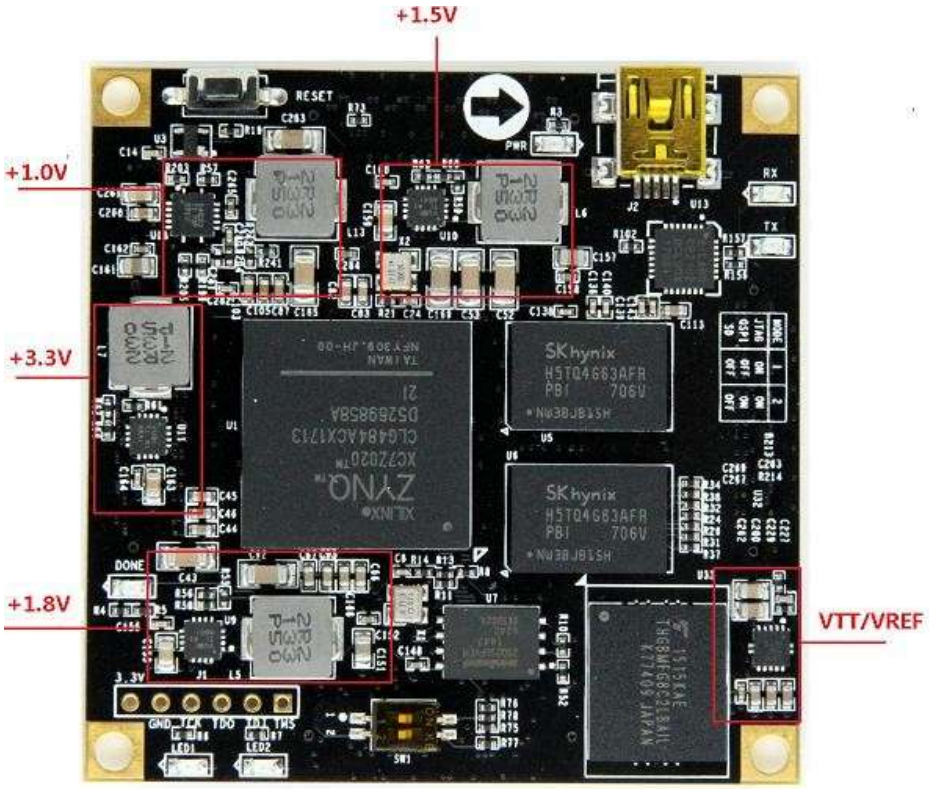

Figure 12-2: The Power Supply on the Core Board

Part 13 Structure diagram:

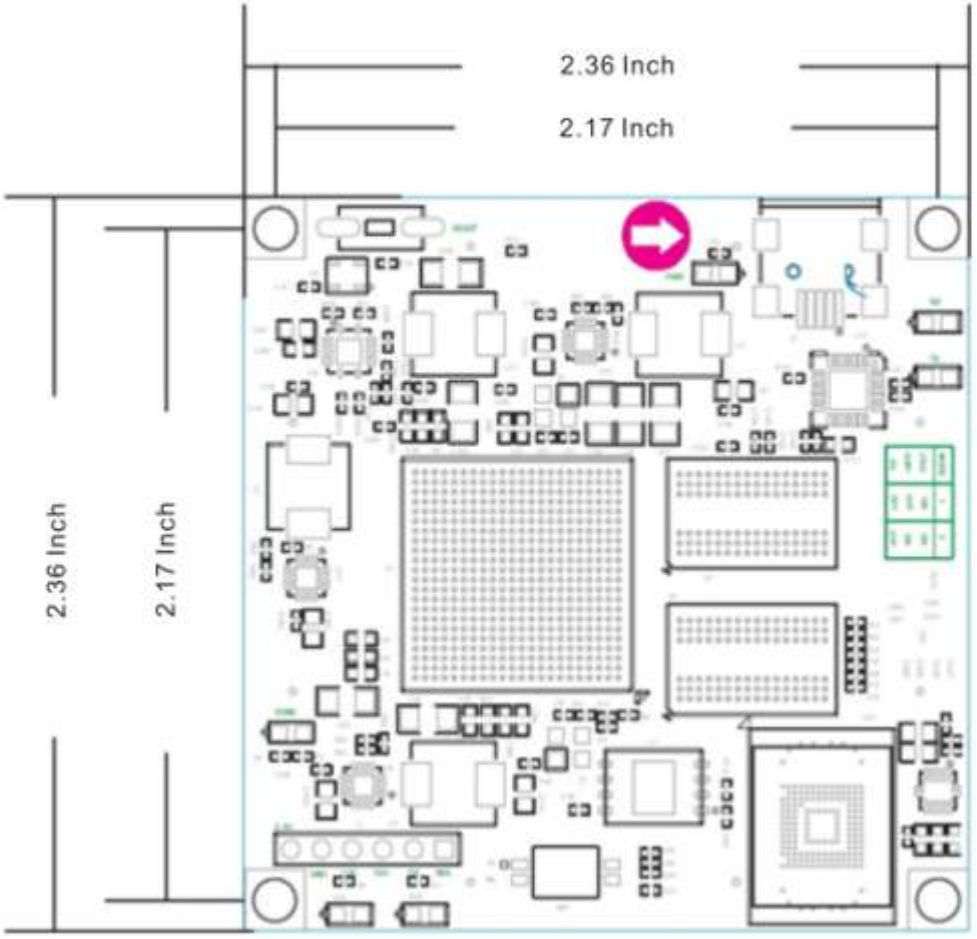

Figure 13-1: The Structure diagram （Top View）

Part 14: Connector pin definition

The core board expands four high-speed carrier ports, and uses four 80Pin inter-board connectors (CON1~CON4) to connect with the backplane. The PIN pitch of the connector is 0.5mm. Among them, CON1 is connected to the power input, the MIO signal of the PS and the JTAG signal, and CON2~CON4 are connected to the IO signals of BANK13, BANK33, BANK34, BANK35 of PL. The IO levels of BANK33 and BANK34 can be changed by changing the level of the LDO chip (U12) on the board. The default is 3.3V. Pin assignment detailed as Table 14-1, Table 14-2, Table 14-3, Table 14-4:

CON1 Pin	Signal Name	ZYNQ Pin	CON1 Pin	Signal Name	ZYNQ Pin
1	+5V	-	2	+5V	-
3	+5V	-	4	+5V	-
5	+5V	-	6	+5V	-
7	+5V	-	8	+5V	-
9	GND	-	10	GND	-
11	PS_MIO13	A6	12	ETH_TXD0	E9
13	PS_MIO12	C5	14	ETH_TXD1	A7
15	-	-	16	ETH_TXD2	E10
17	-	-	18	ETH_TXD3	A8
19	GND	-	20	GND	-
21	-	-	22	ETH_TXCK	D6
23	-	-	24	ETH_TXCTL	F11
25	-	-	26	ETH_RXD3	A13
27	-	-	28	ETH_RXD2	F12
29	GND	-	30	GND	-
31	PS_MIO7	D5	32	ETH_RXD1	B7
33	PS_MIO8	E5	34	ETH_RXD0	E11
35	PS_MIO9	C4	36	ETH_RXCTL	D7
37	PS_MIO11	B4	38	ETH_RXCK	A14
39	GND	-	40	GND	-
41	-	-	42	ETH_MDC	D10
43	-	-	44	ETH_MDIO	C12
45	-	-	46	OTG_STP	A11
47	-	-	48	OTG_DIR	E8
49	GND	-	50	GND	-
51	XADC_VP	L11	52	OTG_CLK	A9
53	XADC_VN	M12	54	OTG_NXT	F9
55	-	-	56	OTG_DATA0	C7
57	PS_MIO10	G7	58	OTG_DATA1	G13
59	GND	-	60	GND	-
61	SD_CLK	E14	62	OTG_DATA2	B12

63	SD_D1	B11	64	OTG_DATA3	F14
65	SD_D0	D8	66	OTG_DATA4	A12
67	SD_CMD	C8	68	OTG_DATA5	B14
69	GND	-	70	GND	-
71	SD_D3	B9	72	OTG_DATA6	F13
73	SD_D2	E13	74	OTG_DATA7	C13
75	-	-	76	-	-
77	FPGA_TMS	G12	78	FPGA_TCK	G11
79	FPGA_TDO	G14	80	FPGA_TDI	H13

Table 14-1: Pin Assignment of CON1

CON2 Pin	Singal Name	ZYNQ Pin	CON2 Pin	Singal Name	ZYNQ Pin
1	B13_L1_N	V9	2	B33_L4_N	W21
3	B13_L1_P	V10	4	B33_L4_P	W20
5	B33_L10_P	AB19	6	B33_L3_N	W22
7	B33_L10_N	AB20	8	B33_L3_P	V22
9	GND	-	10	GND	-
11	B13_L4_N	W12	12	B33_L2_N	U22
13	B13_L4_P	V12	14	B33_L2_P	T22
15	B34_L6_N	M16	16	B13_L5_N	U11
17	B34_L6_P	M15	18	B13_L5_P	U12
19	GND	-	20	GND	-
21	B13_L12_N	Y8	22	B33_IO25	U14
23	B13_IO25	U7	24	B34_IO25	R15
25	B13_L23_N	W7	26	B13_L6_P	U10
27	B13_L23_P	V7	28	B13_L6_N	U9
29	GND	-	30	GND	-
31	B13_L13_N	Y5	32	B13_L19_N	T6
33	B13_L13_P	Y6	34	B13_L19_P	R6
35	B13_L24_N	W5	36	B13_L22_P	U6
37	B13_L24_P	W6	38	B13_L22_N	U5

39	GND	-	40	GND	-
41	B33_L11_P	Y19	42	B13_L20_P	T4
43	B33_L11_N	AA19	44	B13_L20_N	U4
45	B33_L5_P	U20	46	B13_L3_P	W11
47	B33_L5_N	V20	48	B13_L3_N	W10
49	GND	-	50	GND	-
51	B33_L1_P	T21	52	B13_L10_P	Y11
53	B33_L1_N	U21	54	B13_L10_N	Y10
55	B13_L7_P	AA12	56	B13_L2_P	V8
57	B13_L7_N	AB12	58	B13_L2_N	W8
59	GND	-	60	GND	-
61	B13_L8_N	AB11	62	B13_L14_P	AA7
63	B13_L8_P	AA11	64	B13_L14_N	AA6
65	B13_L9_N	AB9	66	B13_L16_P	AB5
67	B13_L9_P	AB10	68	B13_L16_N	AB4
69	GND	-	70	GND	-
71	B13_L11_N	AA8	72	B13_L18_N	AA4
73	B13_L11_P	AA9	74	B13_L18_P	Y4
75	B13_L17_N	AB6	76	B13_L15_N	AB1
77	B13_L17_P	AB7	78	B13_L15_P	AB2
79	B13_L21_N	V4	80	B13_L21_P	V5

Table 14-2: Pin Assignment of CON2

CON3 Pin	Signal Name	ZYNQ Pin	CON3 Pin	Signal Name	ZYNQ Pin
1	B34_L2_P	J16	2	B34_L12_N	L19
3	B34_L2_N	J17	4	B34_L12_P	L18
5	B34_L11_P	K19	6	B34_L10_N	L22
7	B34_L11_N	K20	8	B34_L10_P	L21
9	GND	-	10	GND	-
11	B34_L7_P	J18	12	B34_L3_N	L16
13	B34_L7_N	K18	14	B34_L3_P	K16

15	B34_L1_P	J15	16	B34_L15_N	N22
17	B34_L1_N	K15	18	B34_L15_P	M22
19	GND	-	20	GND	-
21	B34_L17_P	R20	22	B34_L16_P	N22
23	B34_L17_N	R21	24	B34_L16_N	P22
25	B34_L14_N	N20	26	B34_L20_N	P18
27	B34_L14_P	N19	28	B34_L20_P	P17
29	GND	-	30	GND	-
31	B34_L5_N	N18	32	B34_L13_P	M19
33	B34_L5_P	N17	34	B34_L13_N	M20
35	B33_L9_P	Y20	36	B34_L21_N	T17
37	B33_L9_N	Y21	38	B34_L21_P	T16
39	GND	-	40	GND	-
41	B33_L8_P	AA21	42	B33_L6_N	V19
43	B33_L8_N	AB21	44	B33_L6_P	V18
45	B33_L12_N	AA18	46	B33_L16_P	U17
47	B33_L12_P	Y18	48	B33_L16_N	V17
49	GND	-	50	GND	-
51	B33_L13_P	W17	52	B33_L17_N	AB17
53	B33_L13_N	W18	54	B33_L17_P	AA17
55	B33_L18_N	AB16	56	B33_L7_P	AA22
57	B33_L18_P	AA16	58	B33_L7_N	AB22
59	GND	-	60	GND	-
61	B33_L21_N	Y15	62	B33_L19_N	V15
63	B33_L21_P	W15	64	B33_L19_P	V14
65	B33_L24_P	AB14	66	B33_L15_N	U16
67	B33_L24_N	AB15	68	B33_L15_P	U15
69	GND	-	70	GND	-
71	B33_L23_N	AA13	72	B33_L14_P	W16
73	B33_L23_P	Y13	74	B33_L14_N	Y16
75	B33_L20_N	W13	76	B33_L22_P	Y14
77	B33_L20_P	V13	78	B33_L22_N	AA14

79	B34_IO0	H15	80	B33_IO0	U19

Table 14-3: Pin Assignment of CON3

CON4 Pin	Signal Name	ZYNQ Pin	CON4 Pin	Signal Name	ZYNQ Pin
1	B35_L7_N	B15	2	B35_L9_P	A16
3	B35_L7_P	C15	4	B35_L9_N	A17
5	B35_L8_P	B16	6	B35_L10_P	A18
7	B35_L8_N	B17	8	B35_L10_N	A19
9	GND	-	10	GND	-
11	B35_L11_N	C18	12	B35_L15_P	A21
13	B35_L11_P	C17	14	B35_L15_N	A22
15	B35_L13_N	B20	16	B35_L18_N	B22
17	B35_L13_P	B19	18	B35_L18_P	B21
19	GND	-	20	GND	-
21	B35_L14_N	C20	22	B35_L16_N	C22
23	B35_L14_P	D20	24	B35_L16_P	D22
25	B35_L12_P	D18	26	B35_L17_N	D21
27	B35_L12_N	C19	28	B35_L17_P	E21
29	GND	-	30	GND	-
31	B35_L2_N	D17	32	B35_L23_N	F22
33	B35_L2_P	D16	34	B35_L23_P	F21
35	B35_L1_N	E16	36	B35_L22_N	G21
37	B35_L1_P	F16	38	B35_L22_P	G20
39	GND	-	40	GND	-
41	B35_L21_P	E19	42	B34_L8_N	J22
43	B35_L21_N	F19	44	B34_L8_P	J21
45	B35_L24_P	H22	46	B35_L20_N	F19
47	B35_L24_N	G22	48	B35_L20_P	G19
49	GND	-	50	GND	-
51	B35_L6_P	G17	52	B35_L19_N	H20
53	B35_L6_N	F17	54	B35_L19_P	H19
55	B35_L4_P	G15	56	B34_L9_P	J20

57	B35_L4_N	G16	58	B34_L9_N	K21
59	GND	-	60	GND	-
61	B35_L3_N	D15	62	B35_IO25	H18
63	B35_L3_P	E15	64	B35_IO0	H17
65	B34_L24_N	R16	66	B34_L4_P	L17
67	B34_L24_P	P16	68	B34_L4_N	M17
69	GND	-	70	GND	-
71	B34_L23_P	R18	72	B34_L18_N	P21
73	B34_L23_N	T18	74	B34_L18_P	P20
75	B35_L5_P	F18	76	B34_L22_P	R19
77	B35_L5_N	E18	78	B34_L22_N	T19
79	B34_L19_P	N15	80	B34_L19_N	P15

Table 14-4: Pin Assignment of CON4