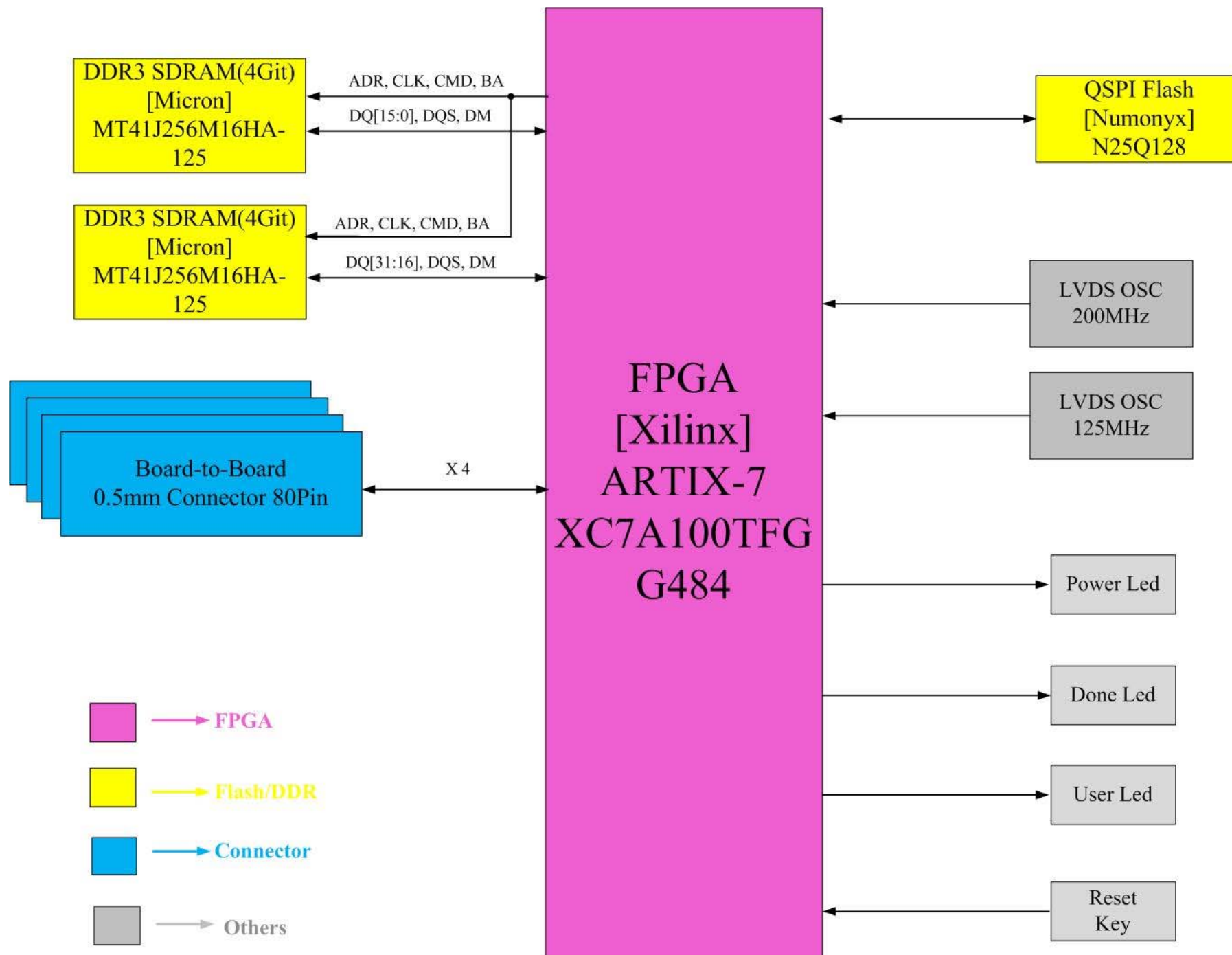


REV	Description	Date
V1.0	First Release	2018-3-06

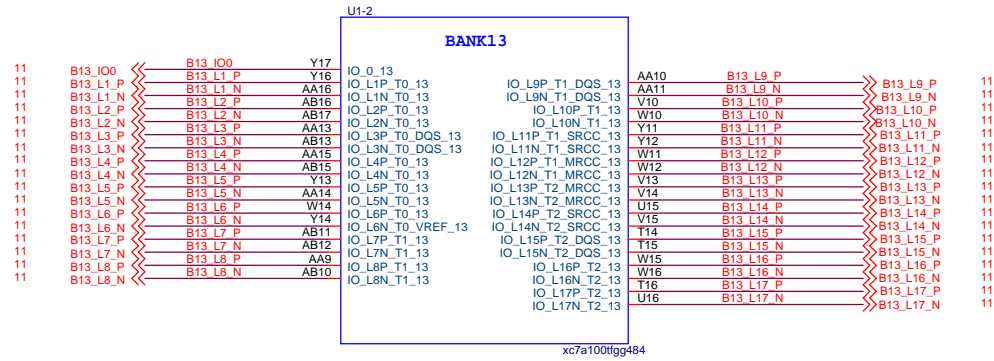
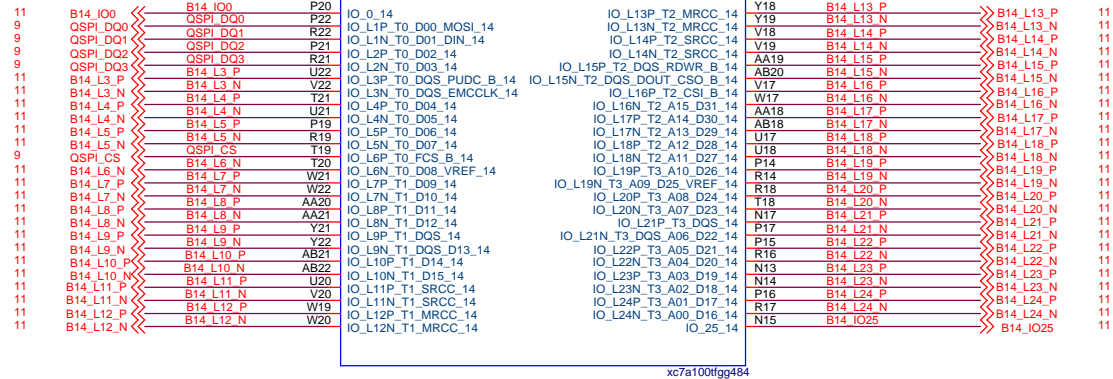
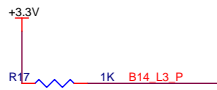
FPGA 核心板

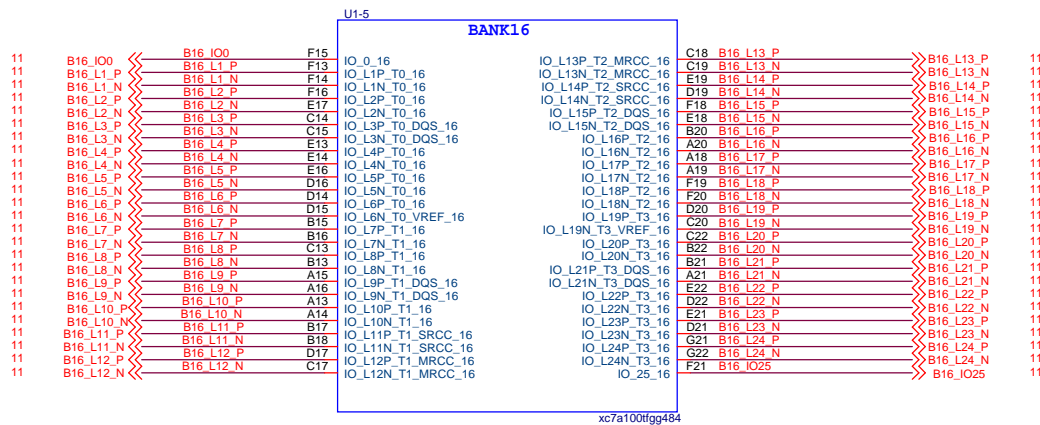
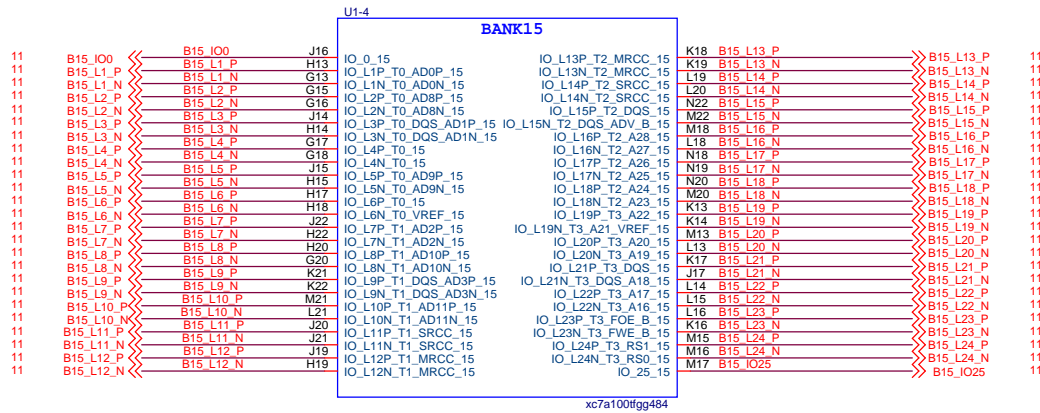
AC7100 Schematics

Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	FPGA BANK0
Page04	FPGA BANK13/14
Page05	FPGA BANK15/16
Page06	FPGA BANK34/35
Page07	FPGA BAN216
Page08	FPGA Power
Page09	DDR3
Page10	CLOCK&FLASH
Page11	POWER
Page12	Connector

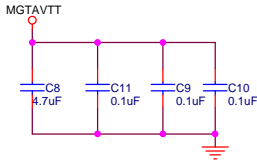


PUDC_B=1: Deactive internal Pull up Resister

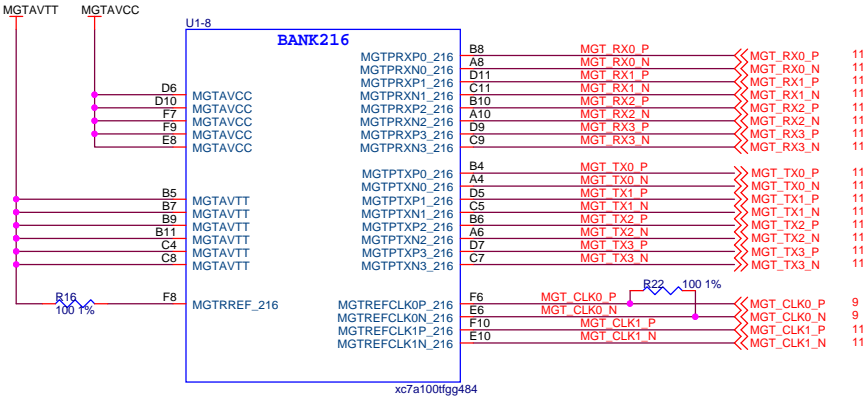
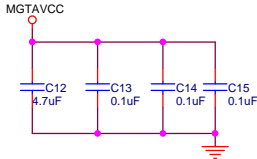


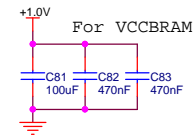
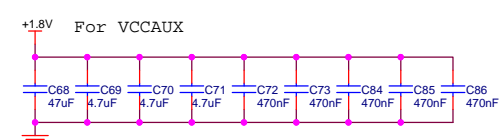
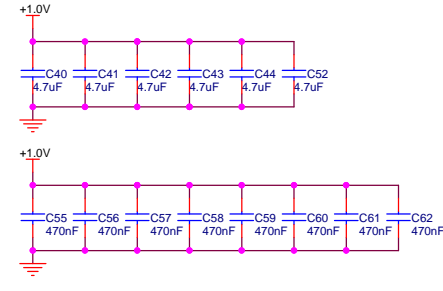
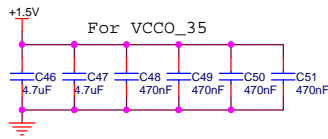
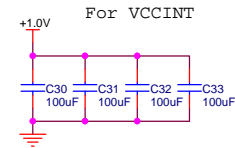
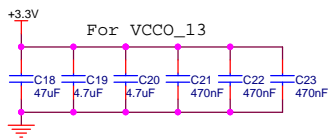


MGTAVTT 4.7uF(1) 0.1uF(2)

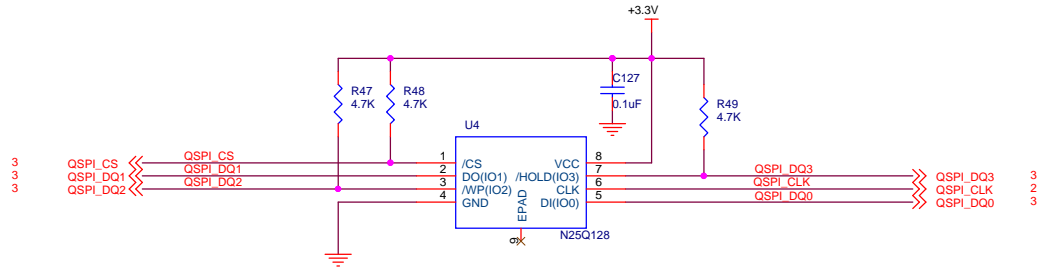


MGTAVCC 4.7uF(1) 0.1uF(2)



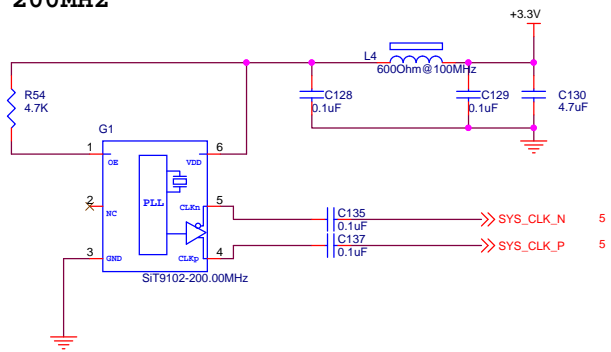


FPGA CONFIG SPI



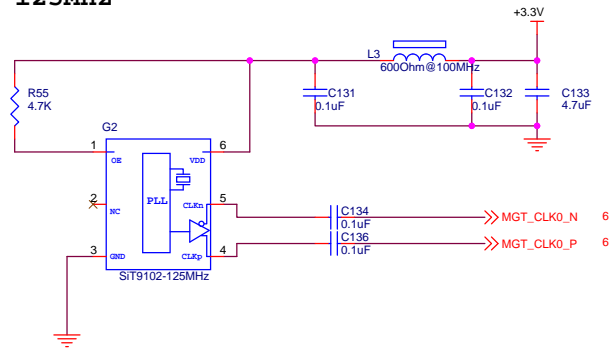
SYSTEM CLOCK

200MHz

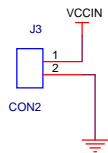


GTP CLOCK

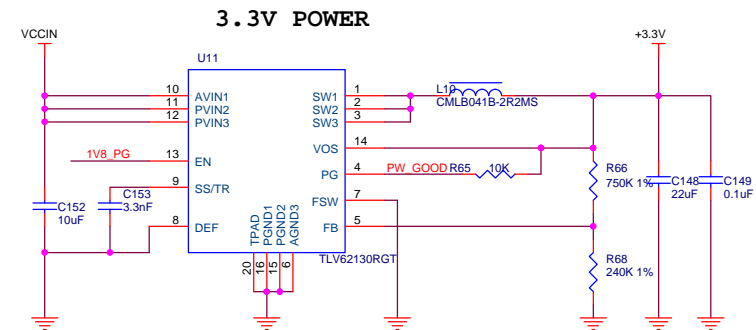
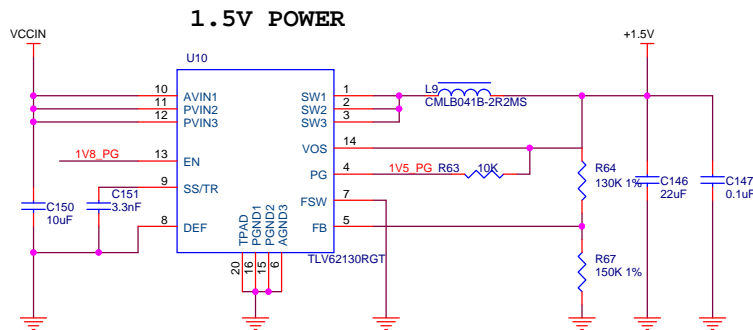
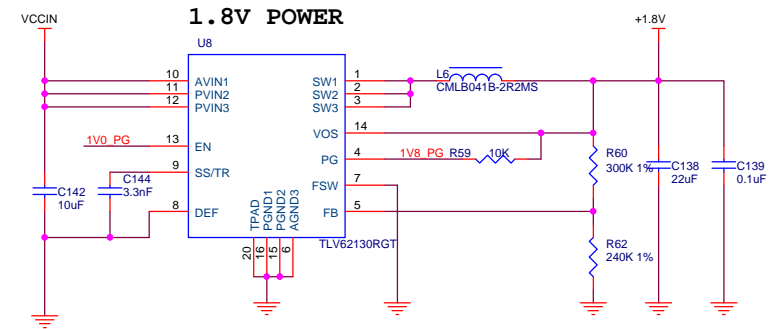
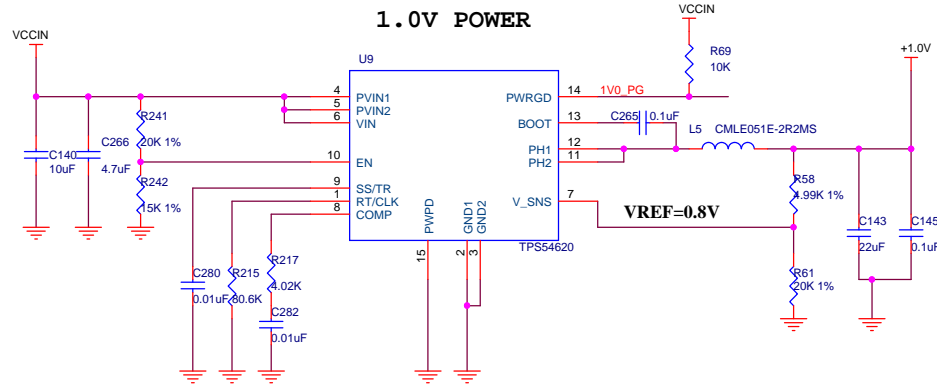
125MHz



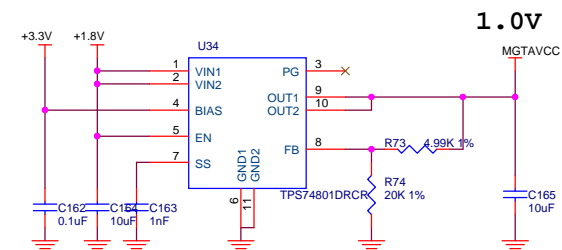
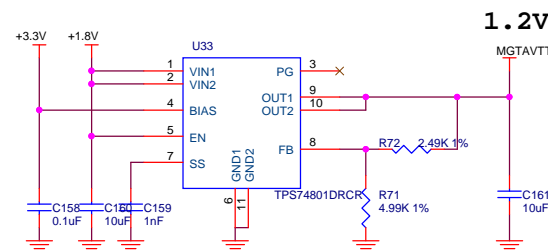
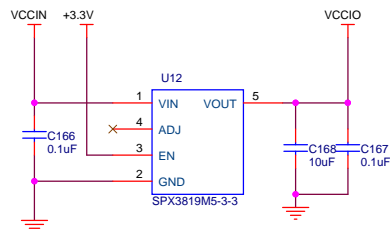
ALINX Confidential



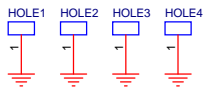
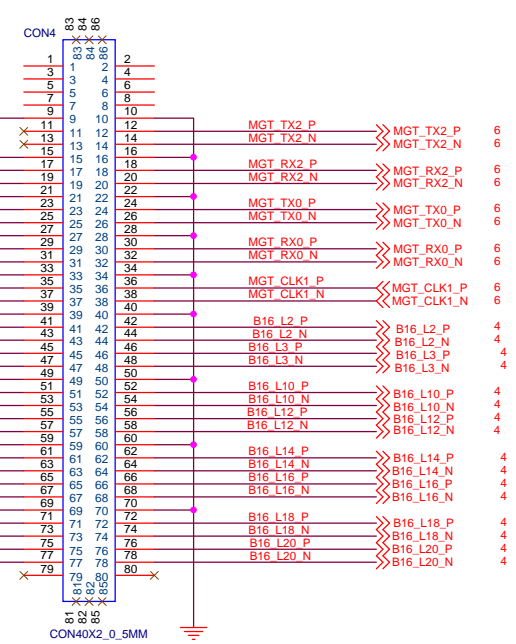
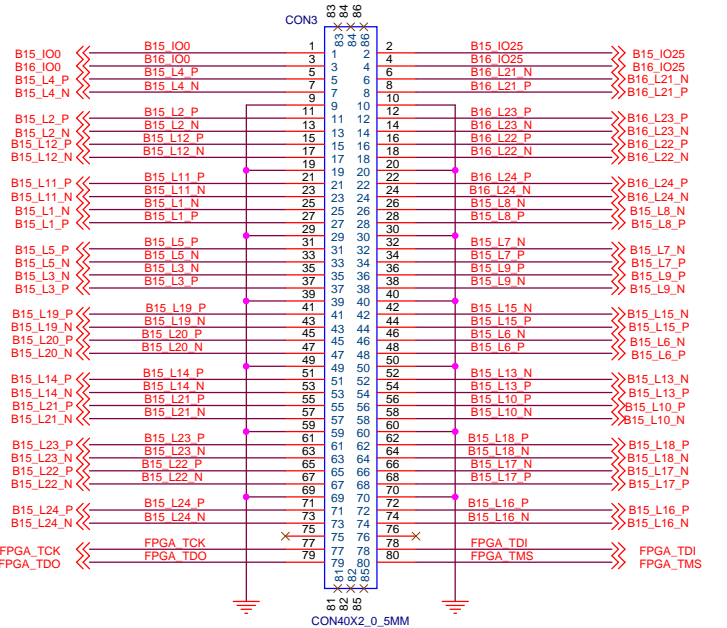
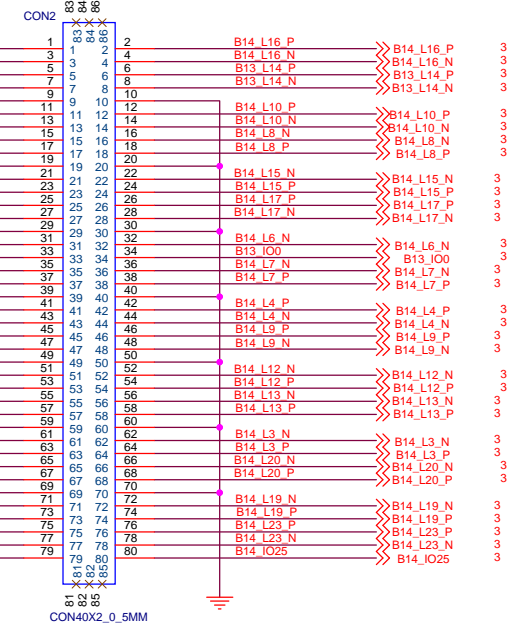
POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)



POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)



Pin	Label	Signal
1	B13_L16_P	P
2	B13_L16_N	N
3	B13_L15_P	P
4	B13_L15_N	N
5	B13_L13_P	P
6	B13_L13_N	N
7	B13_L12_P	P
8	B13_L12_N	N
9	B13_L11_P	P
10	B13_L11_N	N
11	B13_L10_P	P
12	B13_L10_N	N
13	B13_L9_P	P
14	B13_L9_N	N
15	B13_L8_P	P
16	B13_L8_N	N
17	B14_L11_N	N
18	B14_L11_P	P
19	B14_L14_N	N
20	B14_L14_P	P
21	B14_L5_N	N
22	B14_L5_P	P
23	B14_L18_N	N
24	B14_L18_P	P
25	B13_L17_P	P
26	B13_L17_N	N
27	B14_L21_N	N
28	B14_L21_P	P
29	B14_L22_P	P
30	B14_L22_N	N
31	B14_L24_N	N
32	B14_L24_P	P
33	B14_I00	I00



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