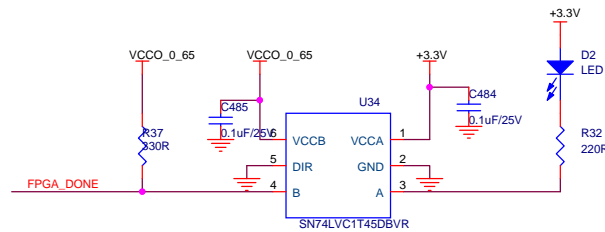
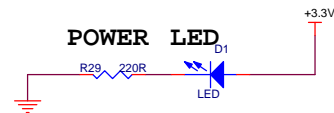


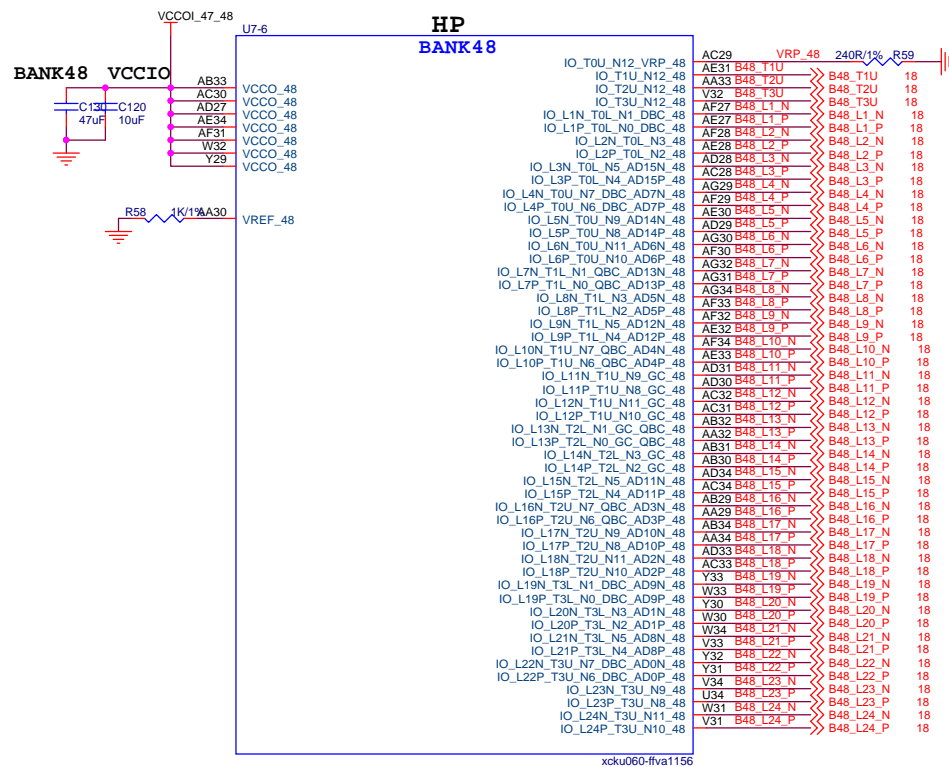
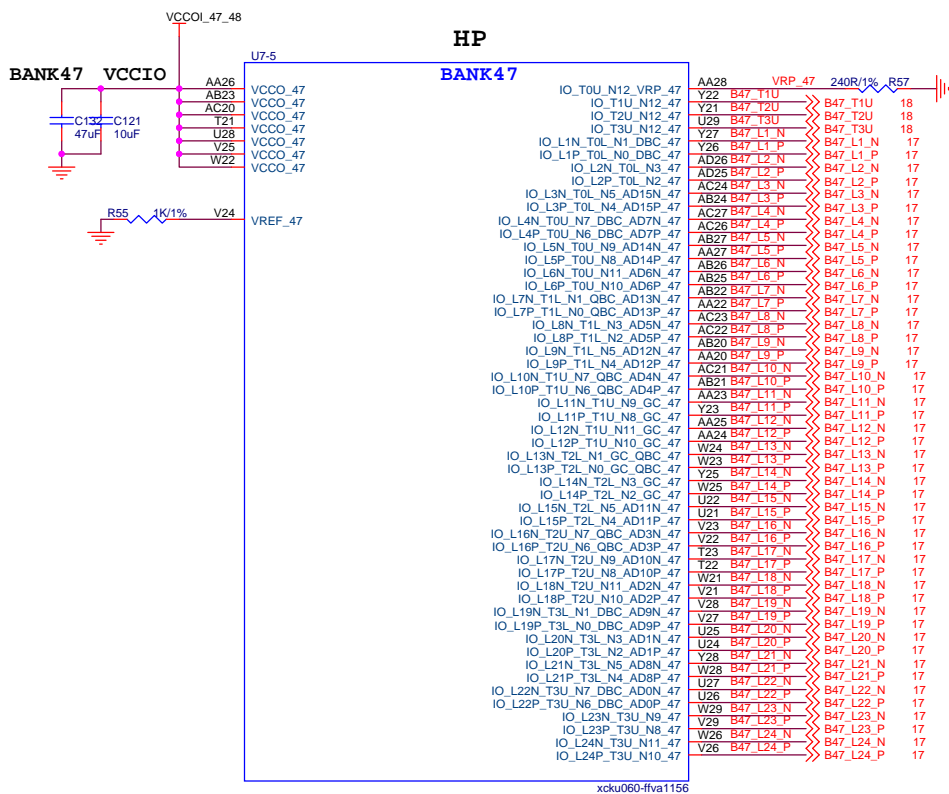
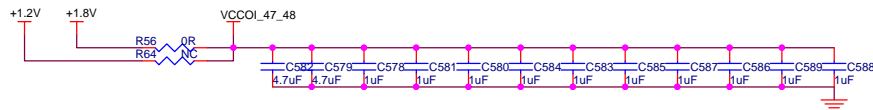
MASTER SPI M[2:0] = 001

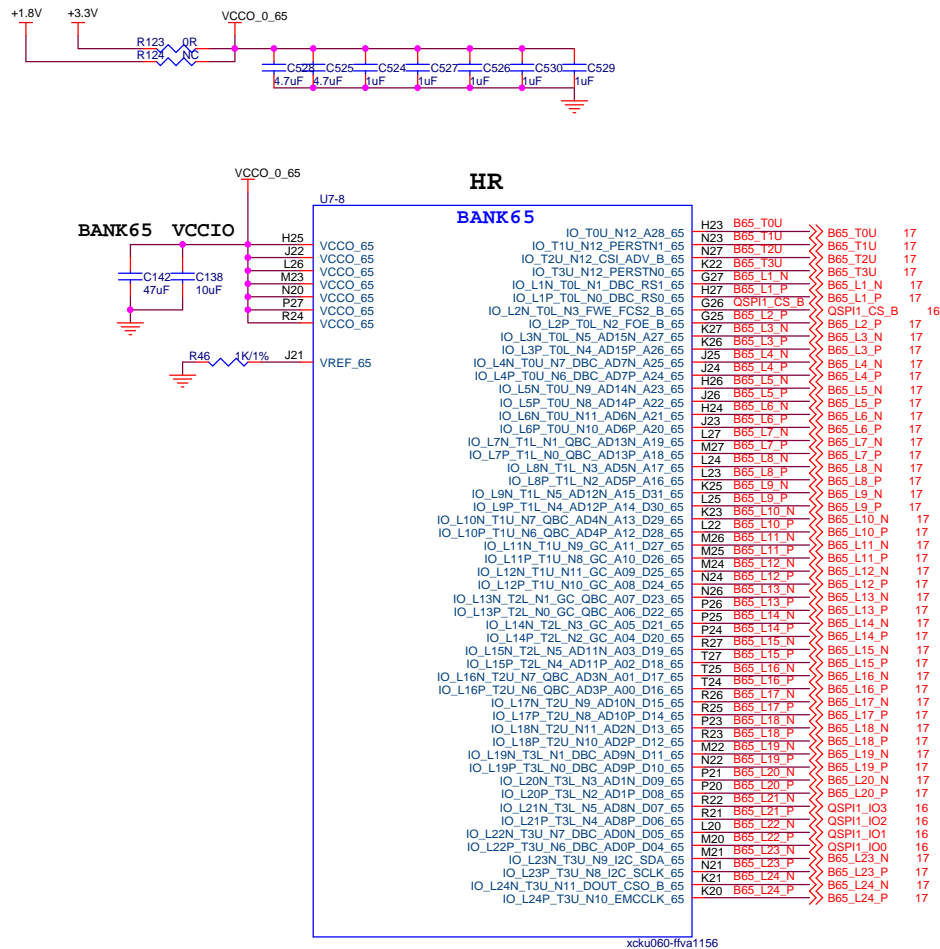
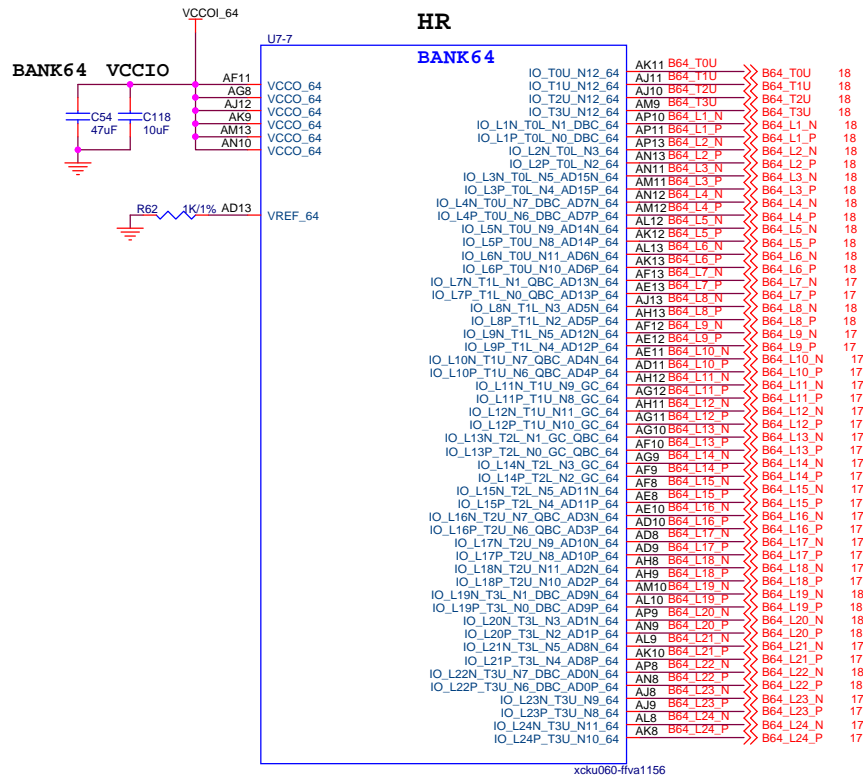
FPGA DONE LED

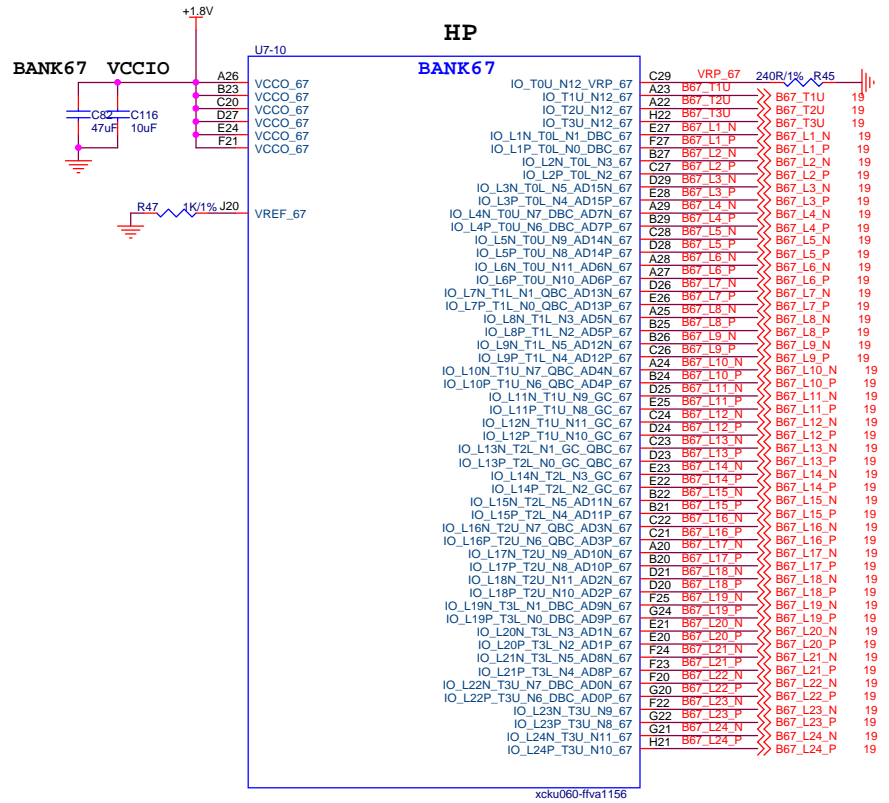
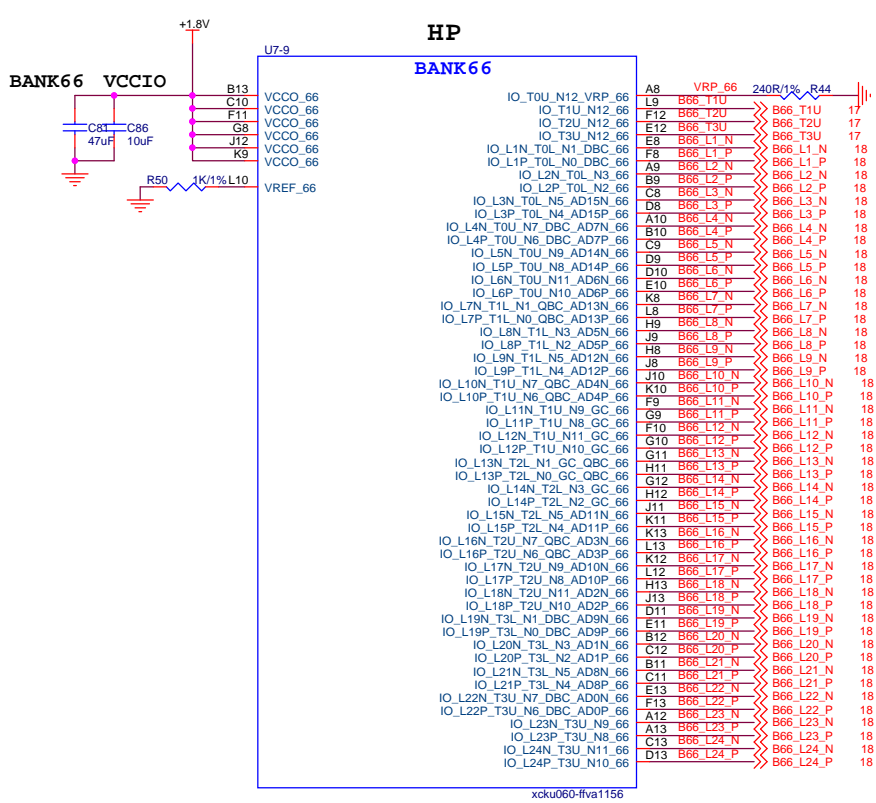


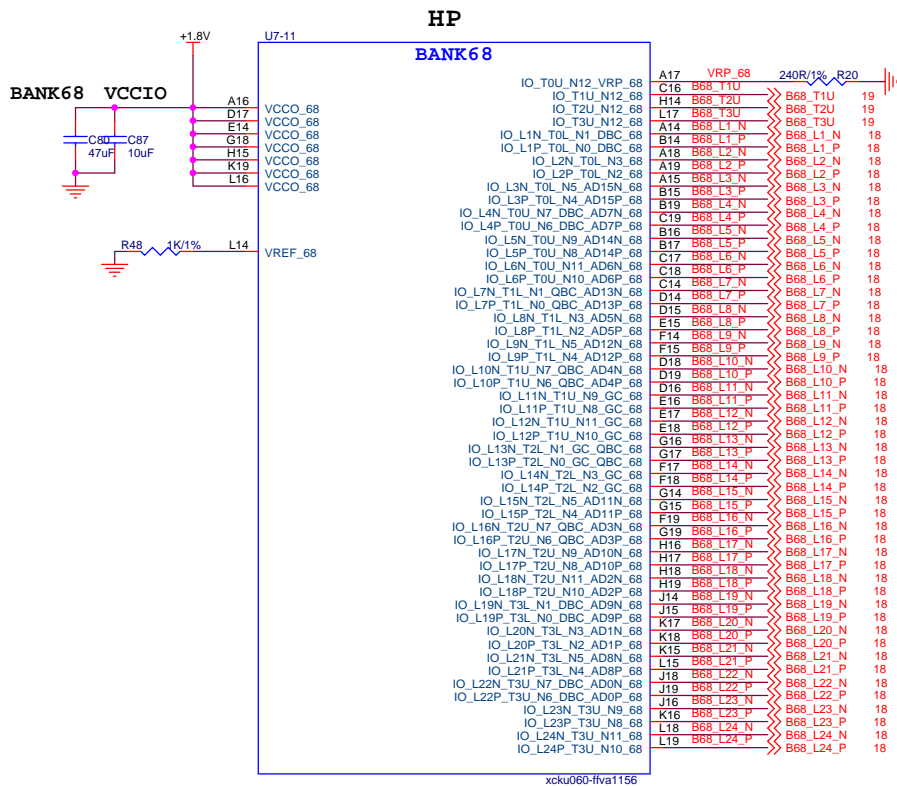
POWER LED











U7-12

MGTHRXN0_224	AP1	224_RX0_N	>>>224_RX0_N	17
MGTHRXP0_224	AP2	224_RX0_P	>>>224_RX0_P	17
MGTHRXN1_224	AM1	224_RX1_N	>>>224_RX1_N	17
MGTHRXP1_224	AM2	224_RX1_P	>>>224_RX1_P	17
MGTHRXN2_224	AK1	224_RX2_N	>>>224_RX2_N	17
MGTHRXP2_224	AK2	224_RX2_P	>>>224_RX2_P	17
MGTHRXN3_224	AJ3	224_RX3_N	>>>224_RX3_N	17
MGTHRXP3_224	AJ4	224_RX3_P	>>>224_RX3_P	17
MGHTTXN0_224	AN3	224_TX0_N	>>>224_TX0_N	17
MGHTTXP0_224	AN4	224_TX0_P	>>>224_TX0_P	17
MGHTTXN1_224	AM5	224_TX1_N	>>>224_TX1_N	17
MGHTTXP1_224	AM6	224_TX1_P	>>>224_TX1_P	17
MGHTTXN2_224	AL3	224_TX2_N	>>>224_TX2_N	17
MGHTTXP2_224	AL4	224_TX2_P	>>>224_TX2_P	17
MGHTTXN3_224	AK5	224_TX3_N	>>>224_TX3_N	17
MGHTTXP3_224	AK6	224_TX3_P	>>>224_TX3_P	17
MGTREFCLK0N_224	AF5	224_CLK0_N	>>>224_CLK0_N	17
MGTREFCLK0P_224	AF6	224_CLK0_P	>>>224_CLK0_P	17
MGTREFCLK1N_224	AD5	224_CLK1_N	>>>224_CLK1_N	17
MGTREFCLK1P_224	AD6	224_CLK1_P	>>>224_CLK1_P	17

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U7-13

MGTREF_R	AH1	225_RX0_N	>>>225_RX0_N	17
MGTAVTTRCAL_R	AH2	225_RX0_P	>>>225_RX0_P	17
MGTHRXN0_225	AF1	225_RX1_N	>>>225_RX1_N	17
MGTHRXP0_225	AF2	225_RX1_P	>>>225_RX1_P	17
MGTHRXN1_225	AD1	225_RX2_N	>>>225_RX2_N	17
MGTHRXP1_225	AD2	225_RX2_P	>>>225_RX2_P	17
MGTHRXN2_225	AB1	225_RX3_N	>>>225_RX3_N	17
MGTHRXP2_225	AB2	225_RX3_P	>>>225_RX3_P	17
MGTHRXN3_225	AH5	225_TX0_N	>>>225_TX0_N	17
MGTHRXP3_225	AH6	225_TX0_P	>>>225_TX0_P	17
MGHTTXN0_225	AG3	225_TX1_N	>>>225_TX1_N	17
MGHTTXP0_225	AG4	225_TX1_P	>>>225_TX1_P	17
MGHTTXN1_225	AE3	225_TX2_N	>>>225_TX2_N	17
MGHTTXP1_225	AE4	225_TX2_P	>>>225_TX2_P	17
MGHTTXN2_225	AC3	225_TX3_N	>>>225_TX3_N	17
MGHTTXP2_225	AC4	225_TX3_P	>>>225_TX3_P	17
MGHTTXN3_225	AB5	225_CLK0_N	>>>225_CLK0_N	17
MGHTTXP3_225	AB6	225_CLK0_P	>>>225_CLK0_P	17
MGTREFCLK0N_225	Y5	225_CLK1_N	>>>225_CLK1_N	17
MGTREFCLK0P_225	Y6	225_CLK1_P	>>>225_CLK1_P	17
MGTREFCLK1N_225				
MGTREFCLK1P_225				

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Trace length from the resistor pins to the
FPGA pins MGTREF and MGTAVTTRCAL.
Connection must be equal in length

U7-14

MGTHRXN0_226	Y1	226_RX0_N	>>>226_RX0_N	17
MGTHRXP0_226	Y2	226_RX0_P	>>>226_RX0_P	17
MGTHRXN1_226	V1	226_RX1_N	>>>226_RX1_N	17
MGTHRXP1_226	V2	226_RX1_P	>>>226_RX1_P	17
MGTHRXN2_226	T1	226_RX2_N	>>>226_RX2_N	19
MGTHRXP2_226	T2	226_RX2_P	>>>226_RX2_P	19
MGTHRXN3_226	P1	226_RX3_N	>>>226_RX3_N	19
MGTHRXP3_226	P2	226_RX3_P	>>>226_RX3_P	19
MGHTTXN0_226	AA3	226_TX0_N	>>>226_TX0_N	17
MGHTTXP0_226	AA4	226_TX0_P	>>>226_TX0_P	17
MGHTTXN1_226	W3	226_TX1_N	>>>226_TX1_N	17
MGHTTXP1_226	W4	226_TX1_P	>>>226_TX1_P	17
MGHTTXN2_226	U3	226_TX2_N	>>>226_TX2_N	19
MGHTTXP2_226	U4	226_TX2_P	>>>226_TX2_P	19
MGHTTXN3_226	R3	226_TX3_N	>>>226_TX3_N	19
MGHTTXP3_226	R4	226_TX3_P	>>>226_TX3_P	19
MGTREFCLK0N_226	V5	226_CLK0_N	>>>226_CLK0_N	19
MGTREFCLK0P_226	V6	226_CLK0_P	>>>226_CLK0_P	19
MGTREFCLK1N_226	T5	226_CLK1_N	>>>226_CLK1_N	19
MGTREFCLK1P_226	T6	226_CLK1_P	>>>226_CLK1_P	19

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U7-15

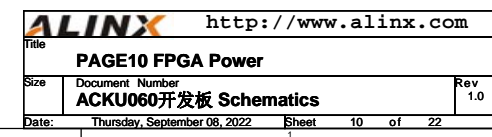
MGTHRXN0_227	M1	227_RX0_N	>>>227_RX0_N	19
MGTHRXP0_227	M2	227_RX0_P	>>>227_RX0_P	19
MGTHRXN1_227	K1	227_RX1_N	>>>227_RX1_N	19
MGTHRXP1_227	K2	227_RX1_P	>>>227_RX1_P	19
MGTHRXN2_227	H1	227_RX2_N	>>>227_RX2_N	19
MGTHRXP2_227	H2	227_RX2_P	>>>227_RX2_P	19
MGTHRXN3_227	F1	227_RX3_N	>>>227_RX3_N	19
MGTHRXP3_227	F2	227_RX3_P	>>>227_RX3_P	19
MGHTTXN0_227	N3	227_TX0_N	>>>227_TX0_N	19
MGHTTXP0_227	N4	227_TX0_P	>>>227_TX0_P	19
MGHTTXN1_227	L3	227_TX1_N	>>>227_TX1_N	19
MGHTTXP1_227	L4	227_TX1_P	>>>227_TX1_P	19
MGHTTXN2_227	J3	227_TX2_N	>>>227_TX2_N	19
MGHTTXP2_227	J4	227_TX2_P	>>>227_TX2_P	19
MGHTTXN3_227	G3	227_TX3_N	>>>227_TX3_N	19
MGHTTXP3_227	G4	227_TX3_P	>>>227_TX3_P	19
MGTREFCLK0N_227	P5	227_CLK0_N	>>>227_CLK0_N	19
MGTREFCLK0P_227	P6	227_CLK0_P	>>>227_CLK0_P	19
MGTREFCLK1N_227	M5	227_CLK1_N	>>>227_CLK1_N	19
MGTREFCLK1P_227	M6	227_CLK1_P	>>>227_CLK1_P	19

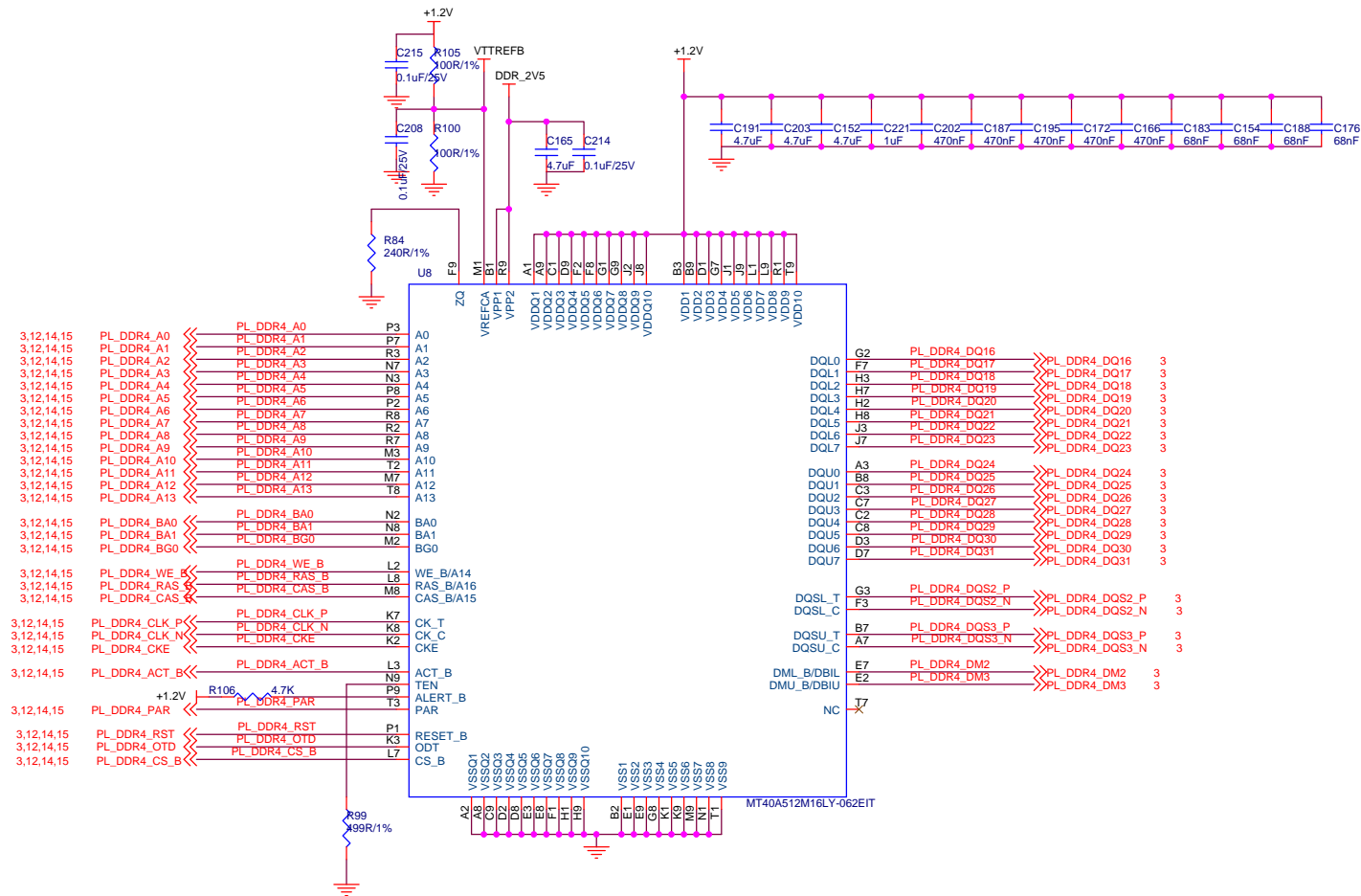
xcku060-fva1156

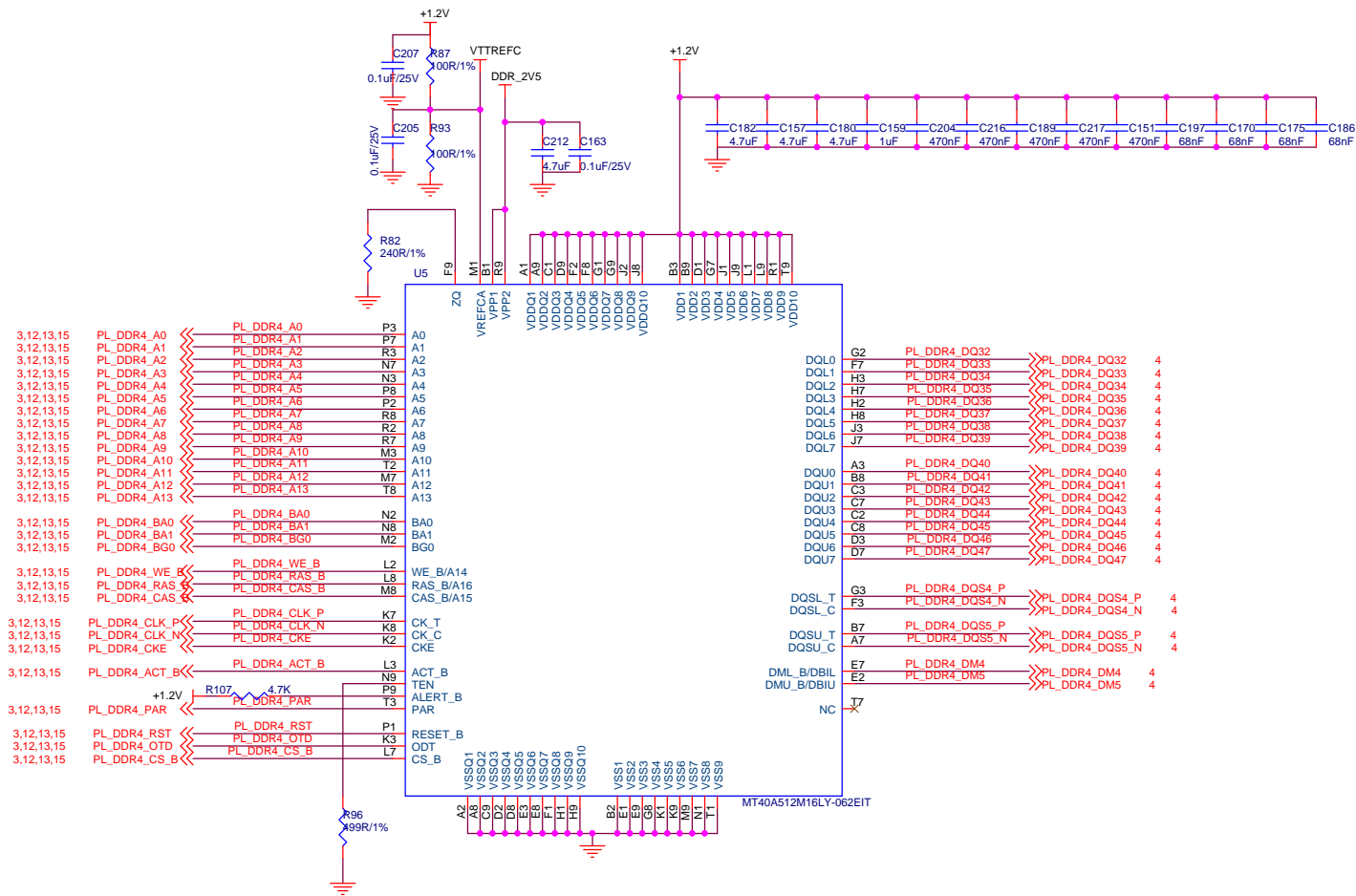
U7-16

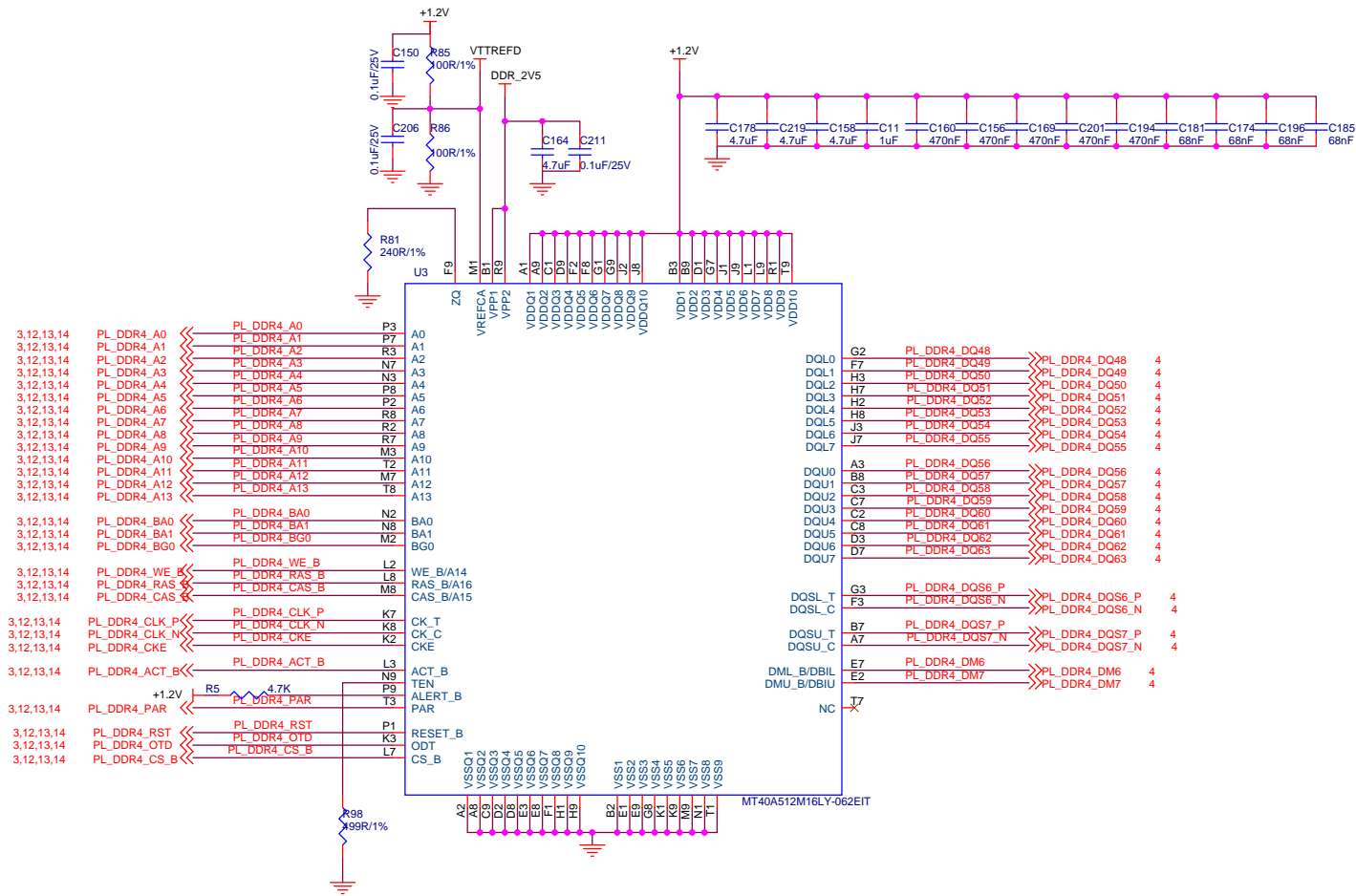
MGTHRXN0_228	E3	228_RX0_N	>>>228_RX0_N	19
MGTHRXP0_228	E4	228_RX0_P	>>>228_RX0_P	19
MGTHRXN1_228	D1	228_RX1_N	>>>228_RX1_N	19
MGTHRXP1_228	D2	228_RX1_P	>>>228_RX1_P	19
MGTHRXN2_228	B1	228_RX2_N	>>>228_RX2_N	19
MGTHRXP2_228	B2	228_RX2_P	>>>228_RX2_P	19
MGTHRXN3_228	A3	228_RX3_N	>>>228_RX3_N	19
MGTHRXP3_228	A4	228_RX3_P	>>>228_RX3_P	19
MGHTTXN0_228	F5	228_TX0_N	>>>228_TX0_N	19
MGHTTXP0_228	F6	228_TX0_P	>>>228_TX0_P	19
MGHTTXN1_228	D5	228_TX1_N	>>>228_TX1_N	19
MGHTTXP1_228	D6	228_TX1_P	>>>228_TX1_P	19
MGHTTXN2_228	C3	228_TX2_N	>>>228_TX2_N	19
MGHTTXP2_228	C4	228_TX2_P	>>>228_TX2_P	19
MGHTTXN3_228	B5	228_TX3_N	>>>228_TX3_N	19
MGHTTXP3_228	B6	228_TX3_P	>>>228_TX3_P	19
MGTREFCLK0N_228	K5	228_CLK0_N	>>>228_CLK0_N	19
MGTREFCLK0P_228	K6	228_CLK0_P	>>>228_CLK0_P	19
MGTREFCLK1N_228	H5	228_CLK1_N	>>>228_CLK1_N	19
MGTREFCLK1P_228	H6	228_CLK1_P	>>>228_CLK1_P	19

xcku060-fva1156

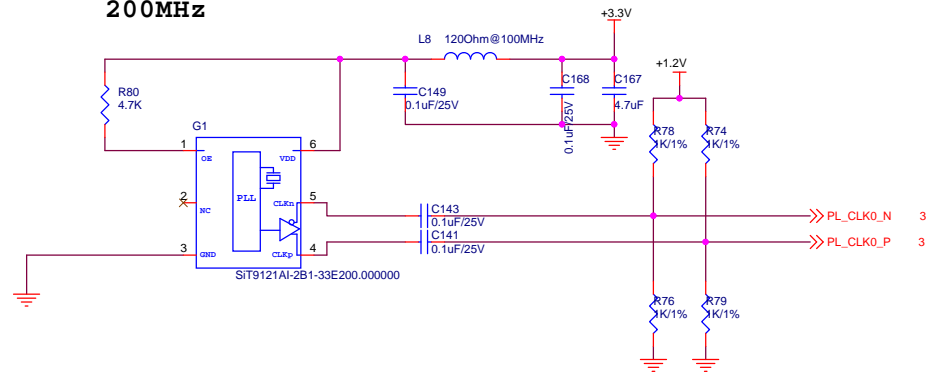




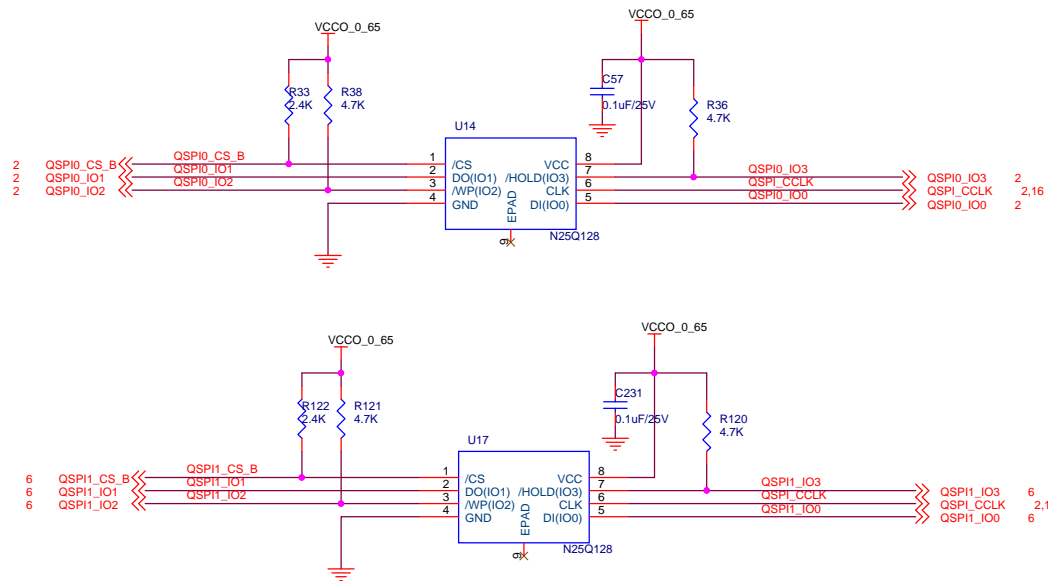


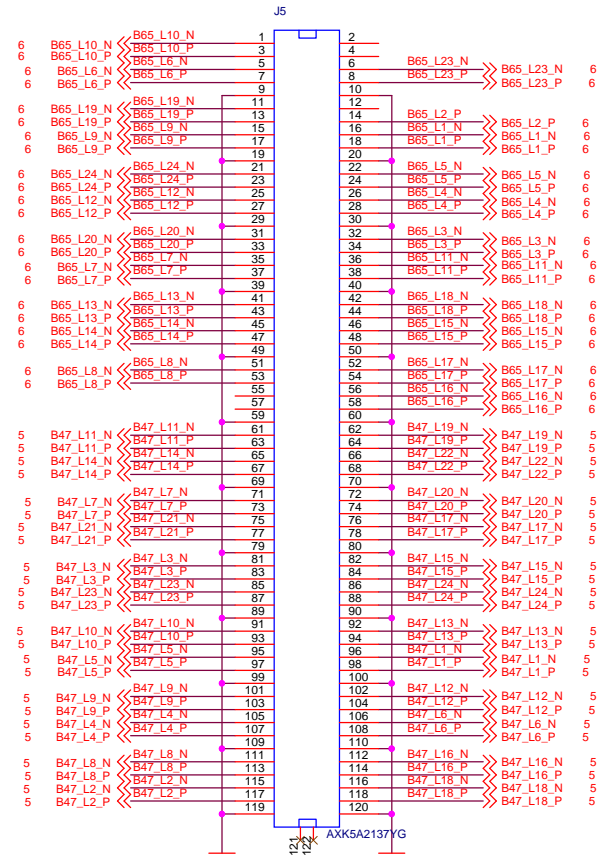
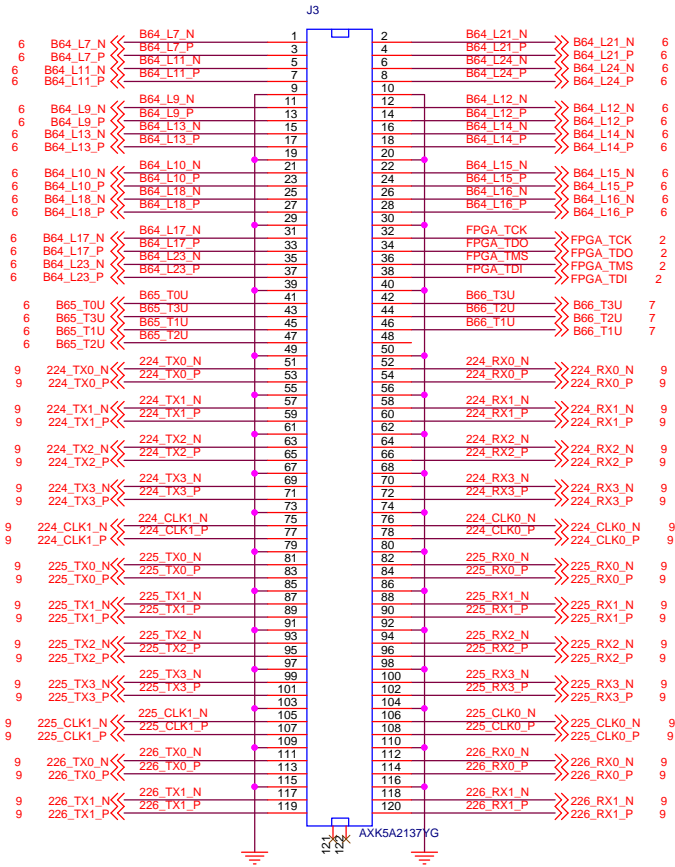


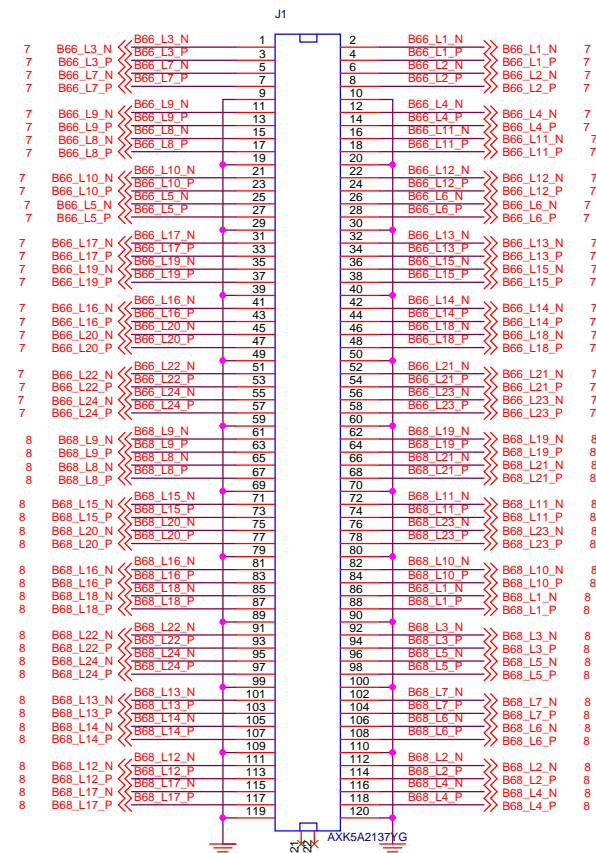
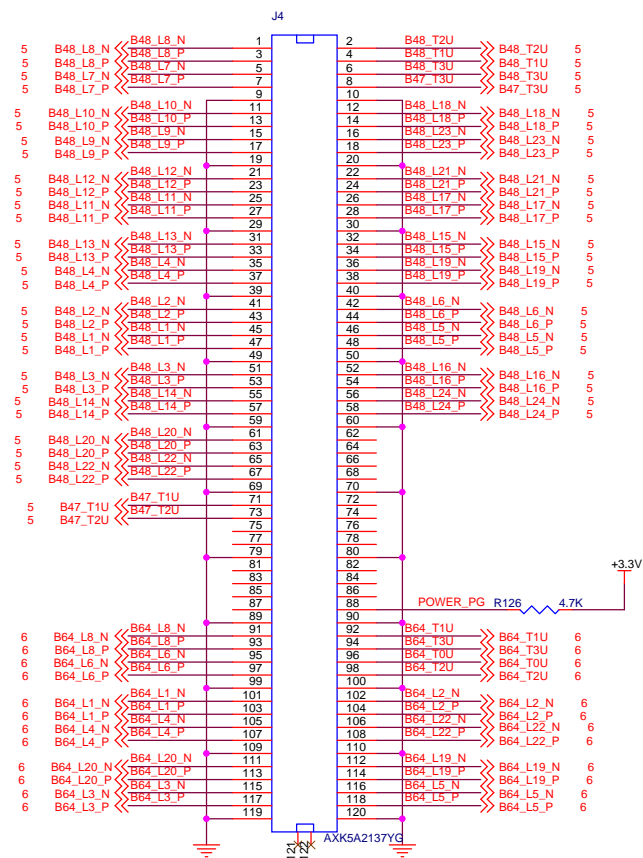
200MHz

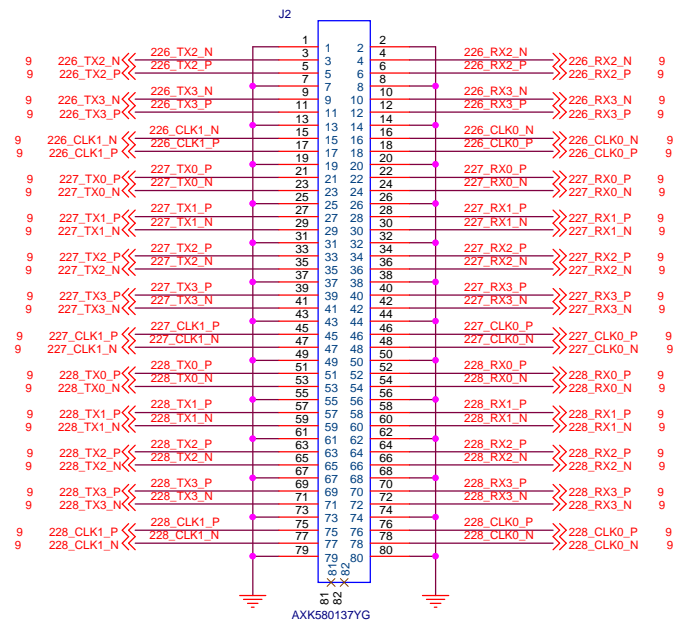


FPGA CONFIG SPI

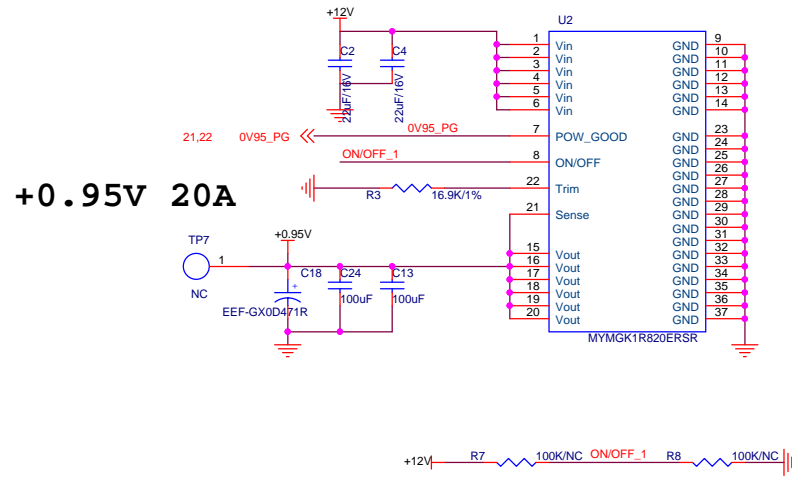


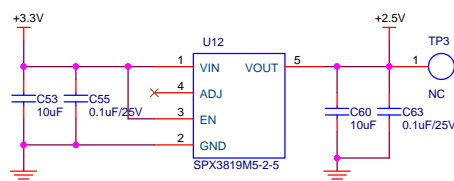
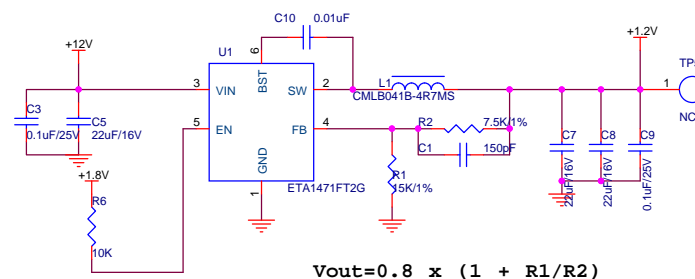
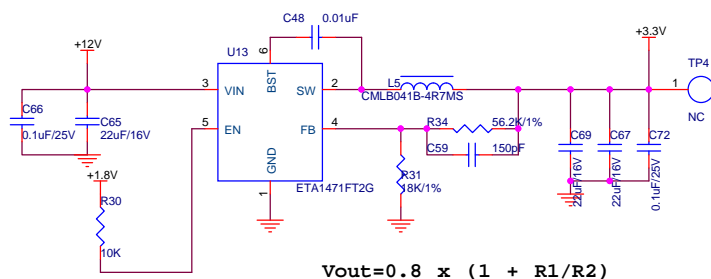
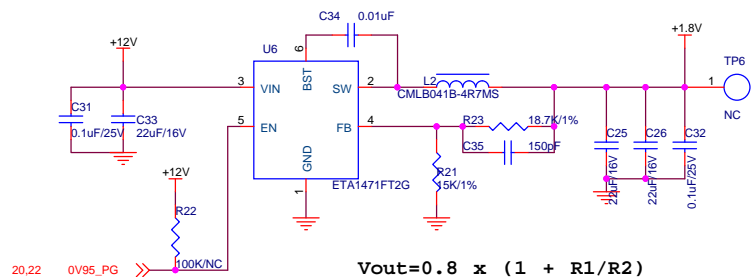




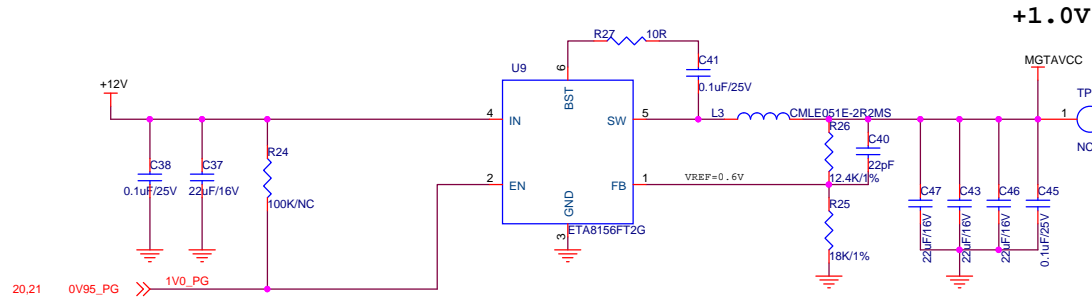


Input: 8V to 15V



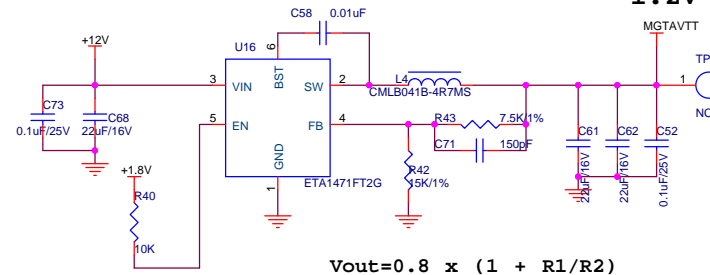


1.0V POWER 6A



$$V_{out} = 0.6 \times (1 + R1/R2)$$

1.2V



$$V_{out} = 0.8 \times (1 + R1/R2)$$

$$V_{out} = 0.8 \times (1 + R1/R2)$$

