ZYNQ UltraScale+ FPGA Development Board ACU5EV

System on Module

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.1	2021-04-24	Rachel Zhou	First Release

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Part 1: ACU5EV Core Board Introduction

ACU5EV (core board model, the same below) FPGA core board, ZYNQ chip is based on XCZU5EV-2SFVC784I of XILINX company Zynq UltraScale+ MPSoCs EV Family.

This core board uses 5 Micron DDR4 chips MT40A512M16GE, of which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity. One DDR4 chip is mounted on the PL end, which is a 16-bit data bus width and a capacity of 1GB. The highest operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the highest operating speed of DDR4 SDRAM on the PL side can reach 1066MHz (data rate 2132Mbps). In addition, a 256MBit QSPI FLASH and an 8GB eMMC FLASH chip are also integrated on the core board to start storage configuration and system files.

In order to connect with the carrier board, the four board-to-board connectors of this core board expand the PS side USB2.0 interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports; also expand 4 pairs of PS MGT high-speed transceiver interface; and almost all IO ports on the PL side (HP I/O: 96, HD I/O: 84). The wiring between the XCZU5EV chip and the interface has been processed with equal length and differential, and the core board size is only 3.15*2.36 (inch), which is very suitable for secondary development.
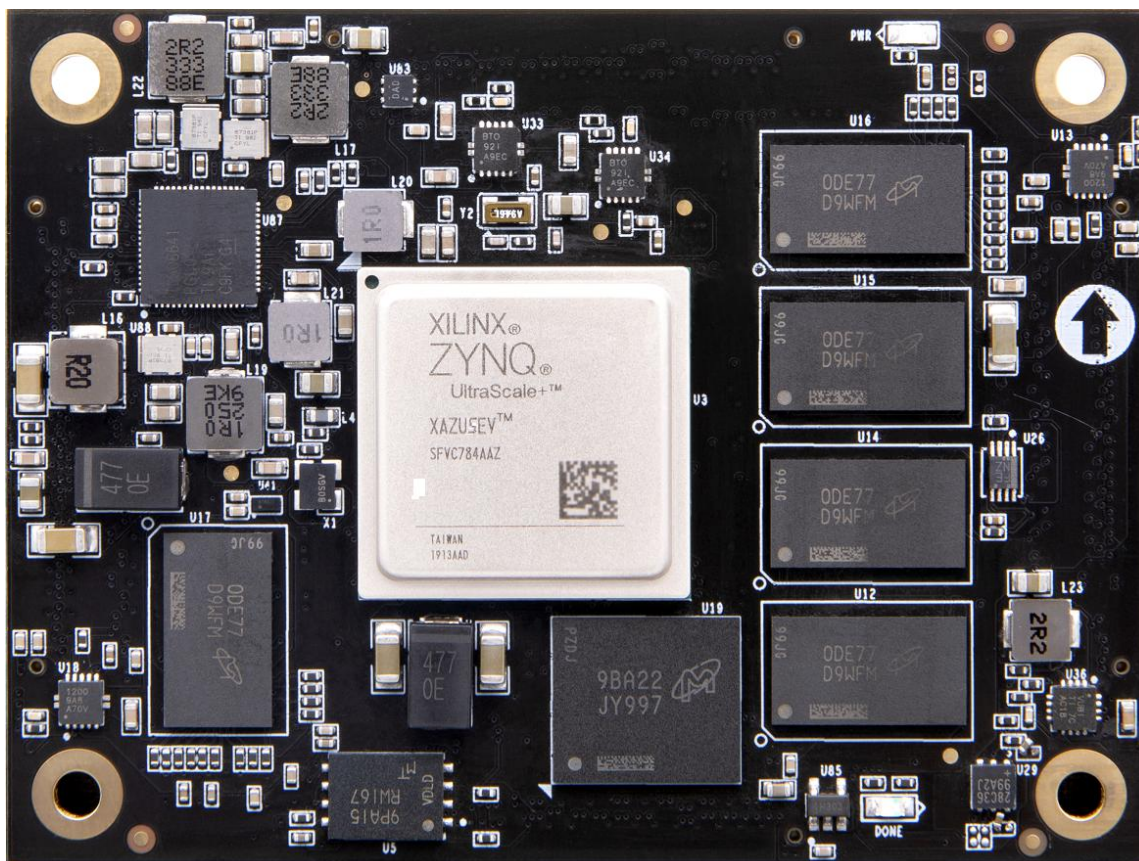
Figure 1-1: ACU5EV Core Board (Front View)

Part 2: ZYNQ Chip

The FPGA core board ACU5EV uses Xilinx's Zynq UltraScale+ MPSoCs EV family chip, module XCZU5EV-2SFVC784I. The PS system of the ZU5EV chip integrates 4 ARM Cortex™-A53 processors with a speed of up to 1.2Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 500Mhz

The ZU5EV chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, with rich high-speed interfaces on the PS side such as PCIE Gen2, USB3.0, SATA 3.1, DisplayPort; it also supports USB2.0 , Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL end contains a wealth of programmable logic units, DSP and internal RAM. .

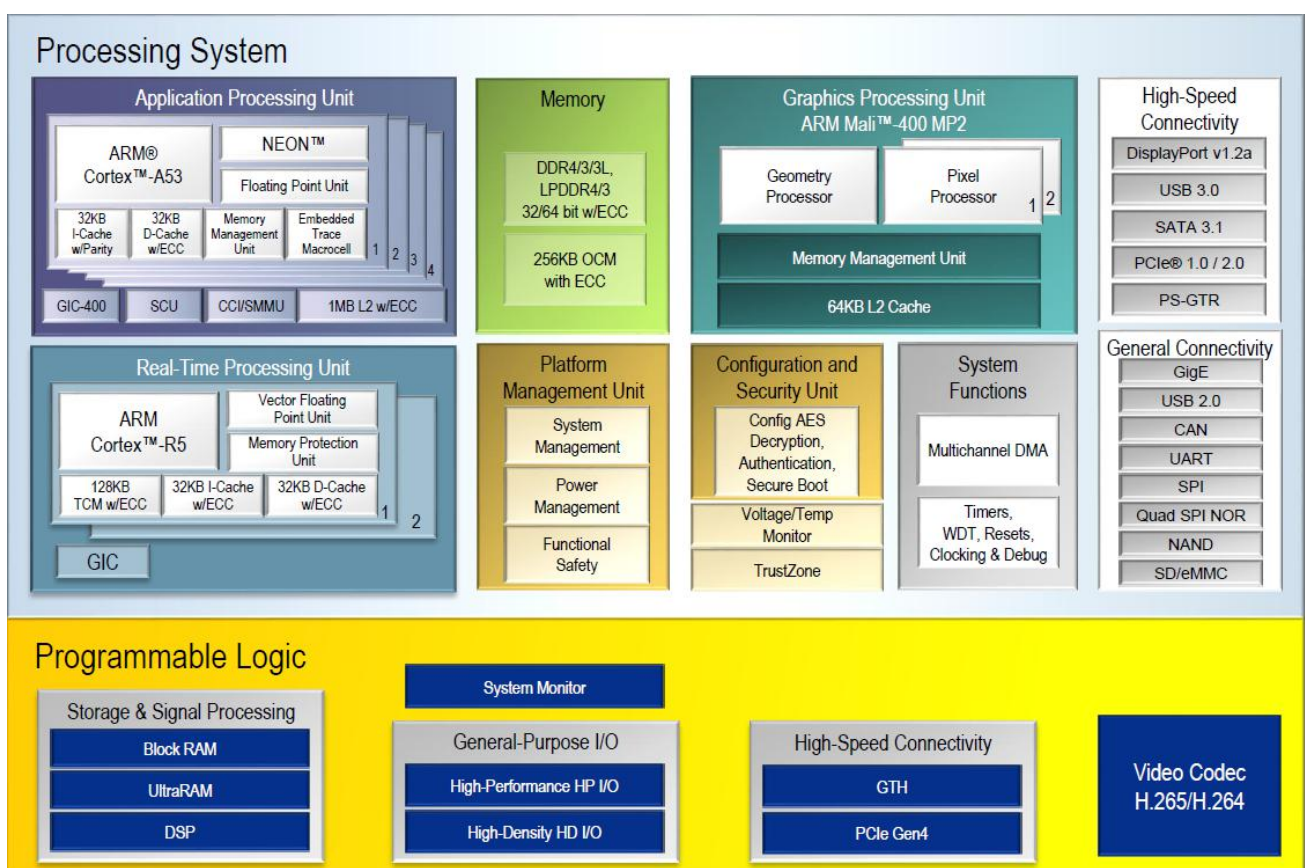Figure 2-1 detailed the Overall Block Diagram of the ZU5EV Chip.

Figure 2-1: Overall Block Diagram of the ZYNQ ZU5EV Chip

The main parameters of the PS system part are as follows:

➢ ARM quad-core Cortex™-A53 processor, speed up to 1.5GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs

➢ ARM dual-core Cortex-R5 processor, speed up to 600MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.

➢ Image Video Processor Mali-400 MP2, speed up to 677MHz, 64KB level 2 cache

➢ External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface

➢ Static storage interface, support NAND, 2xQuad-SPI FLASH.

➢ High-speed connection interface, support PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode Gigabit Ethernet

➢ Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO

➢ Power management: Support the four-part division of power supply Full/Low/PL/Battery

➢ Encryption algorithm: support RSA, AES and SHA.

➢ System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic part are as follows:

➢ Logic Cells: 256.2K

➢ Flip-flops: 234.24K

➢ Look-up-tables (LUTs): 117.12K

➢ Block RAM: 5.1Mb

➢ Clock Management Units (CMTs): 4

➢ DSP Slices: 1248

➢ Video Codec Unit (VCU): 1

➢ PCIE3.0: 2

➢ GTH 12.5Gb/s Transceiver: 4

XCZU5EV-2SFVC784I chip speed grade is -2, industrial grade, package is SFVC784

Part 3: DDR4 DRAM

The ACU5EV core board is equipped with 5 Micron (Micron) 1GB DDR4 chips, model MT40A512M16LY-062E, of which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity. One DDR4 chip is mounted on the PL end, which is a 16-bit data bus width and a capacity of 1GB. The maximum operating speed of the DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the 4 DDR4 storage systems are directly connected to the memory interface of the PS BANK504. The highest operating speed of the DDR4 SDRAM on the PL side can reach 1066MHz (data rate 2133Mbps), and a piece of DDR4 is connected to the BANK64 interface of the FPGA. The specific configuration of DDR4 SDRAM is shown in Table 3-1 below:

Bit Number	Chip Model	Capacity	Factory
U12,U14,U15,U16	MT40A512M16LY-062E	512M x 16bit	Micron

Table 3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection of DDR4 SDRAM on the PS Side is shown in Figure 3-1:
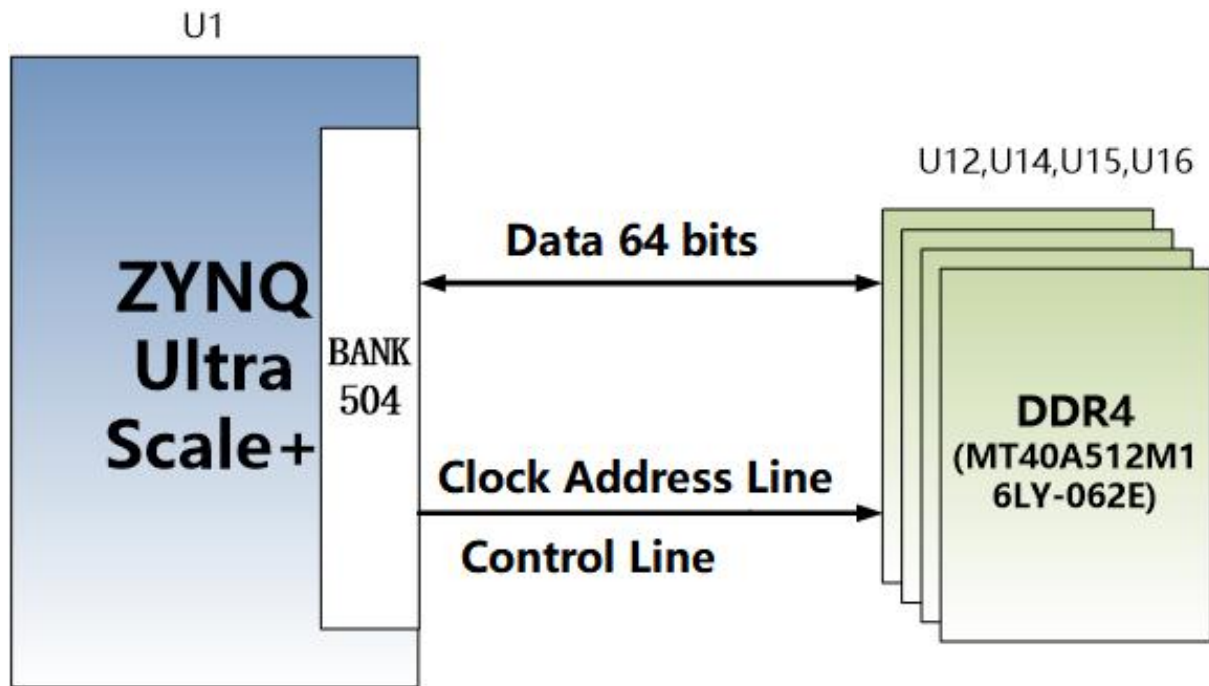
Figure 3-1: DDR3 DRAM schematic diagram

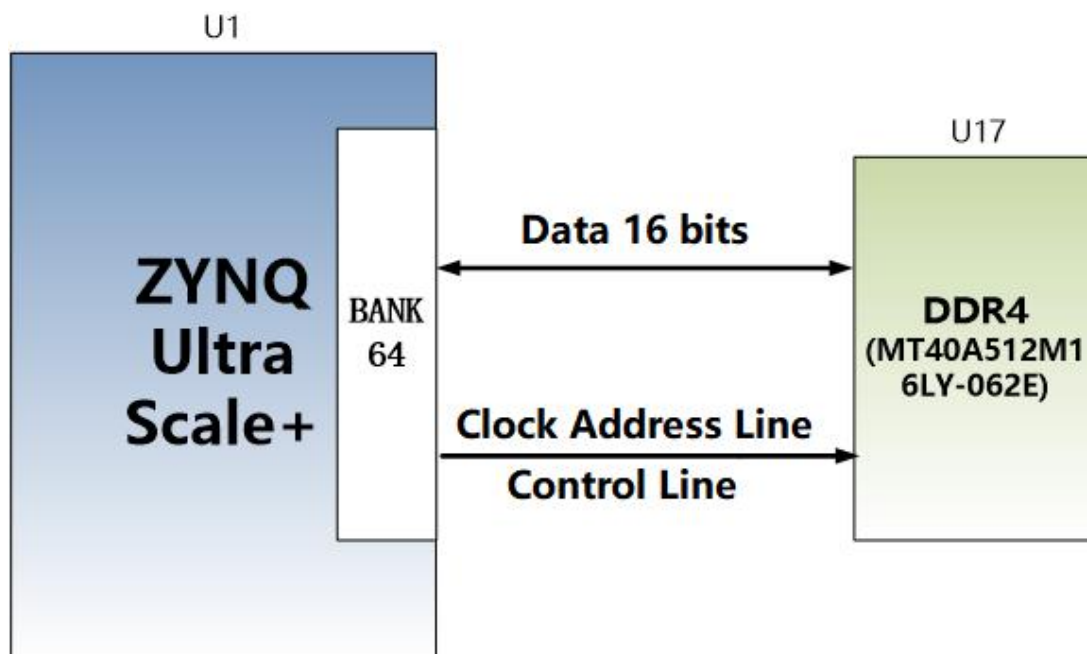The hardware connection of DDR4 SDRAM on the PI Side is shown in Figure 3-2:

Figure 3-2: DDR3 DRAM schematic diagram

PS Side DDR4 DRAM pin assignment:

Signal Name	Pin Name	Pin Number
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AF21
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	AG21
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AF23
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AG23
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AF25
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AF26
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AE27
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AF27
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	N23
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	M23
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	L23
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	K23
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	N26
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	N27
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	J26
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	J27
PS_DDR4_DQ0	PS_DDR_DQ0_504	AD21
PS_DDR4_DQ1	PS_DDR_DQ1_504	AE20
PS_DDR4_DQ2	PS_DDR_DQ2_504	AD20
PS_DDR4_DQ3	PS_DDR_DQ3_504	AF20
PS_DDR4_DQ4	PS_DDR_DQ4_504	AH21
PS_DDR4_DQ5	PS_DDR_DQ5_504	AH20
PS_DDR4_DQ6	PS_DDR_DQ6_504	AH19
PS_DDR4_DQ7	PS_DDR_DQ7_504	AG19
PS_DDR4_DQ8	PS_DDR_DQ8_504	AF22
PS_DDR4_DQ9	PS_DDR_DQ9_504	AH22
PS_DDR4_DQ10	PS_DDR_DQ10_504	AE22
PS_DDR4_DQ11	PS_DDR_DQ11_504	AD22
PS_DDR4_DQ12	PS_DDR_DQ12_504	AH23
PS_DDR4_DQ13	PS_DDR_DQ13_504	AH24
PS_DDR4_DQ14	PS_DDR_DQ14_504	AE24
PS_DDR4_DQ15	PS_DDR_DQ15_504	AG24
PS_DDR4_DQ16	PS_DDR_DQ16_504	AC26
PS_DDR4_DQ17	PS_DDR_DQ17_504	AD26

PS_DDR4_DQ18	PS_DDR_DQ18_504	AD25
PS_DDR4_DQ19	PS_DDR_DQ19_504	AD24
PS_DDR4_DQ20	PS_DDR_DQ20_504	AG26
PS_DDR4_DQ21	PS_DDR_DQ21_504	AH25
PS_DDR4_DQ22	PS_DDR_DQ22_504	AH26
PS_DDR4_DQ23	PS_DDR_DQ23_504	AG25
PS_DDR4_DQ24	PS_DDR_DQ24_504	AH27
PS_DDR4_DQ25	PS_DDR_DQ25_504	AH28
PS_DDR4_DQ26	PS_DDR_DQ26_504	AF28
PS_DDR4_DQ27	PS_DDR_DQ27_504	AG28
PS_DDR4_DQ28	PS_DDR_DQ28_504	AC27
PS_DDR4_DQ29	PS_DDR_DQ29_504	AD27
PS_DDR4_DQ30	PS_DDR_DQ30_504	AD28
PS_DDR4_DQ31	PS_DDR_DQ31_504	AC28
PS_DDR4_DQ32	PS_DDR_DQ32_504	T22
PS_DDR4_DQ33	PS_DDR_DQ33_504	R22
PS_DDR4_DQ34	PS_DDR_DQ34_504	P22
PS_DDR4_DQ35	PS_DDR_DQ35_504	N22
PS_DDR4_DQ36	PS_DDR_DQ36_504	T23
PS_DDR4_DQ37	PS_DDR_DQ37_504	P24
PS_DDR4_DQ38	PS_DDR_DQ38_504	R24
PS_DDR4_DQ39	PS_DDR_DQ39_504	N24
PS_DDR4_DQ40	PS_DDR_DQ40_504	H24
PS_DDR4_DQ41	PS_DDR_DQ41_504	J24
PS_DDR4_DQ42	PS_DDR_DQ42_504	M24
PS_DDR4_DQ43	PS_DDR_DQ43_504	K24
PS_DDR4_DQ44	PS_DDR_DQ44_504	J22
PS_DDR4_DQ45	PS_DDR_DQ45_504	H22
PS_DDR4_DQ46	PS_DDR_DQ46_504	K22
PS_DDR4_DQ47	PS_DDR_DQ47_504	L22
PS_DDR4_DQ48	PS_DDR_DQ48_504	M25
PS_DDR4_DQ49	PS_DDR_DQ49_504	M26
PS_DDR4_DQ50	PS_DDR_DQ50_504	L25
PS_DDR4_DQ51	PS_DDR_DQ51_504	L26
PS_DDR4_DQ52	PS_DDR_DQ52_504	K28
PS_DDR4_DQ53	PS_DDR_DQ53_504	L28

PS_DDR4_DQ54	PS_DDR_DQ54_504	M28
PS_DDR4_DQ55	PS_DDR_DQ55_504	N28
PS_DDR4_DQ56	PS_DDR_DQ56_504	J28
PS_DDR4_DQ57	PS_DDR_DQ57_504	K27
PS_DDR4_DQ58	PS_DDR_DQ58_504	H28
PS_DDR4_DQ59	PS_DDR_DQ59_504	H27
PS_DDR4_DQ60	PS_DDR_DQ60_504	G26
PS_DDR4_DQ61	PS_DDR_DQ61_504	G25
PS_DDR4_DQ62	PS_DDR_DQ62_504	K25
PS_DDR4_DQ63	PS_DDR_DQ63_504	J25
PS_DDR4_DM0	PS_DDR_DM0_504	AG20
PS_DDR4_DM1	PS_DDR_DM1_504	AE23
PS_DDR4_DM2	PS_DDR_DM2_504	AE25
PS_DDR4_DM3	PS_DDR_DM3_504	AE28
PS_DDR4_DM4	PS_DDR_DM4_504	R23
PS_DDR4_DM5	PS_DDR_DM5_504	H23
PS_DDR4_DM6	PS_DDR_DM6_504	L27
PS_DDR4_DM7	PS_DDR_DM7_504	H26
PS_DDR4_A0	PS_DDR_A0_504	W28
PS_DDR4_A1	PS_DDR_A1_504	Y28
PS_DDR4_A2	PS_DDR_A2_504	AB28
PS_DDR4_A3	PS_DDR_A3_504	AA28
PS_DDR4_A4	PS_DDR_A4_504	Y27
PS_DDR4_A5	PS_DDR_A5_504	AA27
PS_DDR4_A6	PS_DDR_A6_504	Y22
PS_DDR4_A7	PS_DDR_A7_504	AA23
PS_DDR4_A8	PS_DDR_A8_504	AA22
PS_DDR4_A9	PS_DDR_A9_504	AB23
PS_DDR4_A10	PS_DDR_A10_504	AA25
PS_DDR4_A11	PS_DDR_A11_504	AA26
PS_DDR4_A12	PS_DDR_A12_504	AB25
PS_DDR4_A13	PS_DDR_A13_504	AB26
PS_DDR4_WE_B	PS_DDR_A14_504	AB24
PS_DDR4_CAS_B	PS_DDR_A15_504	AC24
PS_DDR4_RAS_B	PS_DDR_A16_504	AC23
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	Y23

PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	U25
PS_DDR4_BA0	PS_DDR_BA0_504	V23
PS_DDR4_BA1	PS_DDR_BA1_504	W22
PS_DDR4_BG0	PS_DDR_BG0_504	W24
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	W27
PS_DDR4_ODT0	PS_DDR_ODT0_504	U28
PS_DDR4_PARITY	PS_DDR_PARITY_504	V24
PS_DDR4_RESET_B	PS_DDR_RST_N_504	U23
PS_DDR4_CLK0_P	PS_DDR_CK0_P_504	W25
PS_DDR4_CLK0_N	PS_DDR_CK0_N_504	W26
PS_DDR4_CKE0	PS_DDR_CKE0_504	V28

PL Side DDR4 DRAM pin assignment:

Signal Name	Pin Name	Pin Number
PL_DDR4_DQS0_P	IO_L22P_T3U_N6_DBC_AD0P_64	AE2
PL_DDR4_DQS0_N	IO_L22N_T3U_N7_DBC_AD0N_64	AF2
PL_DDR4_DQS1_P	IO_L16P_T2U_N6_QBC_AD3P_64	AD2
PL_DDR4_DQS1_N	IO_L16N_T2U_N7_QBC_AD3N_64	AD1
PL_DDR4_DQ0	IO_L24N_T3U_N11_64	AG1
PL_DDR4_DQ1	IO_L24P_T3U_N10_64	AF1
PL_DDR4_DQ2	IO_L23N_T3U_N9_64	AH1
PL_DDR4_DQ3	IO_L23P_T3U_N8_64	AH2
PL_DDR4_DQ4	IO_L21N_T3L_N5_AD8N_64	AF3
PL_DDR4_DQ5	IO_L21P_T3L_N4_AD8P_64	AE3
PL_DDR4_DQ6	IO_L20N_T3L_N3_AD1N_64	AH3
PL_DDR4_DQ7	IO_L20P_T3L_N2_AD1P_64	AG3
PL_DDR4_DQ8	IO_L18N_T2U_N11_AD2N_64	AC1
PL_DDR4_DQ9	IO_L18P_T2U_N10_AD2P_64	AB1
PL_DDR4_DQ10	IO_L17N_T2U_N9_AD10N_64	AC2
PL_DDR4_DQ11	IO_L17P_T2U_N8_AD10P_64	AB2
PL_DDR4_DQ12	IO_L15N_T2L_N5_AD11N_64	AB3
PL_DDR4_DQ13	IO_L15P_T2L_N4_AD11P_64	AB4
PL_DDR4_DQ14	IO_L14N_T2L_N3_GC_64	AC3
PL_DDR4_DQ15	IO_L14P_T2L_N2_GC_64	AC4
PL_DDR4_DM0	IO_L19P_T3L_N0_DBC_AD9P_64	AG4

PL_DDR4_DM1	IO_L13P_T2L_N0_GC_QBC_64	AD5
PL_DDR4_A0	IO_L8N_T1L_N3_AD5N_64	AG8
PL_DDR4_A1	IO_L3P_T0L_N4_AD15P_64	AB8
PL_DDR4_A2	IO_L8P_T1L_N2_AD5P_64	AF8
PL_DDR4_A3	IO_L3N_T0L_N5_AD15N_64	AC8
PL_DDR4_A4	IO_L11P_T1U_N8_GC_64	AF7
PL_DDR4_A5	IO_L4P_T0U_N6_DBC_AD7P_64	AD7
PL_DDR4_A6	IO_L9N_T1L_N5_AD12N_64	AH7
PL_DDR4_A7	IO_L2P_T0L_N2_64	AE9
PL_DDR4_A8	IO_L9P_T1L_N4_AD12P_64	AH8
PL_DDR4_A9	IO_L1P_T0L_N0_DBC_64	AC9
PL_DDR4_A10	IO_L4N_T0U_N7_DBC_AD7N_64	AE7
PL_DDR4_A11	IO_L7N_T1L_N1_QBC_AD13N_64	AH9
PL_DDR4_A12	IO_L6N_T0U_N11_AD6N_64	AC6
PL_DDR4_A13	IO_L1N_T0L_N1_DBC_64	AD9
PL_DDR4_BA0	IO_T1U_N12_64	AH6
PL_DDR4_BA1	IO_L5N_T0U_N9_AD14N_64	AC7
PL_DDR4_RAS_B	IO_T2U_N12_64	AB5
PL_DDR4_CAS_B	IO_L5P_T0U_N8_AD14P_64	AB7
PL_DDR4_WE_B	IO_L11N_T1U_N9_GC_64	AF6
PL_DDR4_ACT_B	IO_L13N_T2L_N1_GC_QBC_64	AD4
PL_DDR4_CS_B	IO_L6P_T0U_N10_AD6P_64	AB6
PL_DDR4_BG0	IO_L2N_T0L_N3_64	AE8
PL_DDR4_RST	IO_L7P_T1L_N0_QBC_AD13P_64	AG9
PL_DDR4_CLK_N	IO_L10N_T1U_N7_QBC_AD4N_64	AG5
PL_DDR4_CLK_P	IO_L10P_T1U_N6_QBC_AD4P_64	AG6
PL_DDR4_CKE	IO_T3U_N12_64	AE4
PL_DDR4_OTD	IO_L19N_T3L_N1_DBC_AD9N_64	AH4

Part 4: QSPI Flash

The FPGA core board ACU5EV is equipped with one 256MBit Quad-SPI FLASH chip to form an 8-bit bandwidth data bus, the flash model is MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U5	MT25QU256ABA1EW9	256Mbit	Winbond

Table 4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 4-1 shows the QSPI Flash in the schematic.
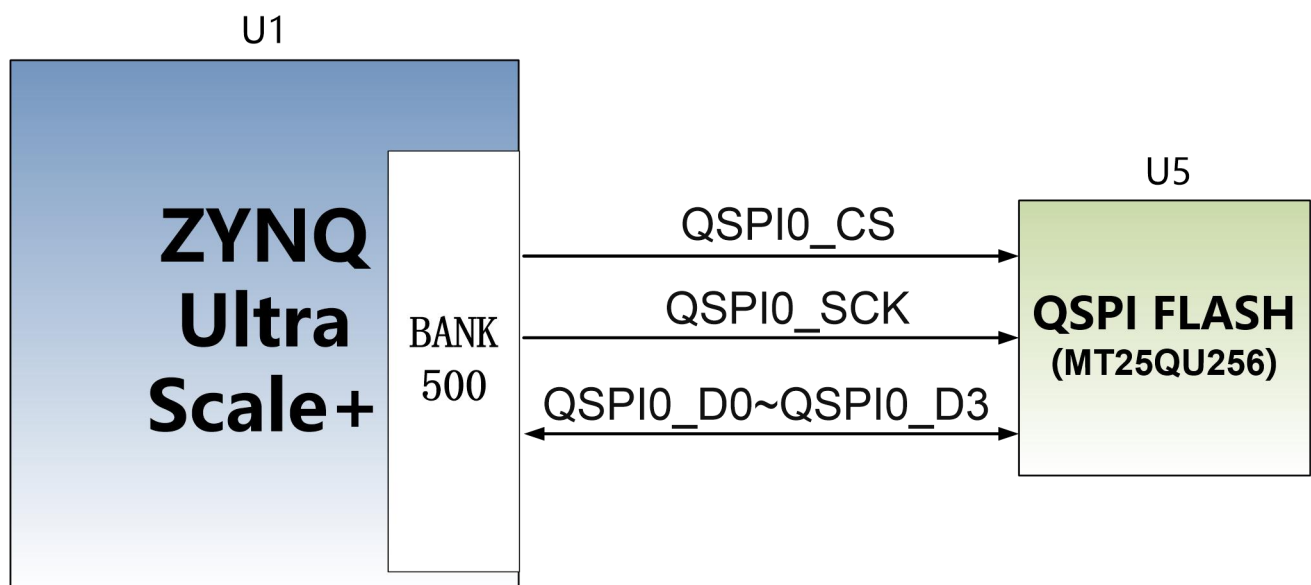
Figure 4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	Pin Name	Pin Number
MIO0_QSPI0_SCLK	PS_MIO0_500	AG15
MIO1_QSPI0_IO1	PS_MIO1_500	AG16
MIO2_QSPI0_IO2	PS_MIO2_500	AF15
MIO3_QSPI0_IO3	PS_MIO3_500	AH15
MIO4_QSPI0_IO0	PS_MIO4_500	AH16
MIO5_QSPI0_SS_B	PS_MIO5_500	AD16

Part 5: eMMC Flash

The ACU5EV core board is equipped with a large-capacity 8GB eMMC FLASH chip, the model is MTFC8GAKAJCN-4M, it supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files and other user data files The specific models and related parameters of eMMC FLASH are shown in Table 5-1.

Position	Model	Capacity	Factory
U19	MTFC8GAKAJCN-4M	8G Byte	Micron

Table 5-1: eMMC FLASH Specification

The eMMC FLASH is connected to the GPIO port of the BANK500 of the PS part of the ZYNQ UltraScale+. In the system design, it is necessary to configure the GPIO port function of the PS side as an EMMC interface. Figure 5-1 shows the part of eMMC Flash in the schematic diagram.
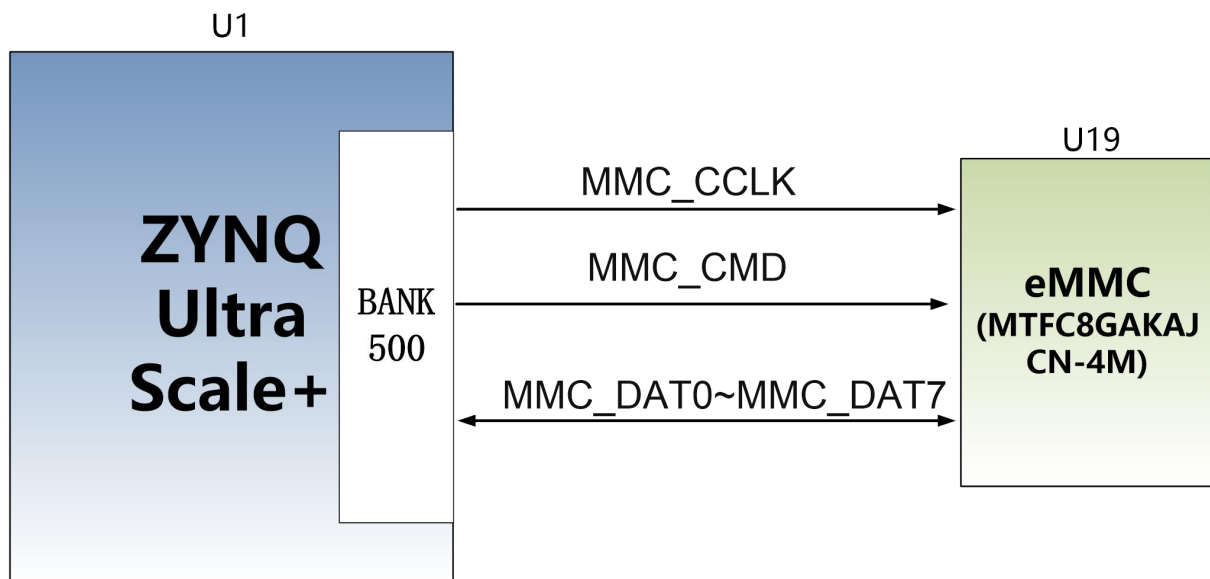
Figure 5-1: QSPI Flash in the schematic

Configuration Chip pin assignment:

Signal Name	Pin Name	Pin Number
MMC_DAT0	PS_MIO13_500	AH18
MMC_DAT1	PS_MIO14_500	AG18
MMC_DAT2	PS_MIO15_500	AE18
MMC_DAT3	PS_MIO16_500	AF18
MMC_DAT4	PS_MIO17_500	AC18
MMC_DAT5	PS_MIO18_500	AC19
MMC_DAT6	PS_MIO19_500	AE19
MMC_DAT7	PS_MIO20_500	AD19
MMC_CMD	PS_MIO21_500	AC21
MMC_CCLK	PS_MIO22_500	AB20
MMC_RSTN	PS_MIO23_500	AB18

Part 6: Clock configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 6-1:
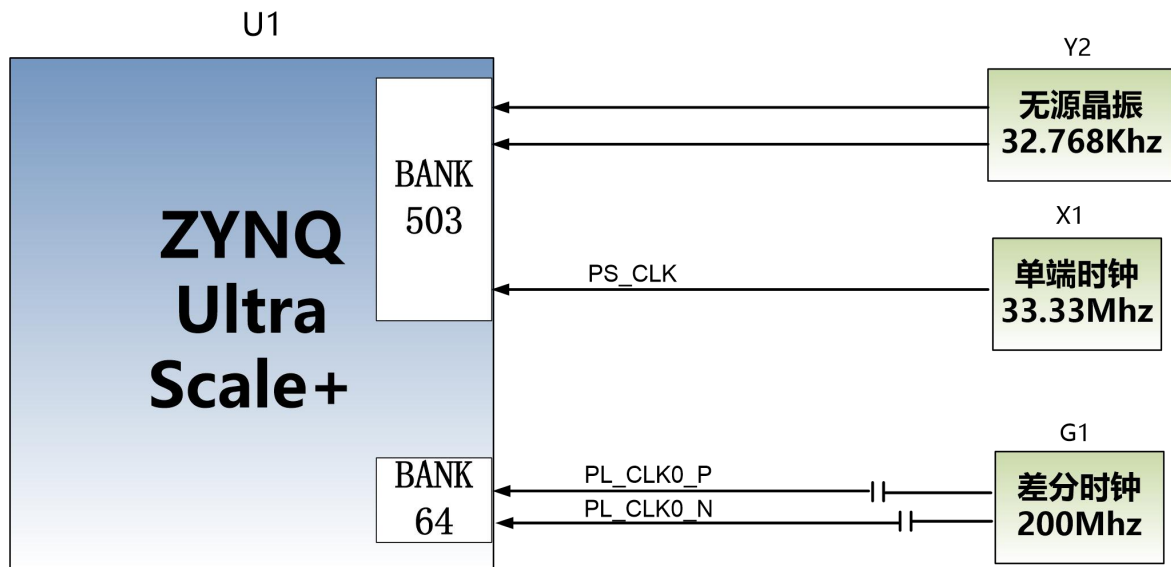
Figure 6-1: Core Board Clock Source

PS System RTC Real Time Clock

The passive crystal Y2 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the PS_PADI_503 and PS_PADO_503 pins of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 6-2:
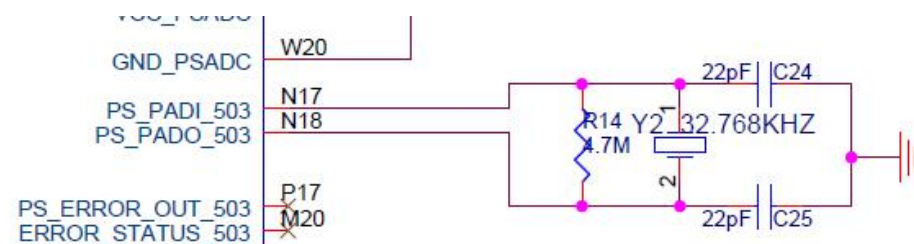
Figure 6-2: Passive Crystal Oscillator for RTC

Clock pin assignment:

Signal Name	Pin
PS_PADI_503	N17
PS_PADO_503	N18

PS System Clock Source

The X1 crystal on the core board provides a 33.333MHz clock input for the PS part. The clock input is connected to the PS_REF_CLK_503 pin of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 6-3:
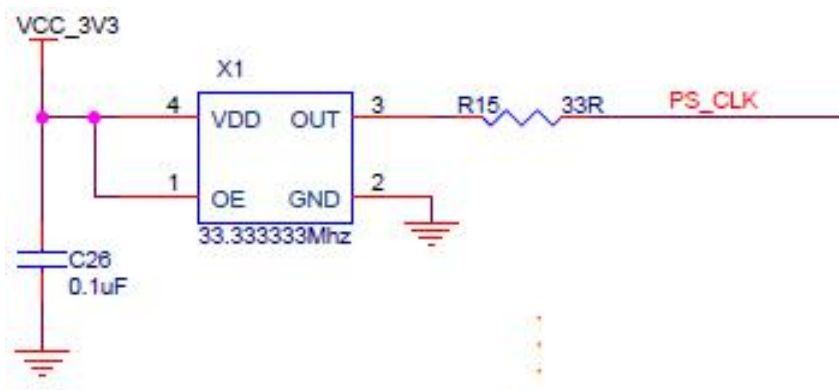
Figure 6-3: Active Crystal in PS part

Clock pin assignment:

Signal Name	Pin
PS_CLK	R16

PL System Clock Source

The core board provides a differential 200MHz PL system clock source for the reference clock of the DDR4 controller. The crystal oscillator output is connected to the global clock (MRCC) of PL BANK64. This global clock can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of this clock source is shown in Figure 6-4
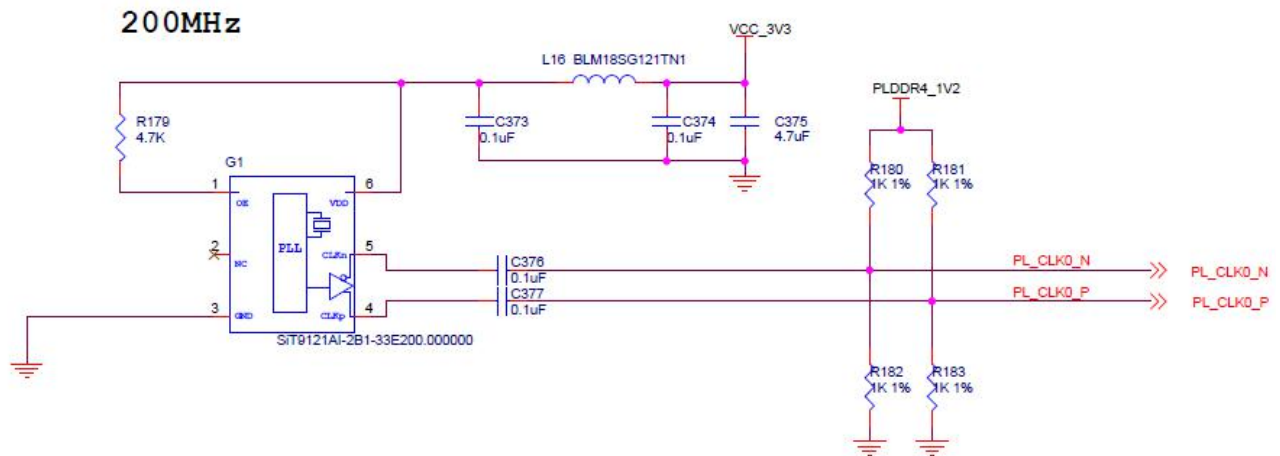
Figure 6-4: PL system clock source

Clock pin assignment:

Signal Name	Pin
PL_CLK0_P	AE5
PL_CLK0_N	AF5

Part 7: LED

There is a red power indicator (PWR) and a configuration LED (DONE) on the ACU5EV core board. When the core board is powered on, the power indicator will light up; after the FPGA configuration program, the configuration LED light will light up. The LED Schematic in the Core Board is shown in Figure 7-1:
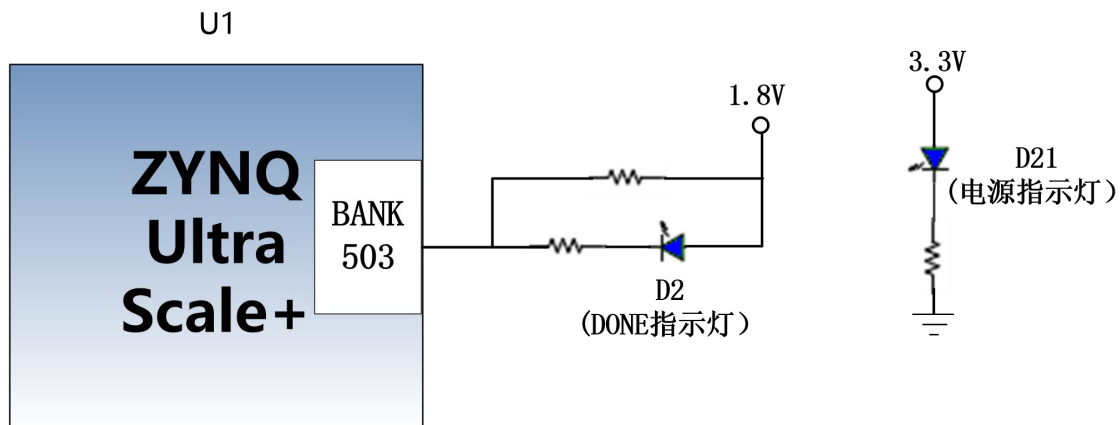
Figure 7-1: LED Schematic in the Core Board

Part 8: Power Supply

The power supply voltage of the ACU5EV core board is DC12V, which is supplied by connecting the carrier board. The core board uses a PMIC chip TPS6508641 to generate all the power required by the XCZU5EV chip. For the TPS6508641 power supply design, please refer to the power supply chip manual. The design block diagram is as follows:
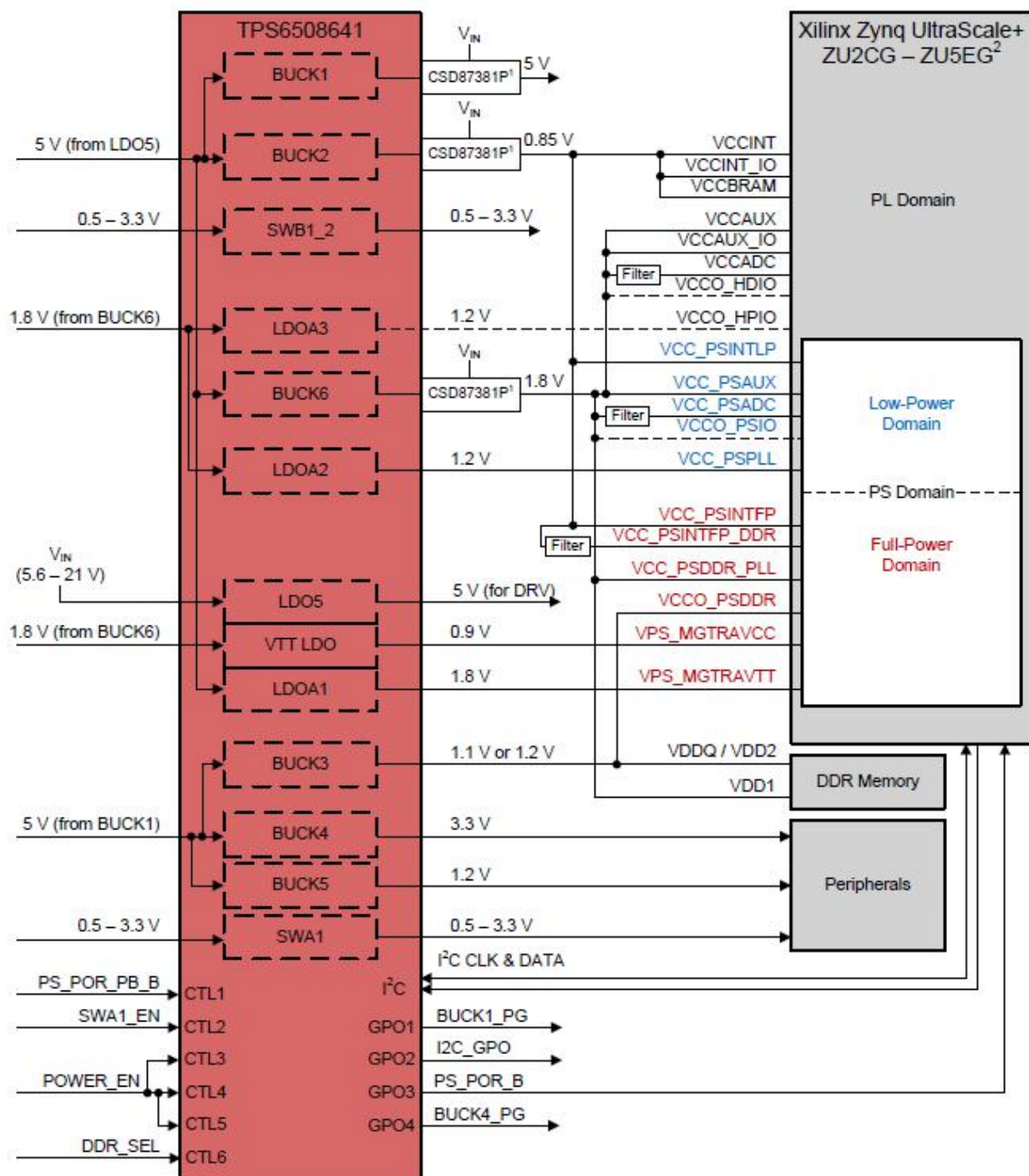
In addition, the VCCIO power supply of BANK65 and BANK66 of XCZU5EV chip is provided by the carrier board, which is convenient for users to modify, but the maximum power supply cannot exceed 1.8V.

Part 9: ACU5EV Core Board Size Dimension
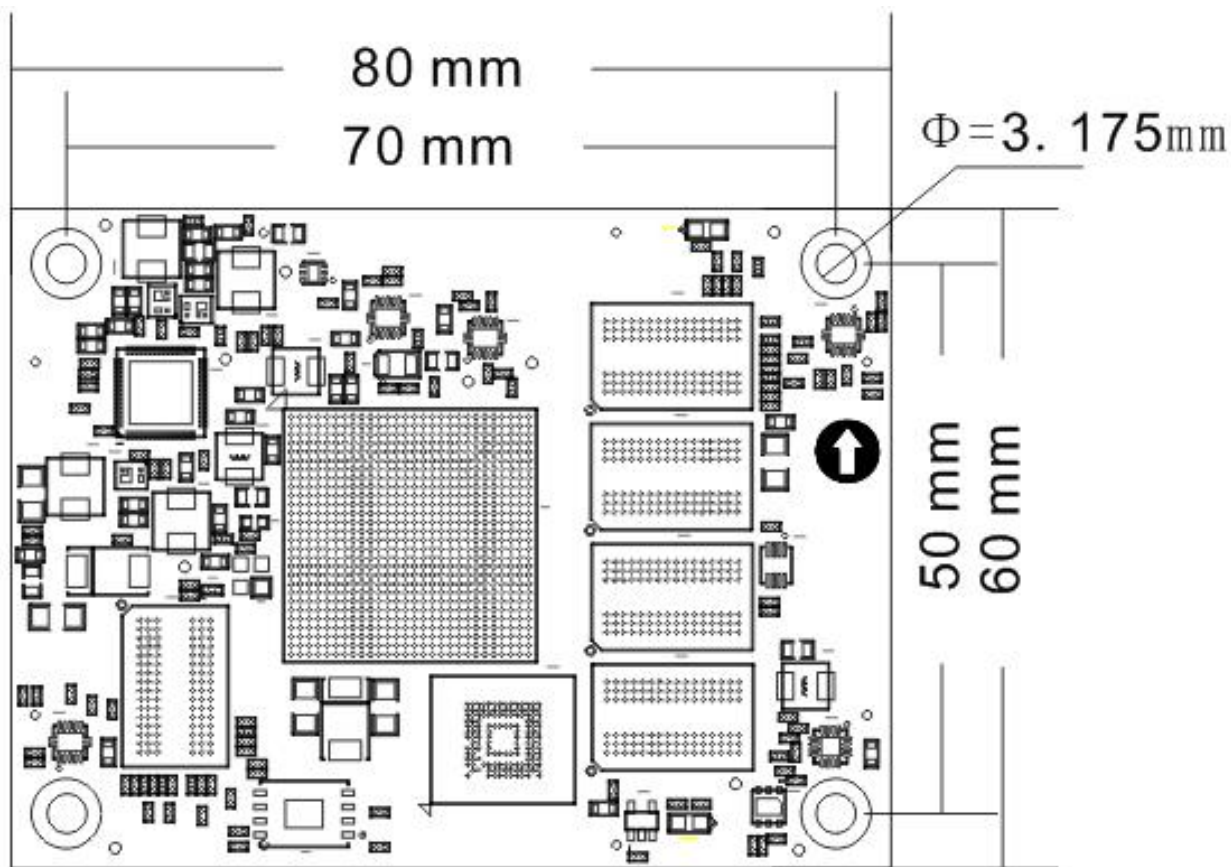
Figure 9-1: ACU5EV Core Board Size Dimension

Part 10: Board to Board Connectors pin assignment

The core board has a total of four high-speed expansion ports. It uses four 120-pin inter-board connectors (J29/J30/J31/J32) to connect to the carrier board.

The connectors used is Panasonic AXK5A2137YG, and the corresponding connector model in the carrier board is Panasonic AXK6A2337YG. Among them, J29 is connected to the IO of BANK65 and BANK66, J30 is connected to the IO of BANK25, BANK26, BANK66 and the transceiver signal of BANK505 MGT, J31 is connected to the IO of BANK24 and BANK44, J32 is connected to the MIO, VCCO_65, VCCO_66 and +12V power supply of PS.

Among them, the IO level standard of BANK43~46 is 3.3V, and the level standard of BANK65 and BANK66 is determined by the VCCO_65 and VCCO_66 power supply of the carrier board, but cannot exceed +1.8V; the level standard of MIO is also 1.8V.

Pin assignment of board to board connector J29

J29 Pin	Signal Name	Pin Number	J29 Pin	Signal Name	Pin Number
1	B65_L2_N	V9	2	B65_L22_P	K8
3	B65_L2_P	U9	4	B65_L22_N	K7
5	GND	-	6	GND	-
7	B65_L4_N	T8	8	B65_L20_P	J6
9	B65_L4_P	R8	10	B65_L20_N	H6
11	GND	-	12	GND	-
13	B65_L1_N	Y8	14	B65_L6_N	T6
15	B65_L1_P	W8	16	B65_L6_P	R6
17	GND	-	18	GND	-
19	B65_L7_P	L1	20	B65_L17_P	N9
21	B65_L7_N	K1	22	B65_L17_N	N8
23	GND	-	24	GND	-

25	B65_L15_P	N7	26	B65_L9_P	K2
27	B65_L15_N	N6	28	B65_L9_N	J2
29	GND	-	30	GND	-
31	B65_L16_P	P7	32	B65_L3_N	V8
33	B65_L16_N	P6	34	B65_L3_P	U8
35	GND	-	36	GND	-
37	B65_L14_P	M6	38	B65_L19_P	J5
39	B65_L14_N	L5	40	B65_L19_N	J4
41	GND	-	42	GND	-
43	B65_L5_N	T7	44	B65_L18_P	M8
45	B65_L5_P	R7	46	B65_L18_N	L8
47	GND	-	48	GND	-
49	B65_L11_N	K3	50	B65_L8_P	J1
51	B65_L11_P	K4	52	B65_L8_N	H1
53	GND	-	54	GND	-
55	B65_L10_N	H3	56	B65_L24_N	H8
57	B65_L10_P	H4	58	B65_L24_P	H9
59	GND	-	60	GND	-
61	B66_L3_P	F2	62	B65_L12_P	L3
63	B66_L3_N	E2	64	B65_L12_N	L2
65	GND	-	66	GND	-
67	B66_L1_P	G1	68	B65_L13_N	L6
69	B66_L1_N	F1	70	B65_L13_P	L7
71	GND	-	72	GND	-
73	B66_L6_P	G5	74	B65_L21_P	J7
75	B66_L6_N	F5	76	B65_L21_N	H7
77	GND	-	78	GND	-
79	B66_L16_P	G8	80	B65_L23_P	K9
81	B66_L16_N	F7	82	B65_L23_N	J9
83	GND	-	84	GND	-
85	B66_L15_P	G6	86	B66_L5_N	E3
87	B66_L15_N	F6	88	B66_L5_P	E4
89	GND	-	90	GND	-
91	B66_L4_P	G3	92	B66_L2_P	E1
93	B66_L4_N	F3	94	B66_L2_N	D1
95	GND	-	96	GND	-

97	B66_L11_P	D4	98	B66_L20_P	C6
99	B66_L11_N	C4	100	B66_L20_N	B6
101	GND	-	102	GND	-
103	B66_L12_P	C3	104	B66_L7_P	C1
105	B66_L12_N	C2	106	B66_L7_N	B1
107	GND	-	108	GND	-
109	B66_L13_N	D6	110	B66_L10_P	B4
111	B66_L13_P	D7	112	B66_L10_N	A4
113	GND	-	114	GND	-
115	B66_L8_N	A1	116	B66_L9_P	B3
117	B66_L8_P	A2	118	B66_L9_N	A3
119	GND	-	120	GND	-

Pin assignment of board to board connector J30

J30 Pin	Signal Name	Pin Number	J30 Pin	Signal Name	Pin Number
1	B66_L14_P	E5	2	FPGA_TDI	R18
3	B66_L14_N	D5	4	FPGA_TCK	R19
5	GND	-	6	GND	-
7	B66_L22_P	C8	8	FPGA_TDO	T21
9	B66_L22_N	B8	10	FPGA_TMS	N21
11	GND	-	12	GND	-
13	B66_L19_N	A5	14	B66_L21_N	A6
15	B66_L19_P	B5	16	B66_L21_P	A7
17	GND	-	18	GND	-
19	B66_L24_P	C9	20	B66_L17_P	F8
21	B66_L24_N	B9	22	B66_L17_N	E8
23	GND	-	24	GND	-
25	B66_L23_N	A8	26	B25_L9_P	C11
27	B66_L23_P	A9	28	B25_L9_N	B10
29	GND	-	30	GND	-
31	B25_L5_N	F10	32	B25_L10_P	B11
33	B25_L5_P	G11	34	B25_L10_N	A10
35	GND	-	36	GND	-
37	B66_L18_N	D9	38	B25_L12_P	D12
39	B66_L18_P	E9	40	B25_L12_N	C12
41	GND	-	42	GND	-
43	B25_L4_N	H12	44	B25_L11_P	A12

45	B25_L4_P	J12	46	B25_L11_N	A11
47	GND	-	48	GND	-
49	B26_L11_P	K14	50	B25_L6_N	F11
51	B26_L11_N	J14	52	B25_L6_P	F12
53	GND	-	54	GND	-
55	B26_L10_N	H13	56	B26_L6_N	E13
57	B26_L10_P	H14	58	B26_L6_P	E14
59	GND	-	60	GND	-
61	B26_L7_N	F13	62	B26_L3_N	A13
63	B26_L7_P	G13	64	B26_L3_P	B13
65	GND	-	66	GND	-
67	B26_L9_N	G14	68	B26_L2_N	A14
69	B26_L9_P	G15	70	B26_L2_P	B14
71	GND	-	72	GND	-
73	B26_L5_N	D14	74	B26_L4_N	C13
79	B26_L5_P	D15	76	B26_L4_P	C14
77	GND	-	78	GND	-
79	B26_L1_P	B15	80	B26_L12_P	L14
81	B26_L1_N	A15	82	B26_L12_N	L13
83	GND	-	84	GND	-
85	505_CLK2_P	C21	86	505_CLK1_P	E21
87	505_CLK2_P	C22	88	505_CLK1_P	E22
89	GND	-	90	GND	-
91	505_CLK0_P	F23	92	505_CLK3_P	A21
93	505_CLK0_N	F24	94	505_CLK3_N	A22
95	GND	-	96	GND	-
97	505_TX3_P	B23	98	505_TX1_P	D23
99	505_TX3_N	B24	100	505_TX1_N	D24
101	GND	-	102	GND	-
103	505_RX3_P	A25	104	505_TX0_P	E25
105	505_RX3_N	A26	106	505_TX0_N	E26
107	GND	-	108	GND	-
109	505_TX2_P	C25	110	505_RX1_P	D27
111	505_TX2_N	C26	112	505_RX1_N	D28
113	GND	-	114	GND	-
115	505_RX2_P	B27	116	505_RX0_P	F27

| 117 | 505_RX2_N | B28 | 118 | 505_RX0_N | F28 |
| 119 | GND | - | 120 | GND | - |

Pin assignment of board to board connector J31

J31 Pin	Signal Name	Pin Number	J31 Pin	Signal Name	Pin Number
1	B24_L10_P	Y14	2	B24_L7_P	AA13
3	B24_L10_N	Y13	4	B24_L7_N	AB13
5	GND	-	6	GND	-
7	B24_L6_P	AC14	8	B44_L6_P	AC12
9	B24_L6_N	AC13	10	B44_L6_N	AD12
11	GND	-	12	GND	-
13	B24_L5_P	AD15	14	B44_L7_P	AD11
15	B24_L5_N	AD14	16	B44_L7_N	AD10
17	GND	-	18	GND	-
19	B24_L1_P	AE15	20	B44_L8_N	AC11
21	B24_L1_N	AE14	22	B44_L8_P	AB11
23	GND	-	24	GND	-
25	B24_L12_P	Y12	26	B24_L2_P	AG14
27	B24_L12_N	AA12	28	B24_L2_N	AH14
29	GND	-	30	GND	-
31	B24_L3_P	AG13	32	-	-
33	B24_L3_N	AH13	34	-	-
35	GND	-	36	GND	-
37	B44_L12_N	AB9	38	B44_L9_P	AA11
39	B44_L12_P	AB10	40	B44_L9_N	AA10
41	GND	-	42	GND	-
43	B44_L10_N	Y10	44	B44_L3_P	AH12
45	B44_L10_P	W10	46	B44_L3_N	AH11
47	GND	-	48	GND	-
49	B24_L11_N	W11	50	B44_L1_N	AH10
51	B24_L11_P	W12	52	B44_L1_P	AG10
53	GND	-	54	GND	-
55	B24_L9_N	W13	56	B24_L4_P	AE13
57	B24_L9_P	W14	58	B24_L4_N	AF13
59	GND	-	60	GND	-

61	B24_L8_P	AB15	62	B44_L5_P	AE12
63	B24_L8_N	AB14	64	B44_L5_N	AF12
65	GND	-	66	GND	-
67	B44_L2_N	AG11	68	B44_L4_N	AF10
69	B44_L2_P	AF11	70	B44_L4_P	AE10
71	GND	-	72	GND	-
73	VBAT_IN	Y18	74	B44_L11_P	Y9
75	MR	-	76	B44_L11_N	AA8
77	GND	-	78	GND	-
79	-	-	80	PS_POR_B	P16
81	-	-	82	-	-
83	GND	-	84	GND	-
86	-	-	86	-	-
87	-	-	88	-	-
89	GND	-	90	GND	-
91	224_CLK0_P	Y6	92	224_CLK1_P	V6
93	224_CLK0_N	Y5	94	224_CLK1_N	V5
95	GND	-	96	GND	-
97	224_RX3_P	P2	98	224_TX3_P	N4
99	224_RX3_N	P1	100	224_TX3_N	N3
101	GND	-	102	GND	-
103	224_RX2_P	T2	104	224_TX2_P	R4
105	224_RX2_N	T1	106	224_TX2_N	R3
107	GND	-	108	GND	-
109	224_RX1_P	V2	110	224_TX1_P	U4
111	224_RX1_N	V1	112	224_TX1_N	U3
113	GND	-	114	GND	-
115	224_RX0_P	Y2	116	224_TX0_P	W4
117	224_RX0_N	Y1	118	224_TX0_N	W3
119	GND	-	120	GND	-

Pin assignment of board to board connector J32

J32 Pin	Signal Name	Pin Number	J32 Pin	Signal Name	Pin Number
1	PS_MIO35	H17	2	PS_MIO30	F16
3	PS_MIO29	G16	4	PS_MIO31	H16

5	GND	-	-	GND	-
7	-	-	8	PS_MIO58	F18
9	-	-	10	PS_MIO53	D16
11	GND	-	12	GND	-
13	PS_MODE0	P19	14	PS_MIO52	G18
15	PS_MODE1	P20	16	PS_MIO55	B16
17	GND	-	18	GND	-
19	PS_MODE2	R20	20	PS_MIO56	C16
21	PS_MODE3	T20	22	PS_MIO57	A16
23	GND	-	24	GND	-
25	PS_MIO36	K17	26	PS_MIO54	F17
27	PS_MIO37	J17	28	PS_MIO27	J15
29	GND	-	30	GND	-
31	-	-	32	PS_MIO28	K15
33	PS_MIO77	F20	34	PS_MIO59	E17
35	GND	-	36	GND	-
37	PS_MIO76	B20	38	PS_MIO60	C17
39	-	-	40	PS_MIO61	D17
41	GND	-	42	GND	-
43	PS_MIO39	H19	44	PS_MIO62	A17
45	PS_MIO38	H18	46	PS_MIO63	E18
47	GND	-	48	GND	-
49	-	-	50	PS_MIO65	A18
51	PS_MIO40	K18	52	PS_MIO66	G19
53	GND	-	54	GND	-
55	PS_MIO44	J20	56	PS_MIO67	B18
57	PS_MIO45	K20	58	PS_MIO68	C18
59	GND	-	60	GND	-
61	PS_MIO47	H21	62	PS_MIO64	E19
63	PS_MIO48	J21	64	PS_MIO69	D19
65	GND	-	66	GND	-
67	PS_MIO41	J19	68	PS_MIO74	D20
69	PS_MIO32	J16	70	PS_MIO73	G21
71	GND	-	72	GND	-
73	PS_MIO46	L20	74	PS_MIO72	G20
75	PS_MIO50	M19	76	PS_MIO71	B19

77	GND	-	78	GND	-
79	PS_MIO49	M18	80	PS_MIO75	A19
81	PS_MIO34	L17	82	PS_MIO70	C19
83	GND	-	84	GND	-
85	PS_MIO26	L15	86	PS_MIO43	K19
87	PS_MIO24	AB19	88	PS_MIO51	L21
89	GND	-	90	GND	-
91	PS_MIO25	AB21	92	PS_MIO42	L18
93	-	-	94	PS_MIO33	L16
95	GND	-	96	GND	-
97	-	-	98	-	-
99	VCCO_65	-	100	VCCO_66	-
101	VCCO_65	-	102	VCCO_66	-
103	VCCO_65	-	104	VCCO_66	-
105	GND	-	106	GND	-
107	+12V	-	108	+12V	-
109	+12V	-	110	+12V	-
111	+12V	-	112	+12V	-
113	+12V	-	114	+12V	-
115	+12V	-	116	+12V	-
117	+12V	-	118	+12V	-
119	+12V	-	120	+12V	-