# 16-channel GMSL2 On-board Camera Acquisition Module

# FH9712

# User Manual

**Rev 1.0**

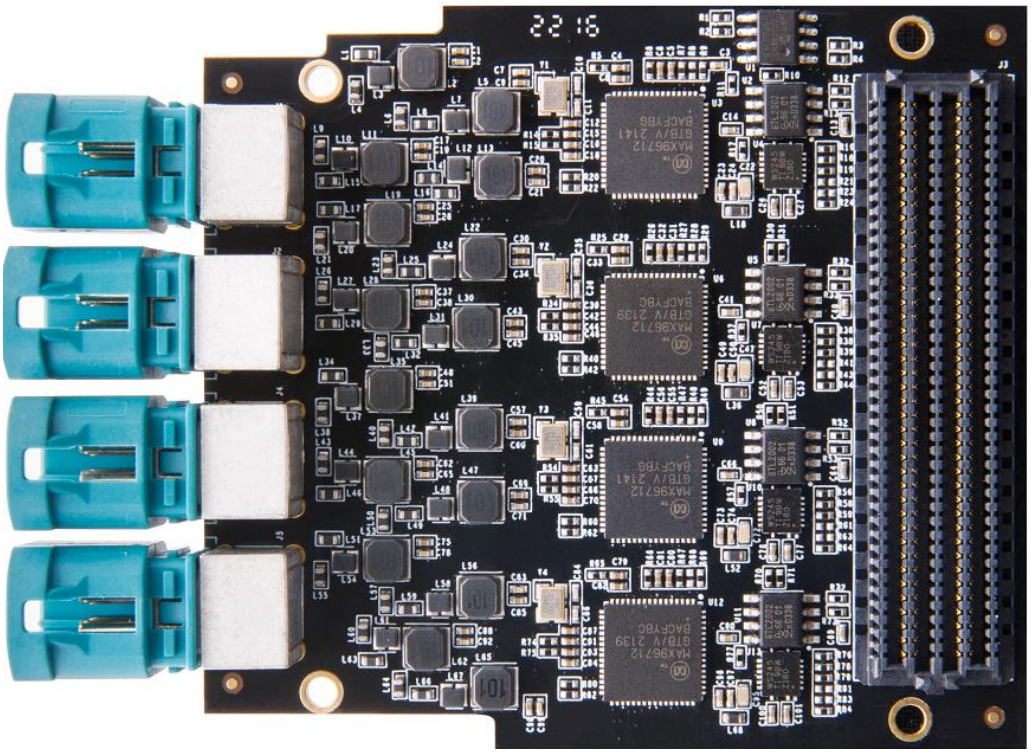
ALINX

# Part 1: Introduction of Module FH9712

FH9712 is a 16-channel GMSL2/GMSL1 camera acquisition module, which uses four decoder chips MAX96712 to decode 16-channel camera videos. The MAX96712 chip is an automotive-grade 4-channel serial decoder that supports 3Gbps and 6Gbps serial speeds and supports the first-generation GMSL1 and second-generation GMSL2 standards. The camera interface uses a 4-in-1 FAKRA coaxial connector.

The four MAX96712 chips are converted into four 4-LANE MIPI signals to connect to the FPGA development board of ALINX through FMC interface to realize the conversion and transmission of video images. The FMC interface is a standard LPC interface that meets the VITA 57.1 standard. The model of the FMC connector is ASP_134604_01.

The picture of module FH9712 is as follows:



Picture of Module FH9712

## 1.1 Parameters of Module FH9712

1) Support multi-channel GMSL1/2 camera input

It supports 16-channel cameras, 8MP resolution cameras as the highest

2) Cable length

Up to 40m (3Gbps) in GMSL1 mode

Up to 20 m (6Gbps) in GMSL2 mode

3) AG connector

Use Amphenol Z Code FAKRA AG coaxial connectors

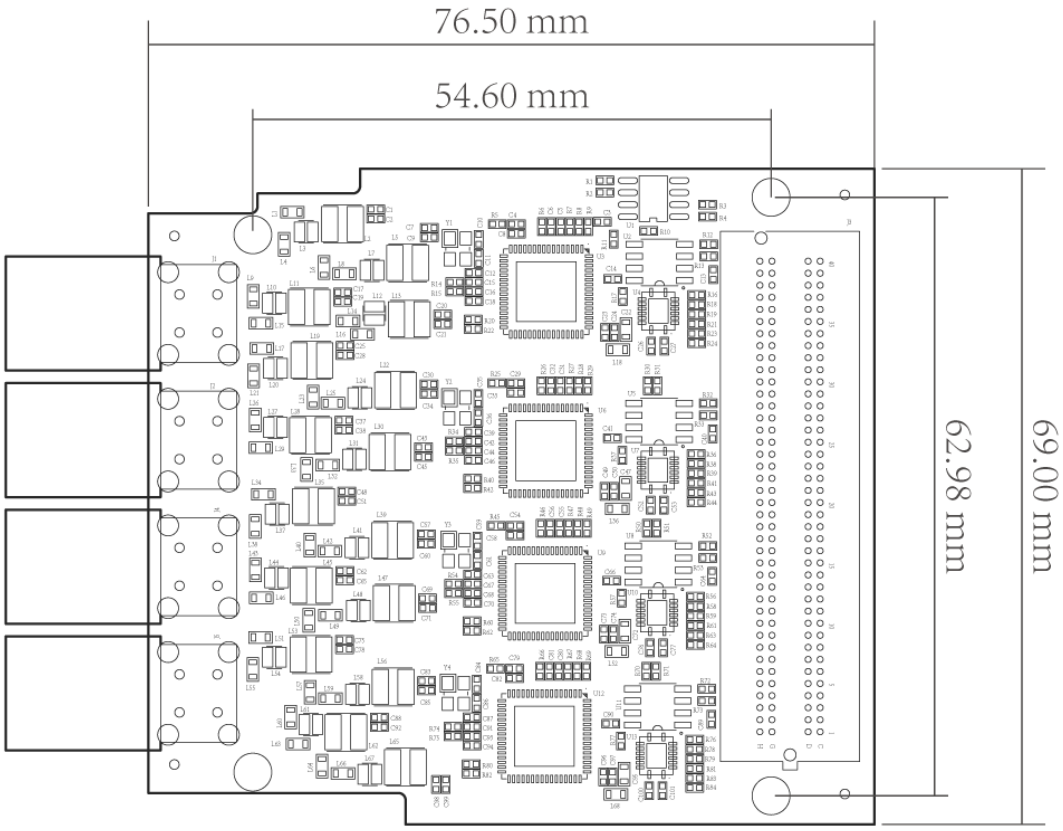
4) Input image format

It supports RAW8/10/12/14/16/20, RGB565/666/888, YUV422 8/10bit video image formats. The remote camera can be configured via I2C

5) FMC interface

Standard LPC connector, four 4-LANE MIPI CSI-2 v1.3 interface, data rate up to 2500Mbps.

## 1.2 Structure Diagram of Module FH9712

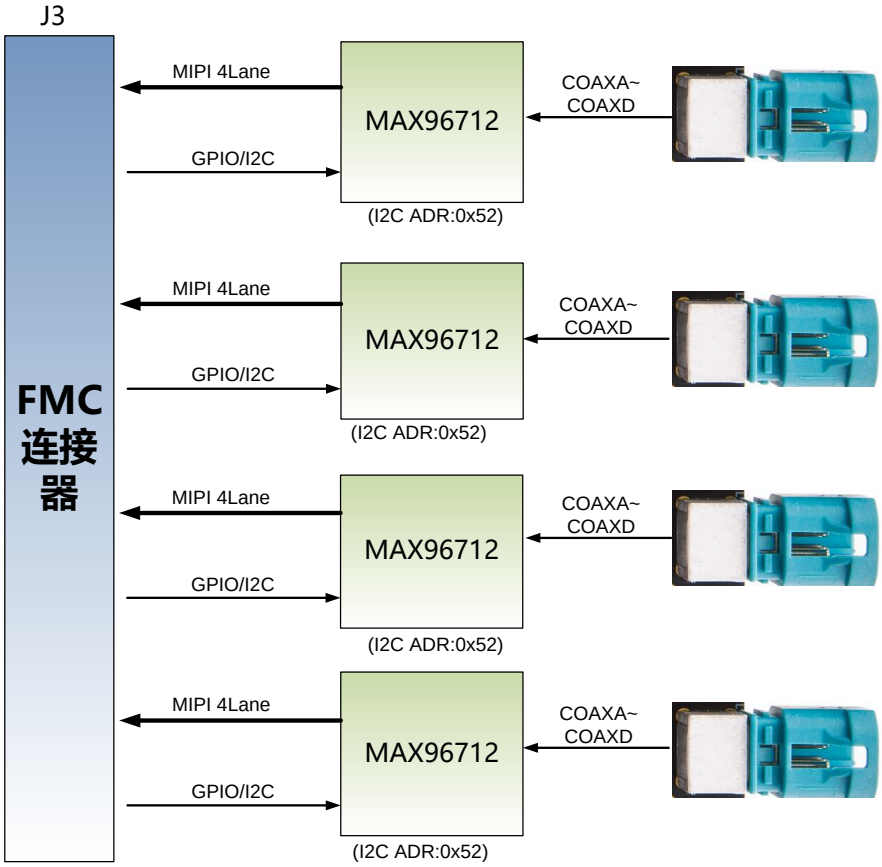



FH9712 Structure Diagram

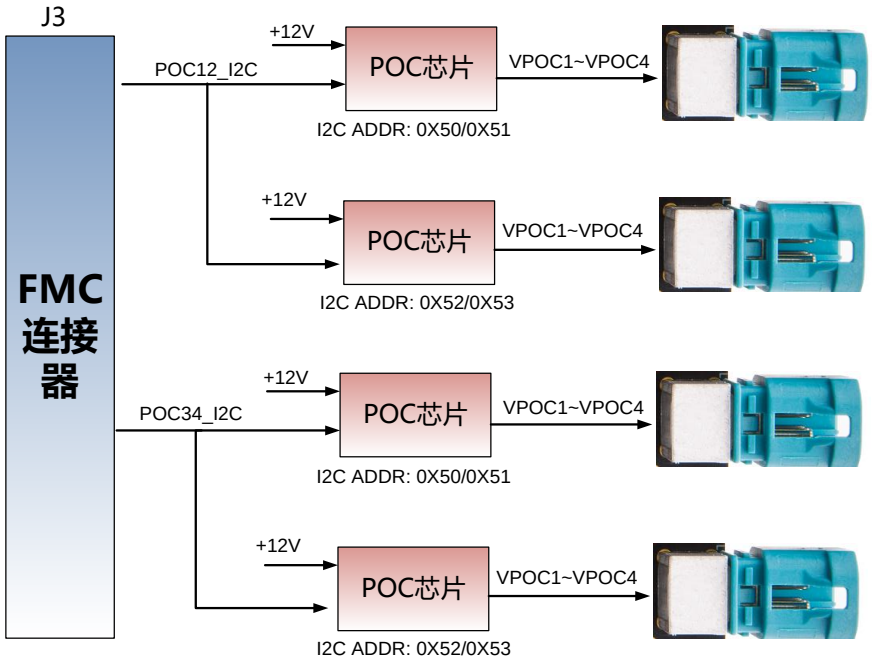
# Part 2: Functions of Module FH9712

## 2.1 Schematic diagram of the module FH9712

The schematic design diagram of the module FH9712 is as follows:




**Design diagram of video input**




**Design diagram of POC power supply**

## 2.2 Pin assignment of Module FMC LPC

Only the signals are listed below, and the power and GND signals are not listed. The following figure is the pin assignment of FH9712 and Z7-P development board.

| FMC Pin No. | Signal Name | FPGA Pin No. | Description |
|---|---|---|---|
| G15 | G1_CKAP | AL20 | 1st-channel MIPI clock P |
| G16 | G1_CKAN | AL21 | 1st-channel MIPI clock N |
| C10 | G1_DA0P | AL22 | 1st-channel MIPI data 0P |
| C11 | G1_DA0N | AL23 | 1st-channel MIPI data 0N |
| D14 | G1_DA1P | AK22 | 1st-channel MIPI data 1P |
| D15 | G1_DA1N | AK23 | 1st-channel MIPI data 1N |
| G12 | G1_DA2P | AJ20 | 1st-channel MIPI data 2P |
| G13 | G1_DA2N | AK20 | 1st-channel MIPI data 2N |
| H13 | G1_DA3P | AJ19 | 1st-channel MIPI data 3P |
| H14 | G1_DA3N | AK19 | 1st-channel MIPI data 3N |
| G7 | G1_GPI0 | AJ22 | 1st-channel MAX96712 input GPI0 |
| G6 | G1_GPI1 | AJ21 | 1st-channel MAX96712 input GPI1 |
| G9 | G1_GPI2 | AF21 | 1st-channel MAX96712 input GPI2 |
| G10 | G1_GPI3 | AF22 | 1st-channel MAX96712 input GPI3 |
| D8 | GMSL1_SCL | AG21 | 1st-channel MAX96712 I2C clock |
| D9 | GMSL1_SDA | AH21 | 1st-channel MAX96712 I2C data |
| H5 | G1_PWDN_B | AK17 | 1st-channel MAX96712 POWER DONW |
| C18 | G2_CKAP | AE18 | 2nd-channel MIPI clock P |

| | | | |
|---|---|---|---|
| C19 | G2_CKAN | AE19 | 2nd-channel MIPI clock N |
| H19 | G2_DA0P | AA18 | 2nd-channel MIPI data 0P |
| H20 | G2_DA0N | AB18 | 2nd-channel MIPI data 0N |
| G18 | G2_DA1P | AC18 | 2nd-channel MIPI data 1P |
| G19 | G2_DA1N | AD19 | 2nd-channel MIPI data 1N |
| D17 | G2_DA2P | AD20 | 2nd-channel MIPI data 2P |
| D18 | G2_DA2N | AE20 | 2nd-channel MIPI data 2N |
| H16 | G2_DA3P | AB19 | 2nd-channel MIPI data 3P |
| H17 | G2_DA3N | AC19 | 2nd-channel MIPI data 3N |
| H7 | G2_GPI1 | AN22 | 2nd-channel MAX96712 input GPI0 |
| H8 | G2_GPI0 | AP23 | 2nd-channel MAX96712 input GPI1 |
| H10 | G2_GPI2 | AM21 | 2nd-channel MAX96712 input GPI2 |
| H11 | G2_GPI3 | AN21 | 2nd-channel MAX96712 input GPI3 |
| C14 | GMSL2_SCL | AP19 | 2nd-channel MAX96712 I2C clock |
| C15 | GMSL2_SDA | AP20 | 2nd-channel MAX96712 I2C data |
| H4 | G2_PWDN_B | AJ17 | 2nd-channel MAX96712 POWER DONW |
| D26 | G3_CKAP | AP18 | 3rd-channel MIPI clock P |
| D27 | G3_CKAN | AP17 | 3rd-channel MIPI clock N |
| C26 | G3_DA0P | AN13 | 3rd-channel MIPI data 0P |
| C27 | G3_DA0N | AP13 | 3rd-channel MIPI data 0N |
| D23 | G3_DA1P | AM18 | 3rd-channel MIPI data 1P |
| D24 | G3_DA1N | AN18 | 3rd-channel MIPI data 1N |
| G24 | G3_DA2P | AM14 | 3rd-channel MIPI data 2P |
| G25 | G3_DA2N | AN14 | 3rd-channel MIPI data 2N |
| H25 | G3_DA3P | AP16 | 3rd-channel MIPI data 3P |
| H26 | G3_DA3N | AP15 | 3rd-channel MIPI data 3N |
| D21 | G3_GPI0 | AG18 | 3rd-channel MAX96712 input GPI0 |
| D20 | G3_GPI1 | AF18 | 3rd-channel MAX96712 input GPI1 |
| C22 | G3_GPI2 | AH18 | 3rd-channel MAX96712 input GPI2 |
| C23 | G3_GPI3 | AH17 | 3rd-channel MAX96712 input GPI3 |
| H22 | GMSL3_SCL | AM16 | 3rd-channel MAX96712 I2C clock |
| H23 | GMSL3_SDA | AM15 | 3rd-channel MAX96712 I2C data |
| G3 | G3_PWDN_B | AJ15 | 3rd-channel MAX96712 POWER DONW |
| G30 | G4_CKAP | AD15 | 4th-channel MIPI clock P |
| G31 | G4_CKAN | AE15 | 4th-channel MIPI clock N |
| H37 | G4_DA0P | AB16 | 4th-channel MIPI data 0P |
| H38 | G4_DA0N | AB15 | 4th-channel MIPI data 0N |
| G33 | G4_DA1P | AC17 | 4th-channel MIPI data 1P |
| G34 | G4_DA1N | AC16 | 4th-channel MIPI data 1N |
| G36 | G4_DA2P | AA14 | 4th-channel MIPI data 2P |
| G37 | G4_DA2N | AB14 | 4th-channel MIPI data 2N |
| H34 | G4_DA3P | AA16 | 4th-channel MIPI data 3P |
| H35 | G4_DA3N | AA15 | 4th-channel MIPI data 3N |

| | | | |
|---|---|---|---|
| G28 | G4_GPI0 | AK14 | 4th-channel MAX96712 input GPI0 |
| G27 | G4_GPI1 | AK15 | 4th-channel MAX96712 input GPI1 |
| H28 | G4_GPI2 | AH14 | 4th-channel MAX96712 input GPI2 |
| H29 | G4_GPI3 | AJ14 | 4th-channel MAX96712 input GPI3 |
| H31 | GMSL4_SCL | AF16 | 4th-channel MAX96712 I2C clock |
| H32 | GMSL4_SDA | AF15 | 4th-channel MAX96712 I2C data |
| G2 | G4_PWDN_B | AJ16 | 4th-channel MAX96712 POWER DONW |
| D11 | POC12_SCL | AG19 | I2C clock of POC12 power chip |
| D12 | POC12_SDA | AG20 | I2C data of POC12 power chip |
| G21 | POC34_SCL | AE17 | I2C clock of POC34 power chip |
| G22 | POC34_SDA | AF17 | I2C data of POC34 power chip |
| C30 | FMC_SCL | M10 | I2C clock of FMC |
| C31 | FMC_SDA | L10 | I2C data of FMC |

# Part 3: Installation of FMC Module

At present, FH9712 module can only be adapted to three development boards: Z7-P, Z19 and Z19-P. The following is the installation diagram of FH9712 module and Z7-P.


The images acquired by 16-channel videos are transmitted through PCIE, displayed and analyzed by AI on the computer interface.


FPGA+GPU 实现
16路车载摄像头实
时AI智能分析显示
0:15 / 0:15