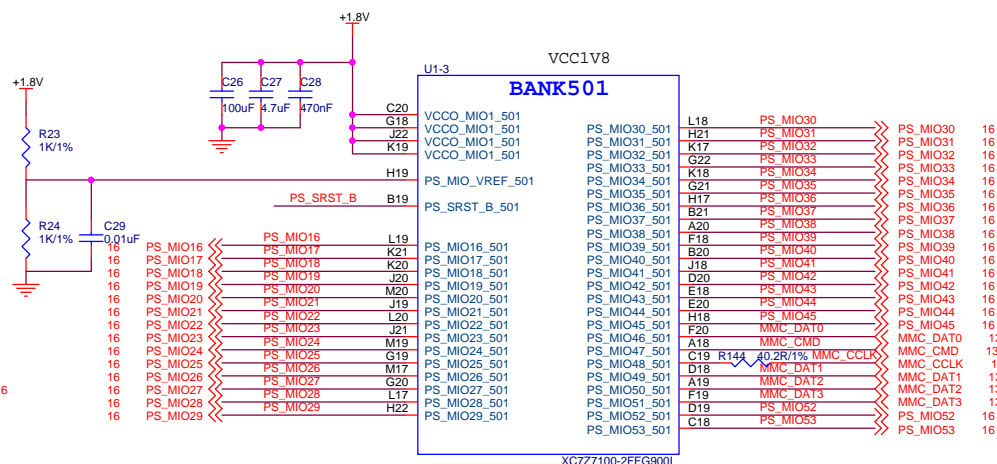
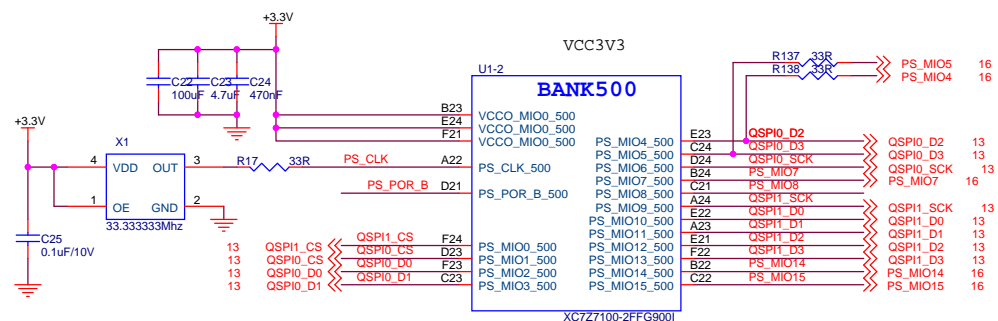
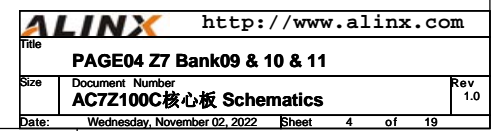
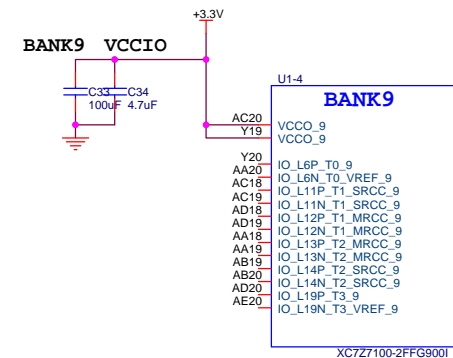


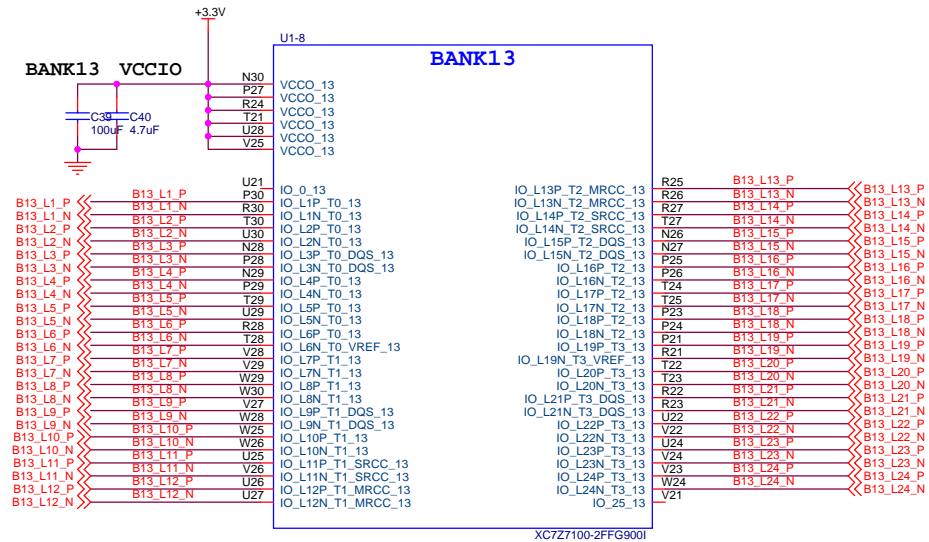
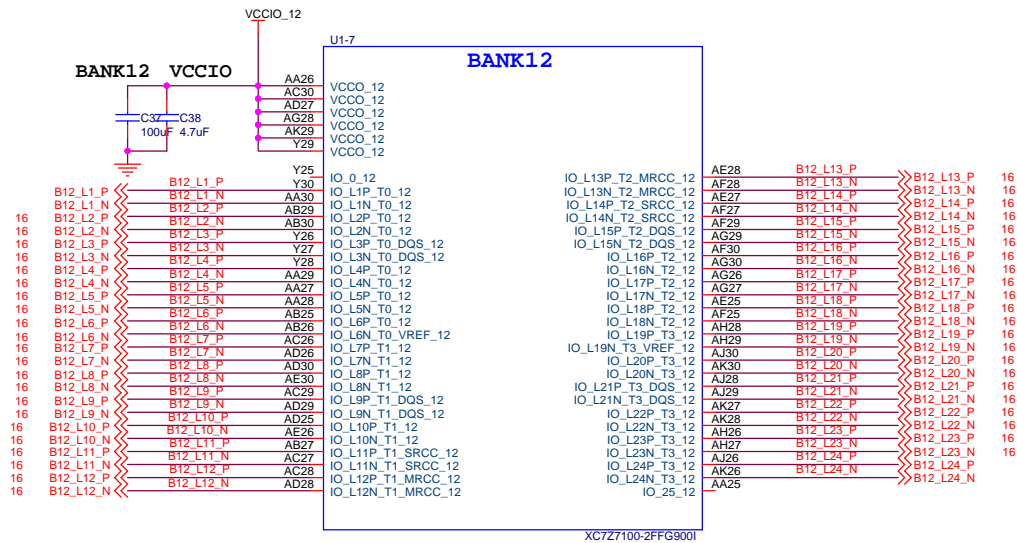
**BOOT OPTION**

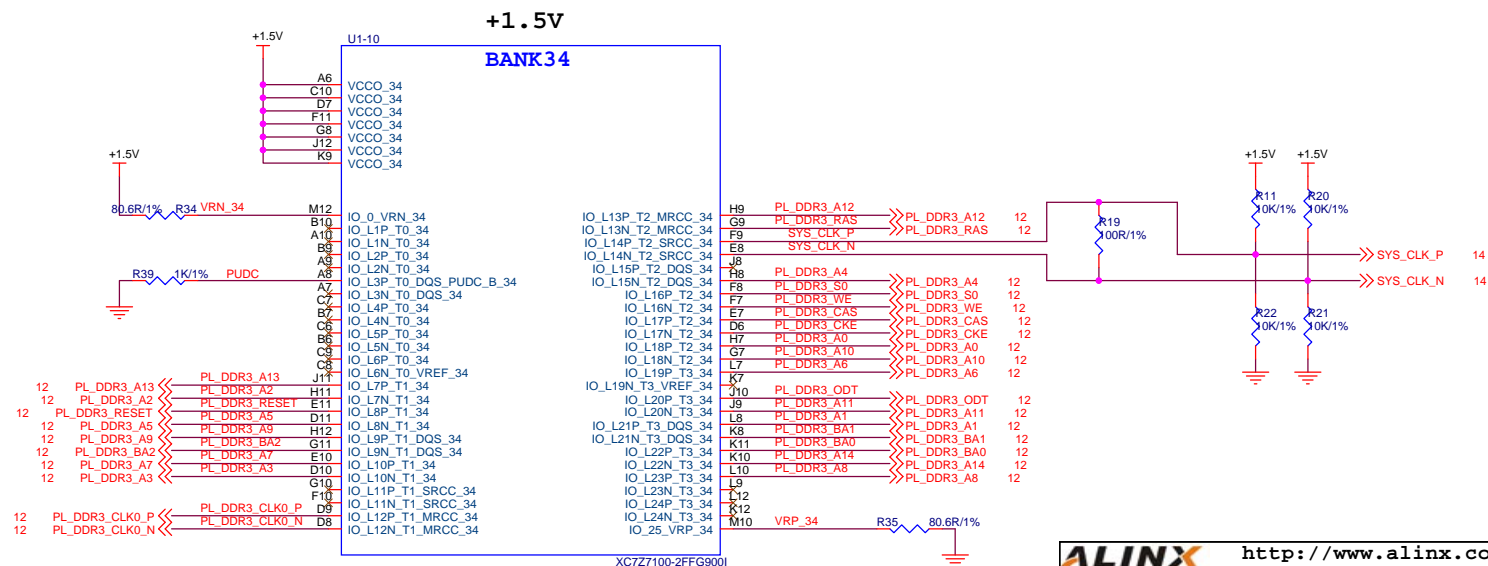
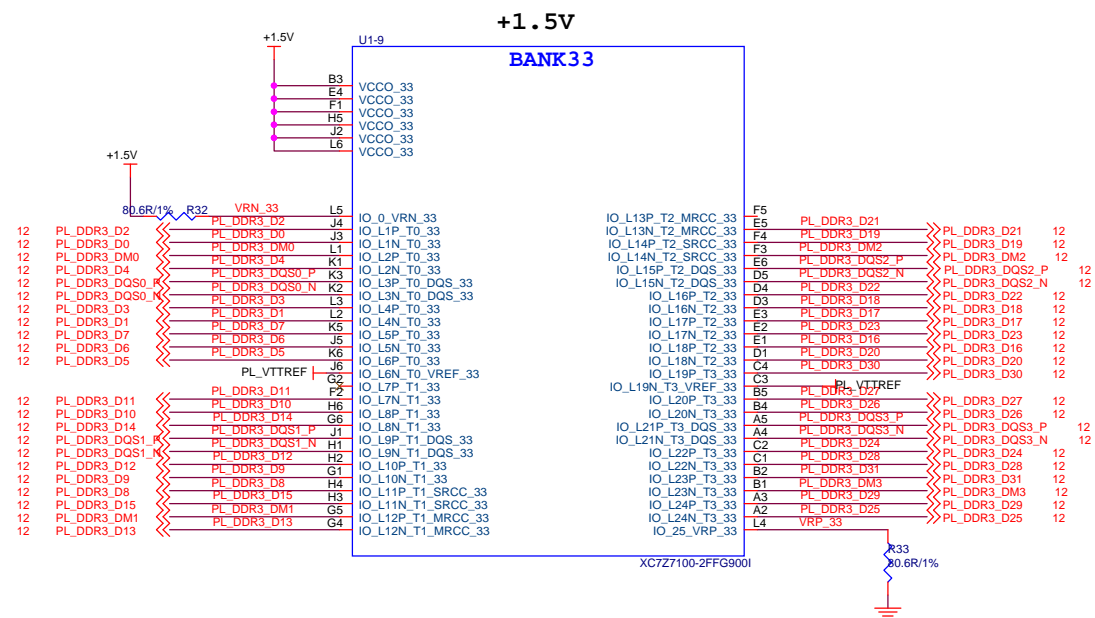
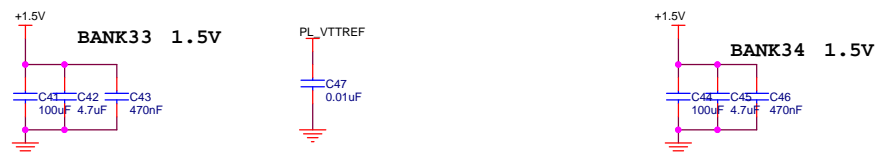
+3.3V  
 R14 20K PS\_MIO8  
 R13 20K QSPI0\_D0  
 R15 20K QSPI0\_D1  
 R18 20K QSPI0\_SCK  
 R16 20K PS\_MIO7  
 R17 20K

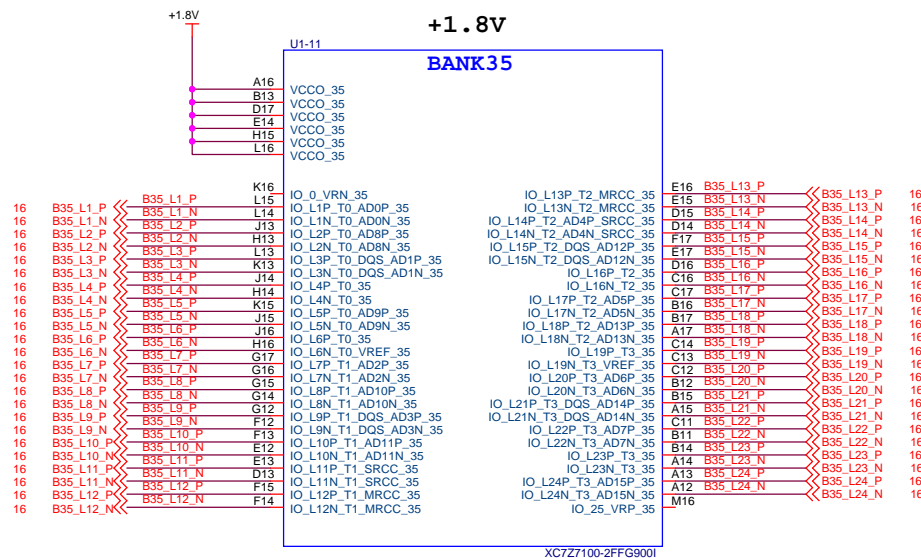
MIO[8]=1 ----MIO bank1 voltage=1.8V  
 MIO[2]=0 ----cascaded JTAG  
 MIO[3]=0 ----JTAG/NAND/Quad-SPI/SD  
 MIO[6]=0 ----PLL used  
 MIO[7]=0 ----MIO bank0 voltage=3.3V

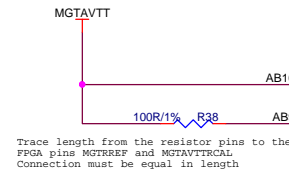
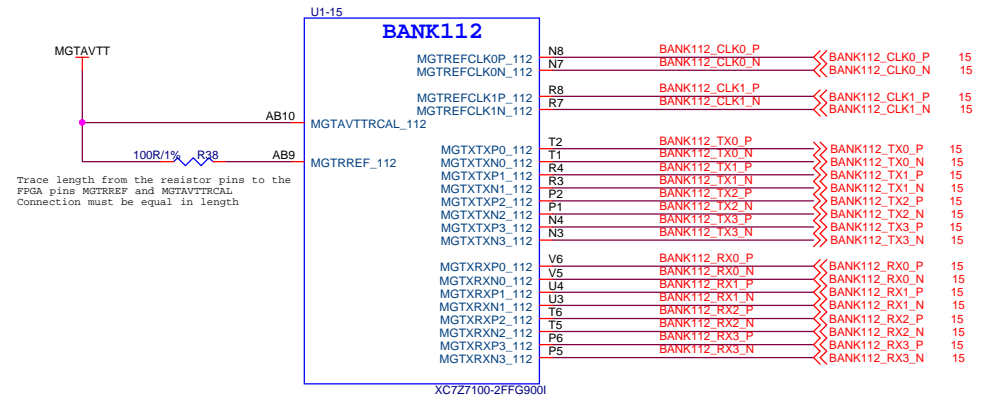
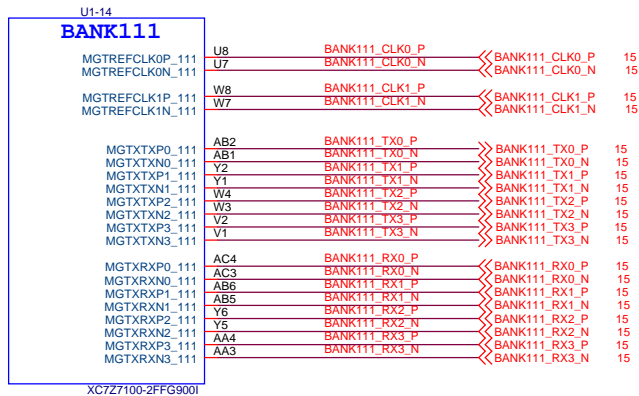
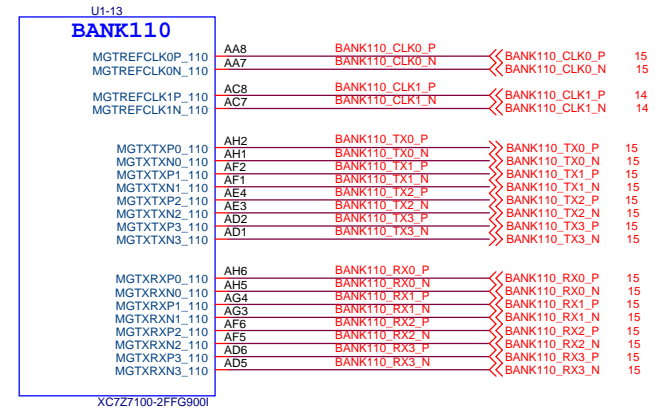
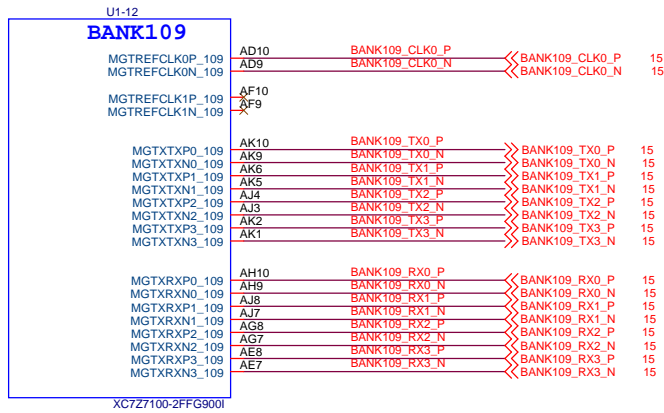




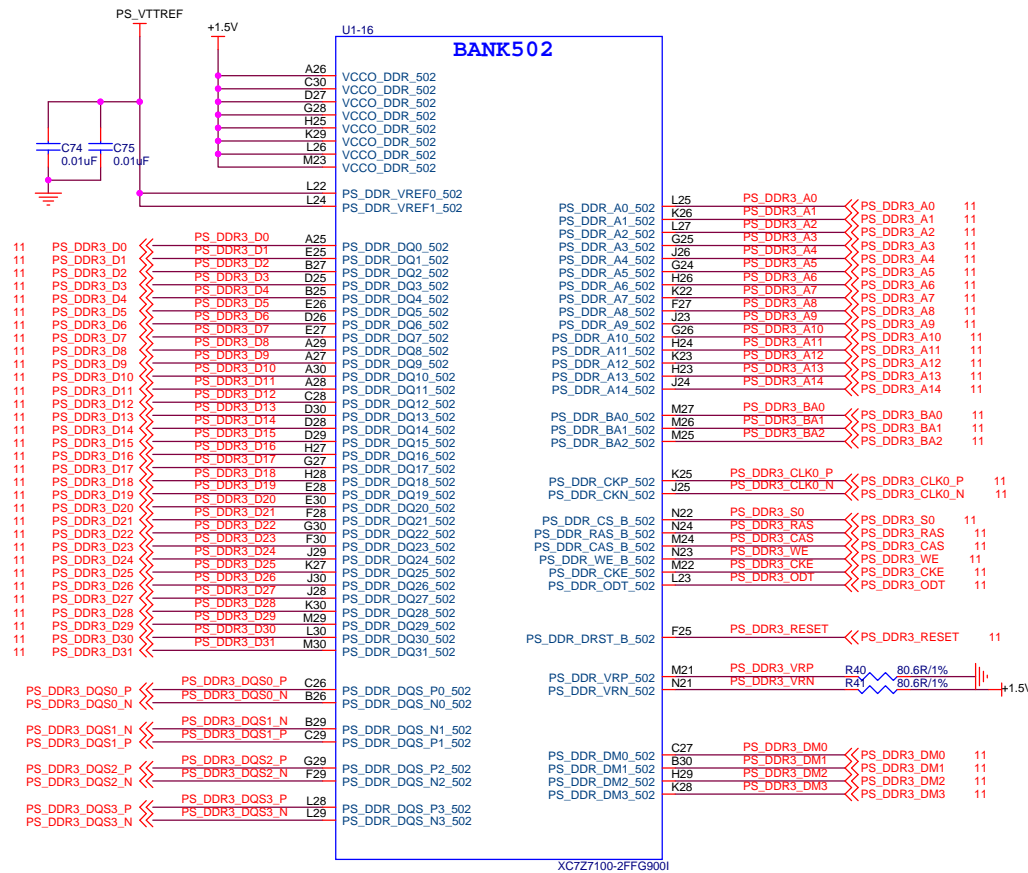





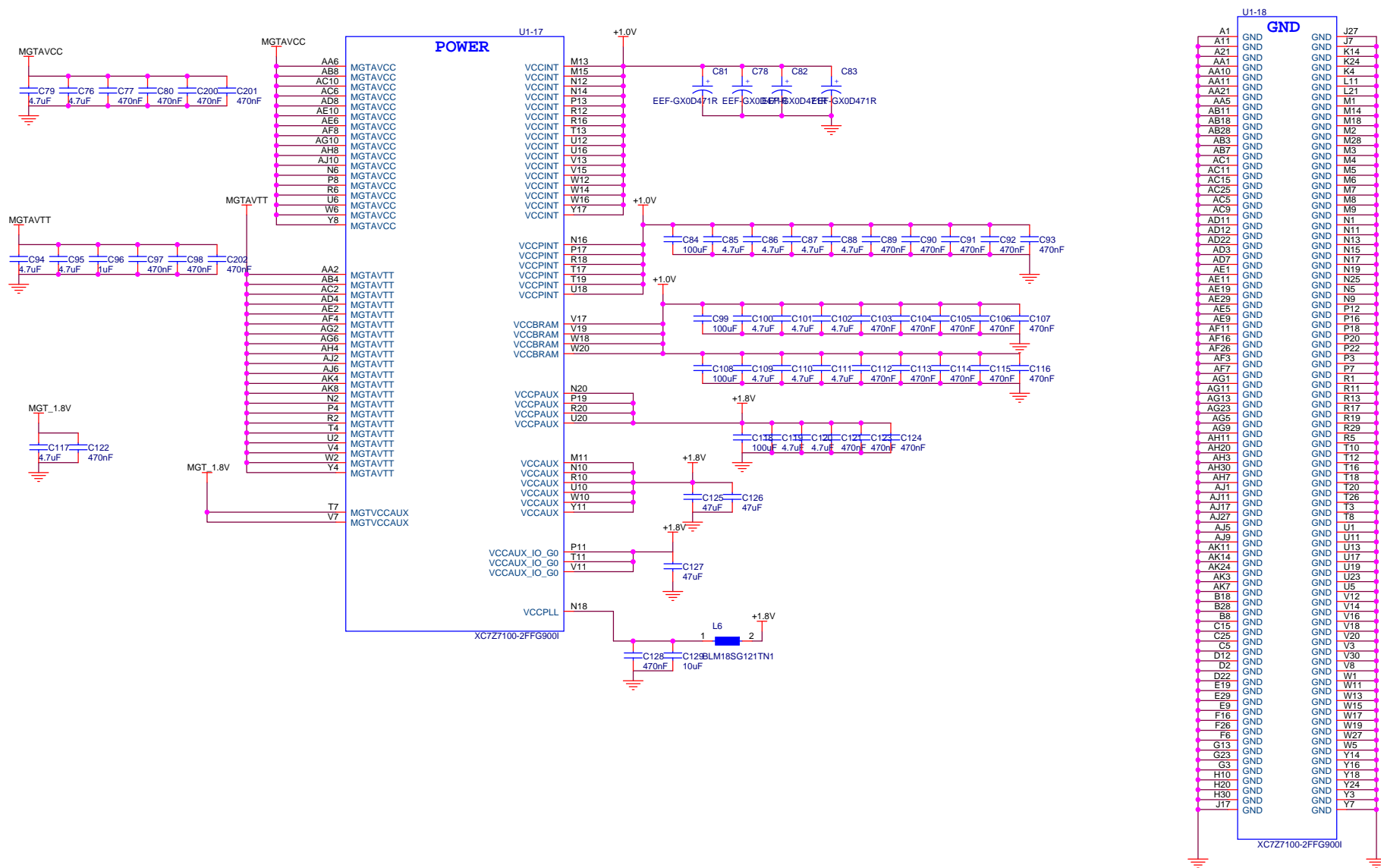


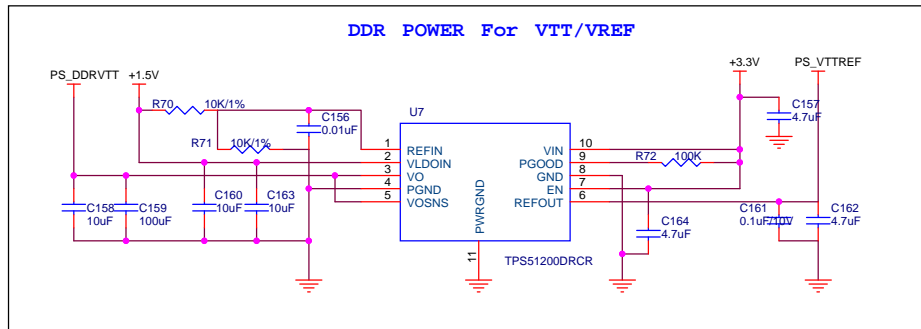
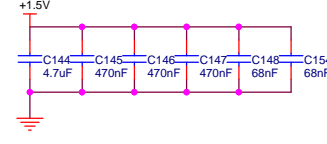
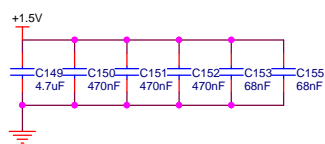
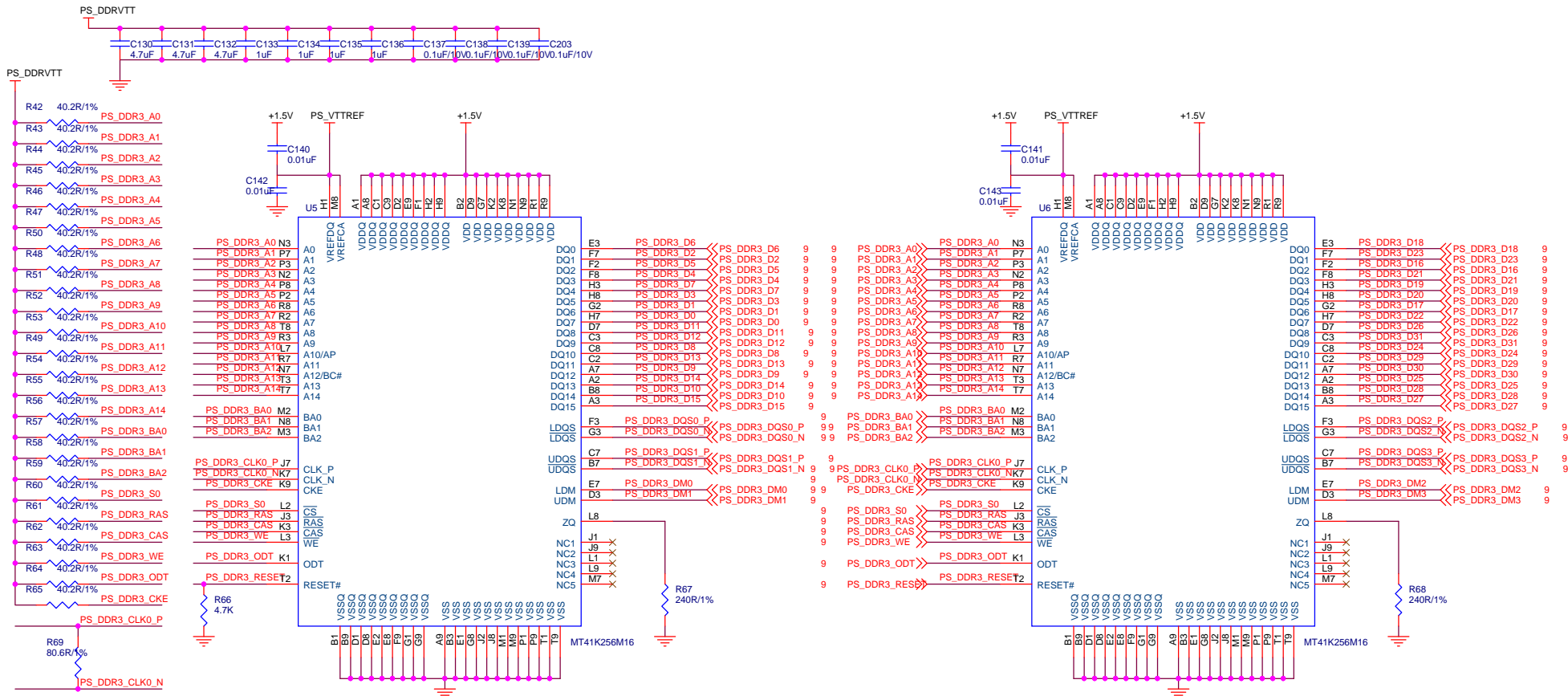


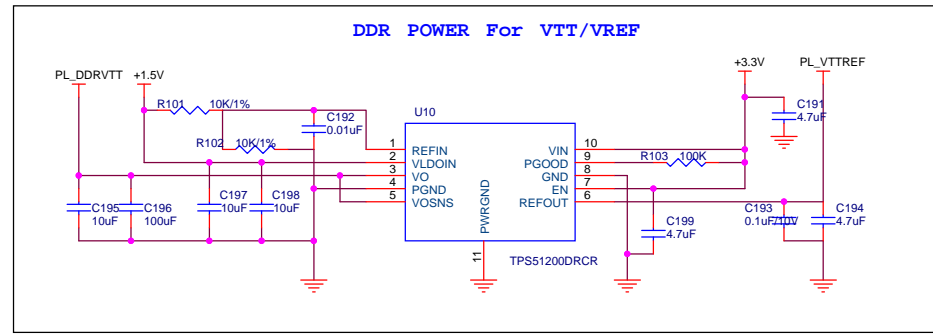
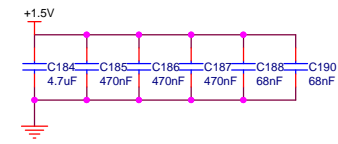
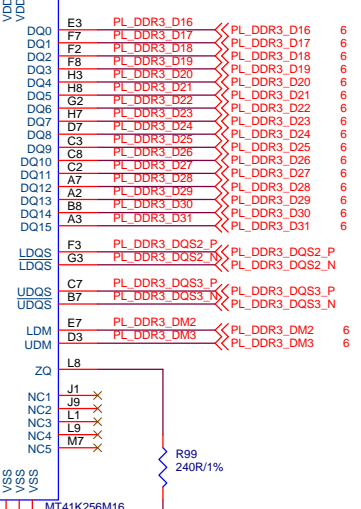
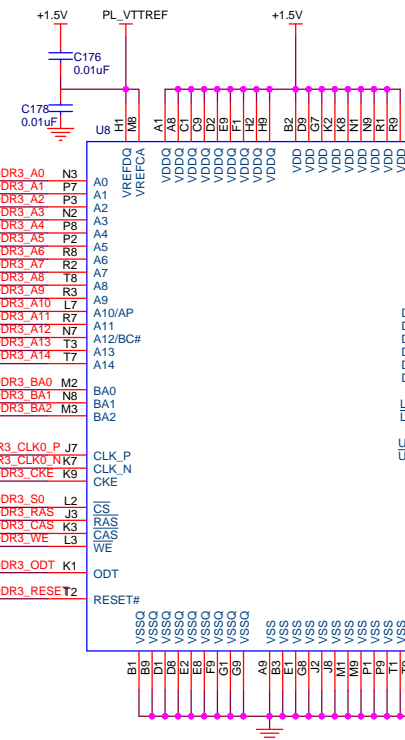
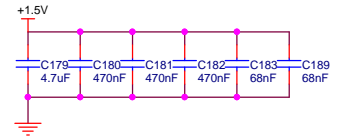
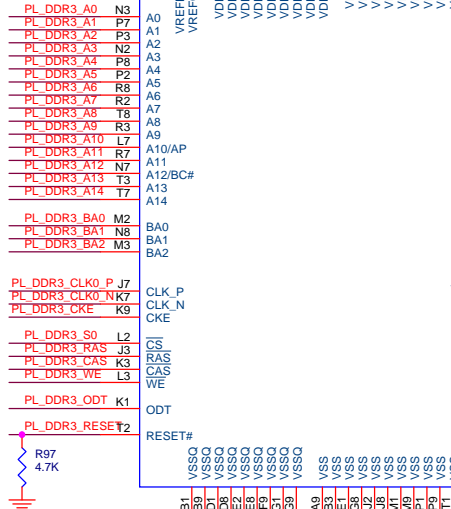
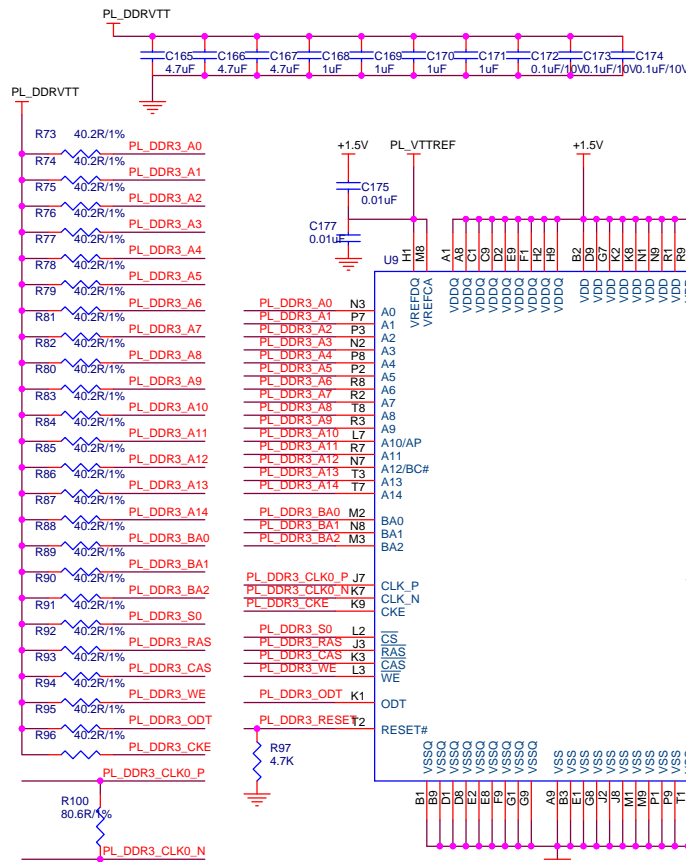


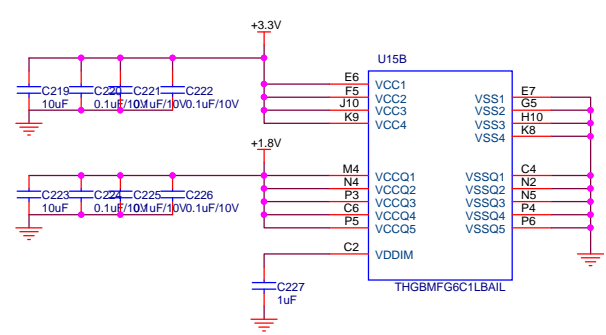
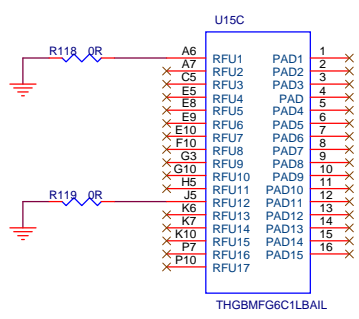
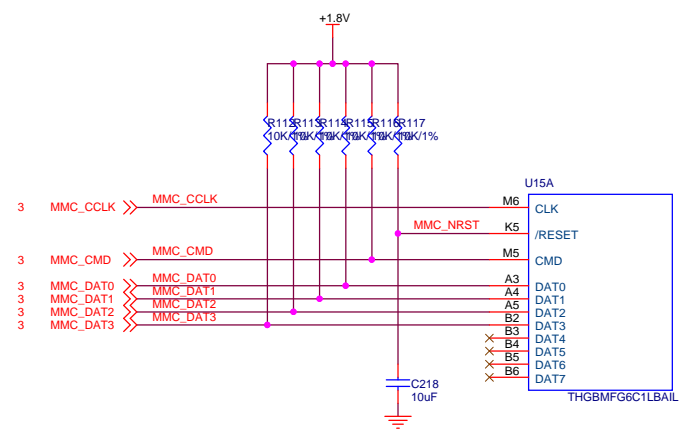
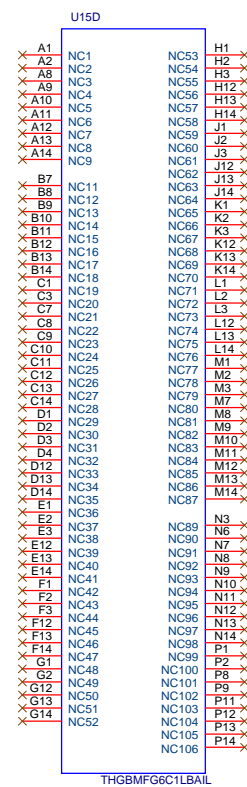
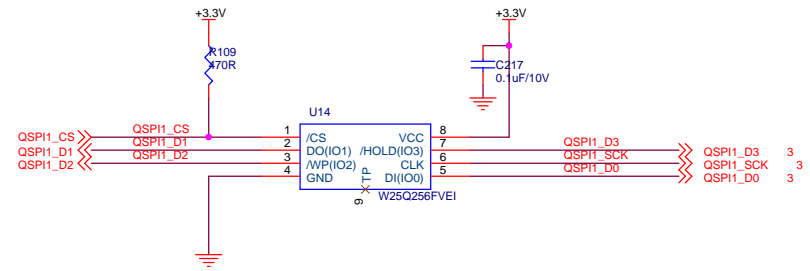
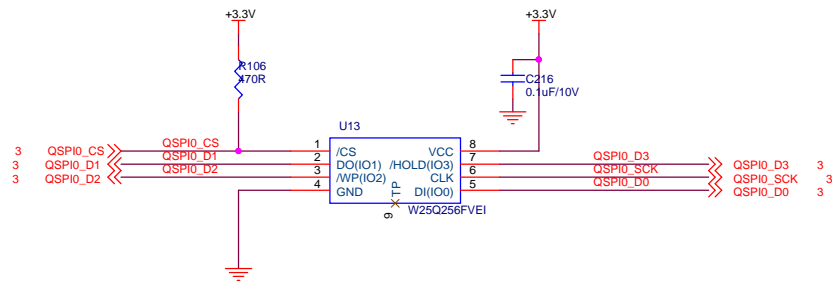


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<b>PAGE09 Z7 Bank502</b>			
Size	Document Number <b>AC7Z100C核心板 Schematics</b>		Rev 1.0
Date:	Wednesday, November 02, 2022	Sheet	9 of 19



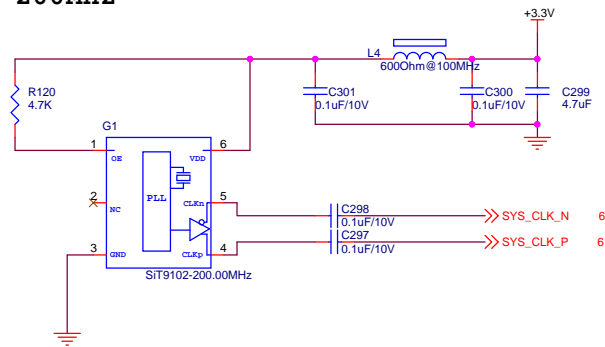






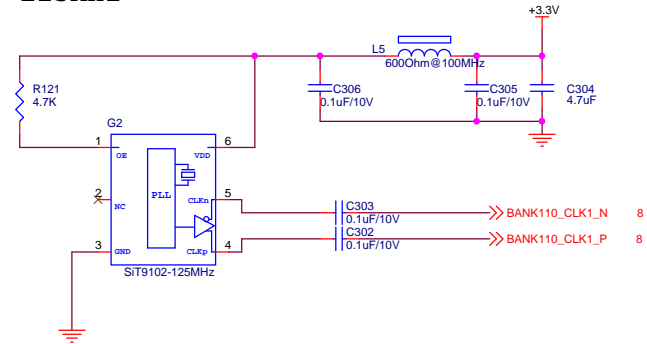
## SYSTEM CLOCK

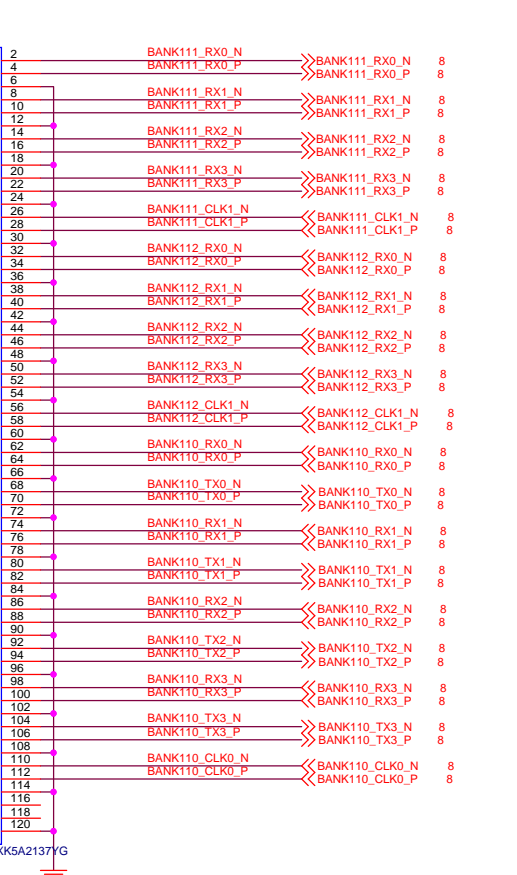
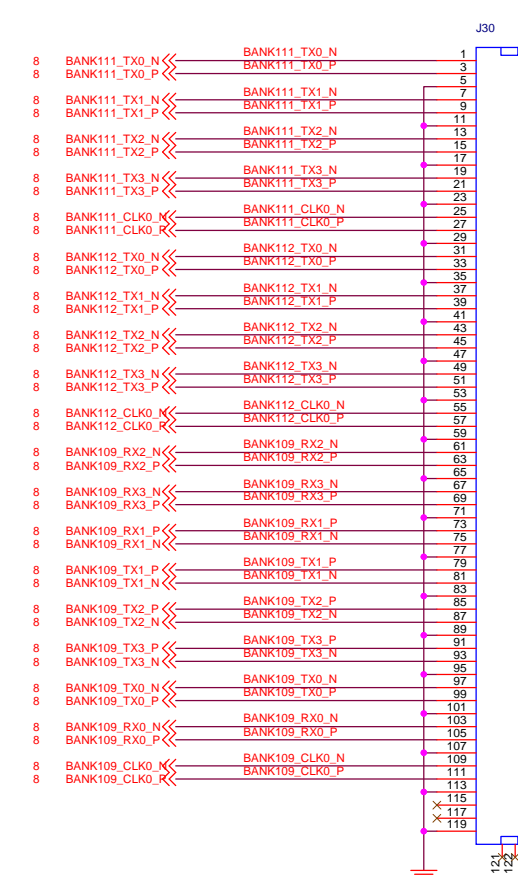
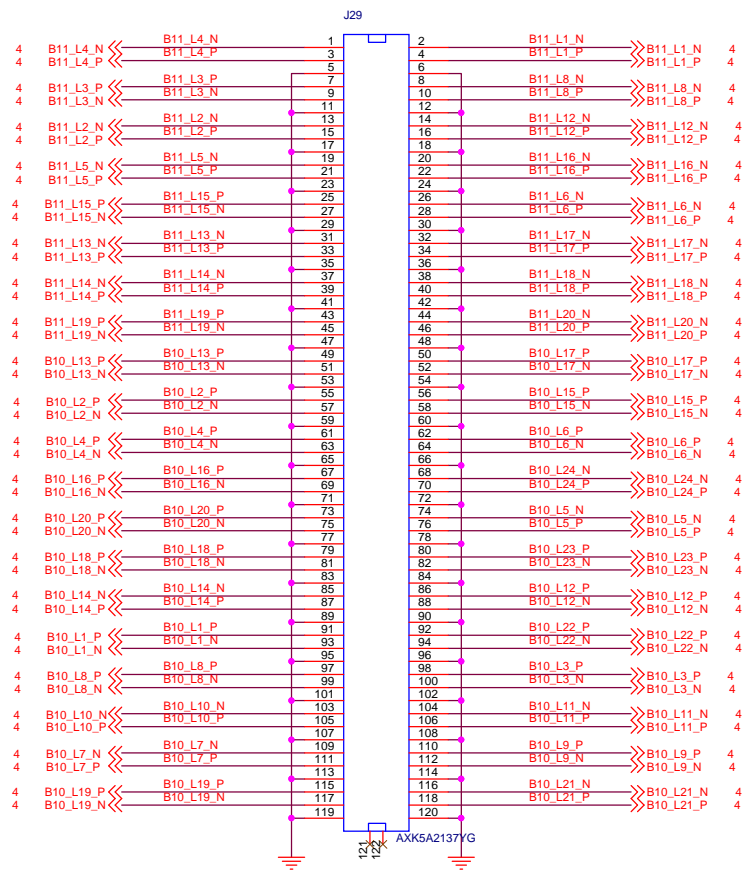
200MHz



## GTX CLOCK

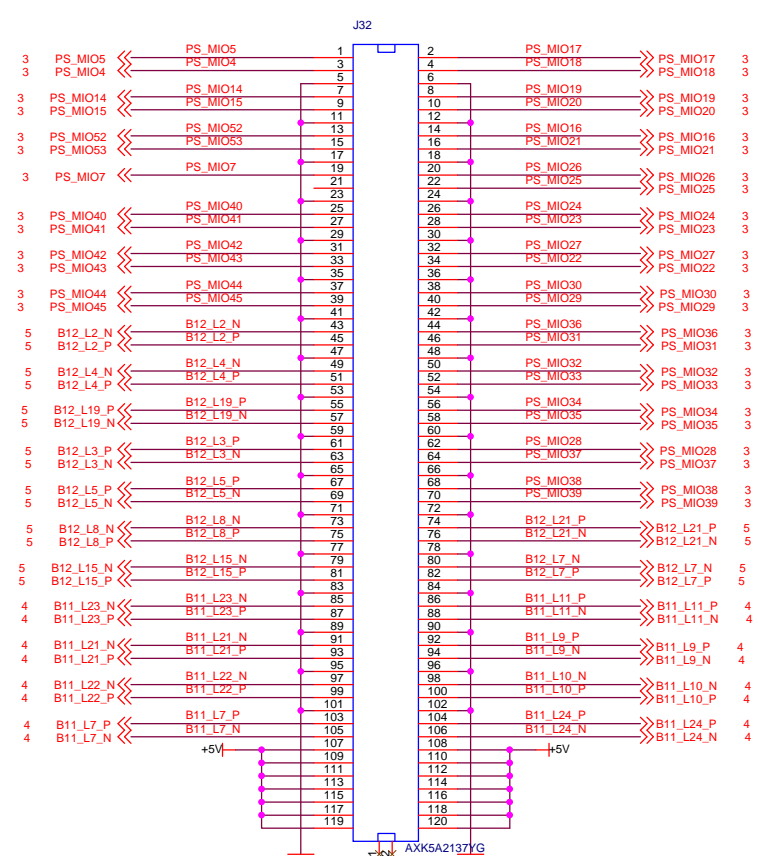
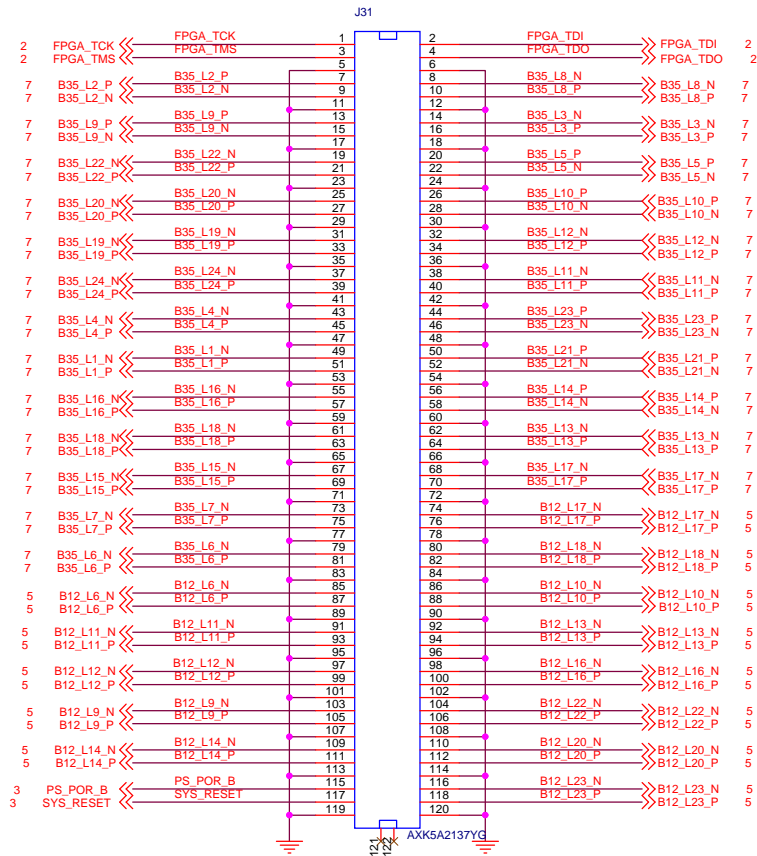
125MHz





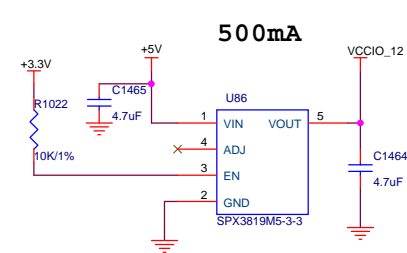
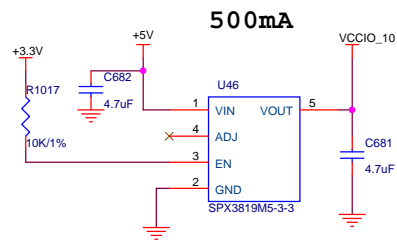
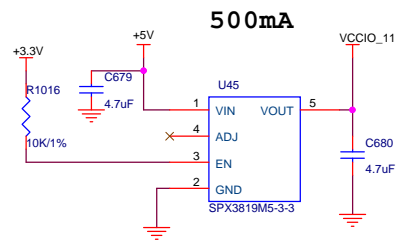
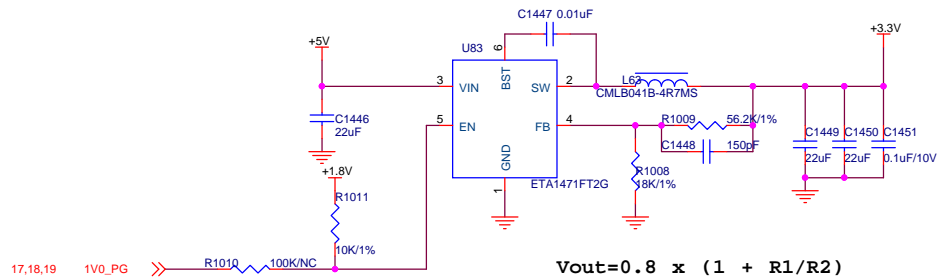
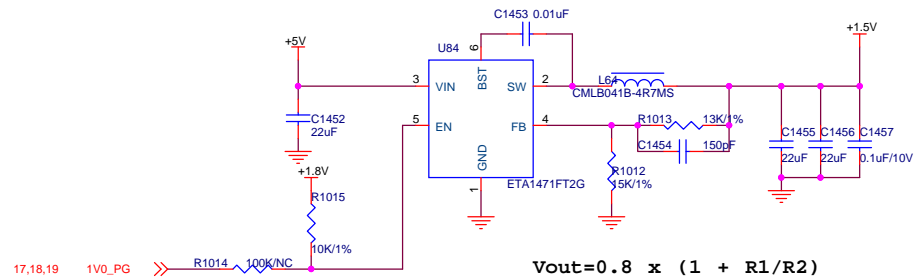
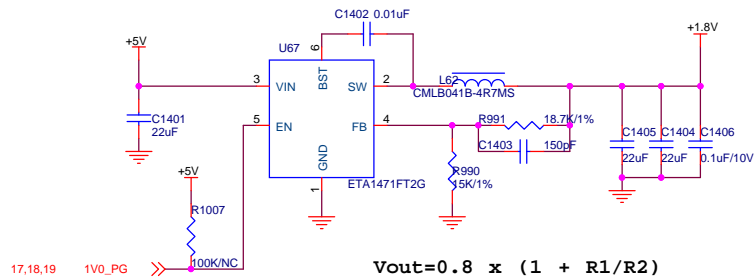
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BANK35 IO is 1.8V





The schematic diagram illustrates the power supply section for the MYMGK1R820FRSR module. It features a +5V input connected to the U31 regulator. The input is filtered by capacitors C683 (22uF) and C348 (22uF) to pin 2 (Vin), and by C349 (22uF) to pin 3 (Vin). Pin 4 (Vin) is connected to GND. Pin 5 (Vin) is connected to GND. Pin 6 (Vin) is connected to GND. Pin 7 (POW\_GOOD) is connected to the 1V0\_PG signal. Pin 8 (ON/OFF) is connected to the ON/OFF\_1 signal. Pin 22 (Trim) is connected to a 16K/1% resistor (R254) to GND. Pin 21 (Sense) is connected to the Sense signal. The output of the regulator is connected to pin 15 (Vout), pin 16 (Vout), pin 17 (Vout), pin 18 (Vout), pin 19 (Vout), and pin 20 (Vout). The output is filtered by capacitors C432 (EEF-GX0D471R), C429 (100uF), C430 (100uF), and C684 (100uF) to GND. The output is also connected to the +5V output of the module, which is filtered by capacitor R256 (100K/NC) and the ON/OFF\_1 signal.



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# 1.0V POWER 6A

