# KINTEX-7 FPGA Development Board AX7325B

# User Manual

**ALINX**

# Version Record

| Version | Date | Release By | Description |
|---------|------|------------|-------------|
| Rev 1.1 | 2022-08-30 | Rachel Zhou | First Release |

# Table of Contents

The AX7325B FPGA development board, it is the XILINX KINTEX-7 FPGA development platform.

The AX7325B FPGA development platform uses XILINX's KINTEX-7 chip XC7K325 solution. The FPGA development board mounts four pieces of 512MB high-speed DDR3 SDRAM chips, and a SODIMM interface on the board is used to expand the memory strip of DDR3. FPGA chip configuration uses a 128Mb QSPI FLASH chip

In the design of expansion board, we have extended a wealth of interfaces for users, such as 1 PCIex8 interface, 4 10G SFP interface, 1 40G QSFP+ optical interface, 1 UART serial port, 1 SD card slot, 1 FMC extension port, 1 40-pin expansion ports. It meets users' requirements for high-speed data exchange, data storage, video transmission processing and industrial control. It is a "professional" FPGA development platform, for high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in KINTEX-7FPGA development.
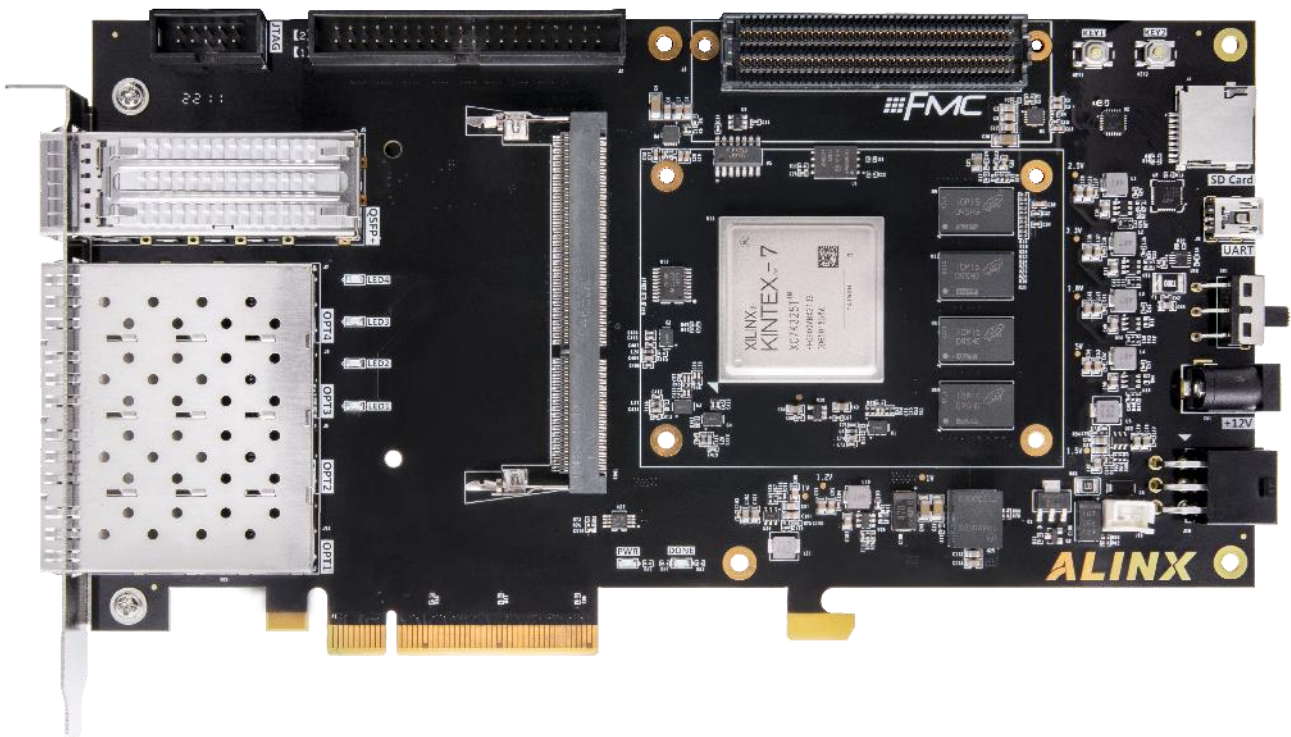
# Part 1: FPGA Development Board Introduction

The AX7325B FPGA development board is mainly composed of KINTEX-7 main chip, 4 DDR3, 1 memory stick SODIMM interface, 1 QSPI FLASH and some peripheral interfaces. The FPGA development board uses Xilinx's KINTEX-7 series of chips, model number XC7K325TFFG900. Four DDR3 memory chips are connected to the HP port of the FPGA chip, each with a DDR3 capacity of up to 512M bytes, which makes up 64-bit data bandwidth. A SODIMM interface is connected to the HR port of the FPGA to fit a 64-bit DDR3 memory module. A 128Mb QSPI FLASH is used to statically store configuration files or other user data of the FPGA chip.

The AX7325B development board expands the rich peripheral interface, including one PCIex8 interface, four 10G optical SFP interfaces, one 40G optical fiber + QSFP interface, one UART serial interface, one SD card interface, and one FMC expansion interface. 1 40-pin expansion port and some button LEDs.
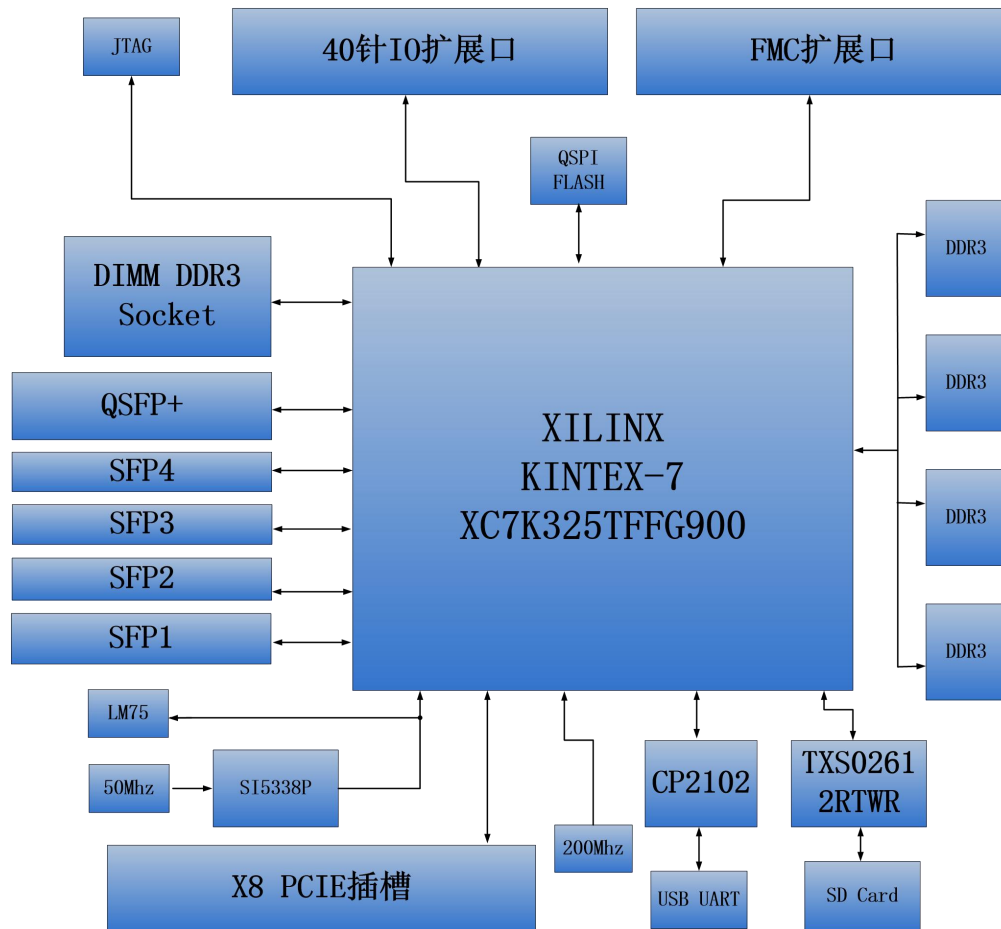
Figure 1-1: The Schematic Diagram of the AX7325B

Through this diagram, you can see the interfaces and functions that the AX7325B FPGA Development Board contains:

➢ Xilinx KINTEX-7 FPGA chip XC7K325TFFG900

➢ DDR3

With four large-capacity 512 Mbytes (2 GB total) high-speed DDR3 SDRAM, used as FPGA data storage, image analysis cache, data processing.

➢ QSPI FLASH

A 128Mbit QSPI FLASH memory chip can be used as a storage for FPGA chip configuration files and user data;

➢ PCIe x8 interface

A standard PCIEx8 interface for PCIE communication with computer motherboards, supports the PCI Express 2.0 standard, and

single-channel communication rates up to 5Gbps.

➢ 4 SFP interfaces

The four high-speed transceivers of the GTX transceiver of the FPGA are connected to the transmission and reception of four optical modules to realize four high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds of up to 10 Gb/s.

➢ 1 QSFP + optical interface

The four high-speed transceivers of the GTX transceiver of the FPGA are connected to the optical module interface of a QSPF+, to implement the optical communication interface of the QSFP+. Fiber optic data communications receive and transmit at speeds of up to 40 Gb/s.

➢ DDR3 memory module interface

One SODIMM memory module interface is used to assemble a DDR3 memory module, and the DDR3 data width of the interface is 64 bits. The memory stick SODIMM interface expands the storage space and data bandwidth for the FPGA development board.

➢ USB Uart interface

1-channel Uart to USB interface for communication with the computer for user debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

➢ Micro SD slot

1 Micro SD card slot

➢ Temperature and humidity sensor

Onboard a temperature and humidity sensor chip LM75 for detecting the temperature and humidity of the environment around the board

➢ FMC expansion ports

A standard FMC LPC expansion port can be connected to various FMC

modules of XILINX or ALINX (HDMI input/output module, binocular camera module, high-speed AD module etc.)

➢ JTAG Interface

A 10-pin0.1 spacing standard JTAG ports for FPGA program download and debugging. Users can debug and download FPGAs through XILINX downloader.

➢ Clock

2 * 200Mhz differential crysta, A 156.25Mhz and A 125Mhz on the board .

➢ LED Light

6LEDs, 1 power indicator, 1 DONE configuration indicator, 4 FPGA control indicators

➢ Button

2 user buttons, connect to the normal IO of the FPGA.

# Part 2: FPGA Chip

The FPGA development board uses Xilinx's KINTEX-7 FPGA chip, model number XC7K325T-2FFG900I. The speed class is 2 and the temperature class is industrial. This model is a FGG900 package with 900 pins and a 1.0mm pitch. The chip naming rules for Xilinx KINTEX-7 FPGA are shown in Figure 2-1 below:
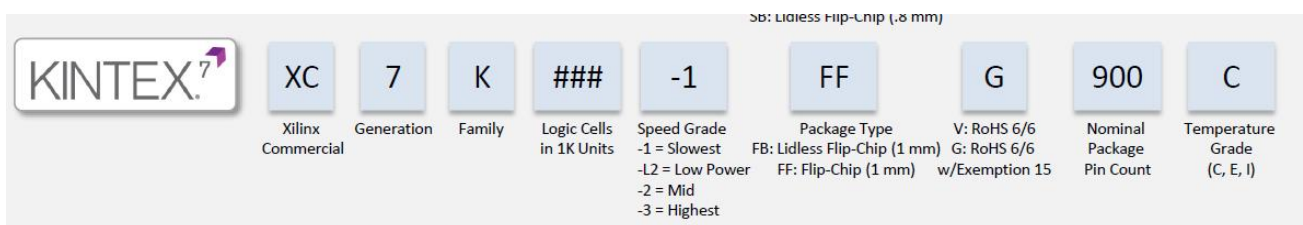


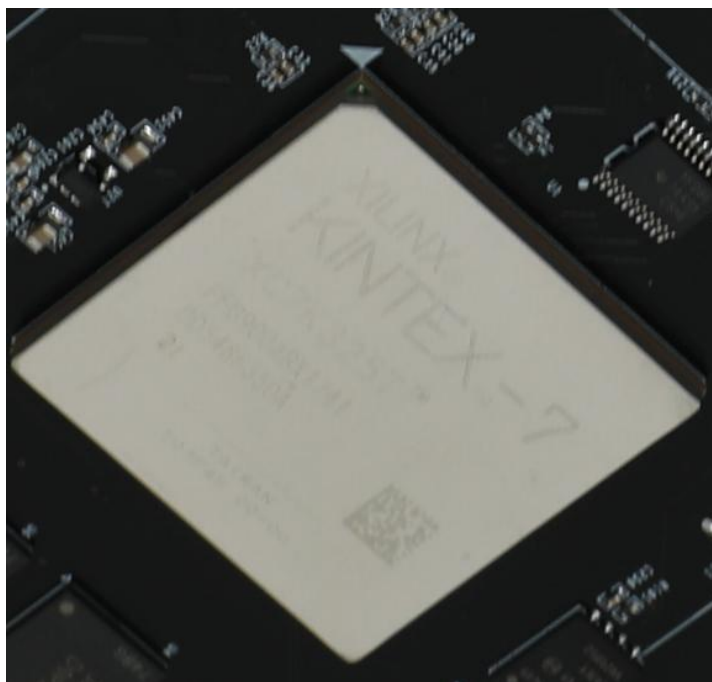Figure 2-1: The Specific Chip Model Definition of KINTEX-7 Series

Figure 2-2: FPGA chip XC7K325T on board

## The main parameters of the FPGA chip XC7K325T are as follows

| Name | Specific parameters |
|---|---|
| Logic Cells | 33,280 |
| Slices | 5,200 |
| CLB flip-flops | 41,600 |
| Block RAM（kb） | 1,800 |
| DSP48 Slices | 90 |
| PCIe Gen2 | 1 |
| XADC | 12bit, 1Mbps AD |
| GTP Transceiver | 16，12.5Gb/s max |
| Speed Grade | -2 |
| Temperature Grade | Industrial |

### FPGA power supply system

KINTEX-7 FPGA power supplies are $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, $V_{CCAUX\_IO}$ $V_{CCO}$, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. $V_{CCINT}$ is the FPGA core power supply pin, which needs to be connected to 1.0V; $V_{CCBRAM}$ is the power supply pin of FPGA Block RAM, connect to 1.0V; $V_{CCAUX}$ is FPGA auxiliary power supply pin, connect 1.8V; $V_{CCO}$

is the voltage of each BANK of FPGA, including BANK0, BANK12~18, BANK32~34. On the AX7325B development board, BANK12~13 is connected to the FMC connector. The default voltage of $V_{CCO}$ is 2.5V, which enables IO to support LVDS interface. BANK16~18, BANK33~35 need to connect DDR3 memory and DDR3 chip, BANK voltage is 1.5V, other BANK voltage is 3.3V. $V_{MGTAVCC}$ is the supply voltage of the internal GTP transceiver of the FPGA, connected to 1.0V, $V_{MGTAVTT}$ is the termination voltage of the GTP transceiver, connected to 1.2V.

The KINTEX-7 FPGA system requires that the power-up sequence be powered by $V_{CCINT}$, then $V_{CCBRAM}$, then $V_{CCAUX}$ and finally $V_{CCO}$. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same voltage, they can be powered up at the same time. The order of power outages is reversed. The power-up sequence of the GTP transceiver is $V_{CCINT}$, then $V_{MGTAVCC}$, then $V_{MGTAVTT}$. If $V_{CCINT}$ and $V_{MGTAVCC}$ have the same voltage, they can be powered up at the same time. The power-off sequence is just the opposite of the power-on sequence.

# Part 3:DDR3 DRAM

TheAX7325B FPGA development board is equipped with four 512MB DDR3 chips, model MT41K256M16HA-125 (Compatible with MT41J256M16HA-125). Four DDR3 SDRAMs form a 64-bit bus width. Because four DDR3 chips are connected to the HP port of the FPGA, the DDR3 SDRAM can run at speeds up to 800MHz (data rate 1600Mbps), and four DDR3 memory systems are directly connected to the BANK32, BANK33, and BANK34 interfaces of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 3-1.

| Bit Number | Chip Model | Capacity | Factory |
|---|---|---|---|
| U3,U4,U6,U7 | MT41K256M16HA-125 Or MT41J256M16HA-125 | 256M x 16bit | Micron |

Table 3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.
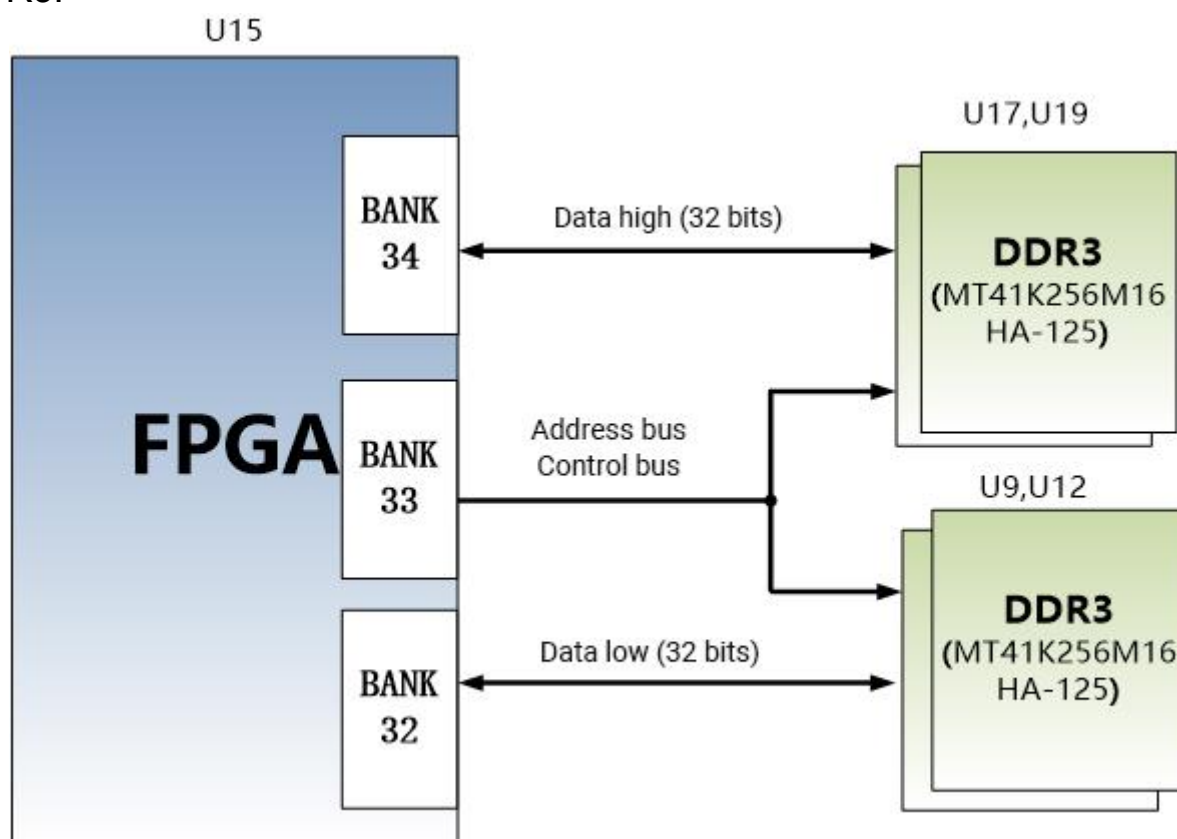


Figure 3-1: The DDR3 DRAM Schematic
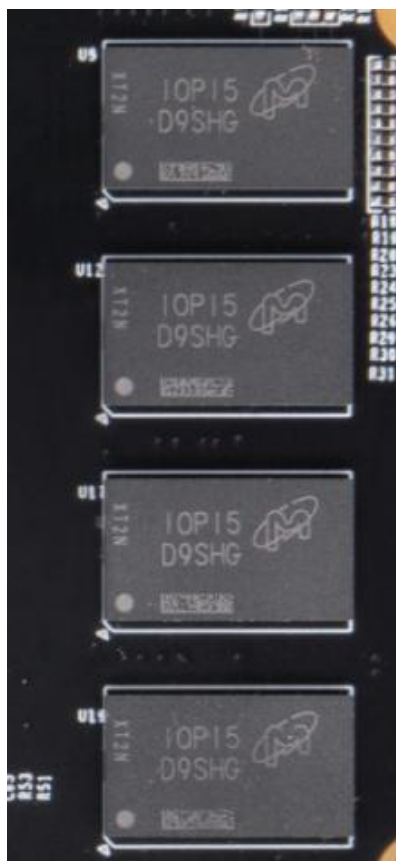
Figure 3-2: The DDR3 on the FPGA Board

## 4 DDR3 DRAM pin assignments:

| Signal Name | FPGA Pin Name | FPGA Pin |
|---|---|---|
| DDR3_D0 | IO_L13P_T2_MRCC_32 | AD18 |
| DDR3_D1 | IO_L16N_T2_32 | AB18 |
| DDR3_D2 | IO_L14P_T2_SRCC_32 | AD17 |
| DDR3_D3 | IO_L17P_T2_32 | AB19 |
| DDR3_D4 | IO_L14N_T2_SRCC_32 | AD16 |
| DDR3_D5 | IO_L17N_T2_32 | AC19 |
| DDR3_D6 | IO_L13N_T2_MRCC_32 | AE18 |
| DDR3_D7 | IO_L18P_T2_32 | AB17 |
| DDR3_D8 | IO_L8P_T1_32 | AG19 |
| DDR3_D9 | IO_L7N_T1_32 | AK19 |
| DDR3_D10 | IO_L10P_T1_32 | AD19 |
| DDR3_D11 | IO_L7P_T1_32 | AJ19 |
| DDR3_D12 | IO_L11P_T1_SRCC_32 | AF18 |
| DDR3_D13 | IO_L8N_T1_32 | AH19 |

| DDR3_D14 | IO_L10N_T1_32 | AE19 |
|---|---|---|
| DDR3_D15 | IO_L11N_T1_SRCC_32 | AG18 |
| DDR3_D16 | IO_L1N_T0_32 | AK15 |
| DDR3_D17 | IO_L5N_T0_32 | AJ17 |
| DDR3_D18 | IO_L2N_T0_32 | AH15 |
| DDR3_D19 | IO_L4P_T0_32 | AF15 |
| DDR3_D20 | IO_L4N_T0_32 | AG14 |
| DDR3_D21 | IO_L5P_T0_32 | AH17 |
| DDR3_D22 | IO_L2P_T0_32 | AG15 |
| DDR3_D23 | IO_L1P_T0_32 | AK16 |
| DDR3_D24 | IO_L19P_T3_32 | AE15 |
| DDR3_D25 | IO_L24P_T3_32 | Y16 |
| DDR3_D26 | IO_L22P_T3_32 | AC14 |
| DDR3_D27 | IO_L20P_T3_32 | AA15 |
| DDR3_D28 | IO_L23P_T3_32 | AA17 |
| DDR3_D29 | IO_L22N_T3_32 | AD14 |
| DDR3_D30 | IO_L23N_T3_32 | AA16 |
| DDR3_D31 | IO_L20N_T3_32 | AB15 |
| DDR3_D32 | IO_L22N_T3_34 | AK6 |
| DDR3_D33 | IO_L23P_T3_34 | AJ8 |
| DDR3_D34 | IO_L22P_T3_34 | AJ6 |
| DDR3_D35 | IO_L19P_T3_34 | AF8 |
| DDR3_D36 | IO_L24N_T3_34 | AK4 |
| DDR3_D37 | IO_L23N_T3_34 | AK8 |
| DDR3_D38 | IO_L24P_T3_34 | AK5 |
| DDR3_D39 | IO_L20N_T3_34 | AG7 |
| DDR3_D40 | IO_L10P_T1_34 | AE4 |
| DDR3_D41 | IO_L8N_T1_34 | AF1 |
| DDR3_D42 | IO_L11P_T1_SRCC_34 | AE5 |
| DDR3_D43 | IO_L8P_T1_34 | AE1 |
| DDR3_D44 | IO_L12P_T1_MRCC_34 | AF6 |
| DDR3_D45 | IO_L10N_T1_34 | AE3 |
| DDR3_D46 | IO_L11N_T1_SRCC_34 | AF5 |
| DDR3_D47 | IO_L7N_T1_34 | AF2 |

| | | |
|---|---|---|
| DDR3_D48 | IO_L13P_T2_MRCC_34 | AH4 |
| DDR3_D49 | IO_L16N_T2_34 | AJ2 |
| DDR3_D50 | IO_L14N_T2_SRCC_34 | AH5 |
| DDR3_D51 | IO_L13N_T2_MRCC_34 | AJ4 |
| DDR3_D52 | IO_L16P_T2_34 | AH2 |
| DDR3_D53 | IO_L17N_T2_34 | AK1 |
| DDR3_D54 | IO_L14P_T2_SRCC_34 | AH6 |
| DDR3_D55 | IO_L17P_T2_34 | AJ1 |
| DDR3_D56 | IO_L2P_T0_34 | AC2 |
| DDR3_D57 | IO_L4P_T0_34 | AC5 |
| DDR3_D58 | IO_L1N_T0_34 | AD3 |
| DDR3_D59 | IO_L6P_T0_34 | AC7 |
| DDR3_D60 | IO_L5N_T0_34 | AE6 |
| DDR3_D61 | IO_L5P_T0_34 | AD6 |
| DDR3_D62 | IO_L2N_T0_34 | AC1 |
| DDR3_D63 | IO_L4N_T0_34 | AC4 |
| DDR3_DM0 | IO_L16P_T2_32 | AA18 |
| DDR3_DM1 | IO_L12P_T1_MRCC_32 | AF17 |
| DDR3_DM2 | IO_L6P_T0_32 | AE16 |
| DDR3_DM3 | IO_L24N_T3_32 | Y15 |
| DDR3_DM4 | IO_L20P_T3_34 | AF7 |
| DDR3_DM5 | IO_L7P_T1_34 | AF3 |
| DDR3_DM6 | IO_L18P_T2_34 | AJ3 |
| DDR3_DM7 | IO_L1P_T0_34 | AD4 |
| DDR3_DQS0_P | IO_L15P_T2_DQS_32 | Y19 |
| DDR3_DQS0_N | IO_L15N_T2_DQS_32 | Y18 |
| DDR3_DQS1_P | IO_L9P_T1_DQS_32 | AJ18 |
| DDR3_DQS1_N | IO_L9N_T1_DQS_32 | AK18 |
| DDR3_DQS2_P | IO_L3P_T0_DQS_32 | AH16 |
| DDR3_DQS2_N | IO_L3N_T0_DQS_32 | AJ16 |
| DDR3_DQS3_P | IO_L21P_T3_DQS_32 | AC16 |
| DDR3_DQS3_N | IO_L21N_T3_DQS_32 | AC15 |
| DDR3_DQS4_P | IO_L21P_T3_DQS_34 | AH7 |
| DDR3_DQS4_N | IO_L21N_T3_DQS_34 | AJ7 |

| DDR3_DQS5_P | IO_L9P_T1_DQS_34 | AG4 |
|---|---|---|
| DDR3_DQS5_N | IO_L9N_T1_DQS_34 | AG3 |
| DDR3_DQS6_P | IO_L15P_T2_DQS_34 | AG2 |
| DDR3_DQS6_N | IO_L15N_T2_DQS_34 | AH1 |
| DDR3_DQS7_P | IO_L3P_T0_DQS_34 | AD2 |
| DDR3_DQS7_N | IO_L3N_T0_DQS_34 | AD1 |
| DDR3_A0 | IO_L1P_T0_33 | AA12 |
| DDR3_A1 | IO_L1N_T0_33 | AB12 |
| DDR3_A2 | IO_L2P_T0_33 | AA8 |
| DDR3_A3 | IO_L2N_T0_33 | AB8 |
| DDR3_A4 | IO_L3P_T0_DQS_33 | AB9 |
| DDR3_A5 | IO_L3N_T0_DQS_33 | AC9 |
| DDR3_A6 | IO_L6N_T0_VREF_33 | AB13 |
| DDR3_A7 | IO_L4N_T0_33 | Y10 |
| DDR3_A8 | IO_L5P_T0_33 | AA11 |
| DDR3_A9 | IO_L5N_T0_33 | AA10 |
| DDR3_A10 | IO_L6P_T0_33 | AA13 |
| DDR3_A11 | IO_L8P_T1_33 | AD8 |
| DDR3_A12 | IO_L7P_T1_33 | AB10 |
| DDR3_A13 | IO_L7N_T1_33 | AC10 |
| DDR3_A14 | IO_L15P_T2_DQS_33 | AJ9 |
| DDR3_BA0 | IO_L8N_T1_33 | AE8 |
| DDR3_BA1 | IO_L9P_T1_DQS_33 | AC12 |
| DDR3_BA2 | IO_L9N_T1_DQS_33 | AC11 |
| DDR3_WE | IO_L10P_T1_33 | AD9 |
| DDR3_RAS | IO_L10N_T1_33 | AE9 |
| DDR3_CAS | IO_L11P_T1_SRCC_33 | AE11 |
| DDR3_S0 | IO_L11N_T1_SRCC_33 | AF11 |
| DDR3_CKE0 | IO_L12P_T1_MRCC_33 | AD12 |
| DDR3_ODT | IO_L12N_T1_MRCC_33 | AD11 |
| DDR3_CLK0_P | IO_L13P_T2_MRCC_33 | AG10 |
| DDR3_CLK0_N | IO_L13N_T2_MRCC_33 | AH10 |
| DDR3_RESET | IO_L4P_T0_33 | Y11 |

# Part 4:SODIMM memory module interface

The AX7325B development board has a 204PIN SODIMM memory socket that expands the board's storage and data bandwidth and supports up to 8GB of Micron SODIMM DDR3 memory. The FPGA and SODIMM DDR3 memory banks have a data width of 64 bits and a maximum operating speed of 400 MHz (data rate 800 Mbps). By default, the SODIMM memory module is not included. If you need to test it, you need to prepare it yourself. The following Figure 4-1 detailed the 2GB Micron SODIMM memory strip we tested.



Figure 4-1: SODIMM memory test sample

The SODIMM memory module interface is directly connected to the interface of BANK16, BANK17 and BANK18 of FPGA. The hardware connection mode of FPGA and SODIMM DDR3 is shown in Figure 4-2.
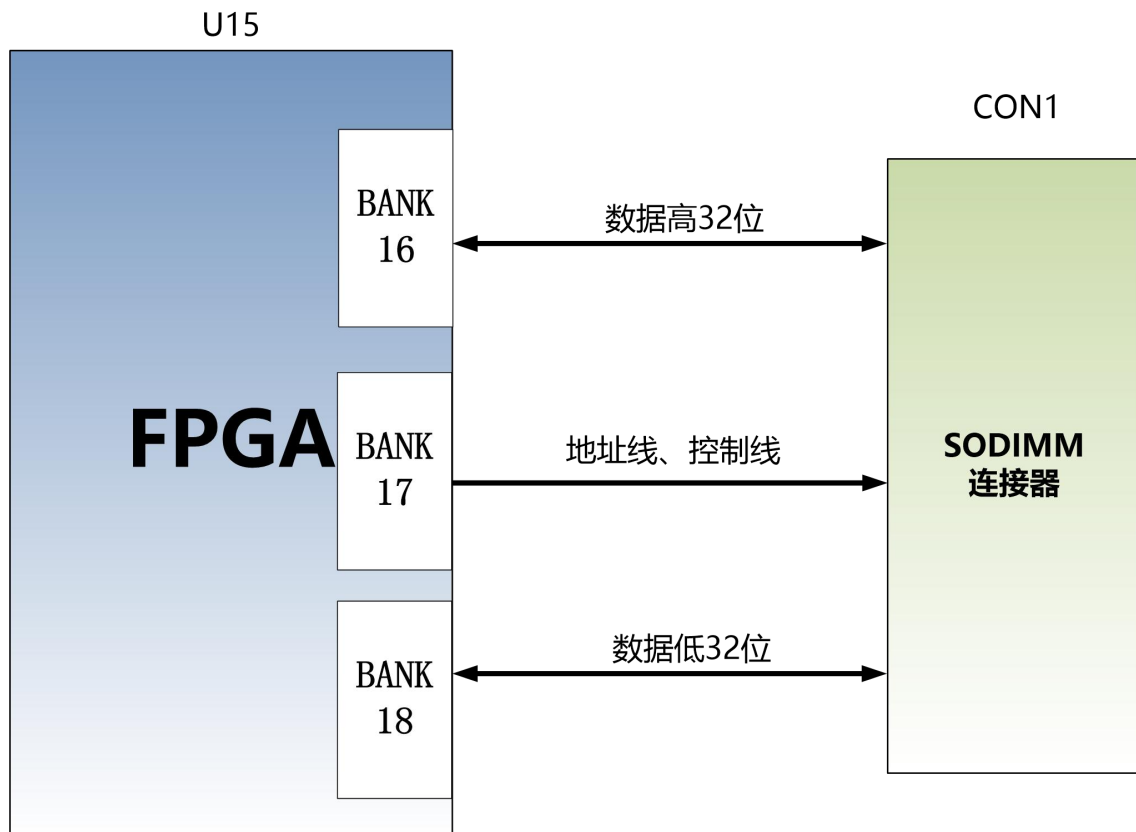
U15
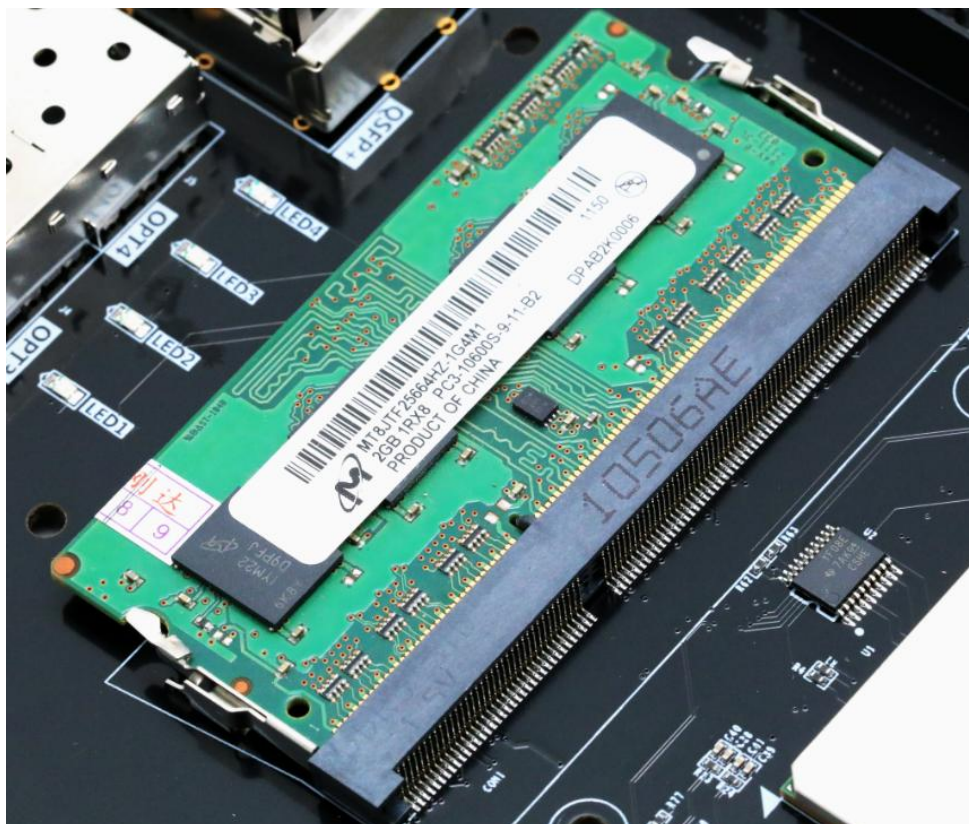


Figure 4-2: SODIMM interface Connection Diagram



Figure 4-3: SODIMM slot on the FPGA Board

## SODIMM slot pin assignments:

| Signal Name | FPGA Pin Name | FPGA Pin |
|---|---|---|
| DIMM_DDR3_D0 | IO_L2P_T0_18 | L15 |
| DIMM_DDR3_D1 | IO_L5P_T0_18 | K14 |
| DIMM_DDR3_D2 | IO_L5N_T0_18 | J14 |
| DIMM_DDR3_D3 | IO_L6P_T0_18 | L11 |
| DIMM_DDR3_D4 | IO_L2N_T0_18 | K15 |
| DIMM_DDR3_D5 | IO_L1P_T0_18 | L16 |
| DIMM_DDR3_D6 | IO_L4N_T0_18 | J13 |
| DIMM_DDR3_D7 | IO_L1N_T0_18 | K16 |
| DIMM_DDR3_D8 | IO_L8N_T1_18 | J12 |
| DIMM_DDR3_D9 | IO_L8P_T1_18 | J11 |
| DIMM_DDR3_D10 | IO_L7P_T1_18 | H15 |
| DIMM_DDR3_D11 | IO_L11N_T1_SRCC_18 | G14 |
| DIMM_DDR3_D12 | IO_L10P_T1_18 | H11 |
| DIMM_DDR3_D13 | IO_L10N_T1_18 | H12 |
| DIMM_DDR3_D14 | IO_L12P_T1_MRCC_18 | G13 |
| DIMM_DDR3_D15 | IO_L7N_T1_18 | G15 |
| DIMM_DDR3_D16 | IO_L13P_T2_MRCC_18 | D12 |
| DIMM_DDR3_D17 | IO_L17P_T2_18 | A11 |
| DIMM_DDR3_D18 | IO_L13N_T2_MRCC_18 | D13 |
| DIMM_DDR3_D19 | IO_L14N_T2_SRCC_18 | E13 |
| DIMM_DDR3_D20 | IO_L16P_T2_18 | F11 |
| DIMM_DDR3_D21 | IO_L16N_T2_18 | E11 |
| DIMM_DDR3_D22 | IO_L17N_T2_18 | A12 |
| DIMM_DDR3_D23 | IO_L14P_T2_SRCC_18 | F12 |
| DIMM_DDR3_D24 | IO_L22P_T3_18 | B13 |
| DIMM_DDR3_D25 | IO_L22N_T3_18 | A13 |
| DIMM_DDR3_D26 | IO_L23N_T3_18 | B15 |
| DIMM_DDR3_D27 | IO_L23P_T3_18 | C15 |
| DIMM_DDR3_D28 | IO_L24P_T3_18 | B14 |
| DIMM_DDR3_D29 | IO_L24N_T3_18 | A15 |
| DIMM_DDR3_D30 | IO_L20N_T3_18 | E15 |
| DIMM_DDR3_D31 | IO_L19P_T3_18 | F15 |

| | | |
|---|---|---|
| DIMM_DDR3_D32 | IO_L1N_T0_16 | A23 |
| DIMM_DDR3_D33 | IO_L4N_T0_16 | D24 |
| DIMM_DDR3_D34 | IO_L4P_T0_16 | E24 |
| DIMM_DDR3_D35 | IO_L5N_T0_16 | E26 |
| DIMM_DDR3_D36 | IO_L2P_T0_16 | E23 |
| DIMM_DDR3_D37 | IO_L1P_T0_16 | B23 |
| DIMM_DDR3_D38 | IO_L2N_T0_16 | D23 |
| DIMM_DDR3_D39 | IO_L6P_T0_16 | G23 |
| DIMM_DDR3_D40 | IO_L8N_T1_16 | B24 |
| DIMM_DDR3_D41 | IO_L8P_T1_16 | C24 |
| DIMM_DDR3_D42 | IO_L11N_T1_SRCC_16 | C26 |
| DIMM_DDR3_D43 | IO_L7N_T1_16 | A27 |
| DIMM_DDR3_D44 | IO_L10P_T1_16 | A25 |
| DIMM_DDR3_D45 | IO_L10N_T1_16 | A26 |
| DIMM_DDR3_D46 | IO_L7P_T1_16 | B27 |
| DIMM_DDR3_D47 | IO_L11P_T1_SRCC_16 | D26 |
| DIMM_DDR3_D48 | IO_L13P_T2_MRCC_16 | D27 |
| DIMM_DDR3_D49 | IO_L17N_T2_16 | A30 |
| DIMM_DDR3_D50 | IO_L16N_T2_16 | C30 |
| DIMM_DDR3_D51 | IO_L16P_T2_16 | D29 |
| DIMM_DDR3_D52 | IO_L13N_T2_MRCC_16 | C27 |
| DIMM_DDR3_D53 | IO_L17P_T2_16 | B30 |
| DIMM_DDR3_D54 | IO_L18P_T2_16 | E29 |
| DIMM_DDR3_D55 | IO_L14P_T2_SRCC_16 | E28 |
| DIMM_DDR3_D56 | IO_L20N_T3_16 | F28 |
| DIMM_DDR3_D57 | IO_L22N_T3_16 | F30 |
| DIMM_DDR3_D58 | IO_L24P_T3_16 | H30 |
| DIMM_DDR3_D59 | IO_L20P_T3_16 | G28 |
| DIMM_DDR3_D60 | IO_L19P_T3_16 | H24 |
| DIMM_DDR3_D61 | IO_L22P_T3_16 | G29 |
| DIMM_DDR3_D62 | IO_L23N_T3_16 | H27 |
| DIMM_DDR3_D63 | IO_L23P_T3_16 | H26 |
| DIMM_DDR3_DM0 | IO_L4P_T0_18 | K13 |
| DIMM_DDR3_DM1 | IO_L11P_T1_SRCC_18 | H14 |

| DIMM_DDR3_DM2 | IO_L18P_T2_18 | D11 |
|---|---|---|
| DIMM_DDR3_DM3 | IO_L20P_T3_18 | E14 |
| DIMM_DDR3_DM4 | IO_L5P_T0_16 | F26 |
| DIMM_DDR3_DM5 | IO_L12P_T1_MRCC_16 | C25 |
| DIMM_DDR3_DM6 | IO_L14N_T2_SRCC_16 | D28 |
| DIMM_DDR3_DM7 | IO_L24N_T3_16 | G30 |
| DIMM_DDR3_DQS0_P | IO_L3P_T0_DQS_18 | L12 |
| DIMM_DDR3_DQS0_N | IO_L3N_T0_DQS_18 | L13 |
| DIMM_DDR3_DQS1_P | IO_L9P_T1_DQS_18 | J16 |
| DIMM_DDR3_DQS1_N | IO_L9N_T1_DQS_18 | H16 |
| DIMM_DDR3_DQS2_P | IO_L15P_T2_DQS_18 | C12 |
| DIMM_DDR3_DQS2_N | IO_L15N_T2_DQS_18 | B12 |
| DIMM_DDR3_DQS3_P | IO_L21P_T3_DQS_18 | D14 |
| DIMM_DDR3_DQS3_N | IO_L21N_T3_DQS_18 | C14 |
| DIMM_DDR3_DQS4_P | IO_L3P_T0_DQS_16 | F25 |
| DIMM_DDR3_DQS4_N | IO_L3N_T0_DQS_16 | E25 |
| DIMM_DDR3_DQS5_P | IO_L9P_T1_DQS_16 | B28 |
| DIMM_DDR3_DQS5_N | IO_L9N_T1_DQS_16 | A28 |
| DIMM_DDR3_DQS6_P | IO_L15P_T2_DQS_16 | C29 |
| DIMM_DDR3_DQS6_N | IO_L15N_T2_DQS_16 | B29 |
| DIMM_DDR3_DQS7_P | IO_L21P_T3_DQS_16 | G27 |
| DIMM_DDR3_DQS7_N | IO_L21N_T3_DQS_16 | F27 |
| DIMM_DDR3_A0 | IO_L11P_T1_SRCC_17 | F21 |
| DIMM_DDR3_A1 | IO_L8P_T1_17 | D21 |
| DIMM_DDR3_A2 | IO_L11N_T1_SRCC_17 | E21 |
| DIMM_DDR3_A3 | IO_L16N_T2_17 | F18 |
| DIMM_DDR3_A4 | IO_L3N_T0_DQS_17 | H17 |
| DIMM_DDR3_A5 | IO_L17N_T2_17 | B17 |
| DIMM_DDR3_A6 | IO_L4P_T0_17 | J19 |
| DIMM_DDR3_A7 | IO_L17P_T2_17 | C17 |
| DIMM_DDR3_A8 | IO_L1N_T0_17 | J18 |
| DIMM_DDR3_A9 | IO_L15N_T2_DQS_17 | C16 |
| DIMM_DDR3_A10 | IO_L6P_T0_17 | K19 |
| DIMM_DDR3_A11 | IO_L16P_T2_17 | G18 |

| | | |
|---|---|---|
| DIMM_DDR3_A12 | IO_L1P_T0_17 | K18 |
| DIMM_DDR3_A13 | IO_L9P_T1_DQS_17 | G22 |
| DIMM_DDR3_A14 | IO_L15P_T2_DQS_17 | D16 |
| DIMM_DDR3_A15 | IO_L5N_T0_17 | L18 |
| DIMM_DDR3_BA0 | IO_L4N_T0_17 | H19 |
| DIMM_DDR3_BA1 | IO_L2P_T0_17 | H20 |
| DIMM_DDR3_BA2 | IO_L3P_T0_DQS_17 | J17 |
| DIMM_DDR3_WE | IO_L7P_T1_17 | H21 |
| DIMM_DDR3_RAS | IO_L2N_T0_17 | G20 |
| DIMM_DDR3_CAS | IO_L6N_T0_VREF_17 | K20 |
| DIMM_DDR3_S0 | IO_L9N_T1_DQS_17 | F22 |
| DIMM_DDR3_S1 | IO_L8N_T1_17 | C21 |
| DIMM_DDR3_CKE0 | IO_L5P_T0_17 | L17 |
| DIMM_DDR3_CKE1 | IO_L18P_T2_17 | G17 |
| DIMM_DDR3_ODT0 | IO_L10P_T1_17 | D22 |
| DIMM_DDR3_ODT1 | IO_L7N_T1_17 | H22 |
| DIMM_DDR3_CLK0_P | IO_L12P_T1_MRCC_17 | D17 |
| DIMM_DDR3_CLK0_N | IO_L12N_T1_MRCC_17 | D18 |
| DIMM_DDR3_CLK1_P | IO_L14P_T2_SRCC_17 | E19 |
| DIMM_DDR3_CLK1_N | IO_L14N_T2_SRCC_17 | D19 |
| DIMM_DDR3_RESET | IO_L18N_T2_17 | F17 |

# Part 5: QSPI Flash

The AX7325B FPGA development board is equipped with one128MBit Quad-SPI FLASH, and the model is N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store FPGA configuration Bin files and other user data files in use. The specific models and related parameters of QSPI FLASH are shown in Table 5-1.

| Position | Model | Capacity | Factory |
|---|---|---|---|
| U7 | N25Q128 | 128M Bit | Numonyx |

Table 5-1: QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of

the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip select signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 5-1 shows the hardware connection of QSPI Flash.
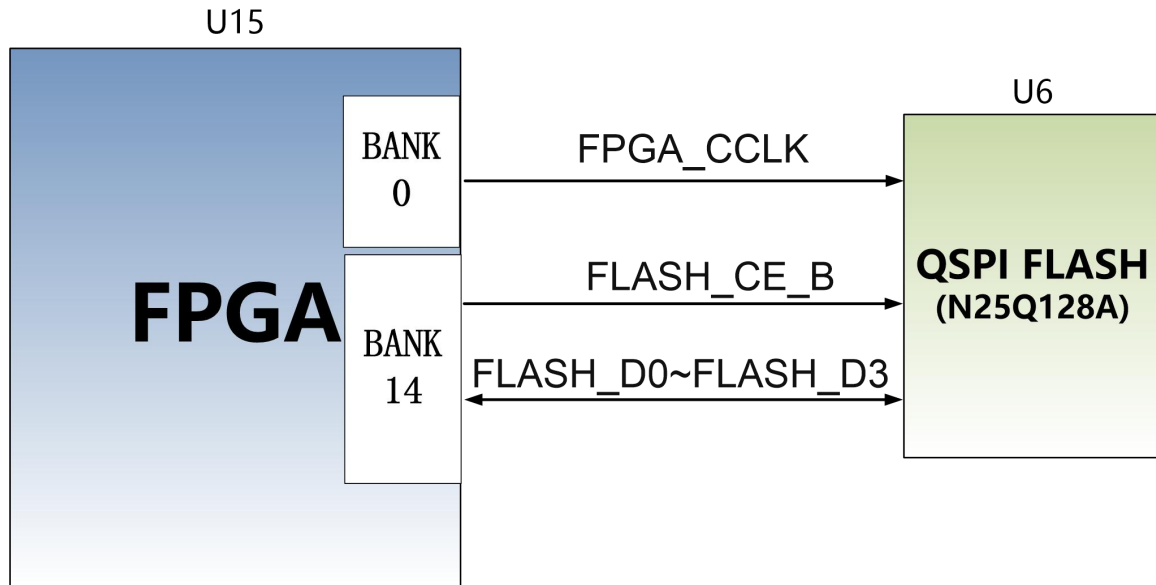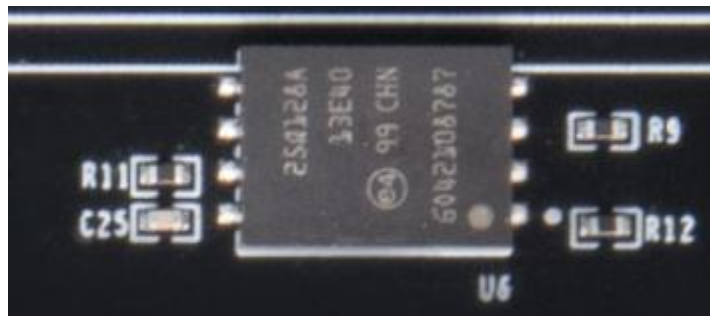


Figure 5-1: QSPI Flash Schematic



Figure 5-2: QSPI Flash on the FPGA Board

### QSPI Flash pin assignments:

| Signal Name | FPGA Pin Name | FPGA Pin Number |
|---|---|---|
| FPGA_CCLK | CCLK_0 | B10 |
| FLASH_CE_B | IO_L6P_T0_FCS_B_14 | U19 |
| FLASH_D0 | IO_L1P_T0_D00_MOSI_14 | P24 |
| FLASH_D1 | IO_L1N_T0_D01_DIN_14 | R25 |
| FLASH_D2 | IO_L2P_T0_D02_14 | R20 |
| FLASH_D3 | IO_L2N_T0_D03_14 | R21 |

# Part 6: Clock configuration

The ax7325b development board provides four differential active clocks for the FPGA system. Two 200MHz differential clocks are respectively connected to bank17 and bank33 to provide reference clock for DDR controller. The other two differential clocks, 125MHz and 156.25mhz respectively, are connected to bank117 and bank118 to provide differential clock sources for the GTX part of the high-speed transceiver. The schematic diagram of clock circuit design is shown in Figure 6-1 below:
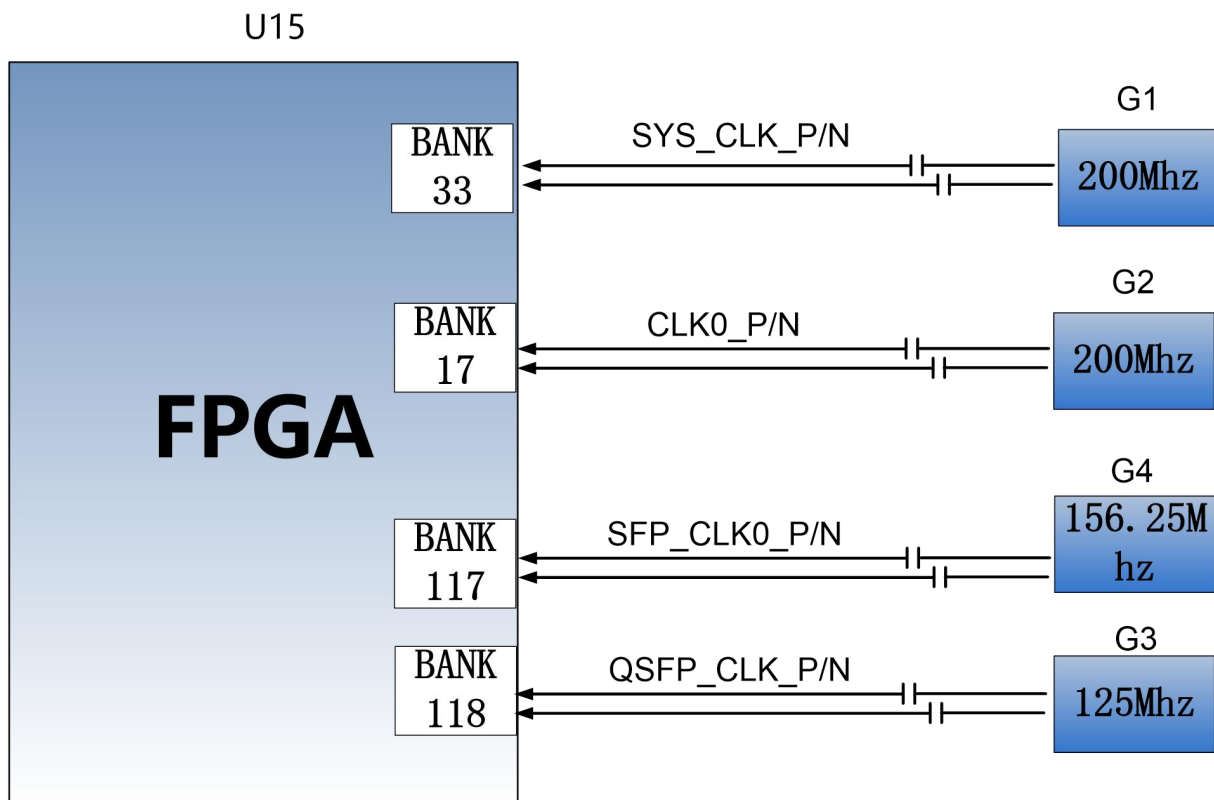


Figure 6-1: Programmable Clock Source Schematic

**Programmable Clock Source FPGA pin assignments:**

| Signal Name | FPGA Pin |
|---|---|
| SYS_CLK_P | AE10 |
| SYS_CLK_N | AF10 |
| CLK0_P | F20 |

| CLK0_N | E20 |
|---|---|
| SFP_CLK0_P | G8 |
| SFP_CLK0_N | G7 |
| QSFP_CLK_P | C8 |
| QSFP_CLK_N | C7 |
| SYS_CLK_P | AE10 |
| SYS_CLK_N | AF10 |

# Part7: USB to Serial Port

The AX7325B FPGA development board is equipped with a Uart to USB interface for serial communication and debugging of the development board. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The CP2102 serial chip and the FPGA are connected by a level-shifting chip to adapt to different FPGA BANK voltages. The USB interface uses the MINI USB interface, which can be connected to the USB port of the upper PC for serial data communication on the FPGA development board with a USB cable. The schematic diagram of the USB Uart circuit design is shown below:
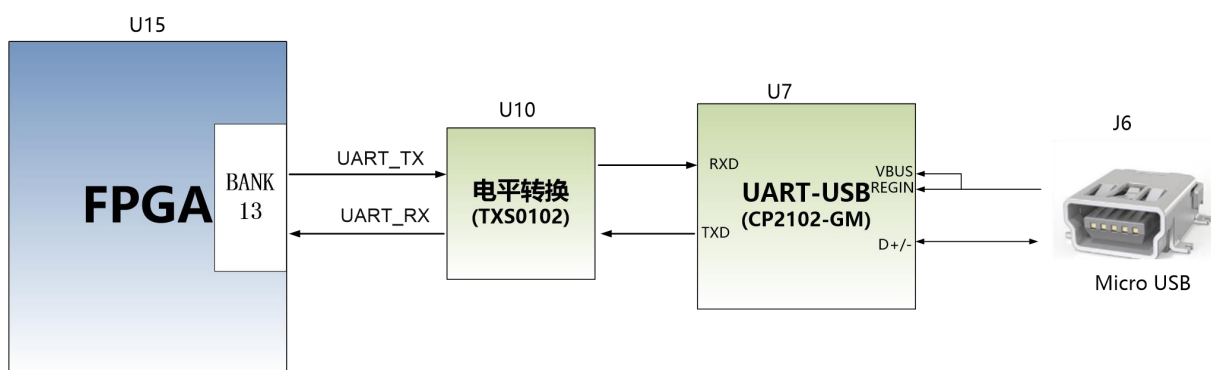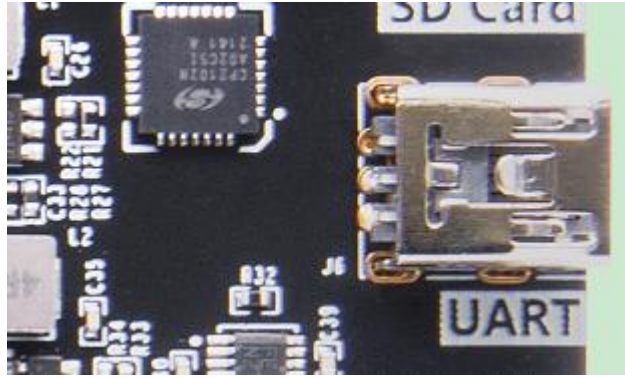


Figure 7-1: USB to serial port schematic

Figure 7-2: USB to serial port on the FPGA Board

**USB to serial port pin assignment:**

| Signal Name | FPGA Pin Name | FPGA Pin Number | Description |
|---|---|---|---|
| UART_RX | PS_MIO13_500 | AJ26 | Uart Data Input |
| UART_TX | PS_MIO12_500 | AK26 | Uart Data Output |

# Part 8: SFP Interface

The AX7325B FPGA development board has four optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5Goptical modules on the market) and insert them into these four optical interfaces for optical data communication. The four fiber interfaces are connected to the four RX/TXs of the GNK transceiver of the FPGA BANK117. The TX signal and the RX signal are connected to the FPGA and the optical module through a DC blocking capacitor in a differential signal mode. Each TX transmit and RX receive data rate is up to 10Gb/s. The BANK117's GTX transceiver reference clock is provided by the 156.25Mhz System Clock.
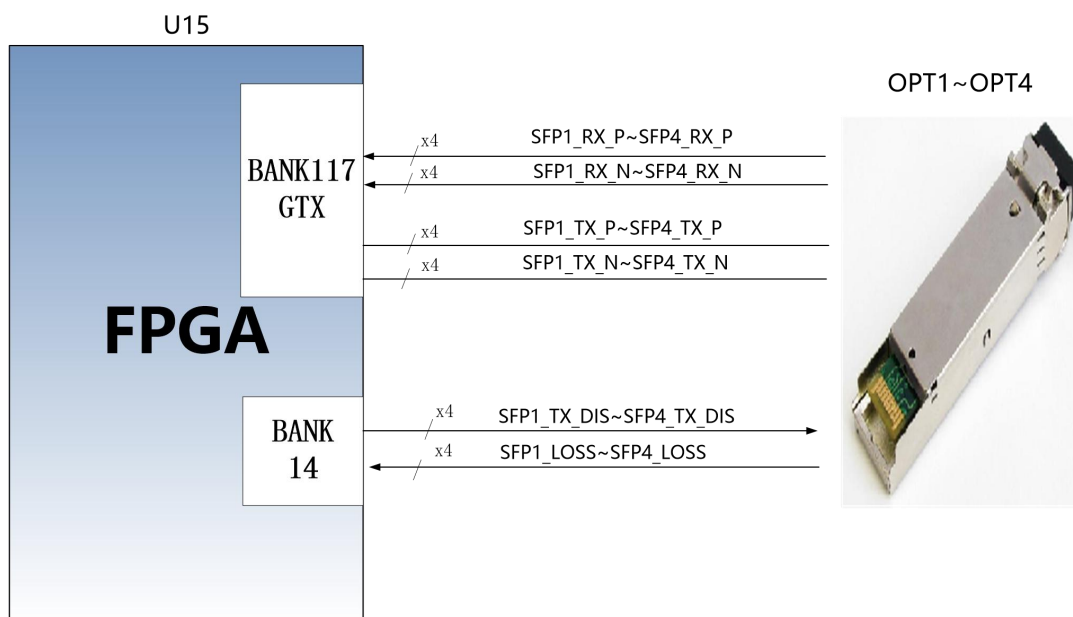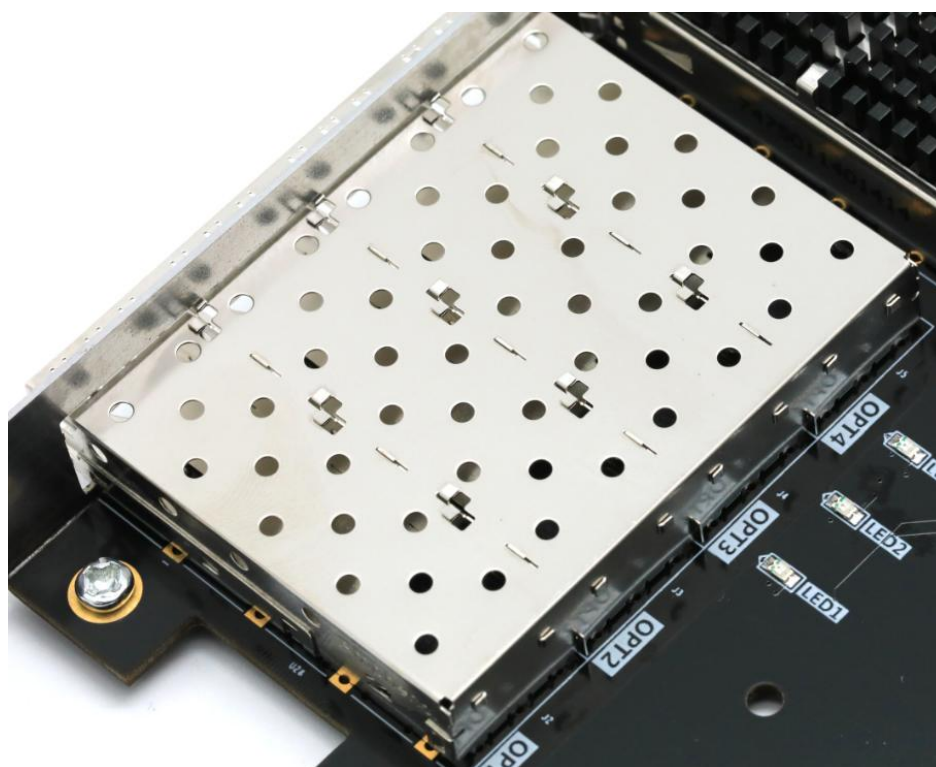
Figure 8-1: Optical Fiber Design Schematic



Figure 8-2: SFP interfaces on the FPGA Board

**The 1st fiber interface FPGA pin assignment is as follows:**

| Signal Name | FPGA PIN | Description |
|---|---|---|
| SFP1_TX_P | K2 | SFP1 Data Transfer (Positive) |

| SFP1_TX_N | K1 | SFP1 Data Transfer (Negative) |
| SFP1_RX_P | K6 | SFP1 Data Receiver (Positive) |
| SFP1_RX_P | K5 | SFP1 Data Receiver (Negative) |
| SFP1_TX_DIS | T28 | SFP1 Optical Transfer Disable, active high |
| SFP1_LOSS | R28 | SFP1 Optical LOSS,High level means no light signal is received |

## The 2ⁿᵈ fiber interface FPGA pin assignment is as follows:

| Signal Name | FPGA PIN | Description |
|---|---|---|
| SFP2_TX_P | J4 | SFP2 Data Transfer (Positive) |
| SFP2_TX_N | J3 | SFP2 Data Transfer (Negative) |
| SFP2_RX_P | H6 | SFP2 Data Receiver (Positive) |
| SFP2_RX_P | H5 | SFP2 Data Receiver (Negative) |
| SFP2_TX_DIS | T28 | SFP2Optical Transfer Disable, active high |
| SFP2_LOSS | T26 | SFP2 Optical LOSS,High level means no light signal is received |

## The 3ʳᵈ fiber interface FPGA pin assignment is as follows:

| Signal Name | FPGA PIN | Description |
|---|---|---|
| SFP3_TX_P | H2 | SFP3 Data Transfer (Positive) |
| SFP3_TX_N | H1 | SFP3 Data Transfer (Negative) |
| SFP3_RX_P | G4 | SFP3 Data Receiver (Positive) |
| SFP3_RX_P | G3 | SFP3 Data Receiver (Negative) |
| SFP3_TX_DIS | U28 | SFP3 Optical Transfer Disable, active high |
| SFP3_LOSS | U27 | SFP3 Optical LOSS,High level means no light signal is received |

## The 4ᵗʰ fiber interface FPGA pin assignment is as follows:

| Signal Name | FPGA PIN | Description |
|---|---|---|
| SFP4_TX_P | F2 | SFP4 Data Transfer (Positive) |
| SFP4_TX_N | F1 | SFP4 Data Transfer (Negative) |
| SFP4_RX_P | F6 | SFP4 Data Receiver (Positive) |
| SFP4_RX_P | F5 | SFP4 Data Receiver (Negative) |
| SFP4_TX_DIS | U25 | SFP4 Optical Transfer Disable, active high |
| SFP4_LOSS | A18 | SFP4 Optical LOSS,High level means no light signal is received |

# Part 9: QSFP+ Fiber interface

The AX7325B development board has a four-small fiber optic interface that plugs into the QSFP+. The fiber optic transceiver integrates 4 transmit channels and 4 receive channels. This 4-channel pluggable interface has a transfer rate of 40Gbps. It need the customer's requirements of Meets users' higher-density, high-speed pluggable fiber-optic communication solutions.

The transceiver signal of the QSFP+ fiber interface is directly connected to the GNK transceiver of the FPGA BANK118. The four TX signals and RX signals of the fiber are directly connected to the GTX transceiver. Because the speed of a single GTX is as high as 10 Gbps, the speed of four GTXs can be as high as 40 Gbps. The reference clock for the BANK118's GTX transceiver is provided by the 125Mhz System Clock.

The QSFP+ fiber design diagram of the FPGA development board is shown in Figure 9-1, where the control signal of the fiber is connected to the BANK14 of the FPGA.
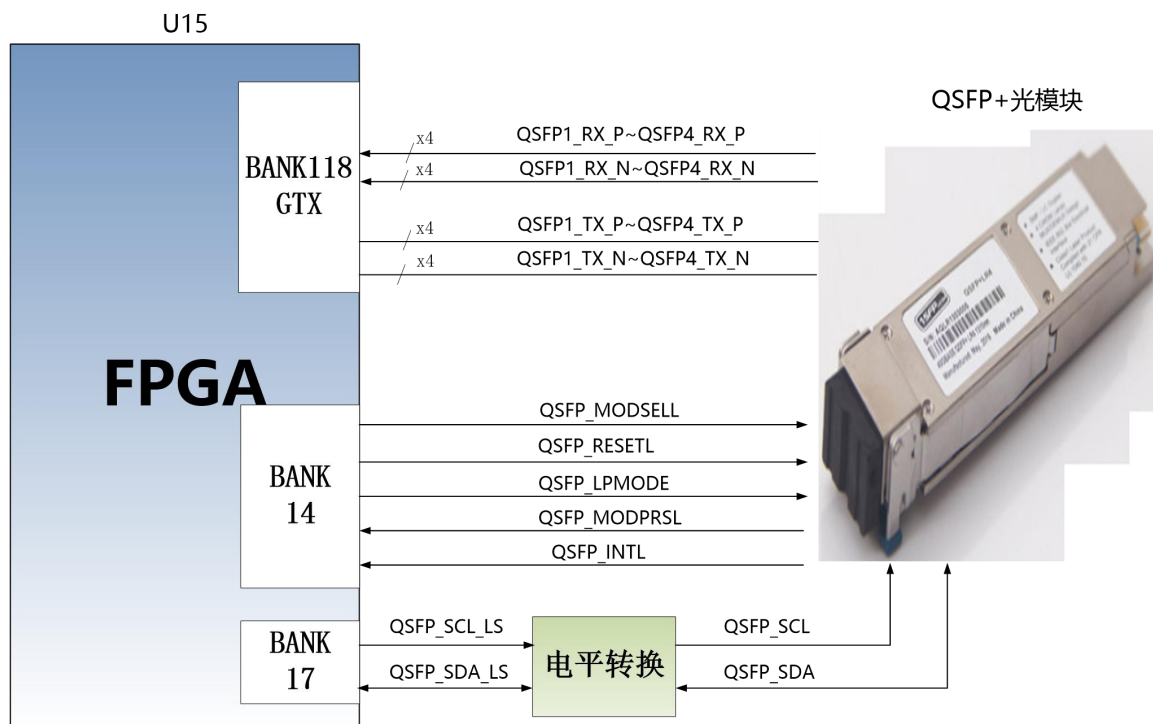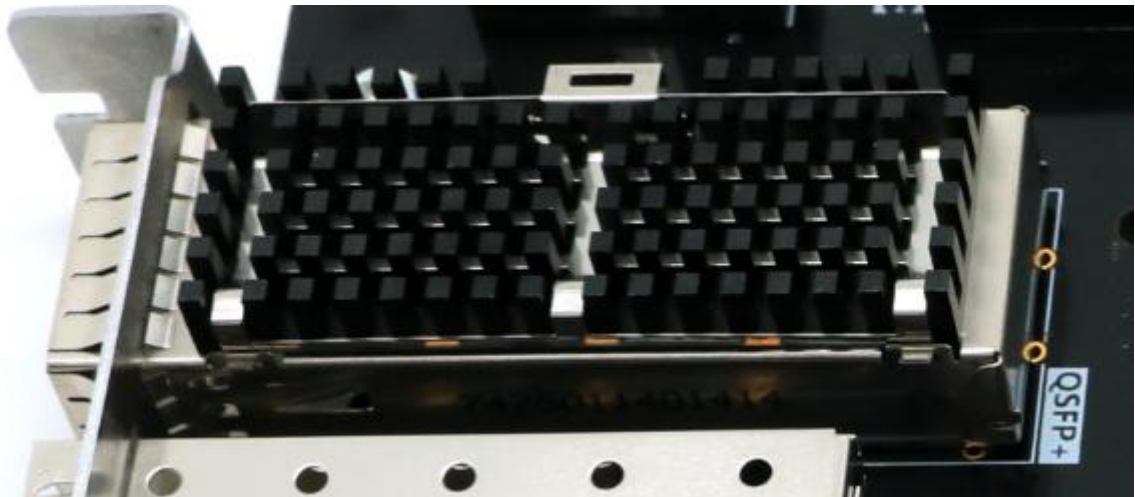


Figure 9-1: QSFP+ Fiber Design Diagram

Figure 9-2: QSFP+ fiber communication interface on the Board

## The QSFP+ fiber interface FPGA pin assignments are as follows:

| Signal Name | FPGA Pin | Description |
|---|---|---|
| QSFP1_TX_P | D2 | QSFP + 1st Channel Data Transmission Positive |
| QSFP1_TX_N | D1 | QSFP + 1st Channel Data Transmission Negative |
| QSFP2_TX_P | B2 | QSFP + 2nd Channel Data Transmission Positive |
| QSFP2_TX_N | B1 | QSFP + 2nd Channel Data Transmission Negative |
| QSFP3_TX_P | C4 | QSFP + 3rd Channel Data Transmission Positive |
| QSFP3_TX_N | C3 | QSFP + 3rd Channel Data Transmission Negative |
| QSFP4_TX_P | A4 | QSFP + 4th Channel Data Transmission Positive |
| QSFP4_TX_N | A3 | QSFP + 4th Channel Data Transmission Negative |
| QSFP1_RX_P | E4 | QSFP + 1st Channel Data Send Positive |
| QSFP1_RX_N | E3 | QSFP + 1st Channel Data Send Negative |
| QSFP2_RX_P | B6 | QSFP + 2nd Channel Data Send Positive |
| QSFP2_RX_N | B5 | QSFP + 2nd Channel Data Send Negative |
| QSFP3_RX_P | D6 | QSFP + 3rd Channel Data Send Positive |
| QSFP3_RX_N | D5 | QSFP + 3rd Channel Data Send Negative |
| QSFP4_RX_P | A8 | QSFP + 4th Channel Data Send Positive |
| QSFP4_RX_N | A7 | QSFP + 4th Channel Data Send Negative |
| QSFP_MODSELL | R30 | Mode selection, low level I2C is valid |
| QSFP_RESETL | U30 | Reset signal, low reset |
| QSFP_MODPRSL | U22 | The optical module has a signal and is active low. |
| QSFP_INTL | R24 | Interrupt Signal, Active Low |

| QSFP_LPMODE | V26 | Low Power Mode Selection |
|---|---|---|
| QSFP_SCL | A20 | I2C Clock Signal |
| QSFP_SDA | A21 | I2C Data Signal |

# Part 10: PCIe slot

The AX7325B FPGA development board provides an industrial-grade high-speed data transfer PCIe x8 interface. The PCIE card interface conforms to the standard PCIe card electrical specifications and can be used directly on the x8 PCIe slot of a normal PC. Data communication between PCIEex8, PCIEex4, PCIex2, and PCIex1 can be realized between the FPGA development board and the computer.

The transmit and receive signals of the PCIe interface are directly connected to the GTX transceivers of the FPGA BANK115 and BANK116. The 8 TX signals and RX signals are connected to the BANK115 and BANK116 by differential signals. Supports PCI Express 2.0 standard, single channel communication rate up to 5Gbps.

The design diagram of the PCIe interface of the AX7325B FPGA development board is shown in Figure 10-1, where the TX transmit signal and the reference clock CLK signal are connected in AC coupled mode.
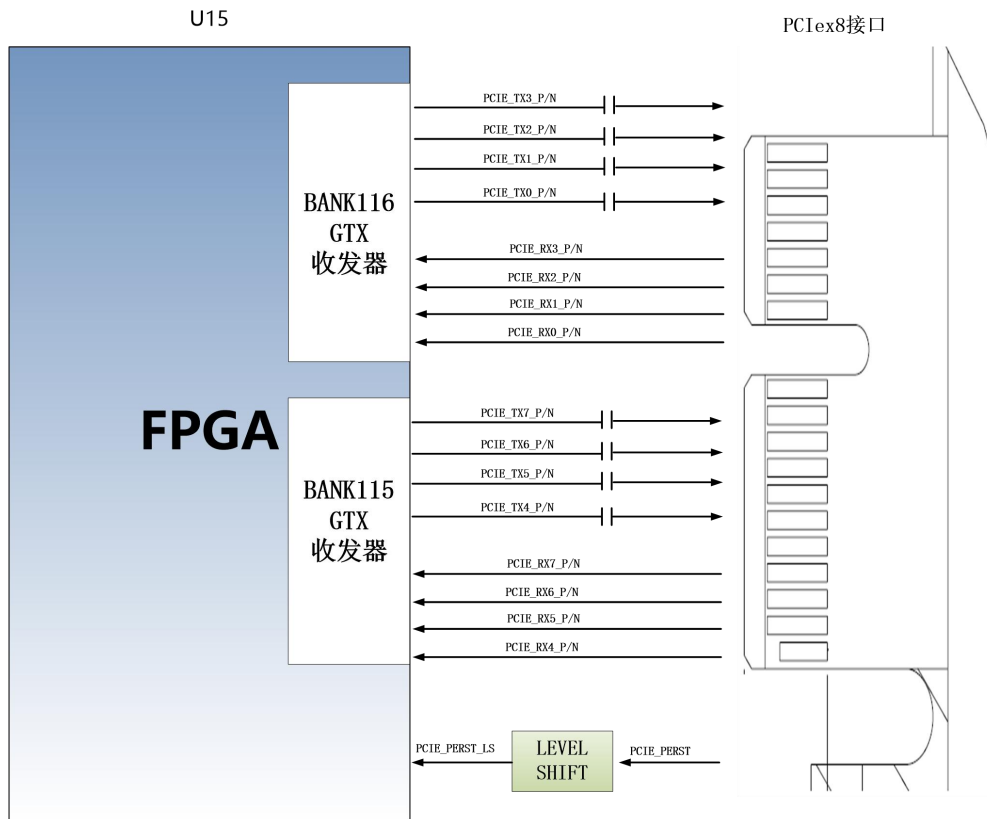
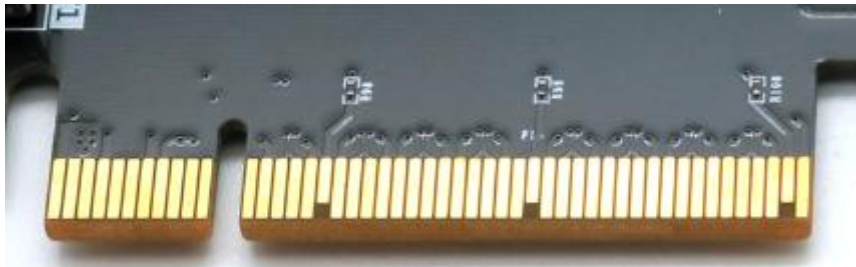Figure 10-1: PCIe x 8 Interface Design Diagram



Figure 10-2: PCIex8 on the FPGA Board

## PCIex8 Interface Pin Assignment:

| Signal Name | FPGA Pin | Description |
|---|---|---|
| PCIE_RX0_P | M6 | PCIE Channel 0 Data Receive Positive |
| PCIE_RX0_N | M5 | PCIE Channel 0 Data Receive Negative |
| PCIE_RX1_P | P6 | PCIE Channel 1 Data Receive Positive |
| PCIE_RX1_N | P5 | PCIE Channel 1 Data Receive Negative |
| PCIE_RX2_P | R4 | PCIE Channel 2 Data Receive Positive |
| PCIE_RX2_N | R3 | PCIE Channel 2 Data Receive Negative |

| | | |
|---|---|---|
| PCIE_RX3_P | T6 | PCIE Channel 3 Data Receive Positive |
| PCIE_RX3_N | T5 | PCIE Channel 3 Data Receive Negative |
| PCIE_RX4_P | V6 | PCIE Channel 4 Data Receive Positive |
| PCIE_RX4_N | V5 | PCIE Channel 4 Data Receive Negative |
| PCIE_RX5_P | W4 | PCIE Channel 5 Data Receive Positive |
| PCIE_RX5_N | W3 | PCIE Channel 5 Data Receive Negative |
| PCIE_RX6_P | Y6 | PCIE Channel 6 Data Receive Positive |
| PCIE_RX6_N | Y5 | PCIE Channel 6 Data Receive Negative |
| PCIE_RX7_P | AA4 | PCIE Channel 7 Data Receive Positive |
| PCIE_RX7_N | AA3 | PCIE Channel 7 Data Receive Negative |
| PCIE_TX0_P | L4 | PCIE Channel 0 Data Transmit Positive |
| PCIE_TX0_N | L3 | PCIE Channel 0 Data Transmit Negative |
| PCIE_TX1_P | M2 | PCIE Channel 1 Data Transmit Positive |
| PCIE_TX1_N | M1 | PCIE Channel 1 Data Transmit Negative |
| PCIE_TX2_P | N4 | PCIE Channel 2 Data Transmit Positive |
| PCIE_TX2_N | N3 | PCIE Channel 2 Data Transmit Negative |
| PCIE_TX3_P | P2 | PCIE Channel 3 Data Transmit Positive |
| PCIE_TX3_N | P1 | PCIE Channel 3 Data Transmit Negative |
| PCIE_TX4_P | T2 | PCIE Channel 4 Data Transmit Positive |
| PCIE_TX4_N | T1 | PCIE Channel 4 Data Transmit Negative |
| PCIE_TX5_P | U4 | PCIE Channel 5 Data Transmit Positive |
| PCIE_TX5_N | U3 | PCIE Channel 5 Data Transmit Negative |
| PCIE_TX6_P | V2 | PCIE Channel 6 Data Transmit Positive |
| PCIE_TX6_N | V1 | PCIE Channel 6 Data Transmit Negative |
| PCIE_TX7_P | Y2 | PCIE Channel 7 Data Transmit Positive |
| PCIE_TX7_N | Y1 | PCIE Channel 7 Data Transmit Negative |
| PCIE_PERST | B18 | PCIE Board Reset Signal |

# Part 11: Temperature Sensor

A high-precision, low-power, digital temperature sensor chip is mounted on the AX7325B FPGA development board, and the model is LM75 of ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees. The sensor and FPGA are directly connected to the I2C digital interface. The FPGA reads the temperature near the current FPGA development board

through the I2C interface. Figure 11-1 below shows the design of the LM75 sensor chip.
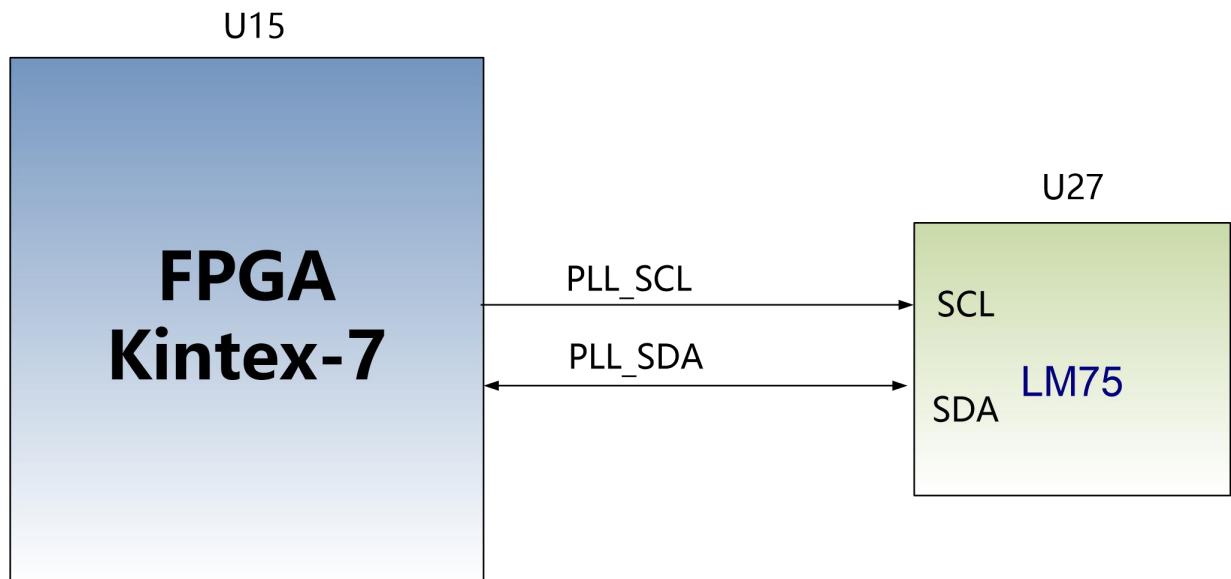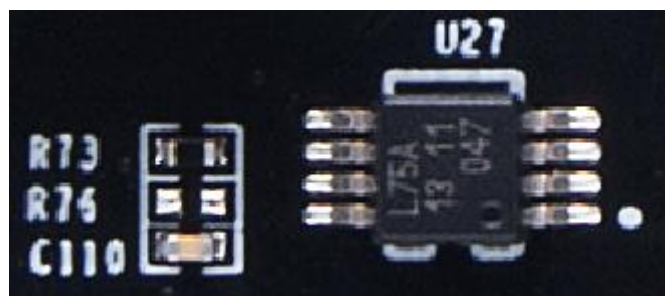
U15



Figure 11-1: LM75 Sensor Schematic



Figure 11-2: LM75 Sensor on the FPGA Board

**LM75 Sensor Pin Assignment**

| Pin Name | FPGA Pin |
|---|---|
| LM75_SCL | P23 |
| LM75_SDA | N25 |

# Part 12: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was

completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted substantial research and development. In 2000, these companies launched the SD Association (Secure Digital Association), which has a strong lineup and attracted a large number of vendors. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

The AX7325B development board includes a Micro SD card interface to provide users with access to SD card memory for storing pictures, music or other user data files.

The SDIO signal is connected to the IO signal of the FPGA BANK12, because the VCCIO of the BANK is VADJ, the default is +2.5V. However, the SD card has a data level of 3.3 and needs to be connected via the TXS02612 level shifter. The schematic diagram of the FPGA and SD card connector is shown in Figure 12-1.
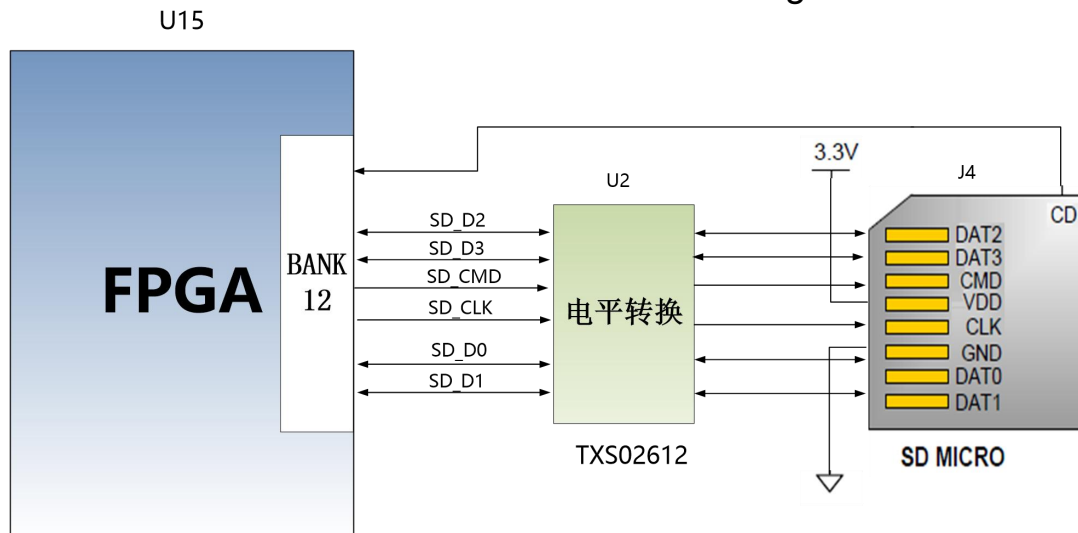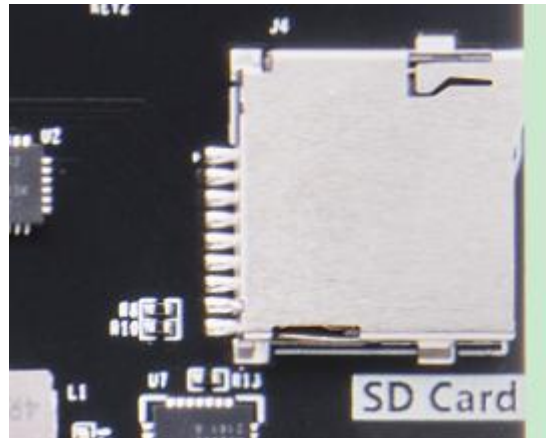


Figure 12-1: SD Card Slot Schematic

Figure 12-2: SD Card Slot on the FPGA Board

**SD Card Slotpin assignment:**

| Signal Name | FPGA Pin | FPGA Pin Number | Description |
|---|---|---|---|
| SD_CLK | IO_L23P_T3_12 | AH21 | SD Clock Signal |
| SD_CMD | IO_L23N_T3_12 | AJ21 | SD Command Signal |
| SD_D0 | IO_L21P_T3_DQS_12 | AJ22 | SDData0 |
| SD_D1 | IO_L21N_T3_DQS_12 | AJ23 | SDData1 |
| SD_D2 | IO_L22P_T3_12 | AG20 | SDData2 |
| SD_D3 | IO_L22N_T3_12 | AH20 | SDData3 |
| SD_CD | IO_25_12 | AE20 | SD card insertion signal |

# Part 13: FMC connector

The AX7325B development board comes with a standard FMC LPC expansion port that can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 34 pairs of differential IO signals and one I2C bus signal.

The 33 pairs of differential signals of the FMC expansion port are connected to the IO of the BANK12 and BANK13 of the FPGA chip. The IO level standard of BANK12 and BANK13 is determined by the voltage VADJ of

BANK. The default is +2.5V. The 34 pairs of differential signals connected to the FMC support LVDS data communication. The schematic of the FPGA and FMC connectors is shown in Figure 13-1:
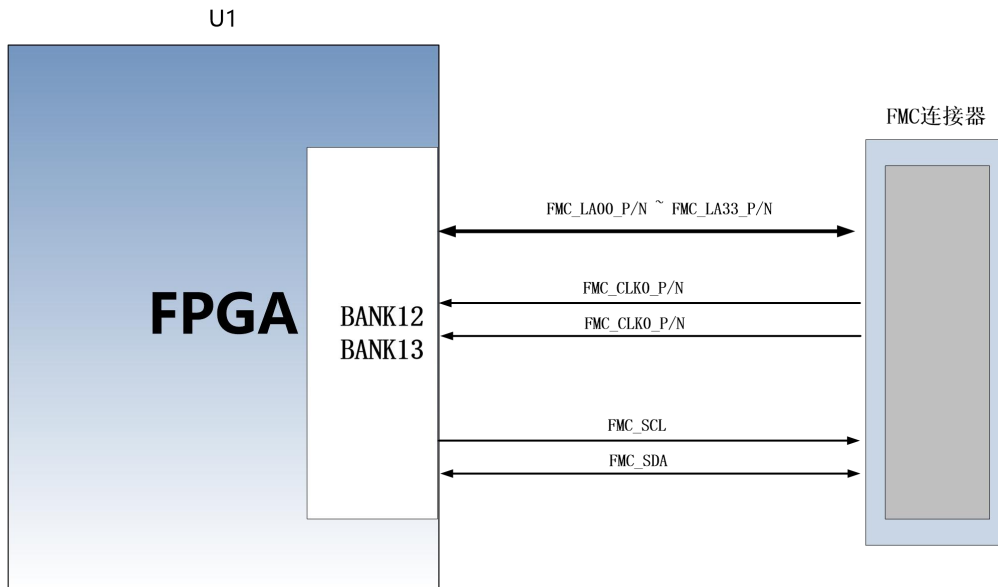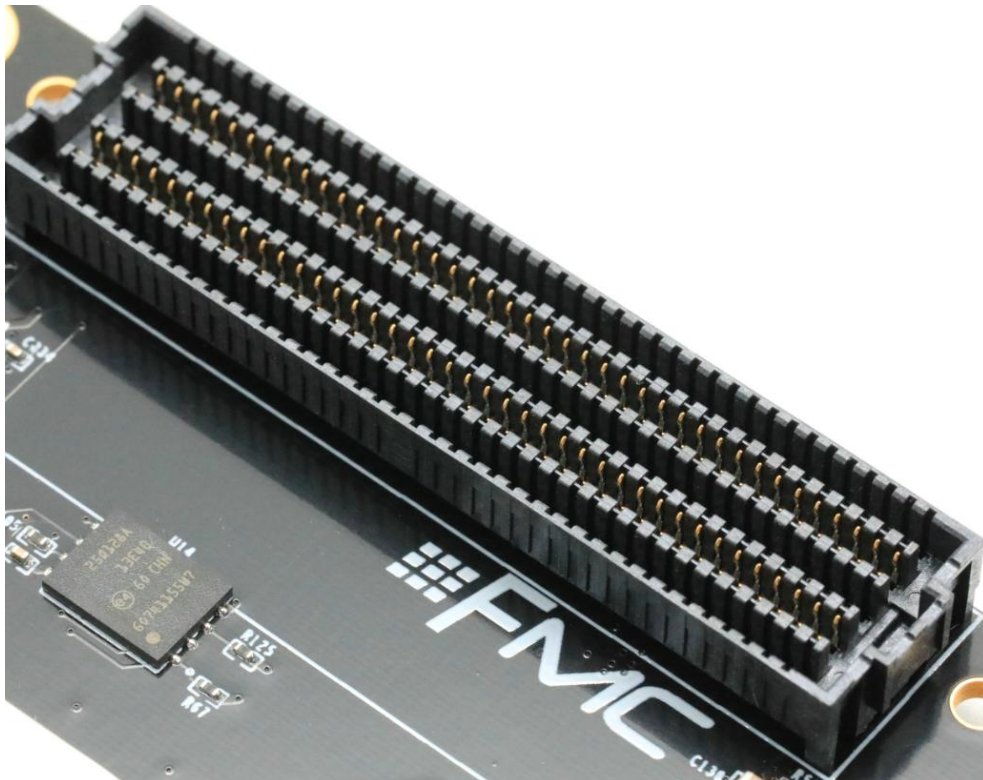


Figure 13-1：FMC Connector diagram



Figure 13-2：FMC Connector on the FPGA Board

**FMC Connectors Pin Assignment**

| Signal Name | FPGA Pin Numer | FPGA Pin Number | Description |
|---|---|---|---|
| FMC_CLK0_P | IO_L12P_T1_MRCC_12 | AD23 | FMC reference 1st reference clock P |
| FMC_CLK0_N | IO_L12N_T1_MRCC_12 | AE24 | FMC reference 1st reference clock N |
| FMC_CLK1_P | IO_L13P_T2_MRCC_13 | AG29 | FMC reference 2nd reference clock P |
| FMC_CLK1_N | IO_L13N_T2_MRCC_13 | AH29 | FMC reference 2nd reference clock N |
| FMC_LA00_CC_P | IO_L13P_T2_MRCC_12 | AF22 | FMC reference 0th channel data (clock) P |
| FMC_LA00_CC_N | IO_L13N_T2_MRCC_12 | AG23 | FMC reference 0th channel data (clock) N |
| FMC_LA01_CC_P | IO_L14P_T2_SRCC_12 | AG24 | FMC reference 1st channel data (clock) P |
| FMC_LA01_CC_N | IO_L14N_T2_SRCC_12 | AH24 | FMC reference 1st channel data (clock) N |
| FMC_LA02_P | IO_L17P_T2_12 | AK23 | FMC reference 2nd channel data P |
| FMC_LA02_N | IO_L17N_T2_12 | AK24 | FMC reference 2nd channel data N |
| FMC_LA03_P | IO_L15P_T2_DQS_12 | AJ24 | FMC reference 3rd channel data P |
| FMC_LA03_N | IO_L15N_T2_DQS_12 | AK25 | FMC reference 3rd channel data N |
| FMC_LA04_P | IO_L18P_T2_12 | AG25 | FMC reference 4th channel data P |
| FMC_LA04_N | IO_L18N_T2_12 | AH25 | FMC reference 4th channel data N |
| FMC_LA05_P | IO_L11P_T1_SRCC_12 | AE23 | FMC reference 5th channel data P |
| FMC_LA05_N | IO_L11N_T1_SRCC_12 | AF23 | FMC reference 5th channel data N |
| FMC_LA06_P | IO_L20P_T3_12 | AG22 | FMC reference 6th channel data P |
| FMC_LA06_N | IO_L20N_T3_12 | AH22 | FMC reference 6th channel data N |
| FMC_LA07_P | IO_L9P_T1_DQS_12 | AC24 | FMC reference 7th channel data P |
| FMC_LA07_N | IO_L9N_T1_DQS_12 | AD24 | FMC reference 7th channel data N |
| FMC_LA08_P | IO_L16P_T2_12 | AE25 | FMC reference 8th channel data P |
| FMC_LA08_N | IO_L16N_T2_12 | AF25 | FMC reference 8th channel data N |
| FMC_LA09_P | IO_L8P_T1_12 | AC22 | FMC reference 9th channel data P |
| FMC_LA09_N | IO_L8N_T1_12 | AD22 | FMC reference 9th channel data N |
| FMC_LA10_P | IO_L10P_T1_12 | AD21 | FMC reference 10th channel data P |
| FMC_LA10_N | IO_L10N_T1_12 | AE21 | FMC reference 10th channel data N |
| FMC_LA11_P | IO_L3P_T0_DQS_12 | AB22 | FMC reference 11th channel data P |
| FMC_LA11_N | IO_L3N_T0_DQS_12 | AB23 | FMC reference 11th channel data N |
| FMC_LA12_P | IO_L7P_T1_12 | AB24 | FMC reference 12th channel data P |
| FMC_LA12_N | IO_L7N_T1_12 | AC25 | FMC reference 12th channel data N |

| FMC_LA13_P | IO_L5P_T0_12 | AC20 | FMC reference 13th channel data P |
|---|---|---|---|
| FMC_LA13_N | IO_L5N_T0_12 | AC21 | FMC reference 13th channel data N |
| FMC_LA14_P | IO_L2P_T0_12 | Y21 | FMC reference 14th channel data P |
| FMC_LA14_N | IO_L2N_T0_12 | AA21 | FMC reference 14th channel data N |
| FMC_LA15_P | IO_L1P_T0_12 | Y23 | FMC reference 15th channel data P |
| FMC_LA15_N | IO_L1N_T0_12 | Y24 | FMC reference 15th channel data N |
| FMC_LA16_P | IO_L4P_T0_12 | AA22 | FMC reference 16th channel data P |
| FMC_LA16_N | IO_L4N_T0_12 | AA23 | FMC reference 16th channel data N |
| FMC_LA17_CC_P | IO_L14P_T2_SRCC_13 | AE28 | FMC reference 17th channel data (clock) P |
| FMC_LA17_CC_N | IO_L14N_T2_SRCC_13 | AF28 | FMC reference 17th channel data (clock) P |
| FMC_LA18_CC_P | IO_L12P_T1_MRCC_13 | AB27 | FMC reference 18th channel data (clock) P |
| FMC_LA18_CC_N | IO_L12N_T1_MRCC_13 | AC27 | FMC reference 18th channel data (clock) P |
| FMC_LA19_P | IO_L15P_T2_DQS_13 | AK29 | FMC reference 19th channel data P |
| FMC_LA19_N | IO_L15N_T2_DQS_13 | AK30 | FMC reference 19th channel data N |
| FMC_LA20_P | IO_L20P_T3_13 | AJ27 | FMC reference 20th channel data P |
| FMC_LA20_N | IO_L20N_T3_13 | AK28 | FMC reference 20th channel data N |
| FMC_LA21_P | IO_L18P_T2_13 | AG30 | FMC reference 21st channel data P |
| FMC_LA21_N | IO_L18N_T2_13 | AH30 | FMC reference 21st channel data N |
| FMC_LA22_P | IO_L17P_T2_13 | AJ28 | FMC reference 22nd channel data P |
| FMC_LA22_N | IO_L17N_T2_13 | AJ29 | FMC reference 22nd channel data N |
| FMC_LA23_P | IO_L5P_T0_13 | AA27 | FMC reference 23rd channel data P |
| FMC_LA23_N | IO_L5N_T0_13 | AB28 | FMC reference 23rd channel data N |
| FMC_LA24_P | IO_L9P_T1_DQS_13 | AD29 | FMC reference 24th channel data P |
| FMC_LA24_N | IO_L9N_T1_DQS_13 | AE29 | FMC reference 24th channel data N |
| FMC_LA25_P | IO_L16P_T2_13 | AE30 | FMC reference 25th channel data P |
| FMC_LA25_N | IO_L16N_T2_13 | AF30 | FMC reference 25th channel data N |
| FMC_LA26_P | IO_L3P_T0_DQS_13 | Y28 | FMC reference 26th channel data P |
| FMC_LA26_N | IO_L3N_T0_DQS_13 | AA28 | FMC reference 26th channel data N |
| FMC_LA27_P | IO_L1P_T0_13 | Y26 | FMC reference 27th channel data P |
| FMC_LA27_N | IO_L1N_T0_13 | AA26 | FMC reference 27th channel data N |
| FMC_LA28_P | IO_L7P_T1_13 | AC29 | FMC reference 28th channel data P |
| FMC_LA28_N | IO_L7N_T1_13 | AC30 | FMC reference 28th channel data N |

| FMC_LA29_P | IO_L11P_T1_SRCC_13 | AD27 | FMC reference 29th channel data P |
|---|---|---|---|
| FMC_LA29_N | IO_L11N_T1_SRCC_13 | AD28 | FMC reference 29th channel data N |
| FMC_LA30_P | IO_L8P_T1_13 | Y30 | FMC reference 30th channel data P |
| FMC_LA30_N | IO_L8N_T1_13 | AA30 | FMC reference 30th channel data N |
| FMC_LA31_P | IO_L10P_T1_13 | AB29 | FMC reference 31st channel data P |
| FMC_LA31_N | IO_L10N_T1_13 | AB30 | FMC reference 31st channel data N |
| FMC_LA32_P | IO_L2P_T0_13 | W27 | FMC reference 32nd channel data P |
| FMC_LA32_N | IO_L2N_T0_13 | W28 | FMC reference 32nd channel data N |
| FMC_LA33_P | IO_L4P_T0_13 | W29 | FMC reference 33rd channel data P |
| FMC_LA33_N | IO_L4N_T0_13 | Y29 | FMC reference 33rd channel data N |
| FMC_SCL | IO_L20P_T3_17 | A16 | FMC I2C Bus Clock |
| FMC_SDA | IO_L20N_T3_17 | A17 | FMC I2C Bus Data |

# Part 14: Expansion Header

The AX7325B FPGA development board is reserved with one 0.1inch spacing standard 40-pin expansion headers J2, which is used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel3.3 V power supply,3-channle ground and 34 IOs. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

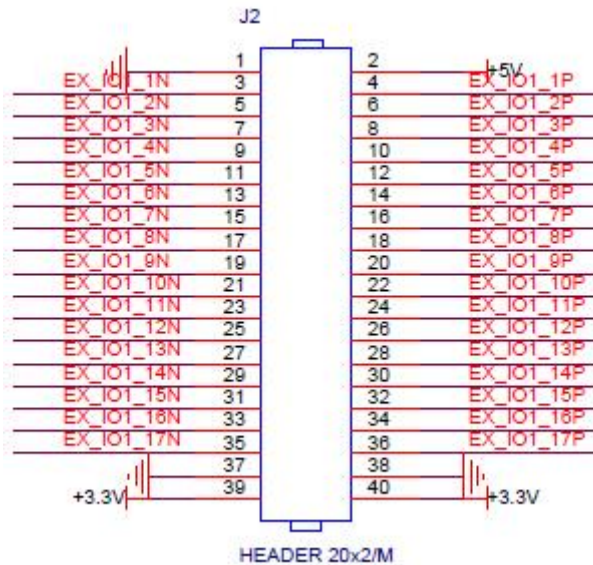The circuit of the expansion port (J2) is shown in Figure 14-1.

Figure 14-1: Expansion header J2 schematic



Figure 14-2: Expansion header J2 on the FPGA Board

## J16 Expansion Header Pin Assignment

| J16 Pin Number | FPGA Pin | J16 Pin Number | FPGA Pin |
|:---:|:---:|:---:|:---:|
| 1 | GND | 2 | +5V（Output） |
| 3 | J24 | 4 | J23 |
| 5 | J22 | 6 | J21 |
| 7 | J26 | 8 | K26 |
| 9 | K30 | 10 | L30 |
| 11 | L28 | 12 | M28 |
| 13 | M27 | 14 | N27 |
| 15 | N30 | 16 | N29 |
| 17 | L27 | 18 | L26 |
| 19 | J28 | 20 | J27 |
| 21 | H29 | 22 | J29 |

| 23 | K29 | 24 | K28 |
|----|-----|----|-----|
| 25 | L20 | 26 | M20 |
| 27 | K21 | 28 | L21 |
| 29 | L23 | 30 | L22 |
| 31 | K24 | 32 | K23 |
| 33 | K25 | 34 | L25 |
| 35 | M29 | 36 | M19 |
| 37 | GND | 38 | GND |
| 39 | +3.3V（Output） | 40 | +3.3V（Output） |

# Part 15: LED Light

There are five red LEDs on the AX7325B FPGA development board, one of which is the power indicator (PWR),one is configure indicator,fourare usersLED lights (LED1~LED4). When the AX7325B FPGA board is powered on, the power indicator will light up; whenthe AX7325B FPGA is configured, the configuration LED will light up; 4 user LEDs (LED1~LED4) are connected to the IO of the FPGA BANK17, the user can control the lighting and extinction through the program. When the IO voltage connected to the user LED is configured low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be extinguished.Because the level of BANK17 is 1.5V, here we have added a three-stage tube to drive the LED to light up.The LEDs hardware connection is shown in Figure 15-1.
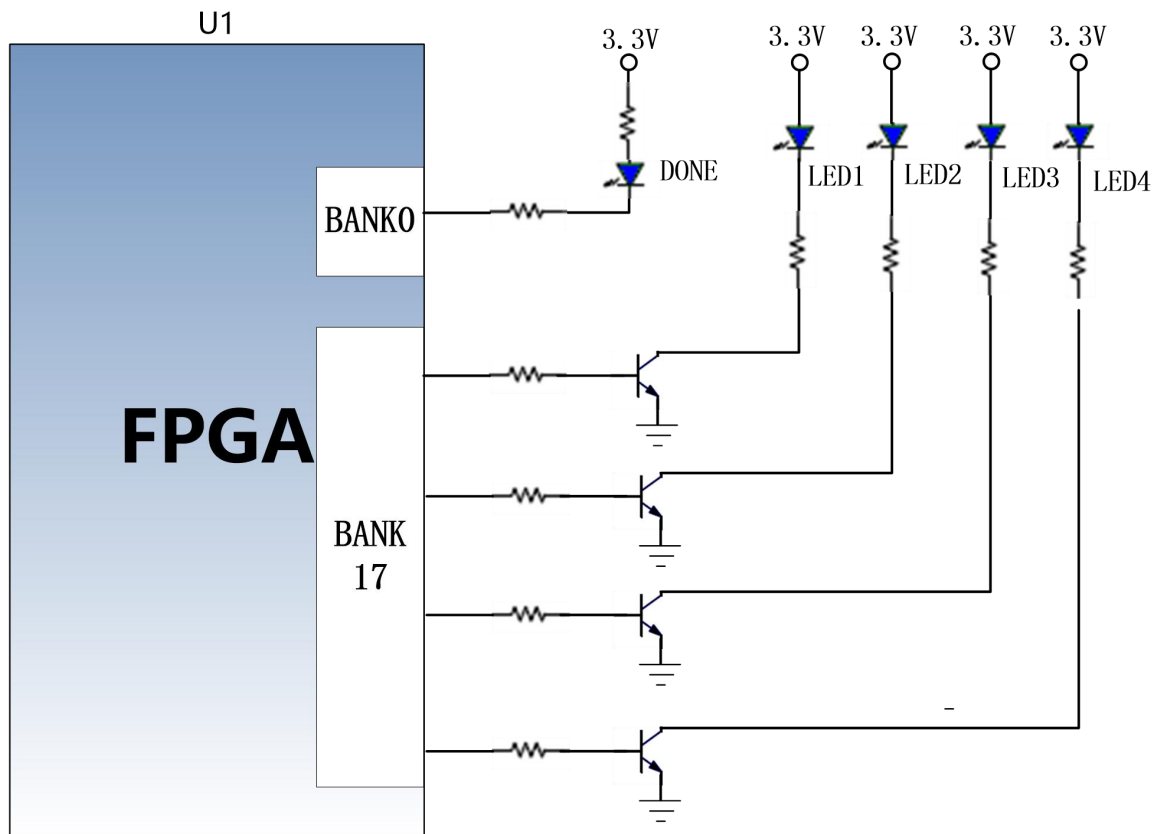
Figure 15-1: The LED lights hardware connection diagram



Figure 15-2: The User LEDs on theFPGA Board

## Pin assignment of user LED lights

| Signal Name | FPGA Pin | FPGA Pin Number | Description |
|:---:|:---:|:---:|:---:|
| LED1 | IO_L23N_T3_17 | A22 | User LED1 |
| LED2 | IO_L24P_T3_17 | C19 | User LED2 |
| LED3 | IO_L24N_T3_17 | B19 | User LED3 |

| LED4 | IO_25_17 | E18 | User LED4 |

# Part16: User Buttons

The AX7325B FPGA development board contains two user buttons KEY1~KEY2. The button is active low. The circuit of user button part is shown in Figure 16-1.
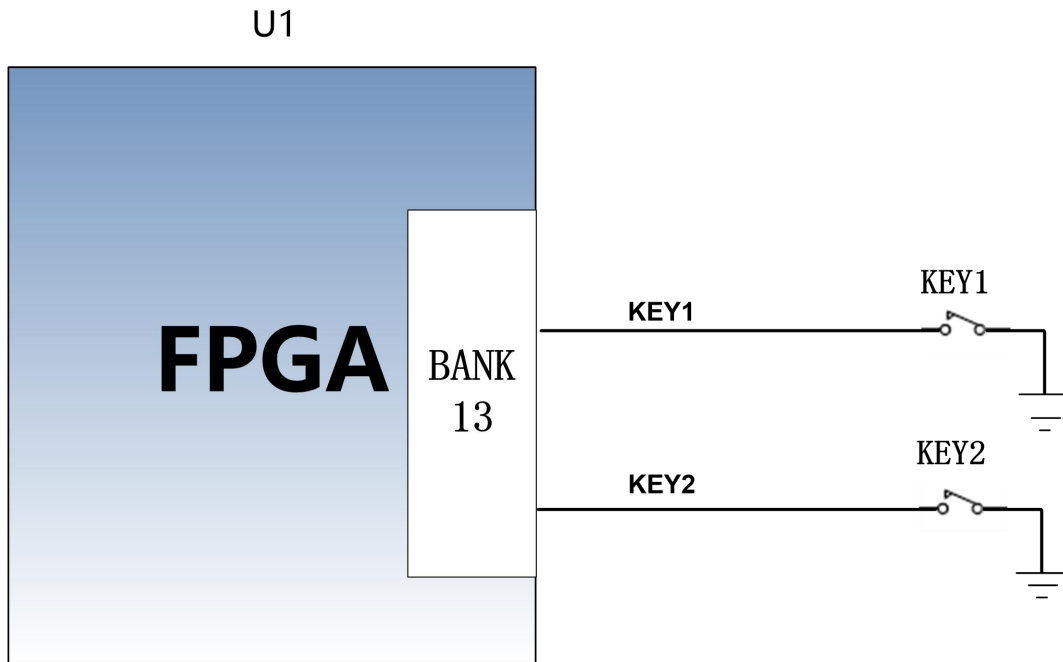


Figure 16-1: User ButtonsSchematic



Figure 16-2: User Buttons on the FPGA Board

## UseButtons Pin Assignment

| Signal Name | FPGA Pin | FPGA Pin Number | Description |
|---|---|---|---|
| KEY1 | IO_L21P_T3_DQS_13 | AG27 | User Buttons KEY1 Input |

| KEY2 | IO_L21N_T3_DQS_13 | AG28 | User Buttons KEY2 Input |
|------|-------------------|------|-------------------------|

# Part 17: JTAG Interface

A JTAG interface is reserved JTAG interface one the AX7325B FPGAdevelopment board for downloading FPGA programs or firmware to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA to avoid damage of the FPGA chip.
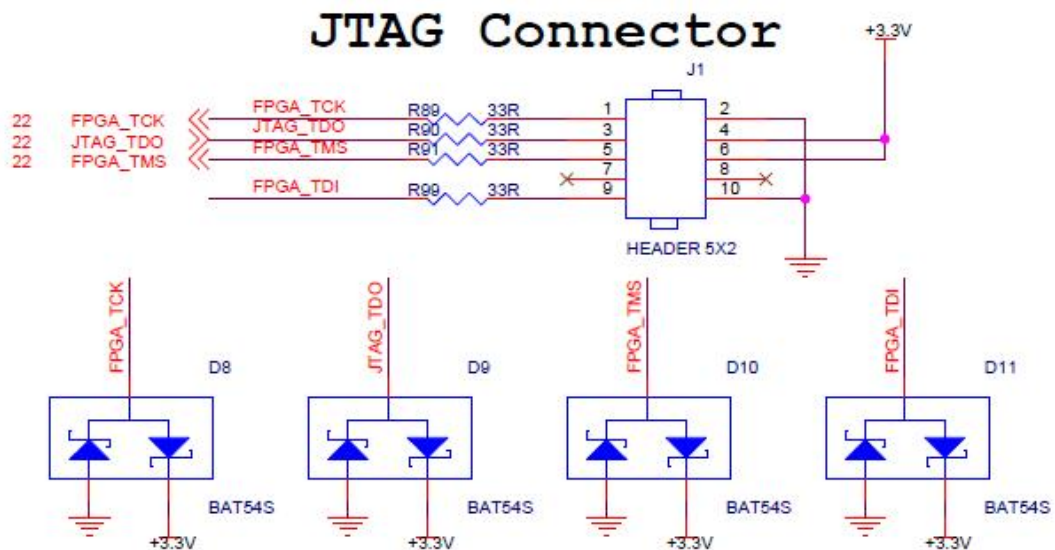


Figure 17-1: JTAG Interface Schematic

The Figure 17-2 detailed the JTAG interface on the AX7325B FPGA development board. Users can connect the PC and JTAG interface to debug the FPGA through the USB downloader provided by us. Be careful not to hot swap when JTAG cable is plugged and unplugged.

Figure 17-2: JTAG Interface on the FPGA board

# Part 18: Power Supply

The power input voltage of the AX7325B FPGA development board is DC12V, and the external +12V power supply supplies power to the FPGA development board. The power supply DC12V is converted into 1.0V for FPGA Core power, which output current is up to 20A, meets the current demand of the core voltage of the FPGA

In addition, + 12V generates + 1.5V and MGTAVCC power through the DC / DC power chip ETA8156FT2G, and generates other power through the DCDC chip ETA1471FT2G.

The VTT and VREF voltages of DDR3 and SODIMM are generated by the TPS51200 chip.

The Power supply design diagramis shown in Figure 18-1.
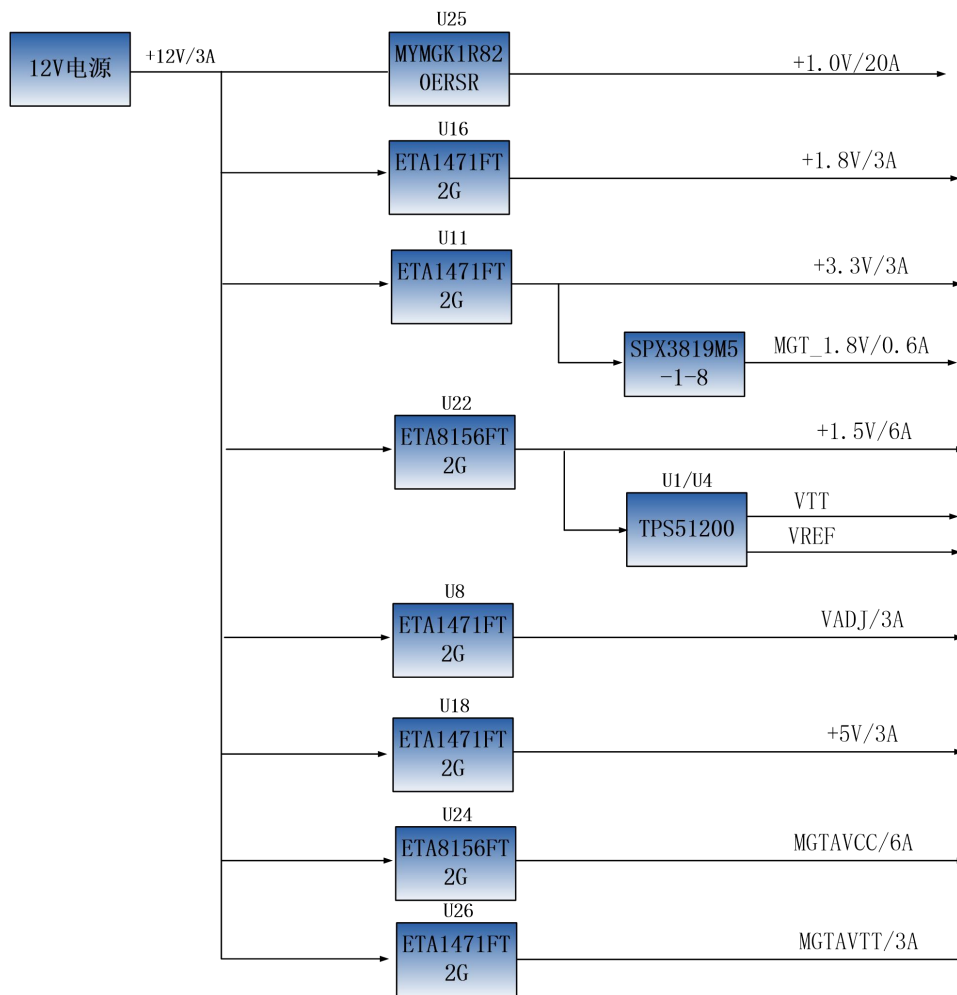
Figure 18-1: Power Supply Design Diagram

The functions of each power distribution are shown in the following table:

| Power Supply | Function |
|---|---|
| +1.0V | FPGA core voltage |
| +3.3V | FPGA Bank0,Bank14，Bank15，QSIP FLASH, Clock Crystal, SD Card, SFP Optical Module |
| +1.8V | Gigabit Ethernet, HDMI, USB |
| +1.5V | DDR3, SODIMM，FPGA Bank33,Bank34，Bank35 |
| VADJ(+2.5V) | FPGA Bank12, Bank13, FMC |

| VREF, VTT（+0.75V） | DDR3, SODIMM |
|---|---|
| MGTAVCC(+1.0V) | FPGA Bank115, Bank116, Bank117, Bank118 |
| MGTAVTT(+1.2V) | FPGA Bank115, Bank116, Bank117, Bank118 |
| MGT_1.8V (+1.2V) | FPGA GTX auxiliary voltage |

Because the power supply of the FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO) circuit design to ensure the normal operation of the chip.

# Part19: Fan

Because AX7325B FPGA development board generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the FPGAChip. The control pin is connected to the IO of the BANK13. If the IO level output is low, the MOSFET is turned on and the fan is working. If the IO level output is high, the fan stops. The fan design on the board is shown in Figure 19-1.
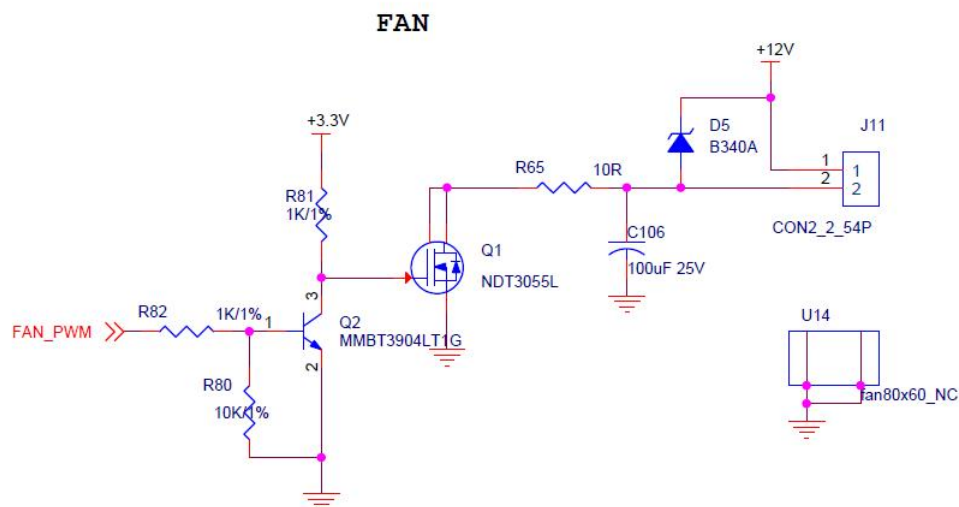


Figure 19-1：Fan design in the schematic

The fan has been screwed to the AX7325B FPGA development board before leaving the factory. The power of the fan is connected to the socket of J11. The red is positive and the black is negative.
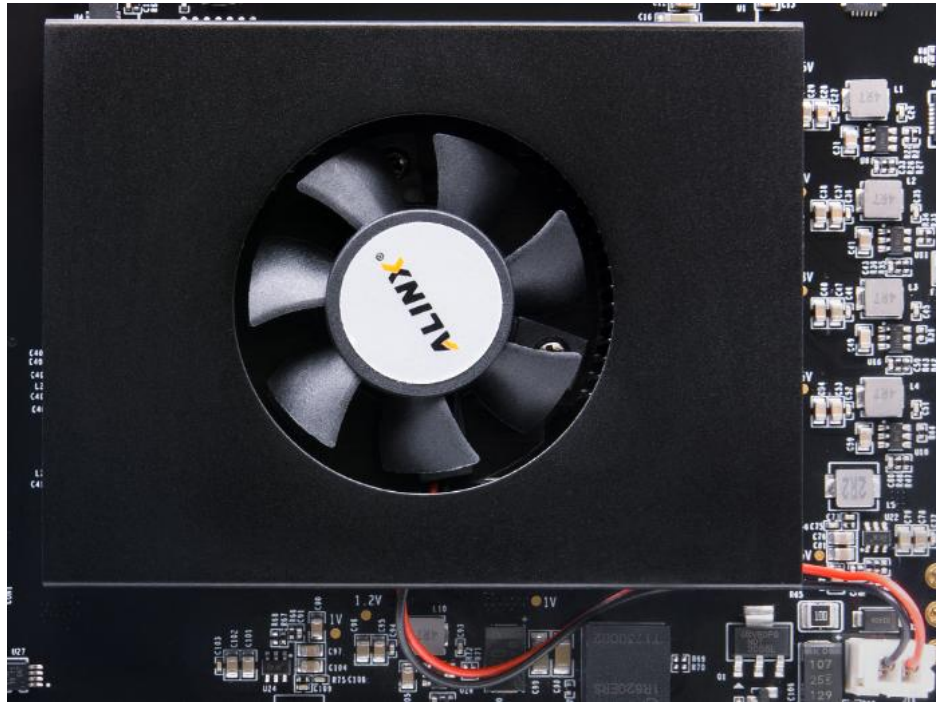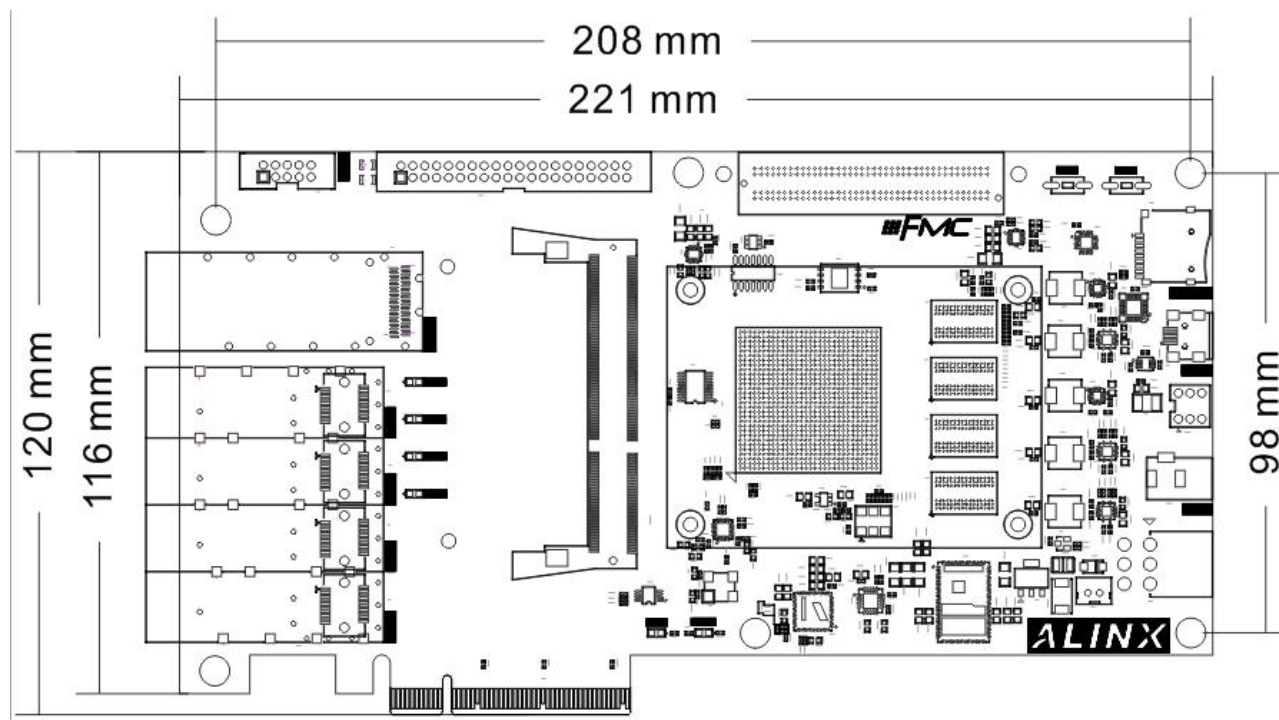


Figure 19-2：Fan on the FPGA Board

# Part 20: Structure Diagram



Figure 20-1: Structure Diagram (Top View)