ZYNQ UltraScale+ MPSOC ZU7EG/7EV/11EG SOM User Manual

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Part 1: SOM Introduction

Part 1.1: SOM Introduction

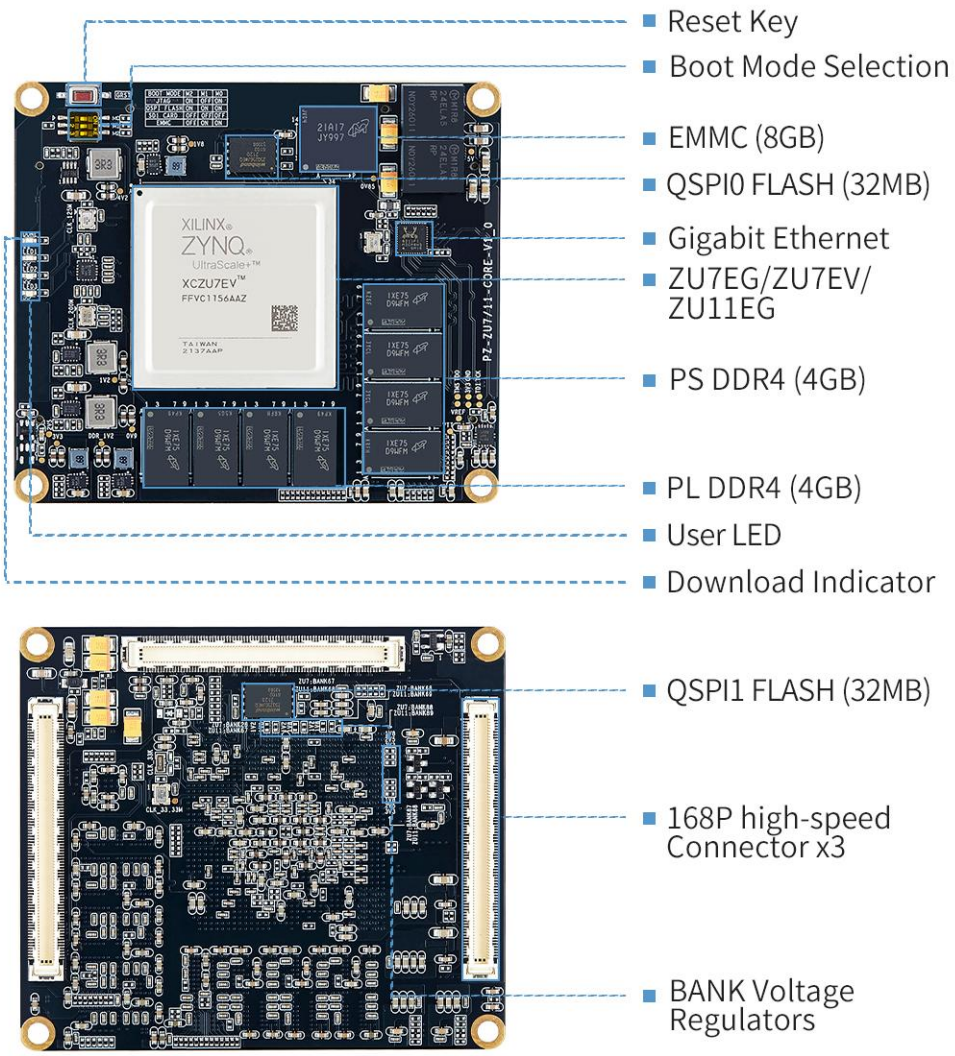
The ZU7EG/ZU7EV/11EG core board adopts the Zynq UltraScale+ XCZU7EG-2FFVC1156I / XCZU7EG-2FFVC1156I / XCZU11EG-2FFVC1156I chip of XILINX company as the main controller. The three core boards are fully compatible, but the FPGA chip is different. The core board is connected to the carrier board with three 0.5mm pitch 168P gold-plated high-speed connectors, and four 3.5mm fixing holes are placed on the four feet of the core board. This hole can be fastened with the carrier board by screws, which ensures stable operation in the environment of strong vibration.

Part 1.2: SOM Specification

ZU7EG/ZU7EV/11EG Industrial Grade SOM Specification			
FPGA CHIP	XCZU7EG-2FFVC1156I	XCZU7EV-2FFVC1156I	XCZU11EG-2FFVC1156I
Processor Core	ARM : 4 x Cortex-A53 1.3Ghz RPU : 2 x Cortex-R5 533Mhz GPU : Mali-400MP2 667Mhz		
logic cells	504K	504K	653K
Lookup Tables (LUTs))	230K	230K	299K
Flip-Flops	461K	461K	597K
Block RAM	11Mb	11Mb	21.1Mb
Ultra RAM	27Mb	27Mb	22.5Mb
DSP Slices	1728	1728	2928
Video Codec	-	H.264 / H.265	-
DDR4/DDR4L	PS-side 4GB 2400Mhz*64bit / PL-side 2GB 2400Mhz*32bit		
QSPI FLASH	2 channels (QSP0+QSPI1), single chip 32MB, total 64MB		
EMMC	8GB, to store startup files and user files		
Start-up Mode	JTAG/QSPI/SD/EMMC, onboard DIP switch selection		
Gigabit Ethernet	1（PS-side）		
User LEDs	3（PL-side, High Level light, Low Level off）		
Number of IOs	MIO: 38 (Fixed 1.8V Level) HP: 144 (1.2/1.8V Adjustable, 1.8V by default) HD: 48 (1.8/2.5/3.3V Adjustable, 3.3 V by default)		
Number of GTR/GTH Interfaces	4 pairs of TX/RX on PS side, 24 pairs of TX/RX on PL side		
Voltage/Current	8-12V/5A (Recommended Voltage 8V)		
Working Temperature	-40° C -- +85° C		
Technology	Immersion Gold Process, 168P Connectors X 3		
Connector Height	4mm		

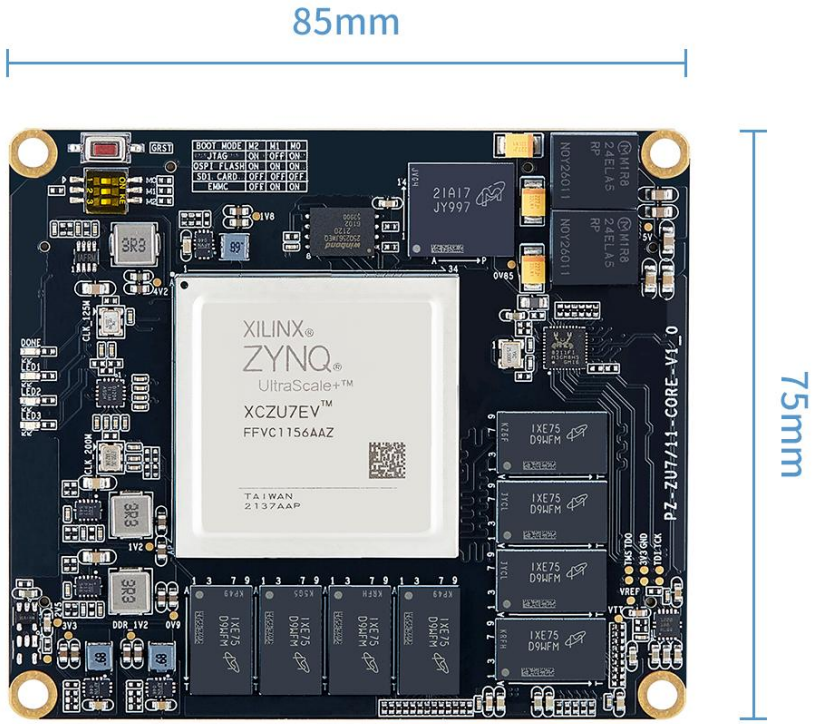
Part 1.3: Product Appearance

As shown in the figure below, the position of each main electronic component on the core board is marked, which is convenient for users to view and identify.



Part 1.4: SOM Form Factors

The Form Factors of the core board is 85 x 75mm. The core board is connected to the Carrier Board through three 0.5mm/168P gold-plated high-speed connectors on the carrier board, with a combined height of 4mm. The following figure shows the dimensions of the core board.


85mm
75mm
XILINX
ZYNQ
UltraScale+
XCZU7EV
FFVC1156AAZ
PZ-ZU7/11-CORE-V1_0

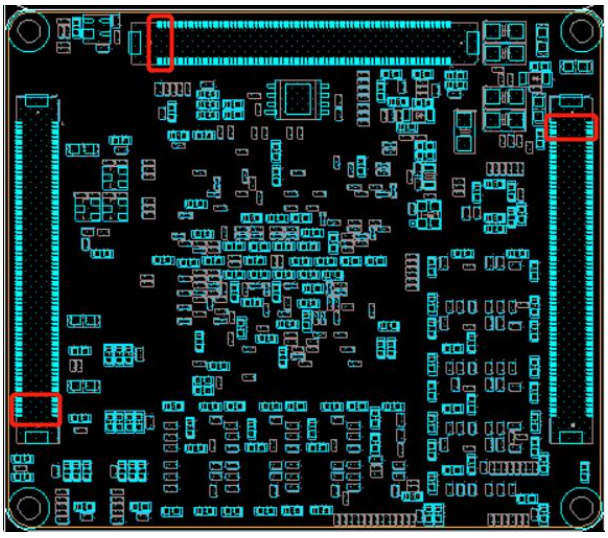

Top MAX Height 3mm
PCB Thickness 1.6mm
Connector Height 3mm

Part 2: SOM User Guide

Part 2.1: Power Connection

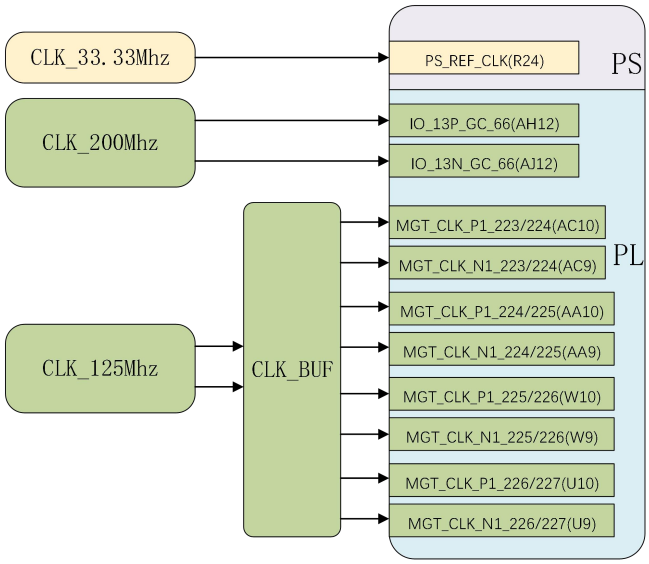
The power supply voltage of the core board is 8-12V, the recommended supply voltage is 8V, There are power input pins on the four corners of the core board. The power pins have been connected inside the module. In the design, you only need to connect the power pin on one corner, and the core board can work. The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two vias. The limit current of the core board power supply is 5A/3A, so the external power supply needs to consider the limit current to ensure the stable operation of the core board.

The output voltage of the power supply to the module needs to be stable. Add a first-level DCDC power conversion to the module power input, from high voltage to 5V, and the DCDC current output capacity can be about 5A. For example, you can refer to the power chip TPS56628. Two **220uF/25V** capacitors should be placed at the power input of the module to ensure power quality. If the DCDC switching frequency used is relatively low, the capacitor tolerance needs to be increased to ensure power supply stability.



Part 2.2: Clock

The core board provides a 33.333Mhz clock input for the PS side, and the input pin position is PS_REF_CLK; it provides a 200Mhz differential clock input for the PL side. The clock input pins on the PL side is IO_13P_GC_66/IO_13N_GC_66, and the pin position is AH12/AJ12; provides a 125Mhz differential clock input for the GTX on the PL side. After the 125M input is converted into four 125M clock outputs through the clock buffer, they are respectively connected to the corresponding positions as shown in the figure.



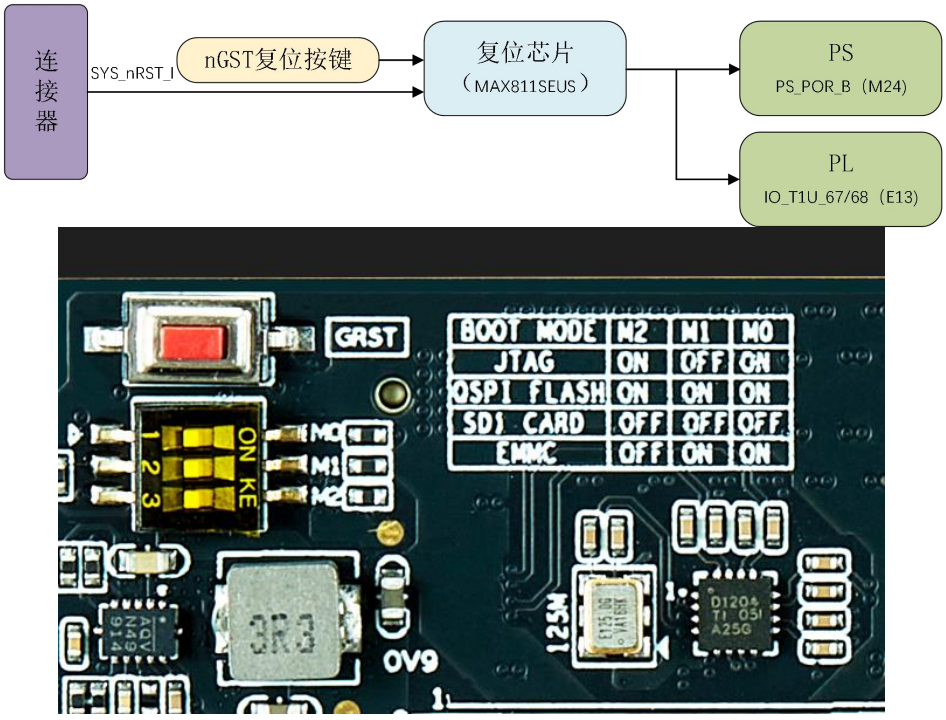
Part 2.3: Global Reset

The core board provides the "**nGST**" reset key, which is a system reset key and is active at low level. This pin is also drawn to the connector, and the signal name is "**SYS_nRST_I**", which is convenient for adding a reset key externally or designing a watchdog reset circuit. At the same time, in order to stabilize the system, we added a reset chip MAX811SEUS to the core board. This signal can be used for the reset of other peripherals on the core board. The signal level is 3.3V. The reset pin is a shared reset for PS/PL, which is connected to the PS_POR_B(M24) pin on the PS side and the IO_T1U_67/68(E13) pin of the BANK67(ZU7) or BANK68(ZU11) on the PL side.

If the reset circuit needs to be designed on the carrier board, the

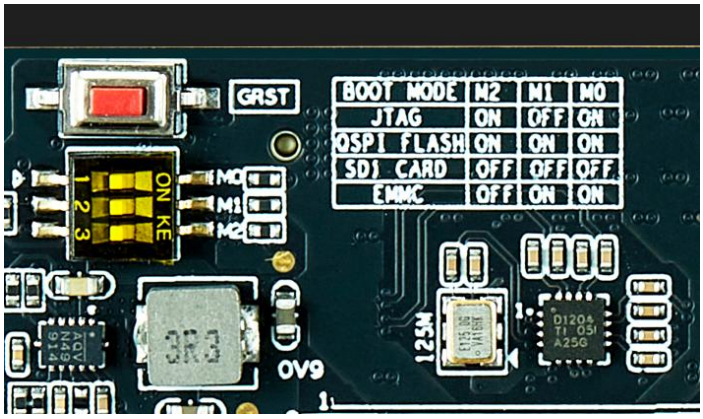
following situations need to be considered.

1) The reset circuit board is used internally, only need to add a reset key and a 10uF capacitor parallel port to the ground.
2) The reset circuit needs to be reserved on the structure for external use. It is necessary to add a key to the ground, and at the same time, connect a 10uF capacitor and a TVS anti-static device to the ground in parallel.



Part 2.4: Boot Mode Selection

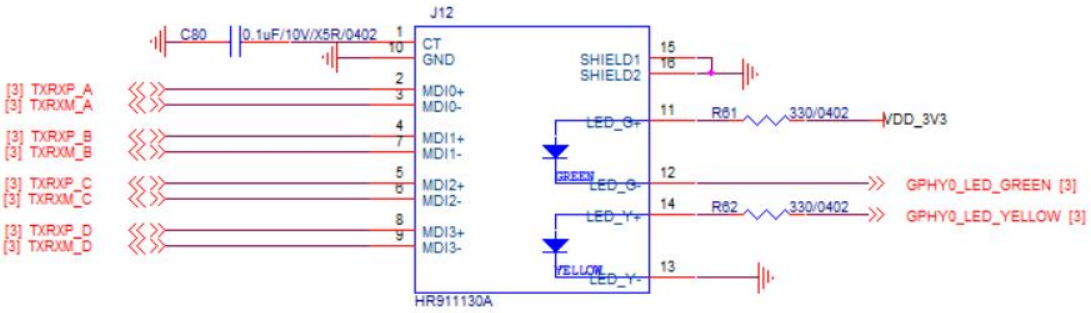
The core board supports four boot modes, namely JTAG, QSPI Flash, EMMC, and SD card. The first three startup methods are installed on the core board, and users can realize the SD card method by connecting with the carrier board. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch. Because the main chip generates a large amount of heat, a heat sink needs to be added on the core board, which will block the BOOT MODE selection table.



Part 2.5: Gigabit Ethernet Chip

The Gigabit Ethernet chip RTL8211FI-CG is placed on the core board. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below. Ethernet external connection only needs an RJ45 with a transformer to use, the chip address PHY_AD[2:0]=001, Please refer to the figure below for the connection schematic diagram (the product circuit needs to be equipped with an ESD protection circuit). In addition, in actual product applications, C80 needs to use high withstand voltage capacitors, such as 0.1uF/2KV.

RMGII Signal	Pin Name	Pin Position
GTX_CLK	MIO26_501	A29
TXD0	MIO27_501	A30
TXD1	MIO28_501	A31
TXD2	MIO29_501	A32
TXD3	MIO30_501	A33
TX_EN	MIO31_501	B30
RX_CLK	MIO32_501	B31
RXD0	MIO33_501	B33
RXD1	MIO34_501	B34
RXD2	MIO35_501	C31
RXD3	MIO36_501	C32
RX_CTL	MIO37_501	C33
MDC	MIO76_502	L33
MDIO	MIO77_502	L34



Part 2.6: EMMC Pin Definition

The capacity of the onboard EMMC is 8GB, and the working temperature is -40 ° C--+85 ° C. The pins are defined in the following table.

EMMC Pin	Pin Name	Pin Position
EMMC_D0	MIO13	AK17
EMMC_D1	MIO14	AL16
EMMC_D2	MIO15	AN16
EMMC_D3	MIO16	AM16
EMMC_D4	MIO17	AP16
EMMC_D5	MIO18	AE18
EMMC_D6	MIO19	AL17
EMMC_D7	MIO20	AD18
EMMC_CLK	MIO22	AD20
EMMC_CMD	MIO21	AF18
EMMC_nRST	MIO23	AD19

Part 2.7: QSPI FLASH

The core board is designed with two channels of QSPI FLASH, with a single chip capacity of 32MB and a total of 64MB. Users can define it as QSPI X8 to speed up startup and reduce startup time. QSPI FLASH can be used to store startup files and user files.

QSPI0 FLASH Pin	Pin Name	Pin Position
DATA0	MIO4	A25
DATA1	MIO1	C24
DATA2	MIO2	B24
DATA3	MIO3	E25
QSPI_CS	MIO5	D25
QSPI_CLK	MIO0	A24

QSPI1 FLASH Pin	Pin Name	Pin Position
DATA0	MIO8	D26
DATA1	MIO9	C26
DATA2	MIO10	F26
DATA3	MIO11	B26
QSPI_CS	MIO7	B25
QSPI_CLK	MIO12	C27

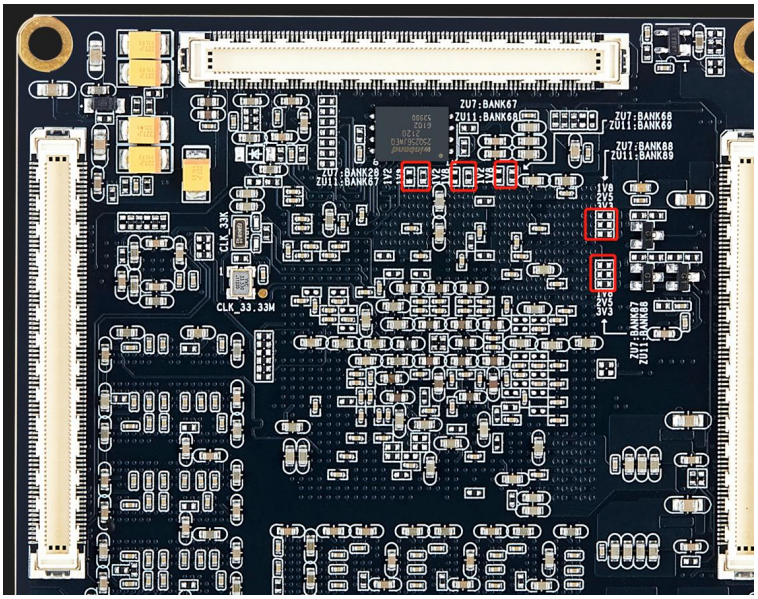
Part 2.8: On-board LED

In order to facilitate debugging, three LEDs are placed on the core board, and the LEDs are connected to the BANK68(ZU7) or BANK69(ZU11) of PL side. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and the low level LED goes out.

Number	Pin Name	Pin Position
LED1	IO-T3U-68/69	A9
LED2	IO-T2U-68/69	G13
LED3	IO-T1U-68/69	D7

Part 2.9: BANK Interface Level Selection

BANK28(ZU7)/BANK67(ZU11), BANK67(ZU7)/BANK68(ZU11), BANK68(ZU7)/BANK69(ZU11) on the core board are HP BANKs The interface level configuration is 1.2/1.8V, and the voltage can be adjusted by selecting and welding a 0 ohm resistor through the instructions provided on the board. The default level is 1.8V. BANK87 (ZU7)/BANK88 (ZU11), BANK88 (ZU7)/BANK89 (ZU11) are HD BANKs, and the BANK level can realize 1.8V/2.5V/3.3V three level conversions, just change the position of the resistor, the default voltage Flat is 3.3V.



Part 2.10: PS-side DDR

The PS side is equipped with four industrial-grade DDR4 chips with a single capacity of 1GB and a total capacity of 4GB. The model is MT40A512M16LY-062E. The DDR4 pin assignment can directly call the system assignment. You can also refer to the routines provided by our company.

Part 2.11: PL-side DDR

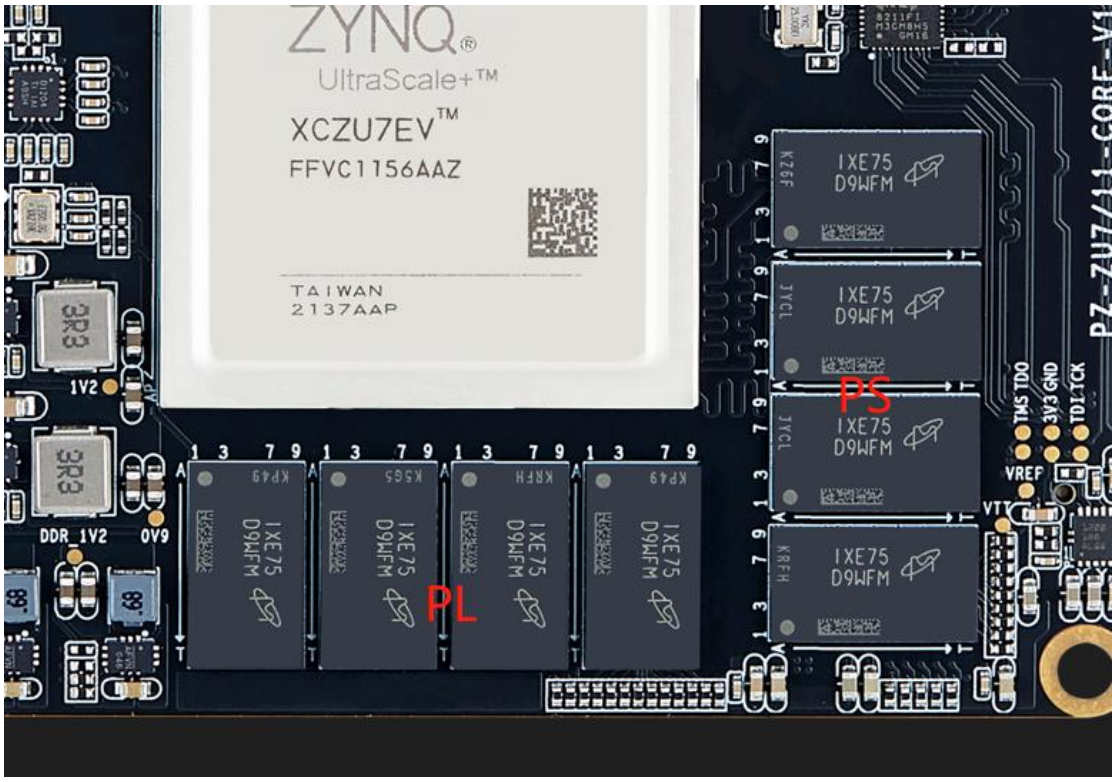
The PL side is equipped with Four industrial-grade DDR4 chips with a single capacity of 1GB, the model is MT40A512M16LY-062E, and the DDR4 pin assignment is shown in the table below.

DDR4 Pin	Pin Name	Pin Position
DDR4_D0	IO-L2P-64	AN13
DDR4_D1	IO-L6P-64	AN17
DDR4_D2	IO-L5N-64	AP15
DDR4_D3	IO-L5P-64	AP16
DDR4_D4	IO-L2N-64	AP13
DDR4_D5	IO-L3N-64	AN18
DDR4_D6	IO-L6N-64	AN16
DDR4_D7	IO-L3P-64	AM18
DDR4_DM0	IO-L1P-64	AP18
DDR4_DQS_P0	IO-L4P-64	AM14
DDR4_DQS_N0	IO-L4N-64	AN14

DDR4_D8	IO-L8N-64	AL15
DDR4_D9	IO-L11N-64	AK17
DDR4_D10	IO-L8P-64	AL16
DDR4_D11	IO-L9P-64	AK18
DDR4_D12	IO-L12N-64	AJ15
DDR4_D13	IO-L12P-64	AJ16
DDR4_D14	IO-L9N-64	AL18
DDR4_D15	IO-L11P-64	AJ17
DDR4_DM1	IO-L7P-64	AM16
DDR4_DQS_P1	IO-L10P-64	AK15
DDR4_DQS_N1	IO-L10N-64	AK14
DDR4_D16	IO-L18P-64	AG15
DDR4_D17	IO-L14P-64	AF18
DDR4_D18	IO-L17P-64	AF16
DDR4_D19	IO-L15N-64	AF17
DDR4_D20	IO-L17N-64	AF15
DDR4_D21	IO-L14N-64	AG18
DDR4_D22	IO-L18N-64	AG14
DDR4_D23	IO-L15P-64	AE17
DDR4_DM2	IO-L13P-64	AH18
DDR4_DQS_P2	IO-L16P-64	AH14
DDR4_DQS_N2	IO-L16N-64	AJ14
DDR4_D24	IO-L23N-64	AB14
DDR4_D25	IO-L24N-64	AD16
DDR4_D26	IO-L21N-64	AB15
DDR4_D27	IO-L24P-64	AD17
DDR4_D28	IO-L23P-64	AA14
DDR4_D29	IO-L20P-64	AC17
DDR4_D30	IO-L21P-64	AB16
DDR4_D31	IO-L20N-64	AC16
DDR4_DM3	IO-L19P-64	AD15
DDR4_DQS_P3	IO-L22P-64	AA16
DDR4_DQS_N3	IO-L22N-64	AA15
DDR4_D32	IO-L3P-65	AP21
DDR4_D33	IO-L5P-65	AN22
DDR4_D34	IO-L3N-65	AP22
DDR4_D35	IO-L5N-65	AP23
DDR4_D36	IO-L2N-65	AN19
DDR4_D37	IO-L6P-65	AM23
DDR4_D38	IO-L2P-65	AM19
DDR4_D39	IO-L6N-65	AN23
DDR4_DM4	IO-L1P-65	AP19
DDR4_DQS_P4	IO-L4P-65	AM21
DDR4_DQS_N4	IO-L4N-65	AN21
DDR4_D40	IO-L9P-65	AJ19
DDR4_D41	IO-L11P-65	AJ20
DDR4_D42	IO-L11N-65	AK20
DDR4_D43	IO-L8N-65	AL23
DDR4_D44	IO-L9N-65	AK19
DDR4_D45	IO-L12N-65	AJ22
DDR4_D46	IO-L8P-65	AL22
DDR4_D47	IO-L12P-65	AJ21
DDR4_DM5	IO-L7P-65	AL20

DDR4_DQS_P5	IO-L10P-65	AK22
DDR4_DQS_N5	IO-L10P-65	AK23
DDR4_D48	IO-L15N-65	AG20
DDR4_D49	IO-L17N-65	AF22
DDR4_D50	IO-L14N-65	AH21
DDR4_D51	IO-L14P-65	AG21
DDR4_D52	IO-L15P-65	AG19
DDR4_D53	IO-L18P-65	AE23
DDR4_D54	IO-L17P-65	AF21
DDR4_D55	IO-L18N-65	AE24
DDR4_DM6	IO-L13P-65	AH22
DDR4_DQS_P6	IO-L16P-65	AF23
DDR4_DQS_N6	IO-L16N-65	AG23
DDR4_D56	IO-L21P-65	AD20
DDR4_D57	IO-L20P-65	AB19
DDR4_D58	IO-L21N-65	AE20
DDR4_D59	IO-L20N-65	AC19
DDR4_D60	IO-L23P-65	AC18
DDR4_D61	IO-L24N-65	AA20
DDR4_D62	IO-L23N-65	AD19
DDR4_D63	IO-L24P-65	AA19
DDR4_DM7	IO-L19P-65	AE18
DDR4_DQS_P7	IO-L22P-65	AA18
DDR4_DQS_N7	IO-L22N-65	AB18
DDR4_A0	IO-L17P-66	AG11
DDR4_A1	IO-L21N-66	AF13
DDR4_A2	IO-L11P-66	AJ10
DDR4_A3	IO-L20N-66	AE14
DDR4_A4	IO-L18N-66	AG8
DDR4_A5	IO-L21P-66	AE13
DDR4_A6	IO-L18P-66	AF8
DDR4_A7	IO-L15P-66	AG13
DDR4_A8	IO-L10N-66	AL8
DDR4_A9	IO-L15N-66	AH13
DDR4_A10	IO-L17N-66	AG10
DDR4_A11	IO-L10P-66	AK8
DDR4_A12	IO-L16N-66	AH9
DDR4_A13	IO-L11N-66	AK10
DDR4_A14	IO-L22N-66	AD12
DDR4_A15	IO-L16P-66	AG9
DDR4_A16	IO-L12P-66	AJ9
DDR4_A17	IO-L12N-66	AK9
DDR4_BA0	IO-L23N-66	AF12
DDR4_BA1	IO-L9N-66	AL12
DDR4_BG0	IO-L23P-66	AE12
DDR4_nCS	IO-L8N-66	AL10
DDR4_nACT	IO-L22P-66	AC12
DDR4_ODT	IO-L20P-66	AD14
DDR4_RESET	IO-L19N-66	AF10
DDR4_CLK_P	IO-L14P-66	AH11
DDR4_CLK_N	IO-L14N-66	AJ11
DDR4_CKE	IO-L8P-66	AL11
DDR4_TEN	IO-L9P-66	AK12

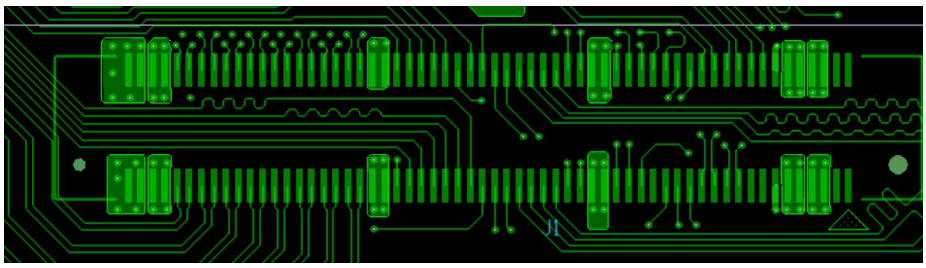
DDR4_PARITY	IO-L19P-66	AF11
DDR4_nALERT	IO-L7N-66	AL13



Part 3: Carrier Board Design

Part 3.1: PCB Design of Power Supply

The power input needs to be connected with copper skin, and enough vias are made to ensure the current carrying capacity, but the power supply voltage is high and the interference is large. Under the condition of ensuring the current flow, do not make the copper skin larger, so as not to interfere with other signals. The ground pins need to be connected to the ground plane, and one ground pin needs to be punched with two vias to ensure flow and sufficient connection.



Part 3.2: High-speed interface layout and routing

1) USB Interface

The parallel port rate of the USB PHY chip is 60Mhz, and the parallel port traces need to be equal in length and not greater than 1000mil (25.4mm), so the PHY should be placed as close to the module as possible, and the USB differential line DP/DM can be pulled longer.

2) Gigabit Ethernet

The signal connected to the RJ45 end needs to keep the same length, and the TX part and the RX part of the RGMII interface need to keep the same length separately.

3) HDMI Interface

The HDMI interface signal needs to be differential, and the same length control must be maintained between the differentials.

Part 3.3: LVDS Signal

The BANK level of the core board can be selected between three levels of 1.2/1.8V/2.5V/3.3V, the default is 3.3V level, if you need to work in LVDS mode, you need to adjust the interface level to 1.8V or 2.5V. At the same time, the LVDS signal traces on the carrier board need to be processed by differential/impedance control, and the lengths between the differentials should be kept the same.

Part 3.4: GTX Signal Routing

There are many issues that need to be considered in GTX wiring. For users who have questions, contact customer service to access technical support.

Part 3.5: Product Protection

For product design, it is necessary to add protective circuits to various interfaces. It needs to be designed according to the requirements of the protection level.

Part 4: SOM Core Board Pins and Signal Isometric

Part 4.1: SOM Core Board Pin Definition

The PZ-ZU7/11 core board has a total of 38 pins on the PS side and 192 pins on the PL side. Among the PL pins, there are 144 signal levels of 1.2/1.8V, 96 signals can be adjusted at three levels of 1.8/2.5/3.3V. For detailed pin definitions, see the folder "PZ-ZU7_11 SOM Core Board Pins and Equal Length".

Part 4.2: Signal Isometric

In order to facilitate the user to design the carrier board and the high-speed signal, we provide the trace length data on the J1-J3 connectors to facilitate the user to coordinate the carrier board design. For the detailed data table, please refer to the folder "PZ-ZU7_11 SOM Core Board Pins and Equal Length".