4-Channel Vehicle Video Acquisition/Integration Module

FL9295 User Manual

Rev 1.0

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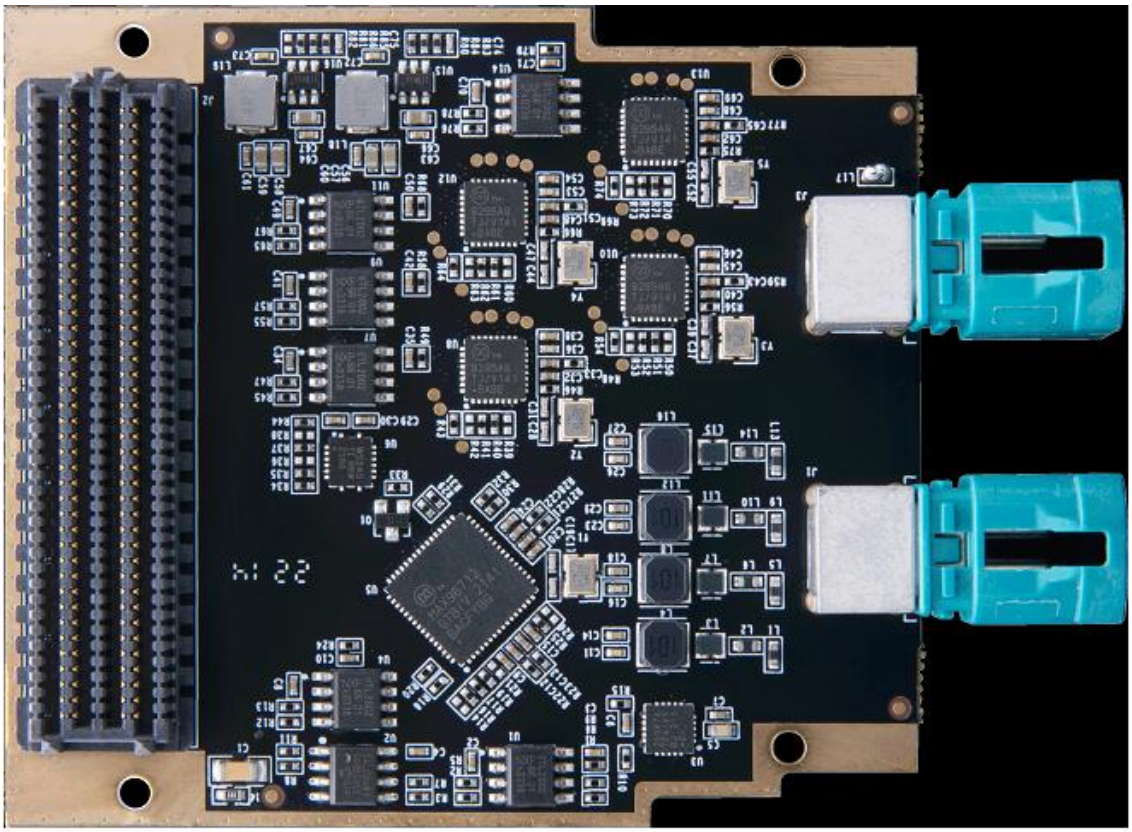
1. FL9295 Introduction

FL9295 is a 4-channel GMSL2 camera acquisition and video simulation injection module, which adopts one MAX96712 to realize 4-channel video decoding input and four MAX9295A to realize video coding output. The MAX96712 and MAX9295A chips are automotive-grade 4-channel serial decoder with serial speeds of 3Gbps and 6Gbps, supporting the first-generation GMSL1 and second-generation GMSL2 standards. The video interface uses a 4-in-1 FAKRA coaxial connector.

The 4-LANE MIPI signals of the MAX96712 and MAX9295A are connected to the ALINX FPGA development board through the FMC interface to achieve video image conversion and transmission, with each LANE supporting up to 2.5Gbps. The FMC interface is a standard LPC interface that meets the VITA 57.1 standard. The connector model of the FMC is ASP_134604_01.

The photo of FL9295 module is as follows:



FL9295 Module

1.1 Parameter Description of FL9295 Module

- Support 4-channel GMSL1/2 camera input and output

  Input: Support 4-channel camera, up to 8MP 30-frame resolution camera.

  Output: Support 4-channel video output, support 2MP/4MP 60 frames, or 8MP 30 frames.

- Cable Length

  Up to 40m (3Gbps) in GMSL1 mode;

  Up to 20 meters (6Gbps) in GMSL2 mode;

- AG connector

  Use Amphenol Z Code FAKRA AG coaxial connectors

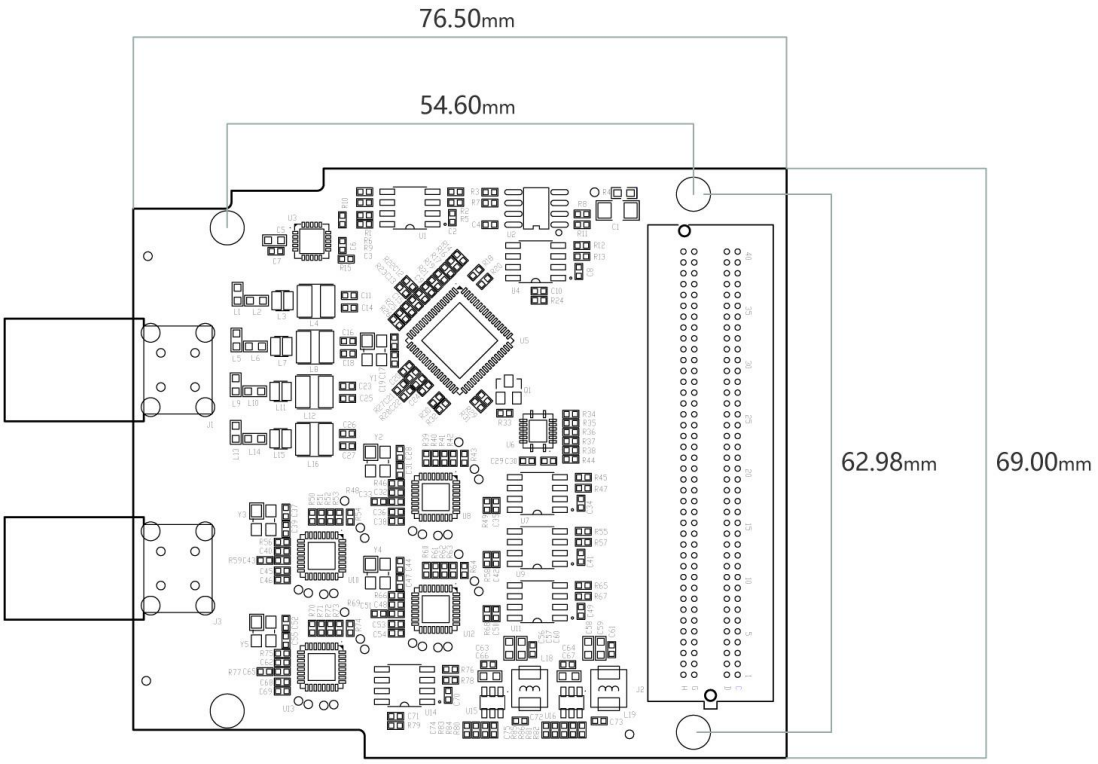
- Input and output image format

  It supports RAW8/10/12/14/16/20, RGB565/666/888, YUV422 8/10bit video image formats and can be configured using I2C

- FMC Interface

  Standard LPC connector

1.2 Structure Diagram of FL9295 Module

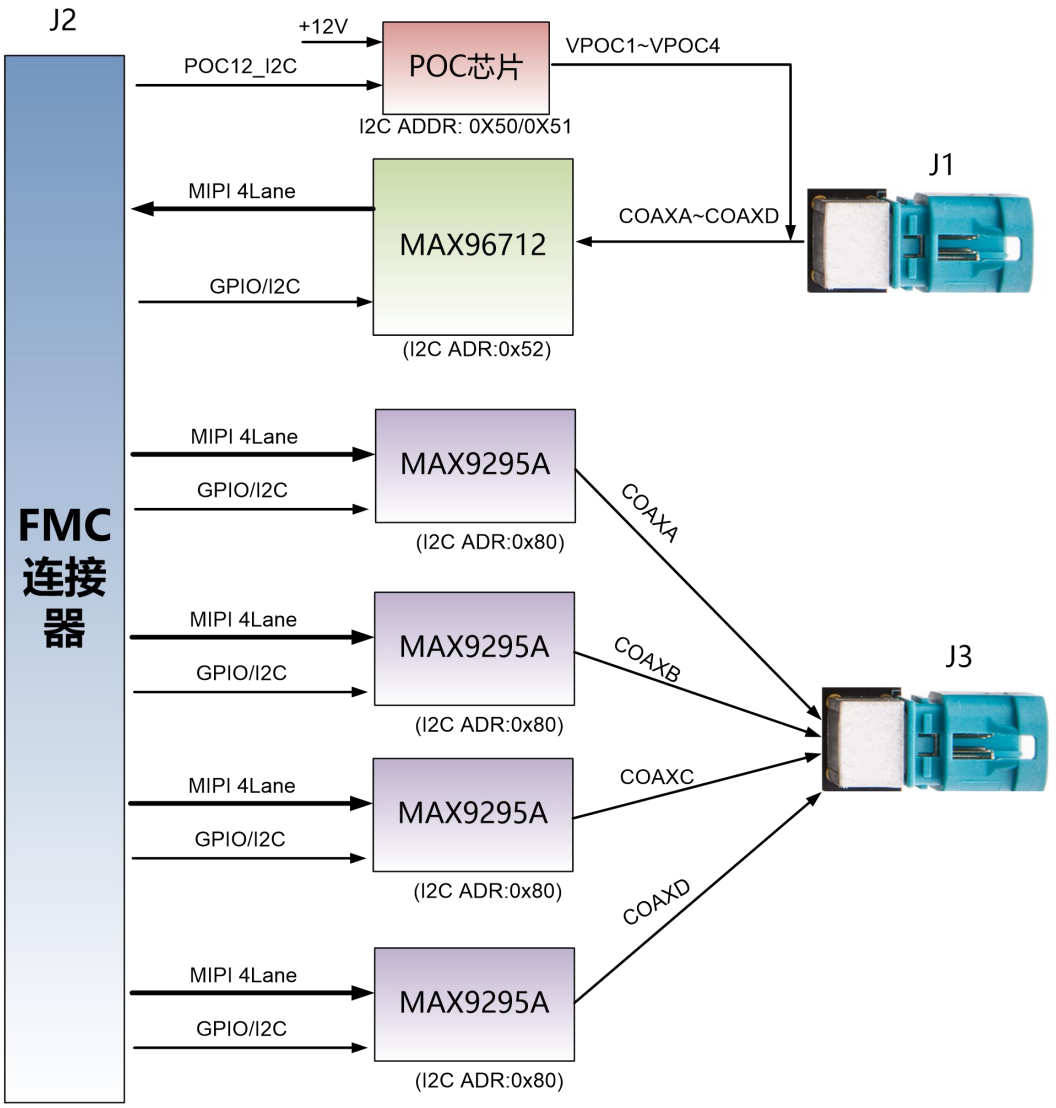


FL9295 Structure Diagram

2. Functions of Module FL9295

2.1 Schematic diagram of the module FL9295

The schematic design diagram of the module FL9295 is as follows:



Design diagram of video input and output

2.2 Pin assignment of Module FMC LPC

Only the signals are listed below, and the power and GND signals are not listed. The following figure is the pin assignment of FL9295 and Z7-P development board.

FMC Pin No.	Signal Name	FPGA Pin No.	Description
C22	G1_CKBP	AH18	1st-channel video output MIPI clock P
C23	G1_CKBN	AH17	1st-channel video output MIPI clock N
H28	G1_DB0P	AH14	1st-channel video output MIPI data 0P
H29	G1_DB0N	AJ14	1st-channel video output MIPI data 0N
H31	G1_DB1P	AF16	1st-channel video output MIPI data 1P
H32	G1_DB1N	AF15	1st-channel video output MIPI data 1N
D20	G1_DB2P	AF18	1st-channel video output MIPI data 2P

D21	G1_DB2N	AG18	1st-channel video output MIPI data 2N
G21	G1_DB3P	AE17	1st-channel video output MIPI data 3P
G22	G1_DB3N	AF17	1st-channel video output MIPI data 3N
D26	G2_CKBP	AP18	2nd-channel video output MIPI clock P
D27	G2_CKBN	AP17	2nd-channel video output MIPI clock N
H25	G2_DB0P	AP16	2nd-channel video output MIPI data 0P
H26	G2_DB0N	AP15	2nd-channel video output MIPI data 0N
C26	G2_DB1P	AN13	2nd-channel video output MIPI data 1P
C27	G2_DB1N	AP13	2nd-channel video output MIPI data 1N
G24	G2_DB2P	AM14	2nd-channel video output MIPI data 2P
G25	G2_DB2N	AN14	2nd-channel video output MIPI data 2N
D23	G2_DB3P	AM18	2nd-channel video output MIPI data 3P
D24	G2_DB3N	AN18	2nd-channel video output MIPI data 3N
C18	G3_CKBP	AE18	3rd-channel video output MIPI clock P
C19	G3_CKBN	AE19	3rd-channel video output MIPI clock N
G18	G3_DB0P	AC18	3rd-channel video output MIPI data 0P
G19	G3_DB0N	AD19	3rd-channel video output MIPI data 0N
H19	G3_DB1P	AA18	3rd-channel video output MIPI data 1P
H20	G3_DB1N	AB18	3rd-channel video output MIPI data 1N
H16	G3_DB2P	AB19	3rd-channel video output MIPI data 2P
H17	G3_DB2N	AC19	3rd-channel video output MIPI data 2N
D17	G3_DB3P	AD20	3rd-channel video output MIPI data 3P
D18	G3_DB3N	AE20	3rd-channel video output MIPI data 3N
G15	G4_CKBP	AL20	4th-channel video output MIPI clock P
G16	G4_CKBN	AL21	4th-channel video output MIPI clock N
H13	G4_DB0P	AJ19	4th-channel video output MIPI data 0P
H14	G4_DB0N	AK19	4th-channel video output MIPI data 0N
D14	G4_DB1P	AK22	4th-channel video output MIPI data 1P
D15	G4_DB1N	AK23	4th-channel video output MIPI data 1N
G12	G4_DB2P	AJ20	4th-channel video output MIPI data 2P
G13	G4_DB2N	AK20	4th-channel video output MIPI data 2N
C10	G4_DB3P	AL22	4th-channel video output MIPI data 3P
C11	G4_DB3N	AL23	4th-channel video output MIPI data 3N
G30	G1_CKAP	AD15	Video input MIPI clock P
G31	G1_CKAN	AE15	Video input MIPI clock N
G33	G1_DA0P	AC17	Video input MIPI data 0P
G34	G1_DA0N	AC16	Video input MIPI data 0N
H34	G1_DA1P	AA16	Video input MIPI data 1P
H35	G1_DA1N	AA15	Video input MIPI data 1N
G36	G1_DA2P	AA14	Video input MIPI data 2P
G37	G1_DA2N	AB14	Video input MIPI data 2N
H37	G1_DA3P	AB16	Video input MIPI data 3P
H38	G1_DA3N	AB15	Video input MIPI data 3N

G10	GMSL1_SCL	AF22	1st-channel MAX9295A I2C clock
G9	GMSL1_SDA	AF21	1st-channel MAX9295A I2C data
D9	GMSL2_SCL	AH21	2nd-channel MAX9295A I2C clock
D8	GMSL2_SDA	AG21	2nd-channel MAX9295A I2C data
H8	GMSL3_SCL	AP23	3rd-channel MAX9295A I2C clock
H7	GMSL3_SDA	AN22	3rd-channel MAX9295A I2C data
G7	GMSL4_SCL	AJ22	4th-channel MAX9295A I2C clock
G6	GMSL4_SDA	AJ21	4th-channel MAX9295A I2C data
G28	96712_SCL	AK14	MAX96712 I2C clock
G27	96712_SDA	AK15	MAX96712 I2C data
C14	POC_SCL	AP19	I2C clock of POC power chip
C15	POC_SDA	AP20	I2C data of POC power chip
H11	G1_GPI0	AN21	MAX96712 input GPI0
H10	G1_GPI1	AM21	MAX96712 input GPI1
D11	G1_GPI2	AG19	MAX96712 input GPI2
D12	G1_GPI3	AG20	MAX96712 input GPI3
H22	G1_PWDNB	AM16	MAX96712 POWER DONW
C30	FMC_SCL	M10	I2C clock of FMC
C31	FMC_SDA	L10	I2C data of FMC

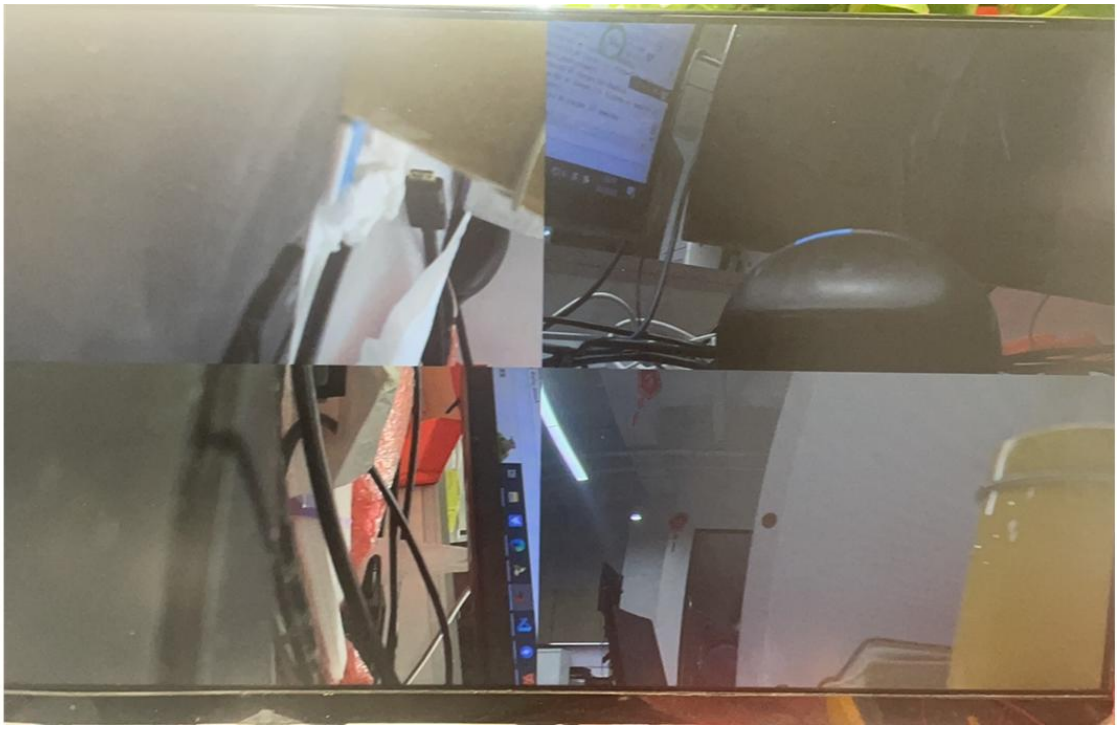
3. Installation of FMC Module

At present, FL9295 module can only be adapted to Z7-P and Z19-P development boards. The following is the installation diagram of FL9295 module and Z7-P.

Experiment 1

The FL9295 is connected to a 4-channel on-board camera (2 million), and the DP interface of the development board is connected to a 4K DP display.

The real-time display of images acquired by 4-channel video on the DP display:



Experiment 2

FL9295 video output and input loops, Z7-P connected to DP display.

The FPGA generates the test image, outputs it to the MAX9295A through MIPI, encodes it to the MAX96712 through the GMSL loop, and the MAX96712 chip decodes and outputs MIPI signal to the Z7-P, and then image will be displayed on the DP display.