# ZYNQ UltraScale+ FPGA Development Board AXU7EV

# User Manual

ALINX

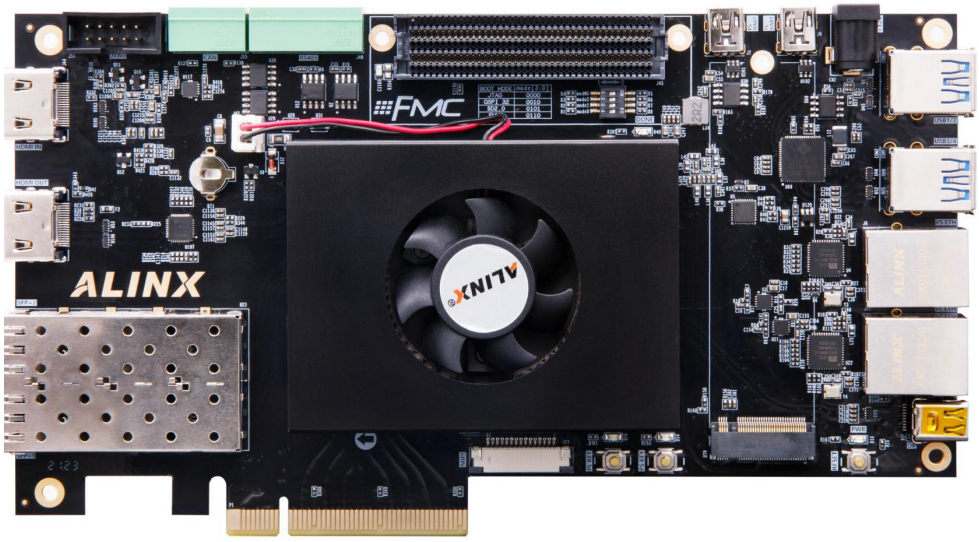
# Version Record

| Version | Date | Release By | Description |
|---|---|---|---|
| Rev 1.1 | 2021-07-28 | Rachel Zhou | First Release |

# Table of Contents

This MPSoCs FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX Zynq UltraScale+ EV chip ZU7EV solution, uses Processing System(PS)+Programmable Logic(PL) technology to integrate dual-core ARM ARM Cortex-A53 and FPGA programmable logic on a single chip. In addition, the PS side of the core board has 4 pieces of 1GB high-speed DDR4 SDRAM chips, 1 piece of 8GB eMMC memory chip and 2 piece of 256Mb QSPI FLASH chip; the PL side of the core board has 4 pieces of 1GB DDR4 SDRAM chip

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 FMC LPC interface, 1 M.2 SSD interface, 1 Mini DP interface, 4 USB 3.0 Interface, 2 Gigabit Ethernet interfaces, 1 HDMI Output, 1 HDMI Input, 2 Uart, 1 PCIe x 8, 1 TF card slot, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 1 MIPI Camera Interface. It meets users' requirements for high-speed data exchange, data storage, Video transmission processing, deep learning, artificial intelligence and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in MPSoCs development.



# Part 1: FPGA Development Board Introduction

The entire structure of the AXU7EV PGA development board is inherited from our consistent core board + carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of the smallest system of ZU7EV + 8 DDR4 + eMMC + 2 QSPI FLASH, the main FPGA chip is Xilinx's Zynq UltraScale+ MPSoCs family chip, the model number is XCZU7EV-2FFVB1156I. ZU7EV chip can be divided into processor system part Processor System (PS) and programmable logic part Programmable Logic (PL). On the PS side and PL side of the ZU7EV chip, there are 4 DDR4 and 4 DDR4 respectively, each with a capacity of up to 1GB, which enables the ARM system and FPGA system to independently process and store data. The 8GB eMMC FLASH memory chip and two 256Mb QSPI FLASH which are on the PS side, used to statically store the operating system, file system and user data of MPSoCs.

The AXU7EV carrier board expands its rich peripheral interface, including 1 FMC_LPC interface, 1 M.2 SSD interface, 1 Mini DP output interface, 2 SFP Interfaces, 4 USB 3.0 Interface, 2 Gigabit Ethernet interfaces, 1 HDMI Input Interfaces, 1 HDMI Output Interfaces, 2 UART, 1 SD card slot, 1 PCIe x8, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 1 MIPI Camera Interface, 40-pin expansion ports and some keys and LEDs.

The following figure shows the structure of the entire development system:

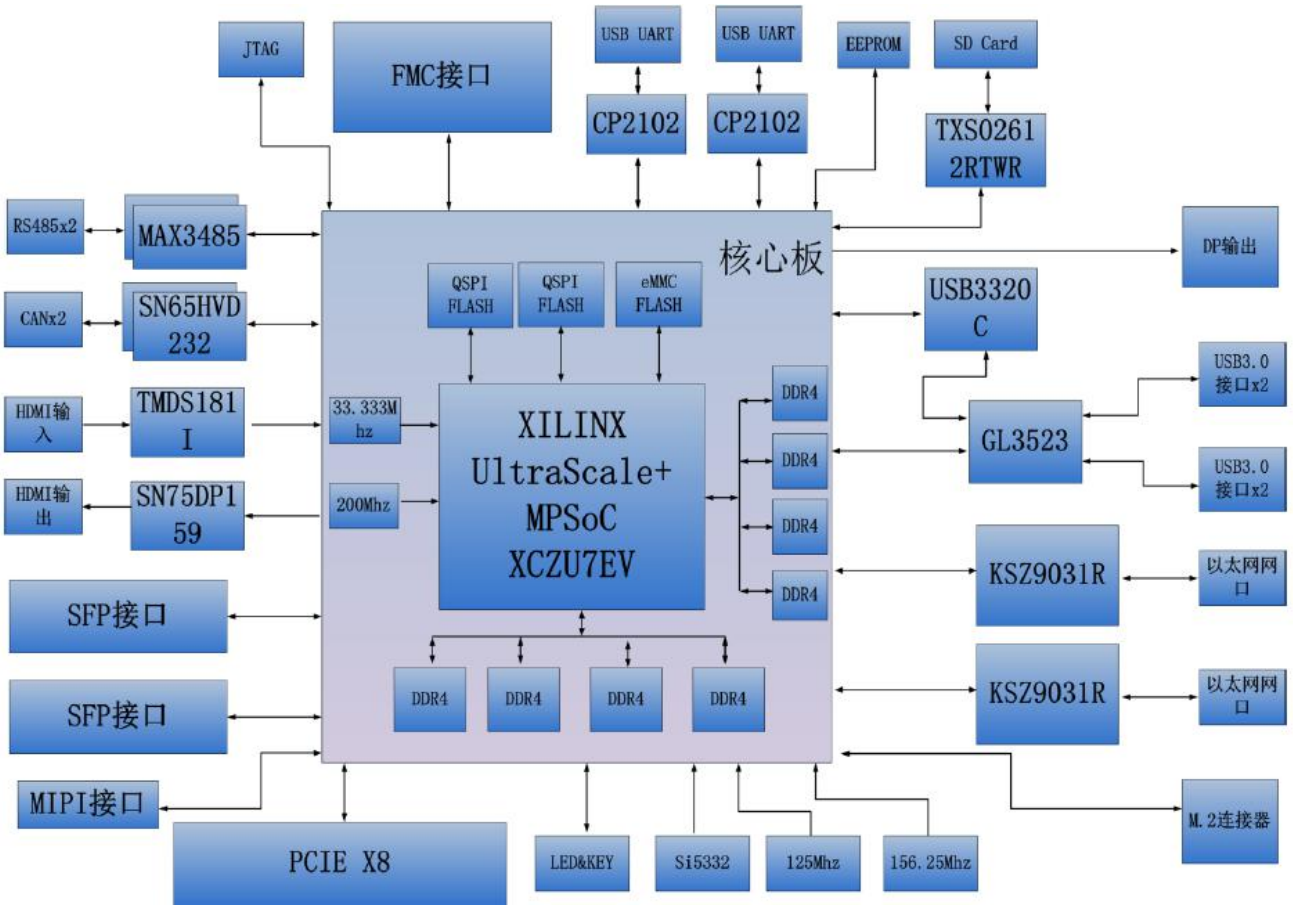



Figure 1-1-1: The Schematic Diagram of the AXU7EV

Through this diagram, you can see the interfaces and functions that the AXU7EV FPGA Development Board contains:

- ZU7EV core board

  It consists of ZU7EV +4GB DDR4（PS）+4GB DDR4（PL）+8GB eMMC FLASH + 512Mb QSPI FLASH, and there are 2 crystal oscillators to provide the clock, a single-ended 33.3333MHz crystal oscillator for the PS system, and a differential 200MHz crystal oscillator for the PL logic DDR reference clock.

- PCIe x 8 Interface

  It supports the PCI Express 3.0 standard, provides a standard PCIe x 8 high-speed data transmission interface, and the single-channel communication rate can be as high as 8GBaud.

- M.2 Interface

  1 PCIEx1 standard M.2 interface, used to connect M.2 SSD solid state drives, with a communication speed of up to 6Gbps.

- DP Output Interface

  1 standard Display Port output display interface, used for video image display. Supports up to 4K@30Hz or 1080P@60Hz output

- USB 3.0 Interface

  4-channel USB3.0 HOST interface, USB interface type is TYPE A. Used to connect external USB peripherals, such as connecting a mouse, keyboard, U disk, etc.

- HDMI Output Interface

  1 HDMI video output interface, using SN75DP159RSBR DP HDMI encoding chip from TI, supports up to 4K@60Hz output.

- HDMI Input Interface

  1 HDMI video input interface, using TMDS181IRGZT HDMI decoding chip from TI, supports up to 4K@60Hz input and supports data input in different formats.

- Gigabit Ethernet Interface

  2-Channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices.

- USB Uart Interface

  2-Channel Uart to USB interfaces for communication with the computer, for user debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- 2-Channel SFP Fiber Interface

  The two high-speed transceivers of the GTH transceiver are connected to the transmitting and receiving of two optical modules, realizing two high-speed optical fiber communication interfaces. The transmitting and

sending speed of each optical fiber data communication is as high as 12.5Gb/s.

- SD Card Slot Interface

  1 Micro SD card holder, used to store operating system image and file system.

- FMC Expansion Interface

  1 standard FMC LPC expansion port, which can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.).

- CAN Communication Interface

  Two-way CAN bus interface, using TI's SN65HVD232 chip, the interface uses 4Pin green terminal blocks.

- 485 Communication Interface

  Two-way 485 communication interface, using MAX3485 chip of MAXIM company. The interface uses 6Pin green terminal blocks.

- MIPI Interface

  2 Lane MIPI camera input interfaces, used to connect MIPI camera module (AN5641).

- 40-pin Expansion Header

  The 40-pin 2.54mm pitch expansion port use for external ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port includes 1 channel of 5V power supply, 2 channels of 3.3V power supply, 3 channels of ground, and 34 channels of IO port.

- JTAG debug port

  A 10-pin 0.1 spacing standard JTAG ports for FPGA program download and debugging. Users can debug and download the ZU7EV system through the XILINX downloader.

- Temperature and humidity sensor chip LM75

On-board temperature and humidity sensor chip LM75, used to detect the temperature and humidity of the surrounding environment around the FPGA development board

- EEPROM

  One EEPROM 24LC04 with I2C interface

- Real Time Clock (RTC)

  1 built-in RTC real-time clock

- LED Lights

  5 LEDs, include 1 LED on the core board, 4 LEDs on the carrier board. There are 1 power indicator and on the core board. There are 1 power indicator,1 DONE Configuration indicator and 2 user indicators on the carrier board.

- KEYs

  3 KEYs, include 1 Rest KEY and 2 User KEYs.

# Part 2: ACU7EV Core Board

## Part 2.1: ACU7EV Core Board Introduction

ACU7EV (core board model, the same below) FPGA core board, ZYNQ chip is based on XCZU7EV-2FFVB1156I of XILINX company Zynq UltraScale+ MPSoCs EG Family.

This core board uses 8 Micron DDR4 chips MT40A512M16GE, of which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity. 4 DDR4 chip is mounted on the PL end, which is a 64-bit data bus width and a capacity of 4GB. The highest operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the highest operating speed of DDR4 SDRAM on the PL side can reach 1200MHz (data rate 2400Mbps). In addition, two 256MBit QSPI FLASH and an 8GB eMMC FLASH chip are also integrated on the core board to start storage configuration and system files.

In order to connect with the carrier board, the four board-to-board connectors of this core board expand the PS side USB2.0 interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports; also expand 4 pairs of PS MGT high-speed transceiver interface; and 16 GTH transceivers and almost all IO ports on the PL side (HP I/O: 143, HD I/O: 46). The wiring between the XCZU7EV chip and the interface has been processed with equal length and differential, and the core board size is only 3.15*2.36 (inch), which is very suitable for secondary development.

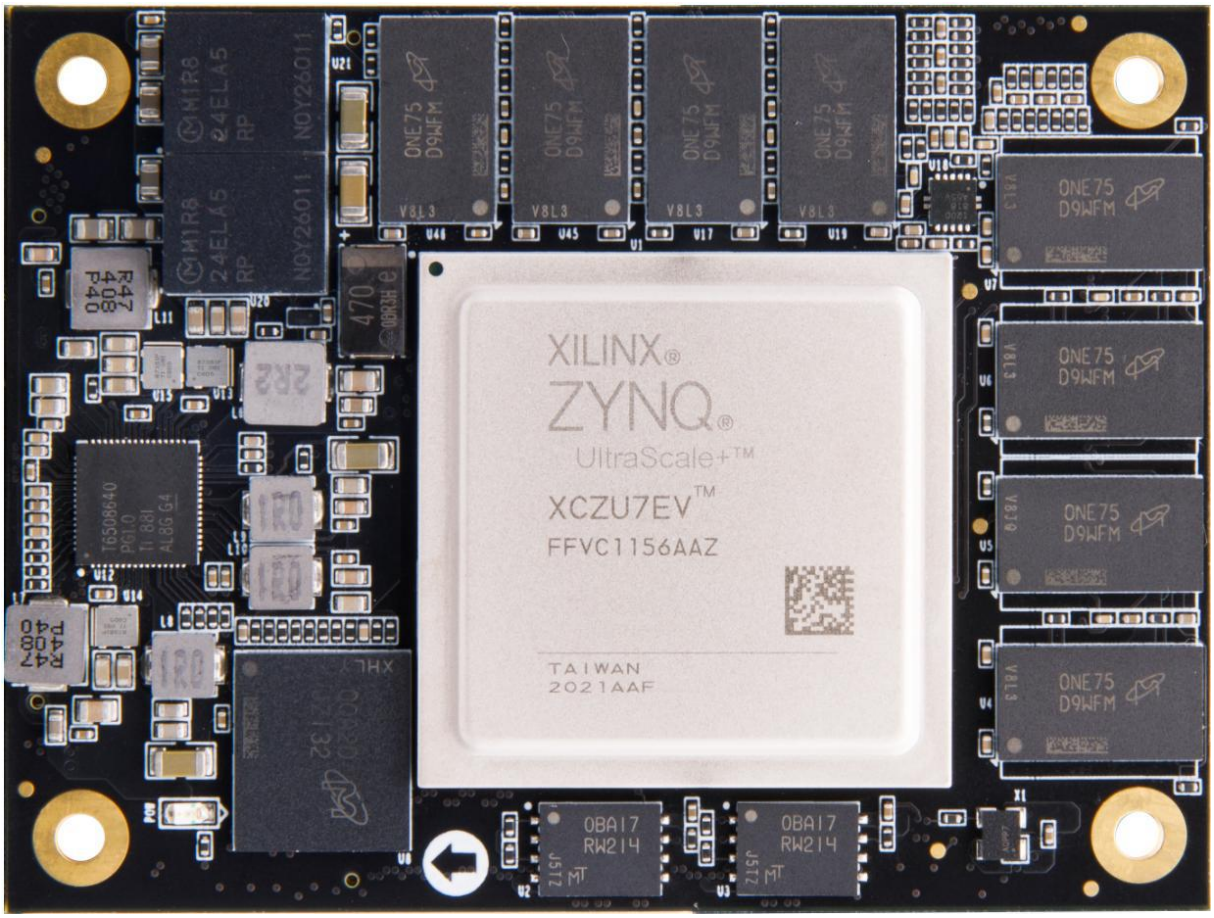



Figure 2-1-1: ACU7EV Core Board (Front View)

## Part 2.2: ZYNQ Chip

The FPGA core board ACU7EV uses Xilinx's Zynq UltraScale+ MPSoCs EV family chip, module XCZU7EV-2FFVB1156I. The PS system of the ZU7EV chip integrates 4 ARM Cortex™-A53 processors with a speed of up to 1.3Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 533Mhz

The ZU7EV chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, with rich high-speed interfaces on the PS side such as PCIE Gen2, USB3.0, SATA 3.1, DisplayPort; it also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL end contains a wealth of programmable logic units, DSP and internal RAM. .

Figure 2-2-1 detailed the Overall Block Diagram of the ZU7EV Chip.

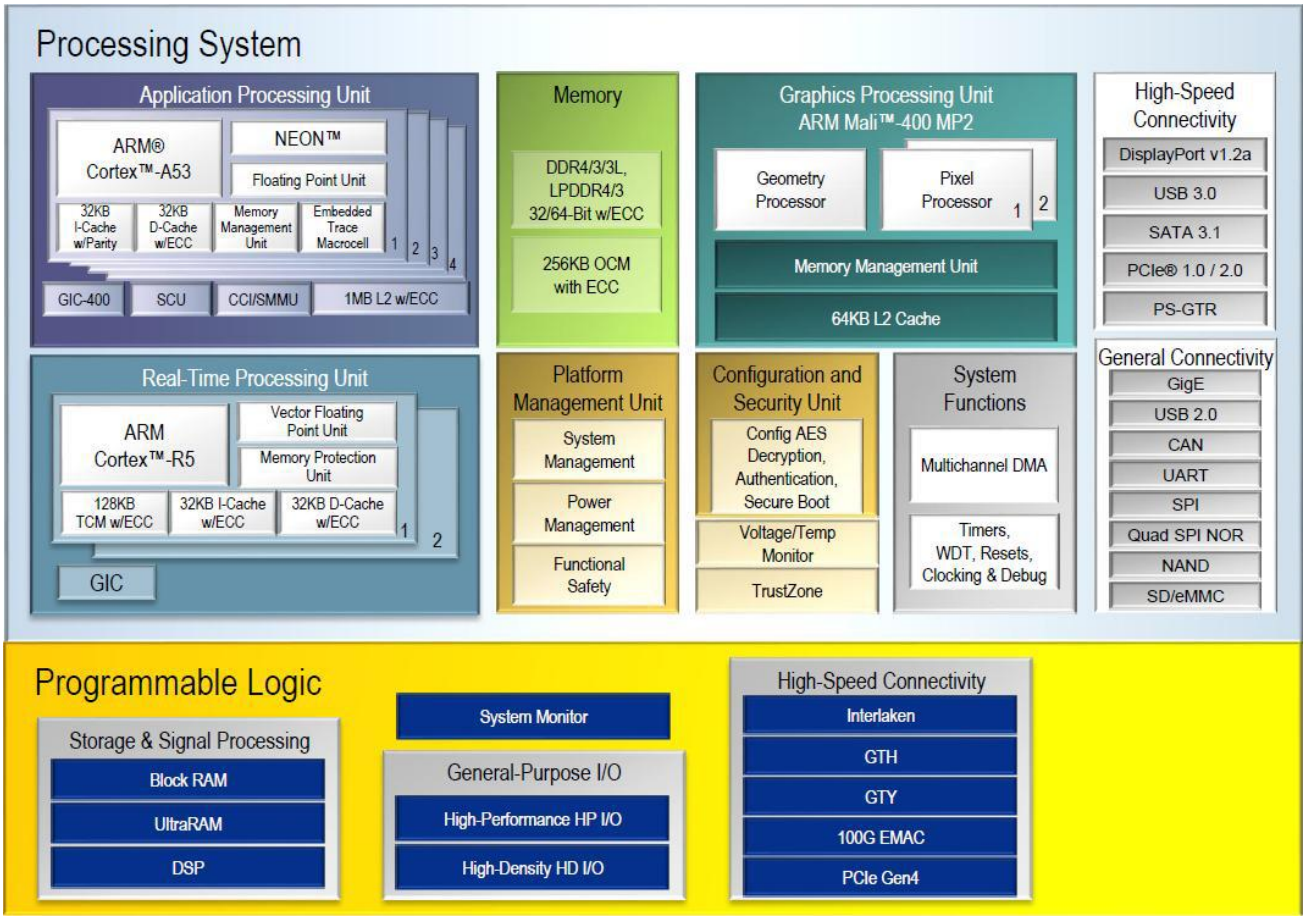



Figure 2-2-1: Overall Block Diagram of the ZYNQ ZU7EV Chip

## The main parameters of the PS system part are as follows:

- ARM quad-core Cortex™-A53 processor, speed up to 1.3GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs
- ARM dual-core Cortex-R5 processor, speed up to 533MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.
- Image video processor Mali-400 MP2, speed up to 677MHz, 64KB level 2 cache.
- External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface

- Static storage interface, support NAND, 2xQuad-SPI FLASH.
- High-speed connection interface, support PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode, Gigabit Ethernet
- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO
- Power management: Support the four-part division of power supply Full/Low/PL/Battery
- Encryption algorithm: support RSA, AES and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

**The main parameters of the PL logic part are as follows:**

- Logic Cells: 504K
- CLB Flip-flops: 460.8K
- Look-up-tables (LUTs): 230.4K
- Block RAM: 11Mb
- Clock Management Units (CMTs): 8
- DSP Slices: 1728
- GTH 16.3Gb/s Transceiver: 24

XCZU7EV-2FFVB1156I chip speed grade is -2, industrial grade, package is FFVB1156.

## Part 2.3: DDR4 DRAM

The ACU7EV core board is equipped with 8 Micron (Micron) 1GB DDR4 chips, model MT40A512M16LY-062E, of which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity. Four DDR4 chip is mounted on the PL end, which is a 64-bit data bus width and a capacity

of 4GB. The maximum operating speed of the DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the 4 DDR4 storage systems are directly connected to the memory interface of the PS BANK504. The highest operating speed of the DDR4 SDRAM on the PL side can reach 1200MHz (data rate 2400Mbps), and four piece of DDR4 is connected to the BANK66,67,68 interface of the FPGA. The specific configuration of DDR4 SDRAM is shown in Table 2-3-1 below:

| Position | Bit Number | Chip Model | Capacity | Factory |
|---|---|---|---|---|
| PS | U4,U5,U6,U7 | MT40A512M16LY-062E | 512M x 16bit | Micron |
| PL | U17,U19,U45,U46 | MT40A512M16LY-062E | 512M x 16bit | Micron |

Table 2-3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection of DDR4 SDRAM on the PS Side is shown in Figure 2-3-1:

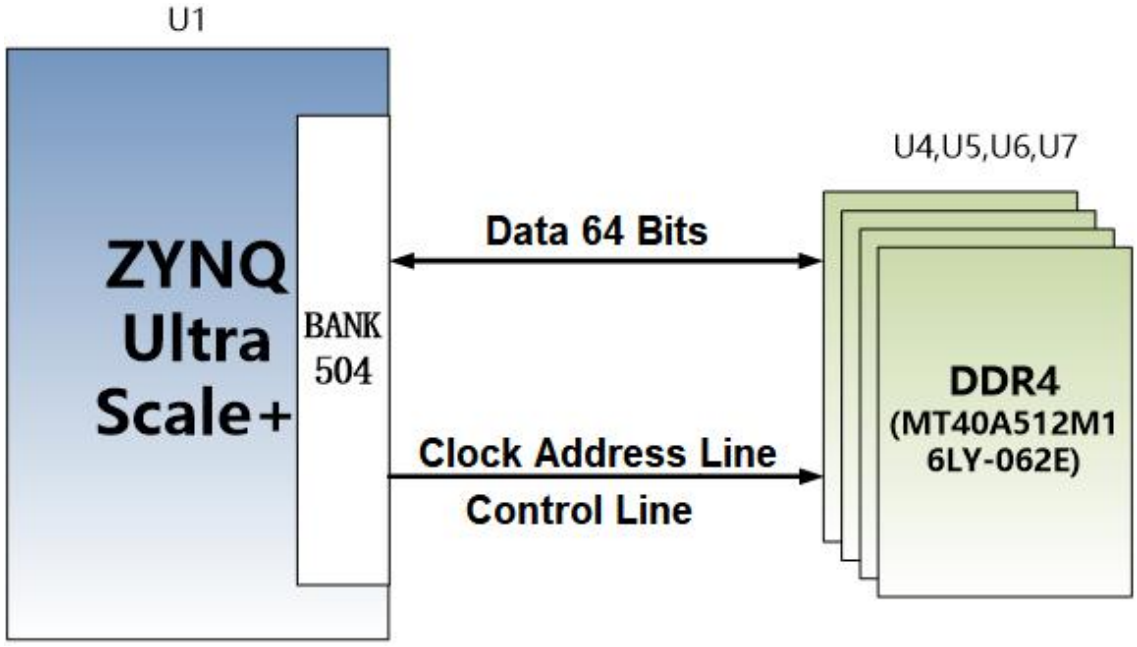



Figure 2-3-1: DDR3 DRAM schematic diagram

The hardware connection of DDR4 SDRAM on the PL Side is shown in Figure 2-3-2:

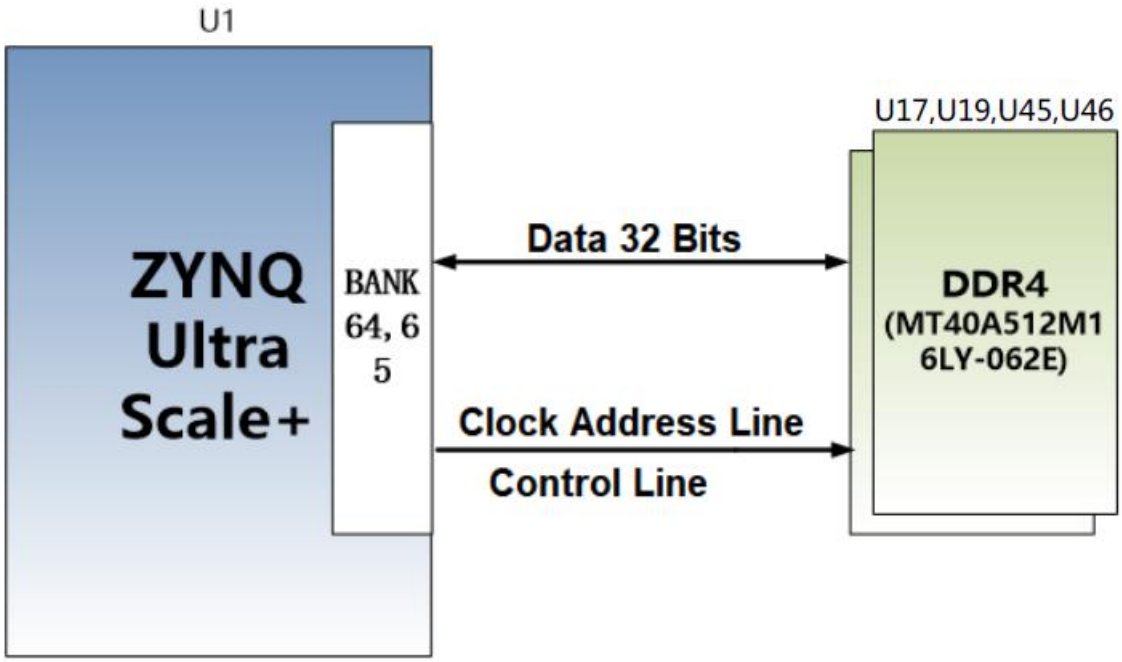



Figure 2-3-2: DDR4 DRAM schematic diagram

**PS Side DDR4 DRAM pin assignment:**

| Signal Name | Pin Name | Pin Number |
|---|---|---|
| PS_DDR4_DQS0_N | PS_DDR_DQS_N0_504 | AN27 |
| PS_DDR4_DQS0_P | PS_DDR_DQS_P0_504 | AN26 |
| PS_DDR4_DQS1_N | PS_DDR_DQS_N1_504 | AP30 |
| PS_DDR4_DQS1_P | PS_DDR_DQS_P1_504 | AN29 |
| PS_DDR4_DQS2_N | PS_DDR_DQS_N2_504 | AJ26 |
| PS_DDR4_DQS2_P | PS_DDR_DQS_P2_504 | AH26 |
| PS_DDR4_DQS3_N | PS_DDR_DQS_N3_504 | AK29 |
| PS_DDR4_DQS3_P | PS_DDR_DQS_P3_504 | AK28 |
| PS_DDR4_DQS4_N | PS_DDR_DQS_N4_504 | AD31 |
| PS_DDR4_DQS4_P | PS_DDR_DQS_P4_504 | AD30 |
| PS_DDR4_DQS5_N | PS_DDR_DQS_N5_504 | Y28 |
| PS_DDR4_DQS5_P | PS_DDR_DQS_P5_504 | Y27 |
| PS_DDR4_DQS6_N | PS_DDR_DQS_N6_504 | AB34 |
| PS_DDR4_DQS6_P | PS_DDR_DQS_P6_504 | AB33 |

| | | |
|---|---|---|
| PS_DDR4_DQS7_N | PS_DDR_DQS_N7_504 | W32 |
| PS_DDR4_DQS7_P | PS_DDR_DQS_P7_504 | W31 |
| PS_DDR4_DQ0 | PS_DDR_DQ0_504 | AP27 |
| PS_DDR4_DQ1 | PS_DDR_DQ1_504 | AP25 |
| PS_DDR4_DQ2 | PS_DDR_DQ2_504 | AP26 |
| PS_DDR4_DQ3 | PS_DDR_DQ3_504 | AM26 |
| PS_DDR4_DQ4 | PS_DDR_DQ4_504 | AP24 |
| PS_DDR4_DQ5 | PS_DDR_DQ5_504 | AL25 |
| PS_DDR4_DQ6 | PS_DDR_DQ6_504 | AM25 |
| PS_DDR4_DQ7 | PS_DDR_DQ7_504 | AM24 |
| PS_DDR4_DQ8 | PS_DDR_DQ8_504 | AM28 |
| PS_DDR4_DQ9 | PS_DDR_DQ9_504 | AN28 |
| PS_DDR4_DQ10 | PS_DDR_DQ10_504 | AP29 |
| PS_DDR4_DQ11 | PS_DDR_DQ11_504 | AP28 |
| PS_DDR4_DQ12 | PS_DDR_DQ12_504 | AM31 |
| PS_DDR4_DQ13 | PS_DDR_DQ13_504 | AP31 |
| PS_DDR4_DQ14 | PS_DDR_DQ14_504 | AN31 |
| PS_DDR4_DQ15 | PS_DDR_DQ15_504 | AM30 |
| PS_DDR4_DQ16 | PS_DDR_DQ16_504 | AF25 |
| PS_DDR4_DQ17 | PS_DDR_DQ17_504 | AG25 |
| PS_DDR4_DQ18 | PS_DDR_DQ18_504 | AG26 |
| PS_DDR4_DQ19 | PS_DDR_DQ19_504 | AJ25 |
| PS_DDR4_DQ20 | PS_DDR_DQ20_504 | AG24 |
| PS_DDR4_DQ21 | PS_DDR_DQ21_504 | AK25 |
| PS_DDR4_DQ22 | PS_DDR_DQ22_504 | AJ24 |
| PS_DDR4_DQ23 | PS_DDR_DQ23_504 | AK24 |
| PS_DDR4_DQ24 | PS_DDR_DQ24_504 | AH28 |
| PS_DDR4_DQ25 | PS_DDR_DQ25_504 | AH27 |
| PS_DDR4_DQ26 | PS_DDR_DQ26_504 | AJ27 |
| PS_DDR4_DQ27 | PS_DDR_DQ27_504 | AK27 |
| PS_DDR4_DQ28 | PS_DDR_DQ28_504 | AL26 |
| PS_DDR4_DQ29 | PS_DDR_DQ29_504 | AL27 |
| PS_DDR4_DQ30 | PS_DDR_DQ30_504 | AH29 |
| PS_DDR4_DQ31 | PS_DDR_DQ31_504 | AL28 |
| PS_DDR4_DQ32 | PS_DDR_DQ32_504 | AB29 |
| PS_DDR4_DQ33 | PS_DDR_DQ33_504 | AB30 |

| | | |
|---|---|---|
| PS_DDR4_DQ34 | PS_DDR_DQ34_504 | AC29 |
| PS_DDR4_DQ35 | PS_DDR_DQ35_504 | AD32 |
| PS_DDR4_DQ36 | PS_DDR_DQ36_504 | AC31 |
| PS_DDR4_DQ37 | PS_DDR_DQ37_504 | AE30 |
| PS_DDR4_DQ38 | PS_DDR_DQ38_504 | AC28 |
| PS_DDR4_DQ39 | PS_DDR_DQ39_504 | AE29 |
| PS_DDR4_DQ40 | PS_DDR_DQ40_504 | AC27 |
| PS_DDR4_DQ41 | PS_DDR_DQ41_504 | AA27 |
| PS_DDR4_DQ42 | PS_DDR_DQ42_504 | AA28 |
| PS_DDR4_DQ43 | PS_DDR_DQ43_504 | AB28 |
| PS_DDR4_DQ44 | PS_DDR_DQ44_504 | W27 |
| PS_DDR4_DQ45 | PS_DDR_DQ45_504 | W29 |
| PS_DDR4_DQ46 | PS_DDR_DQ46_504 | W28 |
| PS_DDR4_DQ47 | PS_DDR_DQ47_504 | V27 |
| PS_DDR4_DQ48 | PS_DDR_DQ48_504 | AA32 |
| PS_DDR4_DQ49 | PS_DDR_DQ49_504 | AA33 |
| PS_DDR4_DQ50 | PS_DDR_DQ50_504 | AA34 |
| PS_DDR4_DQ51 | PS_DDR_DQ51_504 | AE34 |
| PS_DDR4_DQ52 | PS_DDR_DQ52_504 | AD34 |
| PS_DDR4_DQ53 | PS_DDR_DQ53_504 | AB31 |
| PS_DDR4_DQ54 | PS_DDR_DQ54_504 | AC34 |
| PS_DDR4_DQ55 | PS_DDR_DQ55_504 | AC33 |
| PS_DDR4_DQ56 | PS_DDR_DQ56_504 | AA30 |
| PS_DDR4_DQ57 | PS_DDR_DQ57_504 | Y30 |
| PS_DDR4_DQ58 | PS_DDR_DQ58_504 | AA31 |
| PS_DDR4_DQ59 | PS_DDR_DQ59_504 | W30 |
| PS_DDR4_DQ60 | PS_DDR_DQ60_504 | Y33 |
| PS_DDR4_DQ61 | PS_DDR_DQ61_504 | W33 |
| PS_DDR4_DQ62 | PS_DDR_DQ62_504 | W34 |
| PS_DDR4_DQ63 | PS_DDR_DQ63_504 | Y34 |
| PS_DDR4_DM0 | PS_DDR_DM0_504 | AN24 |
| PS_DDR4_DM1 | PS_DDR_DM1_504 | AM29 |
| PS_DDR4_DM2 | PS_DDR_DM2_504 | AH24 |
| PS_DDR4_DM3 | PS_DDR_DM3_504 | AJ29 |
| PS_DDR4_DM4 | PS_DDR_DM4_504 | AD29 |
| PS_DDR4_DM5 | PS_DDR_DM5_504 | Y29 |

| | | |
|---|---|---|
| PS_DDR4_DM6 | PS_DDR_DM6_504 | AC32 |
| PS_DDR4_DM7 | PS_DDR_DM7_504 | Y32 |
| PS_DDR4_A0 | PS_DDR_A0_504 | AN34 |
| PS_DDR4_A1 | PS_DDR_A1_504 | AM34 |
| PS_DDR4_A2 | PS_DDR_A2_504 | AM33 |
| PS_DDR4_A3 | PS_DDR_A3_504 | AL34 |
| PS_DDR4_A4 | PS_DDR_A4_504 | AL33 |
| PS_DDR4_A5 | PS_DDR_A5_504 | AK33 |
| PS_DDR4_A6 | PS_DDR_A6_504 | AK30 |
| PS_DDR4_A7 | PS_DDR_A7_504 | AJ30 |
| PS_DDR4_A8 | PS_DDR_A8_504 | AJ31 |
| PS_DDR4_A9 | PS_DDR_A9_504 | AH31 |
| PS_DDR4_A10 | PS_DDR_A10_504 | AG31 |
| PS_DDR4_A11 | PS_DDR_A11_504 | AF31 |
| PS_DDR4_A12 | PS_DDR_A12_504 | AG30 |
| PS_DDR4_A13 | PS_DDR_A13_504 | AF30 |
| PS_DDR4_ODT0 | PS_DDR_ODT0_504 | AP32 |
| PS_DDR4_PARITY | PS_DDR_PARITY_504 | AA26 |
| PS_DDR4_RAS_B | PS_DDR_A16_504 | AF28 |
| PS_DDR4_RESET_B | PS_DDR_RAM_RST_N_504 | AD26 |
| PS_DDR4_WE_B | PS_DDR_A14_504 | AG29 |
| PS_DDR4_ACT_B | PS_DDR_ACT_N_504 | AE25 |
| PS_DDR4_ALERT_B | PS_DDR_ALERT_N_504 | AB26 |
| PS_DDR4_BA0 | PS_DDR_BA0_504 | AE27 |
| PS_DDR4_BA1 | PS_DDR_BA1_504 | AE28 |
| PS_DDR4_BG0 | PS_DDR_BG0_504 | AD27 |
| PS_DDR4_CAS_B | PS_DDR_A15_504 | AG28 |
| PS_DDR4_CKE0 | PS_DDR_CKE0_504 | AN33 |
| PS_DDR4_CS0_B | PS_DDR_CS_N0_504 | AP33 |
| PS_DDR4_CLK0_N | PS_DDR_CK_N0_504 | AN32 |
| PS_DDR4_CLK0_P | PS_DDR_CK0_504 | AL31 |

## PL Side DDR4 DRAM pin assignment:

| Signal Name | Pin Name | Pin Number |
|---|---|---|
| PL_DDR4_DQS0_N | IO_L10N_T1U_N7_QBC_AD4N_67 | F13 |

| | | |
|---|---|---|
| PL_DDR4_DQS0_P | IO_L10P_T1U_N6_QBC_AD4P_67 | G14 |
| PL_DDR4_DQS1_N | IO_L4N_T0U_N7_DBC_AD7N_67 | B13 |
| PL_DDR4_DQS1_P | IO_L4P_T0U_N6_DBC_AD7P_67 | B14 |
| PL_DDR4_DQS2_N | IO_L16N_T2U_N7_QBC_AD3N_67 | H17 |
| PL_DDR4_DQS2_P | IO_L16P_T2U_N6_QBC_AD3P_67 | H18 |
| PL_DDR4_DQS3_N | IO_L22N_T3U_N7_DBC_AD0N_67 | K15 |
| PL_DDR4_DQS3_P | IO_L22P_T3U_N6_DBC_AD0P_67 | L15 |
| PL_DDR4_DQS4_N | IO_L16N_T2U_N7_QBC_AD3N_68 | D10 |
| PL_DDR4_DQS4_P | IO_L16P_T2U_N6_QBC_AD3P_68 | D11 |
| PL_DDR4_DQS5_N | IO_L22N_T3U_N7_DBC_AD0N_68 | A10 |
| PL_DDR4_DQS5_P | IO_L22P_T3U_N6_DBC_AD0P_68 | B10 |
| PL_DDR4_DQS6_N | IO_L10N_T1U_N7_QBC_AD4N_68 | D9 |
| PL_DDR4_DQS6_P | IO_L10P_T1U_N6_QBC_AD4P_68 | E9 |
| PL_DDR4_DQS7_N | IO_L4N_T0U_N7_DBC_AD7N_68 | J11 |
| PL_DDR4_DQS7_P | IO_L4P_T0U_N6_DBC_AD7P_68 | K12 |
| PL_DDR4_DQ0 | IO_L9N_T1L_N5_AD12N_67 | E17 |
| PL_DDR4_DQ1 | IO_L11P_T1U_N8_GC_67 | D15 |
| PL_DDR4_DQ2 | IO_L8P_T1L_N2_AD5P_67 | D17 |
| PL_DDR4_DQ3 | IO_L12N_T1U_N11_GC_67 | E14 |
| PL_DDR4_DQ4 | IO_L9P_T1L_N4_AD12P_67 | E18 |
| PL_DDR4_DQ5 | IO_L11N_T1U_N9_GC_67 | D14 |
| PL_DDR4_DQ6 | IO_L12P_T1U_N10_GC_67 | E15 |
| PL_DDR4_DQ7 | IO_L8N_T1L_N3_AD5N_67 | C17 |
| PL_DDR4_DQ8 | IO_L2P_T0L_N2_67 | B16 |
| PL_DDR4_DQ9 | IO_L6P_T0U_N10_AD6P_67 | C13 |
| PL_DDR4_DQ10 | IO_L3P_T0L_N4_AD15P_67 | A15 |
| PL_DDR4_DQ11 | IO_L5P_T0U_N8_AD14P_67 | A13 |
| PL_DDR4_DQ12 | IO_L2N_T0L_N3_67 | B15 |
| PL_DDR4_DQ13 | IO_L5N_T0U_N9_AD14N_67 | A12 |
| PL_DDR4_DQ14 | IO_L3N_T0L_N5_AD15N_67 | A14 |
| PL_DDR4_DQ15 | IO_L6N_T0U_N11_AD6N_67 | C12 |
| PL_DDR4_DQ16 | IO_L15P_T2L_N4_AD11P_67 | H19 |
| PL_DDR4_DQ17 | IO_L18P_T2U_N10_AD2P_67 | H16 |
| PL_DDR4_DQ18 | IO_L17P_T2U_N8_AD10P_67 | G18 |
| PL_DDR4_DQ19 | IO_L18N_T2U_N11_AD2N_67 | G16 |
| PL_DDR4_DQ20 | IO_L15N_T2L_N5_AD11N_67 | G19 |

| | | |
|---|---|---|
| PL_DDR4_DQ21 | IO_L14N_T2L_N3_GC_67 | F15 |
| PL_DDR4_DQ22 | IO_L17N_T2U_N9_AD10N_67 | F18 |
| PL_DDR4_DQ23 | IO_L14P_T2L_N2_GC_67 | G15 |
| PL_DDR4_DQ24 | IO_L24N_T3U_N11_67 | L16 |
| PL_DDR4_DQ25 | IO_L21N_T3L_N5_AD8N_67 | J17 |
| PL_DDR4_DQ26 | IO_L23P_T3U_N8_67 | K19 |
| PL_DDR4_DQ27 | IO_L21P_T3L_N4_AD8P_67 | K17 |
| PL_DDR4_DQ28 | IO_L24P_T3U_N10_67 | L17 |
| PL_DDR4_DQ29 | IO_L20P_T3L_N2_AD1P_67 | J16 |
| PL_DDR4_DQ30 | IO_L23N_T3U_N9_67 | K18 |
| PL_DDR4_DQ31 | IO_L20N_T3L_N3_AD1N_67 | J15 |
| PL_DDR4_DQ32 | IO_L18N_T2U_N11_AD2N_68 | C11 |
| PL_DDR4_DQ33 | IO_L17P_T2U_N8_AD10P_68 | F12 |
| PL_DDR4_DQ34 | IO_L17N_T2U_N9_AD10N_68 | E12 |
| PL_DDR4_DQ35 | IO_L14P_T2L_N2_GC_68 | F11 |
| PL_DDR4_DQ36 | IO_L18P_T2U_N10_AD2P_68 | D12 |
| PL_DDR4_DQ37 | IO_L15N_T2L_N5_AD11N_68 | H12 |
| PL_DDR4_DQ38 | IO_L15P_T2L_N4_AD11P_68 | H13 |
| PL_DDR4_DQ39 | IO_L14N_T2L_N3_GC_68 | E10 |
| PL_DDR4_DQ40 | IO_L20N_T3L_N3_AD1N_68 | B8 |
| PL_DDR4_DQ41 | IO_L21N_T3L_N5_AD8N_68 | A6 |
| PL_DDR4_DQ42 | IO_L20P_T3L_N2_AD1P_68 | B9 |
| PL_DDR4_DQ43 | IO_L23N_T3U_N9_68 | A7 |
| PL_DDR4_DQ44 | IO_L24P_T3U_N10_68 | B11 |
| PL_DDR4_DQ45 | IO_L21P_T3L_N4_AD8P_68 | B6 |
| PL_DDR4_DQ46 | IO_L24N_T3U_N11_68 | A11 |
| PL_DDR4_DQ47 | IO_L23P_T3U_N8_68 | A8 |
| PL_DDR4_DQ48 | IO_L12P_T1U_N10_GC_68 | G10 |
| PL_DDR4_DQ49 | IO_L9P_T1L_N4_AD12P_68 | F8 |
| PL_DDR4_DQ50 | IO_L8N_T1L_N3_AD5N_68 | C8 |
| PL_DDR4_DQ51 | IO_L9N_T1L_N5_AD12N_68 | E8 |
| PL_DDR4_DQ52 | IO_L12N_T1U_N11_GC_68 | F10 |
| PL_DDR4_DQ53 | IO_L11P_T1U_N8_GC_68 | H9 |
| PL_DDR4_DQ54 | IO_L8P_T1L_N2_AD5P_68 | C9 |
| PL_DDR4_DQ55 | IO_L11N_T1U_N9_GC_68 | G9 |
| PL_DDR4_DQ56 | IO_L5N_T0U_N9_AD14N_68 | J14 |

| | | |
|---|---|---|
| PL_DDR4_DQ57 | IO_L6N_T0U_N11_AD6N_68 | K13 |
| PL_DDR4_DQ58 | IO_L5P_T0U_N8_AD14P_68 | K14 |
| PL_DDR4_DQ59 | IO_L2P_T0L_N2_68 | K10 |
| PL_DDR4_DQ60 | IO_L6P_T0U_N10_AD6P_68 | L14 |
| PL_DDR4_DQ61 | IO_L3P_T0L_N4_AD15P_68 | L12 |
| PL_DDR4_DQ62 | IO_L2N_T0L_N3_68 | J10 |
| PL_DDR4_DQ63 | IO_L3N_T0L_N5_AD15N_68 | L11 |
| PL_DDR4_DM0 | IO_L7P_T1L_N0_QBC_AD13P_67 | D16 |
| PL_DDR4_DM1 | IO_L1P_T0L_N0_DBC_67 | A17 |
| PL_DDR4_DM2 | IO_L13P_T2L_N0_GC_QBC_67 | F17 |
| PL_DDR4_DM3 | IO_L19P_T3L_N0_DBC_AD9P_67 | L20 |
| PL_DDR4_DM4 | IO_L13P_T2L_N0_GC_QBC_68 | H11 |
| PL_DDR4_DM5 | IO_L19P_T3L_N0_DBC_AD9P_68 | C7 |
| PL_DDR4_DM6 | IO_L7P_T1L_N0_QBC_AD13P_68 | F7 |
| PL_DDR4_DM7 | IO_L1P_T0L_N0_DBC_68 | M13 |
| PL_DDR4_A0 | IO_L10P_T1U_N6_QBC_AD4P_66 | AK8 |
| PL_DDR4_A1 | IO_L6P_T0U_N10_AD6P_66 | AM9 |
| PL_DDR4_A2 | IO_L10N_T1U_N7_QBC_AD4N_66 | AL8 |
| PL_DDR4_A3 | IO_L5N_T0U_N9_AD14N_66 | AM10 |
| PL_DDR4_A4 | IO_L11N_T1U_N9_GC_66 | AK10 |
| PL_DDR4_A5 | IO_L3N_T0L_N5_AD15N_66 | AP11 |
| PL_DDR4_A6 | IO_L14N_T2L_N3_GC_66 | AJ11 |
| PL_DDR4_A7 | IO_L4P_T0U_N6_DBC_AD7P_66 | AN9 |
| PL_DDR4_A8 | IO_L17N_T2U_N9_AD10N_66 | AG10 |
| PL_DDR4_A9 | IO_L6N_T0U_N11_AD6N_66 | AM8 |
| PL_DDR4_A10 | IO_L11P_T1U_N8_GC_66 | AJ10 |
| PL_DDR4_A11 | IO_L5P_T0U_N8_AD14P_66 | AM11 |
| PL_DDR4_A12 | IO_L9N_T1L_N5_AD12N_66 | AL12 |
| PL_DDR4_A13 | IO_L4N_T0U_N7_DBC_AD7N_66 | AN8 |
| PL_DDR4_ODT | IO_L16P_T2U_N6_QBC_AD3P_66 | AG9 |
| PL_DDR4_RAS_B | IO_L8P_T1L_N2_AD5P_66 | AL11 |
| PL_DDR4_RST | IO_L14P_T2L_N2_GC_66 | AH11 |
| PL_DDR4_WE_B | IO_L15N_T2L_N5_AD11N_66 | AH13 |
| PL_DDR4_ACT_B | IO_L16N_T2U_N7_QBC_AD3N_66 | AH9 |
| PL_DDR4_BA0 | IO_L7N_T1L_N1_QBC_AD13N_66 | AL13 |
| PL_DDR4_BA1 | IO_L3P_T0L_N4_AD15P_66 | AN11 |

| | | |
|---|---|---|
| PL_DDR4_BG0 | IO_L7P_T1L_N0_QBC_AD13P_66 | AK13 |
| PL_DDR4_CAS_B | IO_L8N_T1L_N3_AD5N_66 | AL10 |
| PL_DDR4_CKE | IO_L15P_T2L_N4_AD11P_66 | AG13 |
| PL_DDR4_CS_B | IO_L9P_T1L_N4_AD12P_66 | AK12 |
| PL_DDR4_CLK_N | IO_L13N_T2L_N1_GC_QBC_66 | AJ12 |
| PL_DDR4_CLK_P | IO_L13P_T2L_N0_GC_QBC_66 | AH12 |

## Part 2.4: QSPI Flash

The FPGA core board ACU7EV is equipped with two 256MBit Quad-SPI FLASH chip to form an 8-bit bandwidth data bus, the flash model is MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

| Position | Model | Capacity | Factory |
|---|---|---|---|
| U2, U3 | MT25QU256ABA1EW9 | 256Mbit | Winbond |

Table 2-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

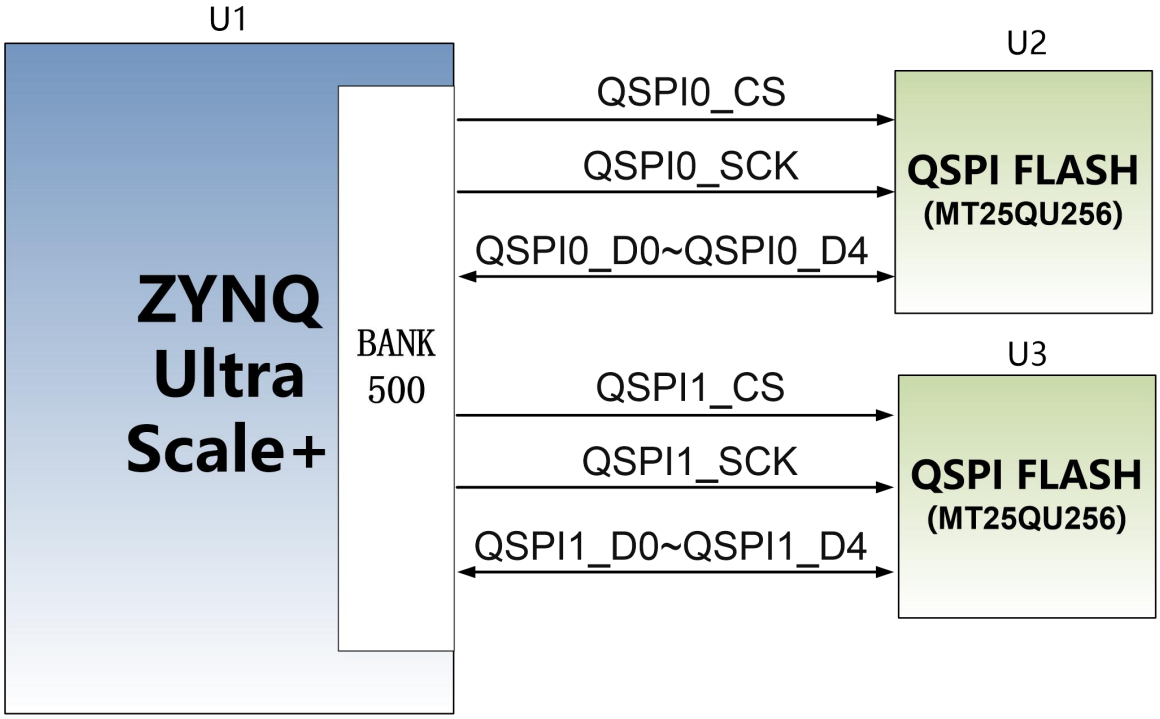



Figure 2-4-1: QSPI Flash in the schematic

**Configure chip pin assignments:**

| Signal Name | Pin Name | Pin Number |
|---|---|---|
| MIO0_QSPI0_SCLK | PS_MIO0_500 | A24 |
| MIO1_QSPI0_IO1 | PS_MIO1_500 | C24 |
| MIO2_QSPI0_IO2 | PS_MIO2_500 | B24 |
| MIO3_QSPI0_IO3 | PS_MIO3_500 | E25 |
| MIO4_QSPI0_IO0 | PS_MIO4_500 | A25 |
| MIO5_QSPI0_SS_B | PS_MIO5_500 | D25 |
| MIO10_QSPI1_IO2 | PS_MIO10_500 | F26 |
| MIO11_QSPI1_IO3 | PS_MIO11_500 | B26 |
| MIO12_QSPI1_SCLK | PS_MIO12_500 | C27 |
| MIO7_QSPI1_SS_B | PS_MIO7_500 | B25 |
| MIO8_QSPI1_IO0 | PS_MIO8_500 | D26 |
| MIO9_QSPI1_IO1 | PS_MIO9_500 | C26 |

## Part 2.5: eMMC Flash

The ACU7EV core board is equipped with a large-capacity 8GB eMMC

FLASH chip, the model is MTFC8GAKAJCN-4M, it supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files and other user data files The specific models and related parameters of eMMC FLASH are shown in Table 2-5-1.

| Position | Model | Capacity | Factory |
|---|---|---|---|
| U19 | MTFC8GAKAJCN-4M | 8G Byte | Micron |

Table 2-5-1: eMMC FLASH Specification

The eMMC FLASH is connected to the GPIO port of the BANK500 of the PS part of the ZYNQ UltraScale+. In the system design, it is necessary to configure the GPIO port function of the PS side as an EMMC interface. Figure 2-5-1 shows the part of eMMC Flash in the schematic diagram.

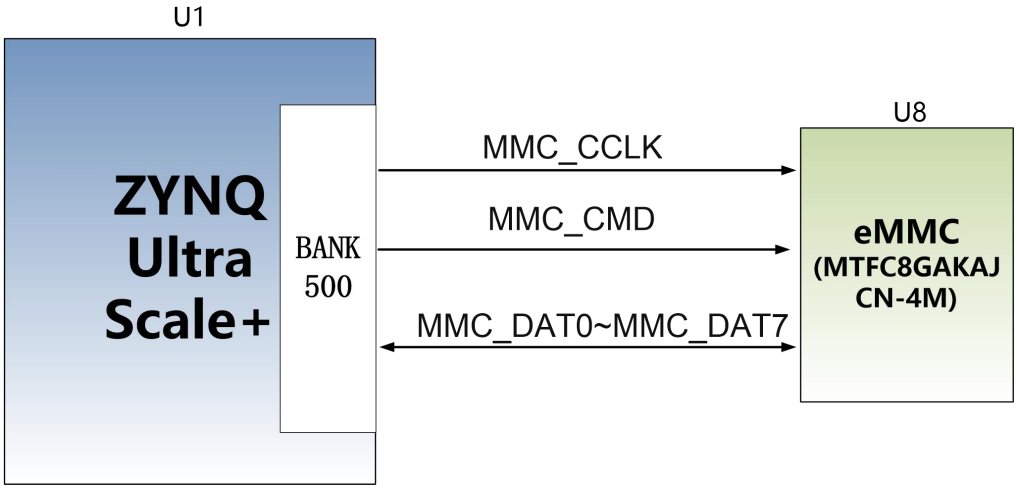



Figure 2-5-1: eMMC Flash in the schematic

**Configuration Chip pin assignment:**

| Signal Name | Pin Name | Pin Number |
|---|---|---|
| MMC_CCLK | PS_MIO22_500 | F28 |
| MMC_CMD | PS_MIO21_500 | C28 |
| MMC_DAT0 | PS_MIO13_500 | D27 |

| | | |
|---|---|---|
| MMC_DAT1 | PS_MIO14_500 | A27 |
| MMC_DAT2 | PS_MIO15_500 | E27 |
| MMC_DAT3 | PS_MIO16_500 | A28 |
| MMC_DAT4 | PS_MIO17_500 | C29 |
| MMC_DAT5 | PS_MIO18_500 | F27 |
| MMC_DAT6 | PS_MIO19_500 | B28 |
| MMC_DAT7 | PS_MIO20_500 | E29 |
| MMC_RSTN | PS_MIO23_500 | B29 |

## Part 2.6: Clock configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 2-6-1:

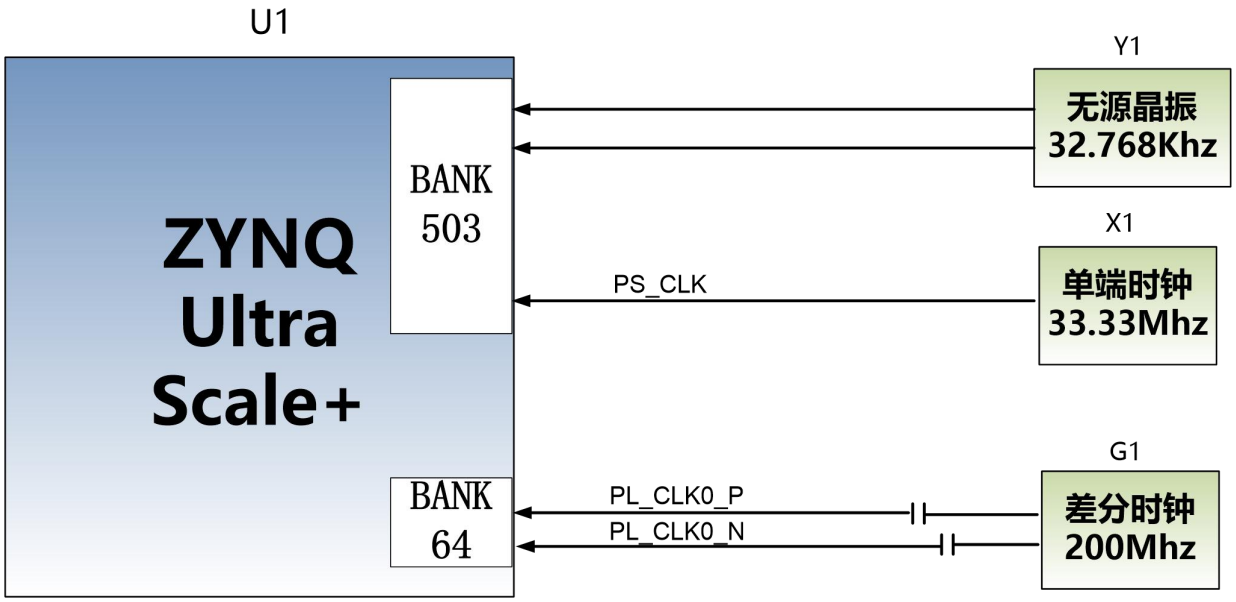



Figure 2-6-1: Core Board Clock Source

### PS System RTC Real Time Clock

The passive crystal Y1 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the PS_PADI_503 and PS_PADO_503 pins of BANK503 of the ZYNQ chip. The schematic

diagram is shown in Figure 2-6-2:

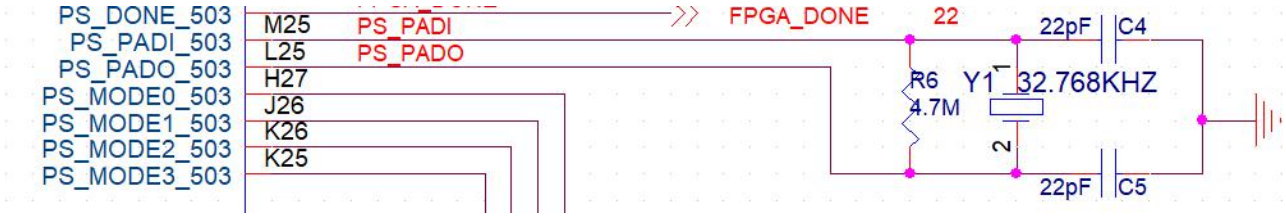



Figure 2-6-2: Passive Crystal Oscillator for RTC

## Clock pin assignment:

| Signal Name | Pin |
|---|---|
| PS_PADI_503 | **M25** |
| PS_PADO_503 | **L25** |

## PS System Clock Source

The X1 crystal on the core board provides a 33.333MHz clock input for the PS part. The clock input is connected to the PS_REF_CLK_503 pin of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-3:

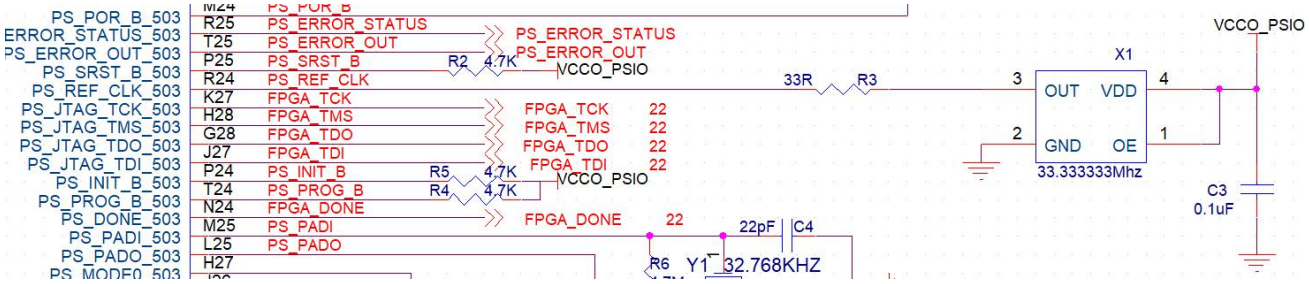



Figure 2-6-3: Active Crystal in PS part

## Clock pin assignment:

| Signal Name | Pin |
|---|---|
| **PS_REF_CLK** | **R24** |

### PL System Clock Source

The core board provides a differential 200MHz PL system clock source for the reference clock of the DDR4 controller. The crystal oscillator output is connected to the global clock (MRCC) of PL BANK64. This global clock can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of this clock source is shown in Figure 2-6-4

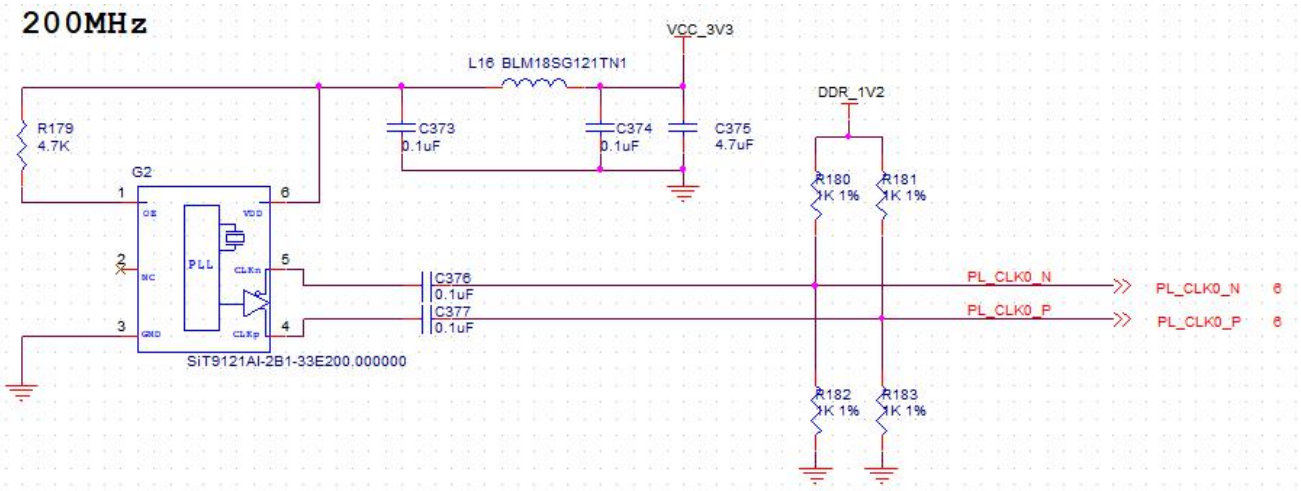


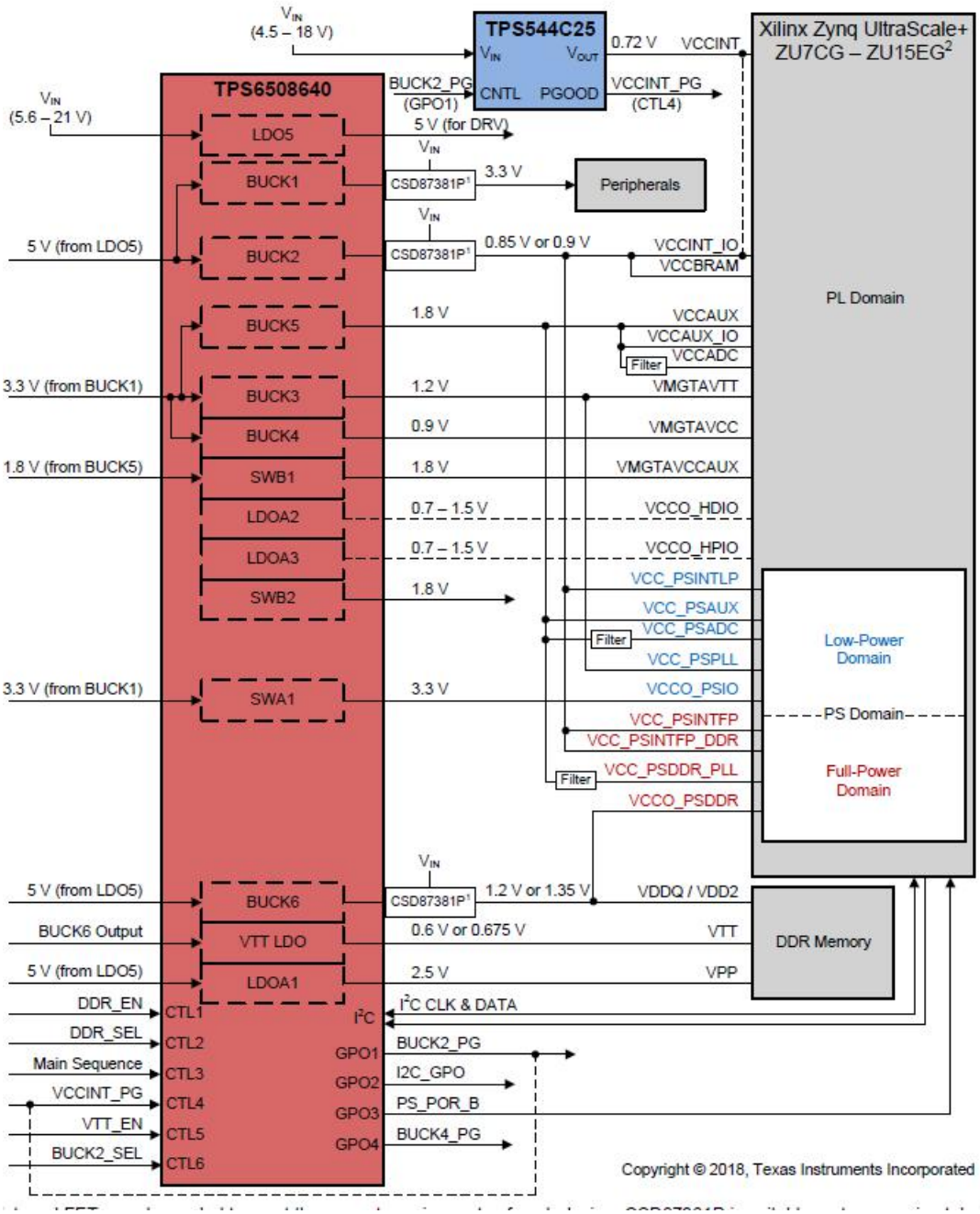

Figure 2-6-4: PL system clock source

### Clock pin assignment:

| Signal Name | Pin |
|---|---|
| PL_CLK0_P | AJ9 |
| PL_CLK0_N | AK9 |

## Part 2.7: Power Supply

The power supply voltage of the ACU7EV core board is DC12V, which is supplied by connecting the carrier board. The core board uses 2 MYMGM1R824 power chips in parallel to achieve a 50A current to provide the core power of the XCZU7EV with 0.85V. In addition, a PMIC chip TPS6508640 is used to generate all other power supplies required by the XCZU7EV chip. For the TPS6508640 power supply design, please refer to the power supply chip manual. The design block diagram is as follows :


TPS544C25
TPS6508640
Xilinx Zynq UltraScale+ ZU7CG – ZU15EG2
PL Domain
Low-Power Domain
PS Domain
Full-Power Domain
DDR Memory
Peripherals
LDO5
BUCK1
BUCK2
BUCK5
BUCK3
BUCK4
SWB1
LDOA2
LDOA3
SWB2
SWA1
BUCK6
VTT LDO
LDOA1
CSD87381P
0.72 V
VCCINT
VCCINT_PG (CTL4)
BUCK2_PG (GPO1)
5 V (for DRV)
3.3 V
0.85 V or 0.9 V
VCCINT_IO
VCCBRAM
1.8 V
VCCAUX
VCCAUX_IO
VCCADC
Filter
1.2 V
VMGTAVTT
0.9 V
VMGTAVCC
VMGTAVCCAUX
0.7 – 1.5 V
VCCO_HDIO
VCCO_HPIO
VCC_PSINTLP
VCC_PSAUX
VCC_PSADC
VCC_PSPLL
VCCO_PSIO
VCC_PSINTFP
VCC_PSINTFP_DDR
VCC_PSDDR_PLL
VCCO_PSDDR
1.2 V or 1.35 V
VDDQ / VDD2
0.6 V or 0.675 V
VTT
2.5 V
VPP
I2C CLK & DATA
BUCK2_PG
I2C_GPO
PS_POR_B
BUCK4_PG
VIN (4.5 – 18 V)
VIN (5.6 – 21 V)
5 V (from LDO5)
3.3 V (from BUCK1)
1.8 V (from BUCK5)
BUCK6 Output
DDR_EN
DDR_SEL
Main Sequence
VCCINT_PG
VTT_EN
BUCK2_SEL
CTL1
CTL2
CTL3
CTL4
CTL5
CTL6
I2C
GPO1
GPO2
GPO3
GPO4
Copyright © 2018, Texas Instruments Incorporated

# Part 2.8: ACU7EV Core Board Size Dimension

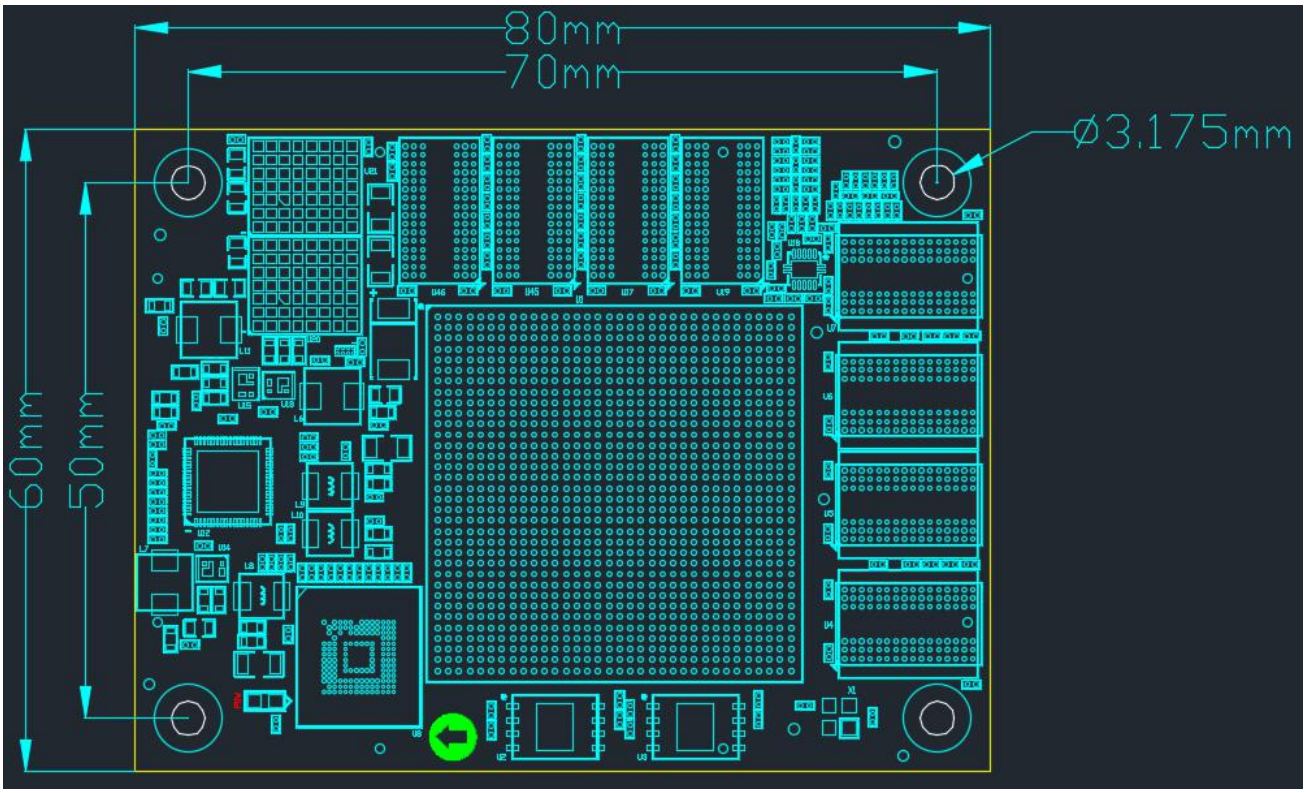



Figure 2-8-1: ACU7EV Core Board Size Dimension

# Part 2.9: Board to Board Connectors pin assignment

The core board has a total of four high-speed expansion ports. It uses four 120-pin inter-board connectors (J29/J30/J31/J32) to connect to the carrier board. The connectors used is Panasonic AXK5A2137YG, and the corresponding connector model in the carrier board is Panasonic AXK6A2337YG.

**J29 connector**

J29 connects to +12V power supply, the IO of BANK28, BANK87,BANK88. the level standard of BANK87, 88 is 3.3V, the level standard of BANK28 is 1.8V, The Level of PS MIO is +1.8V.

**Pin assignment of board to board connector J29**

| J29 Pin | Signal Name | Pin Number | J29 Pin | Signal Name | Pin Number |
|---|---|---|---|---|---|
| 1 | +12V | | 2 | +12V | |
| 3 | +12V | | 4 | +12V | |
| 5 | +12V | | 6 | +12V | |
| 7 | +12V | | 8 | +12V | |
| 9 | +12V | | 10 | +12V | |
| 11 | +12V | | 12 | +12V | |
| 13 | GND | | 14 | GND | |
| 15 | B88_L2_N | B1 | 16 | B88_L1_N | D1 |
| 17 | B88_L2_P | C1 | 18 | B88_L1_P | E1 |
| 19 | GND | | 20 | GND | |
| 21 | B88_L5_N | C2 | 22 | B88_L4_N | E2 |
| 23 | B88_L5_P | D2 | 24 | B88_L4_P | E3 |
| 25 | B88_L8_N | D4 | 26 | B88_L3_N | A2 |
| 27 | B88_L8_P | E4 | 28 | B88_L3_P | A3 |
| 29 | GND | | 30 | GND | |
| 31 | B88_L7_N | B4 | 32 | B88_L6_N | B3 |
| 33 | B88_L7_P | C4 | 34 | B88_L6_P | C3 |
| 35 | B88_L9_N | F4 | 36 | B88_L10_N | A5 |
| 37 | B88_L9_P | F5 | 38 | B88_L10_P | B5 |
| 39 | GND | | 40 | GND | |
| 41 | B88_L11_N | D5 | 42 | B88_L12_N | E5 |
| 43 | B88_L11_P | D6 | 44 | B88_L12_P | F6 |
| 45 | B87_L9_N | J6 | 46 | B87_L10_N | G6 |
| 47 | B87_L9_P | J7 | 48 | B87_L10_P | H6 |
| 49 | GND | | 50 | GND | |
| 51 | B87_L11_N | G7 | 52 | B87_L3_N | M12 |
| 53 | B87_L11_P | H7 | 54 | B87_L3_P | N13 |
| 55 | B87_L5_N | M8 | 56 | B87_L12_N | G8 |
| 57 | B87_L5_P | M9 | 58 | B87_L12_P | H8 |
| 59 | GND | | 60 | GND | |
| 61 | B87_L8_N | J9 | 62 | B87_L7_N | K8 |
| 63 | B87_L8_P | K9 | 64 | B87_L7_P | L8 |
| 65 | B87_L2_N | N8 | 66 | B87_L6_N | L10 |
| 67 | B87_L2_P | N9 | 68 | B87_L6_P | M10 |

| | | | | | |
|---|---|---|---|---|---|
| 69 | GND | | 70 | GND | |
| 71 | B87_L4_N | M11 | 72 | B28_L7_N | D19 |
| 73 | B87_L4_P | N11 | 74 | B28_L7_P | E19 |
| 75 | B28_L20_N | C19 | 76 | B28_L9_N | D21 |
| 77 | B28_L20_P | C18 | 78 | B28_L9_P | D20 |
| 79 | GND | | 80 | GND | |
| 81 | B28_L19_N | A19 | 82 | B28_L10_N | F20 |
| 83 | B28_L19_P | A18 | 84 | B28_L10_P | G20 |
| 85 | B28_L21_N | A21 | 86 | B28_L22_N | B19 |
| 87 | B28_L21_P | A20 | 88 | B28_L22_P | B18 |
| 89 | GND | | 90 | GND | |
| 91 | B28_L24_N | B21 | 92 | B28_L15_N | C22 |
| 93 | B28_L24_P | B20 | 94 | B28_L15_P | C21 |
| 95 | B28_L23_N | A23 | 96 | B28_L17_N | C23 |
| 97 | B28_L23_P | A22 | 98 | B28_L17_P | D22 |
| 99 | GND | | 100 | GND | |
| 101 | PS_MIO43 | E30 | 102 | - | - |
| 103 | PS_MIO26 | A29 | 104 | PS_MIO32 | B31 |
| 105 | PS_MIO27 | A30 | 106 | PS_MIO35 | C31 |
| 107 | PS_MIO31 | B30 | 108 | PS_MIO36 | C32 |
| 109 | PS_MIO40 | D31 | 110 | PS_MIO37 | C33 |
| 111 | PS_MIO44 | E32 | 112 | PS_MIO29 | A32 |
| 113 | PS_MIO39 | D30 | 114 | PS_MIO30 | A33 |
| 115 | PS_MIO33 | B33 | 116 | PS_MIO34 | B34 |
| 117 | PS_MIO41 | D32 | 118 | PS_MIO42 | D34 |
| 119 | PS_MIO28 | A31 | 120 | PS_MIO38 | C34 |

**Pin assignment of board to board connector J30**

J30 is connected to the transceiver signal of BANK505 MGT, MIO of PS and Bank 28. The Level Standard of Bank 28 is 1.8V, the MIO level of PS is 1.8V standard

| J30 Pin | Signal Name | Pin Number | J30 Pin | Signal Name | Pin Number |
|---|---|---|---|---|---|
| 1 | B28_L16_P | E24 | 2 | SD_D2 | F31 |
| 3 | B28_L16_N | D24 | 4 | SD_D3 | F32 |
| 5 | GND | - | 6 | GND | - |

| | | | | | |
|---|---|---|---|---|---|
| 7 | B28_L11_N | E22 | 8 | SD_CMD | F33 |
| 9 | B28_L11_P | F22 | 10 | SD_D0 | E34 |
| 11 | B28_L13_P | F23 | 12 | SD_D1 | F30 |
| 13 | B28_L13_N | E23 | 14 | SD_CLK | F34 |
| 15 | GND | | 16 | GND | |
| 17 | B28_L12_N | F21 | 18 | SD_CD | E33 |
| 19 | B28_L12_P | G21 | 20 | | |
| 21 | B28_L3_P | J21 | 22 | USB_STP | H31 |
| 23 | B28_L3_N | J22 | 24 | USB_DIR | G30 |
| 25 | GND | | 26 | GND | |
| 27 | | | 28 | USB_CLK | G29 |
| 29 | | | 30 | USB_NXT | G33 |
| 31 | | | 32 | USB_DATA0 | G34 |
| 33 | | | 34 | USB_DATA1 | H29 |
| 35 | GND | | 36 | GND | |
| 37 | B28_L18_N | G26 | 38 | USB_DATA2 | G31 |
| 39 | B28_L18_P | G25 | 40 | USB_DATA3 | H32 |
| 41 | B28_L14_N | G24 | 42 | USB_DATA4 | H33 |
| 43 | B28_L14_P | G23 | 44 | USB_DATA5 | H34 |
| 45 | GND | | 46 | GND | |
| 47 | | | 48 | USB_DATA6 | J29 |
| 49 | | | 50 | USB_DATA7 | J30 |
| 51 | | | 52 | PHY1_TXD0 | J32 |
| 53 | | | 54 | PHY1_TXD1 | J34 |
| 55 | GND | | 56 | GND | |
| 57 | | | 58 | PHY1_TXD2 | K28 |
| 59 | | | 60 | PHY1_TXD3 | K29 |
| 61 | PS_POR_B | M24 | 62 | PHY1_TXCK | J31 |
| 63 | FPGA_DONE | N24 | 64 | PHY1_TXCTL | K30 |
| 65 | GND | | 66 | GND | |
| 67 | PS_MODE3 | K25 | 68 | PHY1_RXD3 | L29 |
| 69 | PS_MODE2 | K26 | 70 | PHY1_RXD2 | K34 |
| 71 | PS_MODE1 | J26 | 72 | PHY1_RXD1 | K33 |
| 73 | PS_MODE0 | H27 | 74 | PHY1_RXD0 | K32 |
| 75 | GND | | 76 | GND | |
| 77 | FPGA_TCK | K27 | 78 | PHY1_RXCTL | L30 |

| | | | | | |
|---|---|---|---|---|---|
| 79 | FPGA_TDI | J27 | 80 | PHY1_RXCK | K31 |
| 81 | FPGA_TMS | H28 | 82 | PHY1_MDC | L33 |
| 83 | FPGA_TDO | G28 | 84 | PHY1_MDIO | L34 |
| 85 | GND | | 86 | GND | |
| 87 | 505_RX3_N | N34 | 88 | 505_TX3_N | N30 |
| 89 | 505_RX3_P | N33 | 90 | 505_TX3_P | N29 |
| 91 | GND | - | 92 | GND | - |
| 93 | 505_RX2_N | R34 | 94 | 505_TX2_N | P32 |
| 95 | 505_RX2_P | R33 | 96 | 505_TX2_P | P31 |
| 97 | GND | | 98 | GND | |
| 99 | 505_RX1_N | T32 | 100 | 505_TX1_N | R30 |
| 101 | 505_RX1_P | T31 | 102 | 505_TX1_P | R29 |
| 103 | GND | | 104 | GND | |
| 105 | 505_RX0_N | U34 | 106 | 505_TX0_N | U30 |
| 107 | 505_RX0_P | U33 | 108 | 505_TX0_P | U29 |
| 109 | GND | | 110 | GND | |
| 111 | 505_CLK0_N | T28 | 112 | 505_CLK1_N | P28 |
| 113 | 505_CLK0_P | T27 | 114 | 505_CLK1_P | P27 |
| 115 | GND | | 116 | GND | |
| 117 | 505_CLK2_N | M28 | 118 | 505_CLK3_N | M32 |
| 119 | 505_CLK2_P | M27 | 120 | 505_CLK3_P | M31 |

## Pin assignment of board to board connector J31

J31 connects the IO of BANK64, BANK65, the level standard of BANK66, 67 is +1.8V.

| J31 Pin | Signal Name | Pin Number | J31 Pin | Signal Name | Pin Number |
|---|---|---|---|---|---|
| 1 | POWER_SW | | 2 | VBAT_IN | Y23 |
| 3 | B65_L24_N | AA20 | 4 | B65_L2_N | AN19 |
| 5 | B65_L24_P | AA19 | 6 | B65_L2_P | AM19 |
| 7 | B65_L13_N | AH23 | 8 | B65_L18_N | AE24 |
| 9 | B65_L13_P | AH22 | 10 | B65_L18_P | AE23 |
| 11 | GND | | 12 | GND | |
| 13 | B65_L8_N | AL23 | 14 | B65_L16_N | AG23 |
| 15 | B65_L8_P | AL22 | 16 | B65_L16_P | AF23 |

| | | | | | |
|---|---|---|---|---|---|
| 17 | B65_L12_N | AJ22 | 18 | B65_L3_N | AP22 |
| 19 | B65_L12_P | AJ21 | 20 | B65_L3_P | AP21 |
| 21 | GND | | 22 | GND | |
| 23 | B65_L5_N | AP23 | 24 | B65_L7_N | AL21 |
| 25 | B65_L5_P | AN22 | 26 | B65_L7_P | AL20 |
| 27 | B65_L10_N | AK23 | 28 | B65_L21_N | AE20 |
| 29 | B65_L10_P | AK22 | 30 | B65_L21_P | AD20 |
| 31 | GND | | 32 | GND | |
| 33 | B65_L14_N | AH21 | 34 | B65_L6_N | AN23 |
| 35 | B65_L14_P | AG21 | 36 | B65_L6_P | AM23 |
| 37 | B65_L19_N | AE19 | 38 | B65_L17_N | AF22 |
| 39 | B65_L19_P | AE18 | 40 | B65_L17_P | AF21 |
| 41 | GND | | 42 | GND | |
| 43 | B65_L15_N | AG20 | 44 | B65_L4_N | AN21 |
| 45 | B65_L15_P | AG19 | 46 | B65_L4_P | AM21 |
| 47 | B65_L20_N | AC19 | 48 | B65_L11_N | AK20 |
| 49 | B65_L20_P | AB19 | 50 | B65_L11_P | AJ20 |
| 51 | GND | | 52 | GND | |
| 53 | B65_L23_N | AD19 | 54 | B65_L1_N | AP20 |
| 55 | B65_L23_P | AC18 | 56 | B65_L1_P | AP19 |
| 57 | B65_L22_N | AB18 | 58 | B65_L9_N | AK19 |
| 59 | B65_L22_P | AA18 | 60 | B65_L9_P | AJ19 |
| 61 | GND | | 62 | GND | |
| 63 | B64_L1_P | AP18 | 64 | B64_L9_P | AK18 |
| 65 | B64_L1_N | AP17 | 66 | B64_L9_N | AL18 |
| 67 | B64_L6_P | AN17 | 68 | B64_L14_P | AF18 |
| 69 | B64_L6_N | AN16 | 70 | B64_L14_N | AG18 |
| 71 | GND | | 72 | GND | |
| 73 | B64_L5_P | AP16 | 74 | B64_L11_P | AJ17 |
| 75 | B64_L5_N | AP15 | 76 | B64_L11_N | AK17 |
| 77 | B64_L3_P | AM18 | 78 | B64_L4_P | AM14 |
| 79 | B64_L3_N | AN18 | 80 | B64_L4_N | AN14 |
| 81 | GND | | 82 | GND | |
| 83 | B64_L24_P | AD17 | 84 | B64_L2_P | AN13 |
| 85 | B64_L24_N | AD16 | 86 | B64_L2_N | AP13 |
| 87 | B64_L21_P | AB16 | 88 | B64_L8_P | AL16 |

| | | | | | |
|---|---|---|---|---|---|
| 89 | B64_L21_N | AB15 | 90 | B64_L8_N | AL15 |
| 91 | GND | | 92 | GND | |
| 93 | B64_L7_P | AM16 | 94 | B64_L12_P | AJ16 |
| 95 | B64_L7_N | AM15 | 96 | B64_L12_N | AJ15 |
| 97 | B64_L10_P | AK15 | 98 | B64_L16_P | AH14 |
| 99 | B64_L10_N | AK14 | 100 | B64_L16_N | AJ14 |
| 101 | GND | | 102 | GND | |
| 103 | B64_L20_P | AC17 | 104 | B64_L15_P | AE17 |
| 105 | B64_L20_N | AC16 | 106 | B64_L15_N | AF17 |
| 107 | B64_L18_P | AG15 | 108 | B64_L17_P | AF16 |
| 109 | B64_L18_N | AG14 | 110 | B64_L17_N | AF15 |
| 111 | GND | | 112 | GND | |
| 113 | B64_L22_P | AA16 | 114 | B64_L19_P | AD15 |
| 115 | B64_L22_N | AA15 | 116 | B64_L19_N | AE15 |
| 117 | B64_L13_P | AH18 | 118 | B64_L23_P | AA14 |
| 119 | B64_L13_N | AH17 | 120 | B64_L23_N | AB14 |

## Pin assignment of board to board connector J32

J32 connects to the the transceiver signal of BANK223, 224, 225,226

| J32 Pin | Signal Name | Pin Number | J32 Pin | Signal Name | Pin Number |
|---|---|---|---|---|---|
| 1 | 223_RX0_P | AP4 | 2 | 223_TX0_P | AN6 |
| 3 | 223_RX0_N | AP3 | 4 | 223_TX0_N | AN5 |
| 5 | GND | | 6 | GND | |
| 7 | 223_RX1_P | AN2 | 8 | 223_TX1_P | AM4 |
| 9 | 223_RX1_N | AN1 | 10 | 223_TX1_N | AM3 |
| 11 | GND | | 12 | GND | |
| 13 | 223_RX2_P | AL2 | 14 | 223_TX2_P | AL6 |
| 15 | 223_RX2_N | AL1 | 16 | 223_TX2_N | AL5 |
| 17 | GND | | 18 | GND | |
| 19 | 223_RX3_P | AK4 | 20 | 223_TX3_P | AJ6 |
| 21 | 223_RX3_N | AK3 | 22 | 223_TX3_N | AJ5 |
| 23 | GND | | 24 | GND | |
| 25 | 223_CLK1_P | AC10 | 26 | 223_CLK0_P | AD8 |
| 27 | 223_CLK1_N | AC9 | 28 | 223_CLK0_N | AD7 |
| 29 | GND | | 30 | GND | |

| | | | | | |
|---|---|---|---|---|---|
| 31 | 224_RX0_P | AJ2 | 32 | 224_TX0_P | AH4 |
| 33 | 224_RX0_N | AJ1 | 34 | 224_TX0_N | AH3 |
| 35 | GND | | 36 | GND | |
| 37 | 224_RX1_P | AG2 | 38 | 224_TX1_P | AG6 |
| 39 | 224_RX1_N | AG1 | 40 | 224_TX1_N | AG5 |
| 41 | GND | | 42 | GND | |
| 43 | 224_RX2_P | AF4 | 44 | 224_TX2_P | AE6 |
| 45 | 224_RX2_N | AF3 | 46 | 224_TX2_N | AE5 |
| 47 | GND | | 48 | GND | |
| 49 | 224_RX3_P | AE2 | 50 | 224_TX3_P | AD4 |
| 51 | 224_RX3_N | AE1 | 52 | 224_TX3_N | AD3 |
| 53 | GND | | 54 | GND | |
| 55 | 224_CLK1_P | AA10 | 56 | 224_CLK0_P | AB8 |
| 57 | 224_CLK1_N | AA9 | 58 | 224_CLK0_N | AB7 |
| 59 | GND | | 60 | GND | |
| 61 | 225_CLK1_P | W10 | 62 | 225_CLK0_P | Y8 |
| 63 | 225_CLK1_N | W9 | 64 | 225_CLK0_N | Y7 |
| 65 | GND | | 66 | GND | |
| 67 | 225_RX1_P | AB4 | 68 | 225_RX0_P | AC2 |
| 69 | 225_RX1_N | AB3 | 70 | 225_RX0_N | AC1 |
| 71 | GND | | 72 | GND | |
| 73 | 225_TX1_P | AA6 | 74 | 225_TX0_P | AC6 |
| 75 | 225_TX1_N | AA5 | 76 | 225_TX0_N | AC5 |
| 77 | GND | | 78 | GND | |
| 79 | 225_RX2_P | AA2 | 80 | 225_RX3_P | W2 |
| 81 | 225_RX2_N | AA1 | 82 | 225_RX3_N | W1 |
| 83 | GND | | 84 | GND | |
| 85 | 225_TX2_P | Y4 | 86 | 225_TX3_P | W6 |
| 87 | 225_TX2_N | Y3 | 88 | 225_TX3_N | W5 |
| 89 | GND | | 90 | GND | |
| 91 | 226_CLK0_P | V8 | 92 | 226_CLK1_P | U10 |
| 93 | 226_CLK0_N | V7 | 94 | 226_CLK1_N | U9 |
| 95 | GND | | 96 | GND | |
| 97 | 226_RX3_P | P4 | 98 | 226_TX3_P | N6 |
| 99 | 226_RX3_N | P3 | 100 | 226_TX3_N | N5 |
| 101 | GND | | 102 | GND | |

| | | | | | |
|---|---|---|---|---|---|
| 103 | 226_RX2_P | R2 | 104 | 226_TX2_P | R6 |
| 105 | 226_RX2_N | R1 | 106 | 226_TX2_N | R5 |
| 107 | GND | | 108 | GND | |
| 109 | 226_RX1_P | U2 | 110 | 226_TX1_P | T4 |
| 111 | 226_RX1_N | U1 | 112 | 226_TX1_N | T3 |
| 113 | GND | | 114 | GND | |
| 115 | 226_RX0_P | V4 | 116 | 226_TX0_P | U6 |
| 117 | 226_RX0_N | V3 | 118 | 226_TX0_N | U5 |
| 119 | GND | | 120 | GND | |

# Part 3: Carrier Board

## Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- PCIe x8 interface
- 1-Channel M.2 interface
- 1-Channel DP output interface
- 4 USB 3.0 Interfaces
- 1-Channel HDMI video output interface
- 1-Channel HDMI video input interface
- 2-Channel 10/100M/1000M Ethernet RJ-45 interface
- 2-Channel USB Uart Interfaces
- 2 SFP Interface
- 1-Channel Micro SD card slot
- 1-Channel MIPI camera interface
- 1-Channel FMC interface
- 2-Channel CAN communication interfaces
- 2-Channel 485 communication interfaces
- JTAG debugging interface
- 1-Channel temperature sensor
- 1-Channel EEPROM
- 1-Channel RTC real-time clock
- 2 LED lights
- 2 Keys

## Part 3.2: PCIe Slot

There is a PCIe3.0 x8 interface on the AXU7EV carrier board, and eight pairs of transceivers are connected to the PCIEx8, which can realize PCIe x 8,

PCIe x 4, PCIe x 2, PCIe x 2 data communication.

The transceiver signal of the PCIe interface is directly connected to the GTH transceiver of FPGA BANK223, BANK224, and the single-channel communication rate can be as high as 8G bit bandwidth.

The PCIe interface schematic is shown in Figure 3-2-1 below, where the TX signal is connected in AC coupling mode.

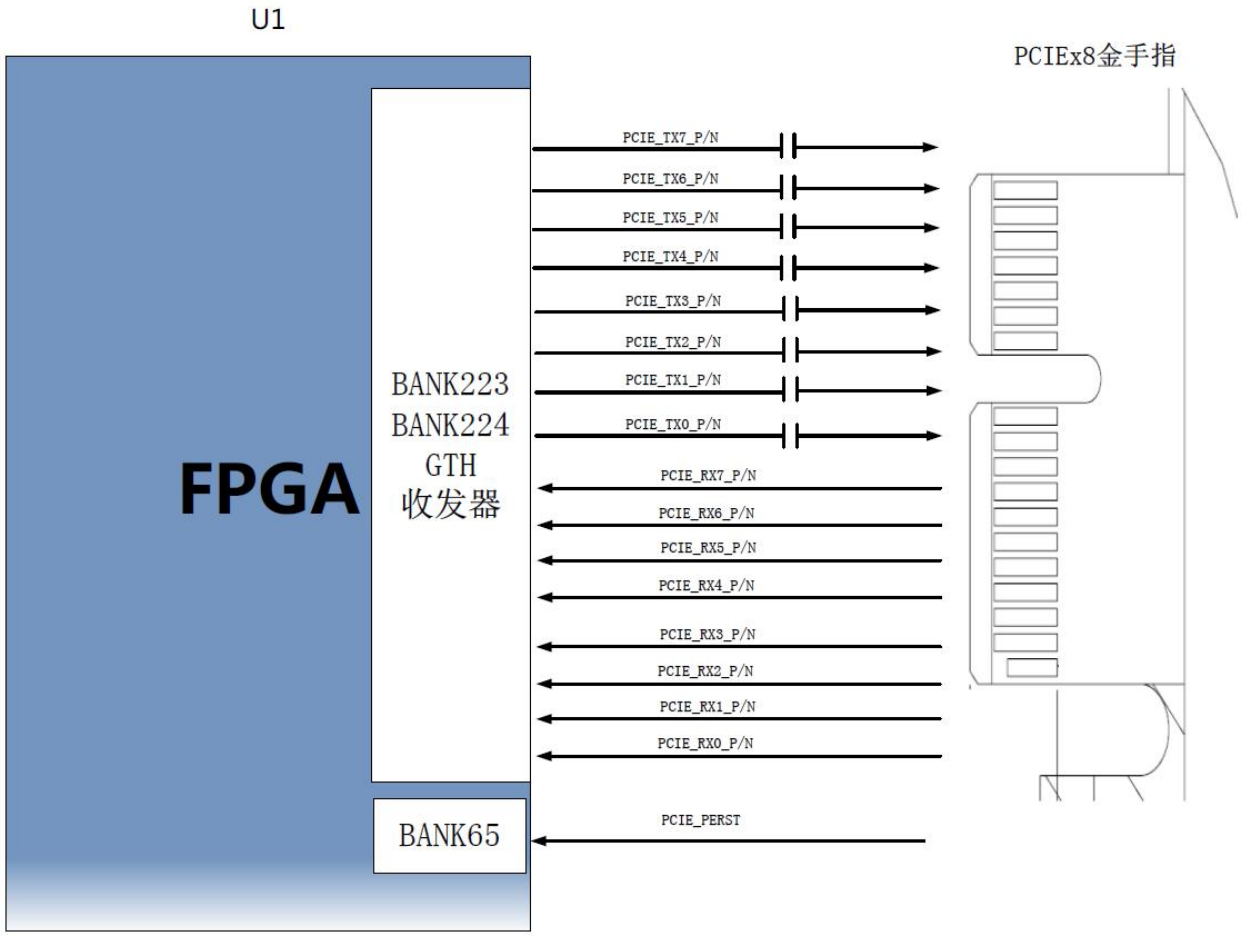



Figure 3-2-1: PCIe Interface Schematic

## PCIe x8 Interface FPGA Pin Assignment

| Signal Name | FPGA Pin Name | Pin Number | Description |
|---|---|---|---|
| PCIE_RX0_N | 223_RX0_N | AP3 | PCIE Channel 0 Data Receive Negative |
| PCIE_RX0_P | 223_RX0_P | AP4 | PCIE Channel 0 Data Receive Positive |
| PCIE_RX1_N | 223_RX1_N | AN1 | PCIE Channel 1 Data Receive Negative |
| PCIE_RX1_P | 223_RX1_P | AN2 | PCIE Channel 1 Data Receive Positive |

| | | | |
|---|---|---|---|
| PCIE_RX2_N | 223_RX2_N | AL1 | PCIE Channel 2 Data Receive Negative |
| PCIE_RX2_P | 223_RX2_P | AL2 | PCIE Channel 2 Data Receive Positive |
| PCIE_RX3_N | 223_RX3_N | AK3 | PCIE Channel 3 Data Receive Negative |
| PCIE_RX3_P | 223_RX3_P | AK4 | PCIE Channel 3 Data Receive Positive |
| PCIE_RX4_N | 224_RX0_N | AJ1 | PCIE Channel 4 Data Receive Negative |
| PCIE_RX4_P | 224_RX0_P | AJ2 | PCIE Channel 4 Data Receive Positive |
| PCIE_RX5_N | 224_RX1_N | AG1 | PCIE Channel 5 Data Receive Negative |
| PCIE_RX5_P | 224_RX1_P | AG2 | PCIE Channel 5 Data Receive Positive |
| PCIE_RX6_N | 224_RX2_N | AF3 | PCIE Channel 6 Data Receive Negative |
| PCIE_RX6_P | 224_RX2_P | AF4 | PCIE Channel 6 Data Receive Positive |
| PCIE_RX7_N | 224_RX3_N | AE1 | PCIE Channel 7 Data Receive Negative |
| PCIE_RX7_P | 224_RX3_P | AE2 | PCIE Channel 7 Data Receive Positive |
| PCIE_TX0_N | 223_TX0_N | AN5 | PCIE Channel 0 Data Receive Negative |
| PCIE_TX0_P | 223_TX0_P | AN6 | PCIE Channel 0 Data Receive Positive |
| PCIE_TX1_N | 223_TX1_N | AM3 | PCIE Channel 1 Data Receive Negative |
| PCIE_TX1_P | 223_TX1_P | AM4 | PCIE Channel 1 Data Receive Positive |
| PCIE_TX2_N | 223_TX2_N | AL5 | PCIE Channel 2 Data Receive Negative |
| PCIE_TX2_P | 223_TX2_P | AL6 | PCIE Channel 2 Data Receive Positive |
| PCIE_TX3_N | 223_TX3_N | AJ5 | PCIE Channel 3 Data Receive Negative |
| PCIE_TX3_P | 223_TX3_P | AJ6 | PCIE Channel 3 Data Receive Positive |
| PCIE_TX4_N | 224_TX0_N | AH3 | PCIE Channel 4 Data Receive Negative |
| PCIE_TX4_P | 224_TX0_P | AH4 | PCIE Channel 4 Data Receive Positive |
| PCIE_TX5_N | 224_TX1_N | AG5 | PCIE Channel 5 Data Receive Negative |
| PCIE_TX5_P | 224_TX1_P | AG6 | PCIE Channel 5 Data Receive Positive |
| PCIE_TX6_N | 224_TX2_N | AE5 | PCIE Channel 6 Data Receive Negative |
| PCIE_TX6_P | 224_TX2_P | AE6 | PCIE Channel 6 Data Receive Positive |
| PCIE_TX7_N | 224_TX3_N | AD3 | PCIE Channel 7 Data Receive Negative |
| PCIE_TX7_P | 224_TX3_P | AD4 | PCIE Channel 7 Data Receive Positive |
| PCIE_CLK_N | 223_CLK0_N | AD7 | PCIE Channel Reference Clock Negative |
| PCIE_CLK_P | 223_CLK0_P | AD8 | PCIE Channel Reference Clock Positive |
| PCIE_RSTN | B65_L24_N | AA20 | The Reset Signal of the PCIE Board |

## Part 3.3: M.2 Interface

The AXU7EV FPGA development board is equipped with a PCIE x1 standard M.2 interface for connecting M.2 SSD solid state drives, with a communication speed of up to 6Gbps. The M.2 interface uses the M key slot, which only supports PCI-E, not SATA. When users choose SSD solid state drives, they need to choose PCIE type SSD solid state drives.

The PCIE signal is directly connected to the BANK505 PS MGT transceiver of ZU7EV, and the TX signal and RX signal of one channel are connected to the LANE1 of MGT in a differential signal mode. The PCIE clock is provided by the Si5332 chip, the frequency is 100Mhz, and the schematic diagram of the M.2 circuit design is shown in Figure 3-2-1:

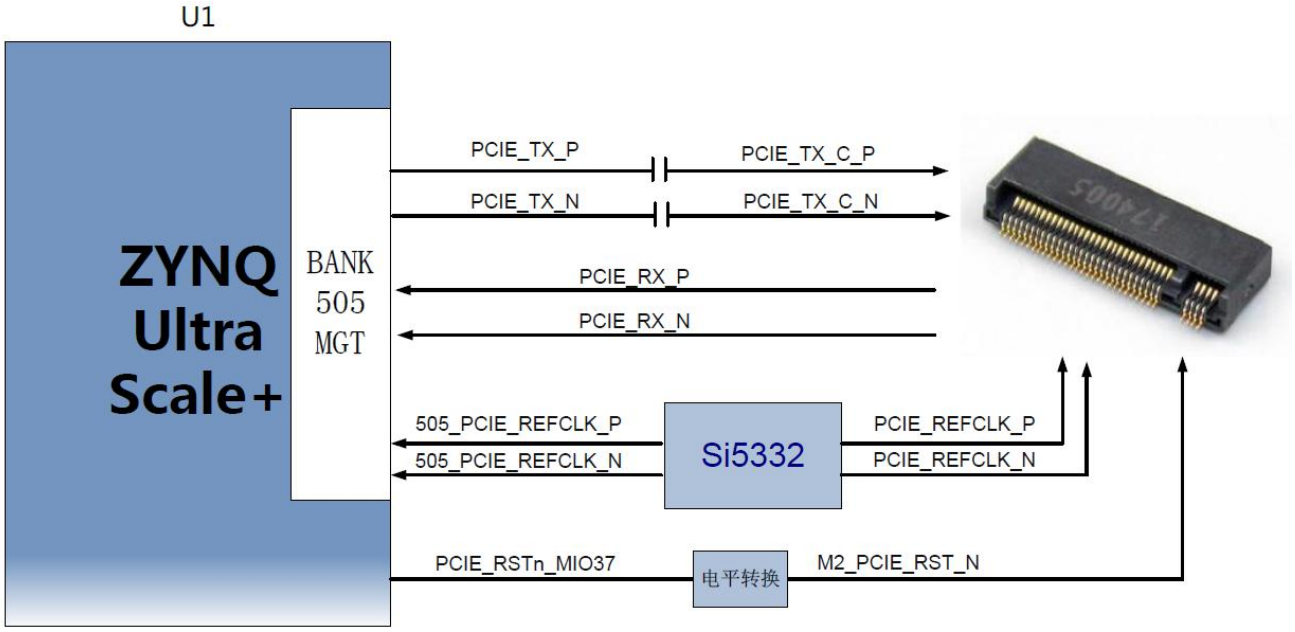



Figure 3-3-1: M.2 Interface Schematic

**The pin assignment of M.2 interface ZYNQ is as follows:**

| Signal Name | Pin Name | Pin Number | Description |
|---|---|---|---|
| PCIE_TX_N | 505_TX0_N | U30 | PCIE Data Transmit Positive |
| PCIE_TX_P | 505_TX0_P | U29 | PCIE Data Transmit Negative |
| PCIE_RX_N | 505_RX0_N | U34 | PCIE Data Receive Positive |
| PCIE_RX_P | 505_RX0_P | U33 | PCIE Data Receive Negative |

| | | | |
|---|---|---|---|
| 505_PCIE_REFCLK_N | 505_CLK0_N | T28 | PCIE Reference Clock Negative |
| 505_PCIE_REFCLK_P | 505_CLK0_P | T27 | PCIE Reference Clock Positive |
| PCIE_RSTN_MIO37 | PS_MIO37 | C33 | PCIE Reset Signal |

## Part 3.4: DP Interface

The AXU7EV FPGA development board has a standard DisplayPort output display interface for video image display. The interface supports VESA DisplayPort V1.2a output standard, up to 4K x 2K@30Fps output, supports Y-only, YCbCr444, YCbCr422, YCbCr420 and RGB video formats, each color supports 6, 8, 10, or 12 bits.

The DisplayPort data transmission channel is directly driven and output by the BANK505 PS MGT of ZU7EV, and the LANE2 and LANE3 TX signals of MGT are connected to the DP connector in a differential signal mode. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. The schematic diagram of the DP output interface design is shown in Figure 3-4-1:

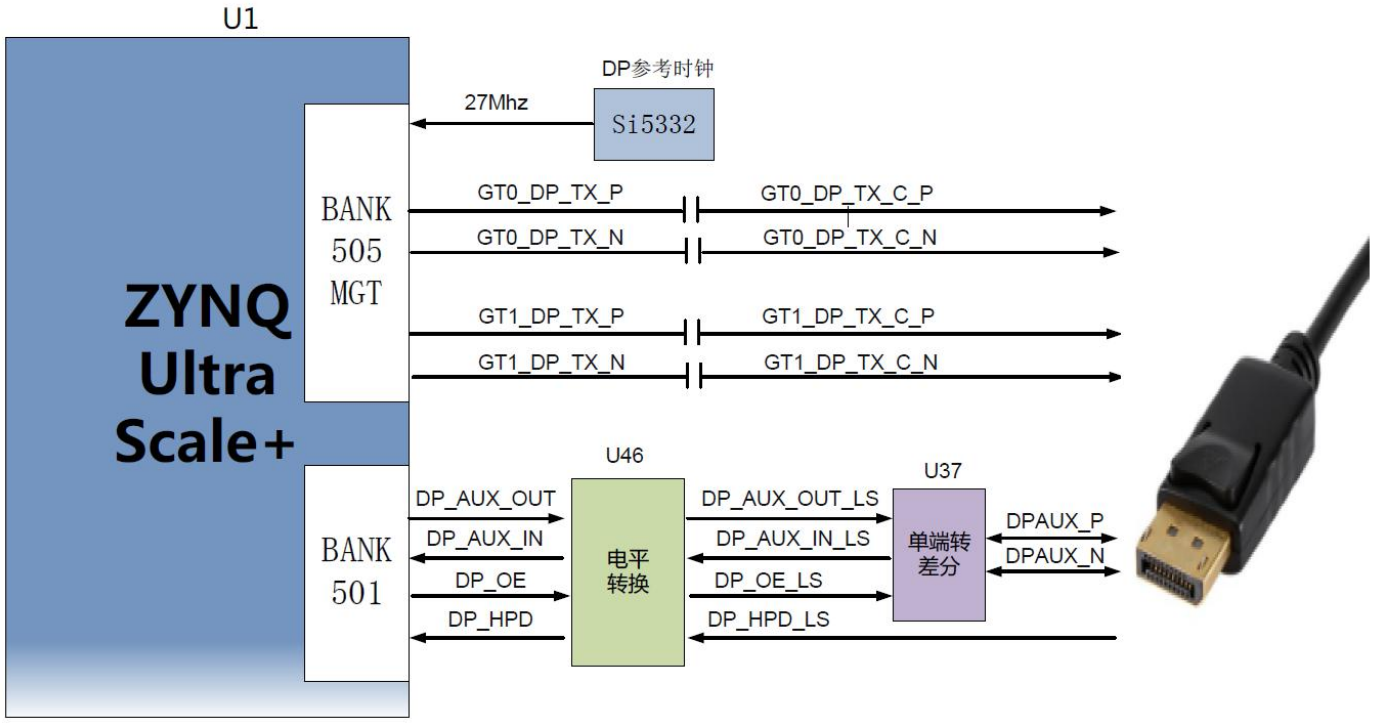



Figure 3-4-1: DP interface design Schematic

**The DisplayPort interface ZYNQ pin assignment is as follows:**

| Signal Name | ZYNQ Pin Number | ZYNQ Pin Number | Description |
|---|---|---|---|
| GT0_DP_TX_N | 505_TX3_N | N30 | Low bits of DP Data Transmit Negative |
| GT0_DP_TX_P | 505_TX3_P | N29 | Low bits of DP Data Transmit Positive |
| GT1_DP_TX_N | 505_TX2_N | P32 | High bits of DP Data Transmit Negative |
| GT1_DP_TX_P | 505_TX2_P | P31 | High bits of DP Data Transmit Positive |
| 505_DP_CLKN | 505_CLK2_N | M28 | DP Reference Clock Positive |
| 505_DP_CLKP | 505_CLK2_P | M27 | DP Reference Clock Negative |
| DP_AUX_OUT_MIO27 | PS_MIO27 | A30 | DP Auxiliary Data Output |
| DP_AUX_IN_MIO30 | PS_MIO30 | A33 | DP Auxiliary Data Input |
| DP_OE_MIO29 | PS_MIO29 | A32 | DP Auxiliary Data Output Enable |
| DP_HPD_MIO28 | PS_MIO28 | A31 | DP Insertion Signal Detection |

## Part 3.5: USB3.0 Interface

There are 4 USB3.0 ports on the AXU7EV carrier board, supporting the HOST working mode, and the data transmission speed is up to 5.0Gb/s. USB3.0 is connected through the PIPE3 interface, and USB2.0 is connected to the external USB3320C chip through the ULPI interface to realize high-speed USB3.0 and USB2.0 data communication.

The USB interface is a flat USB interface (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse, keyboard or U disk) at the same time. The schematic diagram of USB3.0 connection is shown as 3-5-1:

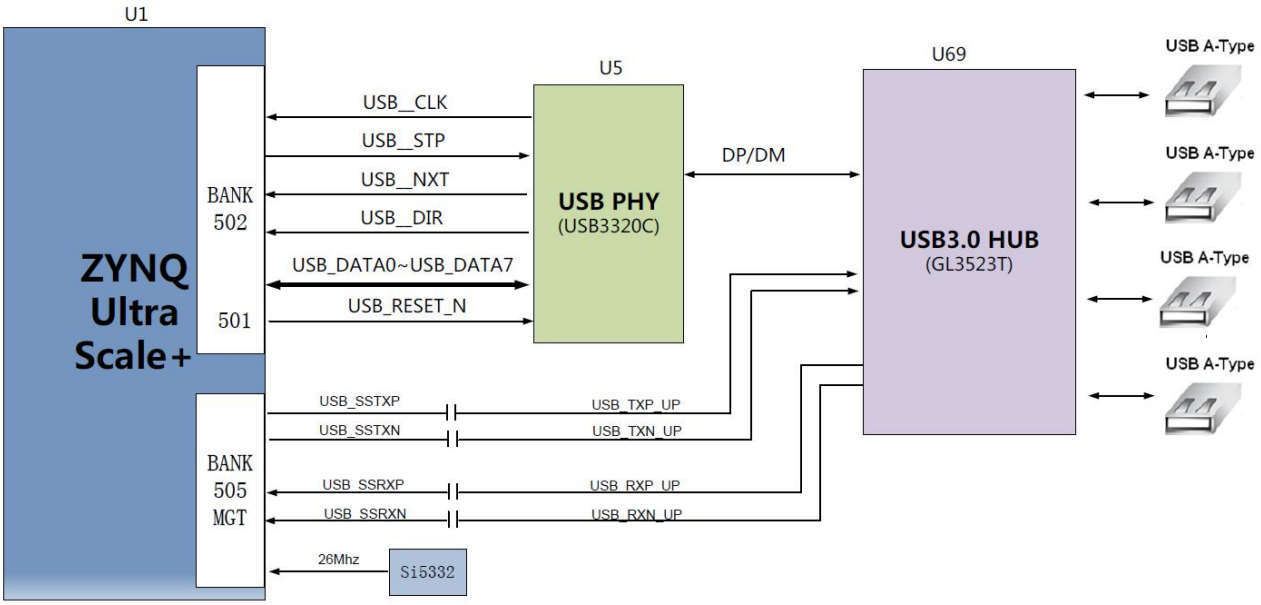



Figure 3-4-1: USB3.0 Interface Schematic

## USB Interface Pin Assignment:

| Signal Name | Pin Name | Pin Number | Description |
|---|---|---|---|
| USB_SSTXP | 505_TX1_N | R30 | USB3.0 Data Transmit Positive |
| USB_SSTXN | 505_TX1_P | R29 | USB3.0 Data Transmit Negative |
| USB_SSRXP | 505_RX1_N | T32 | USB3.0 Data Receive Positive |
| USB_SSRXN | 505_RX1_P | T31 | USB3.0 Data Receive Negative |
| USB_DATA0 | USB_DATA0 | G34 | USB2.0 Data Bit0 |
| USB_DATA1 | USB_DATA1 | H29 | USB2.0 Data Bit1 |
| USB_DATA2 | USB_DATA2 | G31 | USB2.0 Data Bit2 |
| USB_DATA3 | USB_DATA3 | H32 | USB2.0 Data Bit3 |
| USB_DATA4 | USB_DATA4 | H33 | USB2.0 Data Bit4 |
| USB_DATA5 | USB_DATA5 | H34 | USB2.0 Data Bit5 |
| USB_DATA6 | USB_DATA6 | J29 | USB2.0 Data Bit6 |
| USB_DATA7 | USB_DATA7 | J30 | USB2.0 Data Bit7 |
| USB_STP | USB_STP | H31 | USB2.0 Stop Signal |
| USB_DIR | USB_DIR | G30 | USB2.0 Data Direction Signal |
| USB_CLK | USB_CLK | G29 | USB2.0 Clock Signal |
| USB_NXT | USB_NXT | G33 | USB2.0 Next Data Signal |
| USB_RESET_N | PS_MIO32 | B31 | USB2.0 Reset Signal |

# Part 3.6: HDMI Output Interface

There is one HDMI Output Interface on the carrier board. The HMDI chip uses TI's SN75DP159 chip to realize the TMDS level conversion redriver and receiver equalization function, and increase the signal driving capability. The HDMI interface supports up to 4K@60Hz output.

The HDMI video output data is connected to the BANK226 GTH transceiver, the clock is connected to BANK64, and the remaining auxiliary channels are connected to BANK88. The hardware connection between SN75DP159RSBR chip and FPGA is shown in Figure 3-6-1:

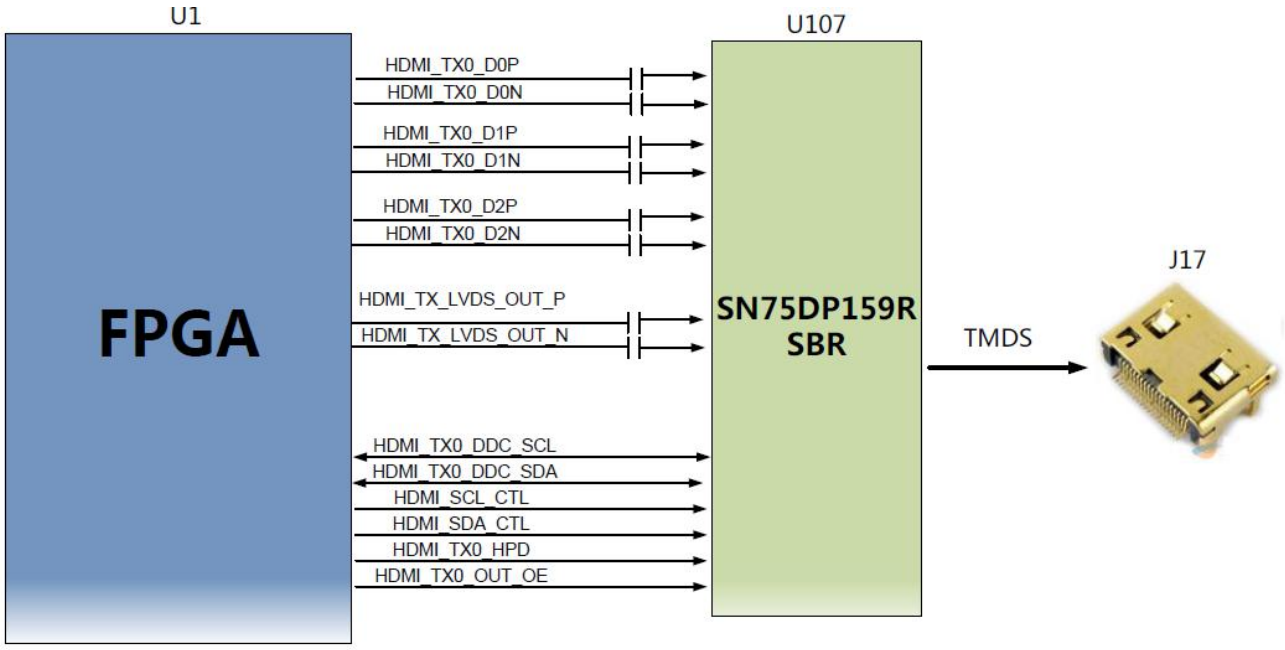



Figure 3-6-1: HDMI Output Interface Schematic

### HDMI Output pin assignment:

| Signal Name | FPGA Pin Name | FPGA Pin Number | Description |
|---|---|---|---|
| HDMI_TX0_D0N | 226_TX0_N | U5 | HDMI Video Output Signal Data 0 Negative |
| HDMI_TX0_D0P | 226_TX0_P | U6 | HDMI Video Output Signal Data 0 Positive |

| | | | |
|---|---|---|---|
| HDMI_TX0_D1N | 226_TX1_N | T3 | HDMI Video Output Signal Data 1 Negative |
| HDMI_TX0_D1P | 226_TX1_P | T4 | HDMI Video Output Signal Data 1 Positive |
| HDMI_TX0_D2N | 226_TX2_N | R5 | HDMI Video Output Signal Data 2 Negative |
| HDMI_TX0_D2P | 226_TX2_P | R6 | HDMI Video Output Signal Data 2 Positive |
| HDMI_TX_LVDS_OUT_N | B64_L13_N | AH17 | HDMI Video Output Clock Negative |
| HDMI_TX_LVDS_OUT_P | B64_L13_P | AH18 | HDMI Video Output Clock Positive |
| HDMI_SCL_CTL | B88_L8_P | E4 | IIC Clock |
| HDMI_SDA_CTL | B88_L8_N | D4 | IIC Data |
| HDMI_TX0_DDC_SCL | B88_L4_N | E2 | TMDS Bidirectional DDC Clock |
| HDMI_TX0_DDC_SDA | B88_L1_P | E1 | TMDS Bidirectional DDC Data |
| HDMI_TX0_HPD | B88_L1_N | D1 | Hot Plug Detection |
| HDMI_TX0_OUT_OE | B88_L4_P | E3 | Operation Enable Pin |

## Part 3.7: HDMI Input Interface

There is 1 HDMI input interface on the carrier board. The HMDI chip uses TI's TMDS181IRGZT, which is a TMDS retimer chip. There is a clock and data recovery (CDR) circuit between the HDMI input port and the output port, supporting data rates up to 6Gbps. The HMDI interface supports up to 4K@60Hz input.

The output end of TMDS181IRGZT is connected to BANK226 GTH transceiver, and the remaining auxiliary channels are connected to BANK88 on the PL end. In addition, there is a PLL clock chip 8T49N241 on the board to generate the clock source required by the HDMI IP. The hardware connection between TMDS181IRGZT chip and FPGA is shown in Figure 3-7-1:

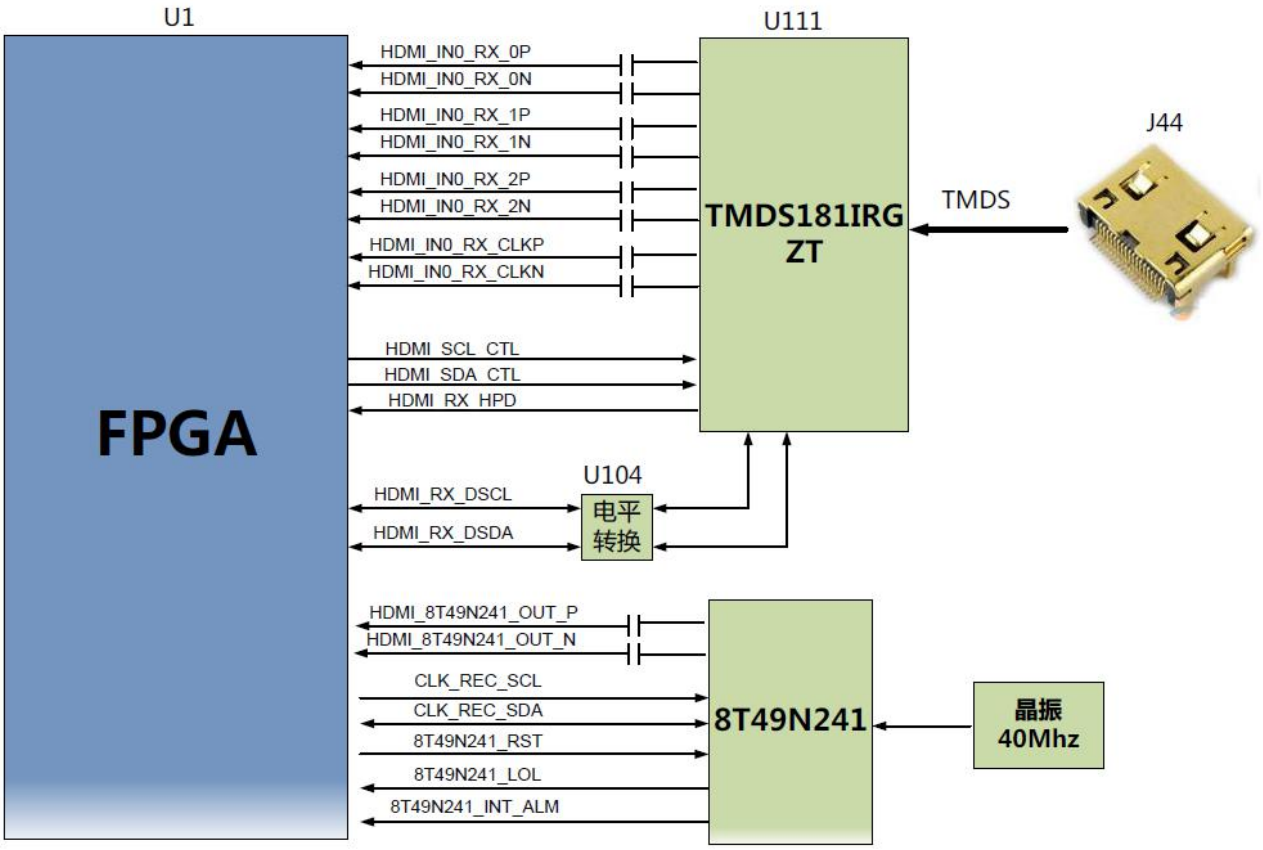



Figure 3-7-1: HDMI Input Interface Schematic

## ZYNQ pin assignment:

| Signal Name | FPGA Pin Name | FPGA Pin Number | Description |
|---|---|---|---|
| HDMI_IN0_RX_0N | 226_RX0_N | V3 | HDMI Video Input Signal Data 0 Negative |
| HDMI_IN0_RX_0P | 226_RX0_P | V4 | HDMI Video Input Signal Data 0 Positive |
| HDMI_IN0_RX_1N | 226_RX1_N | U1 | HDMI Video Input Signal Data 1 Negative |
| HDMI_IN0_RX_1P | 226_RX1_P | U2 | HDMI Video Input Signal Data 1 Positive |
| HDMI_IN0_RX_2N | 226_RX2_N | R1 | HDMI Video Input Signal Data 2 Negative |

| | | | |
|---|---|---|---|
| HDMI_IN0_RX_2P | 226_RX2_P | R2 | HDMI Video Input Signal Data 2 Positive |
| HDMI_IN0_RX_CLKN | 226_CLK0_N | V7 | HDMI Video Input Clock Negative |
| HDMI_IN0_RX_CLKP | 226_CLK0_P | V8 | HDMI Video Input Clock Positive |
| HDMI_SCL_CTL | B88_L8_P | E4 | IIC Clock |
| HDMI_SDA_CTL | B88_L8_N | D4 | IIC Data |
| HDMI_RX_DSCL | B88_L5_N | C2 | TMDS Bidirectional DDC Clock |
| HDMI_RX_DSDA | B88_L2_P | C1 | TMDS Bidirectional DDC Data |
| HDMI_RX_HPD | B88_L2_N | B1 | Hot Plug Detection |
| HDMI_8T49N241_OUT_N | 226_CLK1_N | U9 | PLL Clock Output Negative |
| HDMI_8T49N241_OUT_P | 226_CLK1_P | U10 | PLL Clock Output Positive |
| CLK_REC_SCL | B87_L9_N | J6 | PLL Chip IIC Clock |
| CLK_REC_SDA | B87_L9_P | J7 | PLL Chip IIC Data |
| 8T49N241_INT_ALM | B88_L11_N | D5 | PLL Interrupt Warning Signal |
| 8T49N241_LOL | B88_L11_P | D6 | PLL LOSS Signal |
| 8T49N241_RST | B88_L9_P | F5 | PLL Reset Signal |

## Part 3.8: Gigabit Ethernet Interface

There are 2 Gigabit Ethernet ports on the AXU7EV carrier board, one is connected to the PS end, and the other is connected to the PL end. The GPHY chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide users with network communication services. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate, and communicates with the MAC layer of the ZU7EV system through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and MDIO bus for PHY register management.

When the KSZ9031RNX is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Table 3-8-1 describes the default settings after the GPHY chip is powered on.

| Configuration Pin | Instructions | Configuration value |
|---|---|---|
| PHYAD[2:0] | MDIO/MDC Mode PHY Address | PHY Address 011 |

| | | |
|---|---|---|
| CLK125_EN | Enable 125Mhz clock output selection | Enable |
| LED_MODE | LED light mode configuration | Single LED light mode |
| MODE0~MODE3 | Link adaptation and full duplex configuration | 10/100/1000 adaptive, compatible with full-duplex, half-duplex |

Table 3-8-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

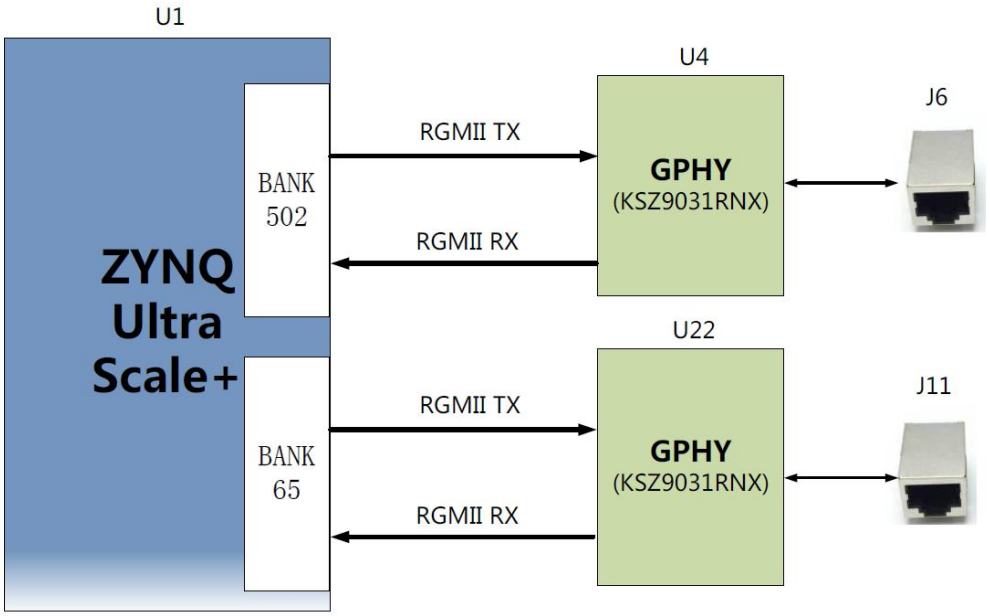



Figure 3-8-1: ZYNQ PS system and GPHY connection diagram

**PS Gigabit Ethernet pin assignment is as follows**

| Signal Name | Pin Name | Pin Number | Description |
|---|---|---|---|
| PHY1_TXCK | PHY1_TXCK | J31 | Ethernet 1 RGMII Transmit Clock |

| | | | |
|---|---|---|---|
| PHY1_TXD0 | PHY1_TXD0 | J32 | Ethernet 1 Transmit data bit0 |
| PHY1_TXD1 | PHY1_TXD1 | J34 | Ethernet 1 Transmit data bit1 |
| PHY1_TXD2 | PHY1_TXD2 | K28 | Ethernet 1 Transmit data bit2 |
| PHY1_TXD3 | PHY1_TXD3 | K29 | Ethernet 1 Transmit data bit3 |
| PHY1_TXCTL | PHY1_TXCTL | K30 | Ethernet 1 Transmit Enable Signal |
| PHY1_RXCK | PHY1_RXCK | K31 | Ethernet 1 RGMII Receive Clock |
| PHY1_RXD0 | PHY1_RXD0 | K32 | Ethernet 1 Receive Data Bit0 |
| PHY1_RXD1 | PHY1_RXD1 | K33 | Ethernet 1 Receive Data Bit1 |
| PHY1_RXD2 | PHY1_RXD2 | K34 | Ethernet 1 Receive Data Bit2 |
| PHY1_RXD3 | PHY1_RXD3 | L29 | Ethernet 1 Receive Data Bit3 |
| PHY1_RXCTL | PHY1_RXCTL | L30 | Ethernet 1 Receive Enable Signal |
| PHY1_MDC | PHY1_MDC | L33 | Ethernet 1 MDIO Clock Management |
| PHY1_MDIO | PHY1_MDIO | L34 | Ethernet 1 MDIO Management Data |

## PL Gigabit Ethernet pin assignment is as follows

| Signal Name | Pin Name | Pin Number | Description |
|---|---|---|---|
| PHY2_TXCK | B65_L14_P | AG21 | Ethernet 2 RGMII Transmit Clock |
| PHY2_TXD0 | B65_L19_P | AE18 | Ethernet 2 Transmit data bit0 |
| PHY2_TXD1 | B65_L19_N | AE19 | Ethernet 2 Transmit data bit1 |
| PHY2_TXD2 | B65_L10_P | AK22 | Ethernet 2 Transmit data bit2 |
| PHY2_TXD3 | B65_L14_N | AH21 | Ethernet 2 Transmit data bit3 |
| PHY2_TXCTL | B65_L10_N | AK23 | Ethernet 2 Transmit Enable Signal |
| PHY2_RXCK | B65_L13_P | AH22 | Ethernet 2 RGMII Receive Clock |
| PHY2_RXD0 | B65_L12_N | AJ22 | Ethernet 2 Receive Data Bit0 |
| PHY2_RXD1 | B65_L12_P | AJ21 | Ethernet 2 Receive Data Bit1 |
| PHY2_RXD2 | B65_L5_N | AP23 | Ethernet 2 Receive Data Bit2 |
| PHY2_RXD3 | B65_L5_P | AN22 | Ethernet 2 Receive Data Bit3 |
| PHY2_RXCTL | B65_L8_P | AL22 | Ethernet 2 Receive Data Enable Signal |
| PHY2_MDC | B65_L8_N | AL23 | Ethernet 2 MDIO Clock Management |
| PHY2_MDIO | B65_L24_P | AA19 | Ethernet 2 MDIO Management Data |
| PHY2_RESET | B65_L13_N | AH23 | Ethernet 2 Reset Signal |

## Part 3.9: USB to Serial Port

The AXU7EV carrier board is equipped with two Uart to USB ports, one is connected to the PS end, and one is connected to the PL end. The conversion chip uses Silicon Labs CP2102GM's USB-UAR chip, and the USB interface is a MINI USB interface. You can use a USB cable to connect it to the PC's USB port for serial data communication. The schematic diagram of the USB Uart circuit design is shown in the figure below:

The schematic diagram of the USB Uart circuit design is shown in Figure 3-9-1:

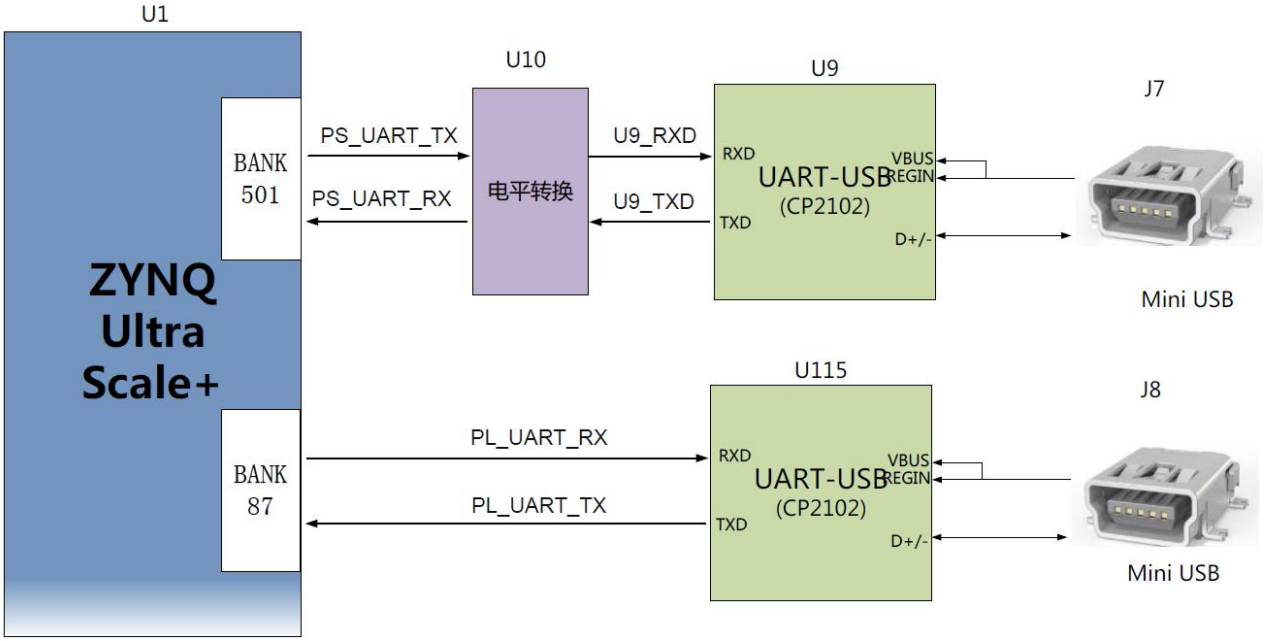



Figure 3-9-1: USB to serial port schematic

**USB to serial port ZYNQ pin assignment:**

| Signal name | Pin Name | Pin Number | Description |
|---|---|---|---|
| PS_UART_TX | PS_MIO42 | D34 | PS Uart Data Input |
| PS_UART_RX | PS_MIO43 | E30 | PS Uart Data Output |
| PL_UART_TX | B87_L2_N | N8 | PL Uart Data Input |
| PL_UART_RX | B87_L2_P | N9 | PL Uart Data Output |

## Part 3.10: SFP Interface

The AXU7EV FPGA carrier board has two optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5G, 10G optical modules on the market) and insert them into these two optical interfaces for optical data communication. The two fiber interfaces are connected to the two RX/TX of the GTH transceivers of ZYNQ BANK225, and the data rate of each TX transmission and RX reception is up to 12.5Gb/s. The reference clock of the GTH transceiver is provided by the 125M differential clock of the core board.

The SFP Schematic detailed is shown in Figure 3-10-1:

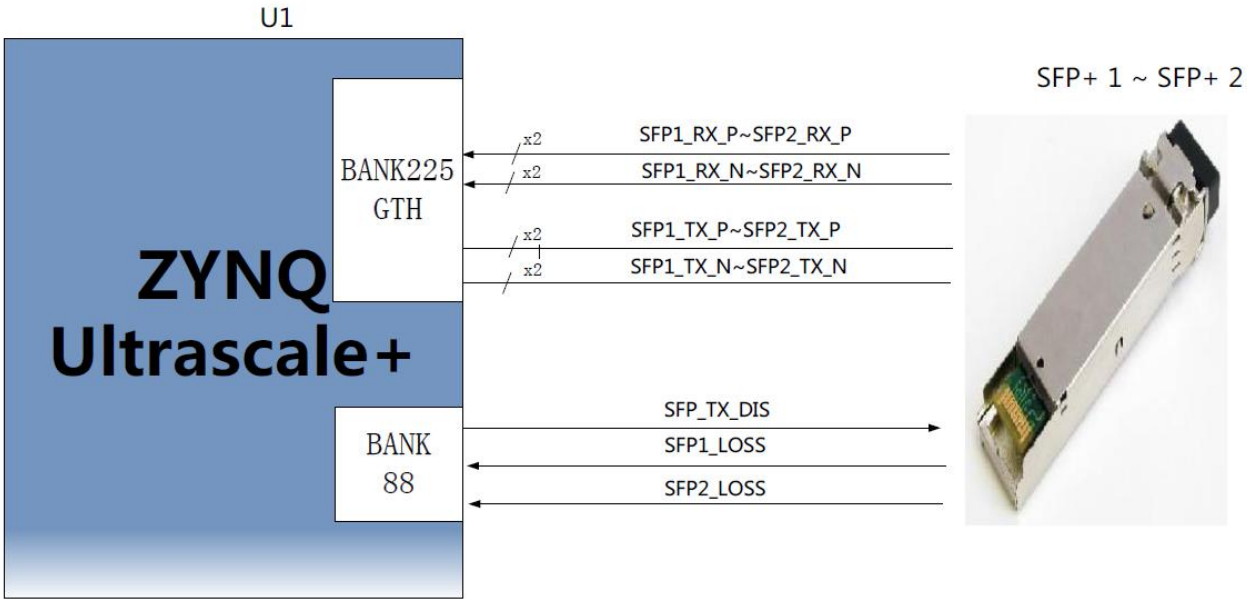



Figure 3-10-1: SFP Schematic

### SFP ZYNQ pin assignment:

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| SFP1_TX_N | 225_TX0_N | AC5 | Optical Module 1 Data Transmit Negative |
| SFP1_TX_P | 225_TX0_P | AC6 | Optical Module 1 Data Transmit Positive |
| SFP1_RX_N | 225_RX0_N | AC1 | Optical Module 1 Data Receive Negative |
| SFP1_RX_P | 225_RX0_P | AC2 | Optical Module 1 Data Receive Positive |

| | | | |
|---|---|---|---|
| SFP2_TX_N | 225_TX3_N | W5 | Optical Module 2 Data Transmit Negative |
| SFP2_TX_P | 225_TX3_P | W6 | Optical Module 2 Data Transmit Positive |
| SFP2_RX_N | 225_RX3_N | W1 | Optical Module 2 Data Receive Negative |
| SFP2_RX_P | 225_RX3_P | W2 | Optical Module 2 Data Receive Positive |
| SFP_TX_DIS | B88_L3_N | A2 | Optical Module Light Emission Prohibited, High Level (Positive) Enable |
| SFP1_LOSS | B88_L7_P | C4 | Optical Module 1 Receive LOSS Detect Signal |
| SFP2_LOSS | B88_L7_N | B4 | Optical Module 2 Receive LOSS Detect Signal |

## Part 3.11: SD Card Slot Interface

The AXU7EV FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZU7EV chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZU7EV. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the ZU7EV PS and SD card connector is shown in Figure 3-11-1:

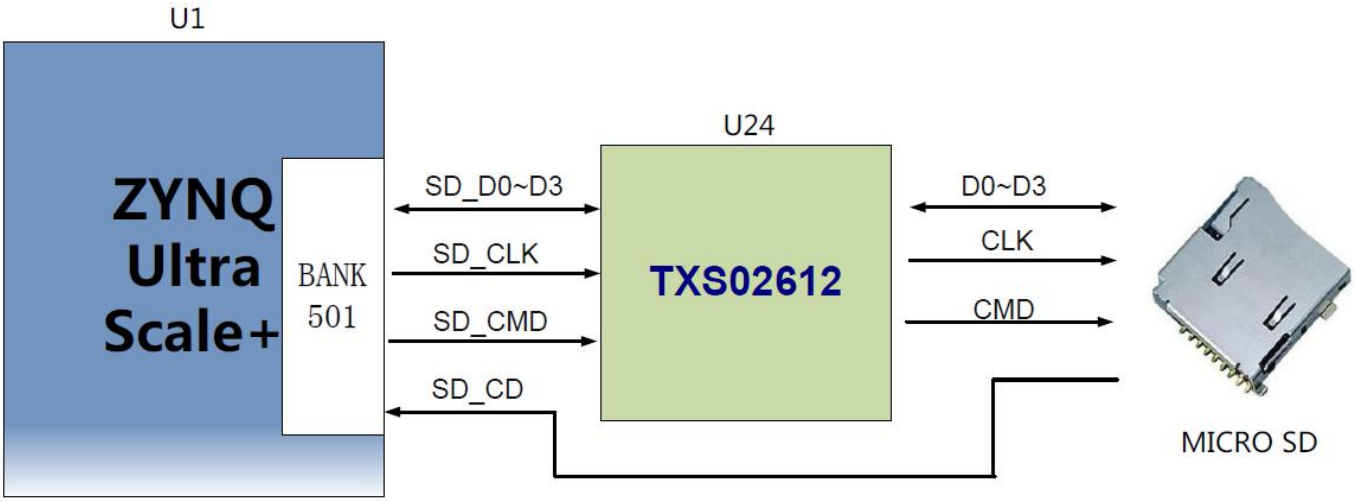



Figure 3-11-1: SD Card Connection Diagram

**SD card slot pin assignment:**

| Signal Name | Pin Name | Pin Number | Description |
|---|---|---|---|
| SD_CLK | SD_CLK | F34 | SD Clock Signal |
| SD_CD | SD_CD | E33 | SD Command Signal |
| SD_D0 | SD_D0 | E34 | SD Data0 |
| SD_D1 | SD_D1 | F30 | SD Data1 |
| SD_D2 | SD_D2 | F31 | SD Data2 |
| SD_D3 | SD_D3 | F32 | SD Data3 |
| SD_CMD | SD_CMD | F33 | SD card insertion signal |

## Part 3.12: MIPI Camera Interface

The AXU7EV carrier board includes a MIPI camera interface, which can be used to connect with the ALINX Brand MIPI OV5640 camera module AN5641. MIPI interface 15PIN FPC connector, 2 LANE data and 1 pair of clock, connected to the differential IO pin of BANK65. other control signals are connected to the IO of BANK87.

The circuit schematic of the MIPI interface part is shown in Figure 3-12-1 below:

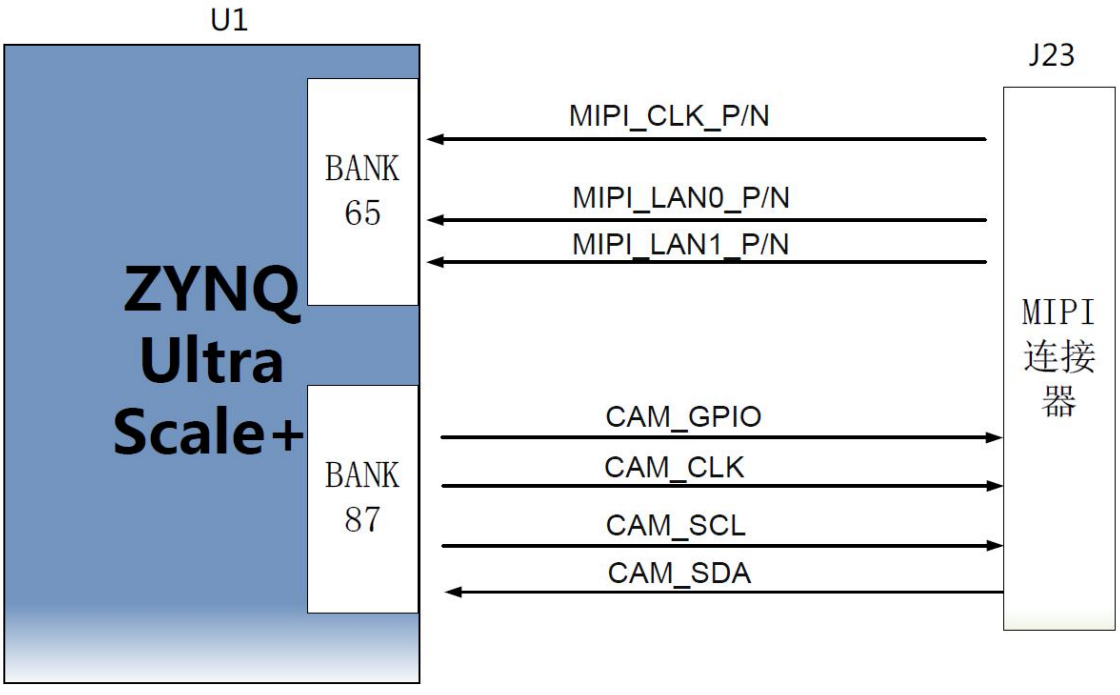



Figure 3-12-1: MIPI camera interface design schematic

**MIPI interface pin assignment**

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| MIPI_CLK_N | B65_L1_N | AP20 | MIPI Input Clock Positive |
| MIPI_CLK_P | B65_L1_P | AP19 | MIPI Input Clock Negative |
| MIPI_LAN0_N | B65_L2_N | AN19 | MIPI Input Date LANE0 Negative |
| MIPI_LAN0_P | B65_L2_P | AM19 | MIPI Input Date LANE0 Positive |
| MIPI_LAN1_N | B65_L3_N | AP22 | MIPI Input Date LANE1 Negative |
| MIPI_LAN1_P | B65_3_P | AP21 | MIPI Input Date LANE1 Positive |
| CAM_GPIO | B87_L5_N | M8 | GPIO Control of Camera |
| CAM_CLK | B87_L5_P | M9 | Clock Input of Camera |
| CAM_SCL | B87_L11_P | H7 | I2C Clock of Camera |
| CAM_SDA | B87_L11_N | G7 | I2C Data of Camera |

# Part 3.13: FMC Interface

The AXU7EV FPGA Carrier board has a standard FMC LPC expansion port that can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 36 pairs of differential IO signals and 8 pairs of GTX Transceivers.

The 36 pairs of differential signals of the FMC expansion port are connected to the IO of the BANK28 and BANK64 of the ZYNQ Ultrascale+ chip. The level standard is 1.8V, and the differential signal supports LVDS data communication, 2 pairs of GTX transceiver signals are connected to BANK225. The schematic diagram of ZYNQ Ultrascale+ and FMC connectors is shown in Figure 3-13-1.

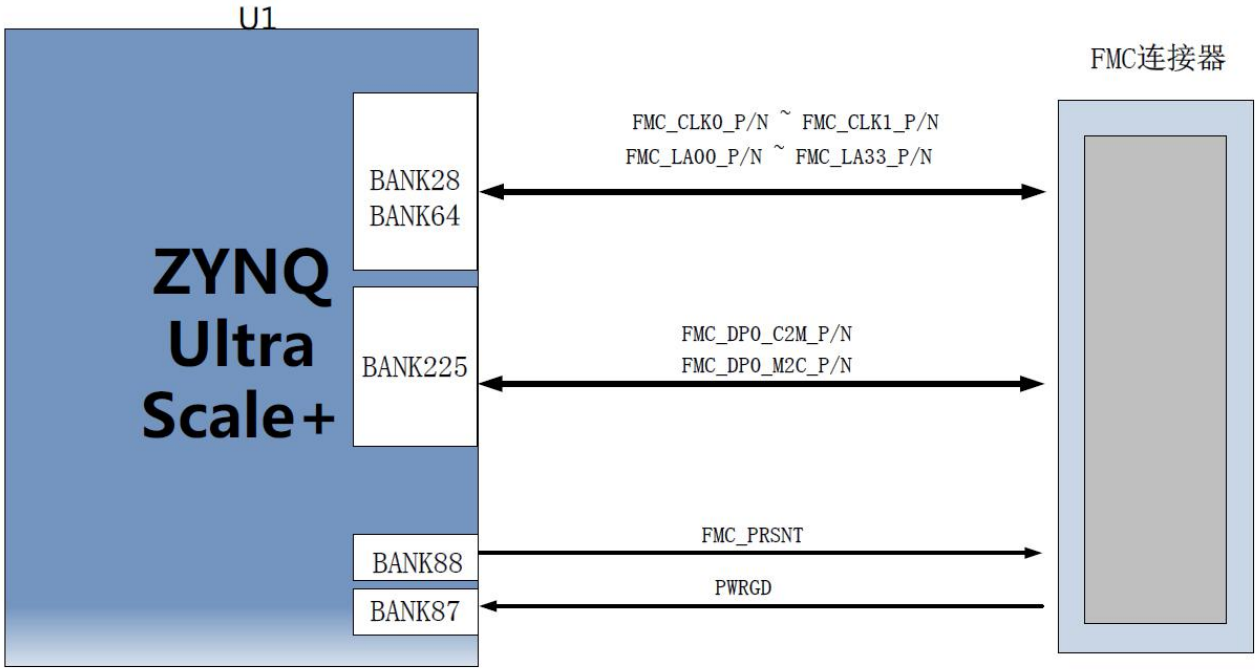



Figure 3-13-1: FMC Schematic

## FMC connector pin assignment

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| FMC_DP0_C2M_N | 225_TX1_N | AA5 | FMC Transceiver Data Transmission 0 Negative |
| FMC_DP0_C2M_P | 225_TX1_P | AA6 | FMC Transceiver Data Transmission 0 Positive |
| FMC_DP0_M2C_N | 225_RX1_N | AB3 | FMC Transceiver Data Receive 0 Negative |
| FMC_DP0_M2C_P | 225_RX1_P | AB4 | FMC Transceiver Data Receive 0 Positive |
| FMC_CLK0_N | B28_L11_N | E22 | FMC Reference 1st Clock Negative |
| FMC_CLK0_P | B28_L11_P | F22 | FMC Reference 1st Clock Positive |
| FMC_CLK1_N | B64_L14_N | AG18 | FMC Reference 2nd Clock Negative |
| FMC_CLK1_P | B64_L14_P | AF18 | FMC Reference 2nd Clock Positive |
| FMC_LA00_CC_N | B28_L13_N | E23 | FMC Reference 0th Data ( Clock ) N |
| FMC_LA00_CC_P | B28_L13_P | F23 | FMC Reference 0th Data ( Clock ) P |
| FMC_LA01_CC_N | B28_L14_N | G24 | FMC Reference 1st Data ( Clock ) N |
| FMC_LA01_CC_P | B28_L14_P | G23 | FMC Reference 1st Data ( Clock ) P |

| | | | |
|---|---|---|---|
| FMC_LA02_N | B28_L16_N | D24 | FMC Reference 2nd Data N |
| FMC_LA02_P | B28_L16_P | E24 | FMC Reference 2nd Data P |
| FMC_LA03_N | B28_L12_N | F21 | FMC Reference 3rd Data N |
| FMC_LA03_P | B28_L12_P | G21 | FMC Reference 3rd Data P |
| FMC_LA04_N | B28_L3_N | J22 | FMC Reference 4th Data N |
| FMC_LA04_P | B28_L3_P | J21 | FMC Reference 4th Data P |
| FMC_LA05_N | B28_L18_N | G26 | FMC Reference 5th Data N |
| FMC_LA05_P | B28_L18_P | G25 | FMC Reference 5th Data P |
| FMC_LA06_N | B28_L17_N | C23 | FMC Reference 6th Data N |
| FMC_LA06_P | B28_L17_P | D22 | FMC Reference 6th Data P |
| FMC_LA07_N | B28_L23_N | A23 | FMC Reference 7th Data N |
| FMC_LA07_P | B28_L23_P | A22 | FMC Reference 7th Data P |
| FMC_LA08_N | B28_L15_N | C22 | FMC Reference 8th Data N |
| FMC_LA08_P | B28_L15_P | C21 | FMC Reference 8th Data P |
| FMC_LA09_N | B28_L24_N | B21 | FMC Reference 9th Data N |
| FMC_LA09_P | B28_L24_P | B20 | FMC Reference 9th Data P |
| FMC_LA10_N | B28_L22_N | B19 | FMC Reference 10th Data N |
| FMC_LA10_P | B28_L22_P | B18 | FMC Reference 10th Data P |
| FMC_LA11_N | B28_L19_N | A19 | FMC Reference 11th Data N |
| FMC_LA11_P | B28_L19_P | A18 | FMC Reference 11th Data P |
| FMC_LA12_N | B28_L21_N | A21 | FMC Reference 12th Data N |
| FMC_LA12_P | B28_L21_P | A20 | FMC Reference 12th Data P |
| FMC_LA13_N | B28_L10_N | F20 | FMC Reference 13th Data N |
| FMC_LA13_P | B28_L10_P | G20 | FMC Reference 13th Data P |
| FMC_LA14_N | B28_L9_N | D21 | FMC Reference 14th Data N |
| FMC_LA14_P | B28_L9_P | D20 | FMC Reference 14th Data P |
| FMC_LA15_N | B28_L20_N | C19 | FMC Reference 15th Data N |
| FMC_LA15_P | B28_L20_P | C18 | FMC Reference 15th Data P |
| FMC_LA16_N | B28_L7_N | D19 | FMC Reference 16th Data N |
| FMC_LA16_P | B28_L7_P | E19 | FMC Reference 16th Data P |
| FMC_LA17_CC_N | B64_L11_N | AK17 | FMC Reference 17th Data ( Clock ) N |
| FMC_LA17_CC_P | B64_L11_P | AJ17 | FMC Reference 17th Data ( Clock ) P |
| FMC_LA18_CC_N | B64_L12_N | AJ15 | FMC Reference 18th Data ( Clock ) N |
| FMC_LA18_CC_P | B64_L12_P | AJ16 | FMC Reference 18th Data ( Clock ) P |

| | | | |
|---|---|---|---|
| FMC_LA19_N | B64_L2_N | AP13 | FMC Reference 19th Data N |
| FMC_LA19_P | B64_L2_P | AN13 | FMC Reference 19th Data P |
| FMC_LA20_N | B64_L4_N | AN14 | FMC Reference 20th Data N |
| FMC_LA20_P | B64_L4_P | AM14 | FMC Reference 20th Data P |
| FMC_LA21_N | B64_L3_N | AN18 | FMC Reference 21st Data N |
| FMC_LA21_P | B64_L3_P | AM18 | FMC Reference 21st Data P |
| FMC_LA22_N | B64_L5_N | AP15 | FMC Reference 22nd Data N |
| FMC_LA22_P | B64_L5_P | AP16 | FMC Reference 22nd Data P |
| FMC_LA23_N | B64_L8_N | AL15 | FMC Reference 23rd Data N |
| FMC_LA23_P | B64_L8_P | AL16 | FMC Reference 23rd Data P |
| FMC_LA24_N | B64_L16_N | AJ14 | FMC Reference 24th Data N |
| FMC_LA24_P | B64_L16_P | AH14 | FMC Reference 24th Data P |
| FMC_LA25_N | B64_L7_N | AM15 | FMC Reference 25th Data N |
| FMC_LA25_P | B64_L7_P | AM16 | FMC Reference 25th Data P |
| FMC_LA26_N | B64_L21_N | AB15 | FMC Reference 26th Data N |
| FMC_LA26_P | B64_L21_P | AB16 | FMC Reference 26th Data P |
| FMC_LA27_N | B64_L24_N | AD16 | FMC Reference 27th Data N |
| FMC_LA27_P | B64_L24_P | AD17 | FMC Reference 27th Data P |
| FMC_LA28_N | B64_L18_N | AG14 | FMC Reference 28th Data N |
| FMC_LA28_P | B64_L18_P | AG15 | FMC Reference 28th Data P |
| FMC_LA29_N | B64_L20_N | AC16 | FMC Reference 29th Data N |
| FMC_LA29_P | B64_L20_P | AC17 | FMC Reference 29th Data P |
| FMC_LA30_N | B64_L17_N | AF15 | FMC Reference 30th Data N |
| FMC_LA30_P | B64_L17_P | AF16 | FMC Reference 30th Data P |
| FMC_LA31_N | B64_L15_N | AF17 | FMC Reference 31st Data N |
| FMC_LA31_P | B64_L15_P | AE17 | FMC Reference 31st Data P |
| FMC_LA32_N | B64_L23_N | AB14 | FMC Reference 32nd Data N |
| FMC_LA32_P | B64_L23_P | AA14 | FMC Reference 32nd Data P |
| FMC_LA33_N | B64_L19_N | AE15 | FMC Reference 33rd Data N |
| FMC_LA33_P | B64_L19_P | AD15 | FMC Reference 33rd Data P |
| FMC_PRSNT | B88_L12_P | F6 | FMC Module Exist Signal |
| PWRGD | B87_L6_P | M10 | FMC Power Good Signal |
| PS_IIC0_SCL | PS_MIO34 | B34 | FMC I2C Communication Data |
| PS_IIC0_SDA | PS_MIO35 | C31 | FMC I2C Communication Clock |

# Part 3.14: CAN Communication Interface

There are 2 CAN communication interfaces on the AXU7EV carrier board, which are connected to the MIO interface of the BANK501 on the PS system side. The CAN transceiver chip selected TI's SN65HVD232C chip for user CAN communication services. The connection of the CAN transceiver chip on the PS side is show as Figure 3-14-1

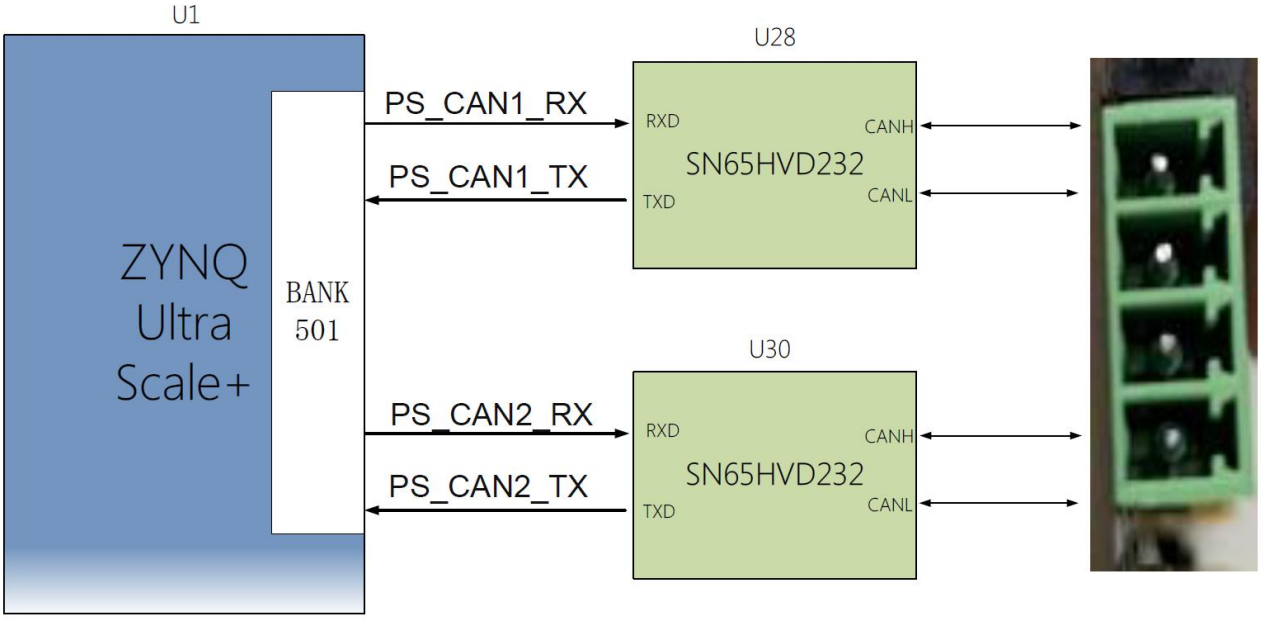



Figure 3-14-1: Connection diagram of CAN transceiver chip on PS side

**The CAN communication pin assignments are as follows:**

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| PS_CAN1_RX | PS_MIO38 | C34 | CAN1 Receiver |
| PS_CAN1_TX | PS_MIO39 | D30 | CAN1 Transmitter |
| PS_CAN2_RX | PS_MIO41 | D32 | CAN2 Receiver |
| PS_CAN2_TX | PS_MIO40 | D31 | CAN2 Transmitter |

# Part 3.15: 485 Communication Interface

There are two 485 communication interfaces on the AXU7EV carrier board. The 485 communication port is connected to the IO interface of BANK88 on the PL system. The 485 transceiver chip selects the MAX3485 chip from MAXIM

for the user's 485 communication service.

Figure 3-15-1 is the connection diagram of the 485 transceiver chip on the PL side

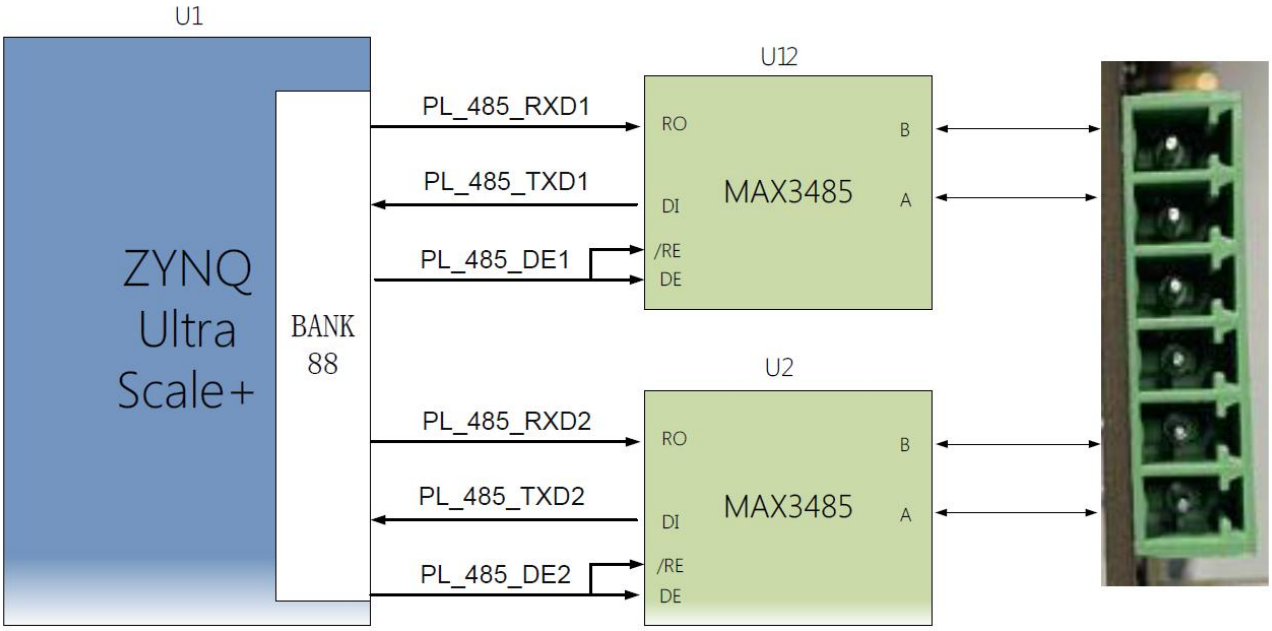



Figure 3-15-1: 485 Communication on the PL Side

**The 485 communication pins are assigned as follows:**

| Signal Name | Pin Name | Pin Number | Description |
|---|---|---|---|
| PL_485_TXD1 | B88_L6_P | C3 | The 1st Channel 485 Transceiver |
| PL_485_RXD1 | B88_L3_P | A3 | The 1st Channel 485 Receiver |
| PL_485_DE1 | B88_L6_N | B3 | The 1st Channel 485 Transmit Enable |
| PL_485_TXD2 | B88_L12_N | E5 | The 2nd Channel 485 Transceiver |
| PL_485_RXD2 | B88_L10_N | A5 | The 2nd Channel 485 Receiver |
| PL_485_DE2 | B88_L10_P | B5 | The 2nd Channel 485 Transmit Enable |

## Part 3.16: JTAG Debug Port

The JTAG interface is reserved on the AXU7EV carrier board for downloading ZYNQ UltraScale+ programs or firmware programs to FLASH. In order to not damage the ZYNQ UltraScale+ chip by plugging and unplugging under power, we aded a protection diode to the JTAG signal to ensure that the

signal voltage is within the range accepted by the FPGA and avoid damage to the ZYNQ UltraScale+ chip.

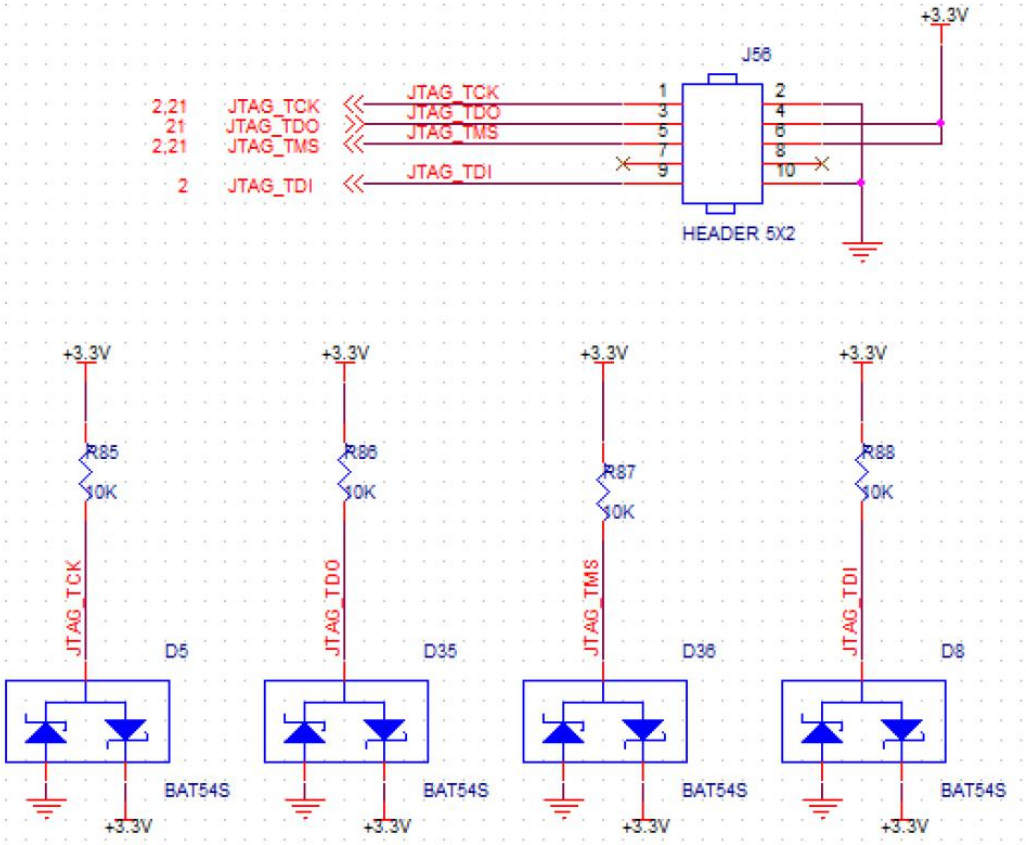



Figure 3-14-1: JTAG Interface Schematic

## Part 3.17: Real-time Clock

The ZU7EV chip has the function of an RTC real-time clock, with timing functions such as year, month, day, hour, minute, and second, and week. External need to connect a 32.768KHz passive clock to provide an accurate clock source to the internal clock circuit, so that the RTC can accurately provide clock information. At the same time, in order for the real-time clock to operate normally after the product is powered off, it is generally necessary to equip the coin battery (**model LR41, voltage is 1.5V**) to supply power to the clock chip. The BT1 on the development board is a battery Socket. After we put the coin battery, even the system is off, the coin battery can also power the RTC system and provide continuous time information.

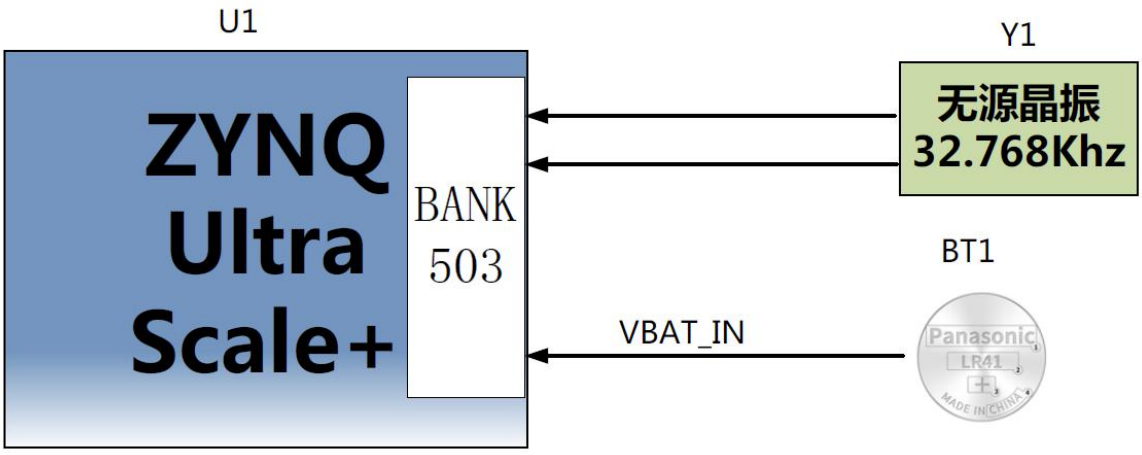



Figure 3-17-1: RTC Schematic

## Part 3.18: EEPROM and Temperature Sensor

The AXU7EV Fpga development board has an EEPROM onboard. The model of the EEPROM is 24LC04, and the capacity is: 4Kbit (2 * 256 * 8bit), which is connected to the PS terminal through the I2C bus.

A high-precision, low-power, digital temperature sensor chip is installed on the AXU7EV FPGA development board, and the model is LM75 from ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees.

The EEPROM and temperature sensor are mounted on the Bank500 MIO of ZYNQ UltraScale+ through the I2C bus. Figure 3-18-1 is the schematic diagram of EEPROM and temperature sensor

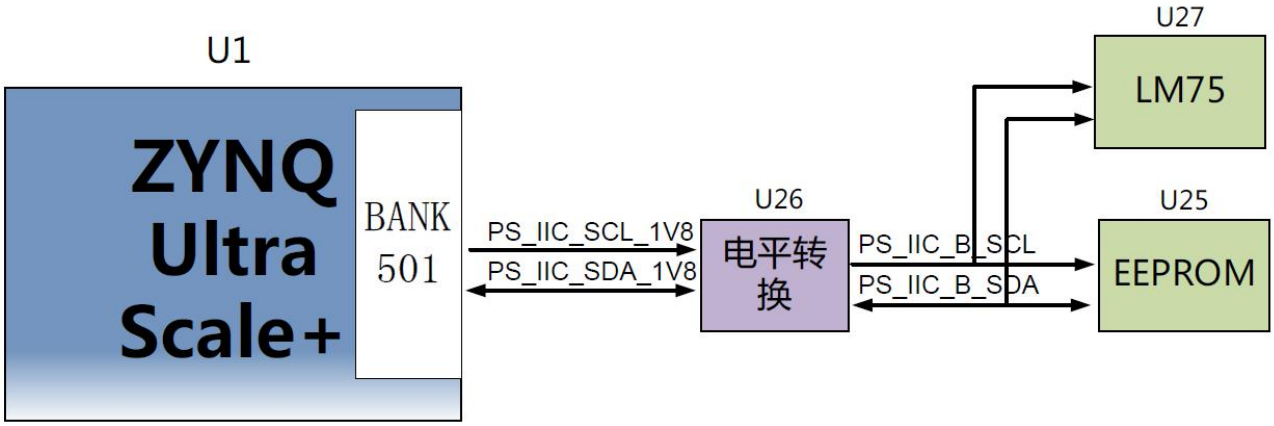



Figure 3-16-1: EEPROM and Sensor connection diagram

**EEPROM pin assignment:**

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| PS_IIC_SCL_1V8 | PS_MIO34 | L22 | I2C Clock Signal |
| PS_IIC_SDA_1V8 | PS_MIO35 | P22 | I2C Data Signal |

## Part 3.19: User LEDs

There are 4 LEDs on the AXU7EV Carrier board. including 1 power indicator light, 1 DONE indicator, 1 PS control indicator, and 1 PL control indicator. The user can control the on and off through the program. The schematic diagram of the user's LED light hardware connection is shown in Figure 3-19-1:

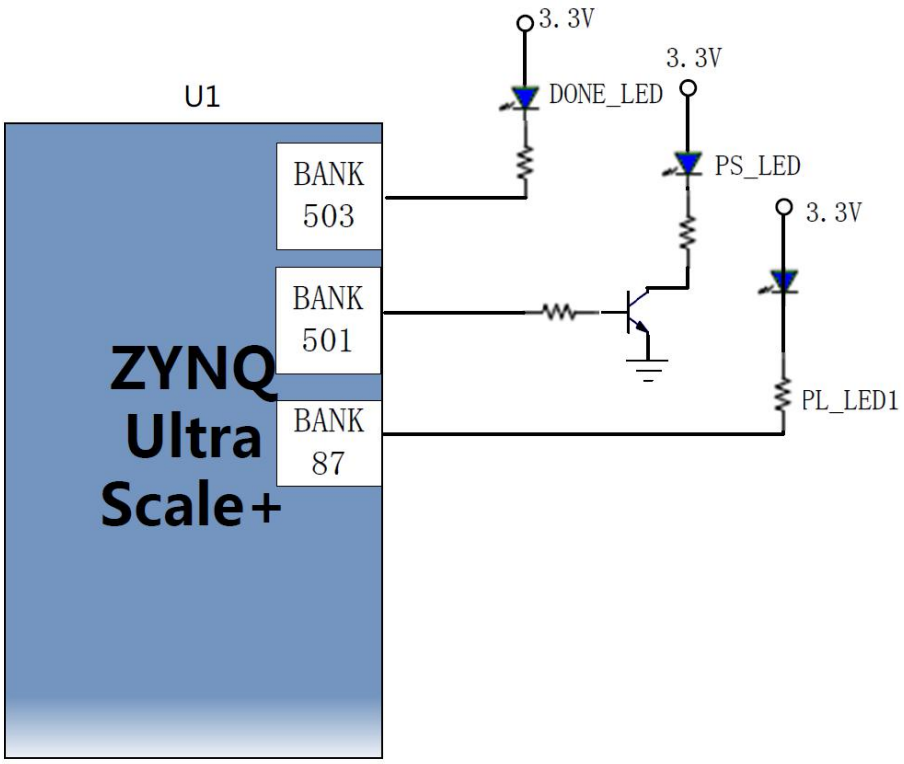



Figure 3-19-1: The User LEDs Hardware Connection Diagram

**Pin assignment of user LED lights**

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| PS_LED | PS_MIO44 | E32 | User PS LED Light |
| PL_LED | B87_L8_P | K9 | User PL LED Light |

## Part 3.20: Keys

There are 1 reset KEY RESET and 2 user KEYs on the AXU7EV carrier board. The reset signal is connected to the reset chip input of the core board ACU7EV, and the user can use this reset KEY to reset the ZYNQ system. One user KEY is connected to the MIO of the PS, and one is connected to the IO of the PL. The reset KEY and the user KEYs are both low-level active. The connection diagram of the user key is shown in Figure 3-20-1:

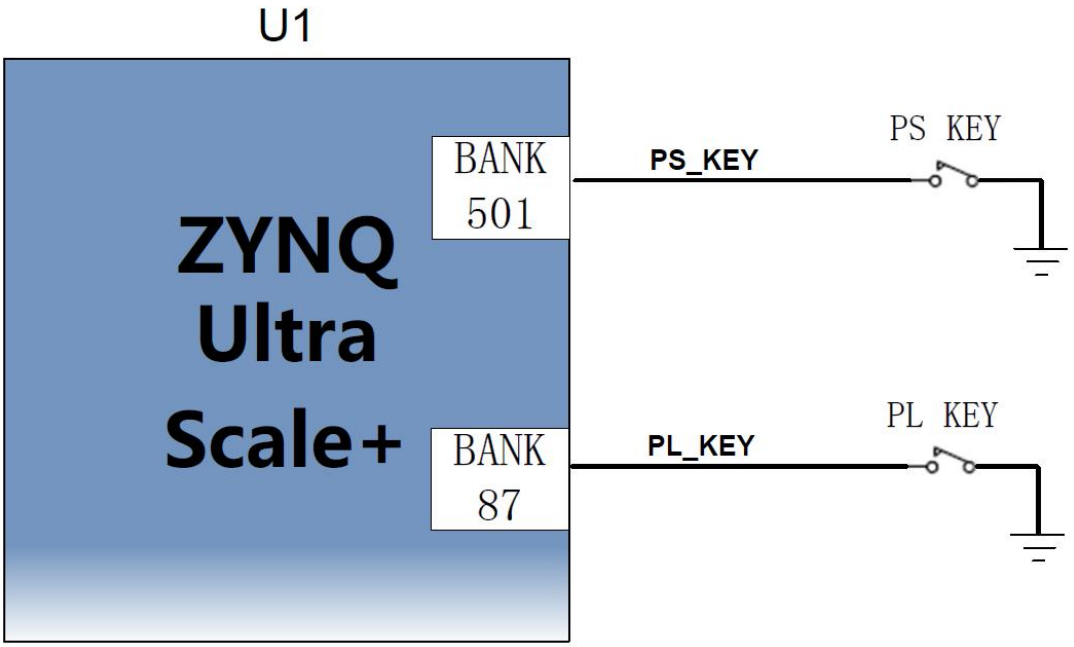



Figure 3-20-1: Rest keys connection diagram

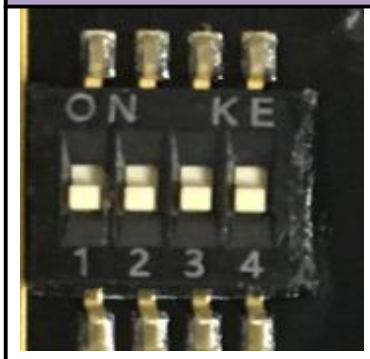
### ZYNQ pin assignment of keys

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|---|---|---|---|
| PS_KEY1 | PS_MIO33 | B33 | PS KEY Input |
| PL_KEY1 | B87_L8_N | J9 | PL KEY Input |

## Part 3.21: DIP Switch Configuration

There is a 4-digit DIP switch SW1 on the FPGA development board to configure the startup mode of the ZYNQ system. The AXU7EV system development platform supports 4 startup modes. The 4 startup modes are

JTAG debug mode, QSPI FLASH, EMMC and SD2.0 card startup mode. After ZU7EV chip is powered on, it will detect the level of (PS_MODE0~3) to determine the startup mode. The user can select different startup modes through the DIP switch SW1 on the carrier board. The SW1 startup mode configuration is shown in the following table 3-21-1.

| SW1 | Dial Position（1，2，3，4） | MODE[3:0] | Start mode |
|---|---|---|---|
|  | ON，ON，ON，ON | 0000 | PS JTAG |
| | ON，ON，OFF ,ON | 0010 | QSPI FLASH |
| | ON，OFF，ON，OFF | 0101 | SD Card |
| | ON，OFF， OFF， ON | 0110 | EMMC |

## Part 3.22: Power Supply

The power input voltage of the AXU7EV development board is DC12V. In the carrier board, the DC12V is converted into +5V, +3.3V, +1.8V, through one-way DC/DC power chip TPS54620 and two-way DC/DC power chip MP2323/MP1482. The schematic diagram of the power supply design on the board is shown in Figure 3-22-1:

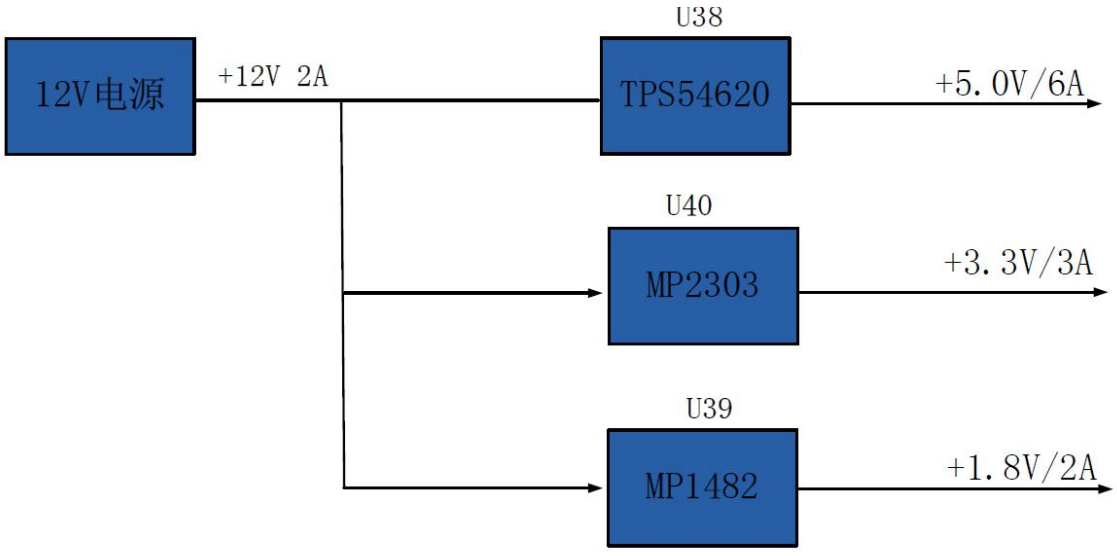



Figure 3-22-1: Carrier Board Power Schematic

The functions of each power distribution are shown in the following table:

| Power | Function |
|---|---|
| +5.0V | USB power supply |
| +1.8V | Ethernet, USB2.0 |
| +3.3V | Ethernet, USB2.0, M.2, SD, DP, CAN, RS485 |

## Part 3.23: ALINX Customized Fan

Because ZU7EV generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the ZYNQ chip. The control pin is connected to the IO of the BANK88 (PIN F4). If the IO level output is high, the MOSFET is turned on and the fan is working. If the IO level output is low, the fan stops. The fan design on the board is shown in Figure 3-21-1.

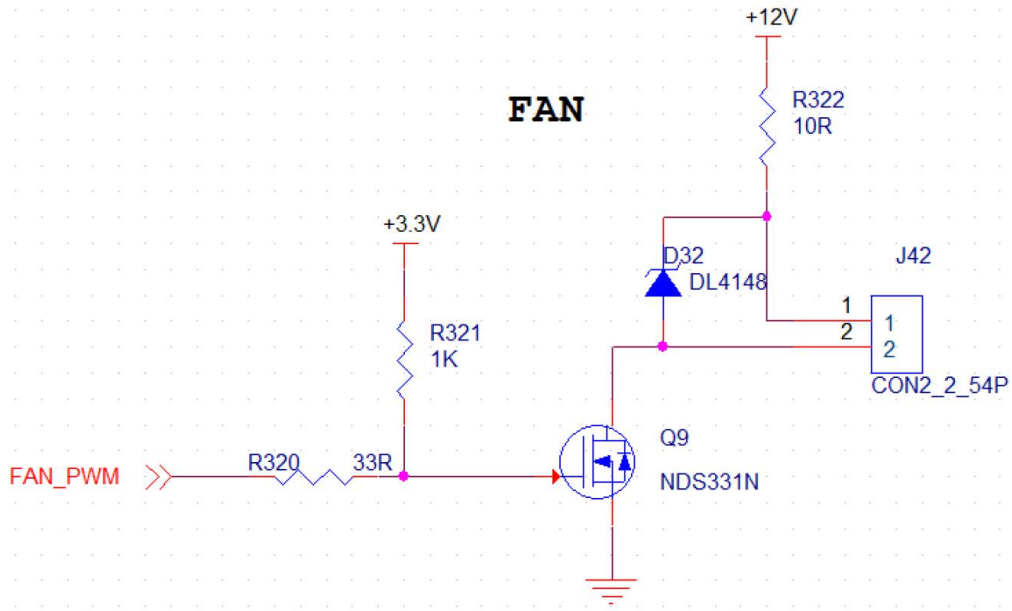



Figure 3-23-1：Fan Design Schematic

The fan has been screwed to the FPGA development board before leaving the factory. The power of the fan is connected to the socket of J55. The red is positive and the black is negative.

# Part 3.24: Carrier Board Size Dimension

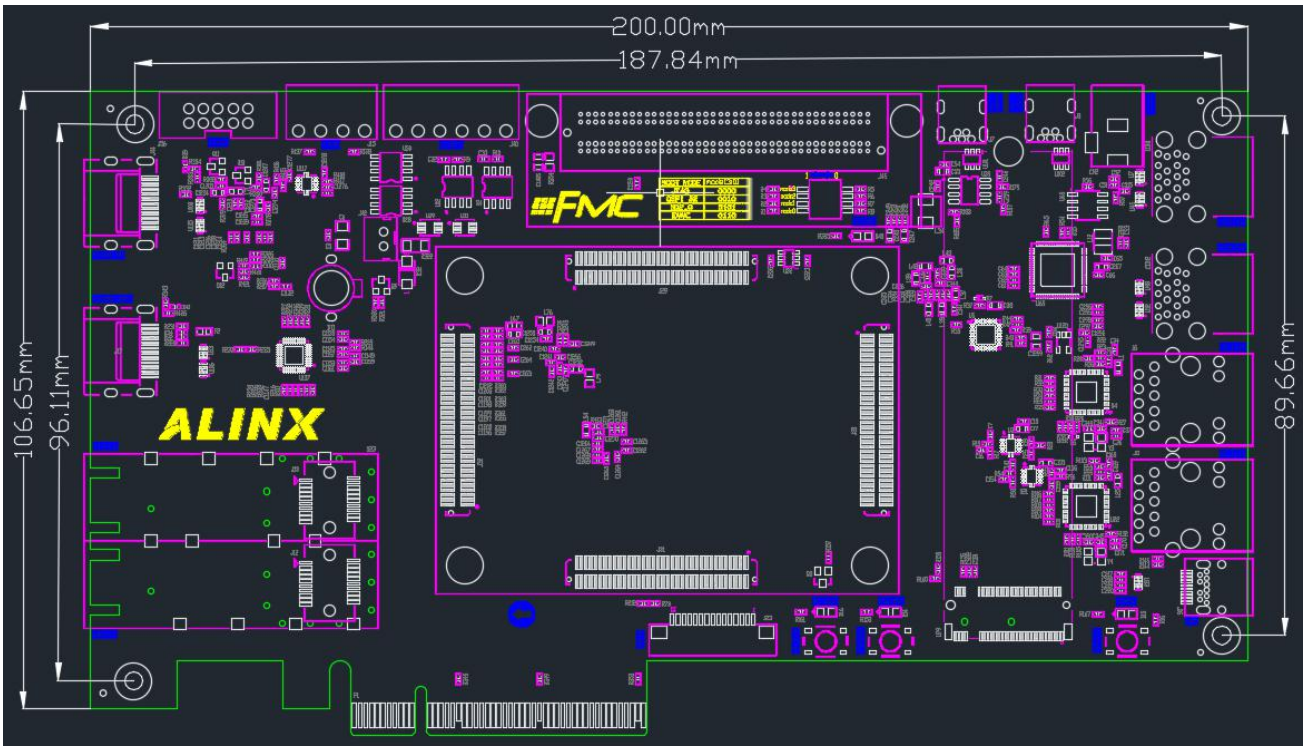



Figure 3-24-1: Top View