ZYNQ UltraScale+ MPSOC

PZ-ZU9/15EG FPGA Board User Manual

Version Records：

Data	Version	Description
2019.5.25	V1.0	initial version

Content

Part 1: UltraScale+ MPSoC Introduction

The **Xilinx Zynq UltraScale MPSoC** architecture is based on **TSMC 16FinFET+** processing technology, enabling the next generation of **Zynq® UltraScale+ MPSoCs**. Building on the success of the **Zynq-7000 SoC** family, the new **UltraScale MPSoC** architecture further expands **Xilinx SoCs** to support true heterogeneous multiprocessing, providing the right engine for the right tasks in smarter systems, including:

- **Smarter Control**

Interconnected Control Machine Room: Flexible/adaptable manufacturing, factory throughput, quality and safety

- **Smarter Vision**

Advanced 2D/3D: Evolving video processing algorithms, object detection and analysis

- **Smarter Network**

Wireless Communication: Supports multiple frequency bands and smart antennas
Wired Communications: Multiple Wired Communications Standards and Context-Aware
Network Services Data Center: Software Defined Networking (SDN), data preprocessing, and analytics

The **ZYNQ UltraScale MPSoC** architecture provides multiple advanced processors that scale from **32-bit** to **64-bit** with virtual support. **Xilinx** has been working with **ARM®** to provide the most efficient **64-bit ARMv8** application processor supporting **Cortex®-A53**, real-time low power coprocessor with **ARM® Cortex®-R5**, and **ARM® OpenGL ES 1.1/2.0** compliant **Mali™-400MP multi-core GPU**, leveraging ARM's leadership in embedded processors and its ecosystem. In addition, the **ZYNQ UltraScale MPSoC** also includes an **H.265/H.264** video codec unit that provides native **UltraHD** compression and a dedicated engine for dynamic power management and security configuration requirements.

Xilinx has a variety of tools to support the benefits of **SoC**s, offering the **Vivado® Design Suite**, **Xilinx SDK**, and **PetaLinux** to further accelerate development using the **SDx™** family of design abstraction environments to efficiently leverage the power of the **ZYNQ UltraScale+ MPSoC**. The basic elements of this architecture include:

- 64-bit quad-core ARM Cortex-A53 processor
- Dual core ARM Cortex-R5
- Real-time processor ARM Mali™-400MP
- Graphics processor H.265/264
- Video codec unit
- Advanced Dynamic Power Management Unit
- Configure security cells
- DDR4/LPDDR4 memory interface support
- 16FinFET+ unit power performance

- SDSoC development environment (design abstraction)
- Next Generation AXI Interconnect

Part 2: PZ-ZU9EG/15EG FPGA Board Overview

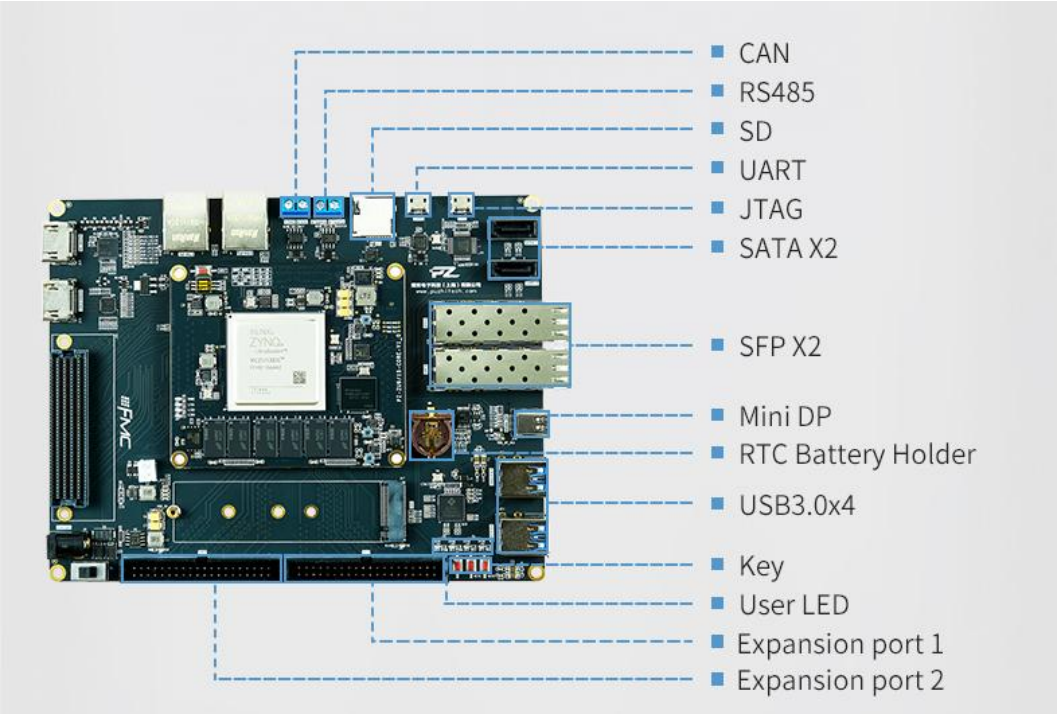
Part 2.1: Board Introduction

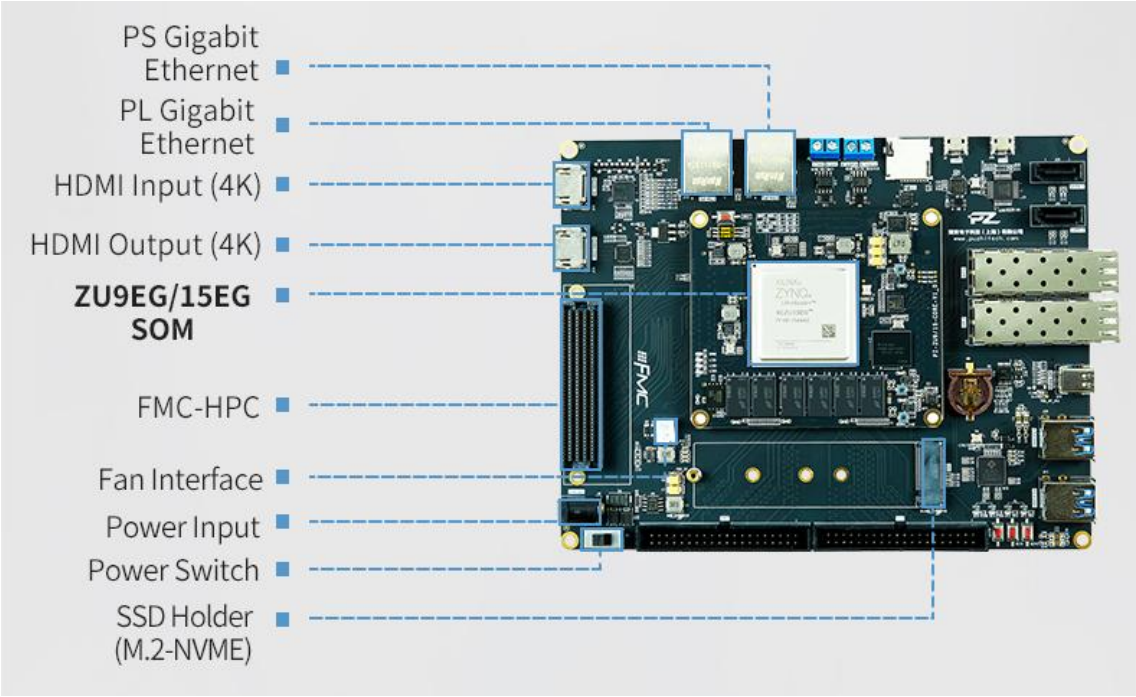
The PZ-ZU9EG/15EG FPGA development board adopts the mode of "Core board + Carrier board". There are two versions: PZ-ZU9EG and PZ-ZU15EG, respectively using XCZU9EG-2FFVB1156I and XCZU15EG-2FFVB1156I chips from XILINX as the main controller. The FPGA development board integrates a wealth of peripheral resources and provides detailed development routines to facilitate the use and verification of users.

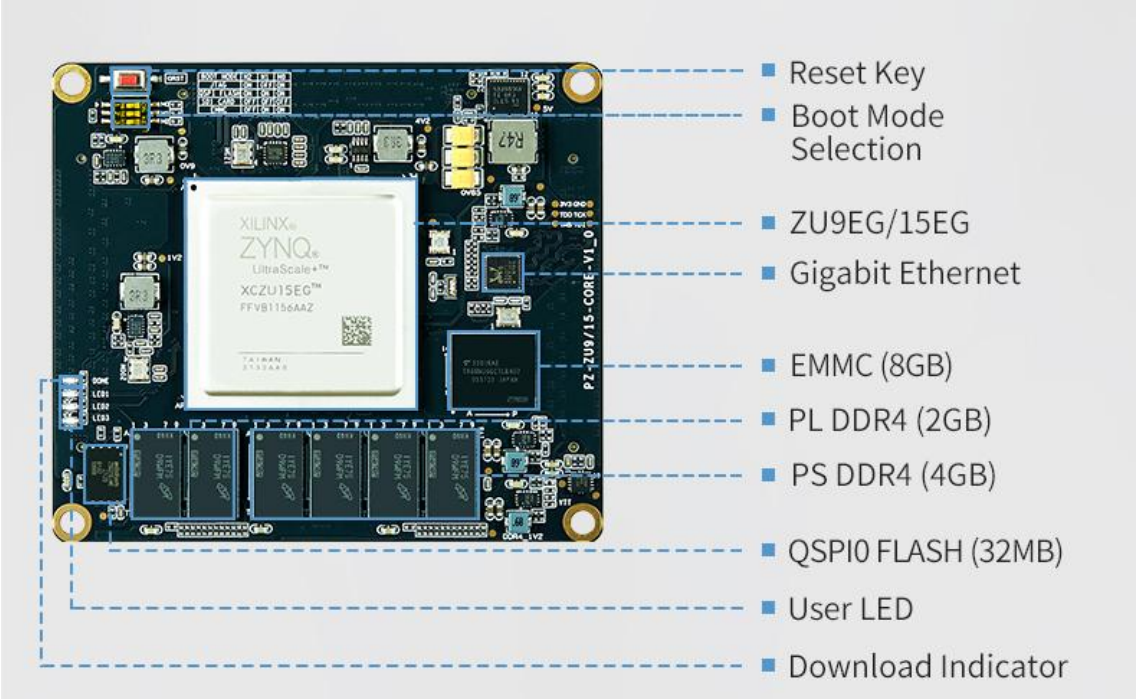
In addition, the FPGA development board integrates a wealth of peripheral resources, provides detailed development routines, and accelerates user learning or project advancement. In addition, the development board also integrates a JTAG debugger, so that a MicroUSB cable and a 12V power cable can make the development board work and be more convenient to use.

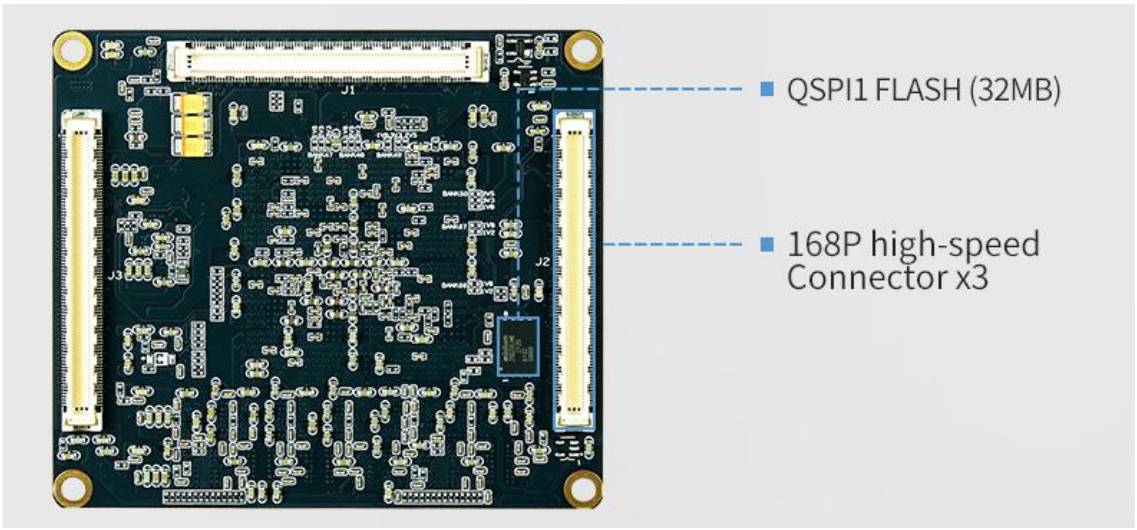
The Form Factors of the FPGA development board is 180 x 140mm, and a fixing hole is placed at each of the four corners of the board to install the support column or fix the board, and the hole diameter is 3.5mm.

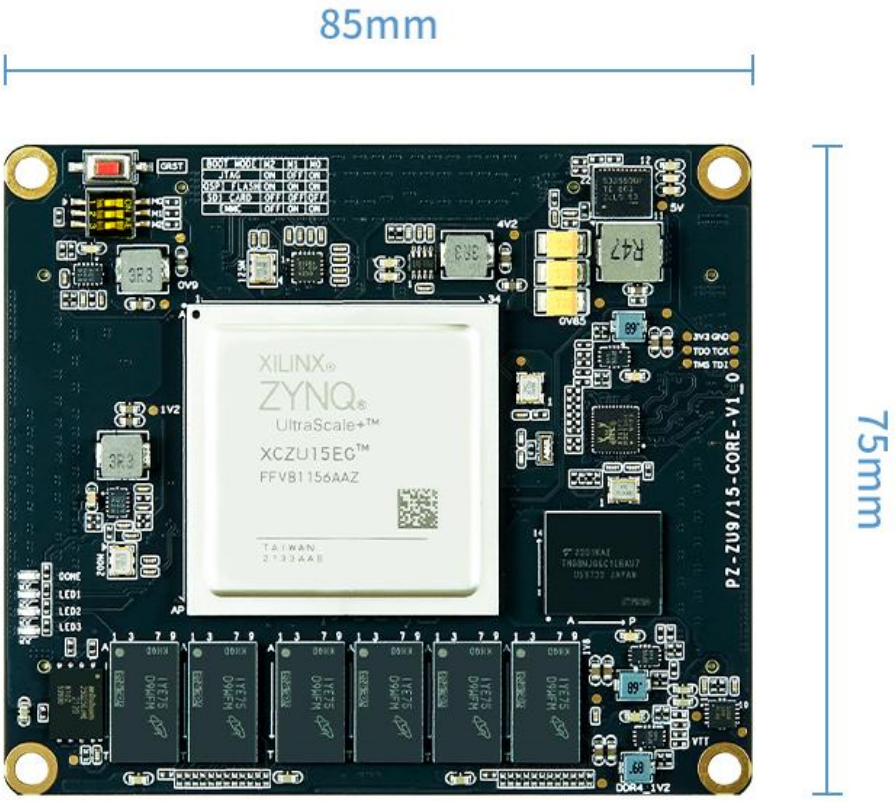
The following Figures are the specification of the functional modules of the development board and the core board respectively. Users can view the location of the peripherals according to the labels.




PS Gigabit Ethernet
PL Gigabit Ethernet
HDMI Input (4K)
HDMI Output (4K)
ZU9EG/15EG SOM
FMC-HPC
Fan Interface
Power Input
Power Switch
SSD Holder (M.2-NVME)


Reset Key
Boot Mode Selection
ZU9EG/15EG
Gigabit Ethernet
EMMC (8GB)
PL DDR4 (2GB)
PS DDR4 (4GB)
QSPI0 FLASH (32MB)
User LED
Download Indicator


QSPI1 FLASH (32MB)
168P high-speed Connector x3

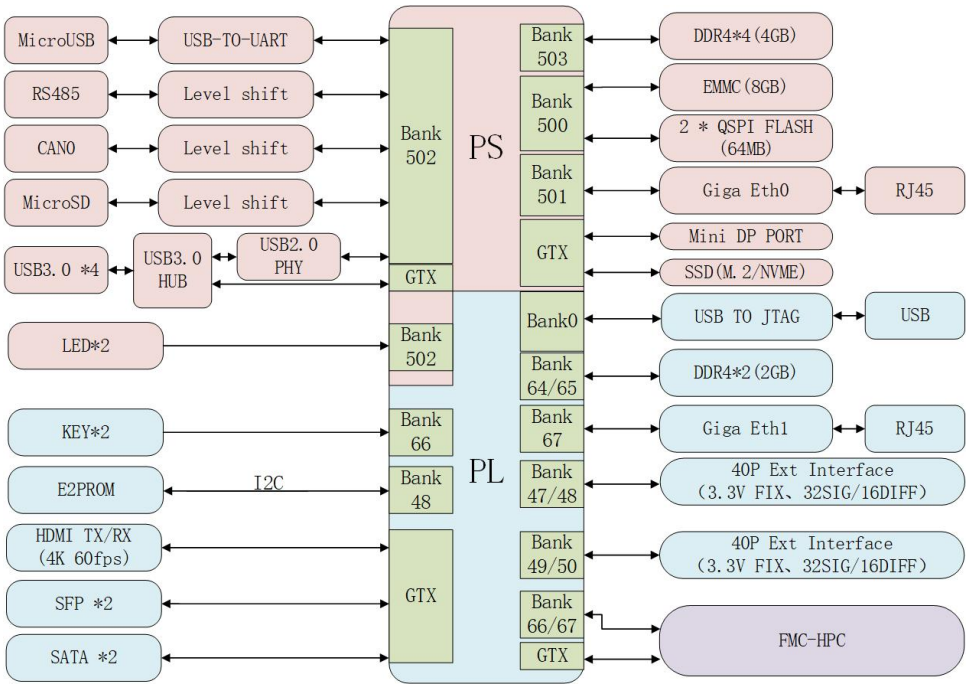

85mm
75mm
XILINX
ZYNQ
UltraScale+
XCZU15EG
FFVB1156AAZ
PZ-ZU9/15-CORE-V1_0


Top MAX Height 3mm
PCB Thickness 1.75mm
Connector Height 4mm

Part 2.2: FPGA Board Resources and Block Diagram

The onboard resources of the FPGA development board are listed in the table and block diagram below, and the functions we have included can be seen from the table below.

FPGA	XCZU9EG-2FFVB1156	XCZU15EG-2FFVB1156I
Processor Core	Quad-Core Arm® Cortex®-A53 (1.333Ghz), Dual Core Arm Cortex-R5F (533Mhz)	
GPU	Mali™-400 MP2, 667Mhz	
Logic Cells (K)	600	747
Lookup Tables (K)	274	341
Flip-Flops (K)	548	682
Max.DistributedRAM (Mb)	8.8	11.3
Block RAM (Mb)	32.1	26.2
Ultra RAM (Mb)	---	31.5
DSP Slices	2520	3528
DDR4	PS-side 4GB, PL-side 2GB	
EMMC	8GB	
QSPI FLASH	64MB, Dual FLASH Boot, Faster Boot	
Boot Mode	JTAG/SD/QSPI/EMMC	
E2PROM	64Kbit	
UART/RS485/CAN	1/ 1/ 1	
SD Card Slot	1	
Gigabit Ethernet	PS-side 1/PL-side 1	
USB3.0	4 Ports	
USB to JTAG	1	
Mini DP Interface	1	
HDMI (4K)	1 Input / 1 Output	
SSD (NVME Protocol)	1	
SFP	2	
SATA	2	
MIPI	2	
FMC	HPC FMC Interface	
Expansion Port	2	
LED	3 LEDs in SOM/4 LEDs in Carrier Board	
Keys	3	
Voltage/Current	12V/3A	


MicroUSB
USB-TO-UART
RS485
Level shift
CAN0
Level shift
MicroSD
Level shift
USB3.0 *4
USB3.0 HUB
USB2.0 PHY
LED*2
KEY*2
E2PROM
I2C
HDMI TX/RX (4K 60fps)
SFP *2
SATA *2
Bank 502
GTX
Bank 502
Bank 66
Bank 48
GTX
PS
PL
Bank 503
Bank 500
Bank 501
GTX
Bank0
Bank 64/65
Bank 67
Bank 47/48
Bank 49/50
Bank 66/67
GTX
DDR4*4(4GB)
EMMC(8GB)
2 * QSPI FLASH (64MB)
Giga Eth0
RJ45
Mini DP PORT
SSD(M.2/NVME)
USB TO JTAG
USB
DDR4*2(2GB)
Giga Eth1
RJ45
40P Ext Interface (3.3V FIX、32SIG/16DIFF)
40P Ext Interface (3.3V FIX、32SIG/16DIFF)
FMC-HPC

Part 3: PZ-ZU9EG/15EG SOM Core Board Overview

Part 3.1: SOM Introduction

The PZ-ZU9EG/15EG SOM core board adopts the XCZU9EG-2FFVB1156I / XCZU15EG-2FFVB1156I chip of XILINX company as the main controller. The two core boards are completely compatible, and the models can be exchanged directly without changing the Carrier Board. The core board is connected to the carrier board with three 0.5mm pitch 168P gold-plated high-speed connectors, and four 3.5mm fixing holes are placed on the four feet of the core board. This hole can be fastened with the carrier board by screws, which ensures stable operation in the environment of strong vibration.

Part 3.2: SOM Specification

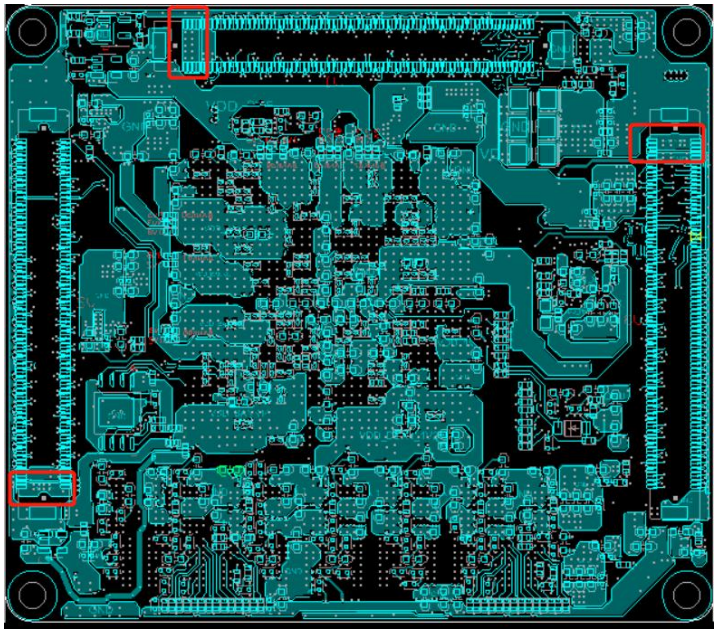
PZ-ZU9/15EG Industrial Grade SOM Specification		
FPGA Chip	XCZU9EG-2FFVB1156I	XCZU15EG-2FFVB1156I
Processor Core	ARM : 4 x Cortex-A53 1.333Ghz RPU : 2 x Cortex-R5 533Mhz GPU : Mali-400MP2 667Mhz	
logic cells	600K	747K
Lookup Tables (LUTs)	274K	341K
Flip-Flops	548K	682K
Block RAM	32.1Mb	26.2Mb
Ultra RAM	/	31.5Mb
DSP Slices	2520	3528
DDR4/DDR4L	PS-side 4GB 2400Mhz*64bit / PL-side 2GB 2400Mhz*32bit	
QSPI FLASH	2 channels (QSP0+QSPI1), single chip 32MB, total 64MB	
EMMC	8GB, to store startup files and user files	
Start-up Mode	JTAG/QSPI/SD/EMMC, onboard DIP switch selection	
Gigabit Ethernet	1 (PS-side)	
User LEDs	3 (PL-side, High Level light, Low Level off)	
Number of IOs	MIO: 38 (Fixed 1.8V Level) HP: 96 (1.2/1.8V Adjustable) HD: 96 (1.8/2.5/3.3V Adjustable)	
Number of GTR/GTH interfaces	4 pairs of TX/RX on PS side, 24 pairs of TX/RX on PL side	
Voltage/Current	8-12V/5A (Recommended Voltage 8V)	

Working Temperature	-40°C -- +85°C
Technology	Immersion Gold Process, 168P Connectors X 3
Connector Height	4mm

Part 3.3: Power Connection

The power supply voltage range of the core board is 8-12V. The recommended power supply voltage is 8V. There are power input pins on the four corners of the core board. The power pins have been connected inside the module. In the design, you only need to connect the power pin on one corner, and the core board can work. The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two vias. The limit current of the core board power supply is 5A, so the external power supply needs to consider the limit current to ensure the stable operation of the core board.

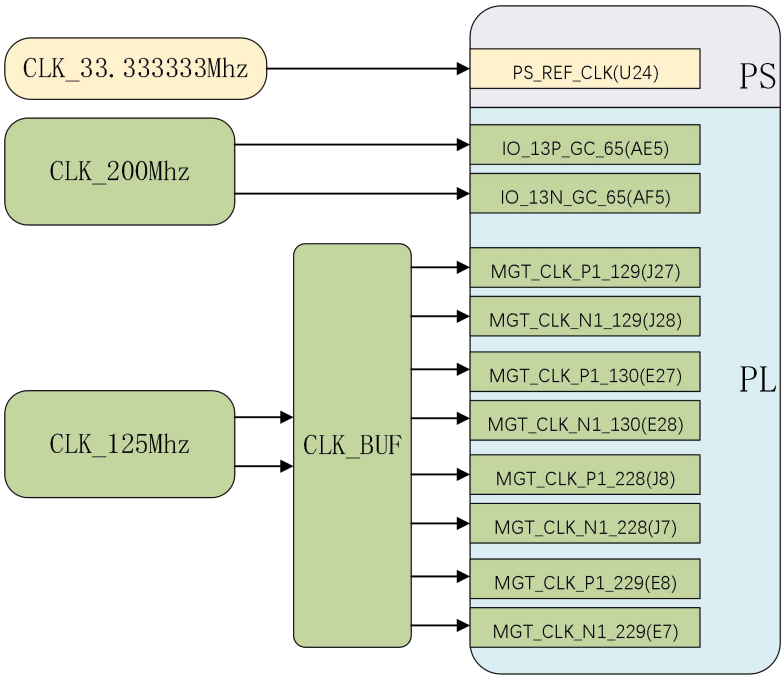
The output voltage of the power supply to the module needs to be stable. Add a first-level DCDC power conversion to the module power input, from high voltage to 8-12V (recommended 8V), and the DCDC current output capacity can be about 6A. For example, you can refer to the power chip TPS56628. Two **220uF/25V** capacitors should be placed at the power input of the module to ensure power quality.



Part 3.4: Clock

The core board provides a 33.333333Mhz clock input for the PS side, and the input pin

position is PS_REF_CLK; it provides a 200Mhz differential clock input for the PL side. The clock input pins on the PL side is IO_13P_GC_65/IO_13N_GC_65, and the pin position is AE5/ AF5; provides a 125Mhz differential clock input for the PL side GTX. After the 125M input is converted into 4 channels of 125M clock output through the clock buffer, they are connected to the corresponding positions as shown in the figure.

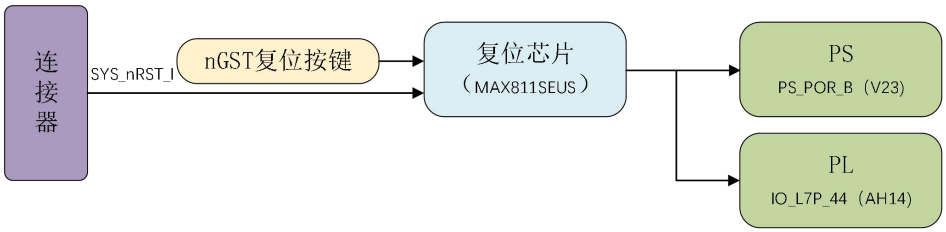


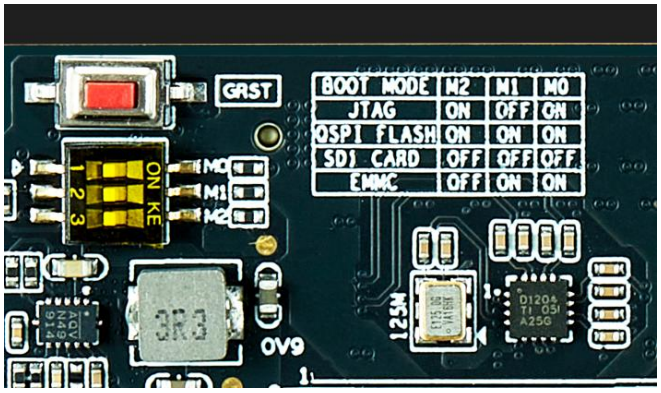
Part 3.5: Global Reset

The core board provides the "**nGST**" reset key, which is a system reset key and is active at low level. This pin is also drawn to the connector, and the signal name is "**SYS_nRST_I**", which is convenient for adding a reset key externally or designing a watchdog reset circuit. At the same time, in order to stabilize the system, we added a reset chip MAX811SEUS to the core board. This signal can be used for the reset of other peripherals on the core board. The signal level is 3.3V. The reset pin is a shared reset for PS/PL, which is connected to the PS_POR_B (V23) pin on the PS side and the IO_L7P_44 (AH14) pin of the BANK44 on the PL side. The level of the AH14 pin is 3.3V.

If the reset circuit needs to be designed on the carrier board, the following situations need to be considered.

1) The reset circuit board is used internally, only need to add a reset key and a 10uF capacitor parallel port to the ground.
2) The reset circuit needs to be reserved on the structure for external use. It is necessary to add a key to the ground, and at the same time, connect a 10uF capacitor and a TVS anti-static device to the ground in parallel.



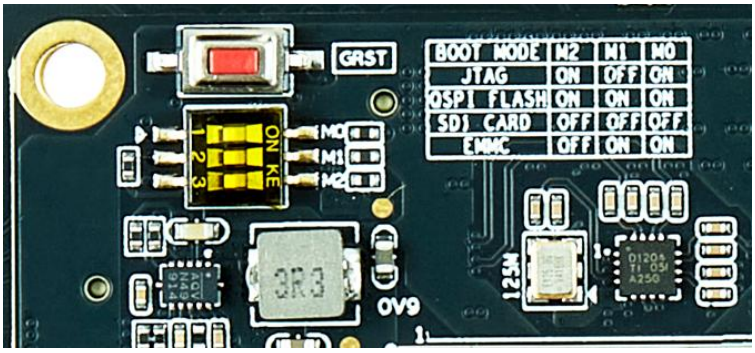


Part 3.6: Boot Mode Selection

The core board supports four boot modes, namely JTAG, QSPI Flash, EMMC, and SD card. The first three startup methods are installed on the core board, and users can realize the SD card method by connecting with the carrier board. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch. Because the main chip generates a large amount of heat, a heat sink needs to be added on the core board, which will block the BOOT MODE selection table.

The startup mode has been set on the core board. The default DIP switches are all OFF, that is, SD card startup. Users can choose other startup modes according to the labels.

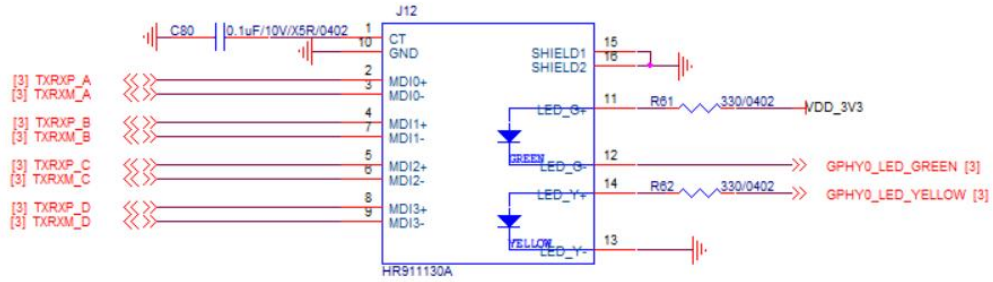
BOOT MODE	M2	M1	M0
JTAG	ON	OFF	ON
QSPI FLASH	ON	ON	ON
SD1 CARD	OFF	OFF	OFF
EMMC	OFF	ON	ON



Part 3.7: Gigabit Ethernet Chip

The Gigabit Ethernet chip RTL8211FI-CG is placed on the core board. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below. Ethernet external connection only needs an RJ45 with a transformer to use, the chip address PHY_AD[2:0]=001, the connection schematic diagram can refer to the following figure (the product circuit needs to add an ESD protection circuit). In addition, in actual product application, C80 needs to use high withstand voltage capacitors, such as 0.1uF/2KV.

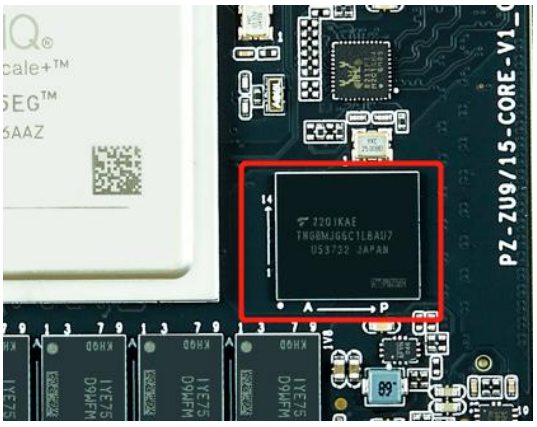
RMGII Signal	Pin Name	Pin Position
GTX_CLK	MIO26_501	P21
TXD0	MIO27_501	M21
TXD1	MIO28_501	N21
TXD2	MIO29_501	K22
TXD3	MIO30_501	L21
TX_EN	MIO31_501	J22
RX_CLK	MIO32_501	H22
RXD0	MIO33_501	H23
RXD1	MIO34_501	L22
RXD2	MIO35_501	P22
RXD3	MIO36_501	K23
RX_CTL	MIO37_501	N22
MDC	MIO76_502	H25
MDIO	MIO77_502	F25



Part 3.8: EMMC Pin Definition

The onboard EMMC has a capacity of 8GB, the operating temperature is -40℃--+85℃, and the pin definitions are as follows.

EMMC Pin	Pin Name	Pin Position
EMMC_D0	MIO13	AK17
EMMC_D1	MIO14	AL16
EMMC_D2	MIO15	AN16
EMMC_D3	MIO16	AM16
EMMC_D4	MIO17	AP16
EMMC_D5	MIO18	AE18
EMMC_D6	MIO19	AL17
EMMC_D7	MIO20	AD18
EMMC_CLK	MIO22	AD20
EMMC_CMD	MIO21	AF18
EMMC_nRST	MIO23	AD19



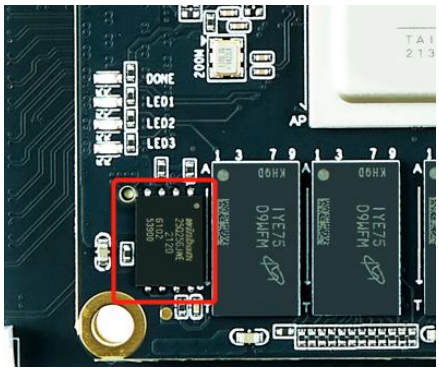
Part 3.9: QSPI FLASH

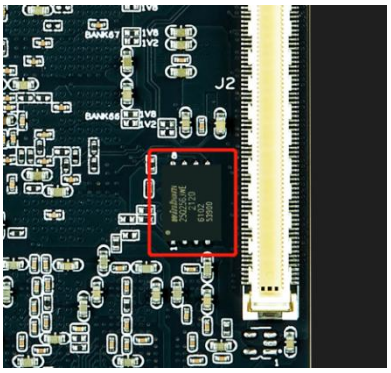
The core board is designed with two channels of QSPI FLASH, the single-chip capacity is

32MB, and the two chips total 64MB. Users can define it as QSPI X8 to speed up the startup and reduce the startup time. QSPI FLASH can be used to store boot files and user files

QSPI0 FLASH Pin	Pin Name	Pin Position
DATA0	MIO4	AH16
DATA1	MIO1	AJ16
DATA2	MIO2	AD16
DATA3	MIO3	AG16
QSPI_CS	MIO5	AM15
QSPI_CLK	MIO0	AF16

QSPI1 FLASH Pin	Pin Name	Pin Position
DATA0	MIO8	AE17
DATA1	MIO9	AP15
DATA2	MIO10	AH17
DATA3	MIO11	AF17
QSPI_CS	MIO7	AD17
QSPI_CLK	MIO12	AJ17





Part 3.10: On-board LED

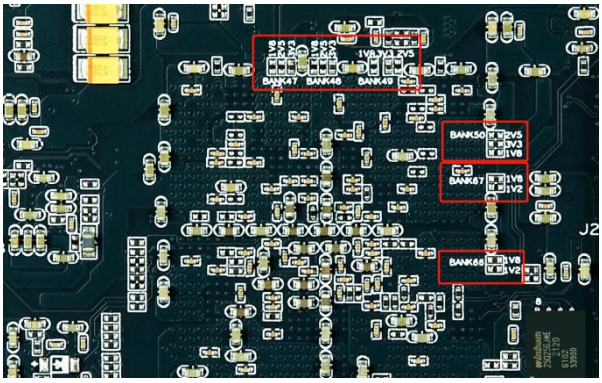
In order to facilitate debugging, three LEDs are placed on the core board, and the LEDs are connected to the PL side. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and the low level LED goes out.

Number	Pin Name	Pin Position
LED1	IO-L7N-44	AH13
LED2	IO-L8P-44	AJ15
LED3	IO-L8N-44	AJ14

Part 3.11: BANK Interface Level Selection

The BANK66/67 on the core board are HP BANK, the interface level is configured as

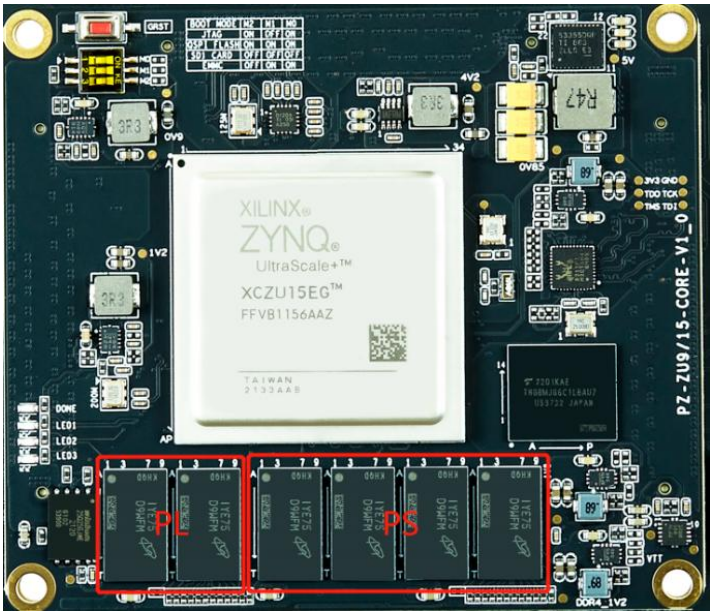
1.2/1.8V, and the voltage can be adjusted by 0 ohm resistance welding through the instructions provided on the single board, and the default level is 1.8V. BANK47/48/49/50 are HD BANK, BANK level can realize 1.8V/2.5V/3.3V three level conversion, just change the resistor position, the default level is 3.3V.



Part 3.12: DDR4

The PS side is equipped with four industrial-grade DDR4 chips with a single capacity of 1GB and a total capacity of 4GB. The model is MT40A512M16LY-062E. The DDR4 pin assignment can directly call the system assignment. You can also refer to the routines provided by our company.

The PL side is equipped with two industrial-grade DDR4 chips with a single capacity of 1GB, the model is MT40A512M16LY-062E, and the DDR4 pin assignment is shown in the table below.



PL side DDR4 pins		
DDR4 Pin	**Pin Name**	**Pin Position**
DDR4_D0	IO-L6P-64	AJ10

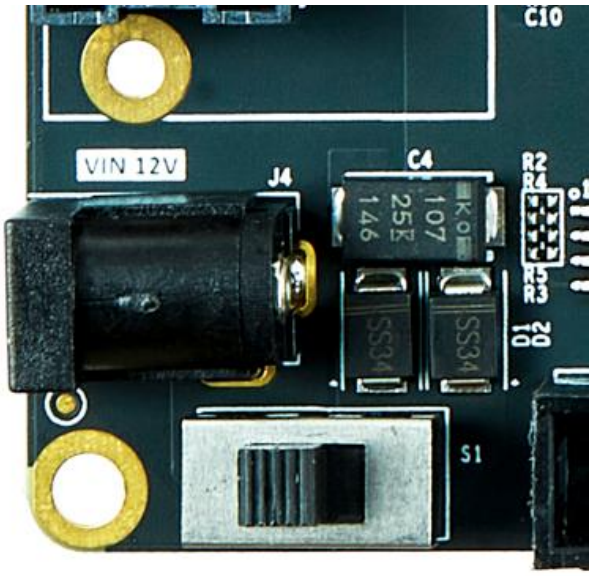
DDR4_D1	IO-L2N-64	AM11
DDR4_D2	IO-L3P-64	AL10
DDR4_D3	IO-L5N-64	AP9
DDR4_D4	IO-L6N-64	AK10
DDR4_D5	IO-L2P-64	AL11
DDR4_D6	IO-L5P-64	AN9
DDR4_D7	IO-L3N-64	AM10
DDR4_DM0	IO-L1P-64	AJ12
DDR4_DQS_P0	IO-L4P-64	AP11
DDR4_DQS_N0	IO-L4N-64	AP10
DDR4_D8	IO-L11P-64	AK8
DDR4_D9	IO-L8P-64	AM9
DDR4_D10	IO-L12P-64	AL8
DDR4_D11	IO-L8N-64	AM8
DDR4_D12	IO-L11N-64	AK7
DDR4_D13	IO-L9P-64	AJ9
DDR4_D14	IO-L12N-64	AL7
DDR4_D15	IO-L9N-64	AK9
DDR4_DM1	IO-L7P-64	AN8
DDR4_DQS_P1	IO-L10P-64	AN7
DDR4_DQS_N1	IO-L10N-64	AP7
DDR4_D16	IO-L18P-64	AK5
DDR4_D17	IO-L15N-64	AP4
DDR4_D18	IO-L14P-64	AM6
DDR4_D19	IO-L15P-64	AP5
DDR4_D20	IO-L18N-64	AK4
DDR4_D21	IO-L17N-64	AN4
DDR4_D22	IO-L14N-64	AM5
DDR4_D23	IO-L17P-64	AM4
DDR4_DM2	IO-L13P-64	AL6
DDR4_DQS_P2	IO-L16P-64	AN6
DDR4_DQS_N2	IO-L16N-64	AP6
DDR4_D24	IO-L23N-64	AL1
DDR4_D25	IO-L24P-64	AK3
DDR4_D26	IO-L24N-64	AK2
DDR4_D27	IO-L20P-64	AN3
DDR4_D28	IO-L23P-64	AK1
DDR4_D29	IO-L21N-64	AN1
DDR4_D30	IO-L21P-64	AM1
DDR4_D31	IO-L20N-64	AP3
DDR4_DM3	IO-L19P-64	AN2

DDR4_DQS_P3	IO-L22P-64	AL3
DDR4_DQS_N3	IO-L22N-64	AL2
DDR4_A0	IO-L12P-65	AE7
DDR4_A1	IO-L17P-65	AE3
DDR4_A2	IO-L10N-65	AF8
DDR4_A3	IO-L10P-65	AE8
DDR4_A4	IO-L11P-65	AF6
DDR4_A5	IO-L20N-65	AH3
DDR4_A6	IO-L11N-65	AG6
DDR4_A7	IO-L18N-65	AE4
DDR4_A8	IO-L16N-65	AJ5
DDR4_A9	IO-L17N-65	AF3
DDR4_A10	IO-L15N-65	AJ4
DDR4_A11	IO-L16P-65	AJ6
DDR4_A12	IO-L12N-65	AF7
DDR4_A13	IO-L18P-65	AD4
DDR4_A14	IO-L21N-65	AF1
DDR4_A15	IO-L22N-65	AJ1
DDR4_A16	IO-L21P-65	AF2
DDR4_A17	IO-L15P-65	AH4
DDR4_BA0	IO-L9N-65	AD6
DDR4_BA1	IO-L9P-65	AD7
DDR4_BG0	IO-20P-65	AG3
DDR4_nCS	IO-L22P-65	AH1
DDR4_nACT	IO-L19N-65	AJ2
DDR4_ODT	IO-L19P-65	AH2
DDR4_RESET	IO-L23P-65	AD2
DDR4_CLK_P	IO-L14P-65	AG5
DDR4_CLK_N	IO-L14N-65	AG4
DDR4_CKE	IO-L6P-65	AD10
DDR4_TEN	IO-L7N-65	AH6
DDR4_PARITY	IO-L8N-65	AH8
DDR4_nALERT	IO-L8P-65	AG8

Part 4: Carrier Board Overview

Part 4.1: Power Supply

The FPGA development board is powered by a 12V/3A adapter. After the power supply is connected, it is converted into 8V, 5V, 3.3V and other multi-channel voltages through DCDC for use by the devices on the board. Access to 12V power supply can be controlled by switching S1 switch, the detailed circuit of the power supply part can refer to the corresponding schematic diagram of the FPGA development board

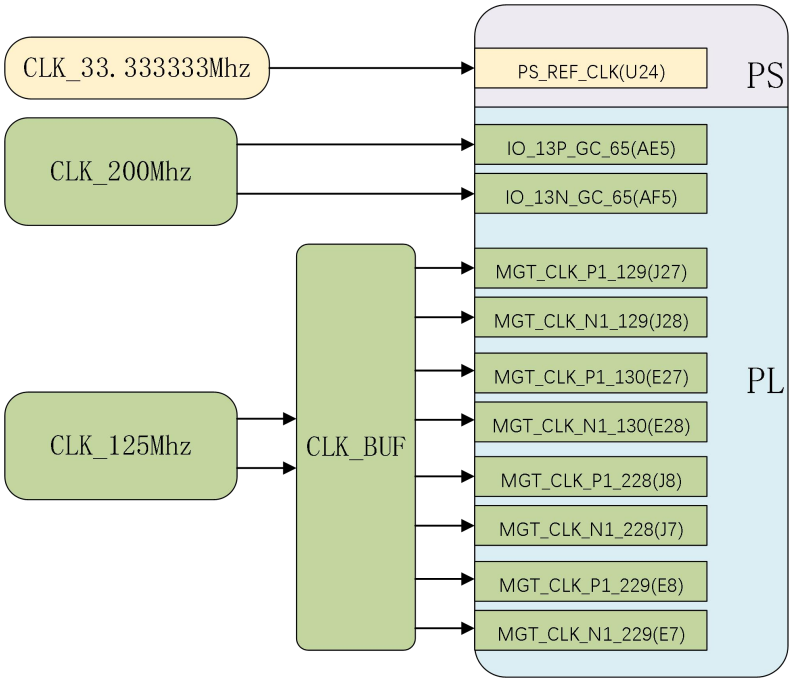


Part 4.2: System Clock

The FPGA development board clock is divided into two parts, the clock on the core board and the clock provided by the peripherals on the carrier board. The core board provides a 33.333333Mhz clock input for the PS side, and the input pin position is PS_REF_CLK; it provides a 200Mhz differential clock input for the PL side. The clock input pins on the PL side are IO_13P_GC_65/IO_13N_GC_65, and the pin position is AE5/ AF5; provides a 125Mhz differential clock input for the PL side GTX. After the 125M input is converted into 4 channels of 125M clock output through the clock buffer, they are connected to the corresponding positions as shown in the figure.

The clock chip 5P49V6965A000NLGI is used on the carrier board to configure 26/27/100Mhz, which provides the clock source for the USB3.0/Mini DP/SSD on the PS side; the clock chip 8T49N241-998NLGI is used to provide the clock source for the HDMI input and output. For detailed clock connections, please refer to page 5 of the provided

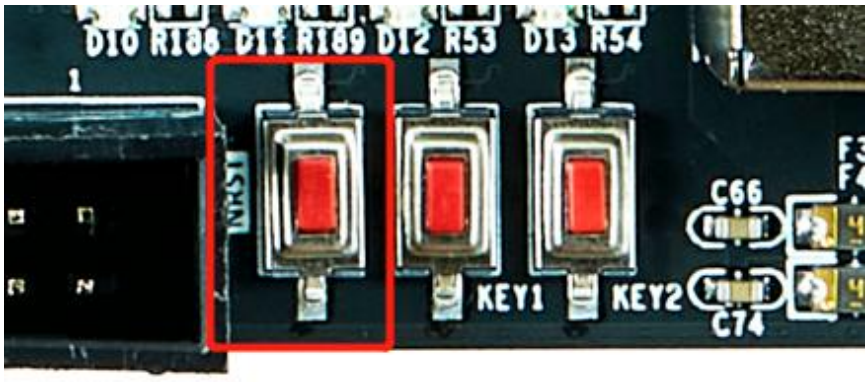
development board schematic.



Part 4.3: System Reset

The reset key is reserved on the FPGA development board and the core board. The two keys are connected together, and the user can choose the key according to the convenience. After pressing the key, a reset chip is placed on the core board, the model is MAX811TEUS. The reset pin is connected to the PS and PL terminals of the MPSOC chip respectively, the PS terminal is connected to BANK0, the corresponding pin is PS_POR_B, the pin position is V23, the BANK44IO_L7P_44 (AH14) pin on the PL side, and the AH14 pin level is 3.3V. The detailed circuit of the reset part can refer to the schematic diagram of the development board.

In addition, the reset pin is also connected to the reset pin of EMMC and Gigabit Ethernet for power-on reset.

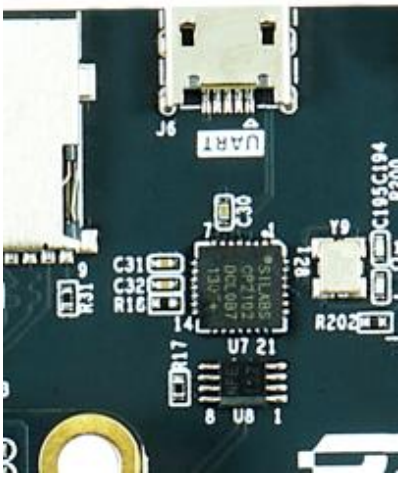


Part 4.4: USB to UART

The FPGA development board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**Micro USB**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK501**" of the "**MPSOC**", and the interface level is 1.8V, so the serial port interface adopts the level conversion to 3.3V and connects with the serial port chip. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined for the MPSOC side.

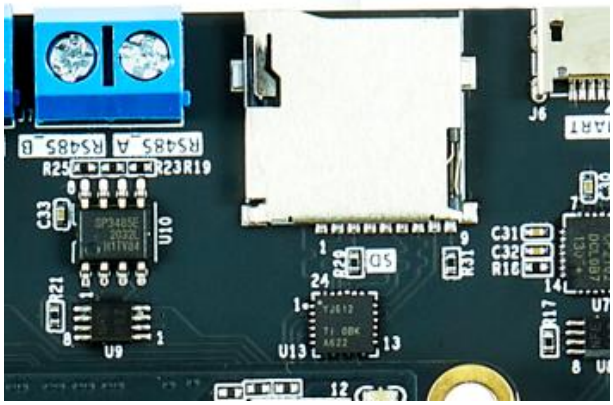
UART0 Pin	MPSOC Pin Name	Pin Position
UART0_TX	MIO_43	K24
UART0_RX	MIO_42	M24



Part 4.5: SD Card

A TF card holder is placed on the FPGA development board, which can be used for "**SD card**" startup, and is also convenient for users to debug or store files. The circuit interface level is "**1.8V**", the SD card signal is connected to the "BANK501" of the MPSOC, the "**TF card**" level is 3.3V, and the SD card signal is converted from "**1.8V**" to "**3.3V**" through a dedicated level conversion chip. The following is the signal correspondence, the detailed circuit can refer to the schematic diagram of the development board.

SD Card Pin	MPSOC Pin Name	Pin Position
SD-CLK	MIO51	N25
SD-CMD	MIO50	P25
SD-DATA0	MIO46	J25
SD-DATA1	MIO47	L25
SD-DATA2	MIO48	M25
SD-DATA3	MIO49	K25

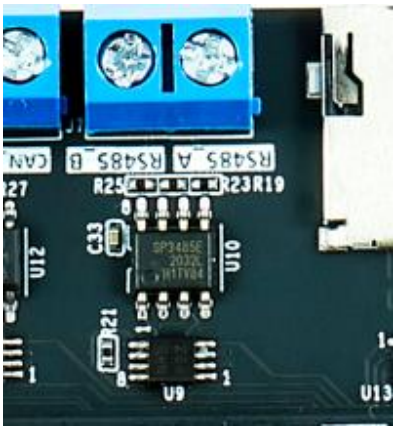


Part 4.6: RS485 Interface

The FPGA development board uses the SP3485EN chip to realize RS485 communication. The TX/RX signal of RS485 is connected to the BANK501 of the MPSOC, and the interface level is 1.8V, so the interface is level-converted to 3.3V and connected to the RS485 chip.

The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined for the MPSOC side.

RS485 Pin	MPSOC Pin Name	Pin Position
RS485_TX	MIO_40	M23
RS485_RX	MIO_41	J24



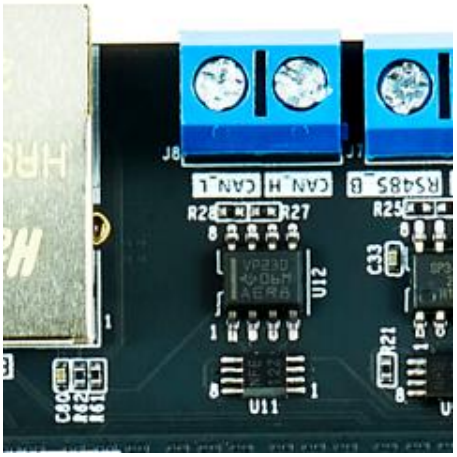
Part 4.7: CAN Bus

The FPGA development board uses the "**SN65HVD230D**" chip to implement **CAN** communication. The **TX/RX** signal of **CAN** is connected to the "**BANK501**" of the **MPSOC**, and the interface level is 1.8V, so the signal interface is level-converted to **3.3V** and

connected to the **CAN** chip.

The following is the signal correspondence table. The **TX/RX** direction is defined by the **MPSOC** terminal. For the detailed circuit, please refer to the schematic diagram of the development board.

CAN Pin	MPSOC Pin Name	Pin Position
CAN_TX	MIO_39	N23
CAN_RX	MIO_38	L23

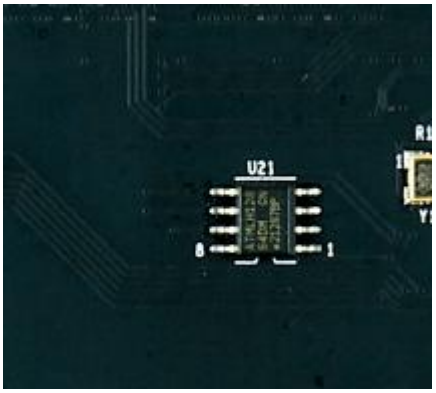


Part 4.8: E2PROM

The **64Kbit EEPROM** chip is placed on the FPGA development board, the model is AT24C64D-SSHM-T Connect with **BANK44/43** of **FPGA** through **IIC** bus. The **EEPROM** read address is **0xA1**, and the write address is **0xA0**.

The following is the pin assignment of the **EEPROM**, the detailed circuit can refer to the schematic diagram of the development board.

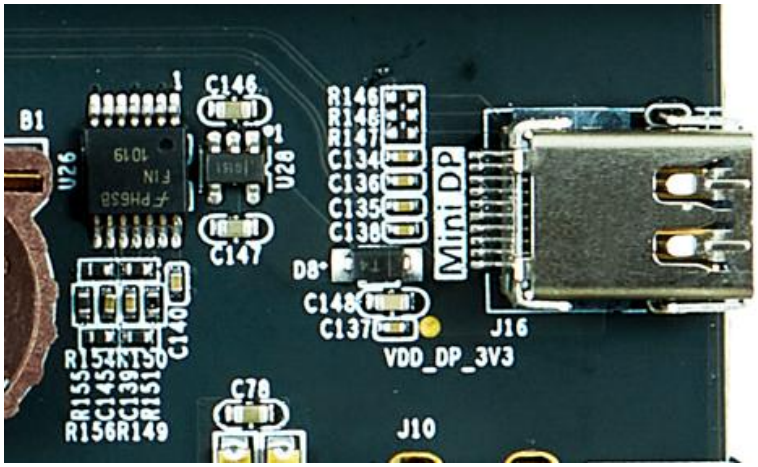
EEPROM Pin	MPSOC Pin Name	Pin Position
IIC-CLK	IO-3P-48	L18
IIC-DATA	IO-3N-48	K18



Part 4.9: Mini DP Interface

The Mini DP output interface is placed on the FPGA development board, and the interface signal is connected to the **BANK50/BANK505** of the FPGA. For details, please refer to the schematic diagram. The following is the pin assignment of Mini DP, the detailed circuit can refer to the schematic diagram of the FPGA development board.

Mini DP Pin	MPSOC Pin Name	Pin Position
DP_LINE_P0	MGT_505_TX_P3	V29
DP_LINE_N0	MGT_505_TX_N3	V30
DP_LINE_P1	MGT_505_TX_P2	W31
DP_LINE_N1	MGT_505_TX_N2	W32
DP_HPD	IO_L7N_HDGC_50	H12
DP_AUX_OUT	IO_L4N_50	D10
DP_OE	IO_L4P_50	D11
DP_AUX_IN	IO_L7P_HDGC_50	J12
DP_CLK_P_27M	MGT_505_CLK_P2	U27
DP_CLK_N_27M	MGT_505_CLK_N2	U28



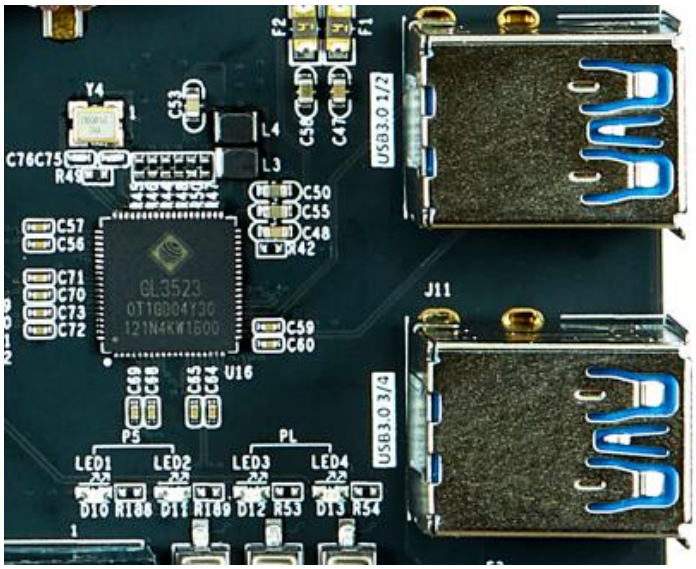
Part 4.10: USB2.0/USB3.0 Main Interface

Four **USB3.0** main interfaces are placed on the FPGA development board, and the main interfaces are compatible with **USB2.0/3.0**. The interface signal is connected with the **BANK501/BANK505** of the FPGA, please refer to the schematic diagram for details. **USB2.0** is realized by connecting the PHY chip **USB3320C-EZK** to **MIO**. **USB3.0** is extended with HUB chip **GL3523-OTY30**.

The following is the pin assignment of **USB2.0/USB3.0**, the detailed circuit can refer to the schematic diagram of the FPGA development board.

USB Pin	MPSOC Pin Name	Pin Position

USBPHY_DATA0	MIO56	C23
USBPHY_DATA1	MIO57	A23
USBPHY_DATA2	MIO54	F23
USBPHY_DATA3	MIO59	B24
USBPHY_DATA4	MIO60	E24
USBPHY_DATA5	MIO61	C24
USBPHY_DATA6	MIO62	G24
USBPHY_DATA7	MIO63	D24
USBPHY_STP	MIO58	G23
USBPHY_NXT	MIO55	B23
USBPHY_DIR	MIO53	E23
USBPHY_CLKOUT	MIO52	F22
USBPHY_RESET	MIO44	N24
GT1_USB3_SSTXP	MGT_505_TX_P1	Y29
GT1_USB3_SSTXN	MGT_505_TX_N1	Y30
GT1_USB3_SSRXP	MGT_505_RX_P1	AA31
GT1_USB3_SSRXN	MGT_505_RX_N1	AA32
USB3_CLK_P_26M	MGT_505_CLK_P1	W27
USB3_CLK_N_26M	MGT_505_CLK_N1	W28

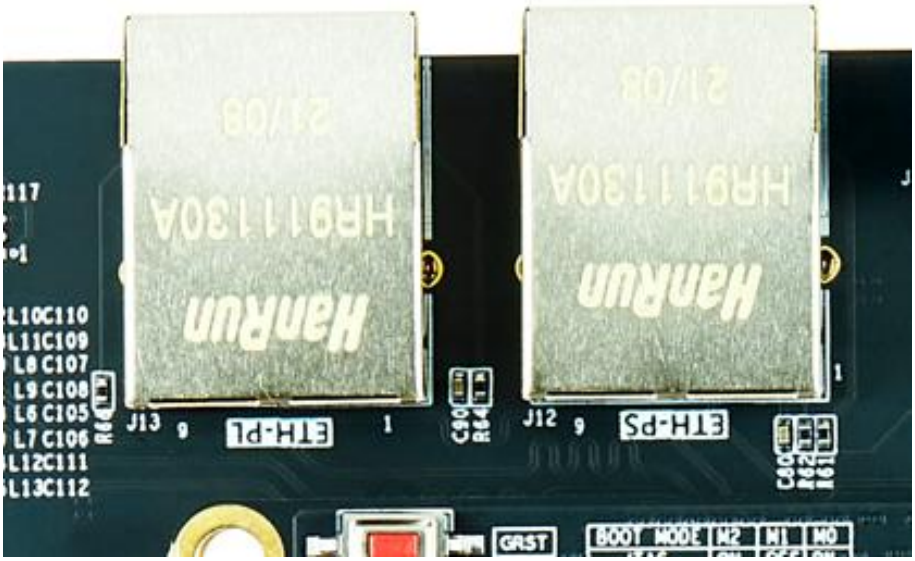


Part 4.11: Gigabit Ethernet

Two Gigabit Ethernets are designed on the FPGA development board, one for the **PS** side and one for the **PL** side, and the PS port network port has been integrated into the core board. The Ethernet chip and the **MPSOC** are interconnected through the **RGMII** interface, and the corresponding pins are shown in the following table. The address of the PS port network port is **PHY_AD[2:0]=001**, and the PL port network port address is

PHY_AD[2:0]=010. For the detailed circuit, please refer to the schematic diagram of the development board.

PS port network port		
RMGII Signal	**MPSOC Pin Name**	**Pin Position**
GTX_CLK	MIO26_501	P21
TXD0	MIO27_501	M21
TXD1	MIO28_501	N21
TXD2	MIO29_501	K22
TXD3	MIO30_501	L21
TX_EN	MIO31_501	J22
RX_CLK	MIO32_501	H22
RXD0	MIO33_501	H23
RXD1	MIO34_501	L22
RXD2	MIO35_501	P22
RXD3	MIO36_501	K23
RX_CTL	MIO37_501	N22
MDC	MIO76_502	H25
MDIO	MIO77_502	F25
PL port network port		
RMGII Signal	**MPSOC Pin Name**	**Pin Position**
TX_CLK	IO_6P _67	U11
TXD0	IO_1N _67	W11
TXD1	IO_1P _67	W12
TXD2	IO_8N _67	U6
TXD3	IO_8P _67	V6
TX_EN	IO_6N _67	T11
RX_CLK	IO_14P_MRCC_67	P10
RXD0	IO_17P_67	M11
RXD1	IO_17N_67	L11
RXD2	IO_22P_67	N13
RXD3	IO_22N_67	M13
RX_CTL	IO_14N_67	P9
PHY_nRST	IO_9P_48	D17
MDC	IO_20N_67	M14
MDIO	IO_20P_67	M15

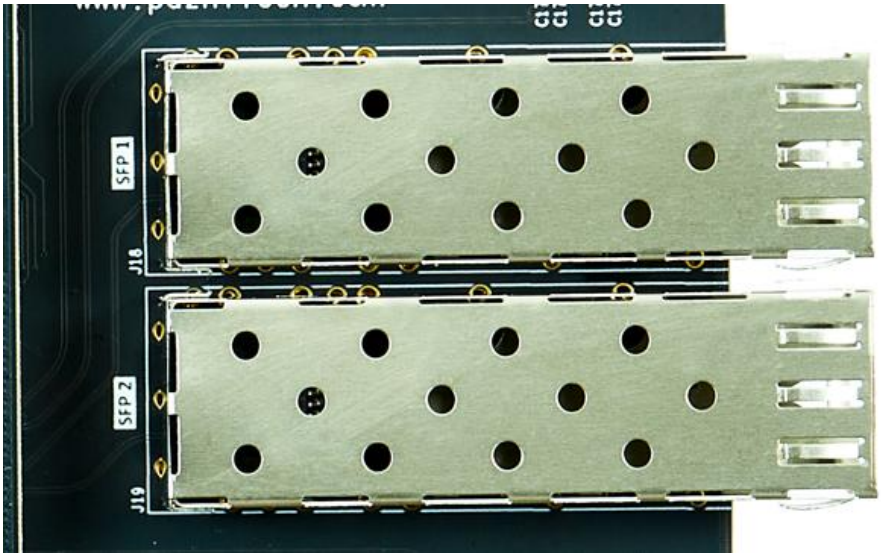


Part 4.12: SFP Interface

Two SFP interfaces are designed on the FPGA development board. The interface signals are connected to the **BANK50/BANK128** of the **MPSOC**. For details, please refer to the schematic diagram. The following is the pin assignment of **SFP**, the detailed circuit can refer to the schematic diagram of the development board.

SFP1 Pin	MPSOC Pin Name	Pin Position
SFP-TX-P1	MGT-TX-P3-128	M29
SFP-TX-N1	MGT-TX-N3-128	M30
SFP-RX-P1	MGT-RX-P3-128	M33
SFP-RX-N1	MGT-RX-N3-128	M34
SFP1-TX-DISABLE	IO-5P-HDGC_50	H11

SFP2 Pin	MPSOC Pin Name	Pin Position
SFP-TX-P2	MGT-TX-P2-128	P29
SFP-TX-N2	MGT-TX-N2-128	P30
SFP-RX-P2	MGT-RX-P2-128	N31
SFP-RX-N2	MGT-RX-N2-128	N32
SFP2-TX-DISABLE	IO-5N-HDGC_50	G11

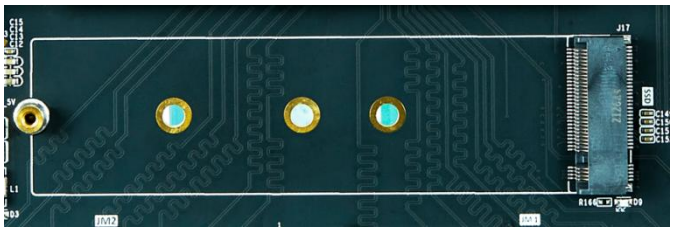


Part 4.13: SSD Interface

One SSD (x1 mode) is designed on the PS side of the FPGA development board, the interface type is M.2, and the NVME protocol is used.

The pin locations of the SSD interface are shown in the table below. For the detailed circuit, please refer to the schematic diagram of the FPGA development board.

SSD Interface	MPSOC Pin Name	Pin Position
SSD_nRST	MIO64_502	A25
REFCLK_P_100M	MGT_505_CLK_P0	AA27
REFCLK_N_100M	MGT_505_CLK_N0	AA28
GT0_SSD_TX_P0	MGT_505_TX_P0	AB29
GT0_SSD_TX_N0	MGT_505_TX_N0	AB30
GT0_SSD_RX_P0	MGT_505_RX_P0	AA33
GT0_SSD_RX_N0	MGT_505_RX_N0	AB34

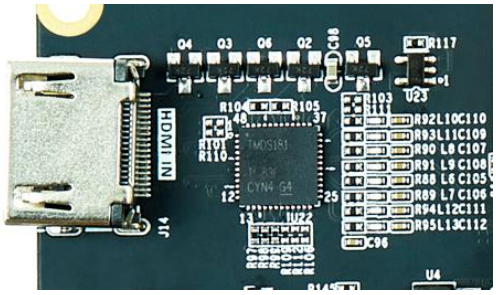


Part 4.14: HDMI Input (4K 60FPS)

The **HDMI** input interface is designed on the FPGA development board, which can realize **4K/60FPS** image input, and can adjust various resolutions and frame rates. The following table lists the corresponding relationship of the pins, and the detailed circuit can

refer to the schematic diagram of the development board.

HDMI Input Interface	MPSOC Pin Name	Pin Position
GTX_HDMI_IN_P0	MGT_RX_P0_230	D2
GTX_HDMI_IN_N0	MGT_RX_N0_230	D1
GTX_HDMI_IN_P1	MGT_RX_P1_230	C4
GTX_HDMI_IN_N1	MGT_RX_N1_230	C3
GTX_HDMI_IN_P2	MGT_RX_P2_230	B2
GTX_HDMI_IN_N2	MGT_RX_N2_230	B1
GTX_HDMI_IN_CLK_P	MGT_CLK1_P_230	B10
GTX_HDMI_IN_CLK_N	MGT_CLK1_N_230	B9
F_HDMI_IN_HPD	IO_L6P_66	Y10
F_HDMI_SCL_CTL	IO_L4P_48	L17
F_HDMI_SDA_CTL	IO_L4N_48	K17
HDMI_IN_PWR_DET	IO_L12N_48	A18

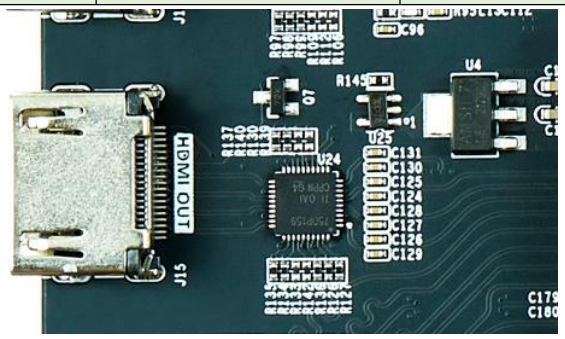


Part 4.15: HDMI Output (4K 60FPS)

The HDMI output interface is designed on the FPGA development board, which can realize 4K/60FPS image output, and various resolutions and frame rates are adjustable. The following table lists the corresponding relationship of the pins, and the detailed circuit can refer to the schematic diagram of the FPGA development board.

HDMI Input Interface	MPSOC Pin Name	Pin Position
GTX_HDMI_OUT_P0	MGT_TX_P0_230	E4
GTX_HDMI_OUT_N0	MGT_TX_N0_230	E3
GTX_HDMI_OUT_P1	MGT_TX_P1_230	D6
GTX_HDMI_OUT_N1	MGT_TX_N1_230	D5
GTX_HDMI_OUT_P2	MGT_TX_P2_230	B6
GTX_HDMI_OUT_N2	MGT_TX_N2_230	B5
GTX_HDMI_OUT_CLK_P	IO_L13P_MRCC_67	P11
GTX_HDMI_OUT_CLK_N	IO_L13N_MRCC_67	N11
F_HDMI_OUT_HPD	IO_L9N_66	W6
F_HDMI_OUT_SCL_SRC	IO_L5P_HDGC_48	G18
F_HDMI_OUT_SDA_SRC	IO_L5N_HDGC_48	G19
F_HDMI_SCL_CTL	IO_L4P_48	L17
F_HDMI_SDA_CTL	IO_L4N_48	K17

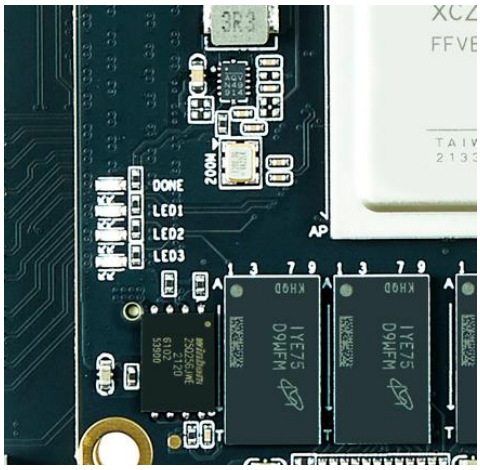
F_HDMI_OUT_OE	IO_L9P_66	W7
F_HDMI_OUT_CEC	IO_L12P_48	A17

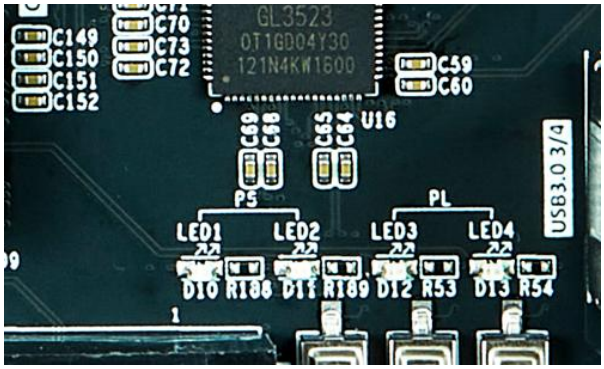


Part 4.16: LED

The core board is designed with three **LEDs**, and the FPGA development board is designed with four **LEDs**, totaling **7 LEDs**. The low level of the **LED** connected to the PS terminal is on, and the high level is off; The high level of the **LED** connected to the PL terminal is on, and the low level is off. For the detailed circuit, please refer to the schematic diagram of the FPGA development board.

LED Bit	MPSOC Pin Name	Pin Position
LED1（SOM Core Board）	IO-L7N-44	AH13
LED2（SOM Core Board）	IO-L8P-44	AJ15
LED3（SOM Core Board）	IO-L8N-44	AJ14
LED1（FPGA Board）	MIO72_502	E25
LED2（FPGA Board）	MIO74_502	G25
LED3（FPGA Board）	IO-L3P_50	F10
LED4（FPGA Board）	IO-L3N_50	E10

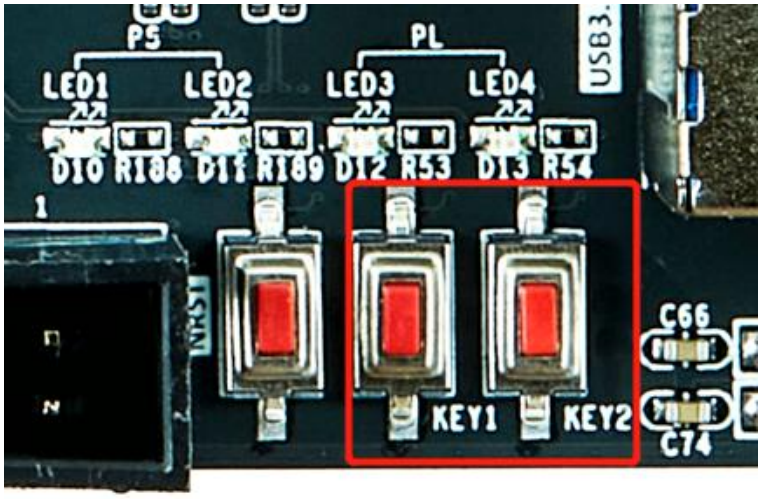




Part 4.17: KEY

The FPGA development board is designed with two KEYs. The KEY defaults to a high level, and the KEY is pressed to a low level. The KEY is connected to the PL side, and can also be assigned to the ARM side through EMIO. The pin positions of the KEYs are as follows.

KEY Bit	MPSOC Pin Name	Pin Position
KEY 1	IO-L18P-66	U5
KEY 2	IO-L18N-66	U4



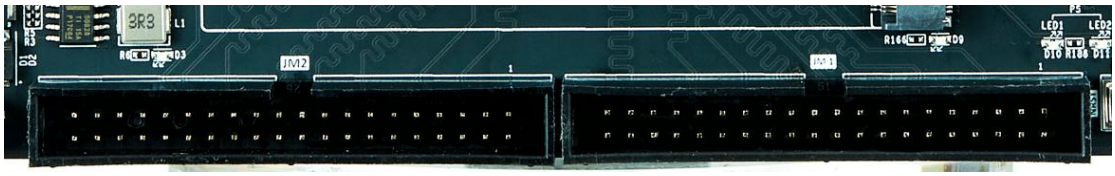
Part 4.18: 40P Expansion Port

The FPGA development board is equipped with two **40P 2.54mm** pitch simple horn sockets for extended signal connection.

The signal is connected with **BANK47/BANK48/BANK49/BANK50** of **FPGA**, and the level is **3.3V**. The following table marks the chip location where the signal is located Refer to the schematic section for detailed connection relationships.

JM1 signal sequence	MPSOC Pin Name	Pin Position	JM2 signal sequence	MPSOC Pin Name	Pin Position
5	IO_L1P_47	L20	5	IO_L1P_49	F16
7	IO_L1N_47	K20	7	IO_L1N_49	F15
9	IO_L2P_47	L19	9	IO_L2P_49	D16
11	IO_L2N_47	K19	11	IO_L2N_49	C16
13	IO_L3P_47	J21	13	IO_L3P_49	B16
15	IO_L3N_47	H21	15	IO_L3N_49	A16
17	IO_L4P_47	J19	17	IO_L4P_49	B15
19	IO_L4N_47	J20	19	IO_L4N_49	A15
21	IO_L5P_47	G21	21	IO_L5P_49	E15

23	IO_L5N_47	F21	23	IO_L5N_49	D15
25	IO_L6P_47	G20	25	IO_L6P_49	E14
27	IO_L6N_47	F20	27	IO_L6N_49	D14
29	IO_L1P_48	H18	29	IO_L1P_50	J11
31	IO_L1N_48	H19	31	IO_L1N_50	J10
37	IO_L2P_48	J17	37	IO_L2P_50	H10
39	IO_L2N_48	H17	39	IO_L2N_50	G10
6	IO_L7P_HDGC_47	E22	6	IO_L7P_HDGC_49	C14
8	IO_L7N_HDGC _47	D22	8	IO_L7N_HDGC_49	B14
10	IO_L8P_HDGC _47	E20	10	IO_L11P_49	E12
12	IO_L8N_HDGC _47	D20	12	IO_L11N_49	D12
14	IO_L9P_47	D21	14	IO_L8P_HDGC_49	C13
16	IO_L9N_47	C22	16	IO_L8N_HDGC_49	B13
18	IO_L10P_47	C21	18	IO_L10P_49	C12
20	IO_L10N_47	B21	20	IO_L10N_49	B12
22	IO_L11P_47	A21	22	IO_L9P_49	A13
24	IO_L11N_47	A22	24	IO_L9N_49	A12
26	IO_L12P_47	B20	26	IO_L12P_49	F13
28	IO_L12N_47	A20	28	IO_L12N_49	E13
30	IO_L7P_HDGC_48	E19	30	IO_L7P_HDGC_50	H16
32	IO_L7N_HDGC _48	D19	32	IO_L7N_HDGC_50	G16
38	IO_L8P_HDGC _48	E17	38	IO_L8P_HDGC_50	J16
40	IO_L8N_HDGC _48	E18	40	IO_L8N_HDGC_50	J15



Part 4.19: FMC-HPC Expansion Port

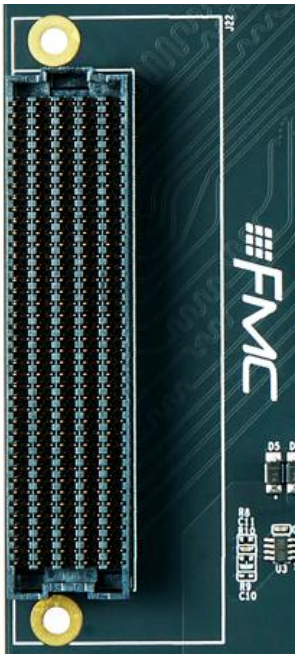
One **FMC-HPC** connector is designed on the FPGA development board, and the signal correspondence is listed in the following table. Refer to the schematic section for detailed connection relationships.

FMC-HPC Pin	MPSOC Pin Name	Pin Position
LA00_P_CC	IO_L11P_SRCC_67	R10
LA00_N_CC	IO_L11N_SRCC_67	R9
LA01_P_CC	IO_L19P_67	L16
LA01_N_CC	IO_L19N_67	K16
LA02_P	IO_L21P_67	P12
LA02_N	IO_L21N_67	N12
LA03_P	IO_L10P_67	T7
LA03_N	IO_L10N_67	T6
LA04_P	IO_L24P_67	L15
LA04_N	IO_L24N_67	K15

LA05_P	IO_L23P_67	L13
LA05_N	IO_L23N_67	K13
LA06_P	IO_L2P_67	T13
LA06_N	IO_L2N_67	R13
LA07_P	IO_L9P_67	U9
LA07_N	IO_L9N_67	U8
LA08_P	IO_L16P_67	N9
LA08_N	IO_L16N_67	N8
LA09_P	IO_L18P_67	L12
LA09_N	IO_L18N_67	K12
LA10_P	IO_L4P_67	T12
LA10_N	IO_L4N_67	R12
LA11_P	IO_L7P_67	V8
LA11_N	IO_L7N_67	V7
LA12_P	IO_L3P_67	U10
LA12_N	IO_L3N_67	T10
LA13_P	IO_L15P_67	M10
LA13_N	IO_L15N_67	L10
LA14_P	IO_L5P_67	V12
LA14_N	IO_L5N_67	V11
LA15_P	IO_L23P_66	V2
LA15_N	IO_L23N_66	V1
LA16_P	IO_L2P_66	AB11
LA16_N	IO_L2N_66	AB10
LA17_P_CC	IO_L13P_MRCC_66	Y4
LA17_N_CC	IO_L13N_MRCC_66	Y3
LA18_P_CC	IO_L14P_SRCC_66	Y5
LA18_N_CC	IO_L14N_SRCC_66	AA5
LA19_P	IO_L22P_66	Y2
LA19_N	IO_L22N_66	Y1
LA20_P	IO_L5P_66	Y12
LA20_N	IO_L5N_66	AA12
LA21_P	IO_L24P_66	W2
LA21_N	IO_L24N_66	W1
LA22_P	IO_L3P_66	AA11
LA22_N	IO_L3N_66	AA10
LA23_P	IO_L17P_66	V4
LA23_N	IO_L17N_66	V3
LA24_P	IO_L21P_66	AA2
LA24_N	IO_L21N_66	AA1
LA25_P	IO_L1P_66	AC12
LA25_N	IO_L1N_66	AC11
LA26_P	IO_L10P_66	AB6
LA26_N	IO_L10N_66	AB5
LA27_P	IO_L15P_66	W5
LA27_N	IO_L15N_66	W4
LA28_P	IO_L16P_66	AB4

LA28_N	IO_L16N_66	AC4
LA29_P	IO_L8P_66	AB8
LA29_N	IO_L8N_66	AC8
LA30_P	IO_L19P_66	AC2
LA30_N	IO_L19N_66	AC1
LA31_P	IO_L7P_66	AC7
LA31_N	IO_L7N_66	AC6
LA32_P	IO_L20P_66	AB3
LA32_N	IO_L20N_66	AC3
LA33_P	IO_L4P_66	AB9
LA33_N	IO_L4N_66	AC9
FMC_PWRGD	IO_11N_48	C19
FMC_PRSNT	IO_11P_48	C18
FMC_IIC_SCL	IO_6P_HDGC_50	F12
FMC_IIC_SDA	IO_6N_HDGC_50	F11
DP0_M2C_P	MGT_RX_P1_229	J4
DP0_M2C_N	MGT_RX_N1_229	J3
DP1_M2C_P	MGT_RX_P3_229	F2
DP1_M2C_N	MGT_RX_N3_229	F1
DP2_M2C_P	MGT_RX_P2_229	H2
DP2_M2C_N	MGT_RX_N2_229	H1
DP3_M2C_P	MGT_RX_P0_229	K2
DP3_M2C_N	MGT_RX_N0_229	K1
DP4_M2C_P	MGT_RX_P2_228	M2
DP4_M2C_N	MGT_RX_N2_228	M1
DP5_M2C_P	MGT_RX_P0_228	T2
DP5_M2C_N	MGT_RX_N0_228	T1
DP6_M2C_P	MGT_RX_P1_228	P2
DP6_M2C_N	MGT_RX_N1_228	P1
DP7_M2C_P	MGT_RX_P3_228	L4
DP7_M2C_N	MGT_RX_N3_228	L3
GBTCLK0_M2C_P	MGT_CLK0_P_229	G8
GBTCLK0_M2C_N	MGT_CLK0_N_229	G7
GBTCLK1_M2C_P	MGT_CLK0_P_228	L8
GBTCLK1_M2C_N	MGT_CLK0_N_228	L7
DP0_C2M_P	MGT_TX_P1_229	H6
DP0_C2M_N	MGT_TX_N1_229	H5
DP1_C2M_P	MGT_TX_P3_229	F6
DP1_C2M_N	MGT_TX_N3_229	F5
DP2_C2M_P	MGT_TX_P2_229	G4
DP2_C2M_N	MGT_TX_N2_229	G3
DP3_C2M_P	MGT_TX_P0_229	K6
DP3_C2M_N	MGT_TX_N0_229	K5
DP4_C2M_P	MGT_TX_P2_228	N4
DP4_C2M_N	MGT_TX_N2_228	N3
DP5_C2M_P	MGT_TX_P0_228	R4
DP5_C2M_N	MGT_TX_N0_228	R3

DP6_C2M_P	MGT_TX_P1_228	P6
DP6_C2M_N	MGT_TX_N1_228	P5
DP7_C2M_P	MGT_TX_P3_228	M6
DP7_C2M_N	MGT_TX_N3_228	M5



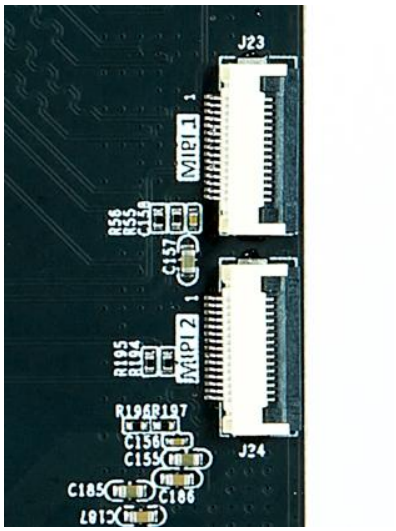
Part 4.20: Dual MIPI CSI interface

The FPGA development board has designed a dual **mipi csi** interface. The following table lists the corresponding relationship of **mipi** signals.

MIPI1 Signal	MPSOC Pin Name	Pin Position
MIPI1_D_P0	IO_23P_66	V2
MIPI1_D_N0	IO_23N_66	V1
MIPI1_D_P1	IO_24P_66	W2
MIPI1_D_N1	IO_24N_66	W1
MIPI1_CLK_P	IO_22P_66	Y2
MIPI1_CLK_N	IO_22N_66	Y1
CAM1_GPIO	IO_10N_50	H14
CAM1_CLK	IO_10P_50	J14
CAM1_SCL	IO_9P_50	G15
CAM1_SDA	IO_9N_50	G14

MIPI2 Signal	MPSOC Pin Name	Pin Position

MIPI2_D_P0	IO_21P_66	AA2
MIPI2_D_N0	IO_21N_66	AA1
MIPI2_D_P1	IO_20P_66	AB3
MIPI2_D_N1	IO_20N_66	AC3
MIPI2_CLK_P	IO_19P_66	AC2
MIPI2_CLK_N	IO_19N_66	AC1
CAM2_GPIO	IO_L8N_HDGC_50	G13
CAM2_CLK	IO_L8P_HDGC_50	H13
CAM2_SCL	IO_L6P_HDGC_50	F12
CAM2_SDA	IO_L6N_HDGC_50	F11



Part 4.21: USB to JTAG Programmer

The FPGA development board has a **USB** to **JTAG** Programmer onboard. After installing the **Vivado** software, use a **USB** cable to connect the USB port corresponding to JTAG. You can realize debugging and downloading, which is very convenient. The following is the location diagram of the interface on the FPGA development board.