ARTIX-7 FPGA Development Board AX7035

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2019-04-26	Rachel Zhou	First Release

Table of Contents

The AX7035 FPGA development board, it is the ARTIX-7 FPGA development platform.

The ARTIX-7 FPGA development platform uses XILINX's ARTIX-7 chip, and theAX7035 FPGA development board are designed with a rich peripheral interface. For example, one HDMI input interface, one HDMI output interface, one Gigabit Ethernet interface, one USB2.0 interface, Uart interface, downloader interface and two 40-pin expansion ports, and so on.It meets user's requirements for high-speed data transmission, video processing and industrial control. It is a "Versatile" ARTIX-7 FPGA development platform. It provides the possibility for pre-verification and post-application of high-speed video transmission, data communication, image processing and data processing. This product is very suitable for students, engineers and other groups engaged in FPGA development.
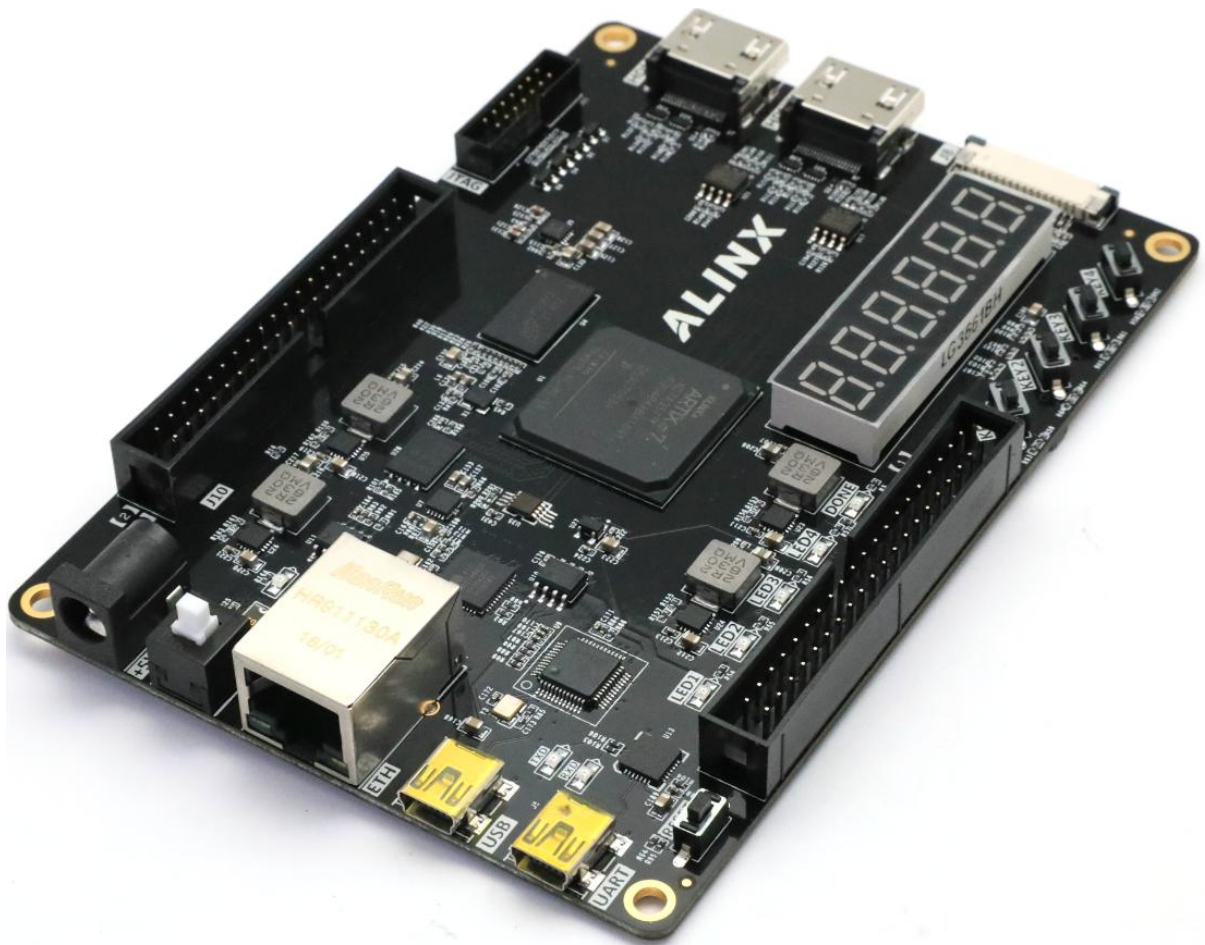
Part 1: FPGA Development Board Introduction

The AX7035 FPGA development board uses Xilinx's ARTIX-7 series of FPGA chipsXC7A35T-2FGG484I, 484-pin FBGA package. The FPGA chip is connected with a 256M byte DDR3 memory chip to achieve high-speed data reading and writing between FPGA and DDR3. The data bit width is 16 bits, the DDR read/write clock frequency reaches 400Mhz, and the bandwidth of the whole system is up to 12.8Gb/s. (800M*16bit), which satisfies the data buffer requirement during data processing. A 128Mbit QSPI FLASH is used as an FPGA configuration chip to store FPGA configuration files and some user data.

The AX7035 FPGA development board has expanded a wide range of peripheral interfaces, including one HDMI output interface, one HDMI input interface, one Gigabit Ethernet interface, one USB2.0 interface, one UART serial interface, one SD card interface, two 40-pin Expansion port, keys, LEDs, EEPROM and sensor circuits.
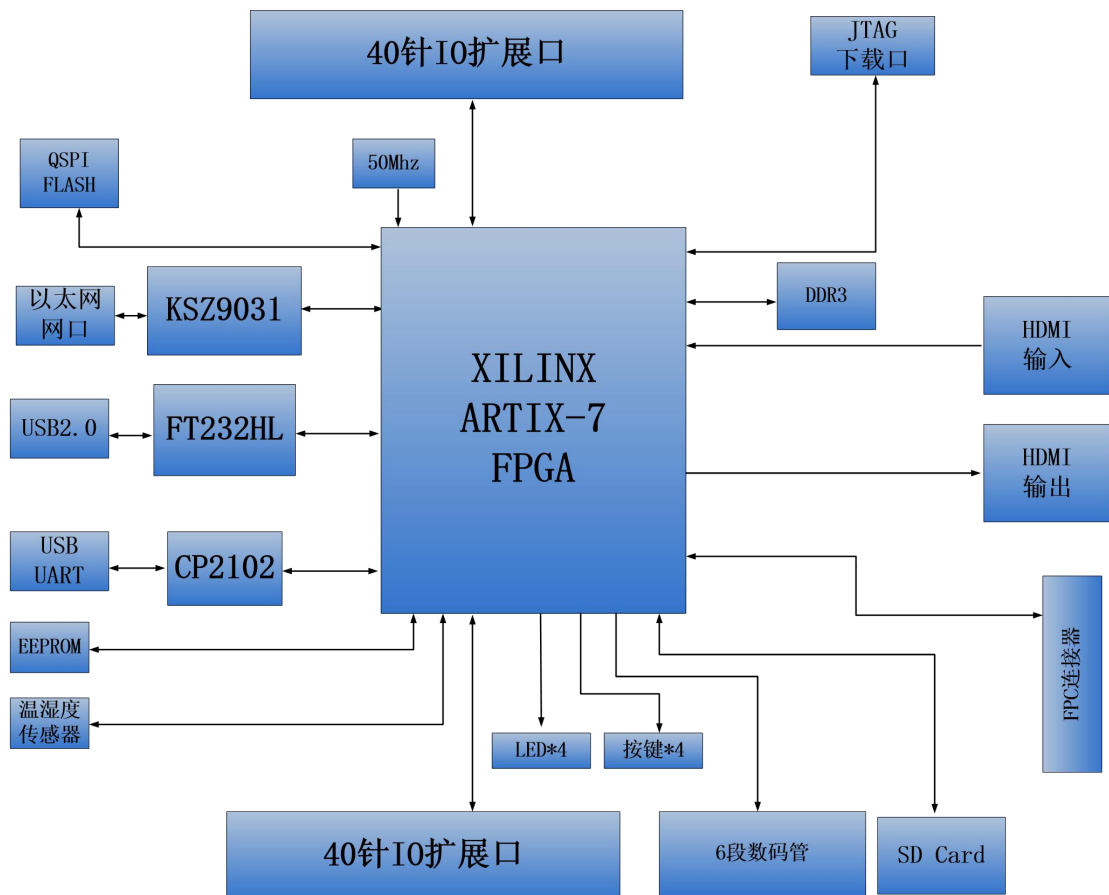
Figure 1-1: TheSchematic Diagram of the AX7035

Through this diagram, you can see the interfaces and functions that the AX7035FPGA Development Board contains:

➢ Xilinx ARTIX-7 Series FPGA Chip XC7A35T-2FGG484I

➢ A large-capacity 2Gbit (256MB) high-speed DDR3 SDRAM can be used as a buffer for FPGA chip data

➢ A 50Mhz active crystal onboard provides a stable clock source for the FPGA system

➢ 1-channelGigabit Ethernet InterfaceRJ-45 interface

The Gigabit Ethernet interface chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide network communication services to users. KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate; full duplex and adaptive

➢ 1-channel HDMI image video output interface

Supports up to 1080P@60Hz output and supports data output in different formats

➢ 1-channel HDMI image video input interface

Supports up to 720P@60Hz input and supports data input in different formats

➢ 1-channel high speed USB2.0 interface

Using FT232H single-channel USB chip of FTDI, it can be used for USB2.0 high-speed communication between development board and PC, with a maximum speed of 480Mb/s.

➢ 1-channel USB Uart interface

1-channel Uart to USB interface for communication with the computer for user debugging. The serial port chip adopts the USB-UAR chip of Silicon LabsCP2102GM, and the USB interface adopts the MINI USB interface.

➢ Micro SD slot

1-channel Micro SDslot, supports SD mode and SPI mode.

➢ A 6-digit digital tube that dynamically displays 6 digits.

➢ Temperature and humidity sensor

Onboard a temperature and humidity sensor chip LM75 for detecting the temperature and humidity of the environment around the board

➢ 2-channel40-pin expansion port

Reserve 2 40-pin 2.54mm pitch expansion ports, which can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1 channel 5V power supply, 2 channel 3.3V power supply, 3 way ground, 34 IOs port.

➢ 1-channel   FPC expansion port

A 15-pin FPC expansion port is reserved for connecting the user's MIPI camera module.

- ➤ JTAG Interface

  A 10-pin0.1 spacing standard JTAG ports for FPGA program download and debugging.

- ➤ Key

  1 reset key, 4 user keys

- ➤ LED Light

  6LEDs, 1 power indicator, 1 DONE configuration indicator, 2 serial transmit and receive indicators, 4 user LEDs.

Part 2: Structure Diagram

The size of the development board is a compact 130mm x 90mm, and the PCB is designed with an 8-layer board. There are 4 screw positioning holes around the FPGA board for fixing the development board. The hole diameter of the positioning hole is 3.5mm (diameter)
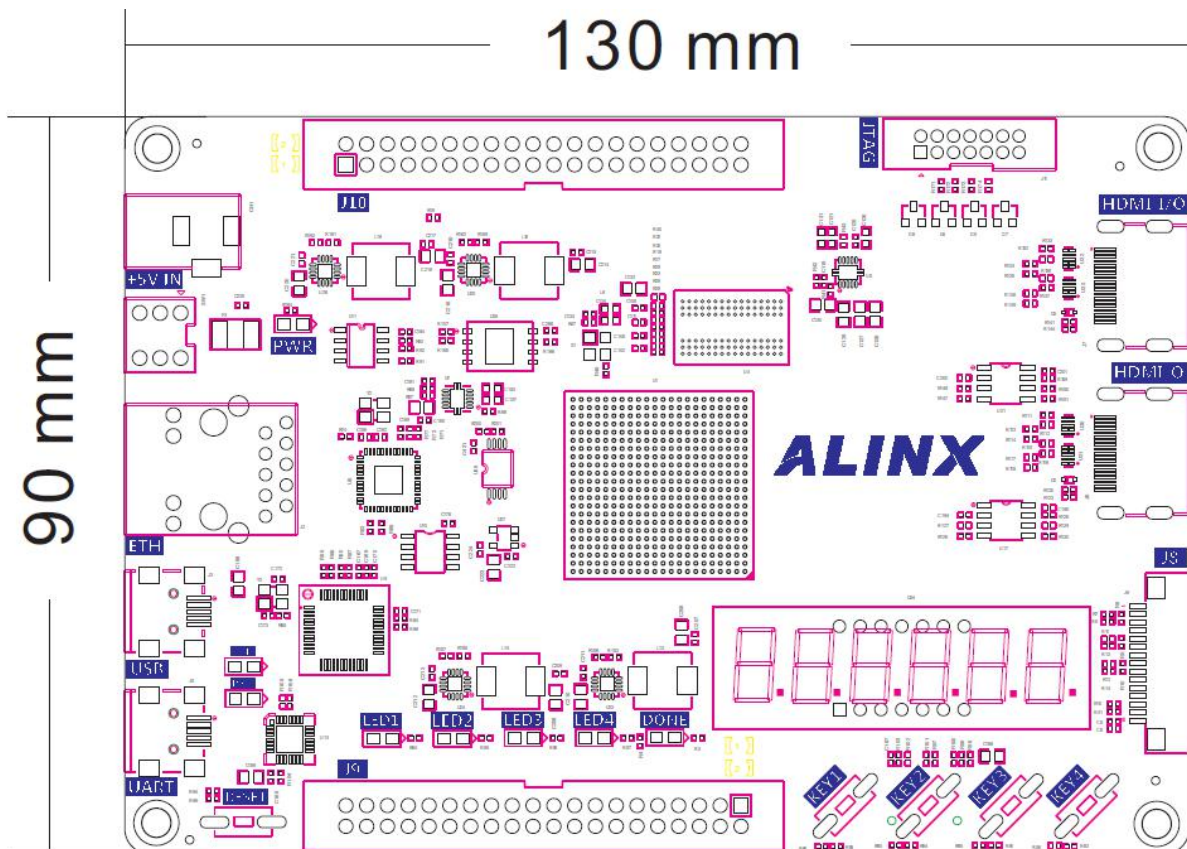

Figure 2-1: Structure Diagram

Part 3: Power Supply

The power supply voltage of the AX7035 FPGA development board is DC5V, and Figure 3-1 is the power supply schematic:
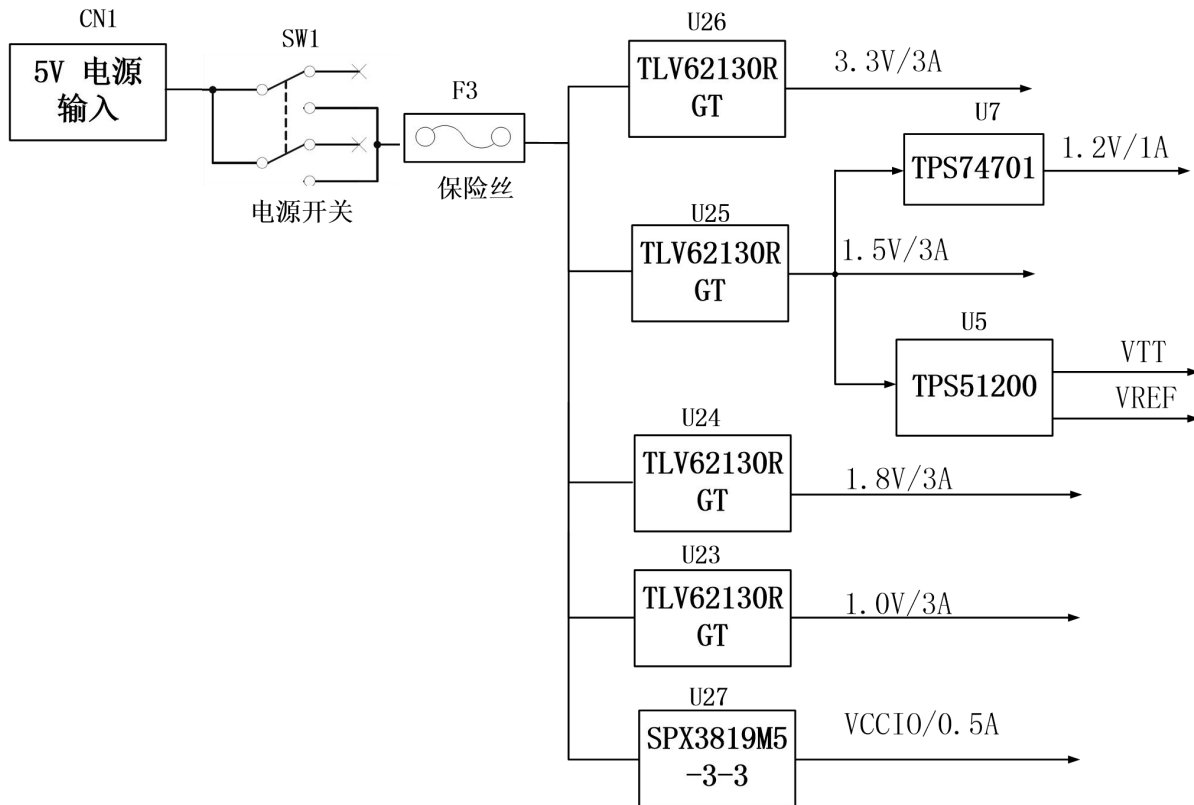

Figure 3-1: Power Supply Schematic

The development board is powered by +5V and converted to +3.3V, +1.5V, +1.8V, +1.0V four-way power supply through four DC/DC power supply chip TLV62130RGT. The output current can be up to 3A per channel. VCCIO is generated by one LDOSPX3819M5-3-3. VCCIO mainly supplies power to BANK16 of FPGA. Users can change the IO of BANK16 to different voltage standards by replacing their LDO chip. 1.5V generates the VTT and VREF voltages required by DDR3 via TI's TPS51200.In addition, 1.5V generates 1.2V to power the network interface chip through an LDO chip TPS74701. The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	FPGACore VoltageVCCINT, VCCBRAM
+1.8V	FPGA auxiliary voltageVCCAUX, VCCBATT,ADC power supply VCCADC
+3.3V	VCCIO ofFPGA, Ethernet, Serial port, HDMI, Sensor, FLASH, EEPROM, and SD Card
+1.5V	DDR3, Bank34 of FPGA
VREF,VTT	DDR3
VCCIO	FPGA Bank16

Because the power supply of Artix-7 FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is 1.0V->1.8V->1.5 V->3.3V->VCCIO.

Part 4: FPGA Chip

As mentioned above, the FPGA model we use is XC7A35T-2FGG484I, which belongs to Xilinx's Artix-7 series. The speed grade is 2, and the temperature grade is industry grade. This model is a FGG484 package with 484 pins. Xilinx ARTIX-7 FPGA chip naming rules as below
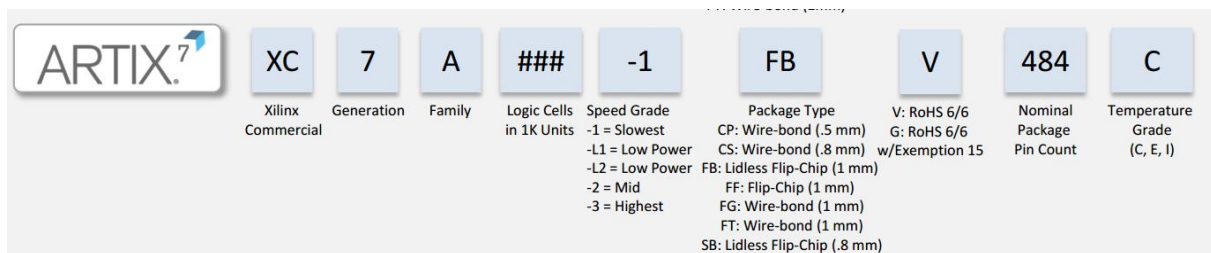

Figure 4-1: The Specific Chip Model Definition of ARTIX-7 Series

Figure 4-2: FPGA chip on board

The main parameters of the FPGA chip XC7A35T are as follows

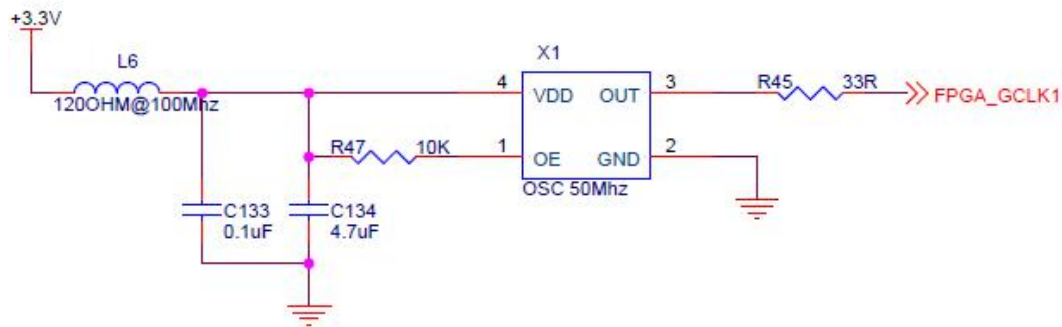| Name	Specific parameters
Logic Cells	33,280
Slices	5,200
CLB flip-flops	41,600
Block RAM（kb）	1,800
DSP Slices	90
Speed Grade	-2
Temperature Grade	Industrial

FPGA power supply system

Artix-7 FPGA power supplies are V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the FPGA core power supply pin, which needs to be connected to 1.0V; V_{CCBRAM} is the power supply pin of FPGA block RAM, connect to 1.0V; V_{CCAUX} is FPGA auxiliary power supply pin, connect 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK14~16, BANK34~35. On AX7035 FPGA development board, BANK34 need to be connected to DDR3, the voltage connection of BANK is 1.5V, and the voltage of other BANK is 3.3V. The V_{CCO} of BANK16 is powered by the LDO, and can be changed by replacing the LDO chip. Because the GTP transceiver function is not used here, the development board does not provide GTP power.

The Artix-7 FPGA system requires that the power-up sequence be powered by V_{CCINT}, then V_{CCBRAM}, then V_{CCAUX} and finally V_{CCO}. If V_{CCINT} and V_{CCBRAM} have the same voltage, they can be powered up at the same time. The order of power outages is reversed.

Part 5: 50M active crystal oscillator

The Sitime 50M active crystal is provided on the development board to the FPGA as the system clock input. The crystal output is connected to the FPGA's global clock (GCLK Pin Y18). This GCLK can be used to drive the user logic

within the FPGA. The user can configure the FPGA's internal PLL and MMCM to achieve a higher clock.
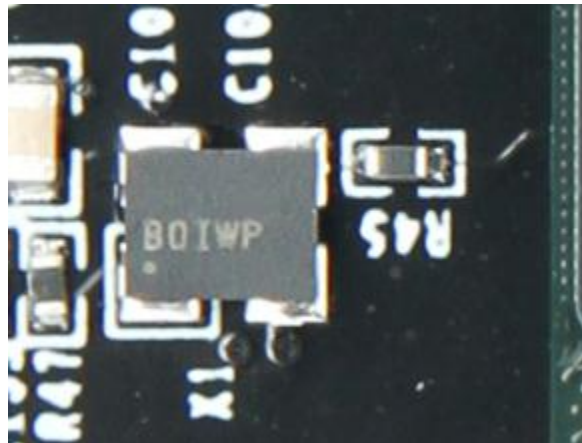

Figure 5-1: 50M active crystal oscillator

Figure 5-2: 50M active crystal oscillator on the FPGA Board

Clock Pin Assignment

Net Name	FPGA PIN
FPGA_GCLK1	V10

Part 6:DDR3 DRAM

TheAX7035 FPGA development board is equipped with one Micron 2Gbit (256MB) DDR3 chips, model MT41J128M16HA-125. DDR bus width is 16bit. The DDR3 SDRAM has a maximum operating speed of 400MHz (data rate 800Mbps). The DDR3 memory system is directly connected to the memory

interface of the BANK 34 of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 6-1.

Bit Number	Chip Model	Capacity	Factory
U4	MT41J128M16HA-125	128M x 16bit	Micron

Table 6-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.
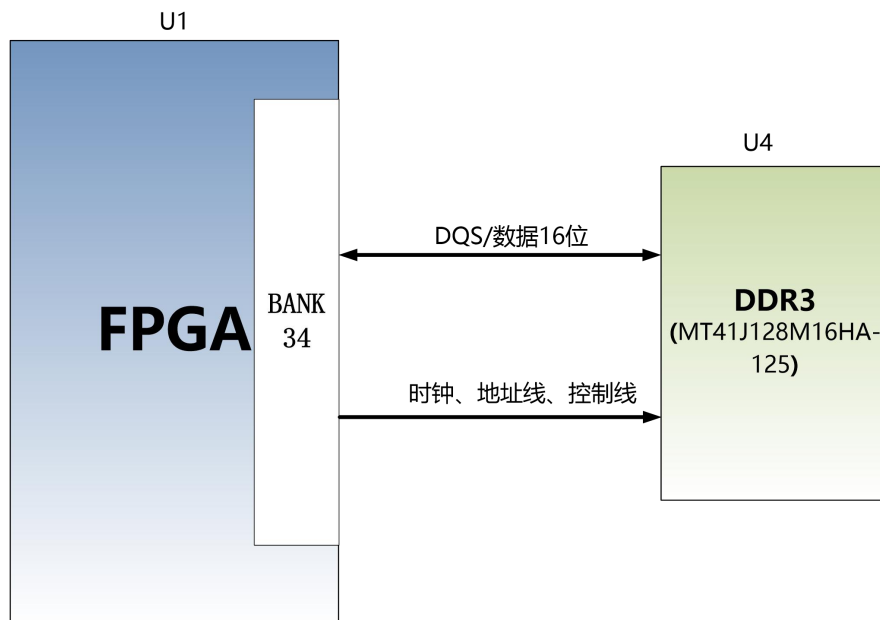

Figure 6-1: The DDR3 DRAM Schematic

Figure 6-2: The DDR3 on the FPGA Board

DDR3 DRAM pin assignment:

Net Name	FPGA PIN Name	FPGA P/N
DDR3_LDQS_P	IO_L9P_T1_DQS_34	Y3
DDR3_LDQS_N	IO_L9N_T1_DQS_34	AA3
DDR3_UDQS_P	IO_L3P_T0_DQS_34	R3
DDR3_UDQS_N	IO_L3N_T0_DQS_34	R2
DDR3_DQ[0]	IO_L12P_T1_MRCC_34	V4
DDR3_DQ [1]	IO_L8N_T1_34	AB2
DDR3_DQ [2]	IO_L8P_T1_34	AB3
DDR3_DQ [3]	IO_L7P_T1_34	AA1
DDR3_DQ [4]	IO_L10P_T1_34	AA5
DDR3_DQ [5]	IO_L11P_T1_SRCC_34	Y4
DDR3_DQ [6]	IO_L10N_T1_34	AB5
DDR3_DQ [7]	IO_L11N_T1_SRCC_34	AA4
DDR3_DQ [8]	IO_L2N_T0_34	V2
DDR3_DQ [9]	IO_L5N_T0_34	Y1
DDR3_DQ [10]	IO_L1N_T0_34	U1
DDR3_DQ [11]	IO_L4N_T0_34	Y2
DDR3_DQ [12]	IO_L1P_T0_34	T1
DDR3_DQ [13]	IO_L5P_T0_34	W1
DDR3_DQ [14]	IO_L2P_T0_34	U2
DDR3_DQ [15]	IO_L6P_T0_34	U3
DDR3_LDM	IO_L7N_T1_34	AB1
DDR3_UDM	IO_L4P_T0_34	W2
DDR3_A[0]	IO_L22P_T3_34	AA8
DDR3_A[1]	O_L14N_T2_SRCC_34	U5
DDR3_A[2]	IO_L24N_T3_34	Y9
DDR3_A[3]	IO_L23P_T3_34	Y8
DDR3_A[4]	IO_L16N_T2_34	V5
DDR3_A[5]	IO_L19N_T3_VREF_34	W7
DDR3_A[6]	IO_L16P_T2_34	U6
DDR3_A[7]	IO_L19P_T3_34	V7
DDR3_A[8]	IO_L14P_T2_SRCC_34	T5
DDR3_A[9]	O_L24P_T3_34	W9
DDR3_A[10]	IO_L18N_T2_34	AA6
DDR3_A[11]	IO_L17N_T2_34	T6

DDR3_A[12]	IO_L18P_T2_34	Y6
DDR3_A[13]	IO_L17P_T2_34	R6
DDR3_BA[0]	IO_L22N_T3_34	AB8
DDR3_BA[1]	IO_L15N_T2_DQS_34	W5
DDR3_BA[2]	IO_L23N_T3_34	Y7
DDR3_S0	IO_25_34	U7
DDR3_RAS	IO_L20P_T3_34	AB7
DDR3_CAS	IO_L13N_T2_MRCC_34	T4
DDR3_WE	IO_L15P_T2_DQS_34	W6
DDR3_ODT	IO_L20N_T3_34	AB6
DDR3_RESET	IO_0_34	T3
DDR3_CLK_P	IO_L21P_T3_DQS_34	V9
DDR3_CLK_N	IO_L21N_T3_DQS_34	V8
DDR3_CKE	IO_L13P_T2_MRCC_34	R4

Part 7: QSPI Flash

The AX7035 FPGA development board is equipped with one128MBit QSPI FLASH, and the model is N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, core application code and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 7-1.

Position	Model	Capacity	Factory
U8	N25Q128	128M Bit	Numonyx

Table 7-1: QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip select signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 7-1 shows the hardware connection of QSPI Flash.
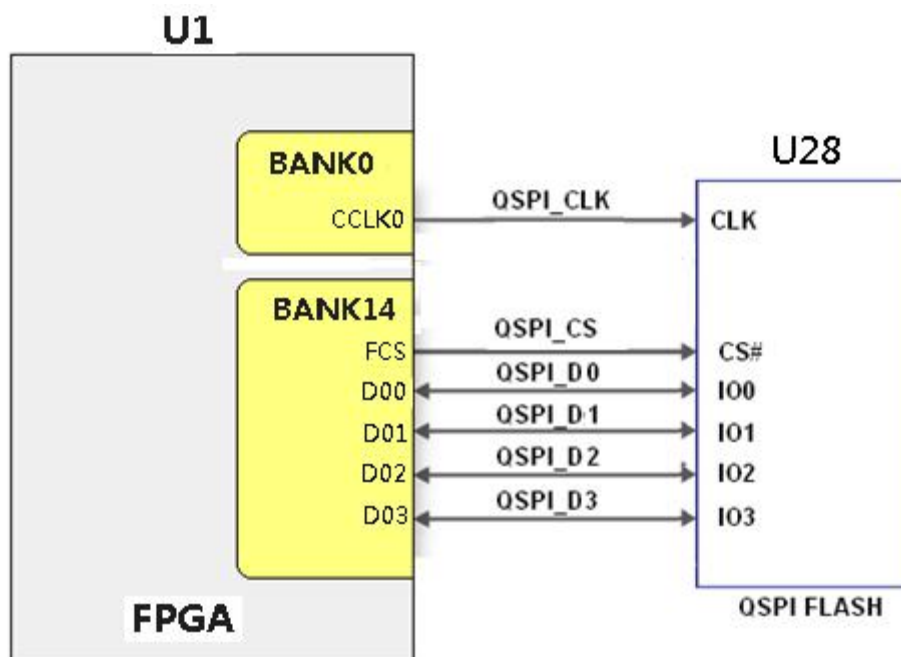
Figure 7-1: QSPI Flash Schematic

QSPI Flash pin assignments:

Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

Figure 7-2: QSPI on the FPGA Board

Part 8: Gigabit Ethernet Interface

The AX7035 development board provides network communication services to users through a Micrel KSZ9031RNX Ethernet PHY chip. The Ethernet PHY chip is connected to the IO interface of the ARTIX7 FPGA. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, supports MDIO bus for PHY register management.

TheKSZ9031RNXwill detect the level status of some specific IOs to determine their working mode after powered on. Table 8-1 describes the default setup information after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 8-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip KSZ9031RNXis communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising and falling of the clock.
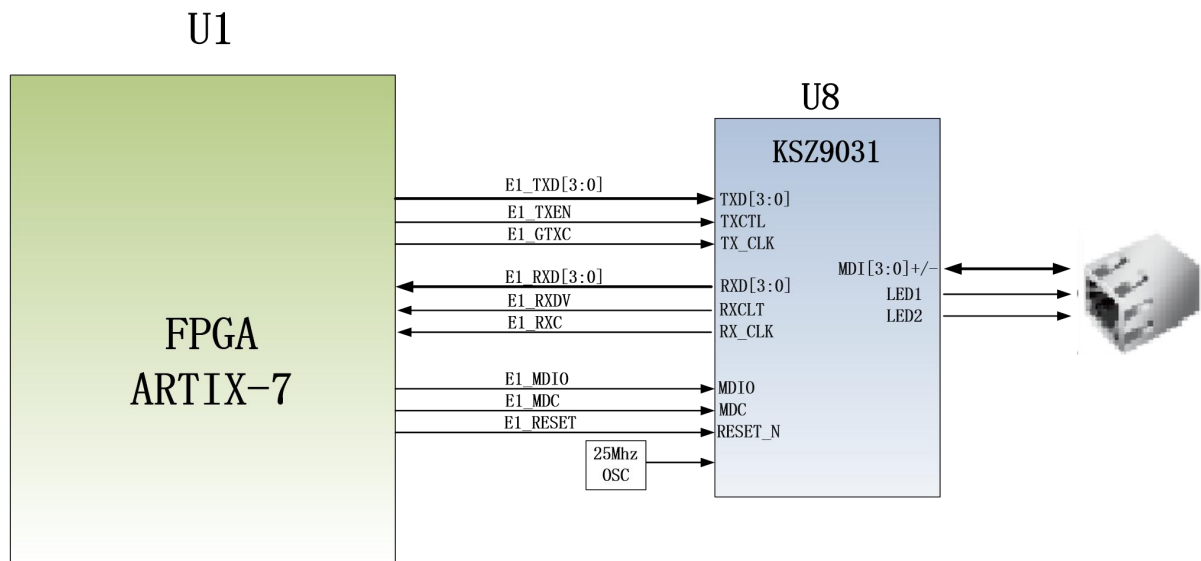
When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip KSZ9031RNXis communicated through the RMII bus, the transmission clock is 25Mhz,and the data is sampled on the rising and falling of the clock.
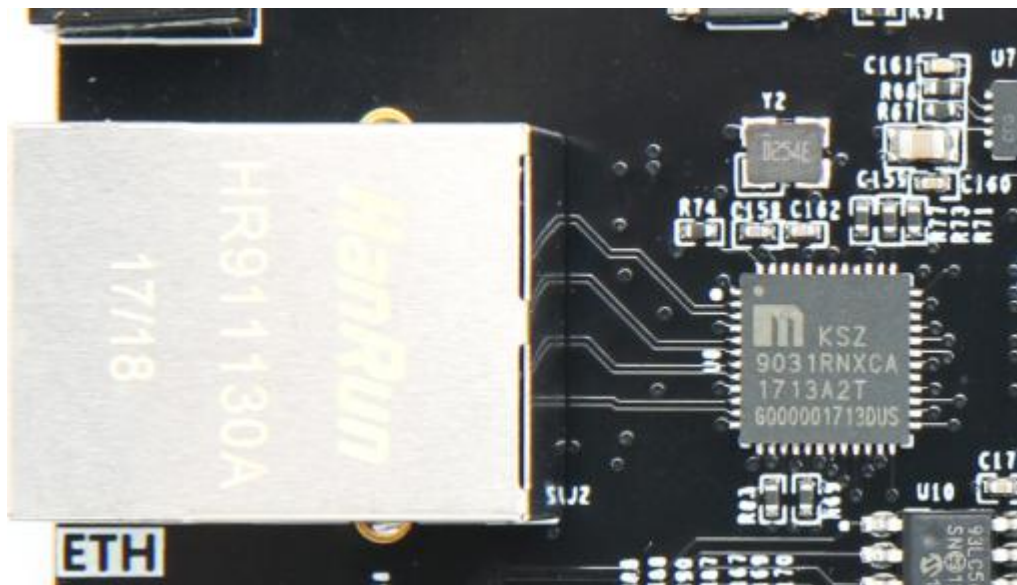
Figure 8-1: Gigabit Ethernet Interface Schematic

Figure 8-2: Gigabit Ethernet interface on the board

Ethernet chip pin assignments are as follows:

Signal Name	FPGA Pin	Description
E1_GTXC	L14	RGMII transmit clock
E1_TXD0	J21	Transmit Data bit0
E1_TXD1	M20	Transmit Data bit1
E1_TXD2	L18	Transmit Data bit2

E1_TXD3	L20	Transmit Data bit3
E1_TXEN	L19	Transmit enable signal
E1_RXC	K18	RGMII receive clock
E1_RXD0	K19	Receive Data Bit0
E1_RXD1	M15	Receive Data Bit1
E1_RXD2	J17	Receive Data Bit2
E1_RXD3	J20	Receive Data Bit3
E1_RXDV	M21	Receive data valid signal
E1_MDC	K17	MDIO Management Clock
E1_MDIO	K16	MDIO Management Data
E1_RESET	L15	PHY Reset Signal

Part 9: HDMI1 Output interface

The implementation of the HDMI output interface on the AX7035 development board is to directly connect the differential signal and clock of the HDMI interface through the differential IO of the FPGA, realize the differential output of the HMDI signal after the data is encoded and parallel-to-differentially converted in the FPGA, and realize the HDMI digital video. The output transmission solution supports up to 1080P@60Hz output.

The differential drive signal of HDMI passes through the IO output of FPGA BANK35, and the ESD protection device is added to the signal interface. In addition, the HPD (hot plug detect) signal is used to detect whether the external HDMI display device is inserted. Figure 9-1 is detailed the HDMI output Interface schematic
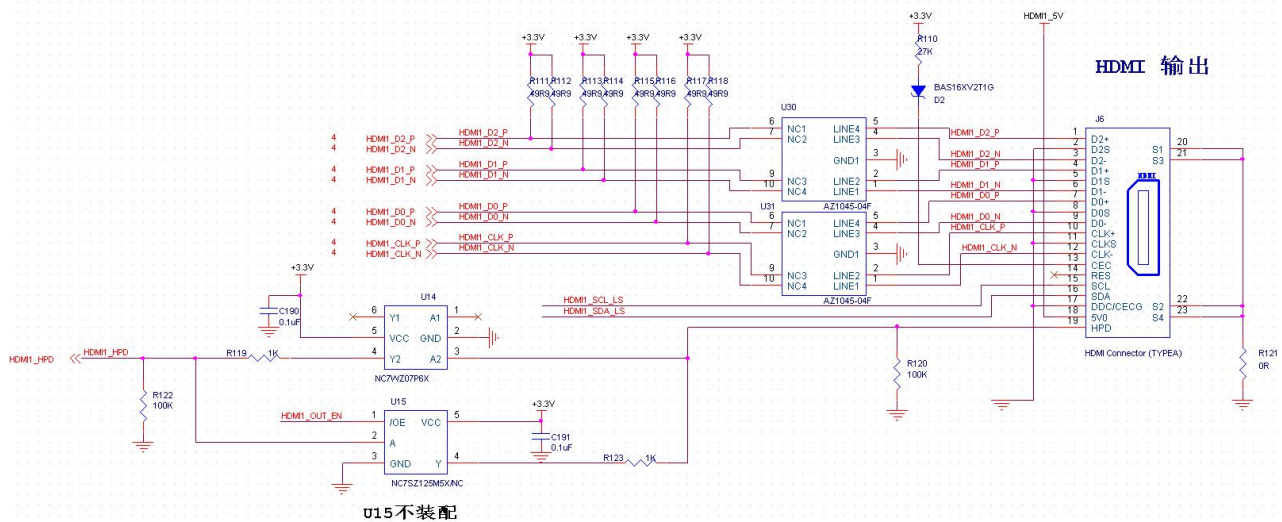
Figure 9-1: HDMI Output Interface Schematic

When the development board is used as an output device for HDMI display, it needs to provide a +5V power supply to the HDMI display device. When the HDMI1_OUT_EN signal is high, it outputs +5V power to the external HDMI device. The power output control circuit is shown in Figure 9-2.
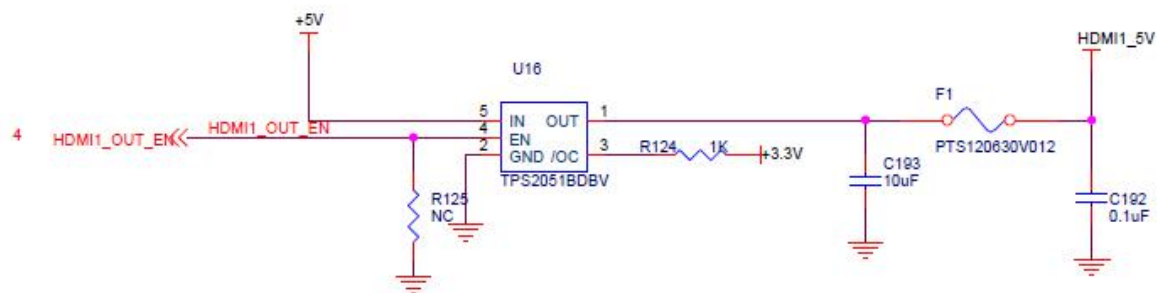

Figure 9-2: HDMI +5V Output Schematic

In addition, the HMDI master device reads the EDID device information of the HDMI display device through the IIC bus. The pin level of the FPGA is 3.3V, but the level of HDMI is +5V. Here, the level conversion chip GTL2002D is required to connect. The conversion circuit of IIC is shown in Figure 9-3
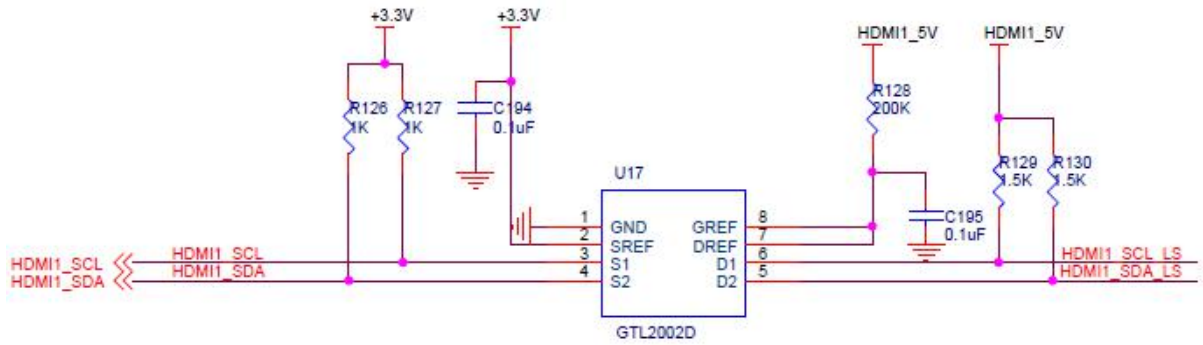
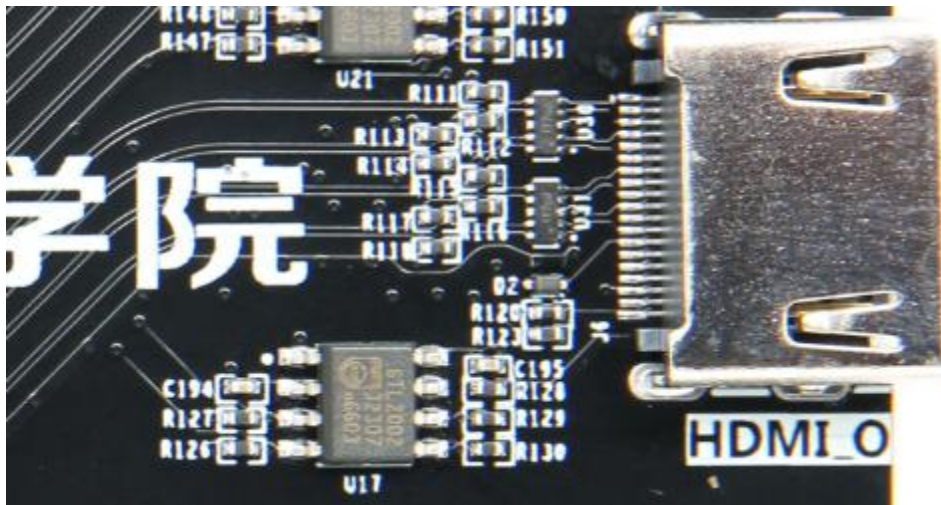Figure 9-3: GTL2002D level conversion circuit

Figure 9-4: HDMI Output Interface on the FPGA Board

HDMI Output Pin Assignment

Pin Name	FPGA Pin
HDMI1_CLK_P	E1
HDMI1_CLK_N	D1
HDMI1_D0_P	G1
HDMI1_D0_N	F1
HDMI1_D1_P	H2
HDMI1_D1_N	G2
HDMI1_D2_P	K1
HDMI1_D2_N	J1
HDMI1_SCL	P4
HDMI1_SDA	N3
HDMI1_OUT_EN	M6
HDMI1_HPD	P5
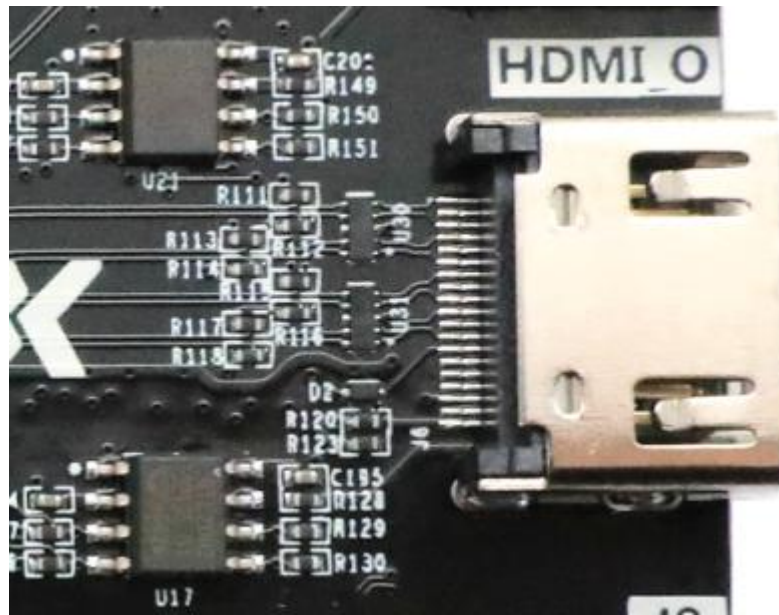
Figure 9-5: HDMI Input Interface on the FPGA Board

Part 10: HDMI1 input interface (also used as an output)

The HDMI2 interface (J7) on the AX7035 development board can be used as both an HDMI input and an HDMI output. By default, the HDMI2 interface is used as an HDMI input. The data differential signal and clock signal of the HDMI interface are directly connected to the differential IO of the FPGA. The HMDI signal is transmitted in parallel and decoded in the FPGA to realize the transmission solution of HDMI digital video input, and the function of up to 720P@60Hz input is supported.

The HDMI differential drive signal is passed through the IO input of the FPGA BANK35, and the ESD protection device is added to the signal interface. In addition, the HPD (hot plug detect) signal is output as the HDMI slave device, and the high level indicates that the HDMI display slave device has been inserted. Figure 10-1 shows the schematic of the HDMI input design.
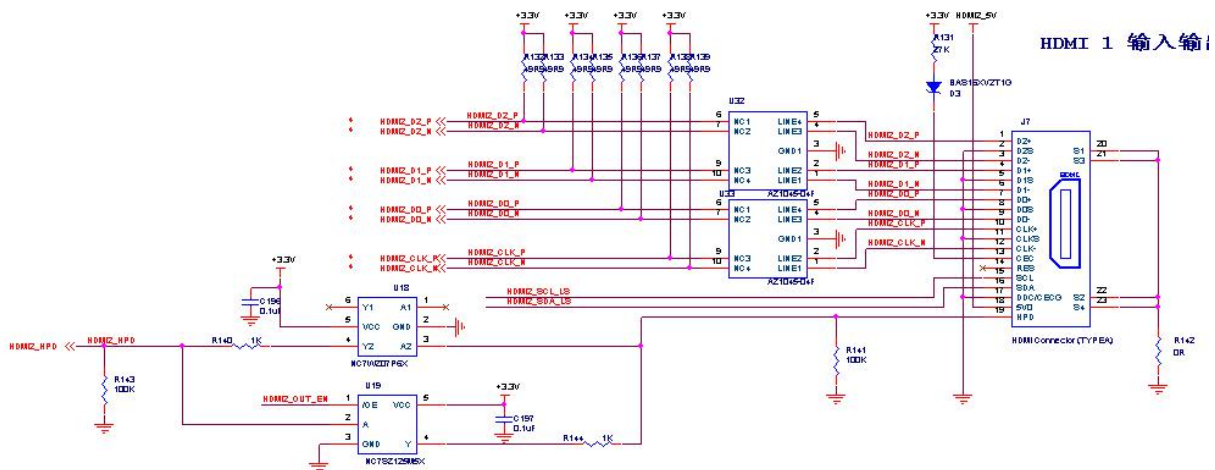
Figure 10-1: HDMI Input Interface Schematic

When the development board is used as an input device for HDMI display, the power supply of HDMI1_5V is provided by the external main device. Here, the signal of HDMI2_OUT_EN needs to be set to low level, and the output of U20 chip is not enabled to be 5V. The HDMI2 power control circuit is shown in Figure 10-2.
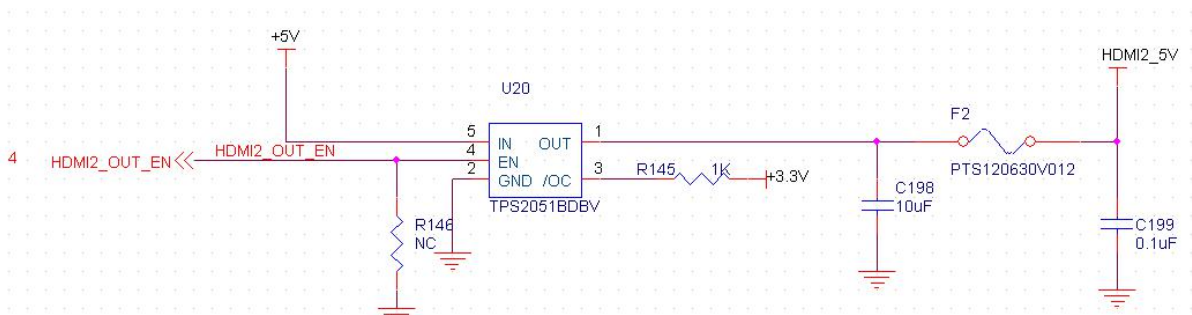

Figure 10-2: HDMI2 power control circuit

In addition, the HMDI master device reads the EDID device information of the HDMI slave device through the IIC bus. The pin level of the FPGA is 3.3V, but the level of HDMI is +5V. Here, the level conversion chip GTL2002D is required to connect. The conversion circuit of IIC is shown in Figure 10-3.
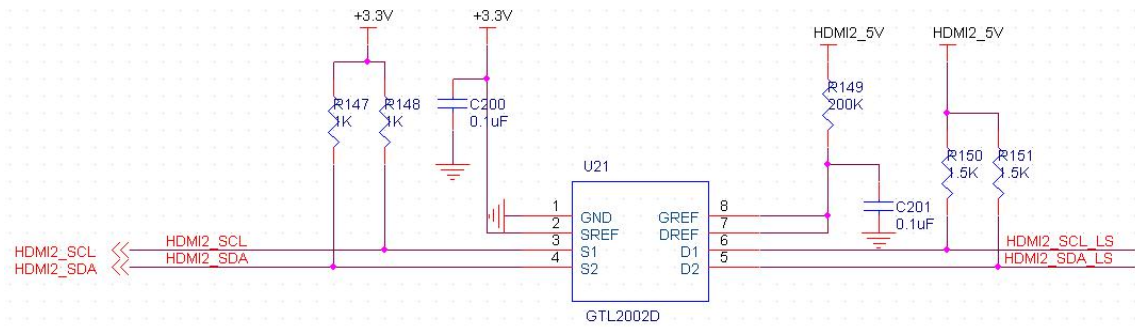
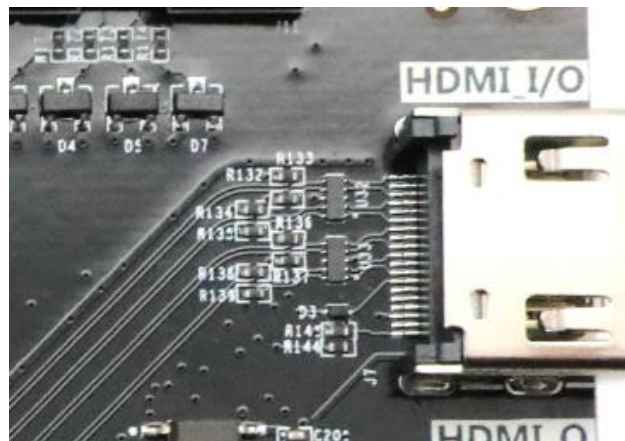Figure 10-3: GTL2002D level conversion circuit

Figure 10-4: HDMI Input Interface on the board

HDMI Input Interface Pin Assignment

Pin Name	FPGA Pin
HDMI2_CLK_P	K4
HDMI2_CLK_N	J4
HDMI2_D0_P	M1
HDMI2_D0_N	L1
HDMI2_D1_P	P2
HDMI2_D1_N	N2
HDMI2_D2_P	R1
HDMI2_D2_N	P1
HDMI2_SCL	N5
HDMI2_SDA	L6
HDMI2_OUT_EN	P6
HDMI2_HPD	M5

Part 11: USB 2.0 Communication Interface

In the AX7035 FPGA development board, usedFT232H single-channel high-speed USB chip of FEDI, to realize USB2.0 data communication between the FPGA development board and the computer. Maximum USB2.0 high-speed communication (480Mb/s) and full-speed communication (12Mb/s). The data interface supports different data communication modes (FIFO, I2C, SPI, JTAG). After power-on, read the external EEPROM configuration. Determining the data communication mode, you can also easily modify the configuration mode through the PC. The function of the interface pins of the USB chip is multiplexed. For details, please refer to the FT232H chip manual.

The data interface signal of the USB chip FT232H is connected to the IO of the FPGA. The data communication of the FT232H is performed by programming of the FPGA. The hardware connection of the FT232H is connected according to the FT245 synchronous FIFO interface. As shown in Figure 11-1.
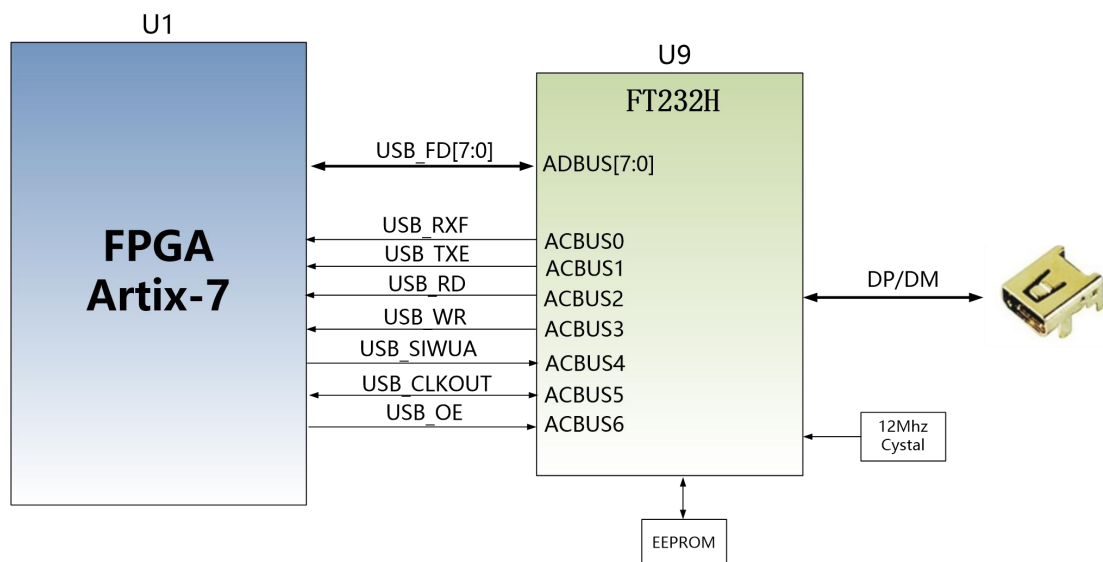

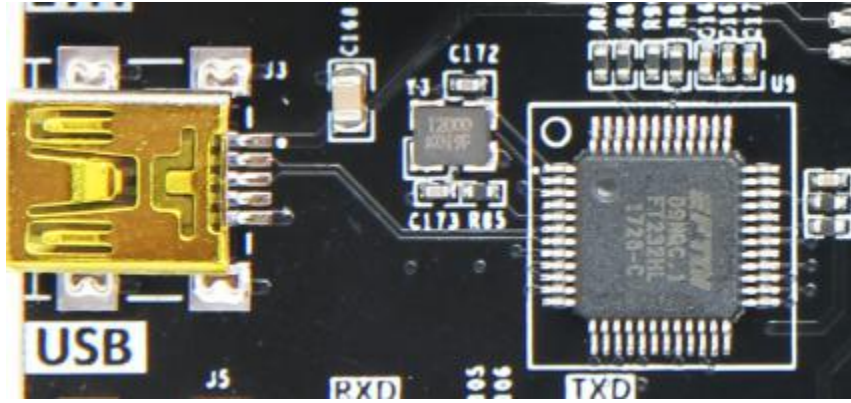Figure 11-1: USB2.0 Interface schematic

Figure 11-2: USB 2.0 part on the FPGA Board

USB 2.0 Pin Assignment

Signal Name	FPGA PIN	Description
USB_FD0	K22	USB2.0 data Bit0
USB_FD1	K21	USB2.0 data Bit1
USB_FD2	J22	USB2.0 data Bit2
USB_FD3	H18	USB2.0 data Bit3
USB_FD4	H22	USB2.0 data Bit4
USB_FD5	J15	USB2.0 data Bit5
USB_FD6	H20	USB2.0 data Bit6
USB_FD7	G20	USB2.0 data Bit7
USB_RXF	H19	Low indicates that the receive FIFO data is readable
USB_TXE	H15	Low indicates that the send FIFO data can be written
USB_RD	L21	Data receive FIFO read signal, low active
USB_WR	G17	Data transmission FIFO write signal, low active
USB_SIWUA	H17	Send immediately/wake up function
USB_CLKOUT	J19	60MHz Clock Output
USB_OE	G18	USB data output enable

Part 12: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted

substantial research and development. In 2000, these companies launched the SD Association (Secure Digital Association), which has a strong lineup and attracted a large number of vendors. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

The SD card is a very common storage device. The SD card that we have extended supports SD and SPI modes. The SD card used is a Micro SD card. The schematic diagram is shown in Figure 12-1.
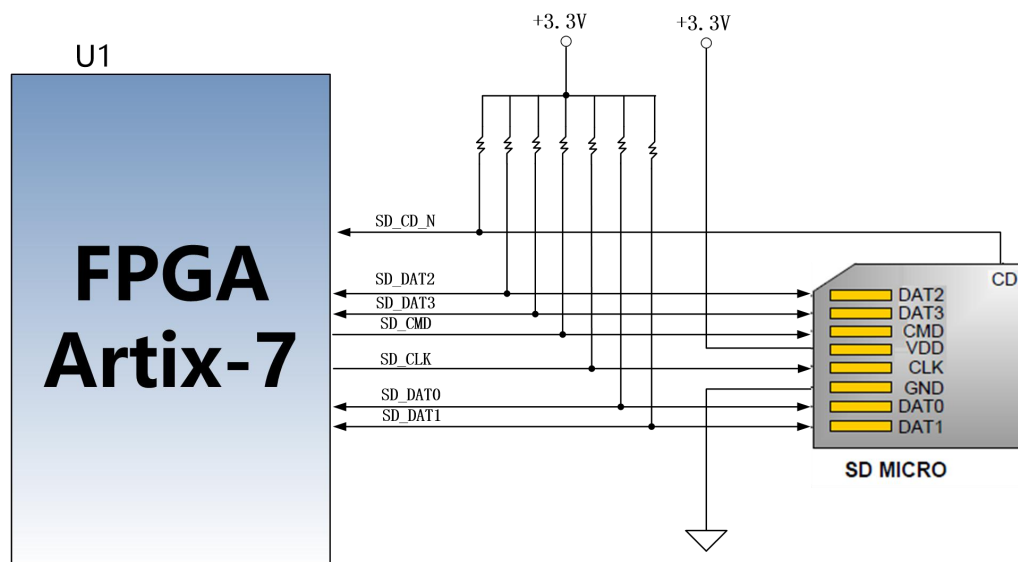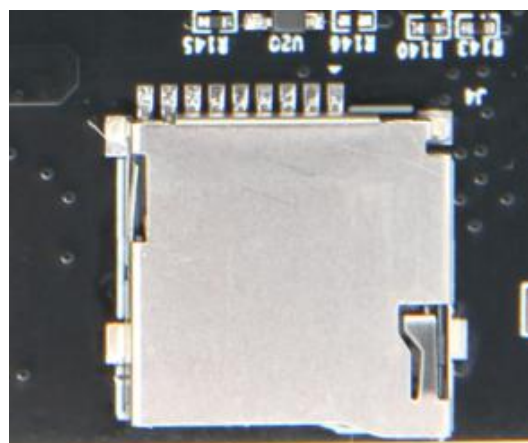

Figure 12-1: SD Card Slot Schematic

Figure 12-2: SD Card Slot on the FPGA Board

SD Card Slot pin assignment:

SPI Mode	
Signal Name	**FPGA Pin**
SD_CLK	N15
SD_CMD	P15
SD_DAT0	P16
SD_DAT1	R17
SD_DAT2	N14
SD_DAT3	N13
SD_CD_N	R16

Part 13: USB to Serial Port

The AX7035 FPGA development board includes the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC for serial data communication with a USB cable. The schematic diagram of the USB Uart circuit design is shown in Figure 13-1:
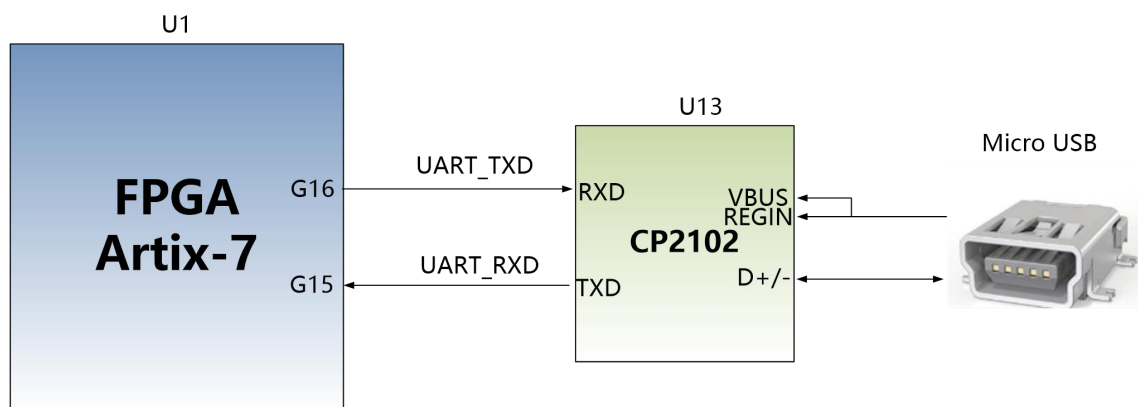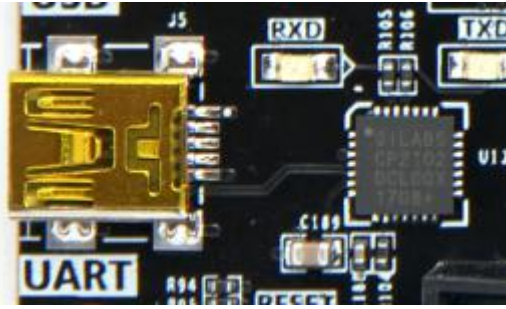

Figure 13-1: USB to serial port schematic

Figure 13-2: USB to serial port on the FPGA Board

Two LED indicators (LED5 and LED6) are set for the serial port signal, and the silkscreen on the PCB is TX and RX, indicating that the serial port has data transmission or reception, as shown in the following Figure 13-3
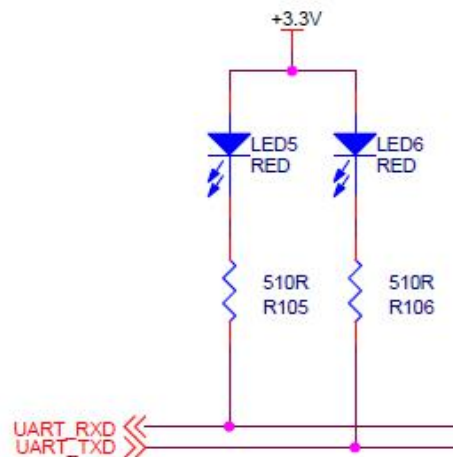

Figure 13-3: Serial Port communication LED Indicators Schematic

USB to serial port pin assignment:

Signal Name	FPGA PIN
UART_RXD	G15
UART_TXD	G16

Part 14: EEPROM 24LC04

The AX7035 development board contains an EEPROM, model 24LC04, and has a capacity of 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn the

communication method of the IIC bus. The EEPROM I2C signal is connected to the IO port of the FPGA. Figure 14-1 below shows the design of the EEPROM.
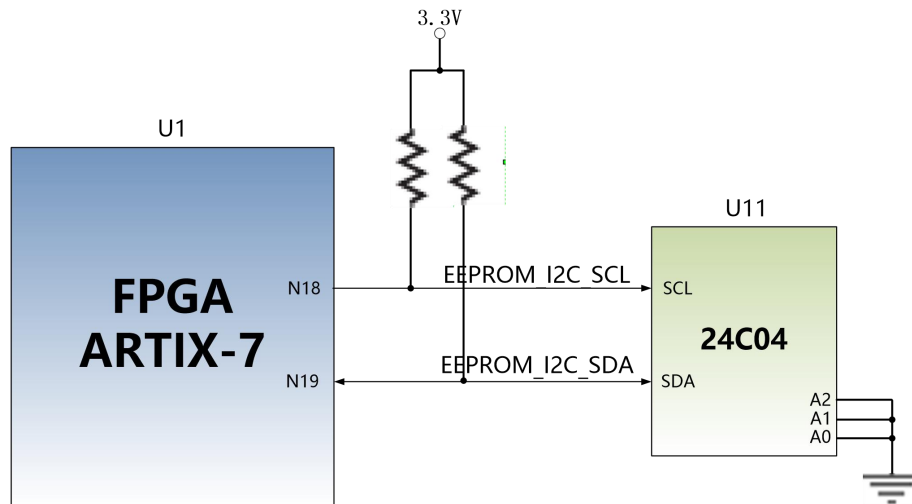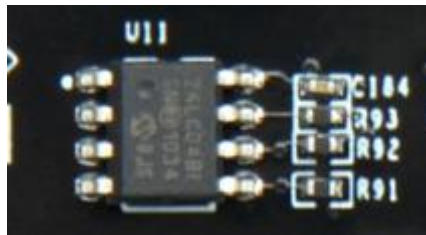

Figure 14-1: EEPROM Schematic

Figure 14-2: EEPROM on the FPGA Board

EEPROM Pin Assignment

Pin Name	FPGA Pin
EEPROM_I2C_SCL	N18
EEPROM_I2C_SDA	N19

Part 15: Digital Tube

The AX7035 development board has 6 digital tubes for displaying digital information. The digital tube we use is a 6-in-one eight-segment digital tube, and the segment structure of a digital tube is shown in Figure 15-1.
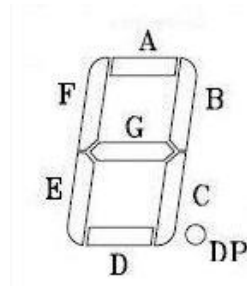
Figure 15-1: Segment structure of digital tube

We use a common anode digital tube. When the corresponding pin of a certain field is low, the corresponding field is lit. When the corresponding pin of a certain field is high, the corresponding field is not lit. The six-in-one digital tube is a dynamic display. Due to the persistence of human vision and the afterglow effect of the LED, although the digital tubes are not lit at the same time, as long as the scanning speed is fast enough, the impression is a group and stable display data, no flickering.

The same segments of the six-in-one digital tube are connected together, a total of 8 pins, and then add 6 control signal pins, a total of 14 pins, as shown in Figure 15-2, where DIG[0. .7] is the corresponding digital tube A, B, C, D, E, F, G, H (ie point DP); SEL [0..5] is the six control pins of the six digital tube, is also low level active, When the control pin is low, the corresponding digital tube has a power supply voltage, so that the digital tube can be lit, otherwise the corresponding digital tube cannot be lit regardless of the change of the segment of the digital tube.
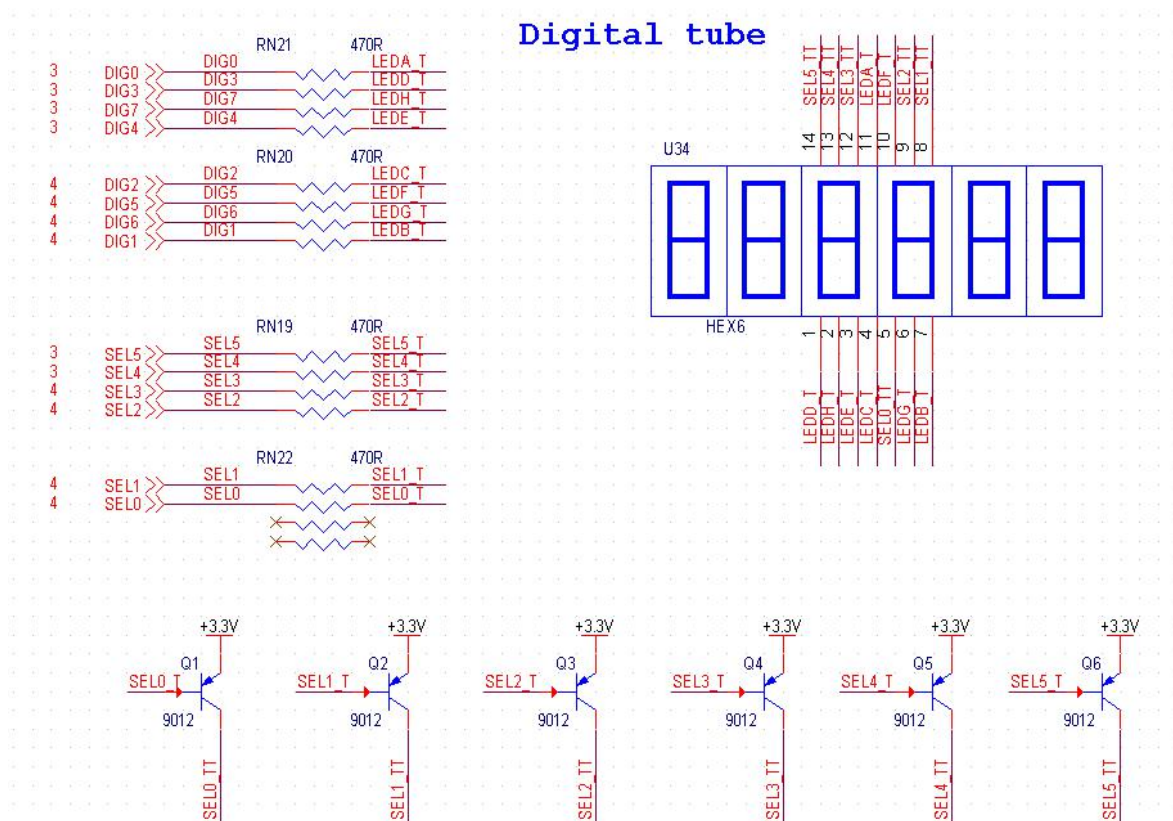
Figure 15-2: Digital Tube Schematic

Figure 15-3: Digital Tube on the FPGA Board

Digital tube pin assignment

Pin Name	FPGA Pin	Description
DIG0	J5	Corresponding segment A
DIG1	M3	Corresponding segment B
DIG2	J6	Corresponding segment C
DIG3	H5	Corresponding segment D
DIG4	G4	Corresponding segment E

DIG5	K6	Corresponding segment F
DIG6	K3	Corresponding segment G
DIG7	H4	Corresponding point DP
SEL0	M2	The first digital tube from the right
SEL1	N4	The second digital tube from the right
SEL2	L5	The third digital tube from the right
SEL3	L4	The fourth digital tube from the right
SEL4	M16	The fifth digital tube from the right
SEL5	M17	The sixth digital tube from the right

Part 16: Temperature Sensor

A high-precision, low-power, digital temperature sensor chip is mounted on the AX7035 FPGA development board, and the model is LM75 of ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees. The sensor and FPGA are directly connected to the I2C digital interface. The FPGA reads the temperature near the current FPGA development board through the I2C interface. Figure 16-1 below shows the design of the LM75 sensor chip.
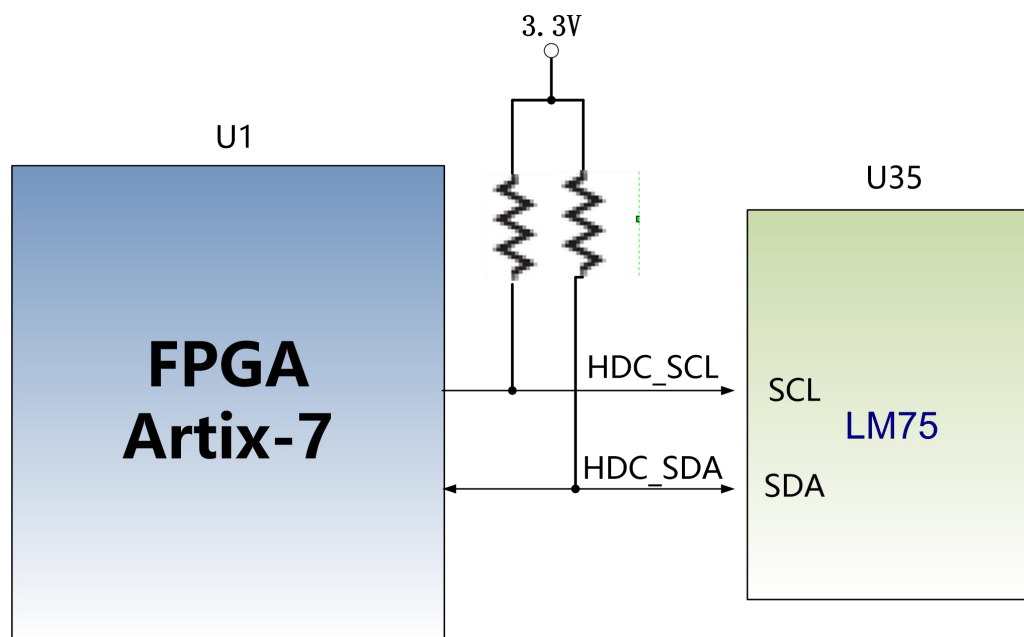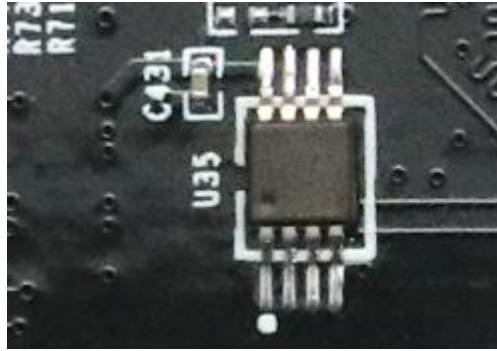
Figure 16-1: LM75 Sensor Schematic

Figure 16-2: LM75 Sensor on the FPGA Board

LM75 Sensor Pin Assignment

Pin Name	FPGA Pin
LM75_SCL	M22
LM75_SDA	N22

Part 17: Expansion Header

The AX7035 FPGA development board is reserved with two 0.1inch spacing standard 40-pin expansion headers J9 and J10. Which are used to connect the ALINX modules or the external circuit designed by the user.The signal of the expansion port J9 is connected to the BANK16 of the FPGA, so the LDO chip (U27) can be replaced to meet different level's standard. The IOs of J10are connected to the BANK14 of the FPGA, so the IOs of J10 level standard is fixed at 3.3V.

The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel3.3 V power supply,3-channle ground and 34 IOs. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The circuit of the expansion port (J9) is shown in Figure 17-1
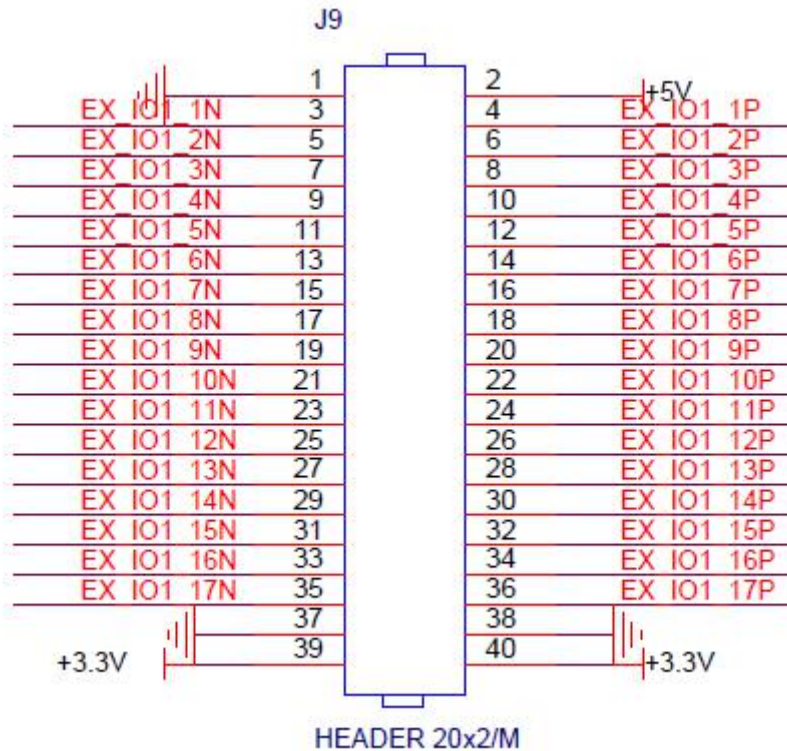
Figure 17-1: Expansion header J9 schematic

Figure 17-2: Expansion header J9on the FPGABoard

J9 Expansion Header Pin Assignment

J9 Pin Number	FPGA Pin	J9 Pin Number	FPGA Pin
1	GND	2	+5V
3	D16	4	E16
5	F14	6	F13
7	E14	8	E13
9	D15	10	D14
11	B13	12	C13
13	A14	14	A13
15	C15	16	C14
17	A16	18	A15
19	B16	20	B15

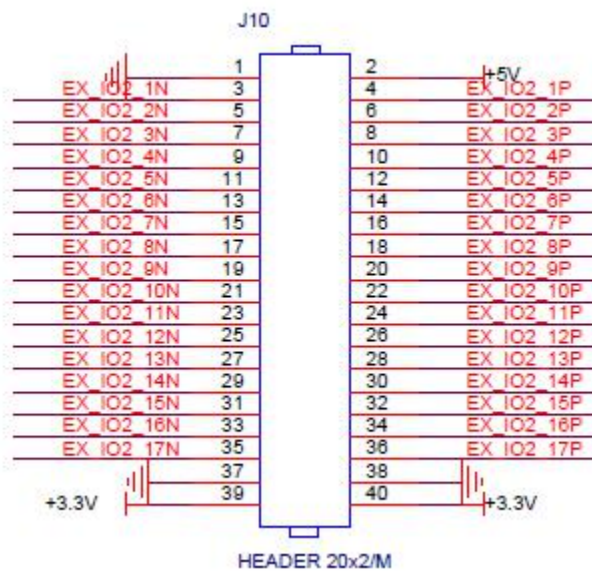| 21	B18	22	B17
23	A19	24	A18
25	C19	26	C18
27	A20	28	B20
29	C17	30	D17
31	D19	32	E19
33	E18	34	F18
35	E17	36	F16
37	GND	38	GND
39	+3.3V	40	+3.3V

Figure 17-3: Expansion header J10 schematic

Figure 17-4: Expansion header J10on the FPGA Board

J10 Expansion Header Pin Assignment

J10 Pin Number	FPGA Pin	J10 Pin Number	FPGA Pin
1	GND	2	+5V
3	P17	4	N17

5	R19	6	P19
7	T18	8	R18
9	U21	10	T21
11	V22	12	U22
13	V20	14	U20
15	W22	16	W21
17	Y22	18	Y21
19	AA21	20	AA20
21	AB22	22	AB21
23	AB20	24	AA19
25	W20	26	W19
27	AB18	28	AA18
29	V19	30	V18
31	W17	32	V17
33	U18	34	U17
35	R14	36	P14
37	GND	38	GND
39	+3.3V	40	+3.3V

Part 18: FPC Expansion Ports

A 15-pin FPC expansion port J8 is reserved on the AX7035 FPGA development board, and an external module (such as a MIPI camera) is connected through a 15-line 1mm pitch FPC cable. The expansion port has 3 pairs of differential signals, 4 control signals, 1-channel 3.3V power supply (output), and 4-channel ground. The circuit of the FPC expansion port (J8) is as shown in Figure 18-1.
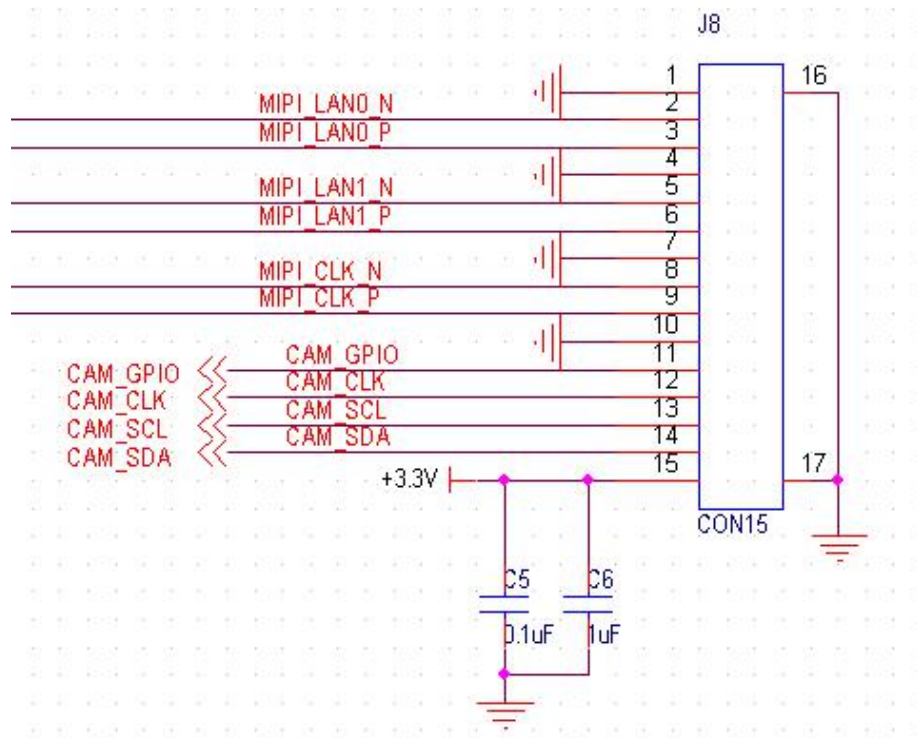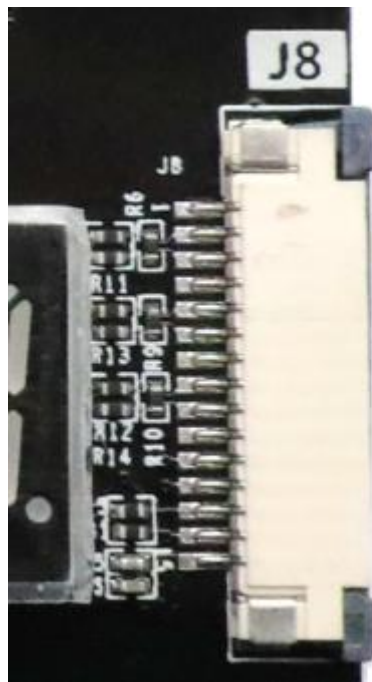
Figure18-1: FPC Expansion Ports Schematic

Figure18-2: FPC Expansion Ports on the FPGA Board

FPC Expansion Ports Pin Assignment

Pin Number	Signal network name	FPGA Pin
1	GND	-
2	MIPI_LAN0_N	D2

3	MIPI_LAN0_P	E2
4	GND	-
5	MIPI_LAN1_N	E3
6	MIPI_LAN1_P	F3
7	GND	-
8	MIPI_CLK_N	G3
9	MIPI_ CLK _P	H3
10	GND	-
11	CAM_GPIO	H13
12	CAM_CLK	H14
13	CAM_SCL	J14
14	CAM_SDA	G13
15	+3.3V	-

Part 19: JTAG Interface

A JTAG interface is reserved JTAG interface one the AX7035 FPGA development board for downloading FPGA programs or firmware to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA to avoid damage of the FPGA chip.
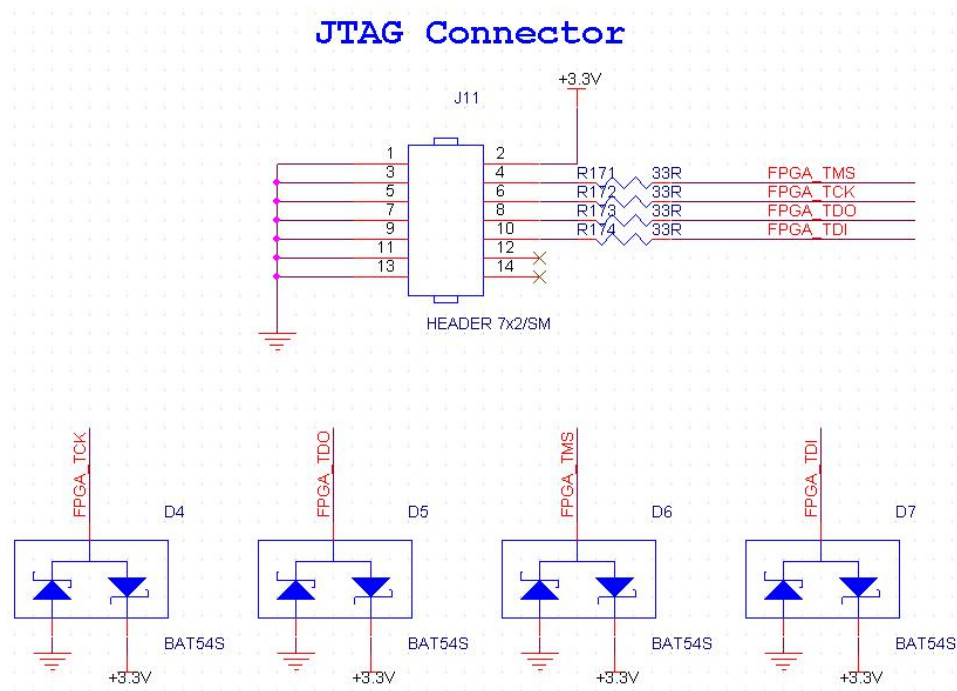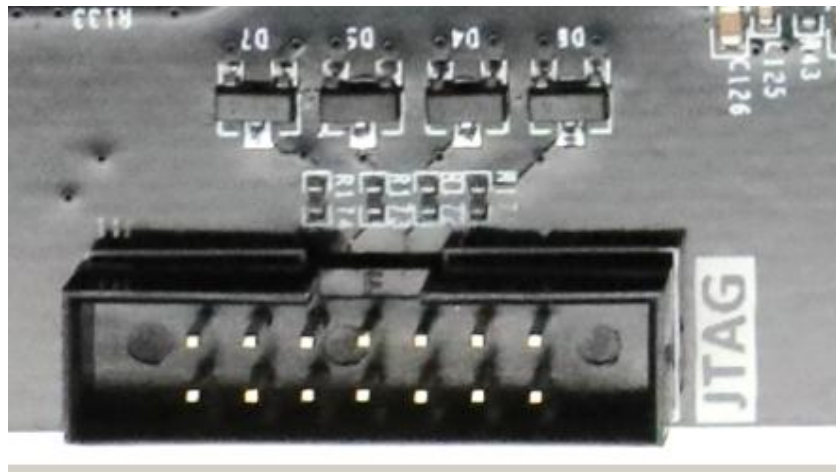
Figure 19-1: JTAG Interface Schematic

Figure 19-2: JTAG Interface on the FPGA board

Be careful not to hot swap when JTAG cable is plugged and unplugged.

Part 20: User Keys

The AX7035 FPGA development board contains one reset key and four user keys KEY1~KEY4. All keys are connected to the normal IO of the FPGA.

The key is active low. When the key is pressed, the IO input voltage of the FPGA is low. When no key is pressed, The IO input voltage of the FPGA is high. The circuit of the key part is shown in Figure 20-1.
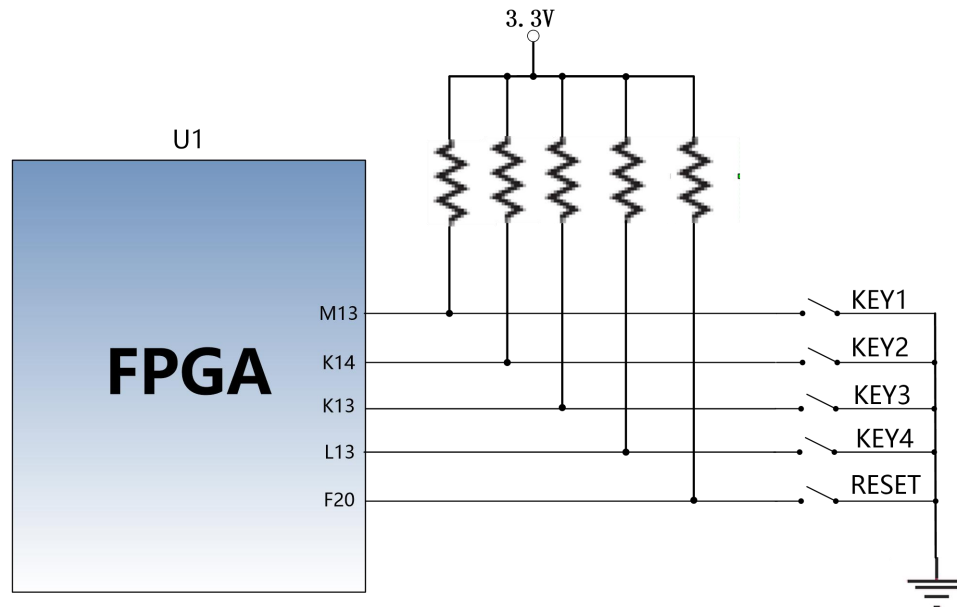

Figure 20-1: Key Schematic

Figure 20-2: Reset Key and User Keys on the FPGA Board

Keys Pin Assignment

Net Name	FPGA PIN
KEY1	M13
KEY2	K14
KEY3	K13
KEY4	L13
RESET	F20

Part 21: LED Light

There are seven red LEDs on the AX7035 FPGA development board, one of which is the power indicator (PWR), two are USB Uart data receiving and sending indicators, four are users LED lights (LED1~LED4). When the AX7035 FPGA board is powered on, the power indicator will light up; User LED1~LE4D are connected to the normal IO of the FPGA. When the IO voltage connected to the user LED is configured low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be extinguished. The schematic diagram of the user LEDs hardware connection is shown in Figure 21-1.
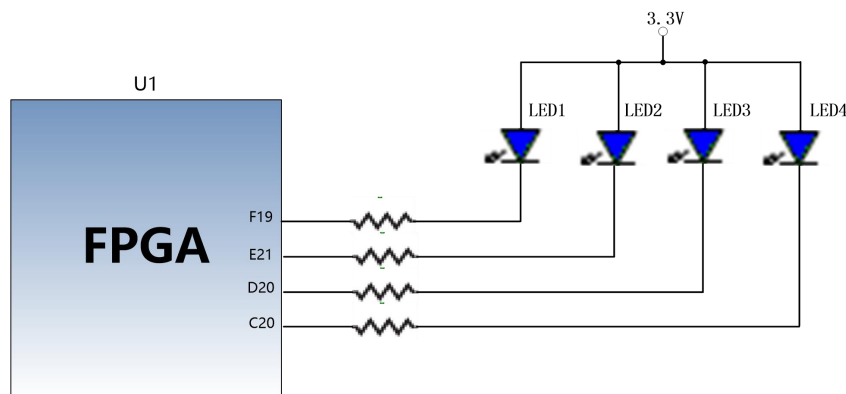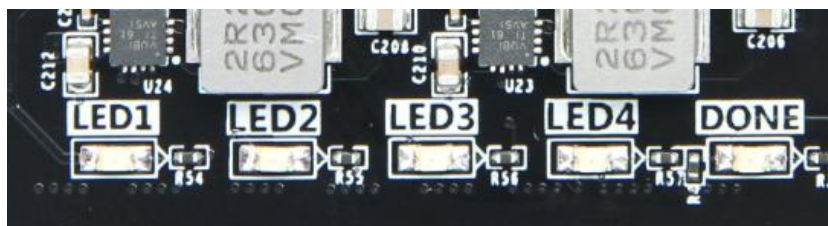

Figure 21-1: The User LEDs Schematic

Figure 21-2: The User LEDs on the FPGA Board

Pin assignment of user LED lights

Signal Name	FPGA PIN
LED1	F19
LED2	E21
LED3	D20
LED4	C20