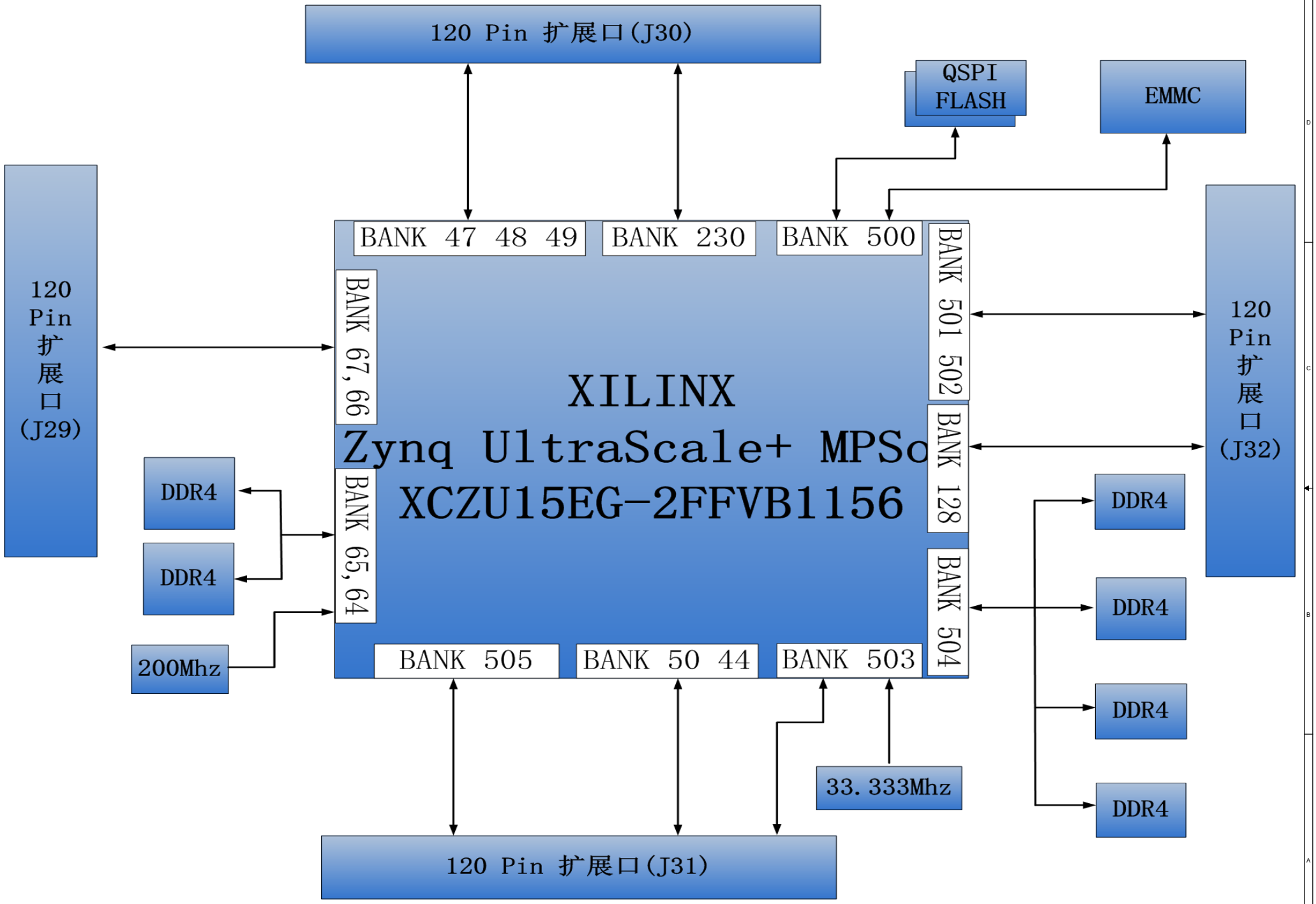

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Title: PAGE01 Block diagram

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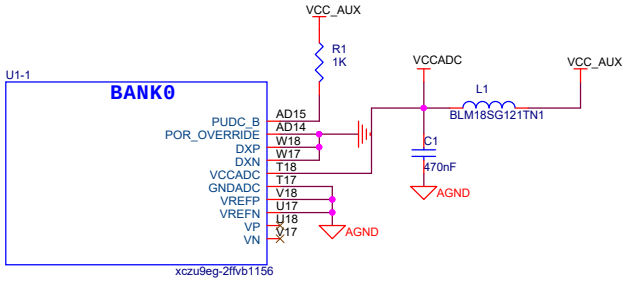
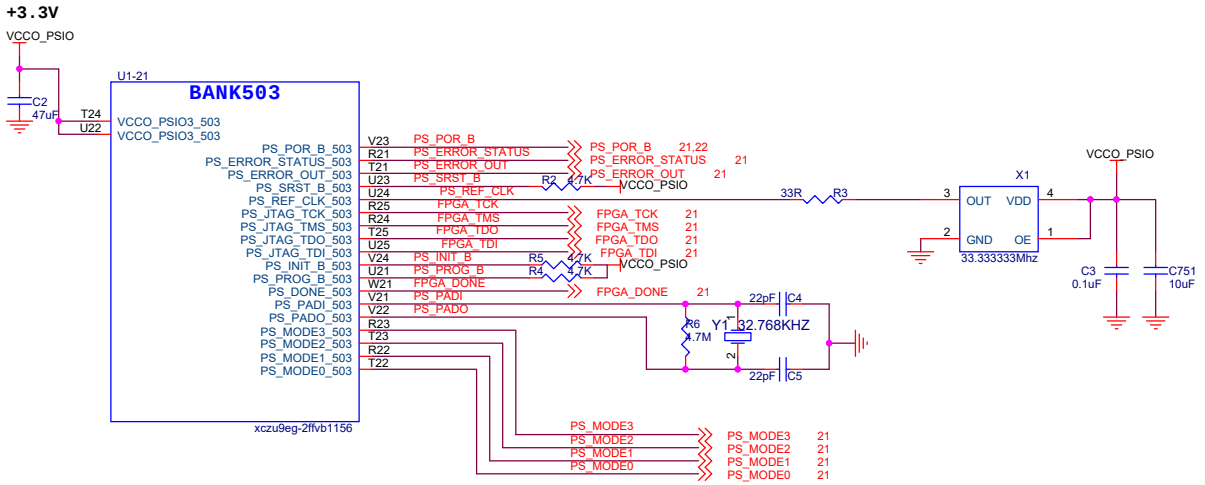


MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1110	SD1 LS(3.0)	SD 3.0



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Title: Page02 Z7 Bank0 & BANK503

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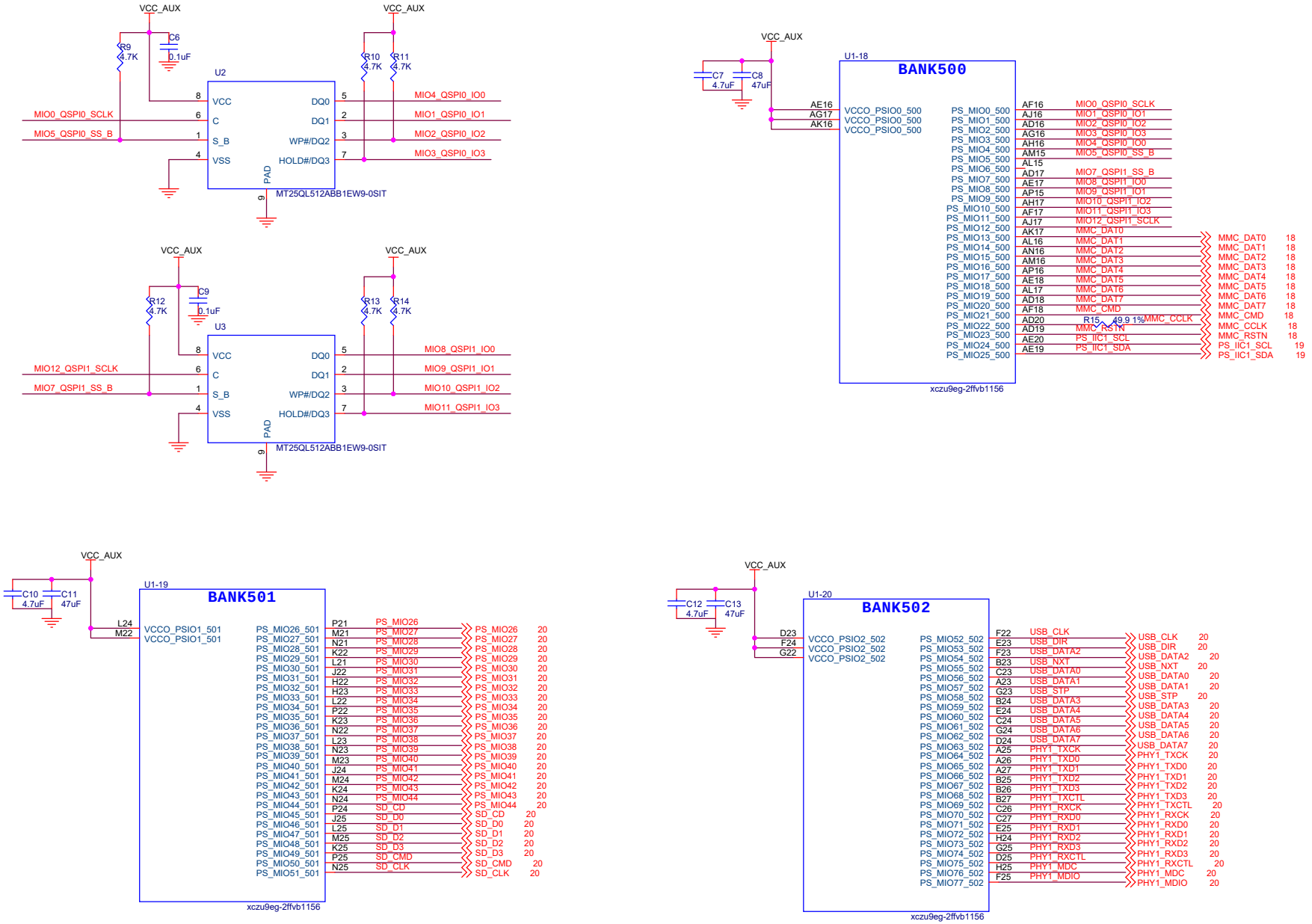

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Title	PAGE03 Z7 MIO-Config
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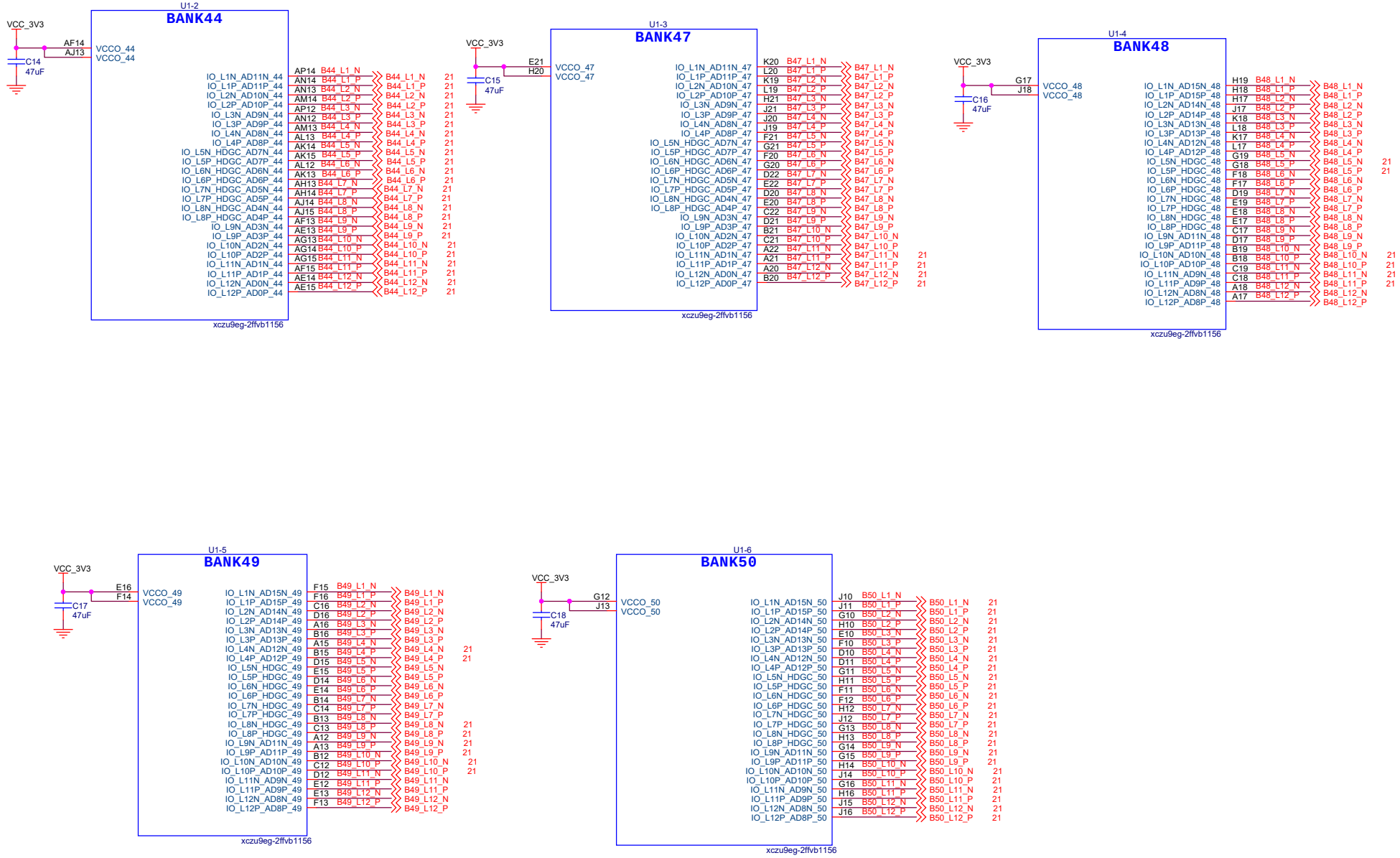

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Title	PAGE04 Z7 Bank44_47_48_49_50
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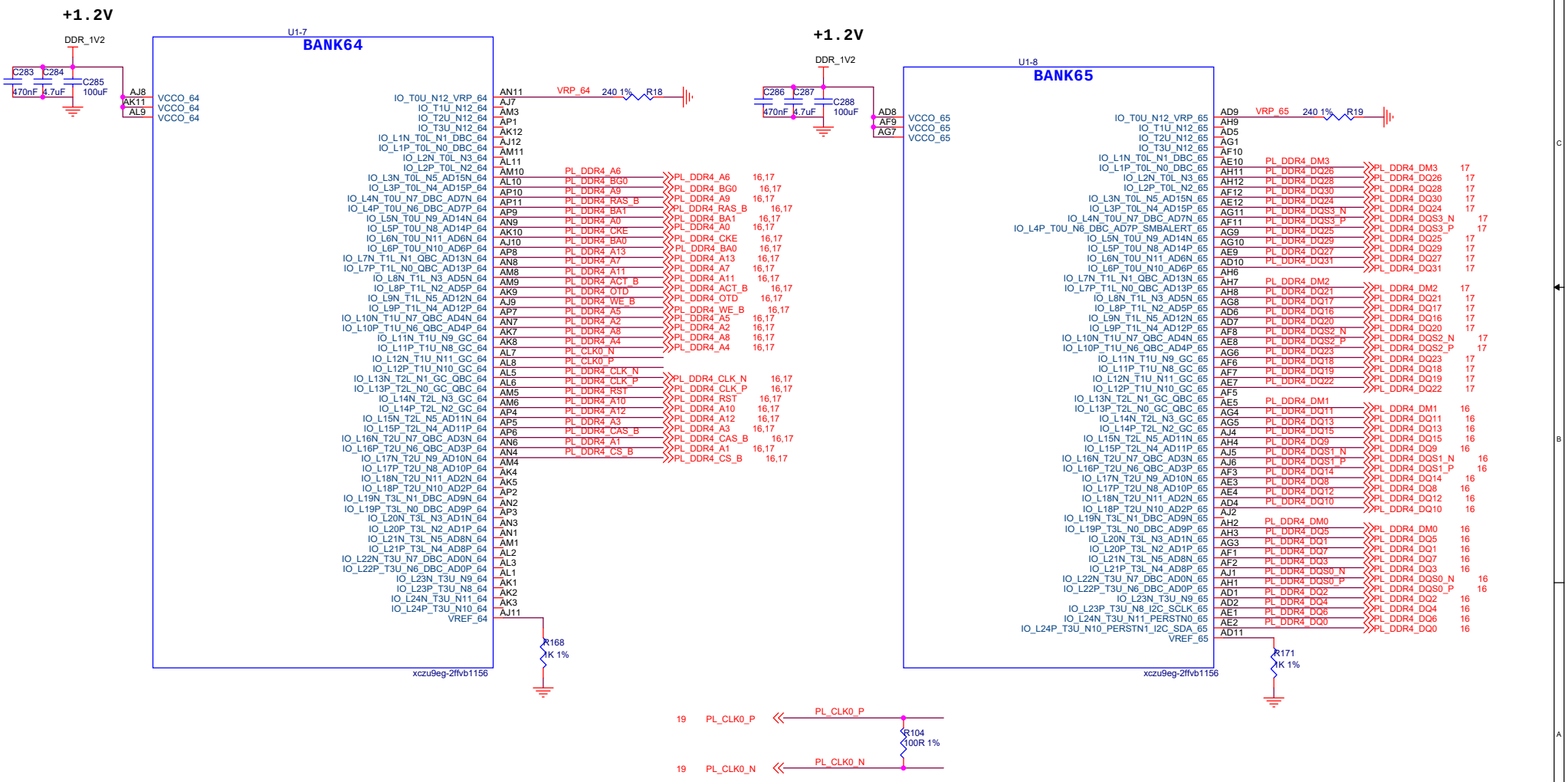

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Title	PAGE05 Z7 Bank64_65	
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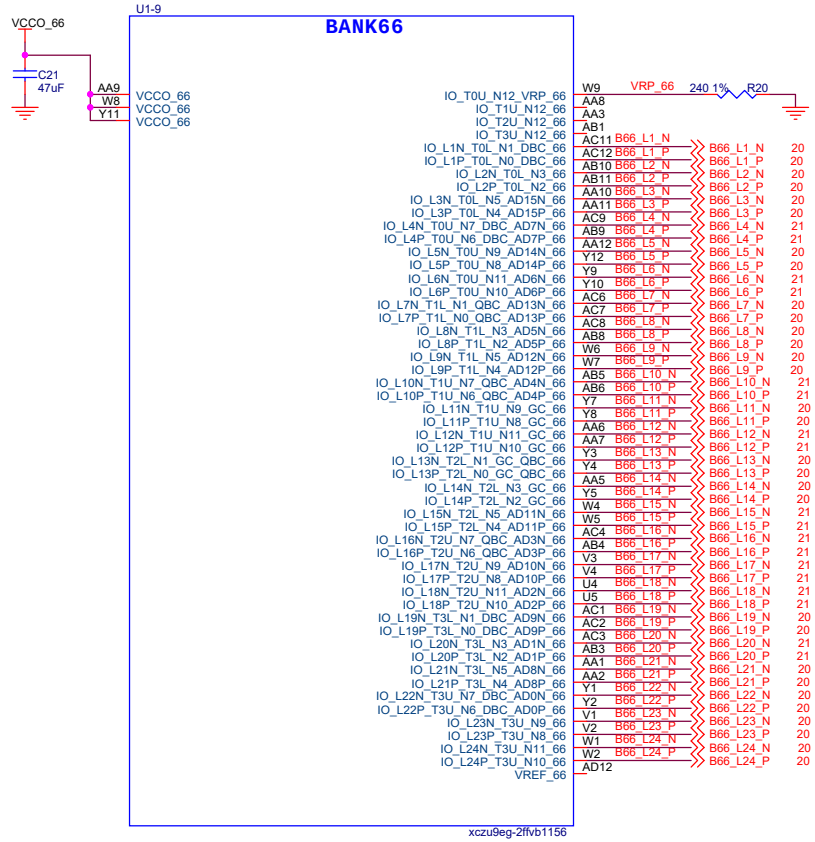
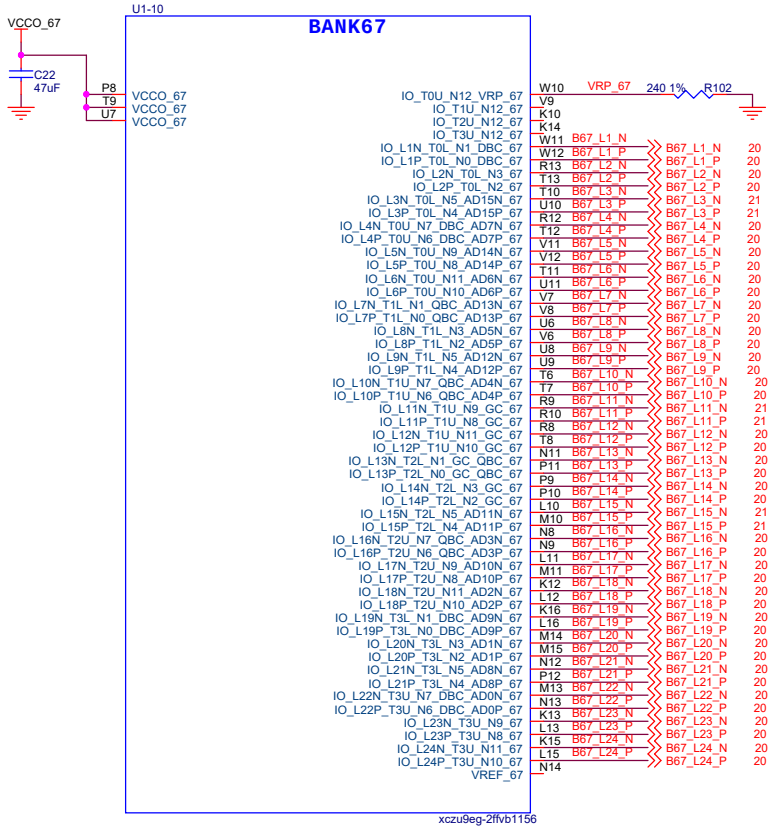
1.2V~1.8V



1.2V~1.8V



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Title	PAGE06 Z7 Bank66_67
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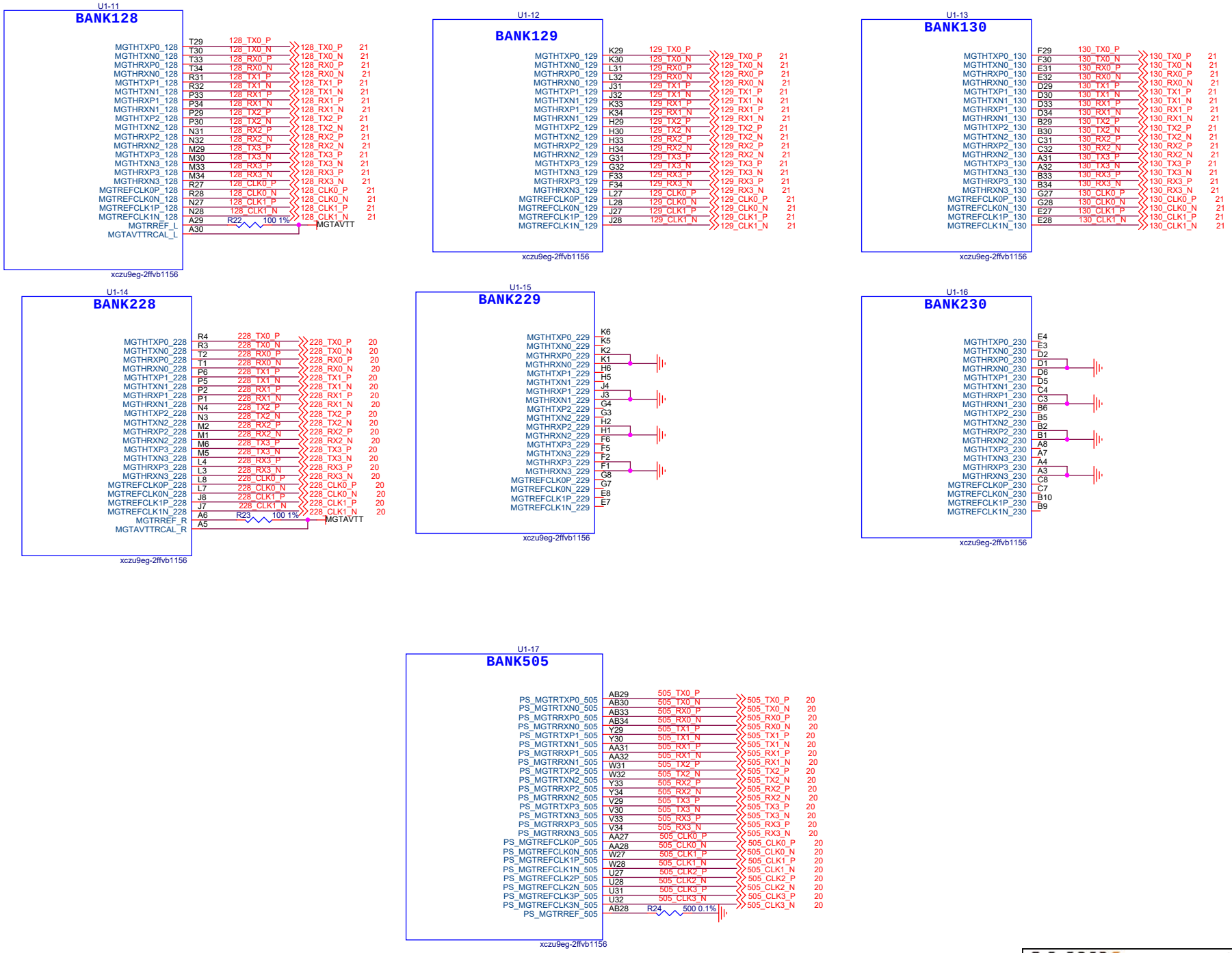

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Title: PAGE07 Z7 Bank505

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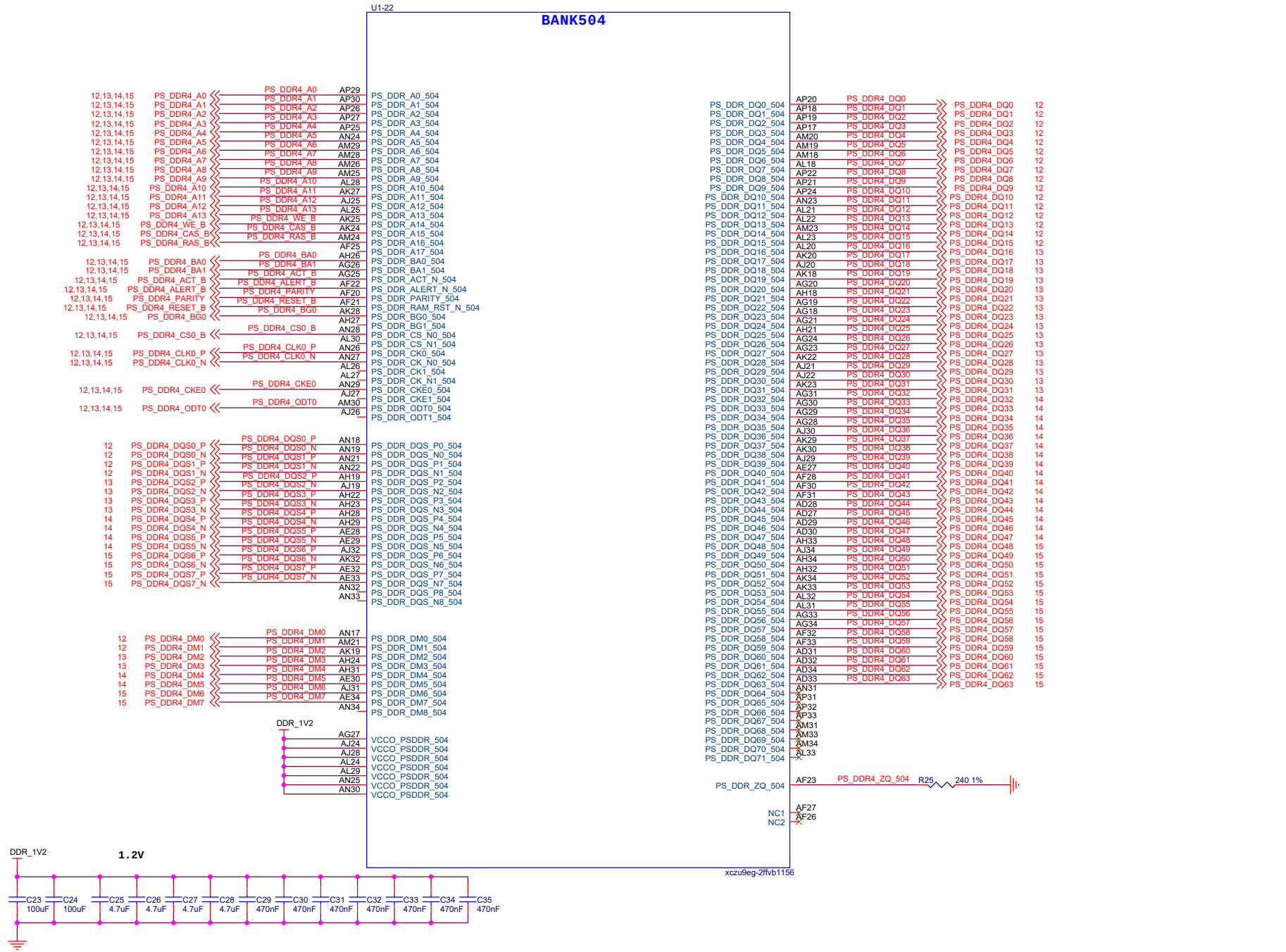

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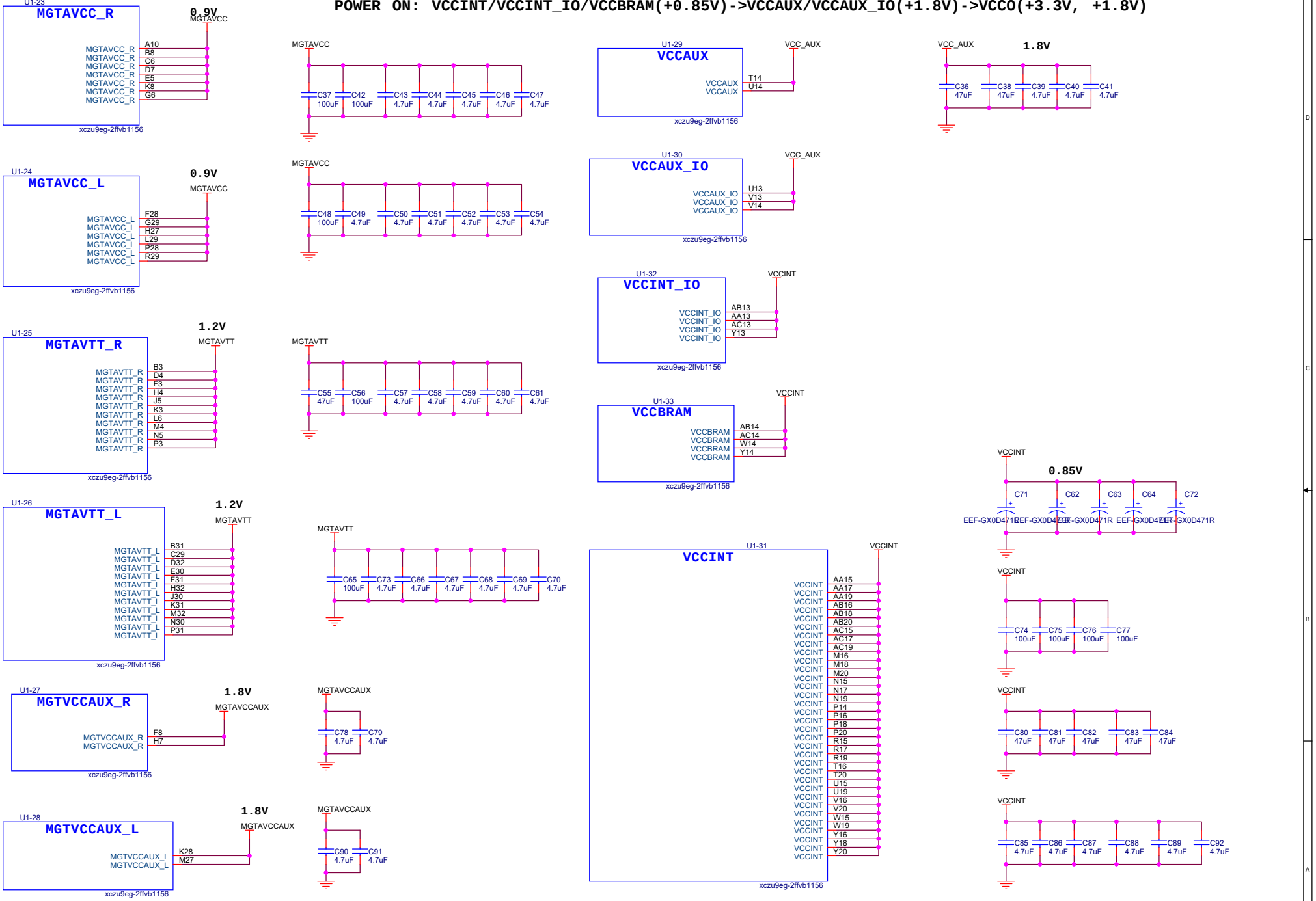
POWER ON: VCCINT/VCCINT_IO/VCCBRAM(+0.85V)->VCCAUX/VCCAUX_IO(+1.8V)->VCCO(+3.3V, +1.8V)



If all of the Quads in a power supply group are not used, the associated power pins can be left unconnected or tied to GND

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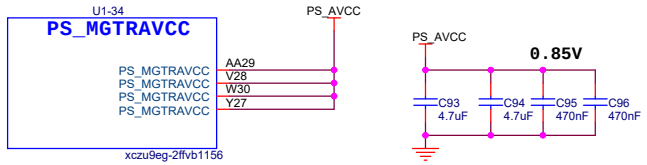
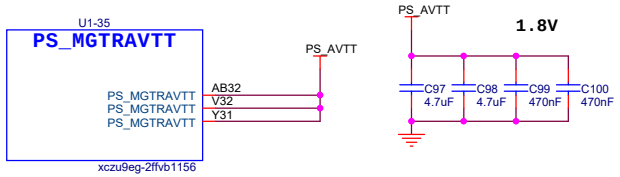
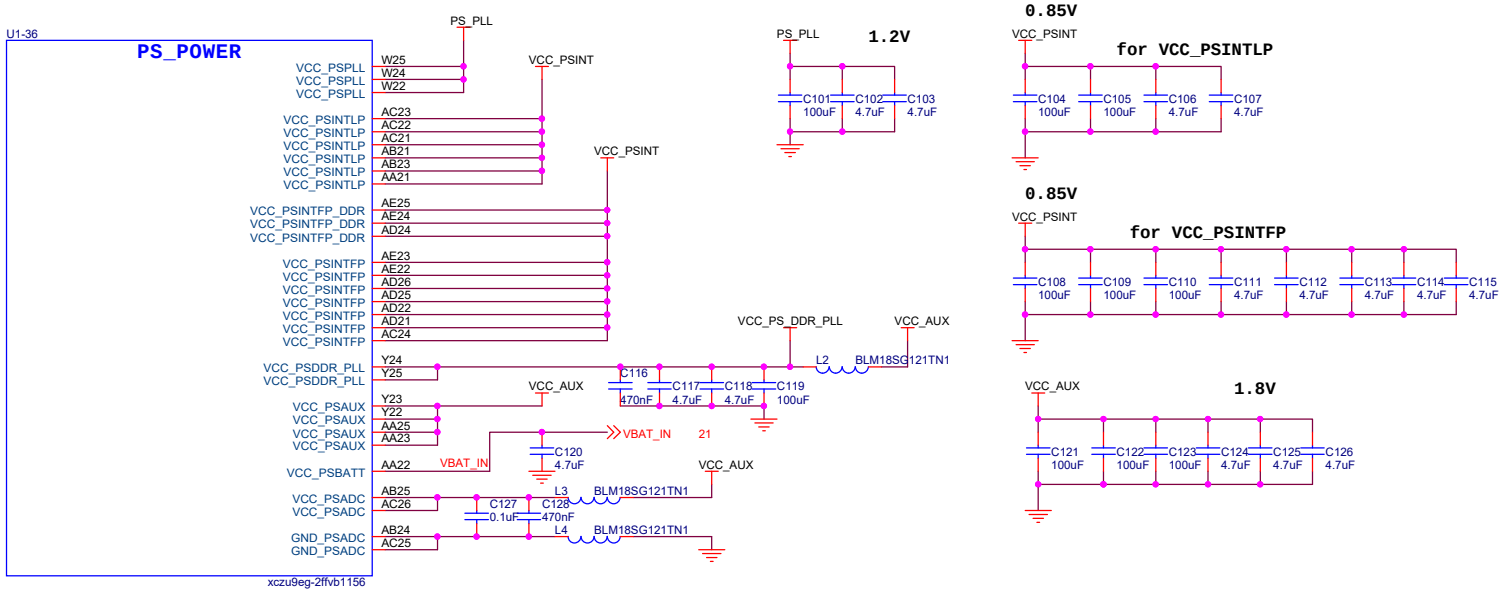
POWER ON: VCC_PSINTFP/VCC_PSINTFP_DDR(+0.85V)->VPS_MGTRAVCC(+0.9V),VCC_PSDDR_PLL(+1.8V)->VPS_MGTRAVTT(+1.8V),VCCO_PSDDR()

POWER ON: VCC_PSINTLP(+0.85V)->VCC_PSAUX(+1.8V),VCC_PSADC(+1.8V),VCC_PSPLL(+1.2V)->VCCO_PSIO(+1.8V)







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Title: PAGE10 Z7 PS Power2

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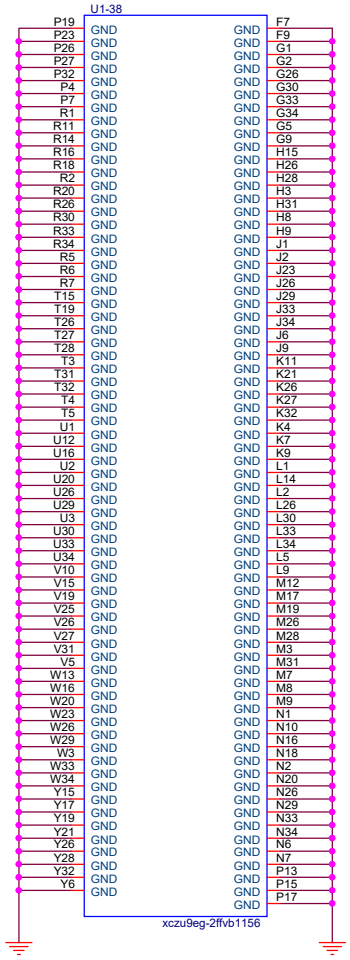

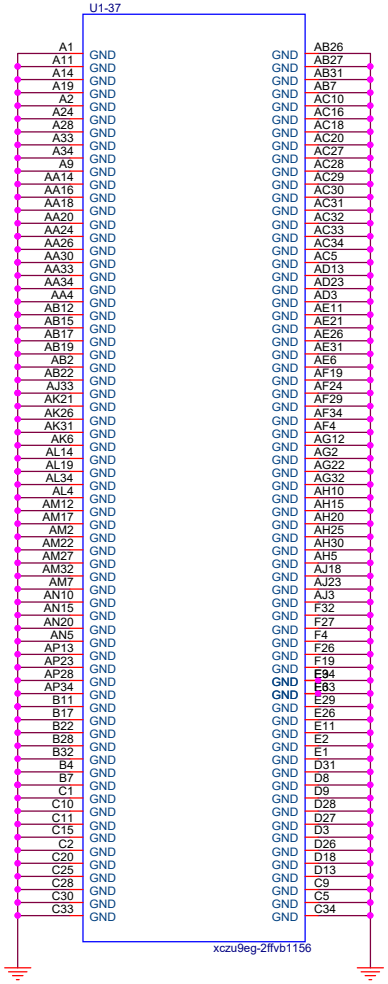

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Title: PAGE11 Z7 GND

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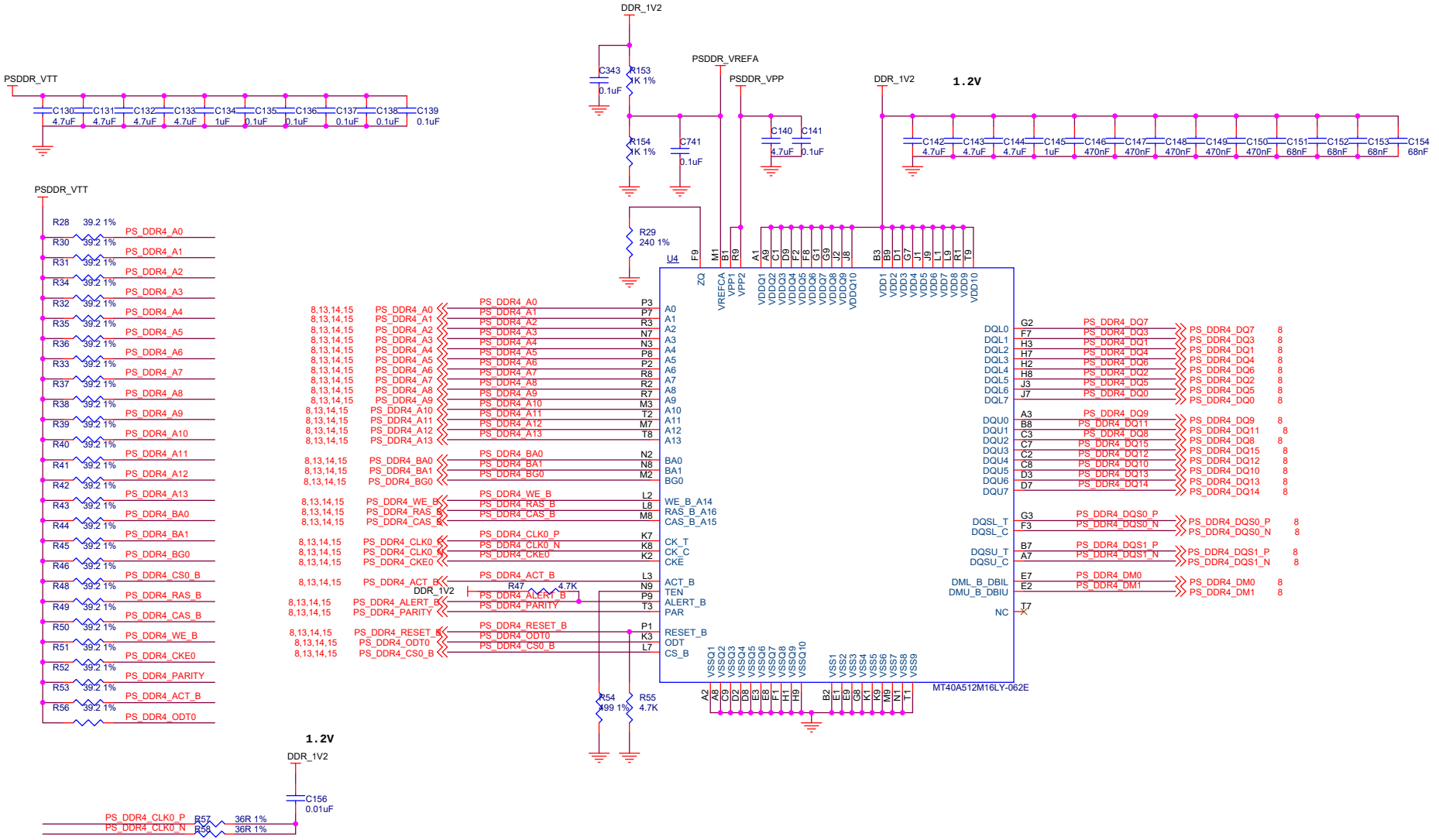

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ALINX	Http://www.alinx.com
Title	PAGE12 PS_DDR4_1
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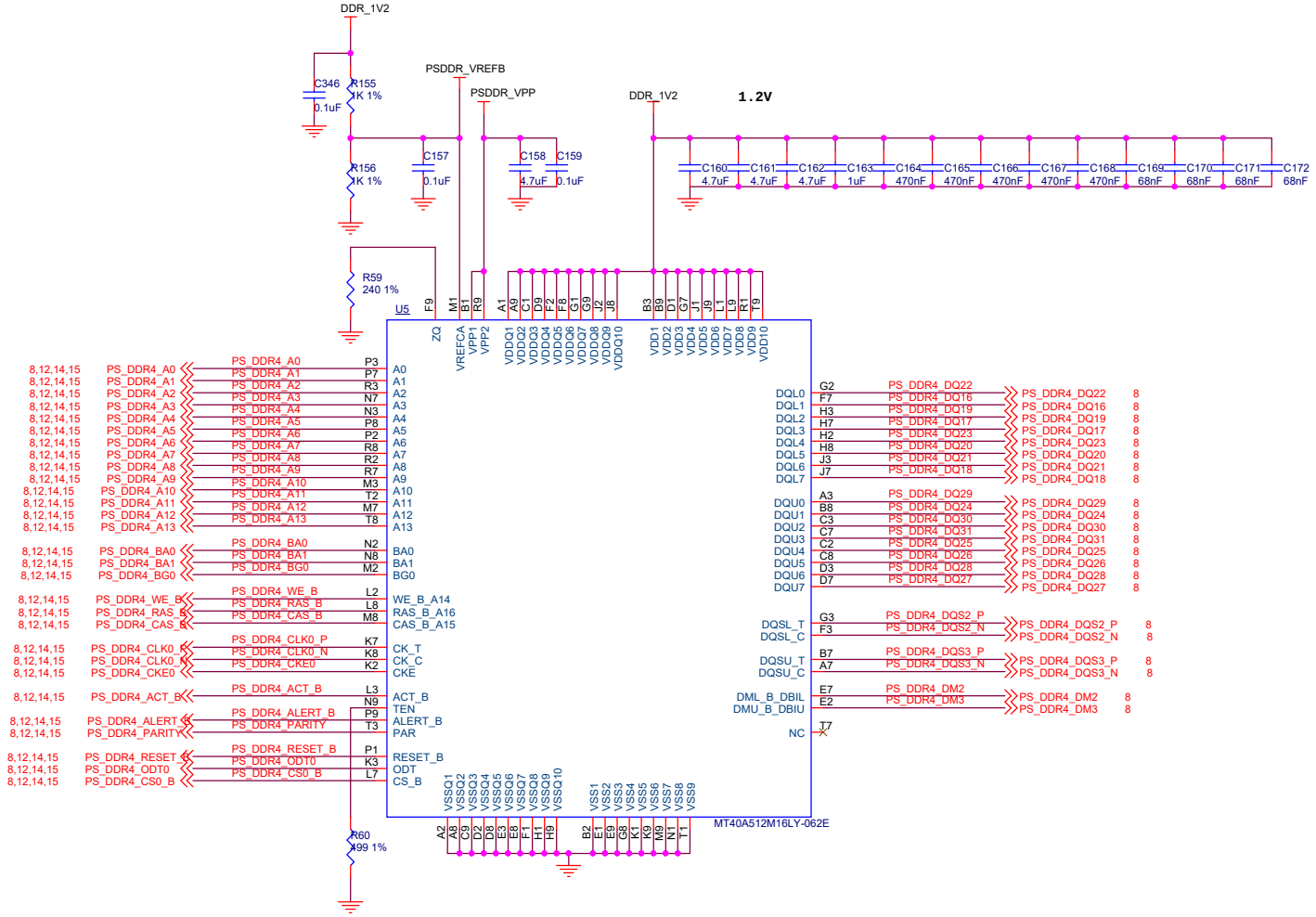

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Http://www.alinx.com	
Title	PAGE13 PS_DDR4_2
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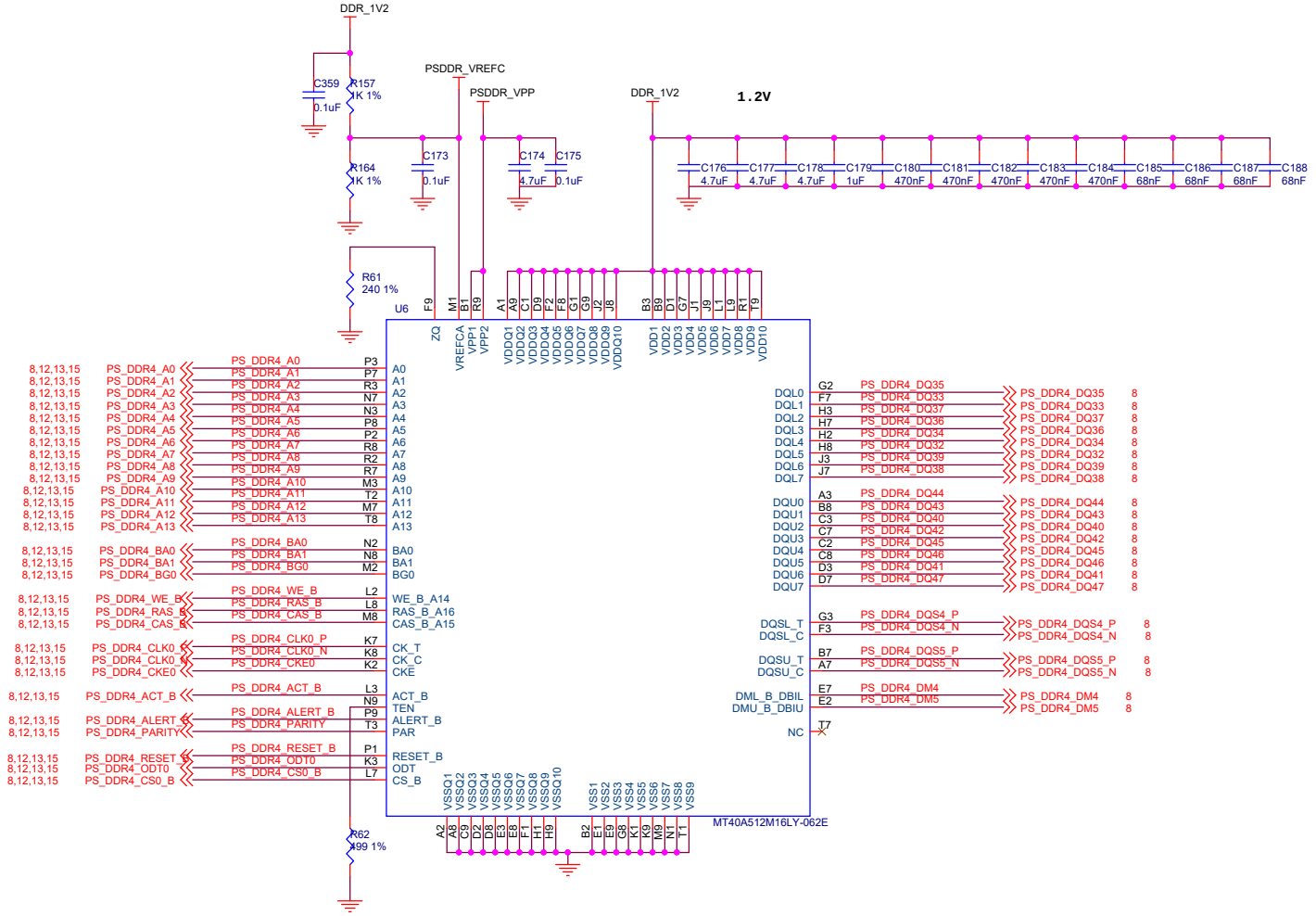

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Title: PAGE14 PS_DDR4_3

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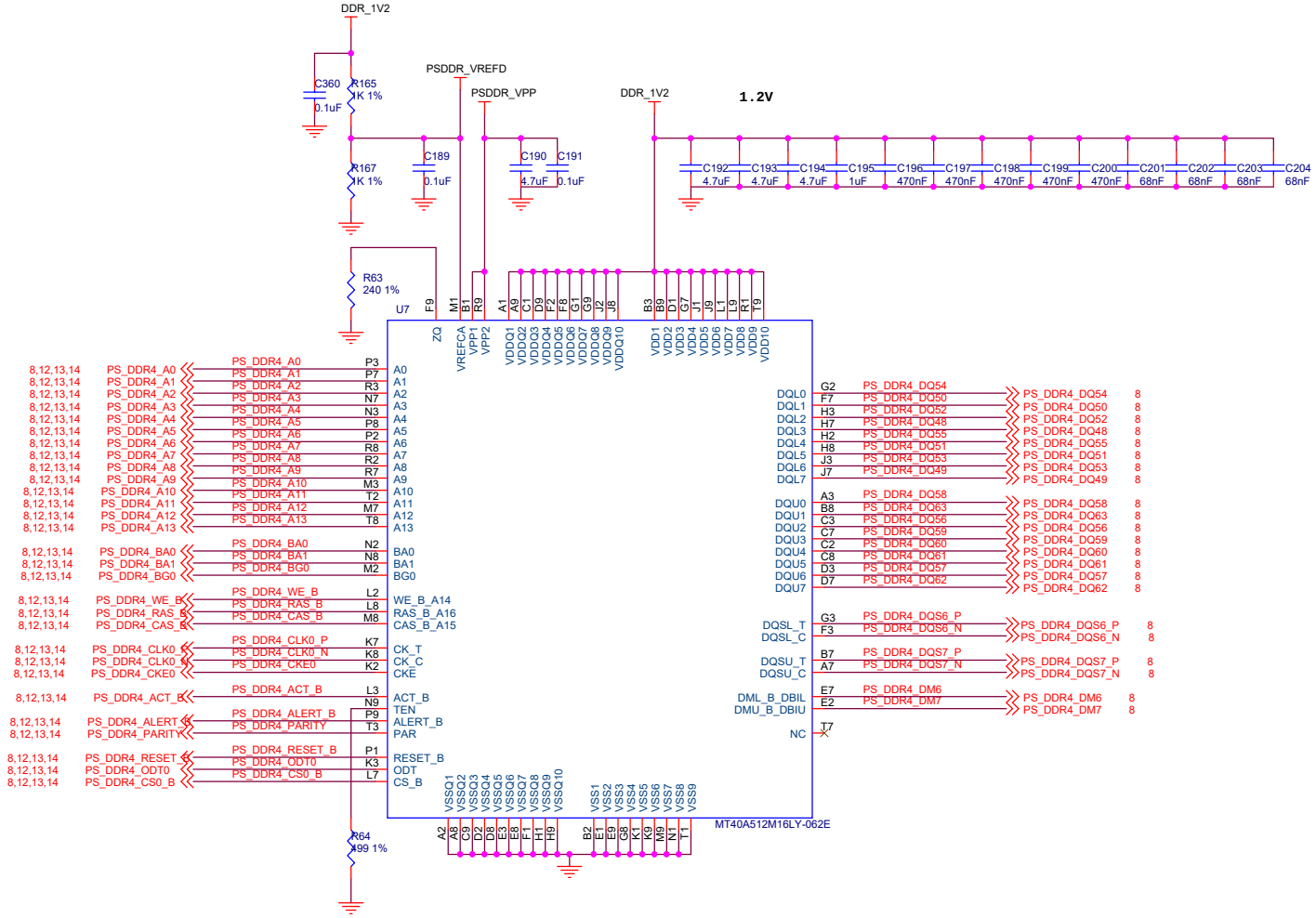

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Title	PAGE15 PS_DDR4_4
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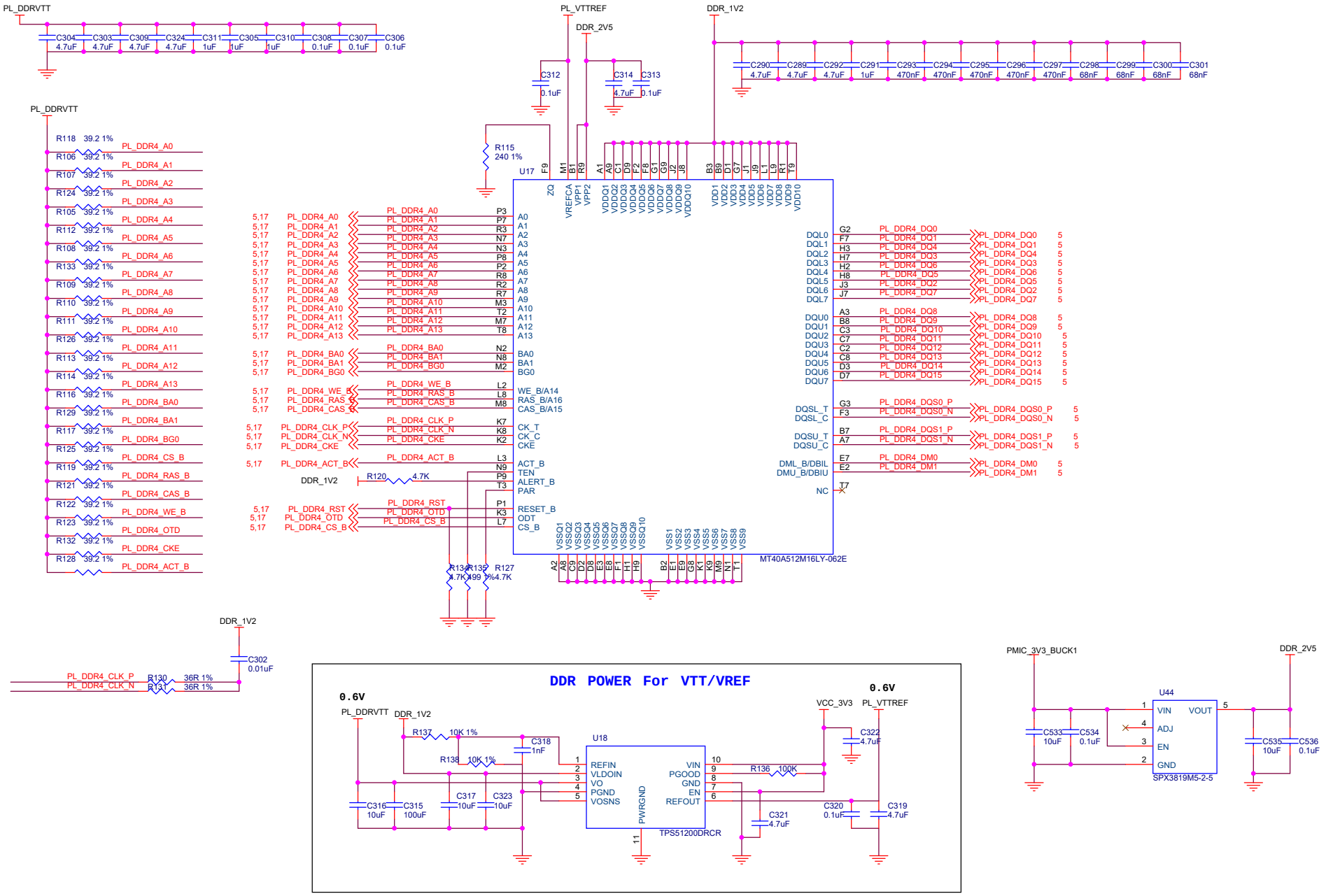

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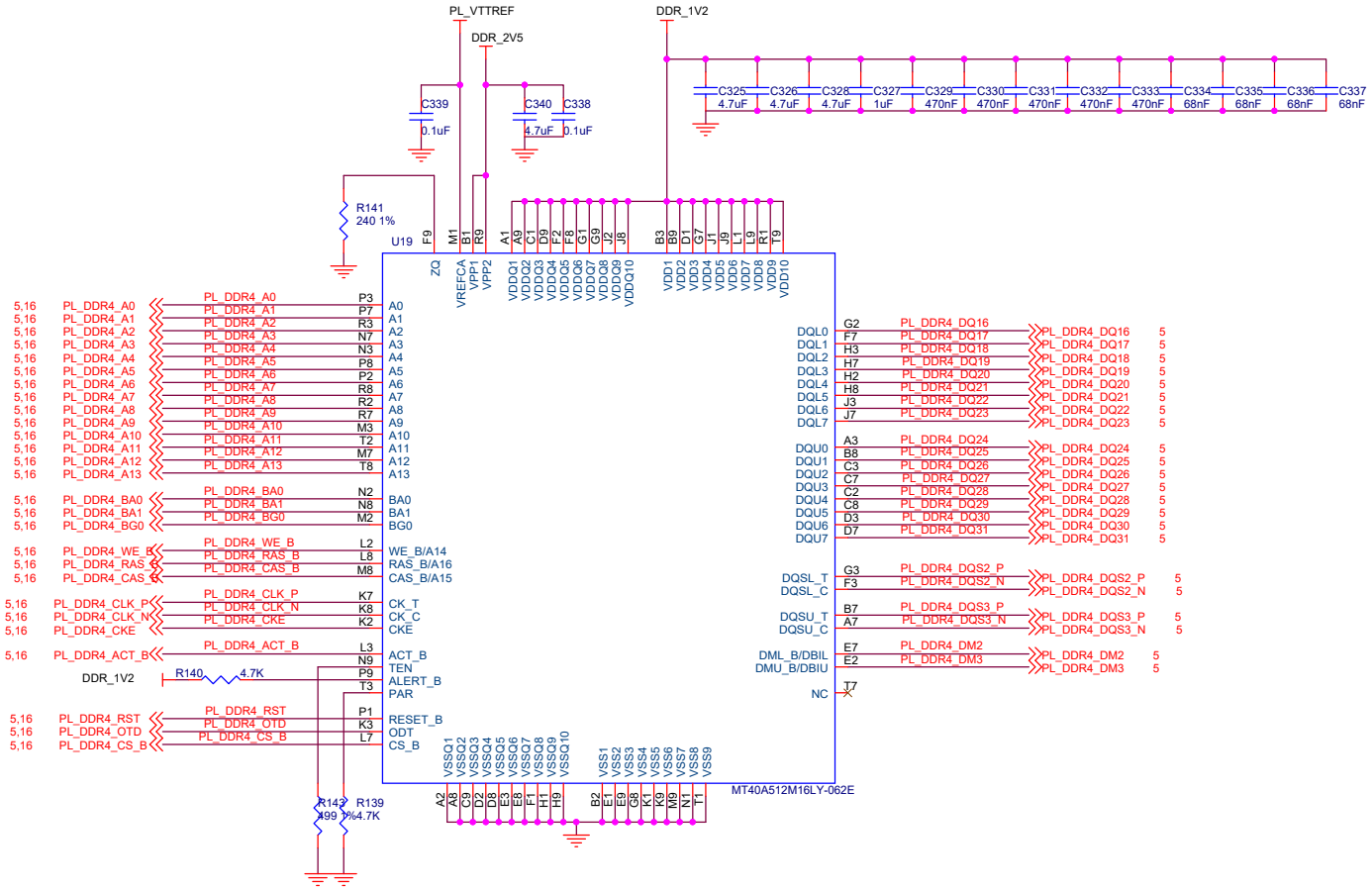

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Title	PAGE17 PL_DDR4_2	
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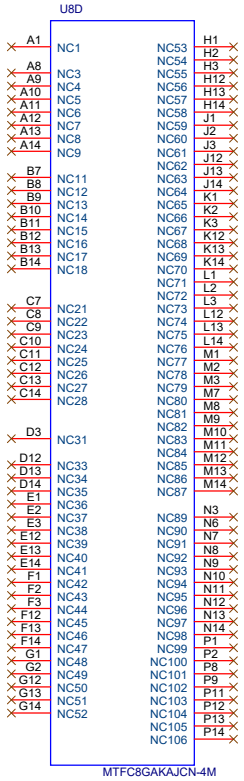

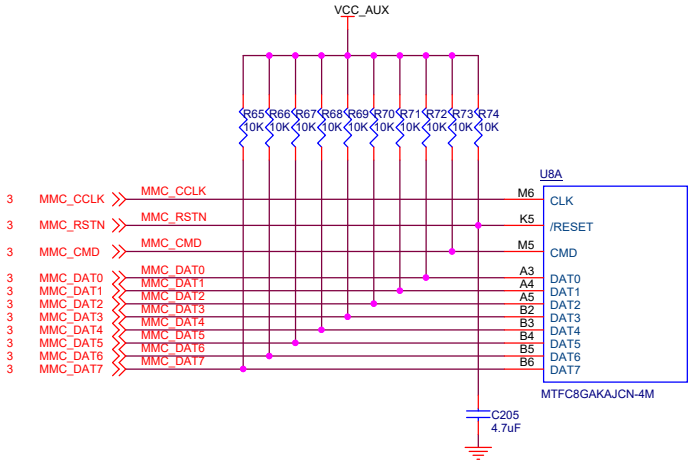

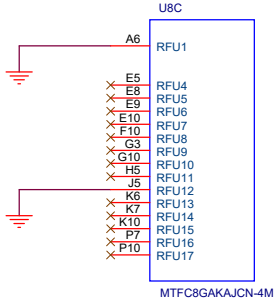

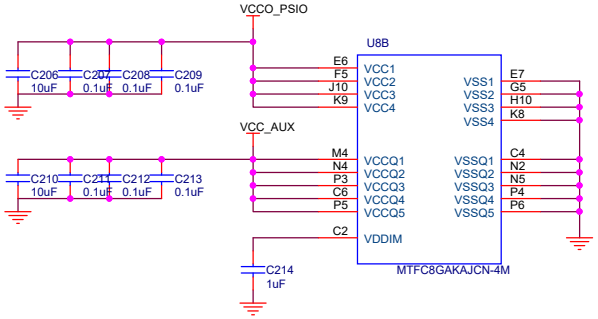

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Title: PAGE18 eMMC

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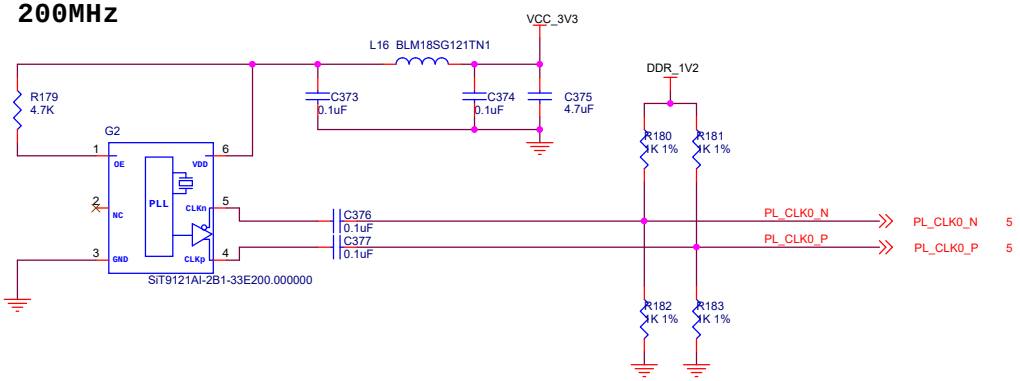
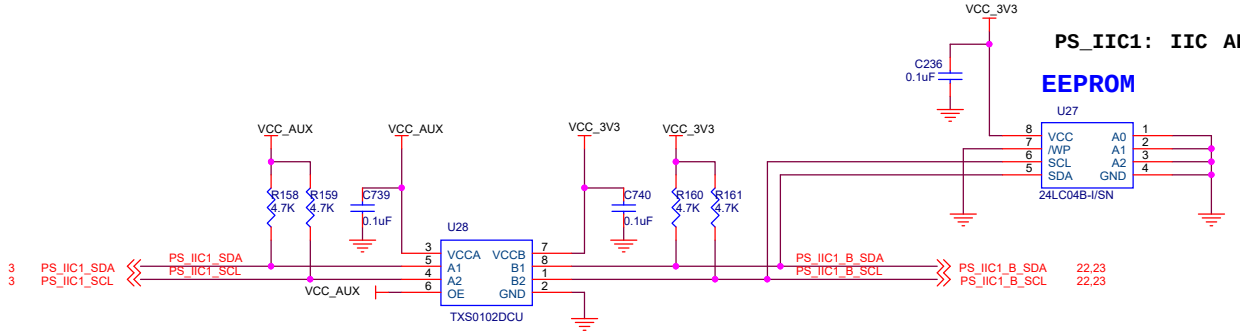
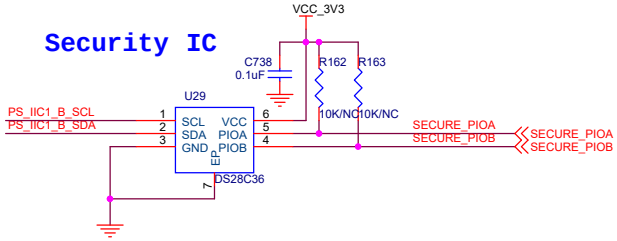
PL SYSTEM CLOCK

200MHz







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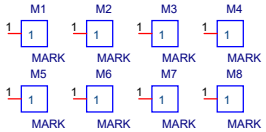

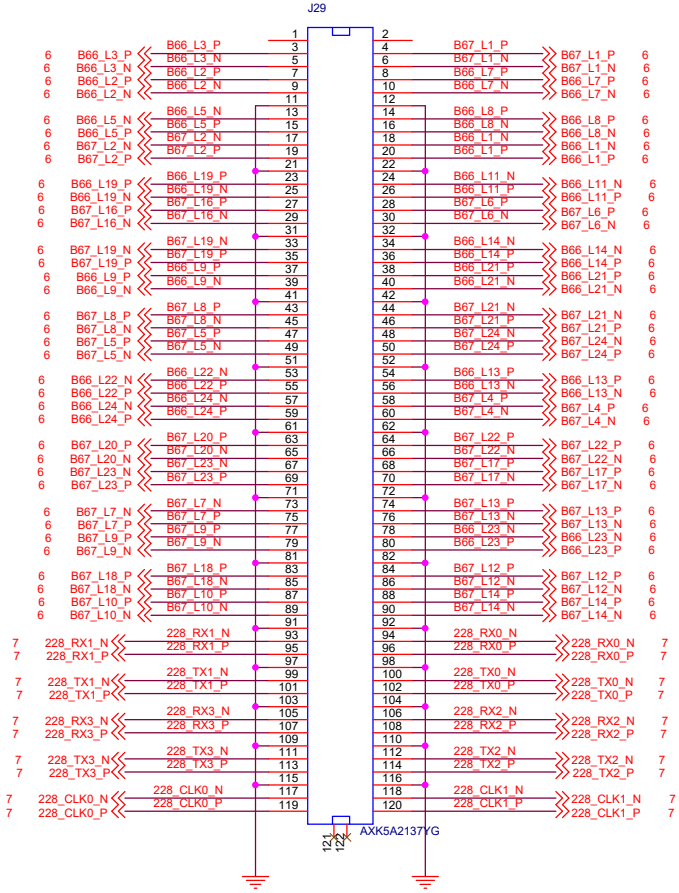

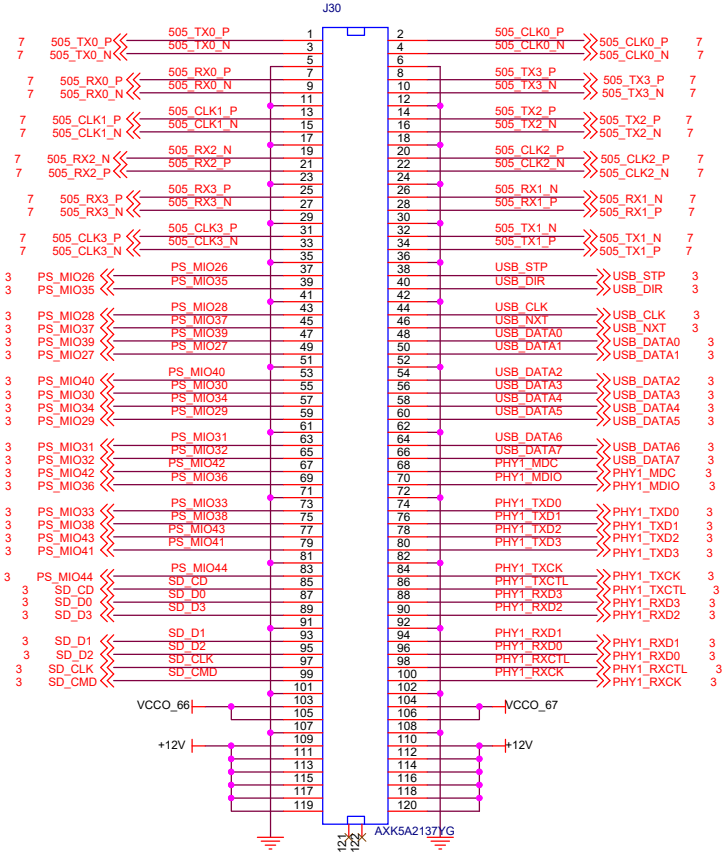

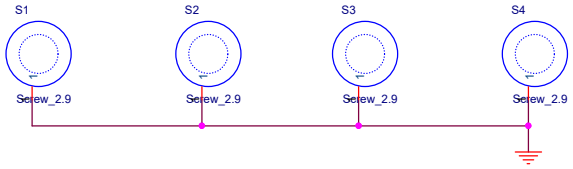

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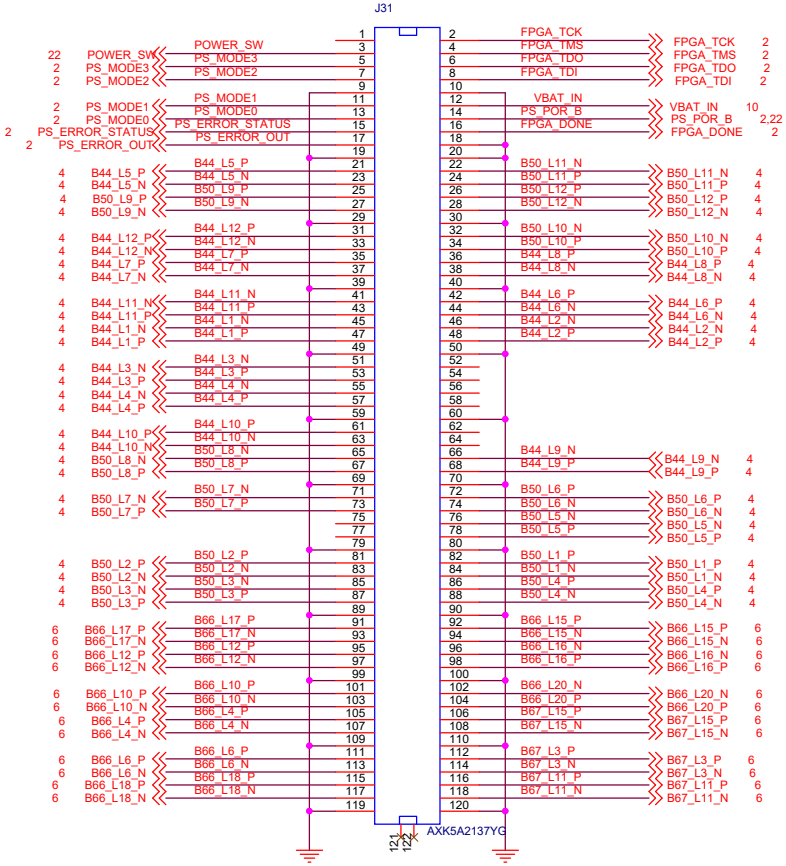

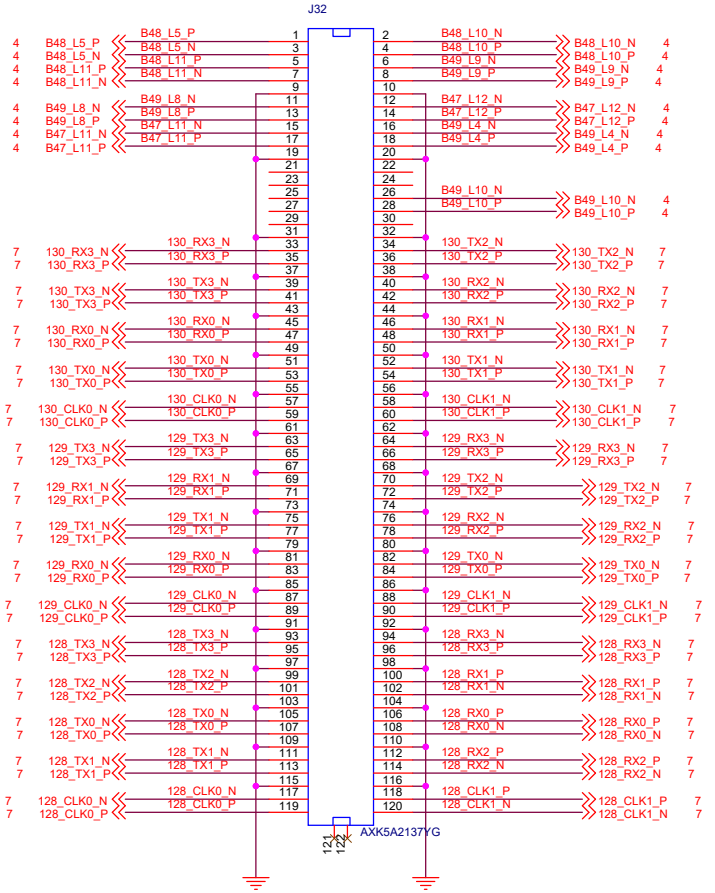

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Title	PAGE21 Connector_2
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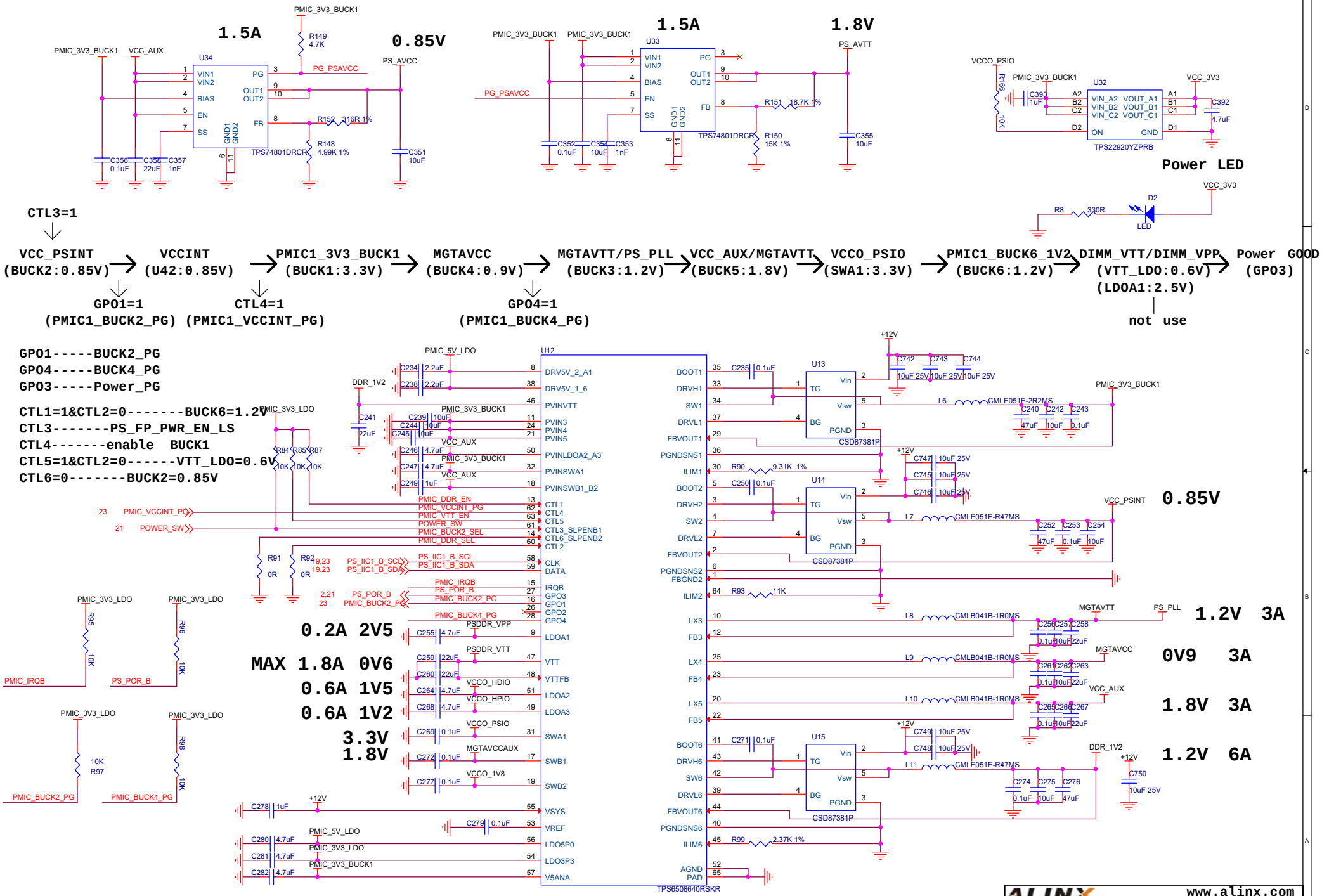
1.5A
0.85V
PMIC_3V3_BUCK1
VCC_AUX
U34
TPS74801DRCR
R149 4.7K
R152 316R 1%
R148 4.99K 1%
PG_PSAVCC
PS_AVCC
C356 0.1uF
C358 22uF
C357 1nF
C351 10uF
1.5A
1.8V
U33
PS_AVTT
R151 18.7K 1%
R150 15K 1%
C352 0.1uF
C354 10uF
C353 1nF
C355 10uF
VCCO_PSIO
U32
TPS22920YZPRB
VCC_3V3
C393 1uF
C392 4.7uF
R166 10K
Power LED
R8 330R
D2
LED
CTL3=1
VCC_PSINT (BUCK2:0.85V)
VCCINT (U42:0.85V)
PMIC1_3V3_BUCK1 (BUCK1:3.3V)
MGTAVCC (BUCK4:0.9V)
MGTAVTT/PS_PLL (BUCK3:1.2V)
VCC_AUX/MGTAVTT (BUCK5:1.8V)
VCCO_PSIO (SWA1:3.3V)
PMIC1_BUCK6_1V2 (BUCK6:1.2V)
DIMM_VTT/DIMM_VPP (VTT_LDO:0.6V) (LDOA1:2.5V)
Power GOOD (GPO3)
GPO1=1 (PMIC1_BUCK2_PG)
CTL4=1 (PMIC1_VCCINT_PG)
GPO4=1 (PMIC1_BUCK4_PG)
not use
GPO1-----BUCK2_PG
GPO4-----BUCK4_PG
GPO3-----Power_PG
CTL1=1&CTL2=0-------BUCK6=1.2V
CTL3-------PS_FP_PWR_EN_LS
CTL4-------enable BUCK1
CTL5=1&CTL2=0------VTT_LDO=0.6V
CTL6=0-------BUCK2=0.85V
U12
TPS6508640RSKR
PMIC_5V_LDO
PMIC_3V3_LDO
DDR_1V2
PMIC_VCCINT_PG
POWER_SW
PMIC_BUCK2_SEL
PMIC_DDR_SEL
PS_IIC1_B_SCL
PS_IIC1_B_SDA
PMIC_IRQB
PS_POR_B
PMIC_BUCK2_PG
PMIC_BUCK4_PG
PSDDR_VPP
PSDDR_VTT
VCCO_HDIO
VCCO_HPIO
VCCO_PSIO
MGTAVCCAUX
VCCO_1V8
0.2A 2V5
MAX 1.8A 0V6
0.6A 1V5
0.6A 1V2
3.3V
1.8V
U13
U14
U15
CSD87381P
CMLE051E-2R2MS
CMLE051E-R47MS
CMLB041B-1R0MS
9.31K 1%
11K
2.37K 1%
VCC_PSINT
0.85V
MGTAVTT
PS_PLL
1.2V 3A
MGTAVCC
0V9 3A
VCC_AUX
1.8V 3A
DDR_1V2
1.2V 6A
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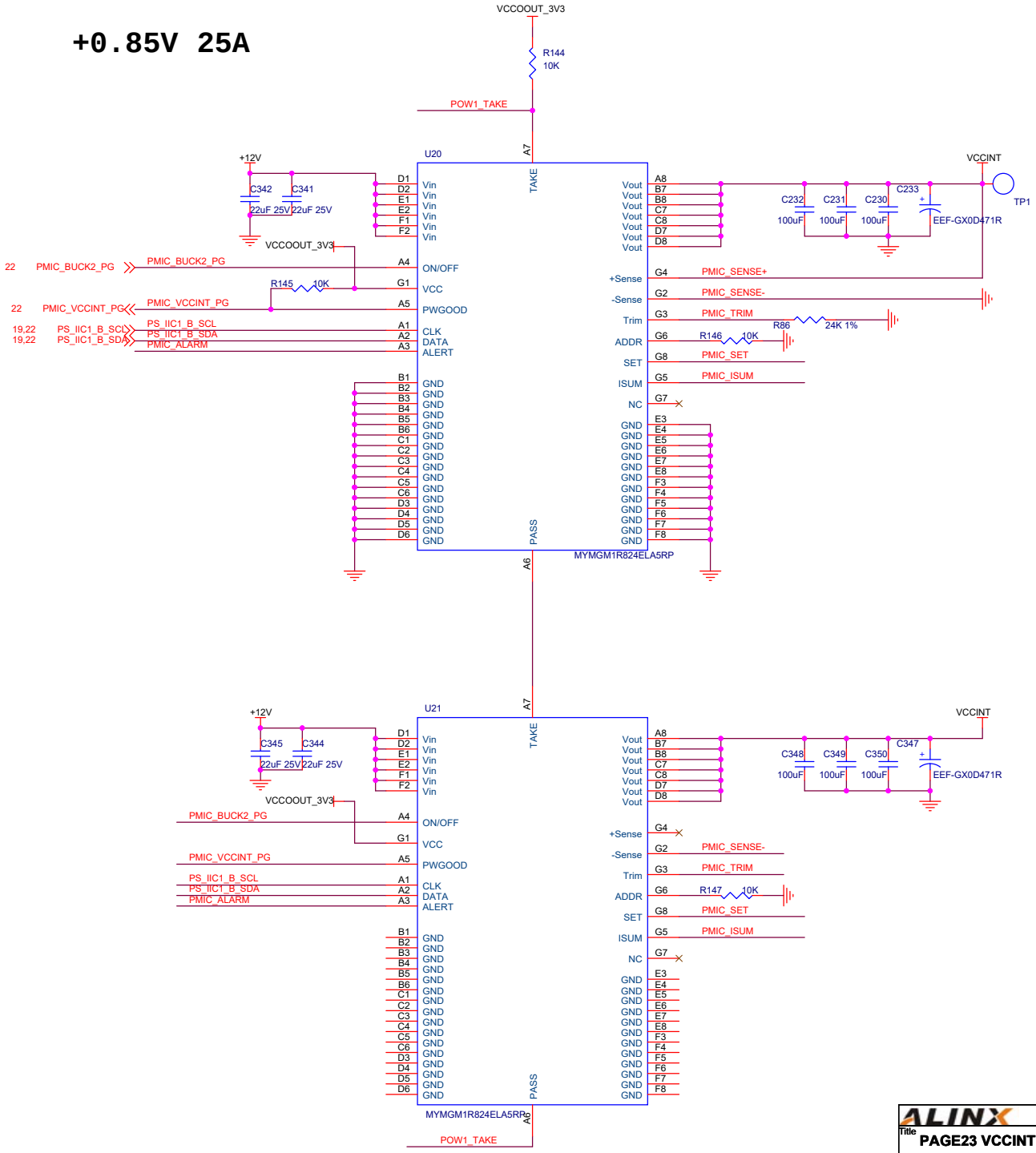
+0.85V 25A



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