



2024 PRODUCTS GUIDE

- SoC/FPGA
- ARM
- Embedded
- AI
- Drone
- Education





TECHNOLOGY

**Technology driven company specializing in embedded,
artificial intelligence, and drones with leading
technologies in Industry 4.0**

► **SoC/ASIC design techniques with Versal™ Premium VP1902 XilinxUltraScale+ VU19P, VU440, ZynqUltrascale+, Virtex7 and more**

Provides the ASIC Prototyping System required for Application Processor, Memory, Camera, D-TV, and Modem designs.

AMD Versal™ Premium VP1902 Adaptive XilinxUltraScale+ FPGA Boards
LPDDR3, DDR3, XAU1, eMMC, UHS-I, HDMI, USB3.0, PCIe, MIPI RDL design
Camera I/F, DMA, and AMBA RDL design
GTX, Impedance Matching technology, Clock Skew minimization
Camera imaging processing technology
Noise minimization with SI/PI
Power design

► **ARMCore (CortexA, CortexR, CortexM) based compiler and debugging technology**

Provides accurate and fast build and debug technology using ArmDS, DSTREAM, and MDK-ARM for ARM system development.

ARM all core Compiler C/C++ toolchain (DS-5) technology
64-bit ARMv8, 32-bit ARMv7 architecture support software technologies
ARMCore Debug and Trace Emulator Technology
Linux, Android debugging and profiling techniques
MCU Integrated development (MDK-ARM) technology based on ARM7, ARM9, and Cortex-M-based

► **Artificial Intelligence (AI) H/W and S/W technology**

It provides technology for handling unstructured data such as video, voice, images, and text and developing artificial intelligence through deep learning techniques.

Deep learning missing person image recognition SW technology
Pattern Recognition Technology Nvidia JETSON - Xavier, NX Platform
Nvidia + FPGAH/W Design Technology
AI, ARM, SoCs, Drones HUINS are here for the Digital World



THE ARCHITECTURE FOR THE DIGITAL WORLD

► Camera (EO/IR) imaging H/W, S/W technologies

We provide EO/IR, MIPI sensor interface technology, image processing algorithms, and network (LTE, WIFI) technology. We have developed solutions for real-time video streaming, camera inspection equipment, video algorithm processing, and many other applications.

- Wireless real-time video transmission technology
- E/O, IR cameras
- 4K video compression (H.264) transmission technology
- 24M, 16M RAW DATA Image Solutions
- Real-time temperature/video monitoring technology

► Embedded/Android Technology with ARMCore, ExynosCore

We provide firmware, Linux kernel, BSP design, and application software design from CPU selection for the optimal embedded system.

- Design and build embedded systems with i.mx8mini modules
- Mobile robots and ground control systems
- Medical devices
- Control terminal
- Designing USB-based application systems
- Monitoring systems with multiple cameras

► Drones, Internet of Things (IoT), and coding systems

- Aircraft Attitude and Guidance Control SW Technology
- 650g ultra-compact surveillance and reconnaissance drone
- Wired drones with 12+ hours of flight time
- EO/IR-based wireless drone with 30+ minute flight time
- Drones for firefighting, police, army, navy, air force, and public sector
- Collect and transmit video and sensor data in real time

HUINS MESSAGE



HUINS Co., Ltd. is a company with expertise in ARM Core-based solutions, SoC verification platforms, embedded solutions, artificial intelligence (AI), imaging technology solutions, IoT solutions, coding-Arduino systems, and DRONEsystems for the 4th industrial revolution, and has grown into a medium-sized company over the past 30 years. This is only possible because of your continued support and love. We'd like to extend a heartfelt thank you to all of our customers.

In recent years, ARM's CortexA, CortexR, and CortexM core technologies have become the standard for architectural design for a more securely connected world and the core technology for all advanced digital products, while multimedia and high-speed processing technologies have also advanced rapidly. HUINS Co., Ltd. provides various development environments for developers to apply more conveniently and reliably with novel and diverse conceptual designs.

For SoC verification, we provide verification platforms based on Xilinx FPGAs (AMD Versal™ Premium VP1902, UltraScale+ VU19P, MPSoC, ZynQ, etc.). With AMBABus, StereoCamera, DDR3/DDR4, LPDDR4, PCIe, USB3.0, SDIO, EMMC, ADC/DAC, and more on the platform, we have all the solutions you need.

HUINS' Embedded Systems provides firmware, middleware, and application technologies based on ARM processors, including embedded Linux kernels, device drivers, and Android, centered on NXP i.mx8mini processors.

For the implementation of AI technologies such as AI edge and server, we first supply the original technologies such as object recognition and autonomous driving based on Nvidia's Xavier NX or AGX core. AI is an important technology of the future that detects and judges objects in real-time through training data construction, labeling, and deep learning.

We are growing into a drone system company with products such as surveillance and reconnaissance micro drones, disaster monitoring drones, and tethered drones. We want to be the best company in Korea with drones for various missions on various airframes.

Growth is a core competency at HUINS and the beginning of everything we do. We will put all our passion into developing new technologies. Most companies have grown by emphasizing their core competencies, such as technology and global leadership. The practice of corporate growth is something only a few companies have achieved through relentless effort.

Your success is our joy. We look forward to being a true partner with you by providing the technology you need to succeed. Knock on HUINS' door. HUINS will continue to be the company that opens its doors and welcomes you today for the technology you need to succeed.

From all of us at HUINS Co., Ltd.

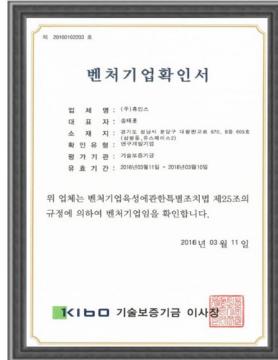
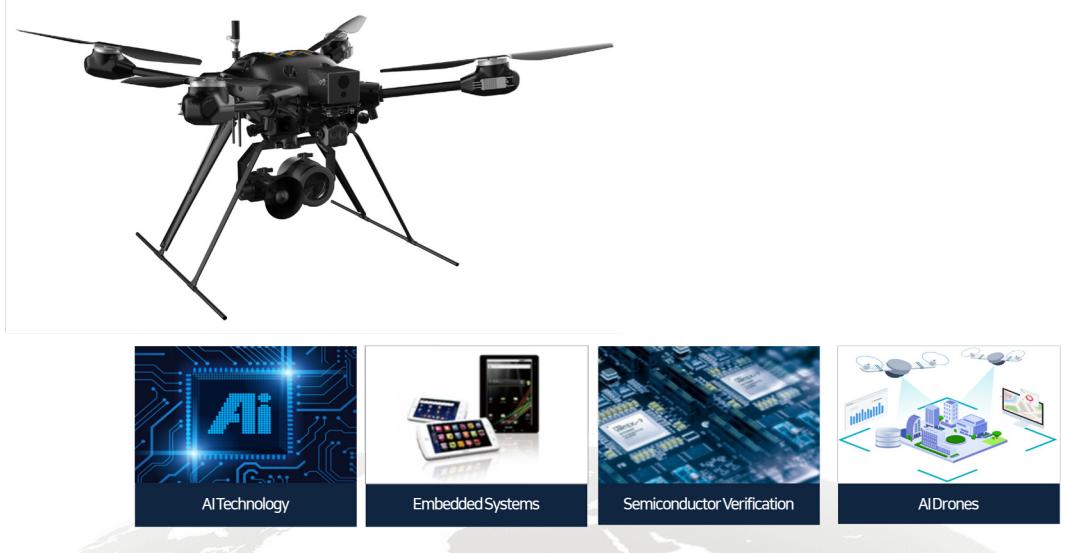
Song Taehoon

CEO of HUINS Co., Ltd./Doctor of Engineering



HUINS VISION

"HUINS is committed to developing products based on **core technologies** that are leading the way in **AI, embedded systems, and Drone innovation**, which are central to the **Fourth Industrial Revolution**."



Venture Business Certificate : 2001~



Innovative Innobiz Companies: 2001-2023



Brainpower Specialty Companies (Ministry of Industry)



Technical Assessment
Certificate of Excellence (T-3)



Corporate Credit Rating Certificate



Quality Management System
Certificate



Drone Factory Registration
Certificate

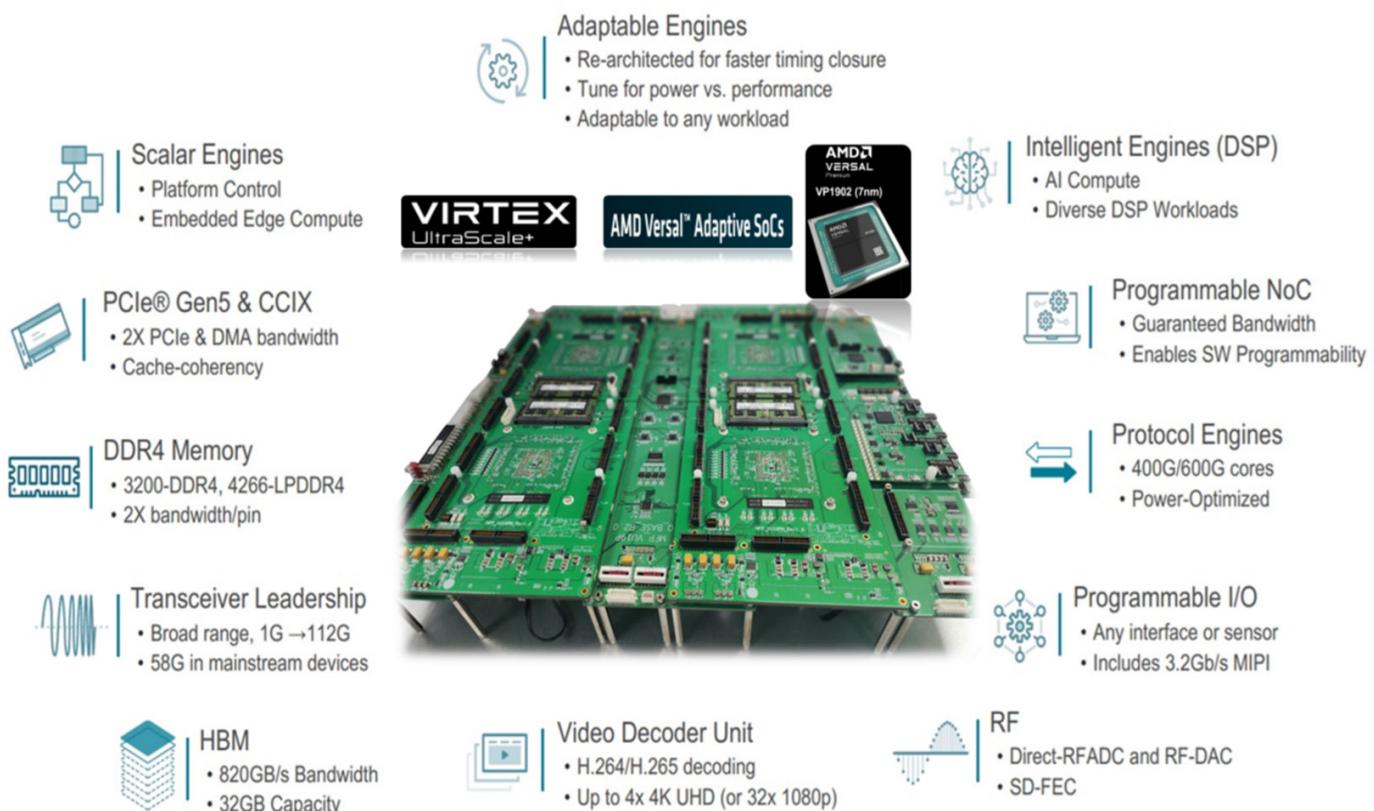
SoC/FPGA DESIGN STORY

► HUINS SoC/ASIC prototyping design is to design high-capacity FPGA boards for stable and reliable RTL and ARM Core verification in a short time.

- It is of utmost importance that FPGA boards operate reliably. In RTL design, behavioral instability of FPGA verification boards often causes engineers to spend a lot of time and fail to complete projects on time. We have the best technology in FPGA efficient placement, CPU module and interface, Clock Scheme, PCB Pattern design, Impedance Matching, SMT, Testing SW, etc.
- HUINS Co., Ltd. has been successfully designing FPGA boards for over 30 years. We design FPGA boards in a fast turnaround time and have the know-how of ARM Core. We also have experience designing Test SW and designing embedded, Linux, Windows CE, and RTOS.
- Beyond FPGA board design, we have skills in ARM Core and ARM Debugging, RTL Verilog HDL analysis, DDR4/DDR3 timing analysis design, high-speed I/O design, DVI module design, HDMI design, PCI Express, Card bus, USB/Ethernet module interfaces, ADC/ADC, etc.
- With the best technology in Korea, HUINS aims to provide the most stable and efficient boards. Users can minimize the cost of unnecessary H/W fabrication and debugging.
- HUINS Co., Ltd. has experience in many projects at Samsung Electronics, LG Electronics, Company E, Company C, and the Korea Electronics and Telecommunications Research Institute.

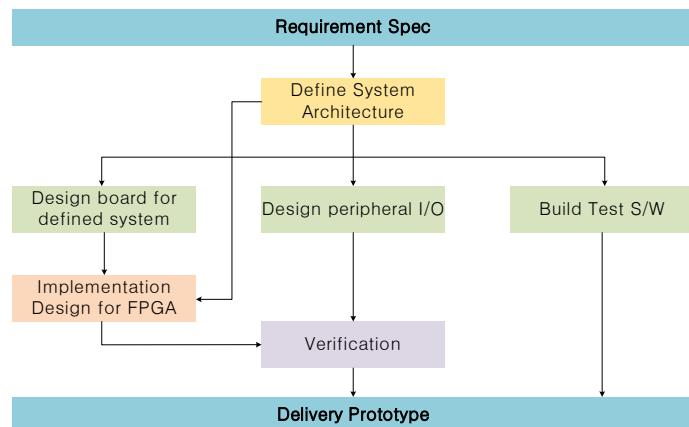
► Possess core semiconductor verification technology

- System-on-chip (System on a Chip) design verification
- Semiconductor RTL Design verification
- FPGA-based Prototyping (Xilinx)
- Zynq Arm Interface
- Possess PCIe, DDR3/4, MIPI, DP, HDMI, Vx1, and USB3.0 technology



► SoC/FPGA Prototyping Service

- System-Level Verification Service with FPGA Prototyping
- RTL and Peripheral H/W Prototyping
- Testing S/W Development
- . Highly efficient
 - Less time than developing a dedicated board and no board familiarization time required
 - Low cost: Reduce unnecessary HW production and debugging costs
- . Prototyping demo from design specification to finalization
 - Using Xilinx and Intel Altera FPGAs
 - System Design with Zynq and Other Processors
 - UFS, DDR4, ADC/DAC, PCIe Gen4, USB 3.0,
 - MIPI C-PHY, D-PHY, Modem I/F, TFT LCD,
 - Various peripheral interfaces, including DVI, HDMI, and more
 - Develop S/W (F/W, OS Driver) for System Level Verification

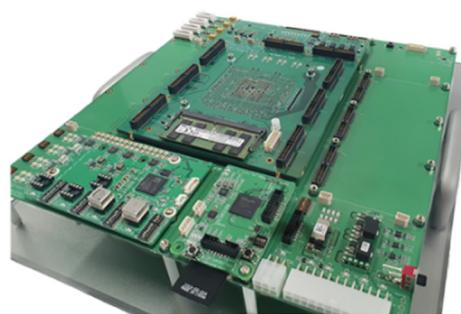
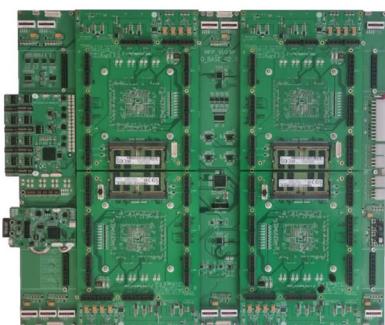


► Versal™ Premium VP1902 Adaptive SoC & ASIC Rapid Prototyping System : MFP-VP1902-S



- VERSAL PREMIUM XCVP1902 single FPGA Board
- XCVP1902-2MSEVSA6865 XILINX VERSAL FPGA Chip mount
- 18.5 Million system logic cells, total 2,000 I/O
- Dual ARM Cortex-A72 MPCore™, Dual ARM Cortex™-R5F
- DDR4 SODIMM x 2, Max. 3200MHz, 32GB x 2
- Peripherals: GigaEth, USB, SD, QSPI, UART
- FMC+ x 8, QTH x 3, NVAF x 2, QSFP-DD x 2 Extension Connector
- GTYP 64 Lane(8 Lane 8ea), GTM 32 Lane(8 Lane 4ea)
- Clock Module (CLK 0~3) Clock Generator 6.25 ~ 400MHz
- Supports up to 8 individually adjustable Vccos
- Supports remote download and control of Power/Reset/Config via USB
- User Daughter Module Support

► Virtex Ultra Scale+ VU19P FPGA ASIC Rapid Prototyping System : MFP-VU19P-Q

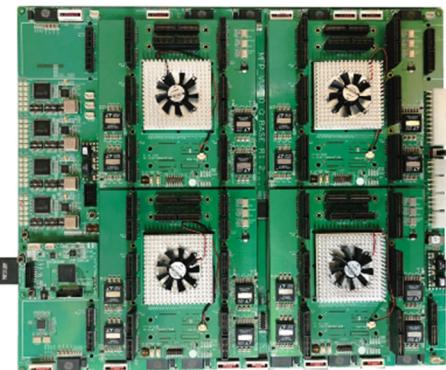


- Consists of four Virtex UltraScale+™ VU19P FPGA modules and board
- FPGA Module with Virtex UltraScale+™ XCVU19P-FSVA3824 Chip Mount or Socket
- 4 MFP-VU19M Module S-mountable Base Board
- Six 119pin extension connectors
- 48 million Asic Gates, providing a total of 1,742 I/O * 4
- High Speed SAMTEC QTH Connector Expansion
- DDR4 So-DIMM (Supports up to 32GB)

- FPGA JTAG & SelectMap Configuration SD card
- Power/Reset/Config control by USB
- Clock 4 Differential Signals and 4 Single Ended Signals, with 8ea Clock
- GTY 48 Lane Connector * 4
- Provides up to four individually adjustable voltages
- Power/Reset/Config control by USB (Remote bit file download & control)
- MFP-Series Daughter Module Compatible

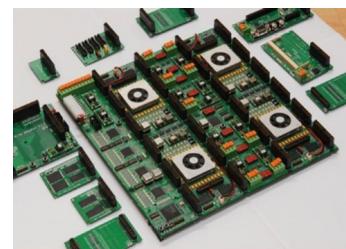
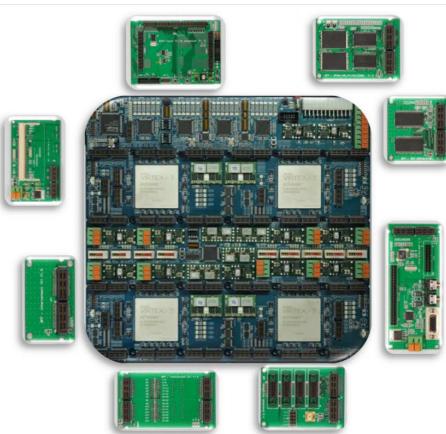
SoC/FPGA DESIGN STORY

► Virtex Ultra Scale VU440 FPGA 4 ASIC Rapid Prototyping System : MFP-VU440-Q



- SoC/ASIC design and verification that can mount one to four Virtex Ultrascale VU440 FPGA
- XCVU440-FLGA2892-1 Logic Cells : 5,065,920
- Universal I/O: 1,244 general-purpose I/Os per FPGA via high-speed SAMTEC connector (Top: 668 Pin I/O, Bottom: 576 Pin I/O) a total of 4,976 Pin I/O
- GTH transceiver: 32 Lane GTH transceiver I/O per FPGA (Top: 16 Lane, Bottom: 8 Lane) 128 GTH I/O in total
- High capacity memory with two DDR4 SO-DIMM sockets up to 32GB DDR4
- JTAG Configuration Config Time 30Sec. SD card SelectMap
- FPGA fast download of 16 design files from Micro SD card
- PCIe Gen3 Dual Port Support (PCIe Gen3, Gen2, and Gen1 standard profile form factors x1, x2, x4)
- Shorten image loading time Config time with SD card Select Map about 30 Sec.
- 1.2/1.5/1.8/2.5/3.3V Variable Regulator
- Chip to Chip connection Variable connection between FPGA
- Provides GTH transceiver 32 Lane GTH transceiver I/O
- DDR4 SO-DIMMs up to 32GB DDR4 memory support
- JTAG Config Time 30Sec. SD card SelectMap

► SoC Prototyping (Virtex7 2000T FPGA) MFP-7V2000T-Q



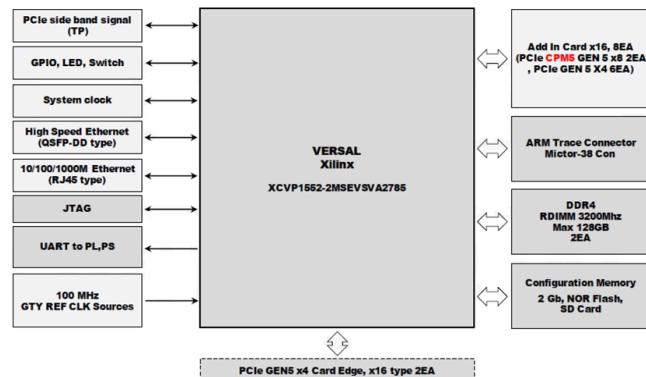
HUINS Prototyping Services helped us to successfully complete our FPGA prototyping project for the next-generation platform.

Samsung Electronics in Korea has developed and distributed Smart-TV system in the worldwide. Samsung wanted to verify IPs of Smart-TV for their next generation of Smart-TV system, Samsung needed to implement a rapid prototyping solution based on Xilinx Virtex7 FPGA platform. And, Samsung wanted to verify many kinds of peripherals on this platform.

The MFP-7V2000T-Q is a high performance ASIC prototyping based on quad Xilinx Virtex7 V2000T FPGAs for SoC/IP Verification. It provides a flexible and expandable ASIC / SoC prototyping platform. The same platform can be reused in several projects or configurations by replacing optional boards containing I/O and custom subsystems.

MFP-7V2000T-Q is carefully designed for maximum performance, with respect to signal integrity, speed and other critical issues

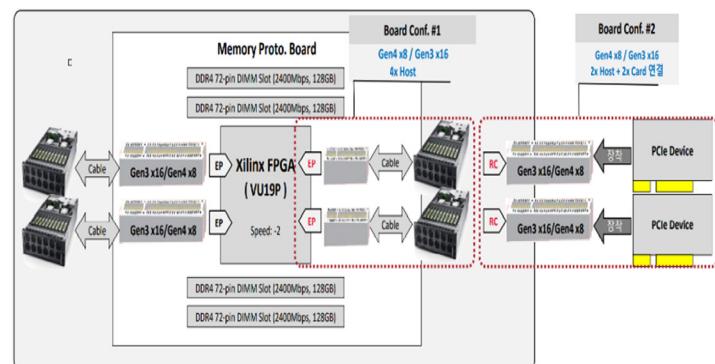
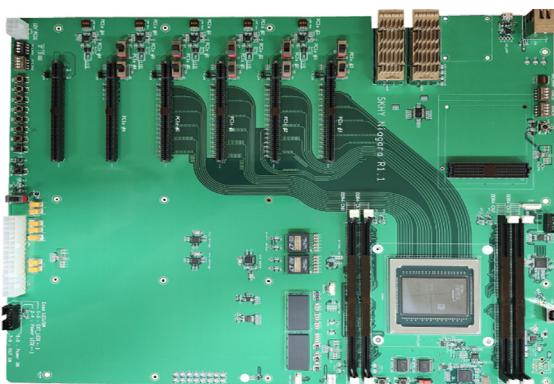
► 1. (Company F) Versal™ Premium VP1552 PCIe Gen5 CXL Bridge Platform



Features

- PCIe/CXL Switch Test Board
- PCIe Gen5 X 8ea interface :CPM5 Gen5, 8 Lane X 2, PL PCIe Gen5, 4 Lane X 6, Edge PL PCIe Gen5, 4 Lane X 2
- DDR4 RDIMM : Target: DDR4 2933Mhz 128GB RDIMM slot 2ea
- QSFP-DD 1 slot
- RJ45 Ethernet, UART

► 2. (Company S) Customizing FPGA Board : PCIe Gen4 CXL Verification Platform

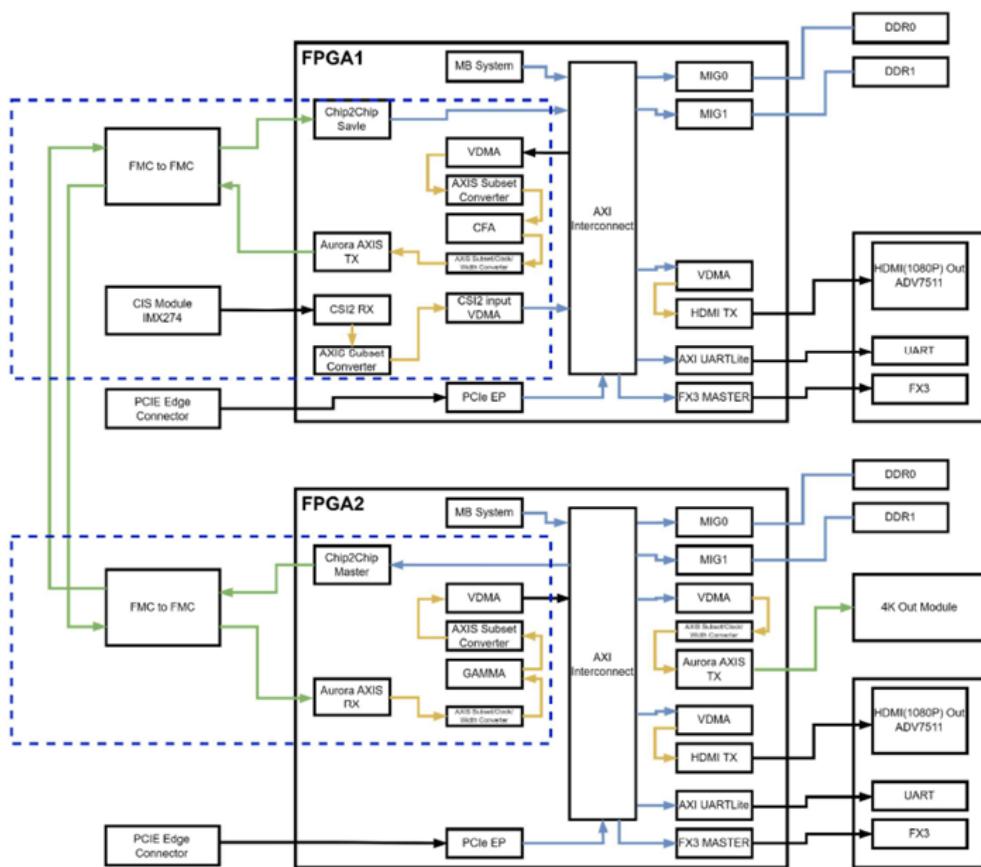
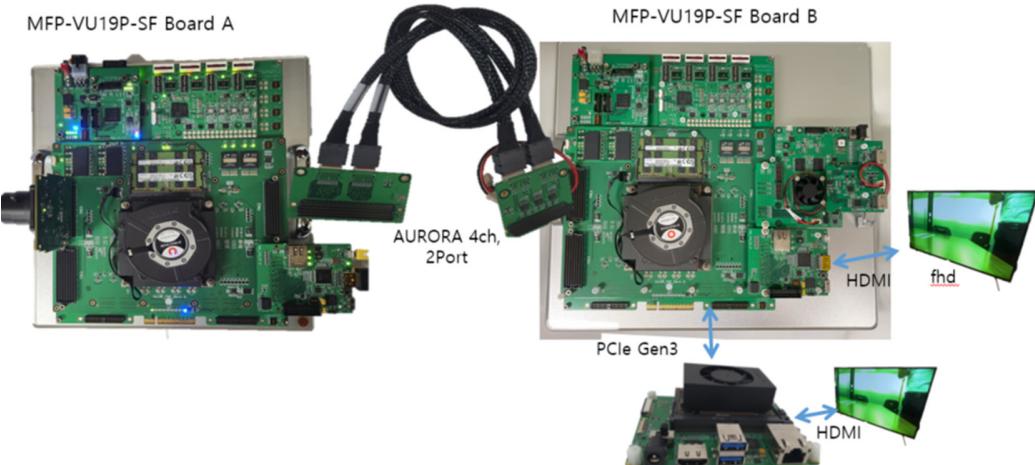


Features

- FPGA Xilinx XCVU19P-2FSVB3824
- 4x PCIe I/F : 4x Host I/F (PCIe Gen4 x8 or Gen3 x16)
- 2x Host I/F + 2x Card I/F (PCIe Gen4 x8 or Gen3 x16)
- 4x DIMM I/F : 4-channel DDR4 72-bit @2400Mbps, Min. 128GB/channel
- PCIe Gen4 x4 (M.2, for NVMe expansion), Option (QSFP, FMC Connector)
- Soft Core (Micro blazer), Debug I/F (JTAG, UART, USB, LED, Button, Switch etc.)

SoC/FPGA DESIGN STORY

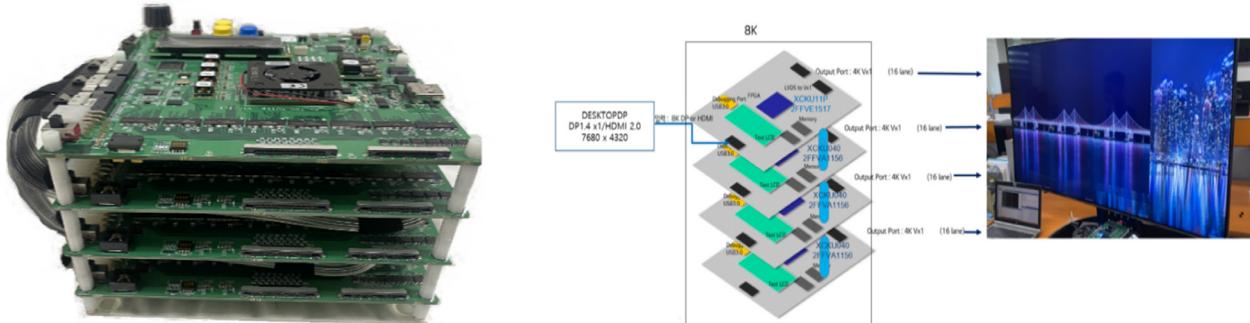
► 3. (Company S) VU19P-FMC CIS HDMI Platform



Features

- Store CIS input into DDR with VDMA via CSI-2 rx subsystem for CIS input
- The raw image is converted into an rgb image by sensor demosaic using the stored data through VDMA
- Outputs RGB data stored in DDR to HDMI TX via VDMA
- Access DDR via USB 3.0, Read write data
- FPGA1 : CIS-2 Input -> DDR4 -> CFA -> FPGA2
- FPGA2 : FPGA1 -> GAMMA -> DDR4 -> HDMI Output

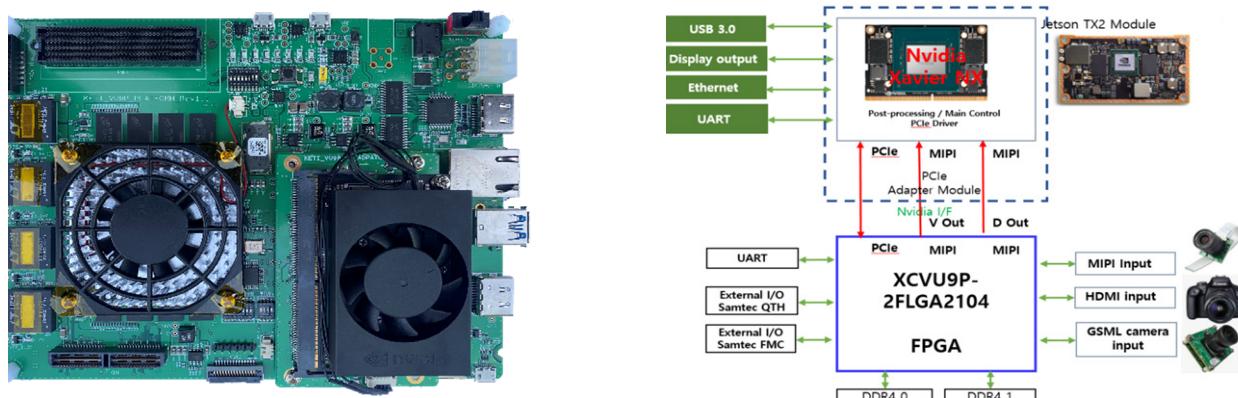
► 4. (Company L) Customizing FPGA Board : 8K Test pattern Generator



Features

- The 8K test pattern generator is a test signal generator equipped with test patterns including HDR patterns up to 4K and 8K images and VX1 and DP
- The 4K and 8K OLED UHD test pattern generator can be conveniently controlled through button operation, automatic playback pattern output, and USB 3.0. You can select and control timings, patterns, color spaces, DP, and VX1 output.
- DP connectors 1Port input, VX1 4port output.
* DP (DP 1.4 to DP 1.4-8k @ 60 Hz 4k @ 120 Hz) and HDMI 2.0 compliant.
- Resolution :
* UHD 3840x2160, FHD 1920x1080, QHD 2576x1440, WQHD 3440x1440
* WQHD 3456x1600, 8K (4-way split), 8K (1 Frame), WQHD 3456x1456, QHD 2576x1456, HD 1366x768, 1920x480, 1366x768
- USB 3.0 : USB C-Type connector.
- RS232 : Micro USB connector.
- TEXT-LCD Panel Interface
- * Display status such as pattern name and encoder value, display input timing

► 5. (Company K) Edge FPGA for Vision AI "NVIDIA Jetson & FPGA Integration, Vision, and Deep Learning Edge Platforms"

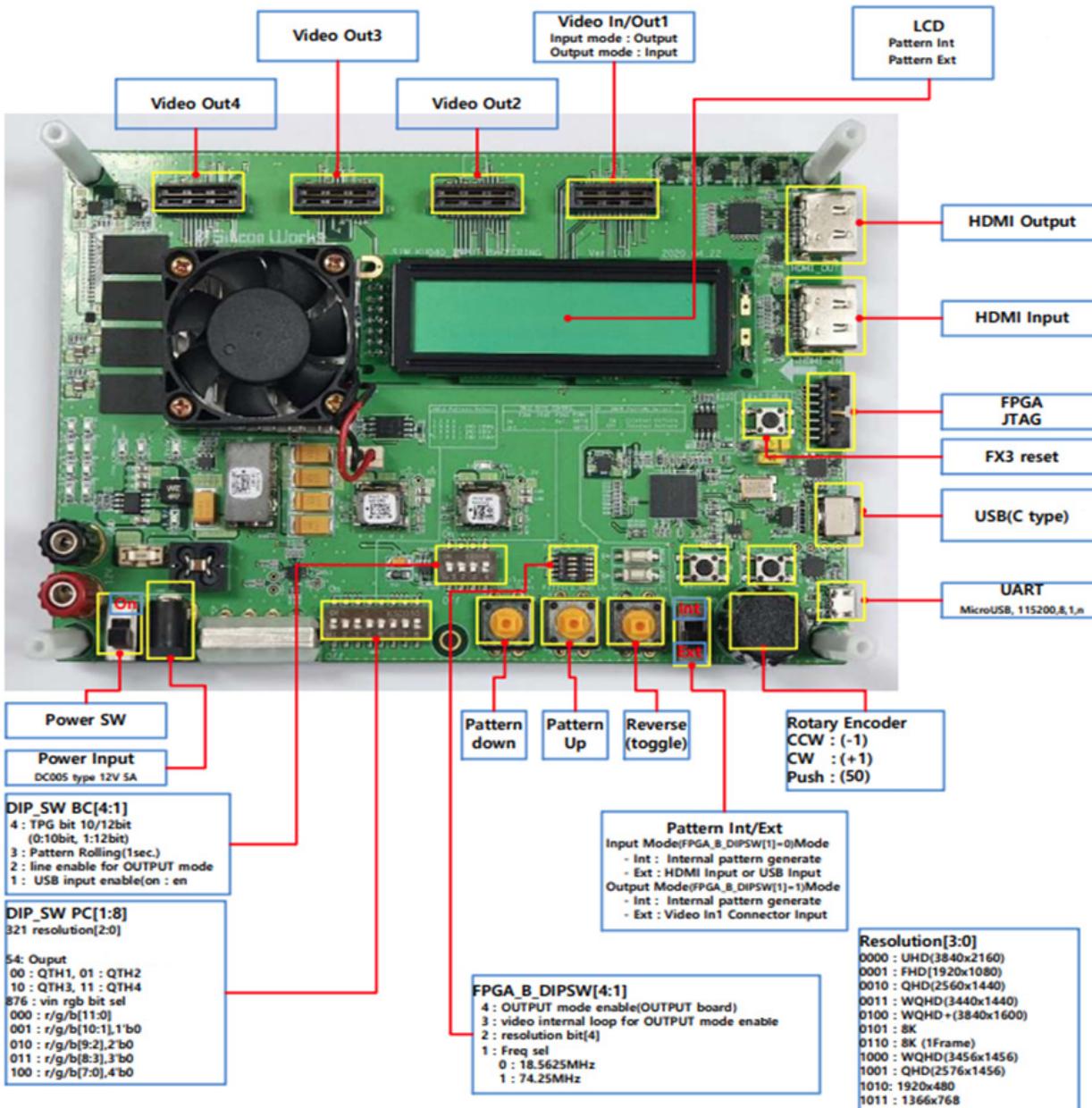


Features

- Xilinx Virtex UltraScale+™ XCVU9P FPGA
- NVIDIA Jetson AGX Xavier
- 2 GB of dual 2x 64bit wide DDR4 Memory to FPGA
- HDMI RX, MIPI, GSML - Camera Interface
- FMC QTH Expansion connector

SoC/FPGA DESIGN STORY

► 6. (Compnay L) KU040 Input/Output Buffer(TV Test Pattern Generator)

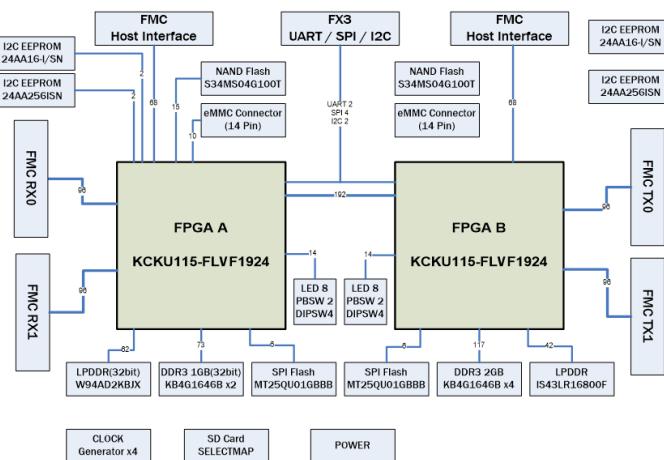


Features

- XCKU040-2FFVA1156I FPGA
- SDRAM 4Gbit *4ea
- INPUT Connector : HDMI-PC Connection
- Output Connector : HDMI-TV Delivery
- Output Timing : real time
- Resolutions : UHD(3840x2160), FHD(1920x1080), QHD(2576x1440), WQHD(3440x1440), * WQHD(3456x1600), 8K(4-way split), 8K(1Frame), WQHD(3456x1456), QHD(2576x1456), * 1366x768, 1920x480, 1366x768
- Video In/Output Port 4ea
- FX3 USB3.0 C-Type connector.
- RS232 : Micro USB connector.
- Display status such as TEXT-LCD pattern name and encoder value, display input timing
- Inside Pattern Generator support
- Power Input: DC 12V, 5A

► 7. (Company L) HDMI 2.0 / Vx1 / DP1.2 - 4K 60Hz, 4K 120Hz Verification Platform

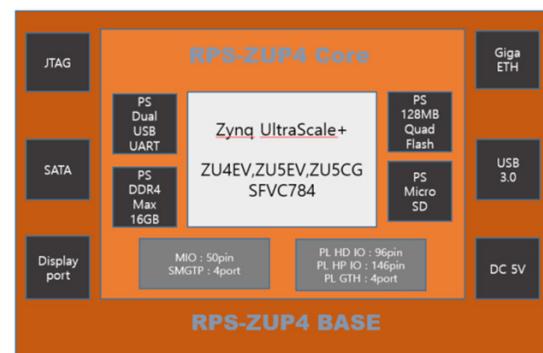
It is an FPGA system that can verify HDMI 2.0, Vx1, Display Port images 4K 60Hz, and 4K 120Hz for timing controller verification.



Features

- Provides IO to test HDMI, Vx1, and Display Port - ARM coat M4 MCU with large buffer memory
- Provides HDMI, Vx1 Pass Test logic to test T-Con
- FPGA (XCKU115-2FLVF1924 *2EA)
- STM32 MCU(UART, Ethernet, USB, I2C, SPI, SDMemory, JTAG..)
- NOR, EEPROM, NAND, DDR3/LPDDR, UART, USB2.0, Ethernet..
- DDR3/LPDDR SDRAM (Data buffer)
- Vx1 / HDMI / DP Daughter Board

► 8. (Company K) Zynq UltraScale+ MPSoC Verification Platform

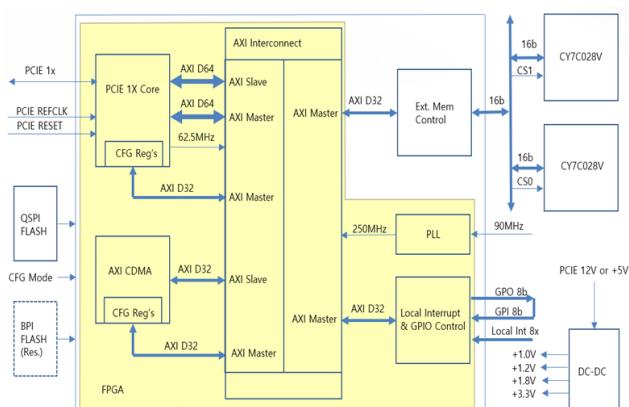
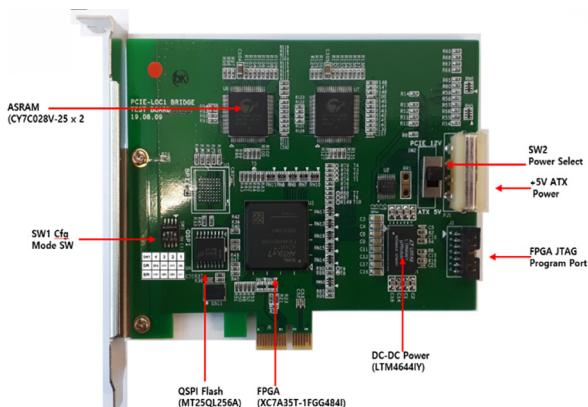


Features

- Platform for automotive, industrial, video, communications applications
- Quad ARM Cortex-A53, Dual Cortex-R5 Realtime Processor
- Based on 16nm FinFET + programmable logic fabric
- Mali-400 MP2 graphics processing unit
- Use PL/PS interface to develop a variety of applications
- The RPS-ZUP4ZYNQ UltraScale+ platform consists of a core module and a base board, and the core module extends to the base and large-capacity VU440 FPGA board with a Samtec connector for application as a CPU module
- MIO 50pin, SMGTP 4port, PL-HD IO 96pin, PL-HP IO 146pin, PL-GTH 4port Provided.

SoC/FPGA DESIGN STORY

► 9. Operational Accelerator Interface FPGA Board

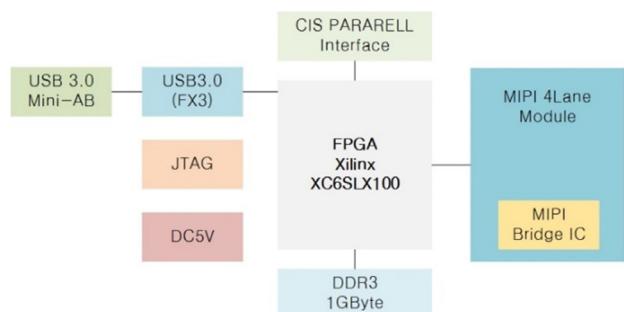


Features

- PCI Express interface and Local Bus
- Root Complex and Endpoint PCI Express mode support
- PCI Express single-lane(x1) port (one Virture Channel)
- PCI Express 2.5Gbps per direction
- Dual Port Memory(200kbytes and above)
- Memory Access on PC, DSP (Read/Write)
- PC : Windows7 32bit, Windows 10 64 bit
- PCIe : Gen2
- Memory : 128Kbyte 2EA
- Memory Access Speed : 10kbytes / 10ms

► 10. (Company S) USB3.0 4Lane MIPI CIS Capture Board

MIPI 4-Lane/Pararell CIS input, and the image captured in the FPGA's Dual DDR3 Memory is USB 3.0 interface. This allows you to implement a full camera module test on your PC.

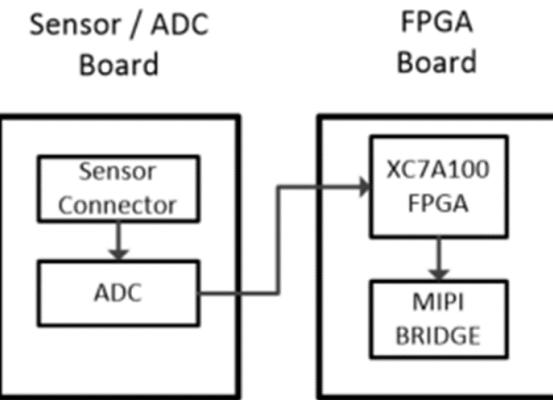
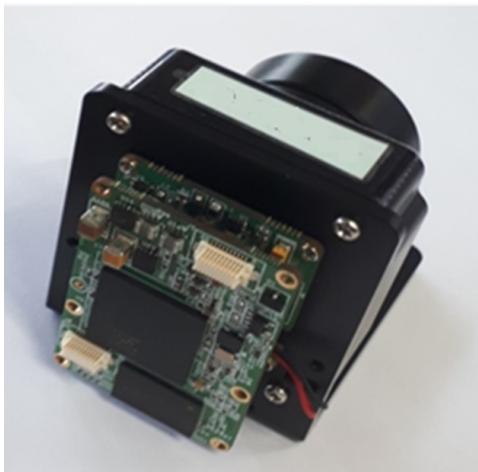


Features

Using an image capture image captured image capture part of the image capability and the PC to PC
It consists of view applications such as pixel quality of the camera module

- Stable, simple H/W, S/W structure
- Customization is possible with FPGA (XC6SLX100).
- DDR3 SDRAM 512MB x 2ch (data buffer)
- MIPI 4-lane sensor support
- Upload capture images using USB 3.0
- Parallel Sensor Support

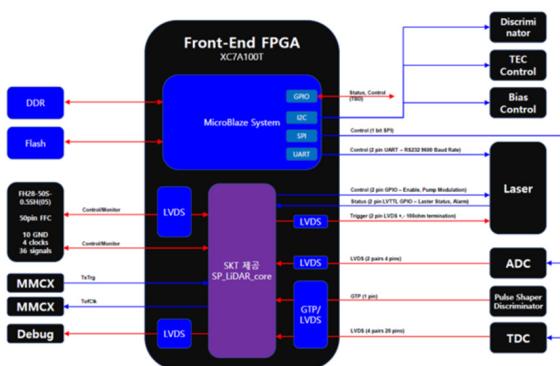
► 11. IR Sensor(Detector) to MIPI C Platform



Features

- Digital change of IR Sensor (Detector) Analyst DATA
- On the FPGA, the wave parameter settings required by Detector are set
- FSYNC/LSYNC, NUC/BPC/AGC/FFC
- Signal output of FV/LV/DATA (RGB565) to MIPI Bridge
- MIPI Bridge (TC358746) is FPGA output
- RGB565 signal MIPI CSI-2 signal conversion output
- FPGA : XC7A100T
- DDR2 SDRAM:MT47H32M16NF-25E (64MB)
- PROM : MT25QU128ABA1EW7-0SIT #0 : config PROM
- MT25QU128ABA1EW7-0SIT #1 : LUT A / LUT B PROM
- MIPI Bridge :TC358746
- ADC : AD9240

► 12. Lidar Integrated Systems

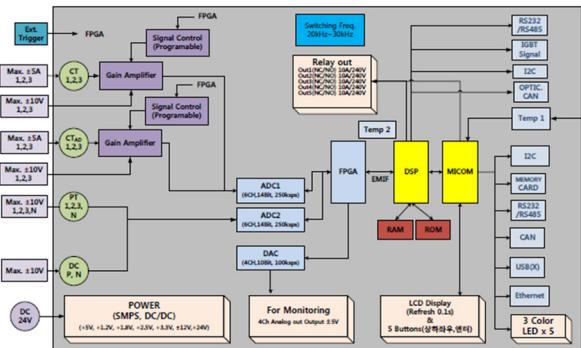


Features

- FPGA : XC7A200T
- DDR2 SDRAM : MT47H128M16RT-25E x 4ea (1024MB)
- PROM : MT25QU128ABA1EW7-0SIT #0 : config PROM
- ADC : HMCAD1511
- POWER 12V DC Power FPGA / Peri, ADC, DRIVER/TDC Power

SoC/FPGA DESIGN STORY

► 13. Active filter control Board



Features

- TI Company's TMS320F28335, ADC 6CH/14bit/250 kHz Simultaneous Sampling
- DAC 4CH, 10bit, 100ksps
- FPGA is ADC1, 2 Read every 200 kHz
- Gain Amplifier(Gain 1~16 adjustment)
- The MCU operates and demonstrates HMI, and implements parameter communication to the FPGA and DSP

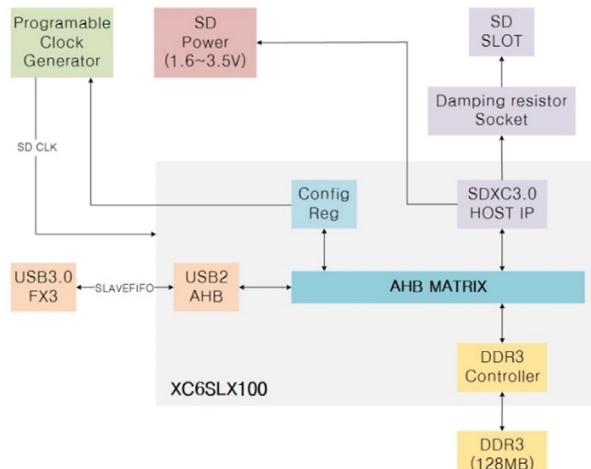
► 14. UHS-I Test System

SDXC3.0 Controller IP is implemented within the FPGA as a system for testing the UHS-IS SD card, and the PC

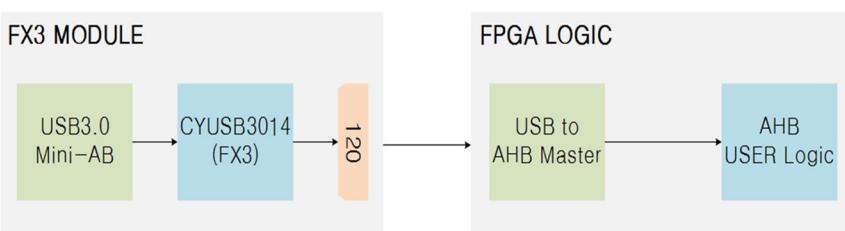
It was directly driven by Firmware and interfaces with USB 3.0.

Features

- XC6SLX100-FF484
- SDXC3.0 HOST Controller
- DDR3 SDRAM Controller(128MB)
- I2C Master IP
- Variable Reference SD CLK
- USB3.0 Peripheral
- SD CARD Power Voltage adjustment



► 15. AHB System via USB 3.0



Features

The solution consists of a USB 3.0 Peripheral Controller module and a USB-to-AHB Master IP inside the FPGA, which allows you to debug AHB systems by reading/writing from a PC host to a target AHB system through an address. AXI systems can also be debugged using AHB2AXI bridges.

▶ 16. MIPI CSI-2 to Parallel Bridge



Bridge module that converts the output of the MIPI CIS sensor to the Parallel method.
It supports up to 4 lanes and supports MIPI interfaces up to 2.4 Gbps with Parallel output up to 24 bits and 100 MHz.
Connect an image sensor in the form of CSI-2 to the FPGA or AP in Parallel.

Features

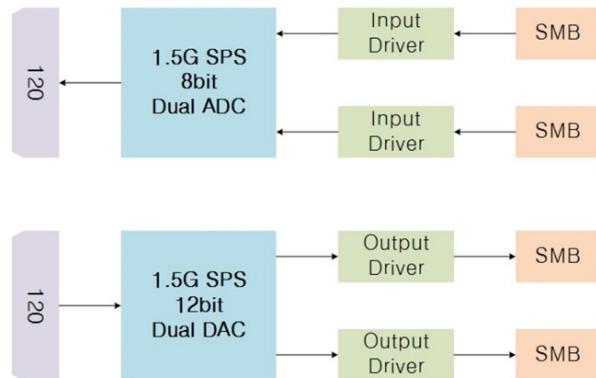
- MIPI Bridge
- 1~4 Lane Support
- 8/10/12/24bit Data
- Max 100Mhz PCLK output

▶ 17. High Speed AD / DA Converter

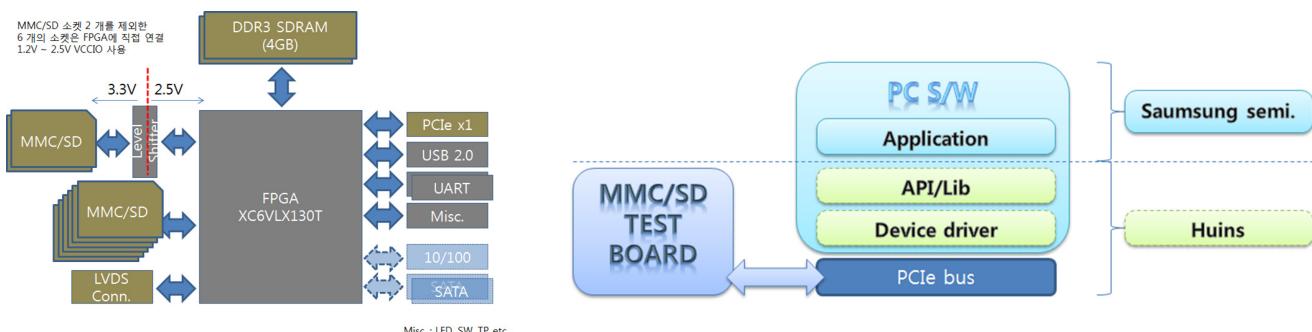
Dual Channel Data Converter Board available for Communication and Data Acquisition System.

Features

- Dual channel 1.5G SPS ADC(8bit)
 - * 16 LVDS Pair(1:2 DEMUX output)
- Dual channel Gpsps DAC(12bit)
 - * 48 LVDS Pair (4:1 MUX input)

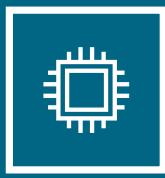


▶ 18. MMC/SD Memory Test Platform

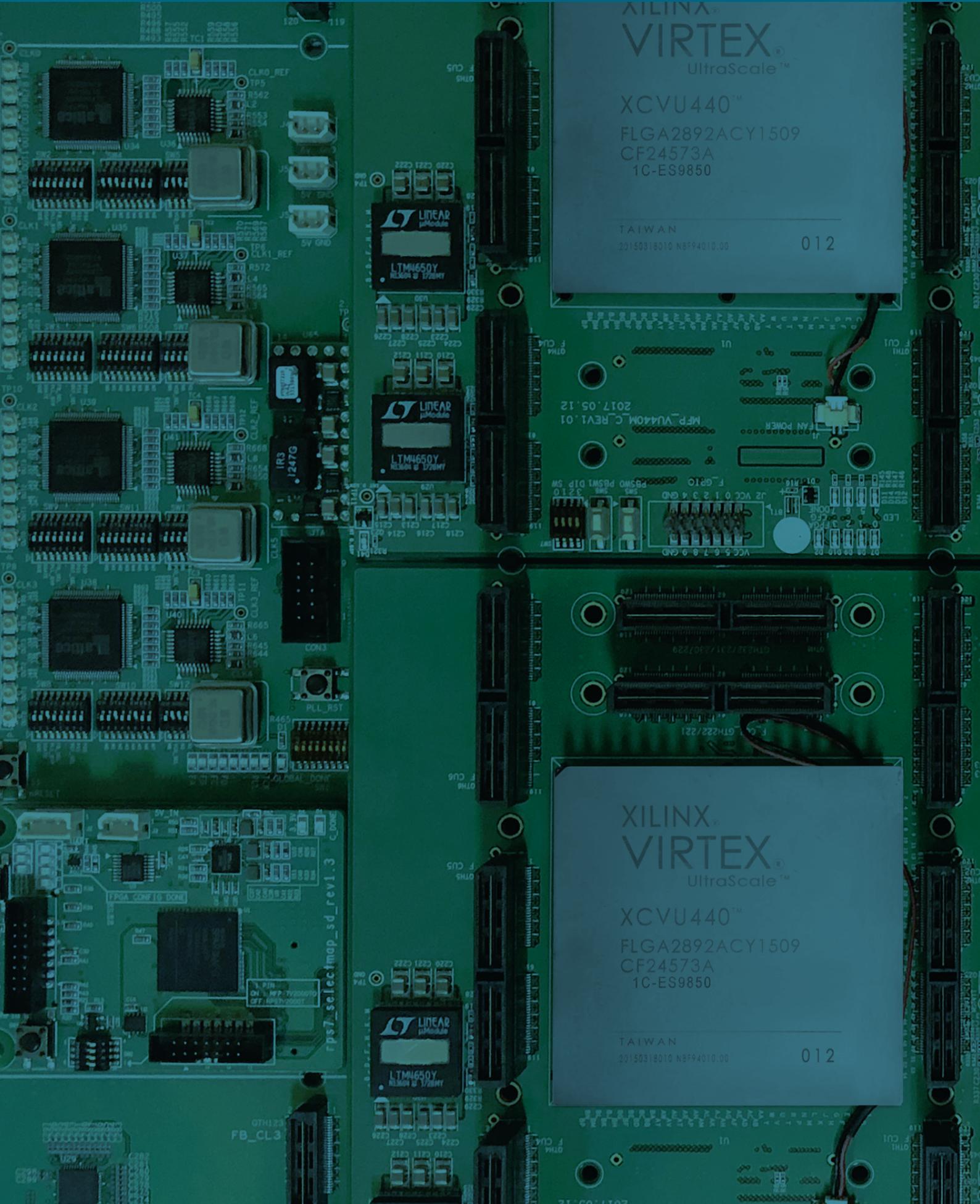


Features

- Provides a socket (8ea) to test multiple MMC/SD memory
- Provides large buffer memory (two DDR3 4GB)
- Provides PCIe for high-speed data transfer with hosts



FPGA/SoC Solution





HUINS has been successfully designing FPGA verification boards for SoC designs for over 30 years, including ARM Core technology, FPGA design technology, and CPU interface technology. We design FPGA boards in a fast turnaround time and have the know-how of ARM Core. We also have DDR4/DDR3, MIPI, HDMI, LPDDR3, eMMC, PCIe, USB interface, ADC/DAC, DSP, Test SW, Embedded Linux, UFS, M1P1, Vx1, RTOS design capabilities.

It is of utmost importance that SoC/FPGA verification boards operate reliably. In RTL design, FPGA behavioral uncertainty often causes engineers to spend a lot of time and fail to complete projects on time. HUINS has the best technology in FPGA efficient placement, CPU module and interface, Clock Scheme, PCB Pattern design, Impedance Matching, SMT, Testing SW, etc.



FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VP1902-S]

AMD Versal™ Premium VP1902 Adaptive SoC & ASIC Rapid Prototyping System



MFP-VP1902-S

- VERSAL PREMIUM XCVP1902 single FPGA Board
- XCVP1902-2MSEVSA6865 XILINX VERSAL FPGA Chip mount
- 18.5 Million system logic cells, total 2,000 I/O
- Dual ARM Cortex -A72 MPCore™, Dual ARM Cortex™-R5F
- DDR4 SODIMM x 2, Max. 3200MHz, 32GB x 2
- Peripherals: Giga Eth, USB, SD, QSPI, UART
- FMC+ x 8, QTH x 3, NVAF x 2, QSFP-DD x 2 Extension Connector
- GTYP 64 Lane(8 Lane 8ea), GTM 32 Lane(8 Lane 4ea)
- Clock Module (CLK 0~3) Clock Generator 6.25 ~ 400MHz
- Supports up to 8 individually adjustable Vccos
- Supports remote download and control of Power/Reset/Config via USB
- User Daughter Module Support

1. Introduction of item

MFP-VP1902-S is a high-end, large-capacity FPGA logic emulation and prototyping target equipped with one Versal Premium XCVP1902-2MSEVSA6865 and is Huins' unique concept product.

As ASIC and SoC design complexity increases rapidly due to the rapid evolution of AI and Machine Learning-based chips, extensive validation of silicon and software prior to tape-out is essential. To meet these requirements, Huins seeks to provide the best, most efficient boards with proven FPGA technology and know-how that are recognized as the best in the country.

The VP1902 has 2.2x more logic cells compared to the previous generation VU19P FPGA, reaching 18.5 million logic cells.

Delivering maximum capacity and connectivity with rammable logic density and 2.4x higher I/O bandwidth, the VP1902 adaptive SoC leverages a universal architecture including programmable network-on-chip to outperform previous generations. Delivers up to 8.5x faster debugging performance compared to VU19P FPGAs.

MFP-VP1902-S can be easily expanded with various functions through FMC+. Supports 3200MHz and 32GB memory.

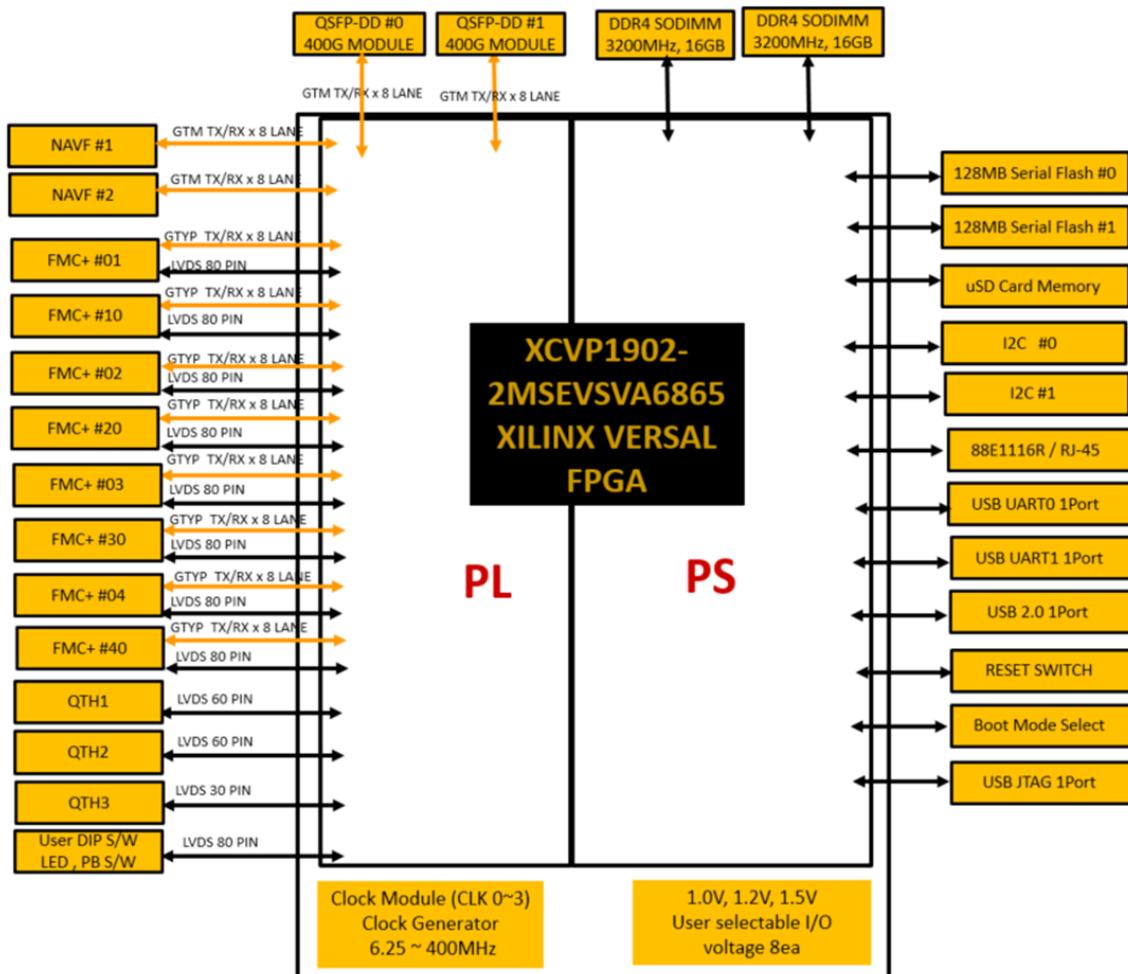
It is possible to manufacture and verify desired expansion modules such as PCIe Gen5, CSI, DSI, USB3.0, DDR4, Ethernet, HDMI, VX1, etc., and remote download and control of Power/Reset/Config control is possible through USB.

Low skew, high-speed clocks are distributed by the clock buffer. The clock can use the clock output of the board's 4 oscillators.

Virtex Ultrascale+ (XCVU19P-FSVA3824) Specification

APU	Dual-core Arm Cortex-A72; 48KB/32KB L1 Cache, ECC; 1MB L2 Cache		
RPU	Dual-core Arm Cortex-R5F; 32KB/32KB L1 Cache, TCM w/ECC		
Memory	256KB On-Chip Memory w/ECC		
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)		
System Logic Cells	18,506,880	NoC Master / Slave Ports	192
CLB Flip-Flops	16,920,576	DDR Bus Width	1,024
LUTs	8,460,288	DDR Memory Controllers	16
Distributed RAM (Mb)	258	PCIe (PLPCIE5)	16 x Gen5x4
Block RAM Blocks	6,808	100G Multirate Eth MAC	12
Block RAM (Mb)	239	600G Ethernet MAC	4
UltraRAM Blocks	2,200	XPIO / HDIO	2,328 / 88
UltraRAM (Mb)	619	GTYP (32.75Gb/s)	64
DSP Engines	6,864	GTM 58Gb/s (112Gb/s)	32

2. Block Diagram



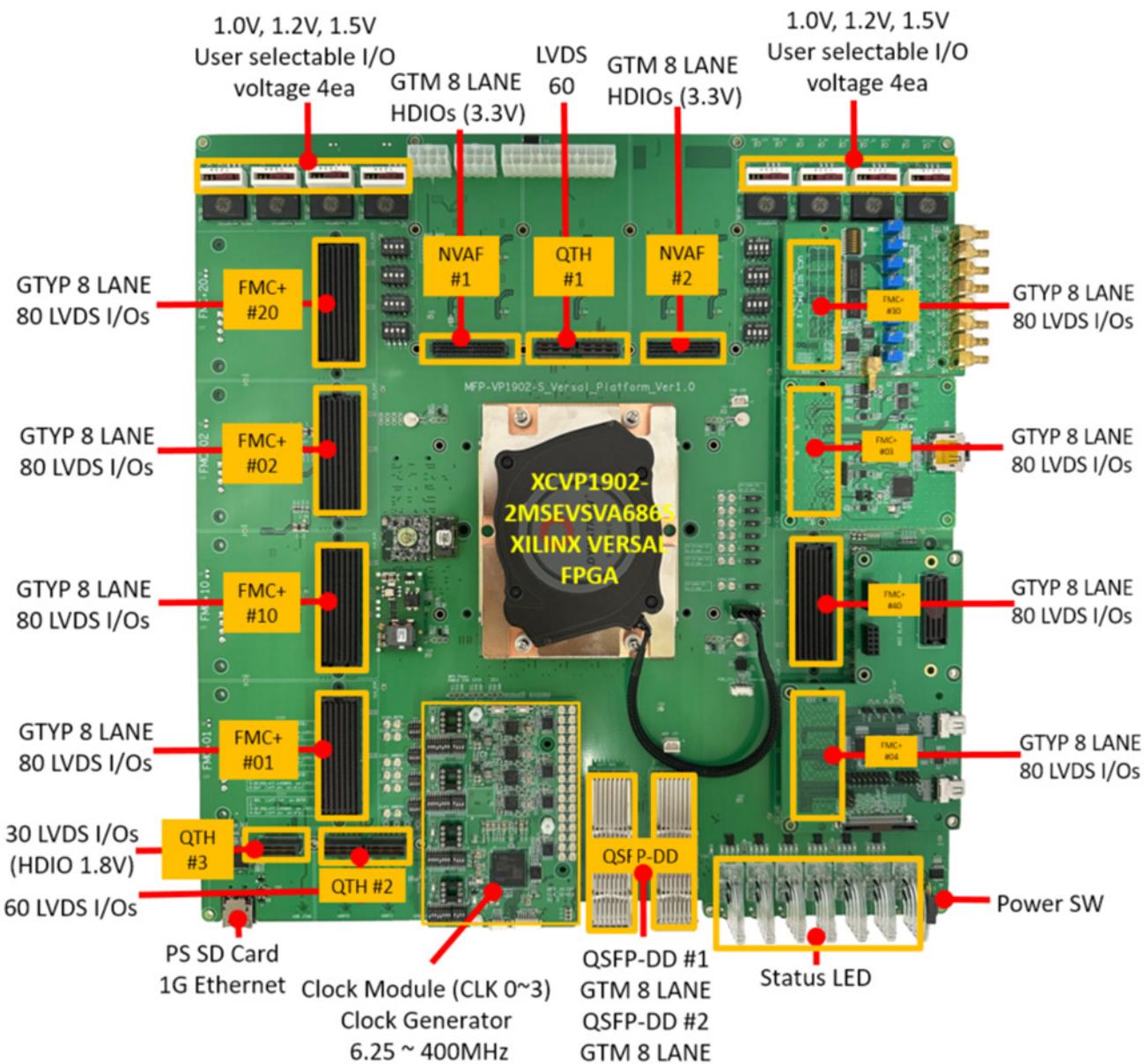


FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VP1902-S]

AMD Versal™ Premium VP1902 Adaptive SoC & ASIC Rapid Prototyping System

2. Block Diagram



3. Specifications

Item		Specification
FPGA	VERSAL PREMIUM XCVP1902-2MSEVSA6865	
MEMORY	SODIMM 2EA	DDR4 SODIMM x 2EA, Max. 3200MHz, 32GB x 2EA
	QSFP-DD "0"	GTM 8 LANE, 400G Optic Module
	QSFP-DD "1"	GTM 8 LANE, 400G Optic Module
	FMC+ "01"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	FMC+ "10"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	FMC+ "02"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	FMC+ "20"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	FMC+ "03"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
High-Speed I/O	FMC+ "30"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	FMC+ "04"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	FMC+ "40"	GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support
	NVAF "1"	GTM 8 LANE, HDIOs (3.3V)
	NVAF "2"	GTM 8 LANE, HDIOs (3.3V)
	QTH "1"	60 LVDS I/Os (XIO 1.5V)
	QTH "2"	60 LVDS I/Os (XIO 1.5V)
	QTH "3"	30 LVDS I/Os (HDIO 1.8V)
Peripheral	JTAG	USB JTAG 1Port, USB C-type
	UART	USB UART 2Port, USB C-type
	SD Card	SD 3.0 1Port, 32GB, uSD 3.0
	USB	USB 2.0 1Port, Host, USB C-type
	QSPI Flash Memory	QSPI Flash Memory 128GB x 2EA
	Gigabit Ethernet	10/100/1000 Base-TX 1Port, Modular Jack
	User SWs	DIP SW (4EA), Push Button SW (3EA)
	User LEDs	LEDs (12EA)
Clock	Global Clock	Clock Module (CLK 0~3) Clock Generator 6.25 ~ 400MHz
Connector I/O Power	Voltage Regulator	FMC+ #1, #2, #3, #4, #5, #6, #7, #8 : 1V, 1.2V, 1.5V select QTH #1, #2 : 1.5V #3 : 1.8V
Power	AXT Power 1500W	FMC+ #1, #2, #3, #4, #5, #6, #7, #8 : 1V, 1.2V, 1.5V select
FAN + Cooler	Cooler	24Pin ATX Power Connector 1ea 8Pin 12V Aux. Power Connector 2ea
Borad Size	PCB	355 mm (W) x 369 mm (D) x 3mm (T), 36Layer
Case	Case	374 mm (W) x 360 mm (D) x 153.6 mm (H)

Documents

User Manual

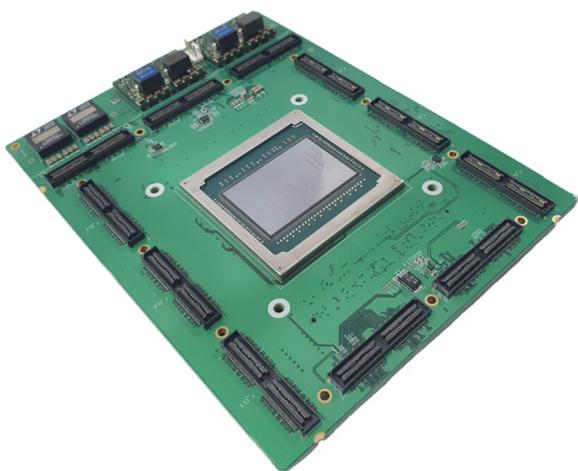
PinOut List, Schematics (in searchable .pdf format)



FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-M]

Virtex UltraScale+™ VU19P FPGA Module SoC and ASIC Rapid Prototyping System



MFP-VU19P-M

- Virtex UltraScale+™ VU19P FPGA Module
- XCVU19P-FSVA3824 Chip Mount Mounting
- 48 million Asic Gates, providing a total of 1,742 I/Os
- GTY 48 Lane Connector
- High Speed SAMTEC QTH Connector Expansion
- DDR4 SODIMM (Supports up to 32GB)
- Provides up to four individually adjustable voltages
- SELECTMAP Configuration, SD card from Baseboard
- MFP-Series Daughter Module Compatible
- MFP-VU19P-M cannot be used alone, must be combined with Baseboard



1. Introduction of item

The MFP-VU19PM is compatible with Single, Duo, and Quad Base boards

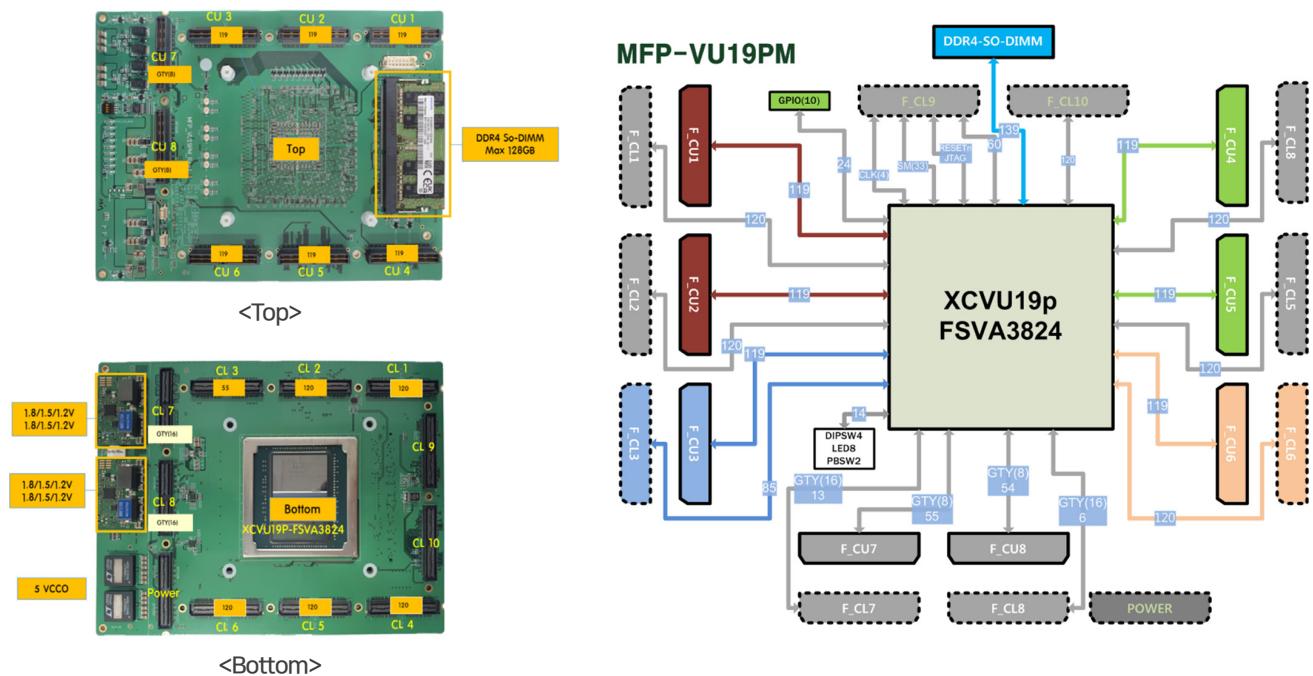
- The MFP-VU19P-M is an FPGA concept product from HUINS based on the VU19P Ultrascale+™ FPGA. When developing SoCs/ASICs, large capacity FPGAs are required to prototype as ASIC gate capacity increases.
- We provide the best, most efficient boards with proven FPGA technology and know-how that are recognized as the best in Korea and MFP-VU19P-S is 1.7 times larger in capacity than the previous XCVU440 and up to 30% faster than the previous XCVU440 to meet the highest demands in high-speed interface verification and test areas.
- Support FPGA gates (48 million Asic gates) for programming various applications and 8 connectors on top of Samtec High-speed QTH (823 I/Os, GTY16lane*2) on the upper side. QSH lower 10 connectors Lower side QSH (919 I/Os, GTY16lane*2) provides an easy and versatile functional expansion site.
- VU19P FPGAs are modularized, so depending on the Base Board build, you can get 1, 2, or 4 VU19P FPGA modules. Custom boards can be built with 8 or more modules, so scalability is not limited.

Virtex Ultrascale+ (XCVU19P-FSVA3824) Specification

Device Name	XCVU19P
System Logic Cells (K)	8,938
CLB Flip-Flops (K)	8,172
CLB LUTs (K)	4,086
Max. Dist. RAM (Mb)	58.4
Total Block RAM (Mb)	75.9
UltraRAM (Mb)	90.0

Device Name	XCVU19P
DSP Slices	3,840
Peak INT8 DSP (TOP/s)	10.4
PCIe Gen3 x16/Gen4 x8	8
Max. Single-Ended HP I/Os	1,976
Max. Single-Ended HD I/Os	96
GTY 32.75Gb/s Transceivers	80

2. Block Diagram



3. Product Specifications

Item	Specification
FPGA	XCVU19P-FSVA3824-1, Chip Mount
I/O	<p>MFP-Series Daughter Module Compatible</p> <p>DDR4 So-DIMM : 1ea, Max 32GB</p> <p>IO Connector</p> <ul style="list-style-type: none"> - Upper Side QTH(823 I/Os, GTY16lane) - 119 I/O Connector x 6 - GTY 8 lane and 54 I/O x 1 - GTY 8 lane and 55 I/O x 1 - Lower side QSH(919 I/Os, GTY16lane) - 120 I/O Connector x 7 - 60 I/O Connector x 1 - GTY 16 lane and 13 I/O x 1 - GTY 16 lane and 6 I/O x 1 <p>ETC IO</p> <ul style="list-style-type: none"> - LED 8ea - DIPSW : 4ea - PB SW : 2ea - Clock Out Connector : 8ea - GPIO Header(14pins) : 10 I/O 5 VCCO Region - CU1/2,CU4/5 : 1.8/1.5/1.2V - CU3L3,CU6L3 : 1.8/1.5/1.2V - ETC : 1.8V fixed
Base Interconnection	<p>Global Clock (8ea)</p> <ul style="list-style-type: none"> - LVDS or SE : 4 - SE : 4 <p>JTAG and RESET, Selectmap Bus</p>



FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-S]

Virtex UltraScale+™ VU19P FPGA with 1 SoC and ASIC Rapid Prototyping System



MFP-VU19P-S

- Consists of a Virtex UltraScale+™ VU19P FPGA module and Base Board
- XCVU19P-FSVA3824 Chip Mount or Socket Mounting
- 48 million Asic Gates, providing a total of 1,742 I/Os
- High Speed SAMTEC QTH Connector Expansion
- DDR4 SODIMM (Supports up to 32GB)
- SELECTMAP Configuration, SD card
- Clock 4 Differential Signals and 4 Single Ended Signals
- GTY 48 Lane Connector
- Provides up to four individually adjustable voltages
- Power/Reset/Config control by USB (Remote Bit file Download & Control)
- MFP-Series Daughter Module Compatible

1. Introduction of item

The MFP-VU19PM is compatible and available with Single, Duo, and Quad Base Boards.

- The MFP-19P-S is a HUINS-exclusive FPGA concept based on the VU19P Ultrascale+™ FPGA. We aim to provide the best technology boards that are efficient with proven FPGA technology and know-how recognized as the best in Korea. The MFP-VU19P-S (XCVU19P FPGA) has 1.7 times the capacity of the previous XCVU440 and can run up to 30% faster.
- It offers programming for a wide range of applications and a wide range of FPGA gates (48 million asic gates). The MFP-VU19PM (Xilinx Virtex UltraScale+™ 19P FPGA) is modularized to allow you to custom design and connect one, two, four or more VU19P FPGAs to your system, so scalability is not limited, and Samtec High-speed QTH connectors provide easy and versatile feature expansion sites via the top 8 bottom 10 connectors.
- The MFP-VU19P-S supports 72-bit ECC DDR4 SODIMM sockets up to 128 GB. You can create and verify the desired expansion modules such as PCIe, CSI, DSI, USB3.0, DDR4, Ethernet, HDMI, VX1, etc. and support remote download and control of power/reset/config control via USB. SelectMap Config Time 40Sec.(using SD card SelectMap) is provided.

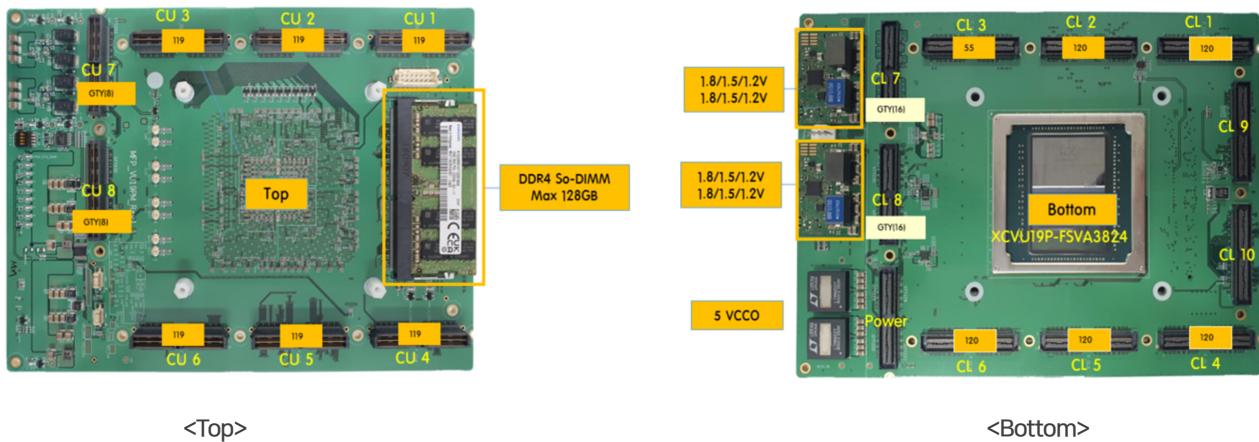
Virtex Ultrascale+ (XCVU19P-FSVA3824) Specification

Device Name	XCVU19P
System Logic Cells (K)	8,938
CLB Flip-Flops (K)	8,172
CLB LUTs (K)	4,086
Max. Dist. RAM (Mb)	58.4
Total Block RAM (Mb)	75.9
UltraRAM (Mb)	90.0

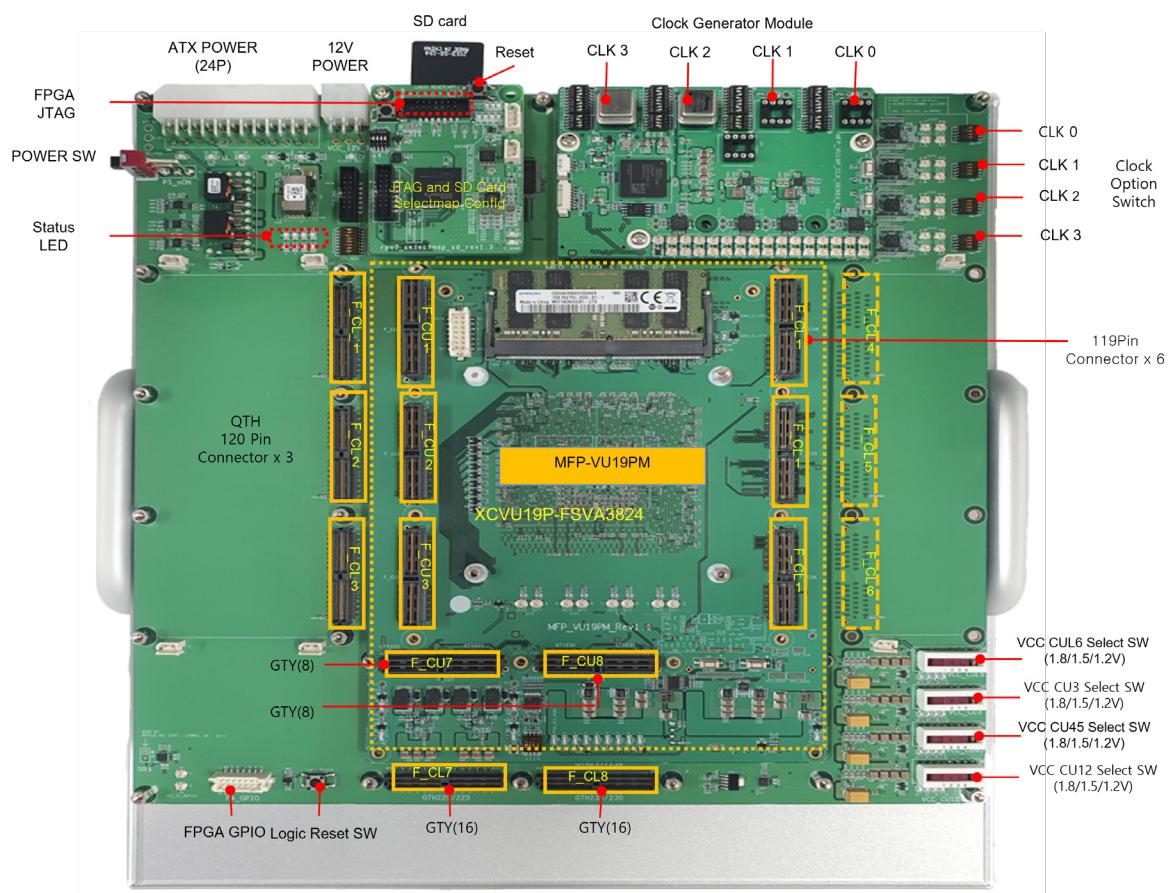
Device Name	XCVU19P
DSP Slices	3,840
Peak INT8 DSP (TOP/s)	10.4
PCIe Gen3 x16/Gen4 x8	8
Max. Single-Ended HP I/Os	1,976
Max. Single-Ended HD I/Os	96
GTY 32.75Gb/s Transceivers	80

2. Block Diagram

MFP-VU19PM (FPGA module)



MFP-VU19P-S (Base Board with 1 FPGA)



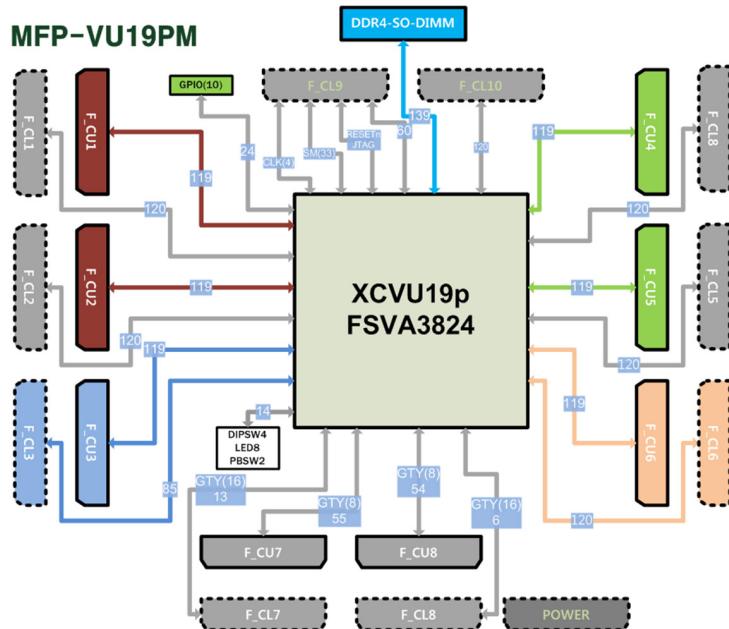


FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-S]

Virtex UltraScale+™ VU19P FPGA with 1 SoC and ASIC Rapid Prototyping System

2. Block diagram



3. Product Specifications

MFP-VU19PM (FPGA module)

Item	Specification
FPGA	XCVU19P-FSVA3824-1, Chip Mount
I/O	MFP-Series Daughter Module Compatible DDR4 So-DIMM : 1ea, Max 32GB IO Connector - Upper Side QTH (823 I/Os, GTY16lane) 119 I/O Connector x 6 GTY 8 lane and 54 I/O x 1 GTY 8 lane and 55 I/O x 1 - Lower side QSH (919 I/Os, GTY16lane) 120 I/O Connector x 7 60 I/O Connector x 1 GTY 16 lane and 13 I/O x 1 GTY 16 lane and 6 I/O x 1 ETC IO - LED 8ea - DIPSW : 4ea - PB SW : 2ea - Clock Out connector : 8ea - GPIO Header(14pins) : 10 I/O 5 VCCO region - CU1/2,CU4/5 : 1.8/1.5/1.2V - CU3L3,CU6L3 : 1.8/1.5/1.2V - ETC : 1.8V fixed
Base Interconnection	Global Clock (8ea) - LVDS or SE : 4 - SE : 4 JTAG and RESET, Selectmap Bus

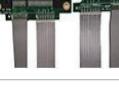
MFP-VU19P-S (Base Board with 1 FPGA)

Item	Specification
FPGA Connection	XCVU440-1FLG2892 1ea
8 Global Clock	LVDS or SE : 1~400MHz 4ea SE : 1~200MHz 4ea
JTAG and Selectmap Configuration	Config Time 40Sec.(using SD card SelectMap) Power/Reset/Config control by USB
Base Interconnect	120pin Connector x 7 85pin Connector x 2 10pin GPIO(1.8V) GTH 16 Lane Connector x 2
Power	Upper side 16 + 8 ch, Lower side 16 + 8 ch, Reference clock 125MHz default

Powered by Daughter Boards

Item	Specification	Comments (Q'ty)
DEBUG	Header Pin connector	2EA
Power	ATX Power supply	1EA

Option Module

Item	Specification	Comments	Item	Specification	Comments
Debug-Header	Pin Header connector 120 pins probe		USB3.0-FX3	Superspeed USB3.0 Peripheral & UART 1Port	
Debug-Mictor	MICTOR Connector 120 pins Probe		HDMI Tx	ADV7511 1080p Output	
DDR4 Module	Max 32GB 72bit ECC DDR4 SODIMM		HDMI Rx	ADV7611 1080p Input	
JTAG2-UART2	JTAG And UART ICE JTAG Port (20pins) 2 UARTs		PCIE-Adaptor	PCIe Adaptor PCIe Gen3 4Lanes	
PCIe Cable	PCIe Jumper Cable		Gigabit Phy / UART	Marvell 88E1111 Gigabit Ethernet Phy (GMII) 2UART ports	
High Speed Cable	120pin Interconnection		QTH to FMC Interconnector	OCuLink PCIe to PCI-Express cable - supplied by AURORA 4ch, 2Port	

Documents

- User Manual
- PinOut List, Schematics (in searchable .pdf format)

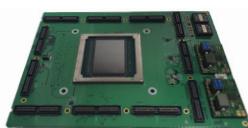
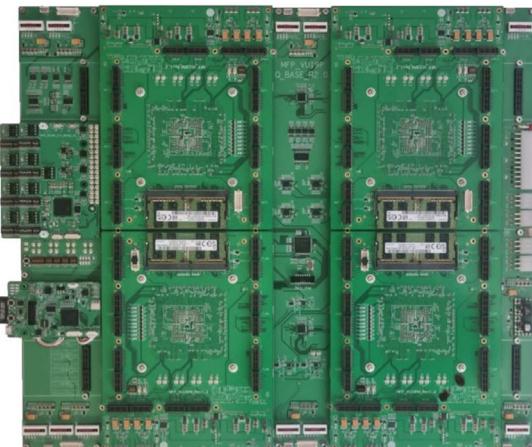


FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-Q]

Virtex UltraScale+™ VU19P FPGA with 4 SoC and ASIC Rapid Prototyping System

MFP-VU19P-Q



- Consists of four Virtex UltraScale+™ VU19P FPGA modules and board
- FPGA Module with Virtex UltraScale+™ XCVU19P-FSVA3824 Chip Mount or Socket
- 4 MFP-VU19M Module S-mountable Base Board
- Six 119pin Extension Connectors
- 48 million Asic Gates, providing a total of 1,742 I/O * 4
- High Speed SAMTEC QTH Connector Expansion
- DDR4 So-DIMM (Supports up to 32GB)
- FPGA JTAG & SelectMap Configuration SD Card
- Clock 4 Differential Signals and 4 Single Ended Signals, with 8ea Clock
- GTY 48 Lane Connector * 4
- Provides up to four individually adjustable voltages
- Power/Reset/Config control by USB (Remote Bit file Download & Control)
- MFP-Series Daughter Module Compatible

1. Introduction of item

The MFP-VU19PM is compatible and available with Single, Duo, and Quad Base Boards.

- The MFP-VU19P-Q is an XCVU19P Vertex Ultrascale+™ four-mount FPGA platform, which is an FPGA concept product from HUINS. We aim to provide the best technology boards that are efficient with proven FPGA technology and know-how recognized as the best in Korea. The XCVU19P FPGA has 1.7 times the capacity of the previous XCVU440 and up to 30% faster performance. The MFP-VU19P-Q offers programming for a variety of applications and a wide range of FPGA gates (48 million asic gates).
- MFP-VU19PM FPGAs are modularized, allowing you to custom design and connect one, two, four or more VU19P FPGAs to your system for unlimited scalability.
- The MFP-VU19P-M features Samtec High-speed QTH connectors on the top 8 and bottom 10 for easy and versatile expansion sites, and supports 72-bit ECC DDR4 SODIMM sockets up to 128GB.
- You can create and verify the desired expansion modules such as PCIe, CSI, DSI, USB3.0, DDR4, Ethernet, HDMI, VX1, etc. and support remote download and control of Power/Reset/Config control via USB. SelectMapConfigTime40Sec.(using SD card SelectMap) is provided.
- LowSkew, High-speed Clocks are distributed by Clock Buffer. The Clock is driven by the Oscillators on the BaseBoard. The baseboard 8 clock outputs are connected to the MFP-VU19PM module. Four MFP-VU19PMs can use eight clocks on the baseboard.

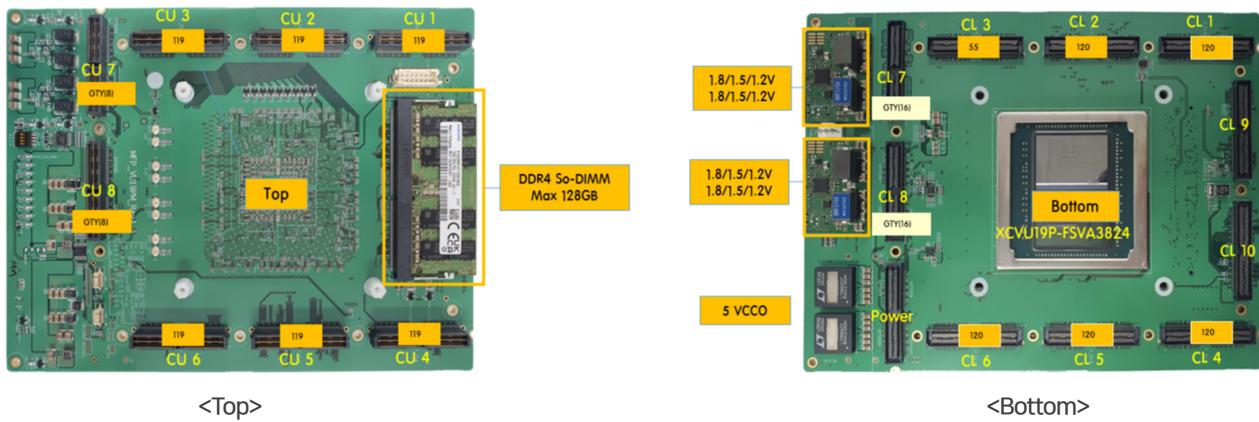
Virtex Ultrascale+ (XCVU19P-FSVA3824) Specification

Device Name	XCVU19P
System Logic Cells (K)	8,938
CLB Flip-Flops (K)	8,172
CLB LUTs (K)	4,086
Max. Dist. RAM (Mb)	58.4
Total Block RAM (Mb)	75.9
UltraRAM (Mb)	90.0

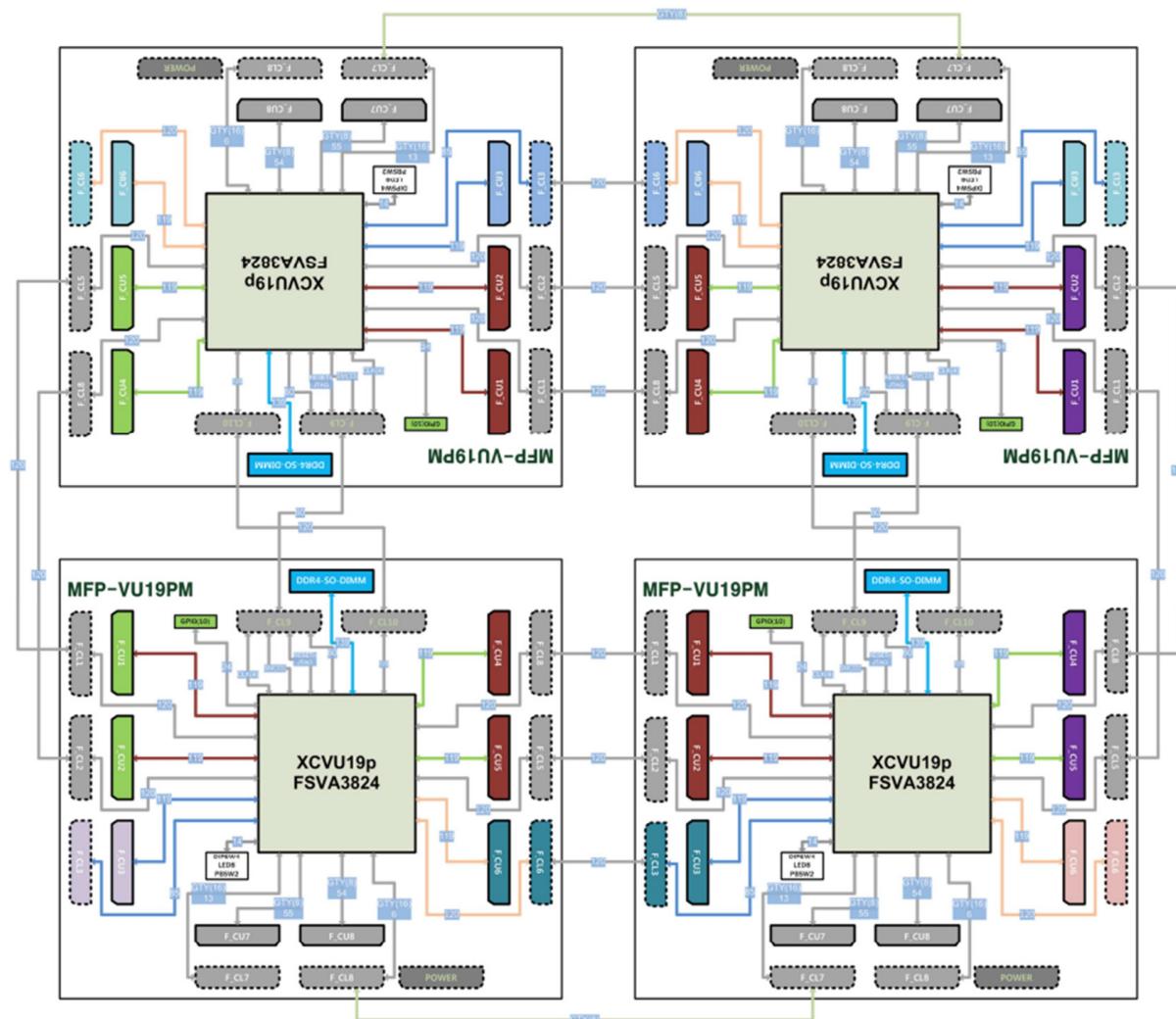
Device Name	XCVU19P
DSP Slices	3,840
Peak INT8 DSP (TOP/s)	10.4
PCIe Gen3 x16/Gen4 x8	8
Max. Single-Ended HP I/Os	1,976
Max. Single-Ended HD I/Os	96
GTY 32.75Gb/s Transceivers	80

2. Block diagram

MFP-VU19PM (FPGA module)



MFP-VU19P-Q (Base Board with 4 FPGA)





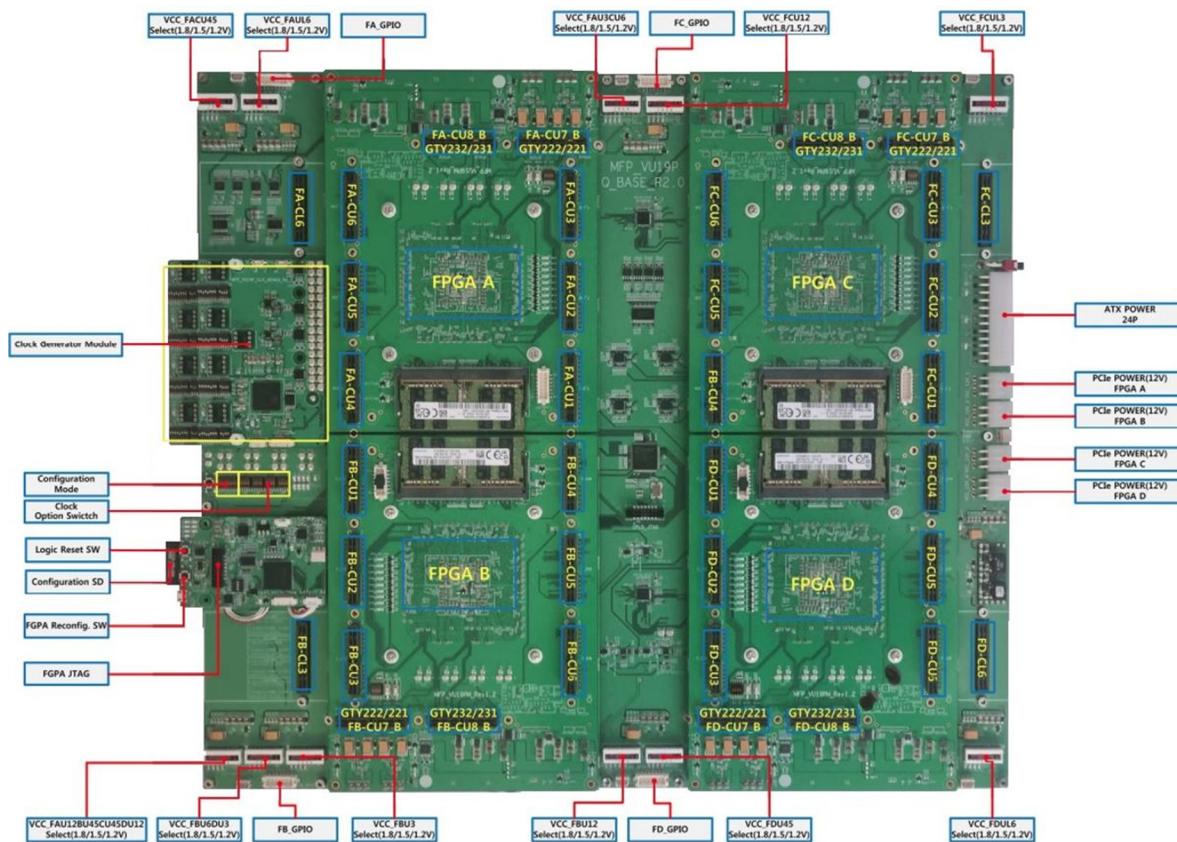
FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-Q]

Virtex UltraScale+™ VU19P FPGA with 4 SoC and ASIC Rapid Prototyping System

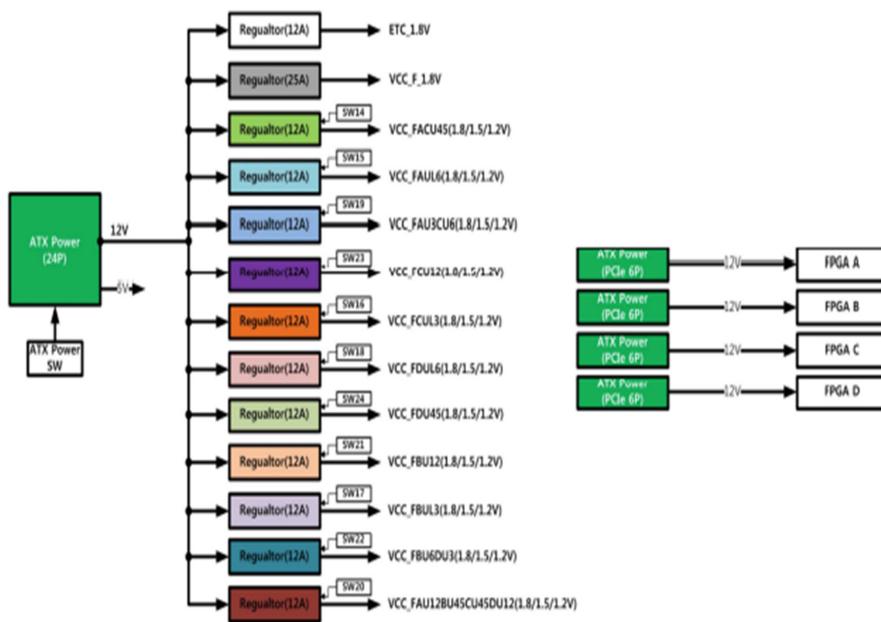
2. Block Diagram

MFP-VU19P-Q (Base Board with 4 FPGA)



Power

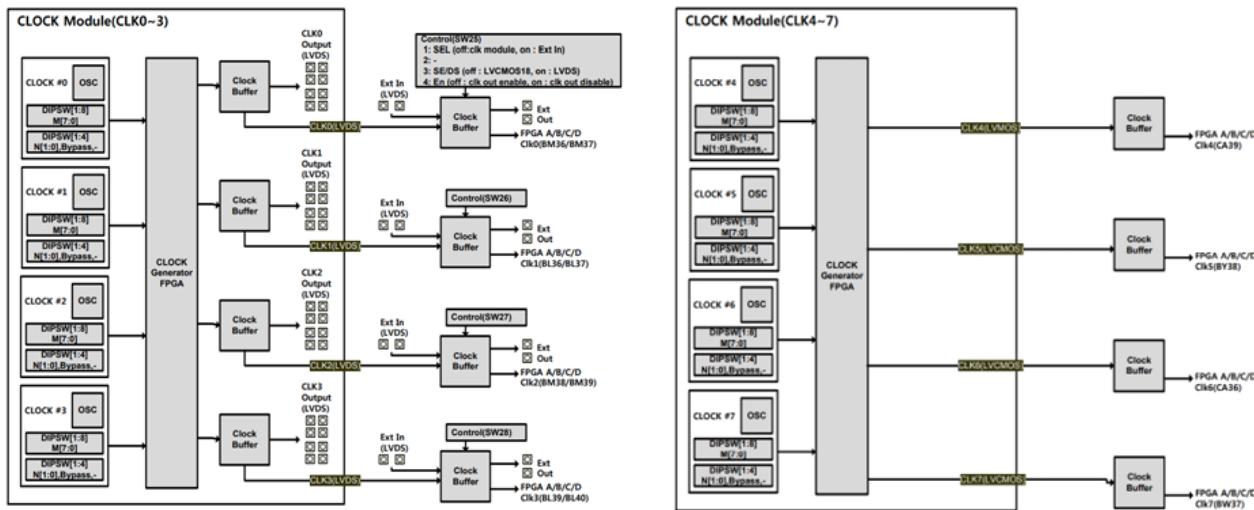
- The ATX Power Supply accepts +12V, 5V, and 12A inputs to power the board. The Voltage Regulator supplies all the voltages of 1.8/1.5/1.2V required by the FPGA.



Clock Structure (MFP-VU19P-Q Clock and JTAG)

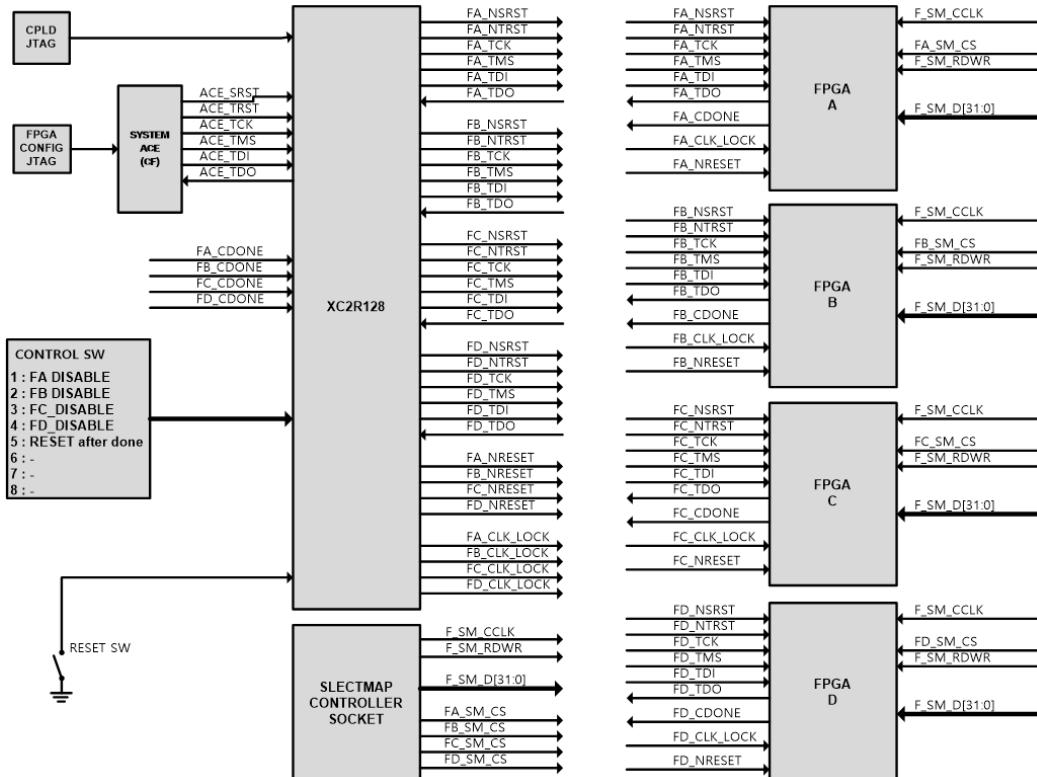
- The clock configuration consists of four clocks: CLK0, CLK1, CLK2, and CLK3.

Each of the clocks CLK0, CLK1, CLK2, and CLK3 are connected to the FPGA module, making four clocks (CLK0 through CLK3) available. There are an additional 4 clocks (CLK4, CLK5, CLK6, CLK7) for a total of 8 clocks available.



Configuration

- FPGA JTAG chain & Selecmap Configuration





FPGA/SoC

Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-Q]

Virtex UltraScale+™ VU19P FPGA with 4 SoC and ASIC Rapid Prototyping System

3. Product Specifications

MFP-VU19PM (FPGA module)

Item	Specification
FPGA	XCVU19P-FSVA3824-1, Chip Mount
I/O	MFP-Series Daughter Module Compatible DDR4 So-DIMM : 1ea, Max 32GB IO Connector - Upper Side QTH(823 I/Os, GTY16lane) 119 I/O Connector x 6 GTY 8 lane and 54 I/O x 1 GTY 8 lane and 55 I/O x 1 - Lower side QSH(919 I/Os, GTY16lane) 120 I/O Connector x 7 60 I/O Connector x 1 GTY 16 lane and 13 I/O x 1 GTY 16 lane and 6 I/O x 1 ETC IO - LED 8ea - DIPSW : 4ea - PB SW : 2ea - Clock Out connector : 8ea - GPIO Header(14pins) : 10 I/O 5 VCCO region - CU1/2,CU4/5 : 1.8/1.5/1.2V - CU3L3,CU6L3 : 1.8/1.5/1.2V - ETC : 1.8V fixed
Base Interconnection	Global Clock (8ea) - LVDS or SE : 4 - SE : 4 JTAG and RESET, Selectmap Bus

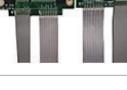
MFP-VU19P-Q (Base Board with 4 FPGA)

Item	Specification
FPGA Connection	4 MFP-VU19M module Site
8 Global Clock	LVDS or SE : 16~400MHz 4ea SE : 1~200MHz 4ea
JTAG and Selectmap Configuration	Config Time 40Sec.(using SD card SelectMap) Power/Reset/Config control by USB
Base Interconnect	4 SelectIO(119) extension connectors 4 GPIO(10) extension connectors 12 GTY(8) extension connectors
Power	ATX Power supply

Powered by Daughter Boards

Item	Specification	Comments (Q'ty)
DEBUG	MICTOR connector	1EA
DEBUG	Header Pin connector	2EA
Power	AC220V / 30A or higher	1EA
Hi-Speed Cable	HQCD-060-15.75-STR-SBL-1 (400mm)	2EA

Option Module

Item	Specification	Comments	Item	Specification	Comments
Debug-Header	Pin Header connector 120 pins probe		USB3.0-FX3	Superspeed USB3.0 Peripheral & UART 1Port	
Debug-Mictor	MICTOR Connector 120 pins Probe		HDMI Tx	ADV7511 1080p Output	
DDR4 Module	Max 32GB 72bit ECC DDR4 SODIMM		HDMI Rx	ADV7611 1080p Input	
JTAG2-UART2	JTAG And UART ICE JTAG Port (20pins) 2 UARTs		PCIE-Adaptor	PCIe Adaptor PCIe Gen3 4Lanes	
PCIe Cable	PCIe Jumper Cable		Gigabit Phy / UART	Marvell 88E1111 Gigabit Ethernet Phy (GMII) 2UART ports	
High Speed Cable	120pin Interconnection		QTH to FMC Interconnector	OCuLink PCIe to PCI-Express cable - supplied by AURORA 4ch, 2Port	

Documents

- User Manual
- PinOutList, Schematics (in searchable .pdf format)



MFP-VU19P-SF (FMC Type)

- Consists of a Virtex UltraScale+™ VU19P FPGA module and Base Board
 - XCVU19P-FSVA3824 Chip Mount
 - 48 million Asic Gates, providing a total of 1,742 I/Os
 - FMC+ HSPC, FMC Connector Extensions
 - FMC Connector x 4 HA24, HB 22, LA34, DP :
FMC1/3/4 (GTY 12Lane) FMC2 (GTY 4Lane)
 - DDR4 So-DIMM (Supports Max 32GB) * 6CH
 - Clock 4 Differential Signals and 4 Single Ended Signals
 - Provides up to four individually adjustable voltages
 - SelectMap Configuration, SD Card
 - Power/Reset/Config control by USB
(Remote Bit File Download & Control)

1. Introduction of item

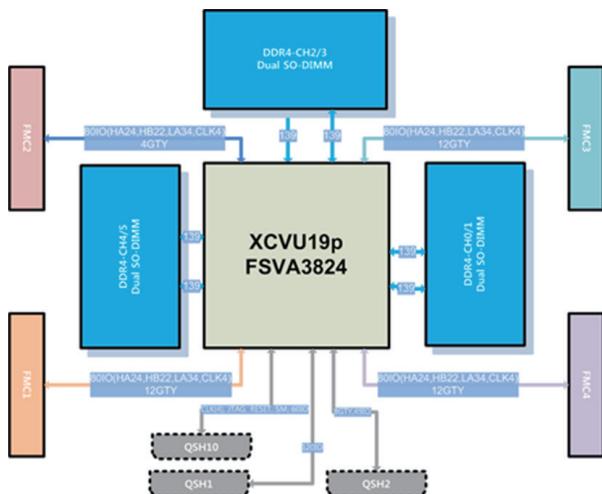
- The MFP-VU19P-SF is an FMC expansion IO connector based on the VU19P Ultrascale+™ FPGA, which is a concept product of HUINS' proprietary FPGA platform. We aim to provide the best technology boards that are efficient with proven FPGA technology and know-how recognized as the best in Korea. The MFP-VU19P-S (XCVU19P FPGA) has 1.7 times the capacity of the previous XCVU440 and can run up to 30% faster.
 - It offers programming for a wide range of applications and a wide range of FPGA gates (48 million asic gates). MFP-VU19P-SF (Xilinx Virtex UltraScale+™ 19P FPGA) is modularized so that one, two, four or more VU19P FPGAs can be custom designed and connected to the customer's system, so scalability is not limited, and it provides easy and diverse functional expansion sites through FMC+ as IO expansion, FMC Connector x4 HA24, HB 22, LA34, DP : FMC1/3/4(GTY 12Lane) FMC2(GTY 4Lane).
 - The MFP-VU19P-SF supports six 72-bit, dual-rank sockets up to 128GB. You can create and verify the desired expansion modules such as PCIe, CSI, DSI, USB3.0, DDR4, Ethernet, HDMI, VX1, etc. and support remote download and control of power/reset/config control via USB. SelectMap Config Time 40Sec.(using SD card SelectMap) is provided.

Verilog Examples for Virtex Ultrascale+ (XCVU19P-FSVA3824) Specification

Device Name	XCVU19P
System Logic Cells (K)	8,938
CLB Flip-Flops (K)	8,172
CLB LUTs (K)	4,086
Max. Dist. RAM (Mb)	58.4
Total Block RAM (Mb)	75.9
UltraRAM (Mb)	90.0

Device Name	XCVU19P
DSP Slices	3,840
Peak INT8 DSP (TOP/s)	10.4
PCIe Gen3 x16/Gen4 x8	8
Max. Single-Ended HP I/Os	1,976
Max. Single-Ended HD I/Os	96
GTY 32.75Gb/s Transceivers	80

2. Block Diagram



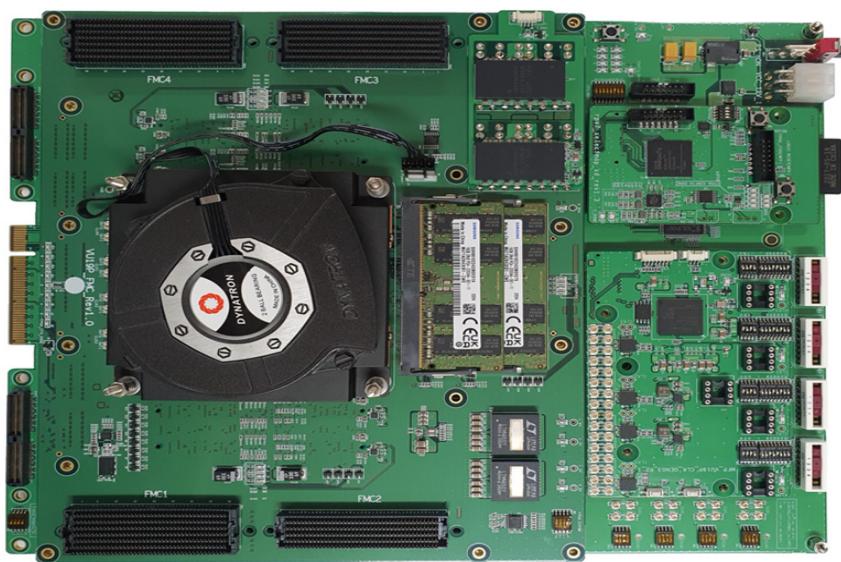
VU19P_FMC FPGA Module



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FPGA/SoC

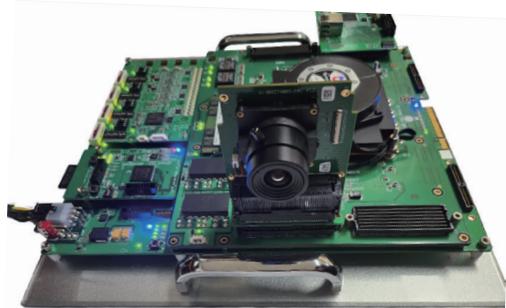
Virtex Ultra Scale VU19P-Based SoC Design Verification Platform [MFP-VU19P-SF]

Virtex UltraScale+™ VU19P FPGA 1x SoC and ASIC Rapid Prototyping System

3. Product Specifications

MFP-VU19PM_FMC (FPGA Module)

Item	Specification
FPGA	XCVU19P-FSVA3824-1
I/O	<ul style="list-style-type: none"> - FMC+ HSPC Compatible - DP12ch Support (FMC1/3/4) - DDR4 So-DIMM : 6ch (bit, Dual rank support) - FMC Connector x 4 HA24(48x2), HB 22(44x2), LA34(68x2) - DP : FMC1/3/4(GTY 12Lane), FMC2(GTY 4Lane) - 5 VCCO Region VCC_FMC1/2/3/4 : 1.8/1.5/1.2V ETC 1.8V - 10 GPIO Header - LED 8ea, DIPSW 4ea, PBSW 2ea
Base Interconnection	<ul style="list-style-type: none"> Clock - LVDS or SE : 4 - JTAG and RESET, Selectmap Bus - Base Interconnect : 180 IO - PCIe Gen3 8Lane



Option Module

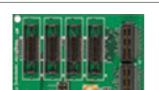
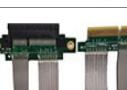
Item	Specification	Comments
FMC_FX3	USB30-FX3 - Superspeed USB 3.0 Peripheral HDMI Tx - ADV7511 1080p Output UART - Micro USB port	

Documents

- User Manual
- Pin Out List, Schematics (in searchable .pdf format)



1. I/O Peripherals for MFP-VU19P-Q

Item	Specification	Comments	Item	Specification	Comments
Interconnect 1x1	CON 1x1 Stackable Height		HDMI Tx	ADV7511 1080p Output	
Interconnect 1x2	CON 1x2 Vertical Interconnection		HDMI Rx	ADV7611 1080p Input	
MFP-De-bug-Header	Pin Header connector 120pins probe		PCIE-Adaptor	PCIe Adaptor PCIe Gen3 4Lanes	
MFP-De-bug-Mictor	MICTOR connector 120pins probe		PCIe Cable	PCIe Jumper Cable	
DDR4 Module	Max 32GB 72bit ECC DDR4 SODIMM		High Speed Cable	120pin Interconnection	
JTAG2-UART2	JTAG And UART ICE JTAG Port (20pins) 2 UARTs		Gigabit Phy / UART	Marvell 88E1111 Gigabit Ethernet Phy (GMII) 2UART Ports	
USB3.0-FX3	Superspeed USB3.0 Peripheral & UART 1Port		QTH to FMC Interconnector	OCuLink PCIe to PCI-Express cable - supplied by AURORA 4ch, 2Port	



FPGA/SoC

Virtex Ultra Scale VU9P-Based SoC Design Verification Platform [RPS-VU9P]

NVIDIA Jetson & FPGA Integration, Vision, and Deep Learning Edge Platforms



RPS-VU9P

- Xilinx Virtex UltraScale+™ XCVU9P FPGA
- NVIDIA Jetson AGX Xavier
- 2 GB of Dual 2x 64bit Wide DDR4 Memory to FPGA
- HDMI RX, MIPI, GSML – Camera Interface
- FMC QTH Expansion Connector

1. Introduction of item

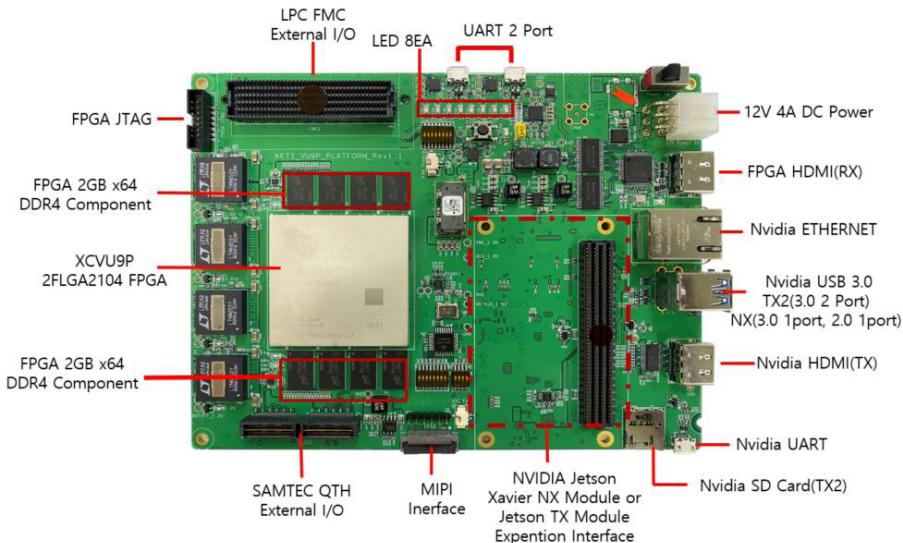
- The RPS-VU9P Platform powered by Virtex UltraScale+ combines Virtex UltraScale+ VU9P FPGAs with Nvidia Xavier NX to create the ideal visionary AI edge verification platform..
- The RPS-VU9P Platform features a reconfigurable Xilinx UltraScale+ XCVU9P-2FLGA2104 FPGA with 6,840 DSP slices and 2,586 logic cells, 2 GB DDR4 buffer memory (dual 2x 32-bit), MIPI, HDMI RX, PCIe Gen3, FMC, and QTH interfaces. The FPGA is connected to the Jetson Xavier NX via PCIe x4 lanes at Gen3 speeds.
- The NVIDIA Jetson Xavier NX is an embedded system-on-module (SoM) that includes an integrated 384-core Volta GPU with Tensor cores, Dual Deep Learning Accelerators (DLAs), and a 6-Core NVIDIA Carmel ARMv8.2 CPU.
- 8GB 128-bit LPDDR4x, 51.2GB/s memory bandwidth, hardware video codec, PCIe Gen 3/4, MIPI CSI-2 Camera lane, and USB 3.1 make it ideal for edge computing for computer vision and deep learning. Jetson Xavier NX supports Linux.

Virtex Ultrascale+ (XCVU9P-2FLGA2104) Specification

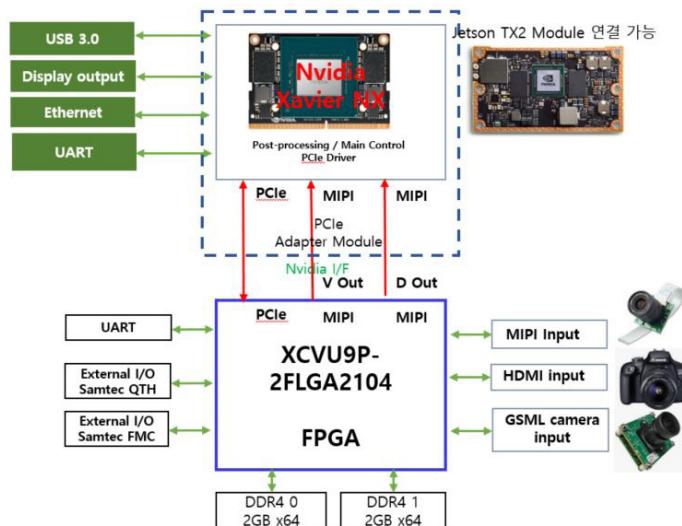
Device Name	XCVU9P
System Logic Cells (K)	2,586
CLB Flip-Flops (K)	2,364
CLB LUTs (K)	1,182
Max. Dist. RAM (Mb)	36.1
Total Block RAM (Mb)	75.9
UltraRAM (Mb)	270

Device Name	XCVU9P
Clock Management Tiles (CMTs)	30
DSP Slices	6,840
PCIe Gen3 x16 / Gen4 x8	6
150G Interlaken	9
100G Ethernet w/ RS-FEC	9

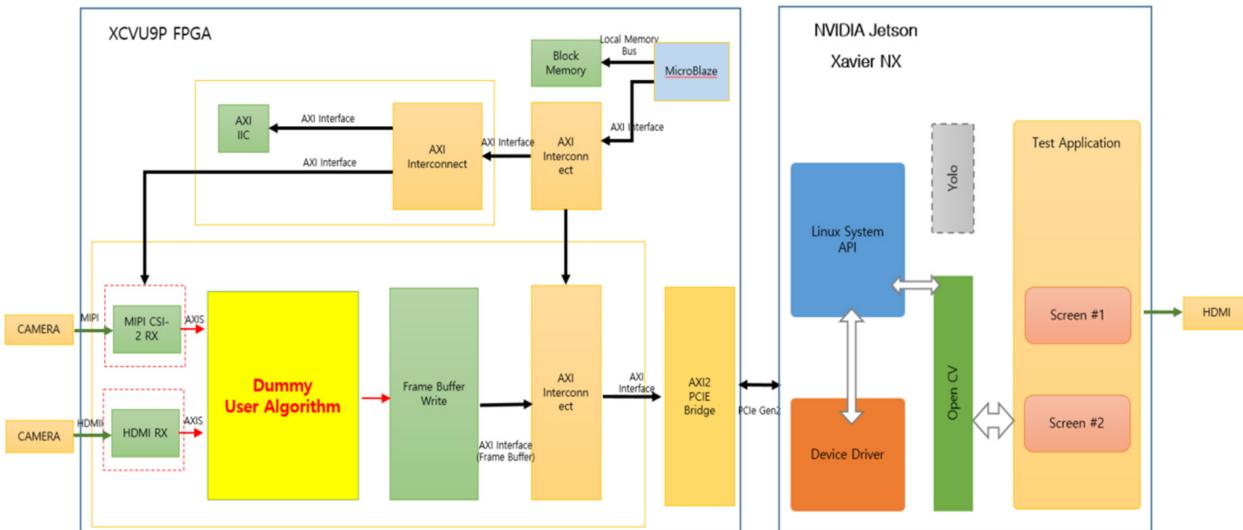
2. Configuration Diagrams



Block Diagram



Example RTL logic





FPGA/SoC

Virtex Ultra Scale VU9P-Based SoC Design Verification Platform [RPS-VU9P]

NVIDIA Jetson & FPGA Integration, Vision, and Deep Learning Edge Platforms

3. Mounting Images

Device Name	XCVU9P	Device Name	XCVU9P
VU9P FPGA Base Board		VU9P FPGA Platform + PCIe Module	
Jecton TX2 Module + VU9P FPGA Platform		1VU9P FPGA Platform + Xavier NX Adapter Module	
Jecton Xavier NX Module + VU9P FPGA Platform		PCIe Module / Xavier NX Adapter Module	

4. Product Specifications

RPS-VU9P Platform

- Xilinx Virtex UltraScale+ XCVU9P-2FLGA2104 FPGA in B2104 package
- x4 PCI Express (TX2 Gen2, NX Gen3)
- DDR4 Component (2GB x64 2ch)
- VITA 57.1 FMC Interface
- QTH 1Port (120EA io)
- USB to UART 2 Port
- HDMI inputs Interface
- GSML Camera Interface
- SPIx8 Flash for configuration
- FPGA Jtag port for configuration and debugging
- x8 LED
- x1 Push Button
- Programmable oscillators & clock generators
- 12V/8A Power
- Nvidia Jetson Xavier NX Interface
 - 1x micro-SD card slot
 - x16 PCI Express Gen 3
 - MIPI Interface
 - HDMI outputs
 - USB3.0 2Port
 - 1x GbE RJ-45
 - 1x UART
- * Jetson Xavier NX Adapter Module (Option)

Jetson Xavier NX Module / Jetson TX2 Module Specification (Option)

- Jetson Xavier NX System-on-Module (SOM)
 - 384-Core Volta GPU
 - 6-Core ARM 64 Bit CPU
 - 8 GB LPDDR4
 - 16 GB eMMC
 - Mechanical: 45 mm x 69.6 mm, 260-pin SO-DI MM connector
- NVIDIA JETSON TX2 4GB MODULE
 - 256-core Pascal GPU
 - Dual-core NVIDIA Denver 2
 - Quad-core ARM A57 complex
 - ARM A57 Complex
 - 4 GB 128 Bit LPDDR4 | 25.6 GB/s
 - 16 GB eMMC 5.1

Documents

- User Manual
- Pin Out List, Schematics (in searchable .pdf format)



FPGA/SoC

MPSOC Ultrascale+ XCZU9EG-based Design Verification Platform [RPS-ZUP9]

Platform for AI, automotive, industrial, video, and telecom applications



RPS-ZUP9

- XCZU9EG-2FFVB1156I, DDR4 16GB, QSPI FLASH 1GB
- Ethernet, I²C, SD, SPI, UART, USB OTG
- Utilize PL / PS interface to develop various applications
- PetaLinux Support

1. Introduction of item

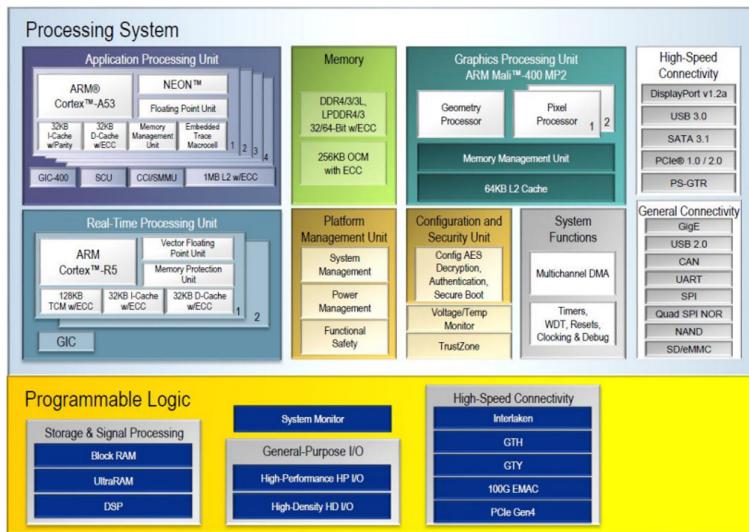
- The RPS-ZUP9 is a ZYNQ development verification platform applicable to high-speed data processing, data storage, video transmission, deep learning, artificial intelligence, and industrial control, suitable for engineers, students, and new project customization.
- The RPS-ZUP9 platform is a small MP SoC Zynq platform that uses the Xilinx MPSOC XCZU9EG-2FFVB1156I and is developed as a single board convenient for users to use standalone and expand via FMC for board-to-board use.
- It consists of a dual-core ARM Cortex-A53 and FPGA programmable logic integrated single chip using Processing System (PS) + Programmable Logic(PL)technology.
- 16GB of high-speed DDR4 SDRAM and 1Gb QSPI FLASH are designed into the PL area for abundant memory, supporting PCIe, USB 3.0, Gigabit Ethernet, Display Port, UART, SD card slot, and FMC HPC interface.

Zynq UltraScale+ XCZU9EG-2FFVB1156 MPSOC Specification

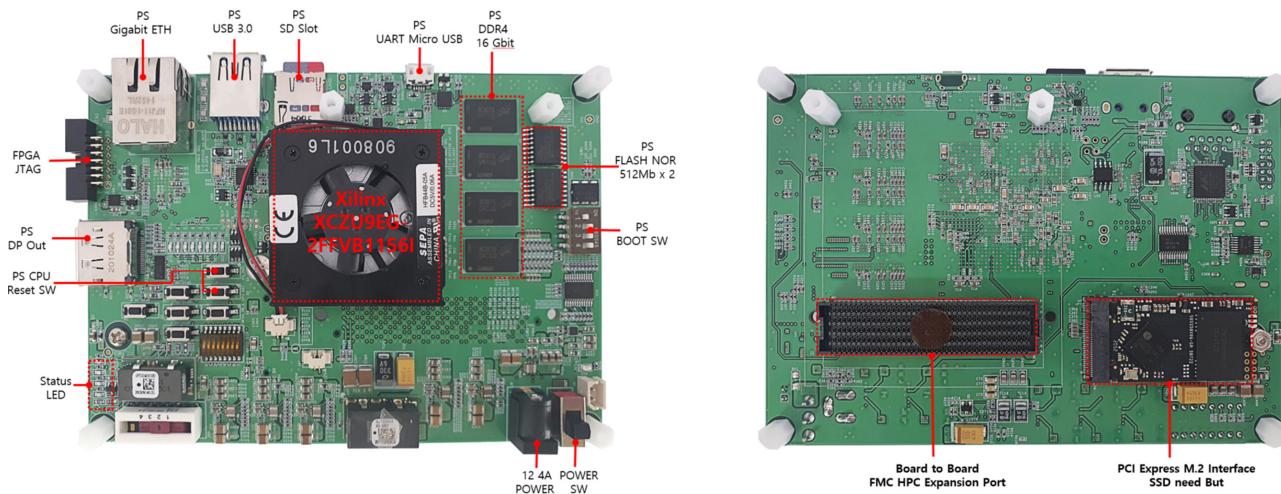
Device Name	XCVU9P	Device Name	XCVU9P
System Logic Cells (K)	600	Primary Attributes	Zynq UltraScale+™ FPGA, 599K+ Logic Cells
Memory (Mb)	32.1	Peripherals	DMA, WDT
DSP Slices	2,520	Number of I/O	328
Maximum I/O Pins	328	MCU RAM	256KB
Speed	600MHz, 1.5GHz	Core Processor	Quad ARM Cortex -A53 MPCore™ with CoreSight™, Dual ARM Cortex™-R5 with CoreSight
Series	Zynq UltraScale+™ MPSOC EG	Connectivity	CAN, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/ USART, USB OTG

2. Block Diagram

ZYNQ ZU9EG Block Diagram



RPS-ZUP9 Block Diagram



3. Product Specifications

Device Name	XCVU9P
FPGA	XCZU9EG 2FFVB11561 Speed Grades -1 Logic Cells 5600K, CLB Flip-Flops 548K
Core Processor	4x ARM Cortex-A53, 1.33GHz, Dual-Core Cortex RS, S3IMH, Mali™400 MP2
Flash NOR	512Mb x 2
SD Memory	Micro SD Socket
DDR Memory	DDR4, 16GBit, 6Abit, 2400Mbps
UART	UART Micro USB 1 Port
USB	USB 3.0 1 Port

Device Name	XCVU9P
ETH	Gigabit Ethernet 1 Port
Display Port	Display port 1 port
PCI Express	SATA M.2 Interface(SSD)
FMC	LA 68pin, clk 8pin, DP(GTH) 10 lane
ETC	DIPSW 8, LED 8, PBSW 6
JTAG	FPGA JTAG 1 port
Power	12V, 4A



FPGA/SoC

Xilinx Zynq UltraScale+ MPSoC-based Design Verification Platform [RPS-ZUP4]

Cortex-A53 dual-core and Cortex-R5 dual-core



RPS-ZUP4

- Platform for automotive, industrial, video, and telecom applications
- Quad ARM Cortex-A53, Dual Cortex-R5 Realtime processor
- Based on 16nm FinFET + Programmable Logic Fabric
- Mali-400 MP2 graphics processing unit
- Utilize PL / PS interface to develop various applications

VIVADO

1. Introduction of item

Zynq UltraScale+ MPSoC Platform Features

- The RPS-ZUP4 ZYNQ UltraScale+ platform consists of a Core module and a Base board, and the Core module can be expanded to the Base and the high-capacity VU440 FPGA board with a Samtec connector to be applied as a CPU module. It can also be used as a standalone host module.
- I/O expansions include MIO 50 pins, SMGTP 4 ports, PL-HD IO 96 pins, PL-HPIO 146 pins, and PL-GTH 4 ports.

Applications

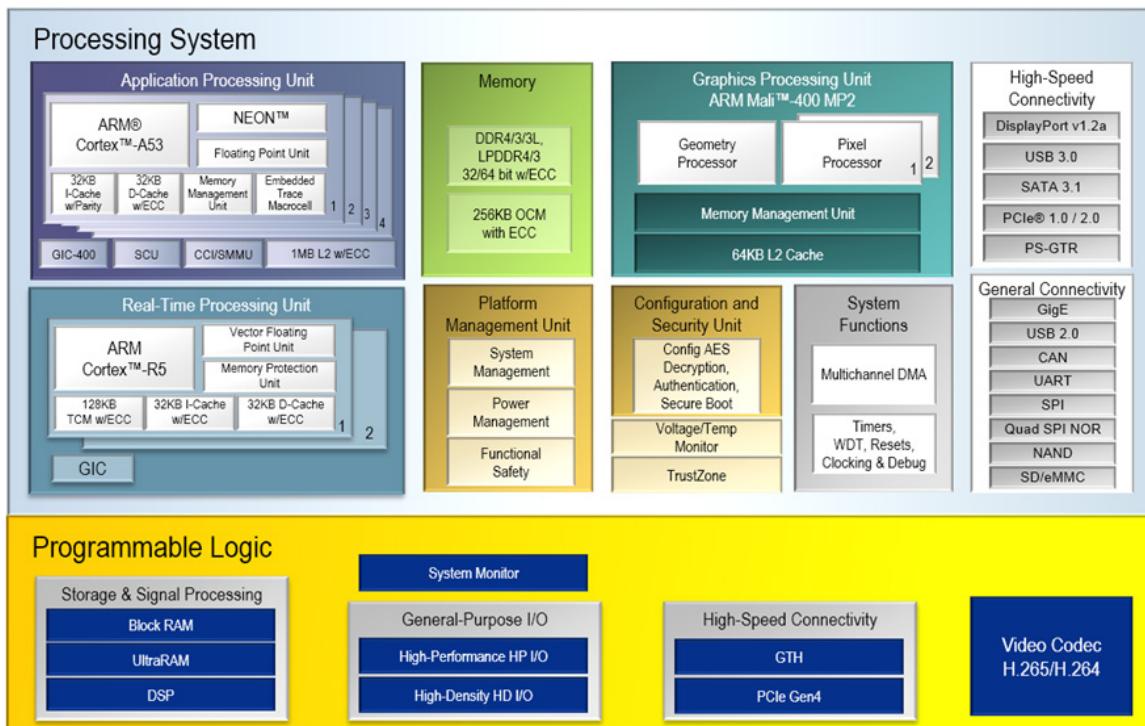
- | | | |
|---|-------------------------------------|--|
| • Motion control | • Solid State Drives (SSDs) | • Baseband L1 Acceleration |
| • Public safety and military mobile radio systems | • 8x8 100 MHz TD-LTE Remote RF Unit | • Camera-based advanced driver assistance systems (ADAS) |
| • Broadcast Video Camera | | |

Zynq UltraScale+ Supported Devices Specifications

Item	Specification		
Series	XCUZ4EV-SFVC784	XCUZ5EV- SFVC784	XCUZ5CG-SFVC784
Core Processor	Quad ARM Cortex -A53 MPCore™ with CoreSight™, Dual ARM Cortex™-R5 with CoreSight™		
MCU RAM	256KB		
Peripherals	DMA, WDT		
Connectivity	CAN, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG		
Speed	600MHz, 1.5GHz		
Primary Attributes	FPGA, 192K+ Logic Cells	FPGA, 256K+ Logic Cells	FPGA, 256K+ Logic Cells
Package / Case	784-BBGA, FCBGA		
Supplier Device Package	784-FCBGA (23x23)		
Number of I/O	252		

2. Block Diagram

Zynq UltraScale + EV Device Block Diagram

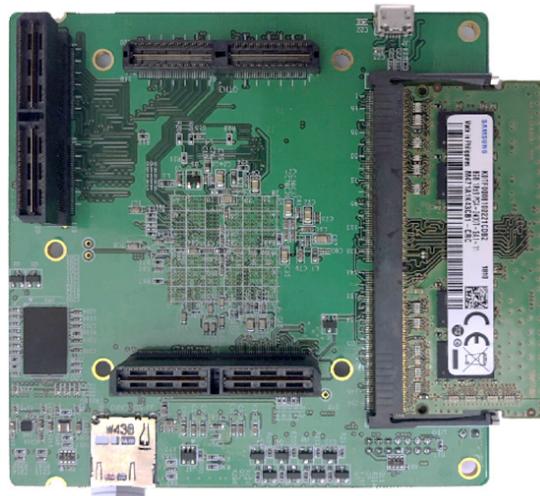


RPS-ZUP4 Block Diagram

- RPS-ZUP4 Core



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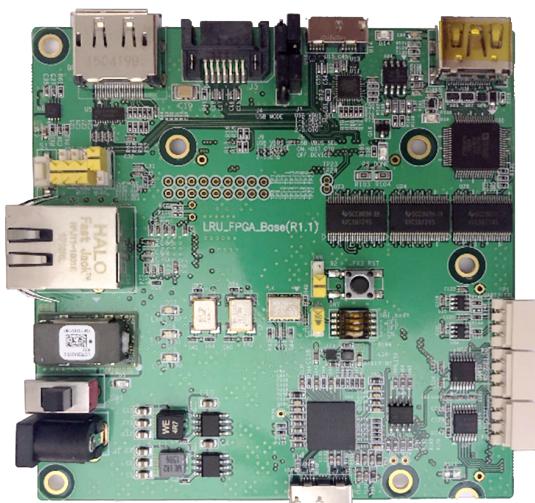
FPGA/SoC

Xilinx Zynq UltraScale+ MPSoC-based Design Verification Platform [RPS-ZUP4]

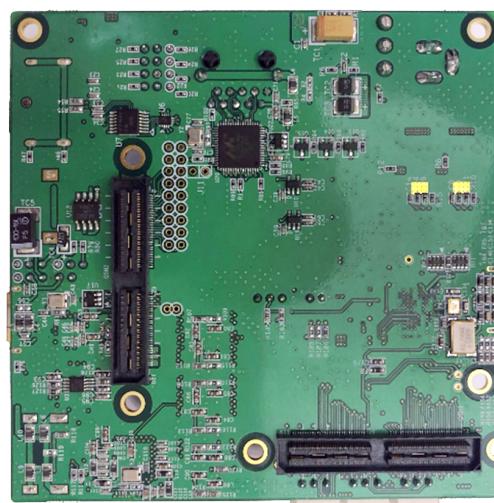
Cortex-A53 dual-core and Cortex-R5 dual-core

RPS-ZUP4 Block Diagram

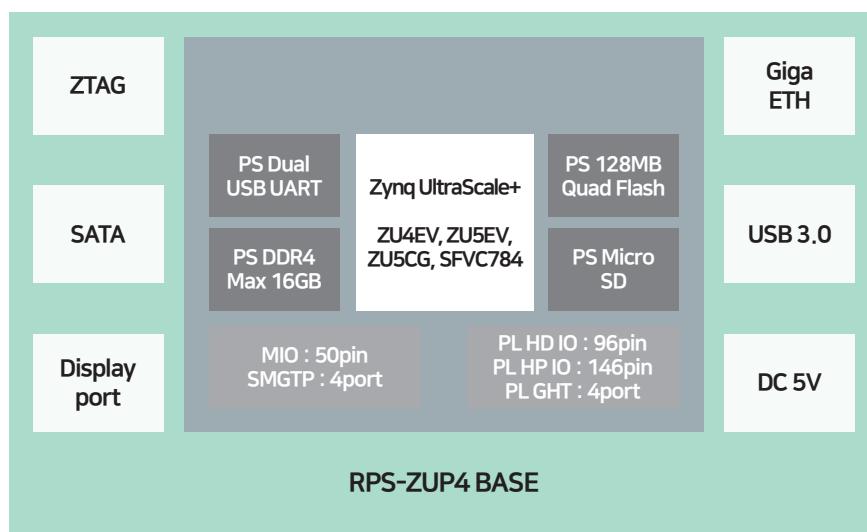
- RPS-ZUP4 BASE



<Top>



<Bottom>



3. Hardware Specifications

RPS-ZUP4 Core

Item	Specification
FPGA	XCZU4EV-SFVC784 / XCZU5EV-SFVC784 / XCZU5CG-SFVC784
Core Processor	Quad ARM Cortex -A53 MPCore™ with CoreSight™, Dual ARM Cortex™-R5 with CoreSight™, 600MHz, 1.5GHz
Flash Memor	128MB Quad Flash
SD Memory	Micro SD socket
DDR Memory	DDR4 SO-DIMM Socket(max 16GB)
USB	Dual USB UART
MIO	50pin
SMGTP	4port
PL-HD IO	96pin
PL-HP IO	146pin
PL-GTH	4port

RPS-ZUP4 Base

Item	Specification
JTAG	1 Port
UART	3 Port
SATA	1 Port
Display port	1 Port
HDMI	1 Port
USB 3.0	1 Port
GETH	1 Port
Power	DC 5V, 2A

Partners





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[LAB] 55, Magokjungang 8-ro 3-gil, Gangseo-gu, Seoul, Republic of Korea | **Lab.** +82-2-3663-8201

The specifications and appearance of the products listed in this catalog are subject to change without prior notice to improve quality.

