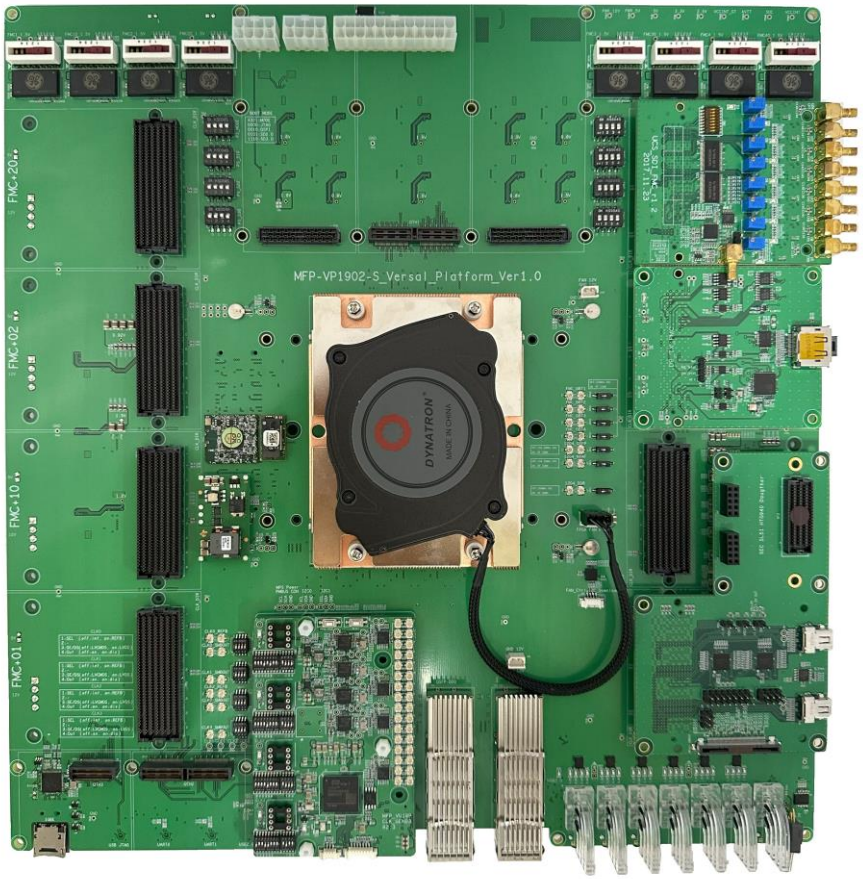
# MFP-VP1902-S

AMD Versal™ Premium VP1902 Adaptive SoC & ASIC Rapid Prototyping System




- VERSAL PREMIUM XCVP1902 single FPGA Board
- XCVP1902-2MSEVSVA6865 XILINX VERSAL FPGA Chip mount
- 18.5 Million system logic cells, total 2,000 I/O
- Dual ARM® Cortex®-A72 MPCore™, Dual ARM® Cortex™-R5F
- DDR4 SODIMM x 2, Max. 3200MHz, 32GB x 2
- Peripherals: Giga Eth, USB, SD, QSPI, UART
- FMC+ x 8, QTH x 3, NVAF x 2, QSFP-DD x 2 Extension Connector
- GTYP 64 Lane(8 Lane 8ea), GTM 32 Lane(8 Lane 4ea)
- Clock Module (CLK 0~3) Clock Generator 6.25 ~ 400MHz
- Supports up to 8 individually adjustable Vccos
- Supports remote download and control of Power/Reset/Config via USB
- User Daughter Module Support

■ MFP-VP1902-S is a high-end, large-capacity FPGA logic emulation and prototyping target equipped with one Versal Premium XCVP1902-2MSEVSVA6865 and is Huins' unique concept product.

As ASIC and SoC design complexity increases rapidly due to the rapid evolution of AI and Machine Learning-based chips, extensive validation of silicon and software prior to tape-out is essential. To meet these requirements, Huins seeks to provide the best, most efficient boards with proven FPGA technology and know-how that are recognized as the best in the country.

The VP1902 has 2.2x more logic cells compared to the previous generation VU19P FPGA, reaching 18.5 million logic cells.

Delivering maximum capacity and connectivity with rammable logic density and 2.4x higher I/O bandwidth, the VP1902 adaptive SoC leverages a universal architecture including programmable network-on-chip to outperform previous generations. Delivers up to 8.5x faster debugging performance compared to VU19P FPGAs.

MFP-VP1902-S can be easily expanded with various functions through FMC+ Supports 3200MHz and 32GB memory.

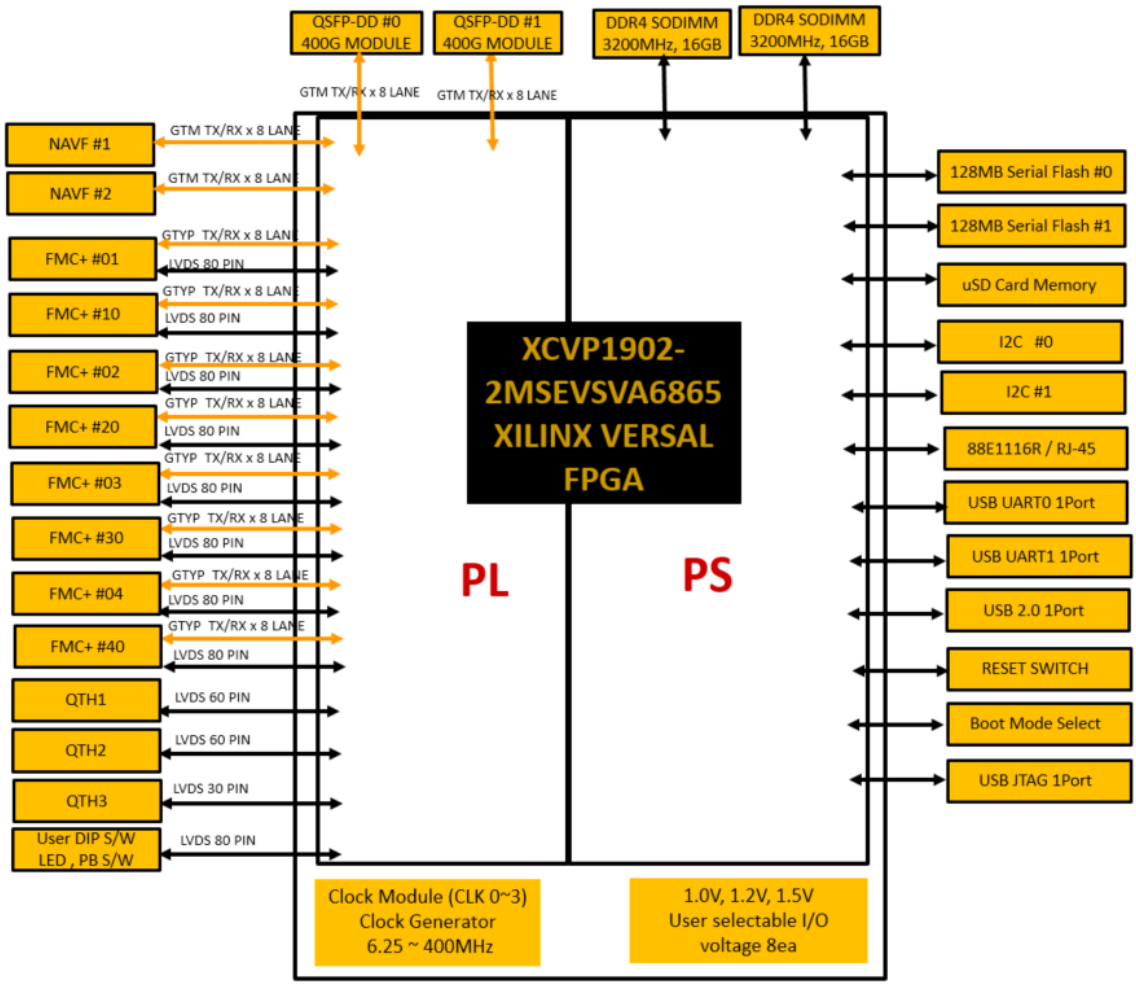
It is possible to manufacture and verify desired expansion modules such as PCIe Gen5, CSI, DSI, USB3.0, DDR4, Ethernet, HDMI, VX1, etc., and remote download and control of Power/Reset/Config control is possible through USB.

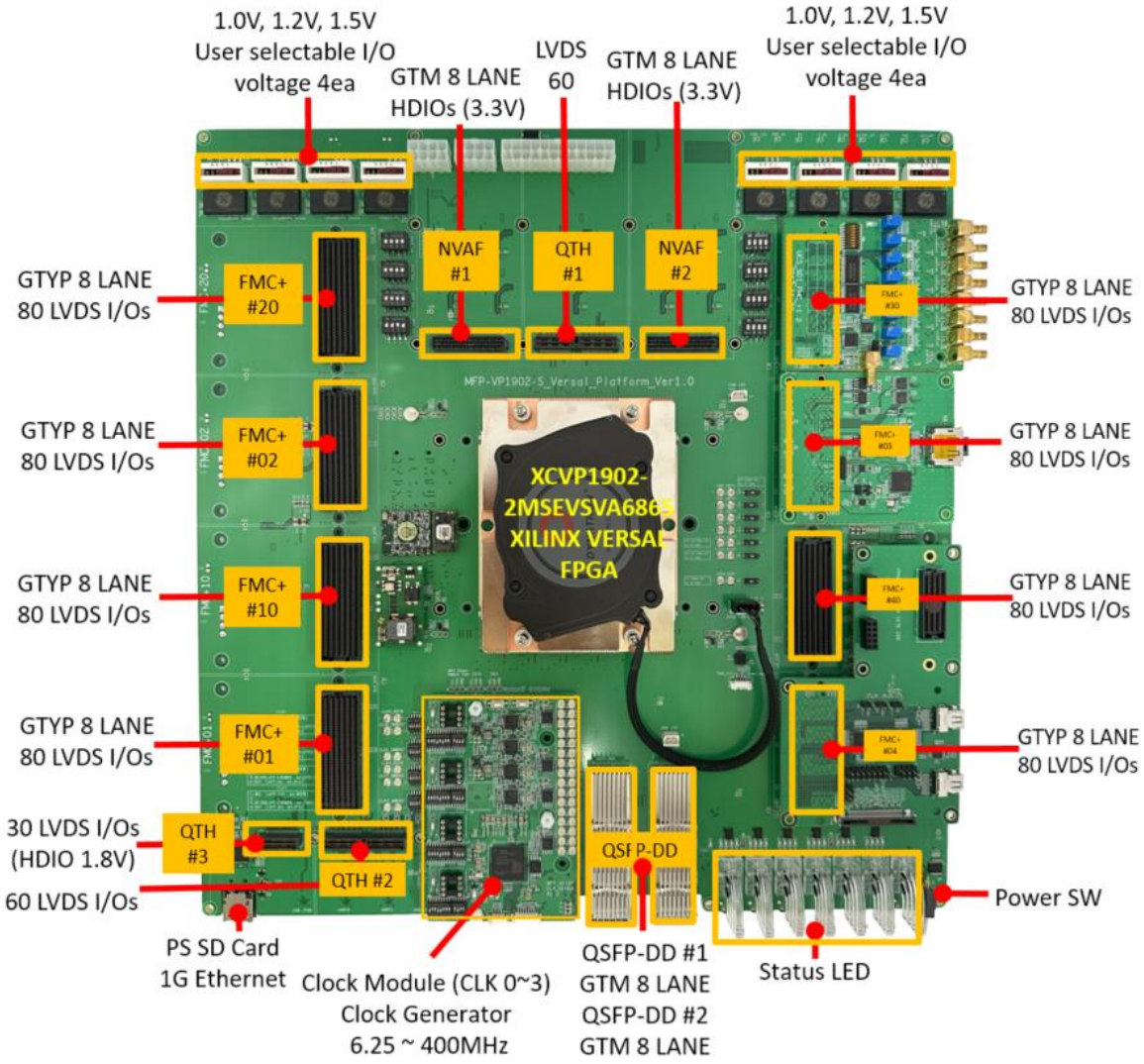
Low skew, high-speed clocks are distributed by the clock buffer. The clock can use the clock output of the board's 4 oscillators.

### XCVP1902 - XILINX VERSAL FPGA Summary

| | | | |
|---|---|---|---|
| APU | Dual-core Arm Cortex-A72; 48KB/32KB L1 Cache, ECC; 1MB L2 Cache | | |
| RPU | Dual-core Arm Cortex-R5F; 32KB/32KB L1 Cache, TCM w/ECC | | |
| Memory | 256KB On-Chip Memory w/ECC | | |
| Connectivity | Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2) | | |
| System Logic Cells | 18,506,880 | NoC Master / Slave Ports | 192 |
| CLB Flip-Flops | 16,920,576 | DDR Bus Width | 1,024 |
| LUTs | 8,460,288 | DDR Memory Controllers | 16 |
| Distributed RAM (Mb) | 258 | PCIe (PLPCIE5) | 16 x Gen5x4 |
| Block RAM Blocks | 6,808 | 100G Multirate Eth MAC | 12 |
| Block RAM (Mb) | 239 | 600G Ethernet MAC | 4 |
| UltraRAM Blocks | 2,200 | XPIO / HDIO | 2,328 / 88 |
| UltraRAM (Mb) | 619 | GTYP (32.75Gb/s) | 64 |
| DSP Engines | 6,864 | GTM 58Gb/s (112Gb/s) | 32 |

## Block diagram






## Specification

| Item | | Specification |
|---|---|---|
| FPGA | VERSAL PREMIUM XCVP1902-2MSEVSVA6865 | |
| MEMORY | SODIMM 2EA | DDR4 SODIMM x 2EA, Max. 3200MHz, 32GB x 2EA |
| High-Speed I/O | QSFP-DD “0” | GTM 8 LANE, 400G Optic Module |
| | QSFP-DD “1” | GTM 8 LANE, 400G Optic Module |
| | FMC+ “01” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | FMC+ “10” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | FMC+ “02” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | FMC+ “20” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |

| | | |
|---|---|---|
| | FMC+ “03” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | FMC+ “30” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | FMC+ “04” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | FMC+ “40” | GTYP 8 LANE + 80 LVDS I/Os (XIO 1.5V), PCIE GEN5 Support |
| | NVAF “1” | GTM 8 LANE, HDIOs (3.3V) |
| | NVAF “2” | GTM 8 LANE, HDIOs (3.3V) |
| | QTH “1” | 60 LVDS I/Os (XIO 1.5V) |
| | QTH “2” | 60 LVDS I/Os (XIO 1.5V) |
| | QTH “3” | 30 LVDS I/Os (HDIO 1.8V) |
| Peripheral | JTAG | USB JTAG 1Port, USB C-type |
| | UART | USB UART 2Port, USB C-type |
| | SD Card | SD 3.0 1Port, 32GB, uSD 3.0 |
| | USB | USB 2.0 1Port, Host, USB C-type |
| | QSPI Flash Memory | QSPI Flash Memory 128GB x 2EA |
| | Gigabit Ethernet | 10/100/1000 Base-TX 1Port, Modular Jack |
| | User SWs | DIP SW (4EA), Push Button SW (3EA) |
| | User LEDs | LEDs (12EA) |
| Clock | Global Clock | Clock Module (CLK 0~3)<br>Clock Generator 6.25 ~ 400MHz |
| Connector I/O Power | Voltage Regulator | FMC+ #1, #2, #3, #4, #5, #6, #7, #8 : 1V, 1.2V, 1.5V select<br>QTH #1, #2 :1.5V #3 : 1.8V |
| Power | AXT Power 1500W | 24Pin ATX Power Connector 1ea<br>8Pin 12V Aux. Power Connector 2ea |
| FAN + Cooler | Cooler | FPGA : Active Air Cooler, Case : FAN 4ea |
| Borad Size | PCB | 355 mm (W) x 369 mm (D) x 3mm (T), 36Layer |
| Case | Case | 374 mm (W) x 360 mm (D) x 153.6 mm (H) |

## Documents

- User Manual
- Pin Out List, Schematics (in searchable .pdf format)