FMC to 2* SSD NVME Module

FH1402

User Manual

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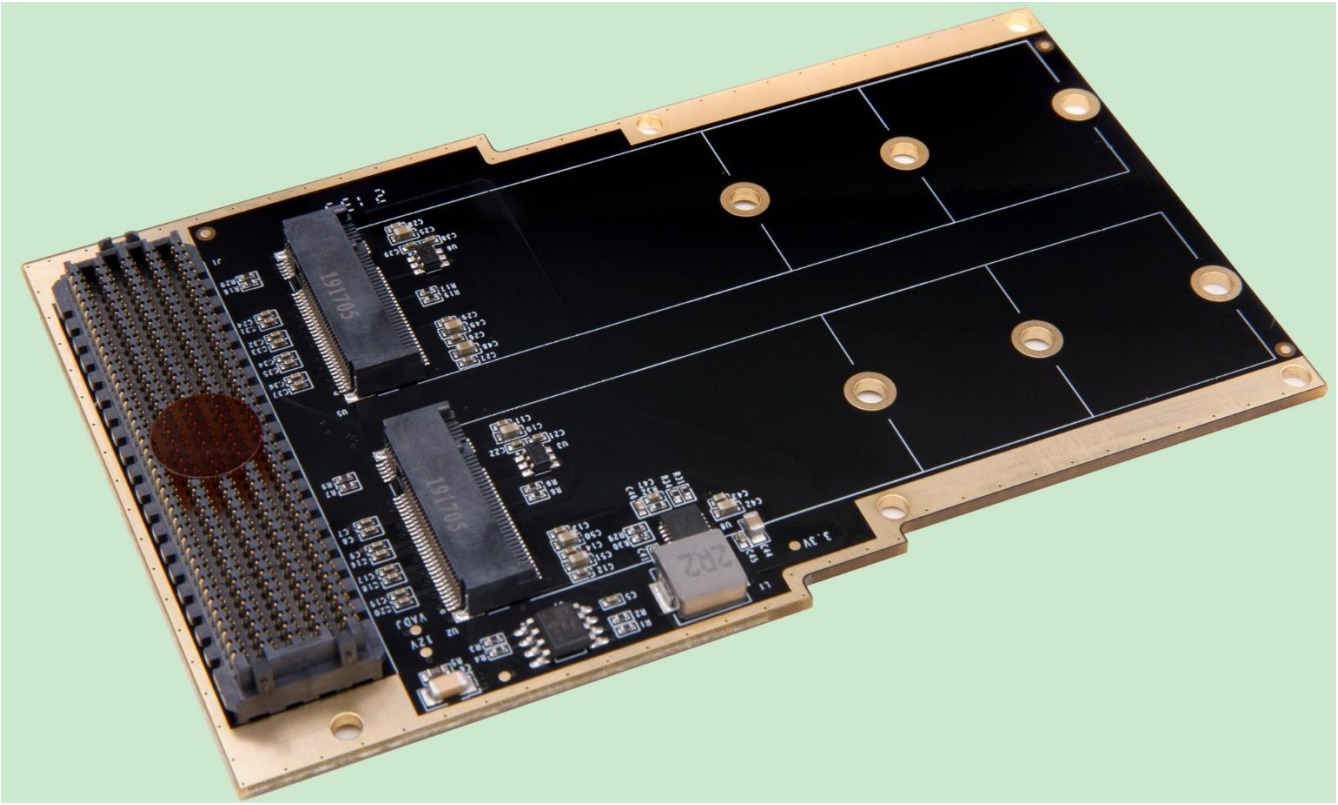
Part 1 FH1402 Module General Introduction

.ALINX FMC to 2* SSD NVME FH1402 is a module that converts FMC interfaces to 2-channel M.2 interfaces and is used to connect SSDS. The M.2 interface uses the M key slot and supports PCI-E X4, but does not support SATA. You need to select a PCIE-type SSD when selecting an SSD.

The FMC interface of the FH1402 is a standard HPC interface for connecting to the FPGA development board and meets the VITA 57.1 standard. The connector type of FMC is: ASP-134488-01.

The photo of FH1402 module is as follows:

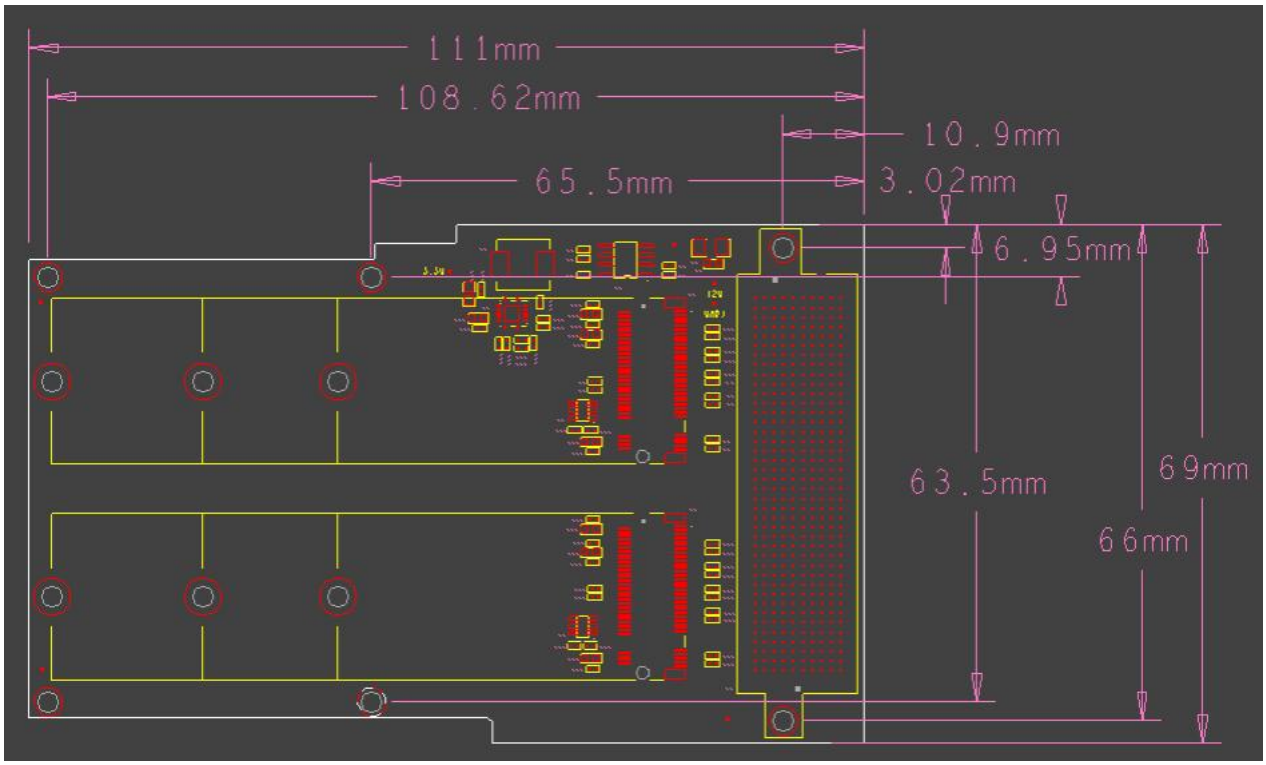


FH1402 Module

1.1 FH1402 Module Detail Parameter

- HPC connectors
- 2-channel M.2 interface, which supports PCIE X4

1.2 FH1402 Module Size Dimension

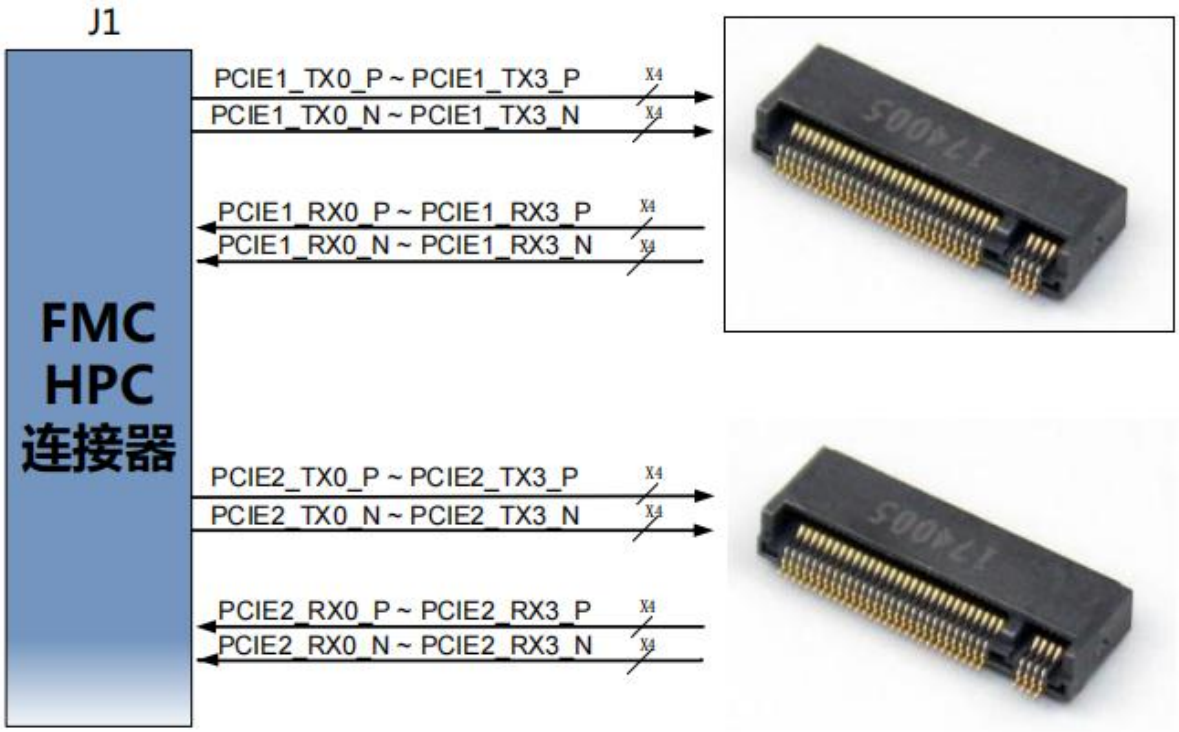


FH1402 Module Size Dimension

Part 2 Function Description of FH1402 Module

2.1 FH1402 Module Size Dimension

The principle design of FH1402 module is as follows:



2.2 Pin Assignment of Module FMC HPC

Only the interface signals are listed below, while the power and GND signals are not listed. Users can refer to the schematic diagram for details:

FMC Pin Number	Network Name	Description
C6	PCIE1_RX0_P	The 1st PCIE data 0 receive, Positive
C7	PCIE1_RX0_N	The 1st PCIE data 0 receive, Negative
A2	PCIE1_RX1_P	The 1st PCIE data 1 receive, Positive

A3	PCIE1_RX1_N	The 1st PCIE data 1 receive, Negative
A6	PCIE1_RX2_P	The 1st PCIE data 2 receive, Positive
A7	PCIE1_RX2_N	The 1st PCIE data 2 receive, Negative
A10	PCIE1_RX3_P	The 1st PCIE data 3 receive, Positive
A11	PCIE1_RX3_N	The 1st PCIE data 3 receive, Negative
C2	PCIE1_TX0_P	The 1st PCIE data 0 transmit, Positive
C3	PCIE1_TX0_N	The 1st PCIE data 0 transmit, Negative
A22	PCIE1_TX1_P	The 1st PCIE data 1 transmit, Positive
A23	PCIE1_TX1_N	The 1st PCIE data 1 transmit, Negative
A26	PCIE1_TX2_P	The 1st PCIE data 2 transmit, Positive
A27	PCIE1_TX2_N	The 1st PCIE data 2 transmit, Negative
A30	PCIE1_TX3_P	The 1st PCIE data 3 transmit, Positive
A31	PCIE1_TX3_N	The 1st PCIE data 3 transmit, Negative
D4	REFCLK0_FPGA_P	The 1st PCIE reference clock input, Positive
D5	REFCLK0_FPGA_N	The 1st PCIE reference clock input, Negative
H20	PCIE1_PEDET	The 1st PCIE device detection signal
H22	PCIE1_RSTN	The 1st PCIE device reset signal
H23	PCIE1_DEVSLP	The 1st PCIE device energy-saving signal
B12	PCIE2_RX0_P	The 2nd PCIE data 0 receive, Positive
B13	PCIE2_RX0_N	The 2nd PCIE data 0 receive, Negative
A14	PCIE2_RX1_P	The 2nd PCIE data 1 receive, Positive

A15	PCIE2_RX1_N	The 2nd PCIE data 1 receive, Negative
B16	PCIE2_RX2_P	The 2nd PCIE data 2 receive, Positive
B17	PCIE2_RX2_N	The 2nd PCIE data 2 receive, Negative
A18	PCIE2_RX3_P	The 2nd PCIE data 3 receive, Positive
A19	PCIE2_RX3_N	The 2nd PCIE data 3 receive, Negative
B32	PCIE2_TX0_P	The 2nd PCIE data 0 transmit, Positive
B33	PCIE2_TX0_N	The 2nd PCIE data 0 transmit, Negative
A34	PCIE2_TX1_P	The 2nd PCIE data 1 transmit, Positive
A35	PCIE2_TX1_N	The 2nd PCIE data 1 transmit, Negative
B36	PCIE2_TX2_P	The 2nd PCIE data 2 transmit, Positive
B37	PCIE2_TX2_N	The 2nd PCIE data 2 transmit, Negative
A38	PCIE2_TX3_P	The 2nd PCIE data 3 transmit, Positive
A39	PCIE2_TX3_N	The 2nd PCIE data 3 transmit, Negative
B20	REFCLK1_FPGA_P	The 2nd PCIE reference clock input, Positive
B21	REFCLK1_FPGA_N	The 2nd PCIE reference clock input, Negative
H7	PCIE2_PEDET	The 2nd PCIE device detection signal
G9	PCIE2_RSTN	The 2nd PCIE device reset signal
G10	PCIE2_DEVSLP	The 2nd PCIE device energy-saving signal