Subject: CEA201

Number of question: 20

**Multiple choice question:**

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| QN=1 | For random-access memory, \_\_\_\_\_\_\_\_\_\_ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use. |
| a. | Memory cycle time |
| b. | Direct access |
| c. | Transfer rate |
| d. | Access time |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=2 | The \_\_\_\_\_\_\_\_ consists of the access time plus any additional time required before a second access can commence. |
| a. | Latency |
| b. | Memory cycle time |
| c. | Direct access |
| d. | Transfer rate |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=3 | A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a \_\_\_\_\_\_\_\_\_. |
| a. | Disk cache |
| b. | Latency |
| c. | Virtual address |
| d. | Miss |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=4 | A line includes a \_\_\_\_\_\_\_\_\_ that identifies which particular block is currently being stored. |
| a. | Cache |
| b. | Hit |
| c. | Tag |
| d. | Locality |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=5 | \_\_\_\_\_\_\_\_\_\_ is the simplest mapping technique and maps each block of main memory into only one possible cache line. |
| a. | Direct mapping |
| b. | Associative mapping |
| c. | Set associative mapping |
| d. | None of the above |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=6 | When using the \_\_\_\_\_\_\_\_\_\_ technique all write operations made to main memory are made to the cache as well. |
| a. | Write back |
| b. | LRU |
| c. | Write through |
| d. | Unified cache |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=7 | The key advantage of the \_\_\_\_\_\_\_\_\_\_ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit. |
| a. | Logical cache |
| b. | Split cache |
| c. | Unified cache |
| d. | Physical cache |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=8 | The Pentium 4 \_\_\_\_\_\_\_\_\_ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers. |
| a. | Fetch/decode unit |
| b. | Out-of-order execution logic |
| c. | Execution unit |
| d. | Memory subsystem |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=9 | In reference to access time to a two-level memory, a \_\_\_\_\_\_\_\_\_ occurs if an accessed word is not found in the faster memory. |
| a. | Miss |
| b. | Hit |
| c. | Line |
| d. | Tag |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=10 | A logical cache stores data using \_\_\_\_\_\_\_\_\_\_. |
| a. | Physical addresses |
| b. | Virtual addresses |
| c. | Random addresses |
| d. | None of the above |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=11 | Which properties do all semiconductor memory cells share? |
| a. | They exhibit two stable states which can be used to represent binary 1 and 0 |
| b. | They are capable of being written into to set the state |
| c. | They are capable of being read to sense the state |
| d. | All of the above |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=12 | One distinguishing characteristic of memory that is designated as \_\_\_\_\_\_\_\_\_ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly. |
| a. | RAM |
| b. | ROM |
| c. | EPROM |
| d. | EEPROM |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=13 | Which of the following memory types are nonvolatile? |
| a. | Erasable PROM |
| b. | Programmable ROM |
| c. | Flash memory |
| d. | All of the above |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=14 | In a \_\_\_\_\_\_\_\_\_, binary values are stored using traditional flip-flop logic-gate configurations. |
| a. | ROM |
| b. | SRAM |
| c. | DRAM |
| d. | RAM |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=15 | A \_\_\_\_\_\_\_\_\_\_ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it. |
| a. | RAM |
| b. | SRAM |
| c. | ROM |
| d. | Flash memory |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=16 | With \_\_\_\_\_\_\_\_\_ the microchip is organized so that a section of memory cells are erased in a single action. |
| a. | Flash memory |
| b. | SDRAM |
| c. | DRAM |
| d. | EEPROM |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=17 | \_\_\_\_\_\_\_\_\_\_ can be caused by harsh environmental abuse, manufacturing defects, and wear. |
| a. | SEC errors |
| b. | Hard errors |
| c. | Syndrome errors |
| d. | Soft errors |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=18 | \_\_\_\_\_\_\_\_\_ can be caused by power supply problems or alpha particles. |
| a. | Soft errors |
| b. | AGT errors |
| c. | Hard errors |
| d. | SEC errors |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=19 | The \_\_\_\_\_\_\_\_\_ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states. |
| a. | DDR-DRAM |
| b. | SDRAM |
| c. | CDRAM |
| d. | None of the above |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |

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| QN=20 | \_\_\_\_\_\_\_\_ can send data to the processor twice per clock cycle. |
| a. | CDRAM |
| b. | SDRAM |
| c. | DDR-DRAM |
| d. | RDRAM |
| e. |  |
| f. |  |
| ANSWER: |  |
| MARK: | 1 |
| UNIT: | 1 |
| MIX CHOICES: | no |