Working with DSP48 Macro IP core version 2.1:

The Xilinx LogiCORE™ DSP48 Macro provides an easy-to-use interface that abstracts the XtremeDSP™ slice and simplifies its dynamic operation by enabling the specification of multiple operations via a set of user defined arithmetic expressions. The specified operations are enumerated and can be selected by the user via a single port on the generated core.

Features:

- Simplified and abstracted interface to XtremeDSP slice enhances ease of use, code readability and portability
- Define XtremeDSP slice operation via a list of user-defined arithmetic expressions
- Support for up to 64 instructions
- Supports the XtremeDSP slice pre-adder
- Configurable latency
- Option to choose between XtremeDSP Slice or fabric implementation
- Support of signed, two’s complement input data

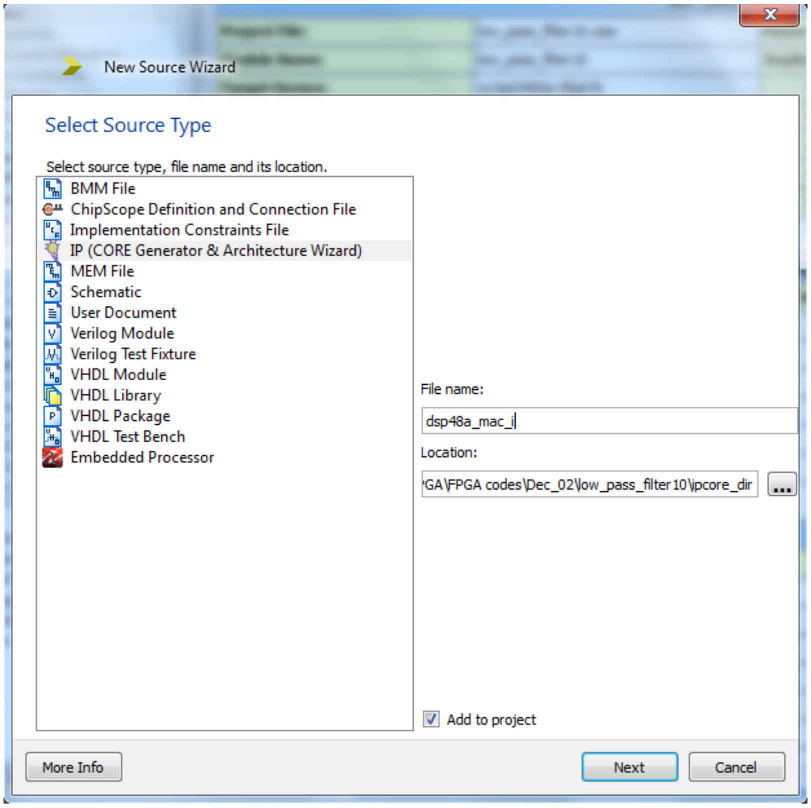
Implementation:

1. From the Project Navigator, select Project -> New Source

2. Select IP (CORE Generator & Architecture Wizard) and enter a Filename (refer Figure1.1)

3. Click Next and then select the type of core (refer Figure1.2)

4. After a few seconds a new window (LogiCore) should pop up. Customize the parameters for your design as you see in the figure below.



New Source Wizard

Select Source Type

Select source type, file name and its location.

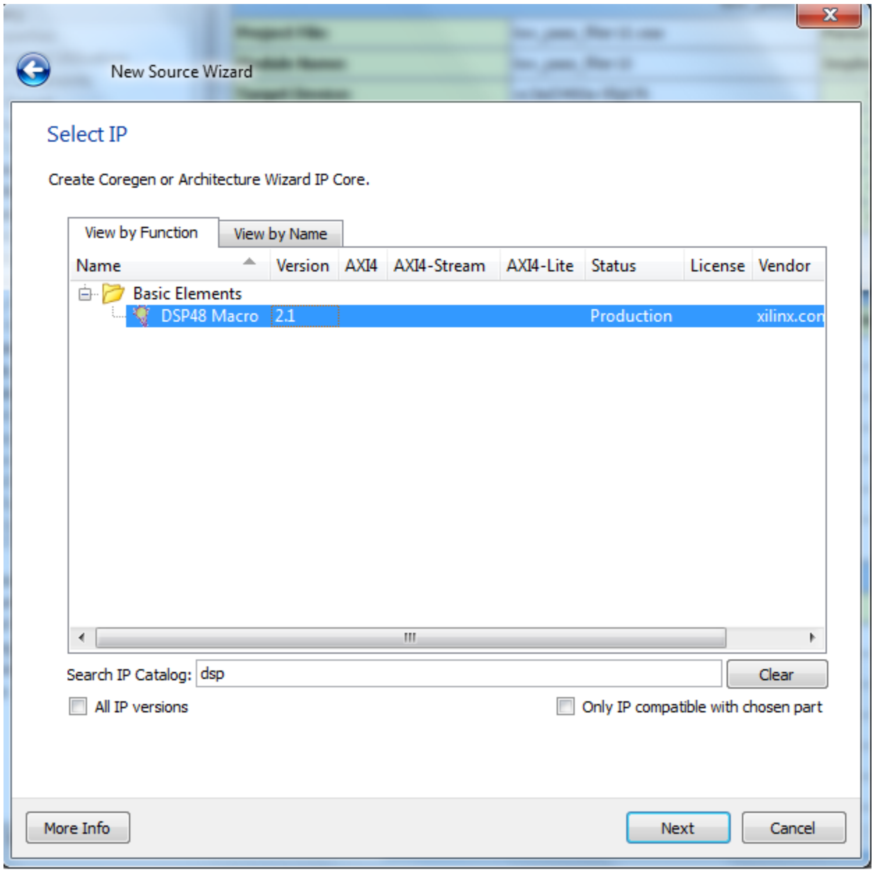
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor

File name: dsp48a_mac_i

Location: GA\FPGA codes\Dec_02\low_pass_filter10\ipcore_dir

☑ Add to project

Figure 1.1 New Source Wizard (Select Source Type)



Create Coregen or Architecture Wizard IP Core.

Name	Version	AXI4	AXI4-Stream	AXI4-Lite	Status	License	Vendor
Basic Elements							
DSP48 Macro	2.1				Production		xilinx.con

Search IP Catalog: dsp

□ All IP versions

□ Only IP compatible with chosen part

Figure 1.2 Select IP Core Type

Take a minute to click on the Data Sheet… button on the bottom of the screen. The provided data sheets are essential in larger designs to understand many timing issues associated with a specific core as well as explaining all the different design choices.

There are three pages of parameters which we can customize based on the application.

a. Instruction page
b. Latency page
c. Port properties page

Instruction page (refer fig 1.3)

In the instruction page user can define their own instructions depends on the application. DSP48 Macro supports for up to 64 instructions. There is a port called "**SEL [ ]**" which enables to access different instructions. For instance, if we need four instructions to perform a single operation, the port size will be changed into SEL [1:0]. This means by selecting '00' we can access first instruction and '01' for second instruction and so on.

Instruction Format:

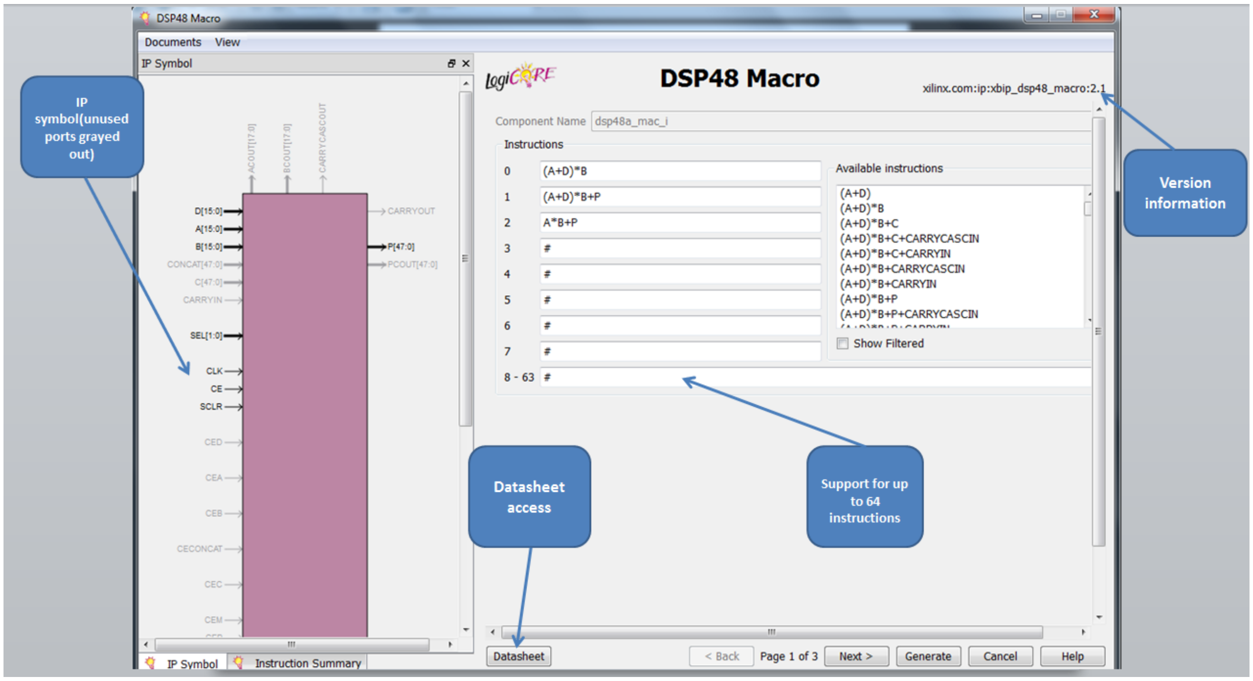
The instructions are case insensitive and ignore spaces between operands. The left side of the arithmetic expression, P=, is implicitly declared and should not be specified

Valid operands: D, A, ACIN, B, BCIN, CONCAT, C, PCIN, CARRYIN, CARRYCASCIN, 0.

Valid operators: +, -, *, >>17, (,).

Valid functions: rndsimple, rndsym

- Rounding functions require that the P output width is less than full precision.



DSP48 Macro

xilinx.com:ip:xbip_dsp48_macro:2.1

Component Name dsp48a_mac_i

Instructions

0 (A+D)*B
1 (A+D)*B+P
2 A*B+P
3 #
4 #
5 #
6 #
7 #
8 - 63 #

Available instructions

(A+D)
(A+D)*B
(A+D)*B+C
(A+D)*B+C+CARRYCASCIN
(A+D)*B+C+CARRYIN
(A+D)*B+CARRYCASCIN
(A+D)*B+CARRYIN
(A+D)*B+P
(A+D)*B+P+CARRYCASCIN

□ Show Filtered

Datasheet

IP symbol(unused ports grayed out)

Version information

Datasheet access

Support for up to 64 instructions

Figure 1.3 Instruction page

Example:

Let us consider 15tap FIR symmetric filter, where data is provided sequentially on the A, D and B inputs in order to perform multiply and accumulation operation. Both A and D are used for the data values and B is used for the filter coefficients. Then we can define the instructions as below as,

1. (A+D)*B: Taps 1 & 15 (here A = tap 1 value, D = tap 15 value)

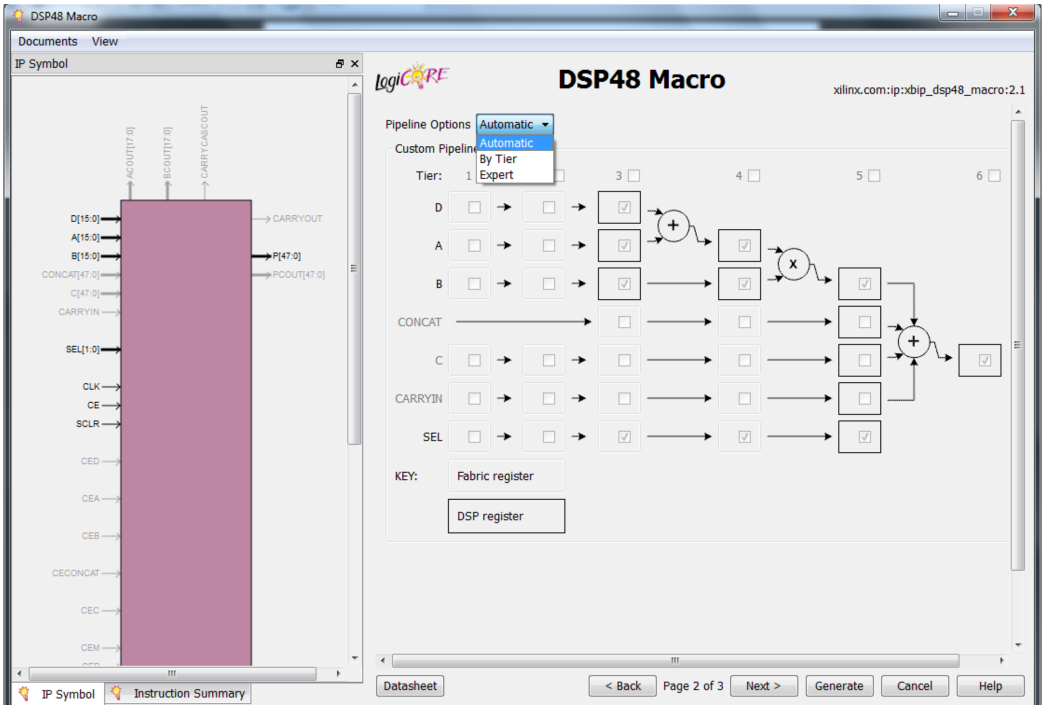
2. (A+D)*B+ P: Taps 2...7 & 14...9 (here A = tap2 value, D = tap 14 value and B = filter coeff 'h0' and so on)

3. A*B+ P: Tap 8

Latency page: (refer fig.1.4)

In the latency page there is an option to choose pipelining depends on the timing constraint of the application. There are three types of custom pipeline as follows:

1. Automatic
2. By tier
3. Expert



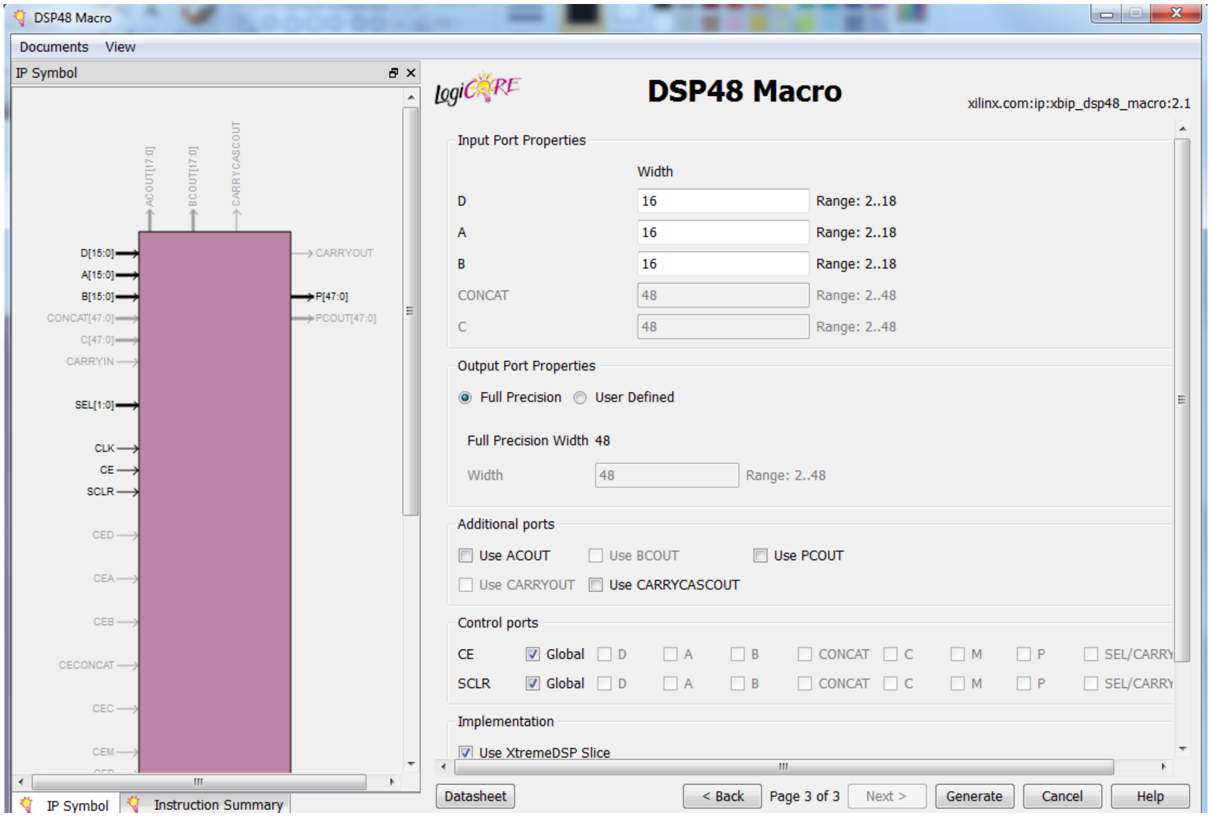
Pipeline Options: Automatic

Custom Pipeline

Figure 1.4 Latency page

Port properties page: (refer fig 1.5)

In this page you can customize the input, output and control port properties. Then click generate to create your IP core design.



Input Port Properties

	Width	
D	16	Range: 2..18
A	16	Range: 2..18
B	16	Range: 2..18
CONCAT	48	Range: 2..48
C	48	Range: 2..48

Output Port Properties

● Full Precision ○ User Defined

Full Precision Width 48

Width 48 Range: 2..48

Additional ports

□ Use ACOUT □ Use BCOUT □ Use PCOUT

□ Use CARRYOUT □ Use CARRYCASCOUT

Control ports

CE	☑ Global	□ D	□ A	□ B	□ CONCAT	□ C	□ M	□ P	□ SEL/CARRY
SCLR	☑ Global	□ D	□ A	□ B	□ CONCAT	□ C	□ M	□ P	□ SEL/CARRY

Implementation

☑ Use XtremeDSP Slice

Figure 1.4 Port properties page