1. OVERVIEW OF XILINX ISE DESIGN SUITE (HDL DESIGN FLOW BASED):

Objective:

a) The primary focus of this tutorial is to show the relationship among the design entry tools, Xilinx and third-party tools, and the design implementation tools.
b) This guide is a learning tool for designers who are unfamiliar with the features of the ISE software or those wanting to refresh their skills and knowledge.
c) Also, this tutorial provides an introduction to the simulation flow within Project Navigator, including highlights of features within the ISim simulators.

Software overview:

The ISE software controls all aspects of the design flow. Through the Project Navigator interface, you can access all of the design entry and design implementation tools. You can also access the files and documents associated with your project.

Project Navigator Interface:

By default, the Project Navigator interface is divided into **four panel sub windows**, as seen in Figure1.1

1. On the top left are the **Start, Design, Files**, and **Libraries** panels, which include display and access to the source files in the project as well as access to running processes for the currently selected source. The Start panel provides quick access to opening projects as well as frequently access reference material, documentation and tutorials.

2. At the bottom of the Project Navigator are the **Console, Errors**, and **Warnings** panels, which display status messages, errors, and warnings.

3. To the right is a multi-document interface (MDI) window referred to as the **Workspace**. The Workspace enables you to view design reports, text files, schematics, and simulation waveforms.

Each window can be resized, undocked from Project Navigator, moved to a new location within the main Project Navigator window, tiled, layered, or closed. You can use the View >Panels menu commands to open or close panels. You can use the Layout > Load Default Layout to restore the default window layout. These windows are discussed in more detail in the following sections.

Design Panel

The Design panel provides access to the View, Hierarchy, and Processes panes.

View Pane

The View pane radio buttons enable you to view the source modules associated with the Implementation or Simulation Design View in the Hierarchy pane. If you select Simulation, you must select a simulation phase from the drop-down list.

Hierarchy Pane

The Hierarchy pane displays the project name, the target device, user documents, and design source files associated with the selected Design View. The View pane at the top of the Design panel allows you to view only those source files associated with the selected Design View, such as Implementation or Simulation.

Each file in the Hierarchy pane has an associated icon. The icon indicates the file type (HDL file, schematic, core, or text file, for example). For a complete list of possible source types and their associated icons, see the “Source File Types” topic in the ISE Help. From Project Navigator, select Help > Help Topics to view the ISE Help.

If a file contains lower levels of hierarchy, the icon has a plus symbol (+) to the left of the name. You can expand the hierarchy by clicking the plus symbol (+). You can open a file for editing by double-clicking on the filename.

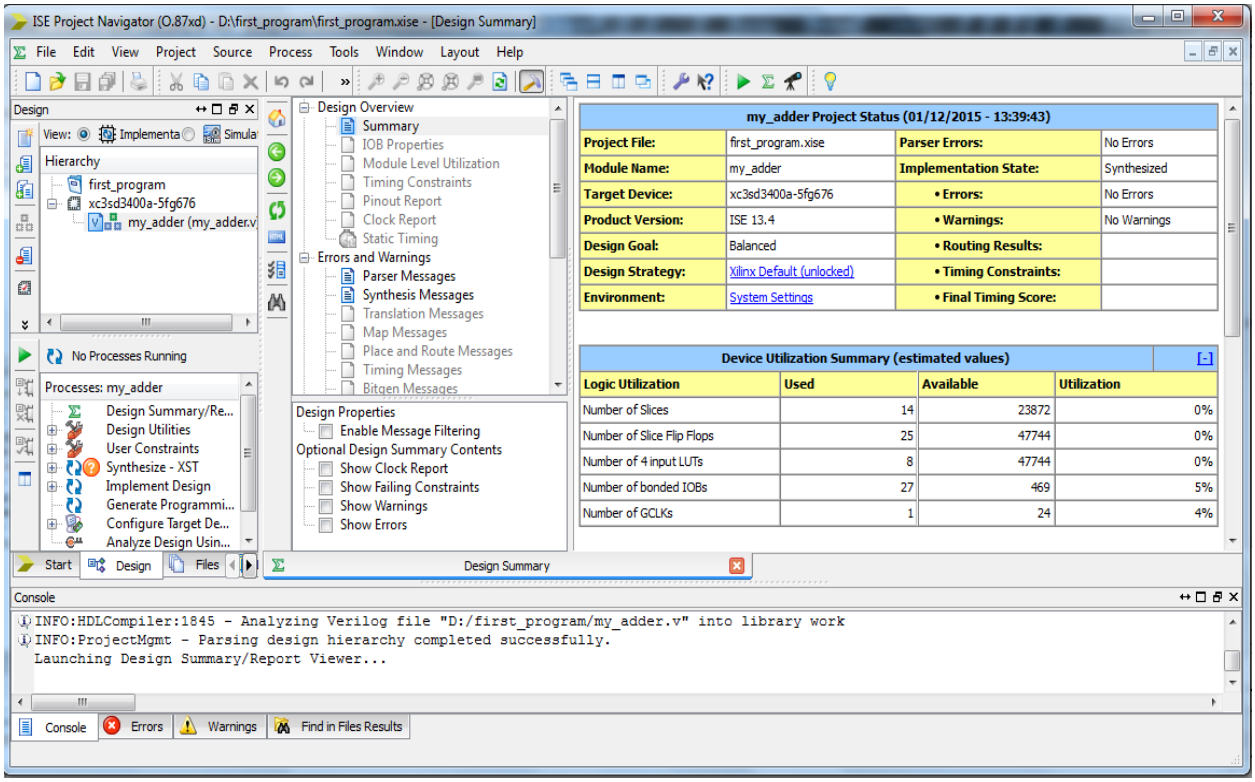

Figure 1.1 Project Navigator Interface

Processes Pane

The Processes pane is context sensitive, and it changes based upon the source type selected in the Sources pane and the top-level source in your project. From the Processes pane, you can run the functions necessary to define, run, and analyze your design.

The Processes pane provides access to the following functions:

- **Design Summary/Reports**
  Provides access to design reports, messages, and summary of results data. Message filtering can also be performed.

- **Design Utilities**
  Provides access to symbol generation, instantiation templates, viewing command line history, and simulation library compilation.

- **User Constraints**
  Provides access to editing location and timing constraints.

- **Synthesis**
  Provides access to Check Syntax, Synthesis, View RTL or Technology Schematic, and synthesis reports. Available processes vary depending on the synthesis tools you use.

- **Implement Design**
  Provides access to implementation tools and post-implementation analysis tools.

- **Generate Programming File**
  Provides access to bit stream generation.

- **Configure Target Device**
  Provides access to configuration tools for creating programming files and programming the device.

The Processes pane incorporates dependency management technology. The tools keep track of which processes have been run and which processes need to be run. Graphical status indicators display the state of the flow at any given time. When you select a process in the flow, the software automatically runs the processes necessary to get to the desired step. For example, when you run the Implement Design process, Project Navigator also runs the Synthesis process because implementation is dependent on up-to-date synthesis results.

Files Panel

The Files panel provides a flat, sortable list of all the source files in the project. Files can be sorted by any of the columns in the view. Properties for each file can be viewed and modified by right-clicking on the file and selecting Source Properties.

Libraries Panel

The Libraries panel enables you to manage HDL libraries and their associated HDL source files. You can create, view, and edit libraries and their associated sources.

Console Panel

The Console provides all standard output from processes run from Project Navigator. It displays errors, warnings, and information messages. Errors are signified by a red X next to the message; while warnings have a yellow exclamation mark (!).

Errors Panel

The Errors panel displays only error messages. Other console messages are filtered out.

Warnings Panel

The Warnings panel displays only warning messages. Other console messages are filtered out.

Error Navigation to Source

You can navigate from a synthesis error or warning message in the Console, Errors, or Warnings panel to the location of the error in a source HDL file. To do so, select the error or warning message, right-click the mouse, and select Go to Source from the right-click menu. The HDL source file opens, and the cursor moves to the line with the error.

Error Navigation to Answer Record

You can navigate from an error or warning message in the Console, Errors, or Warnings panel to relevant Answer Records on the Support page of the Xilinx® website. To navigate to the Answer Record, select the error or warning message, right-click the mouse, and select Go to Answer Record from the right-click menu. The default Web browser opens and displays all Answer Records applicable to this message.

Workspace

The Workspace is where design editors, viewers, and analysis tools open. These include ISE Text Editor, Schematic Editor, Constraint Editor, Design Summary/Report Viewer, RTL and Technology Viewers, and Timing Analyzer. Other tools such as the PlanAhead™ software for I/O planning and floorplanning, ISim, third-party text editors, XPower Analyzer, and iMPACT open in separate windows outside the main Project Navigator environment when invoked.

Design Summary/Report Viewer

The Design Summary provides a summary of key design data as well as access to all of the messages and detailed reports from the synthesis and implementation tools. The summary lists high-level information about your project, including overview information, a device utilization summary, performance data gathered from the Place and Route (PAR) report, constraints information, and summary information from all reports with links to the individual reports. A link to the System Settings report provides information on environment variables and tool settings used during the design implementation.

HDL-BASED DESIGN FLOW:

This chapter guides you to implement a typical HDL-based design. This design targets a Spartan™-3A device; however, all of the principles and flows taught are applicable to any Xilinx® device family, unless otherwise noted.

Starting the ISE Software:

To start the ISE software, double-click the ISE Project Navigator icon on your desktop, or select, **Start > All Programs > Xilinx ISE Design Suite 12.1 > ISE Design Tools > Project Navigator.**

Figure 1.2 Xilinx ISE Design Suite 13.4 icon

Creating a New Project:

To create a new project using the New Project Wizard, do the following:

1. From Project Navigator, select **File > New Project.**
   The New Project Wizard appears (see Fig. 1.3).

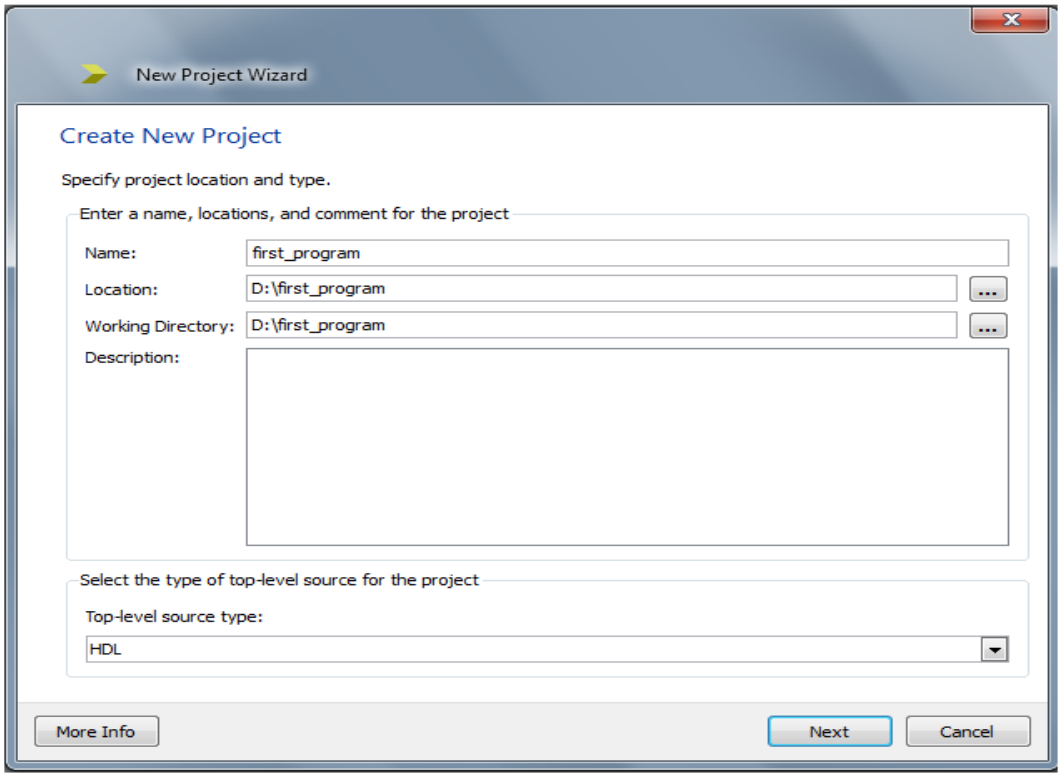

Figure1.3 New Project Wizard

2. In the Location field, browse to c:\xilinx\13.4\ISE\ISEexamples or to the directory in which you installed the project.
3. In the Name field, enter **first_program**
4. Verify that HDL is selected as the Top-Level Source Type, and click **Next**.
   The New Project Wizard—Device Properties page appears.
5. Select the following values in the New Project Wizard—Device Properties page (see Fig. 1.4):
   ♦ Product Category: **All**
   ♦ Family: **Spartan-3A DSP**
   ♦ Device: **XC3SD3400A**
   ♦ Package: **FG676**
   ♦ Speed: **-5**
   ♦ Synthesis Tool: **XST (VHDL/Verilog)**
   ♦ Simulator: **ISim (VHDL/Verilog)**
   ♦ Preferred Language: **VHDL** or **Verilog** depending on preference. This will determine the default language for all processes that generate HDL files. Other properties can be left at their default values.

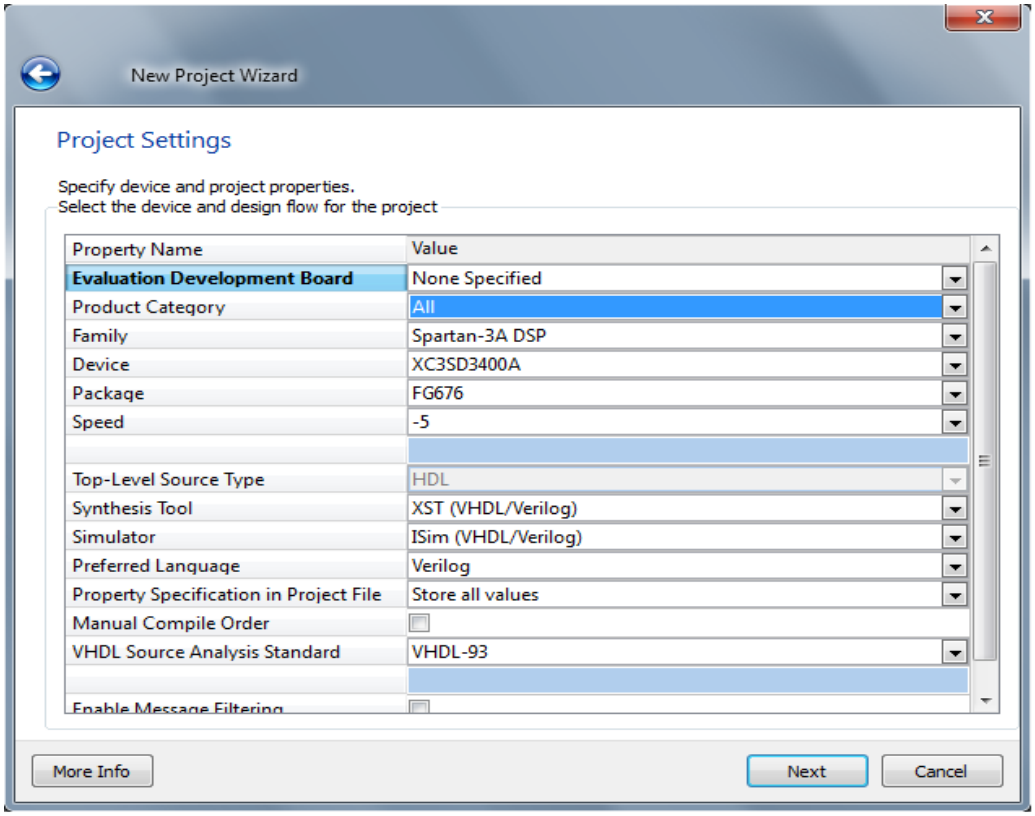

Figure 1.4. Project Settings

6. Click **Next**, then Finish to complete the project creation (see Fig. 1.5).

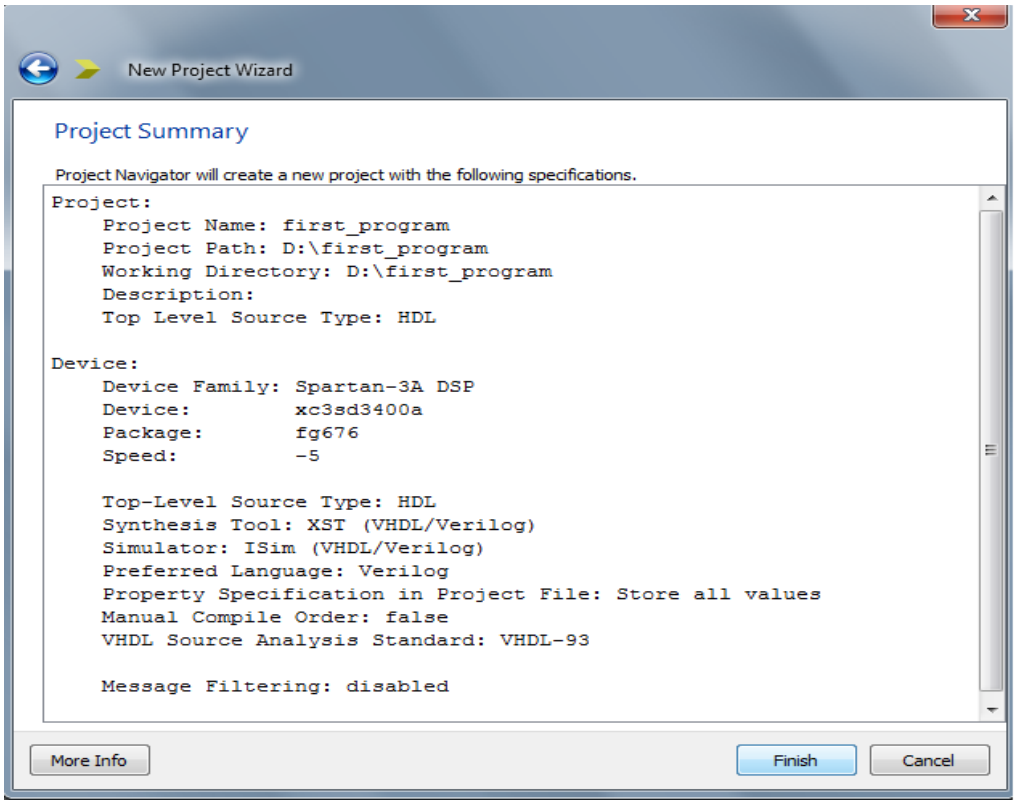

Figure 1.5 Project summary

Creating an HDL-Based Module:

Next you will create a module from HDL code. With the ISE software, you can easily create modules from HDL code using the ISE Text Editor. The HDL code is then connected to your top-level HDL design through instantiation and is compiled with the rest of the design.

Using the New Source Wizard and ISE Text Editor

In this section, you create a file using the New Source wizard, specifying the name and ports of the component. The resulting HDL file is then modified in the ISE Text Editor.

To create the source file, do the following:

1. Select **Project > New Source.**
The New Source Wizard opens in which you specify the type of source you want to create (see Fig. 1.6).

2. In the Select Source Type page, select **VHDL Module** or **Verilog Module**.

3. In the File Name field, enter **my_adder.**

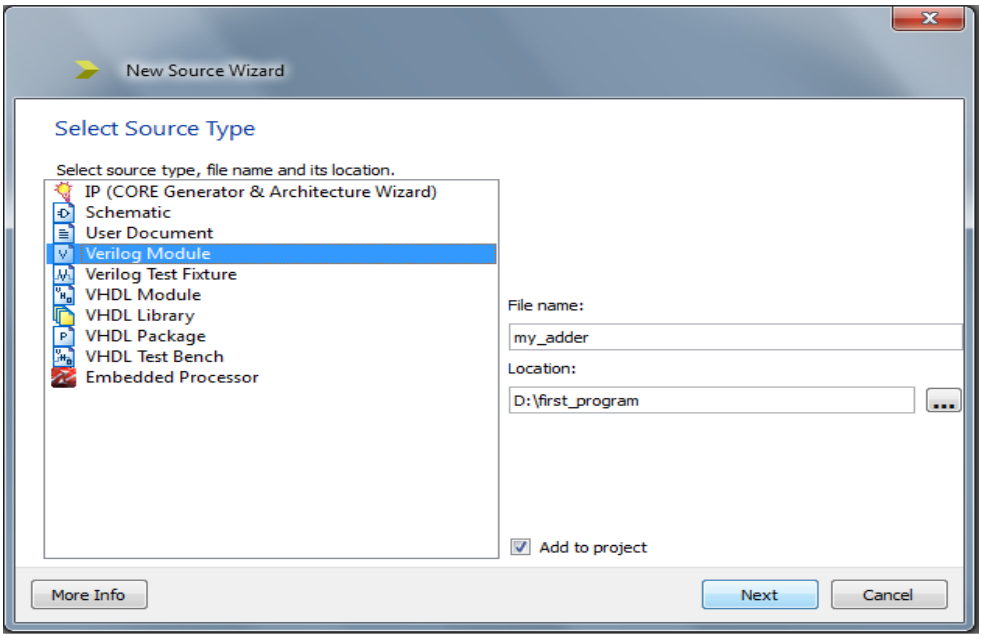

Figure 1.6 New source Wizard

4. Click **Next**.
5. In the Define Module page, enter two input ports named **In_1** and **In_2** and an output port named **Output** for the my_adder component as follows(see Fig. 1.7):
    a. In the first three Port Name fields, enter **In_1, In_2** and **Output**.
    b. Set the Direction field to **input** for In_1 and In_2 and to **output** for Output.
    c. Select the Bus designation boxes if you want to specify your signal dimension.

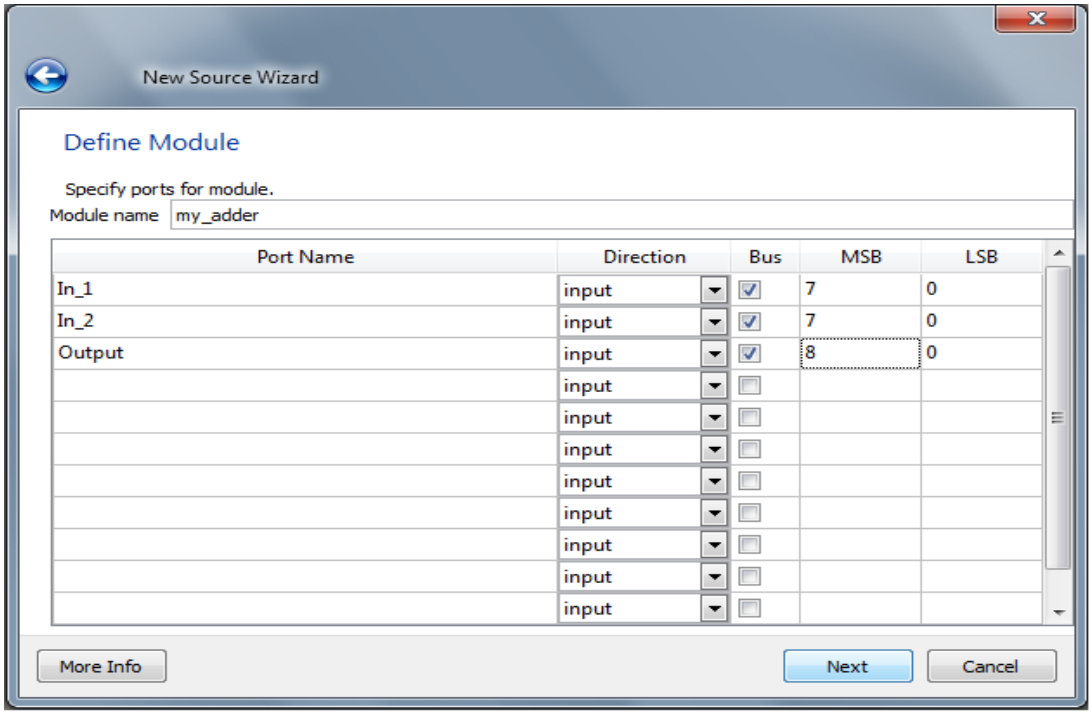

Figure 1.7 Define Module

6. Click **Next** to view a description of the module (see Fig. 1.8).

7. Click **Finish** to open the empty HDL file in the ISE Text Editor (see Fig. 1.9).

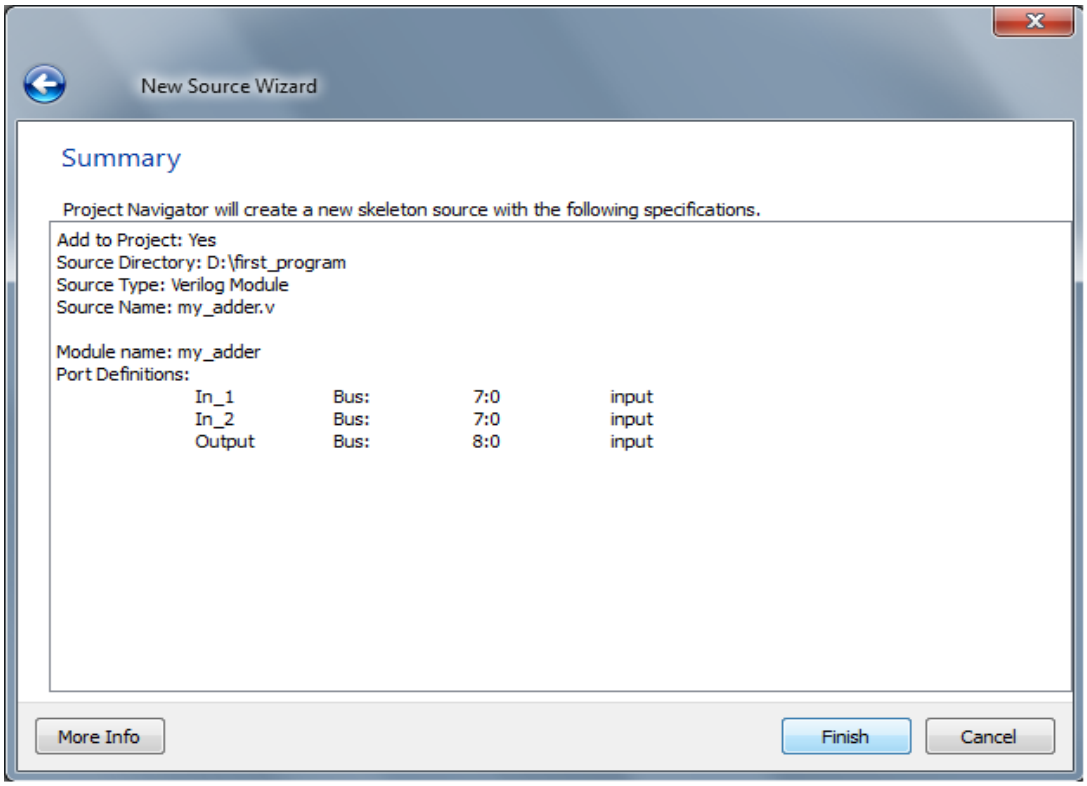

Figure 1.8 Module summary

Following is an example Verilog file. Then enter your logic in this file.

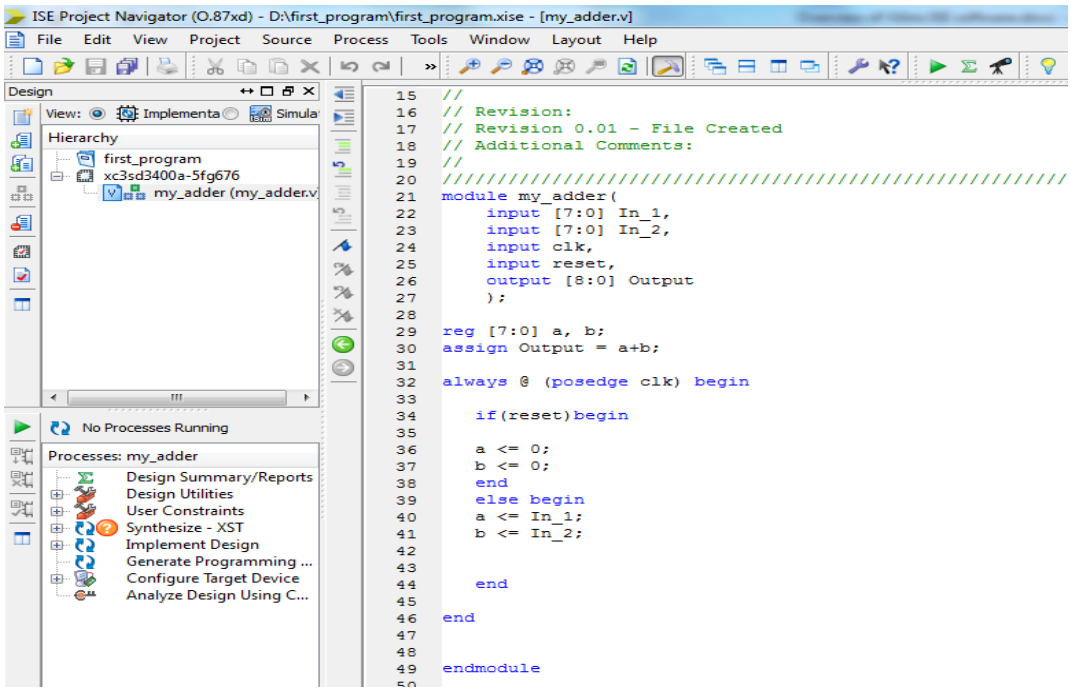

Figure 1.9 Verilog modules (.v)

In the ISE Text Editor, the ports are already declared in the HDL file, and some of the basic file structure is already in place. Keywords are displayed in blue, comments in green, and values are black. The file is color-coded to enhance readability and help you recognize typographical errors.

Creating HDL based test bench:

Once HDL based design entry is done, we can create our own test bench to provide stimulus to the design. To create the source file, do the following:

1. Select **Project > New Source.**
   The New Source Wizard opens in which you specify the source type, file name and its location (see Fig. 1.10).

2. In the Select Source Type page, select **Verilog Test Fixture**.

3. In the File Name field, enter **my_adder_testbench.**

4. Click **Next.**

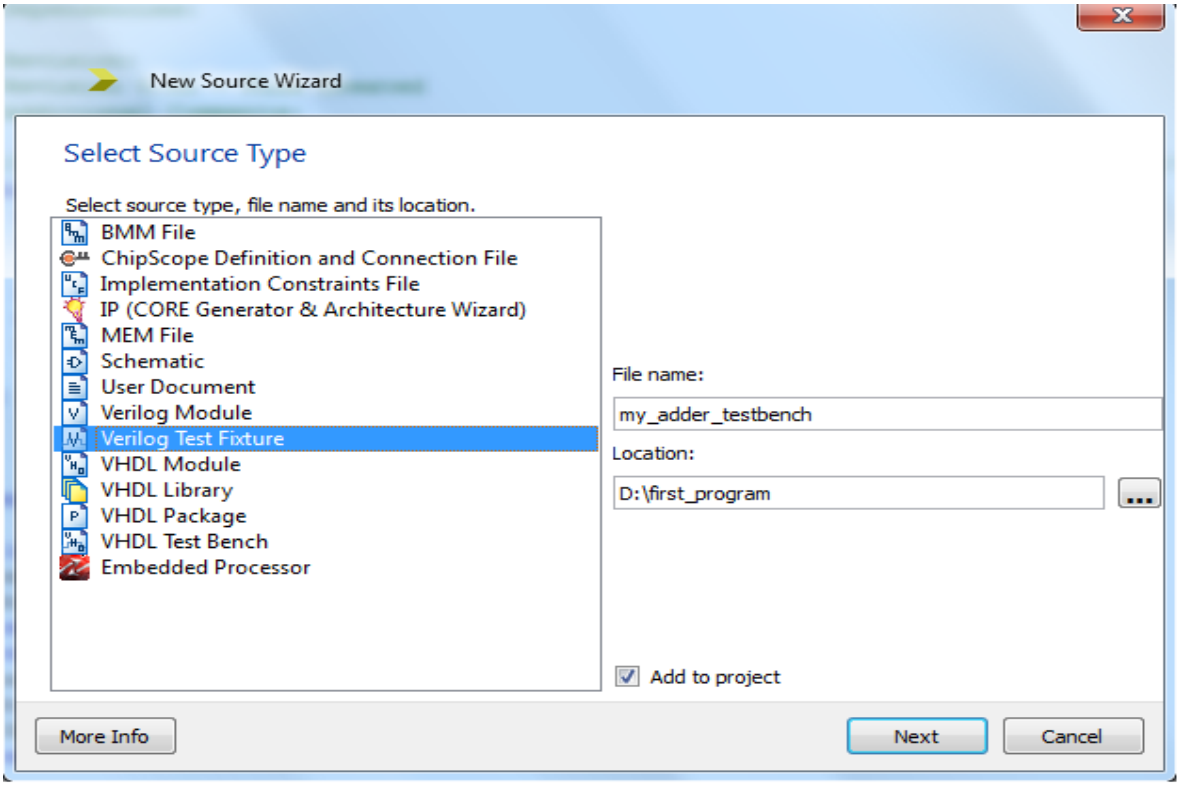

Figure 1.10 New Source Wizard

5. In the Associate Source page, select the source with which to associate the new source (see Fig. 1.11).

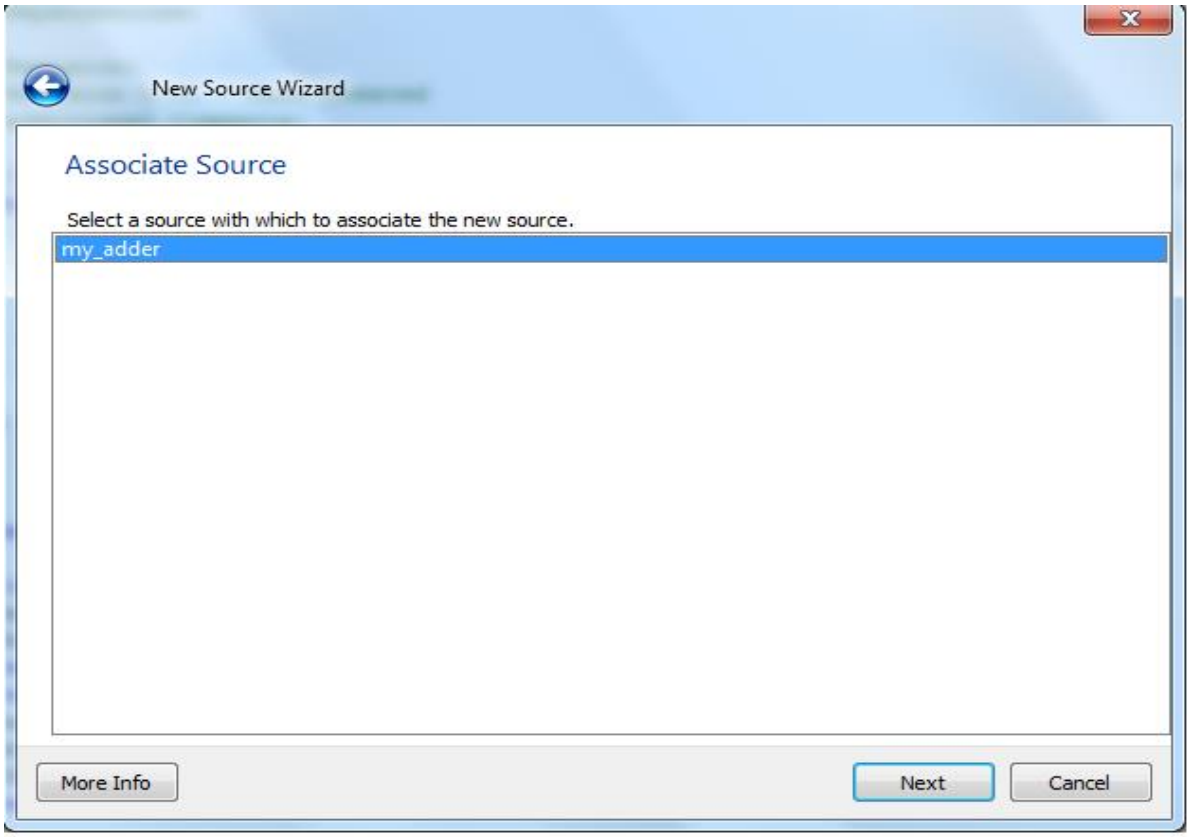

Figure 1.11 Associate Source page

6. Click **Next** to view a description of the test bench (see Fig. 1.12).

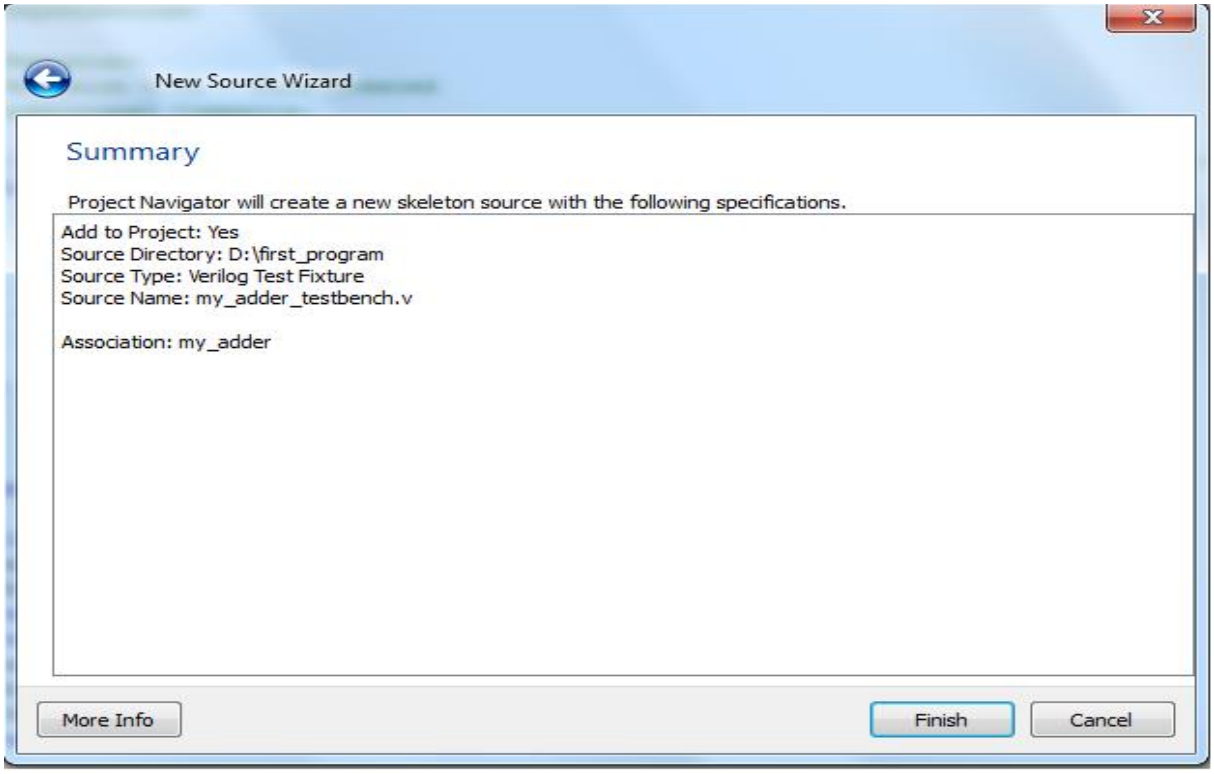

Figure 1.12 Test bench summary

7. Click **Finish** to open the HDL test bench file in the ISE Text Editor (see Fig. 1.13).

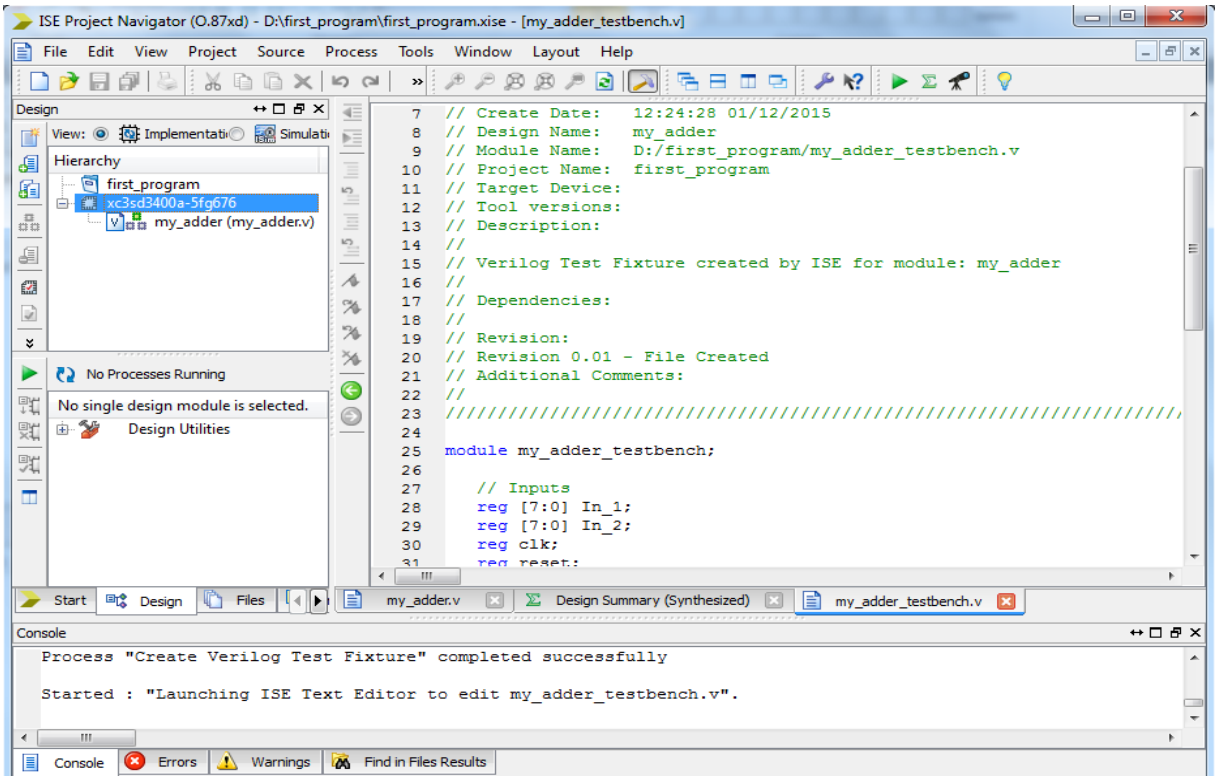

Figure 1.13 Testbench file (.v)

8. Enter your stimulus values in the testbench and then check for the syntax by clicking on the **Behavioral Check Syntax** which is located on the process panel(see Fig. 1.14).

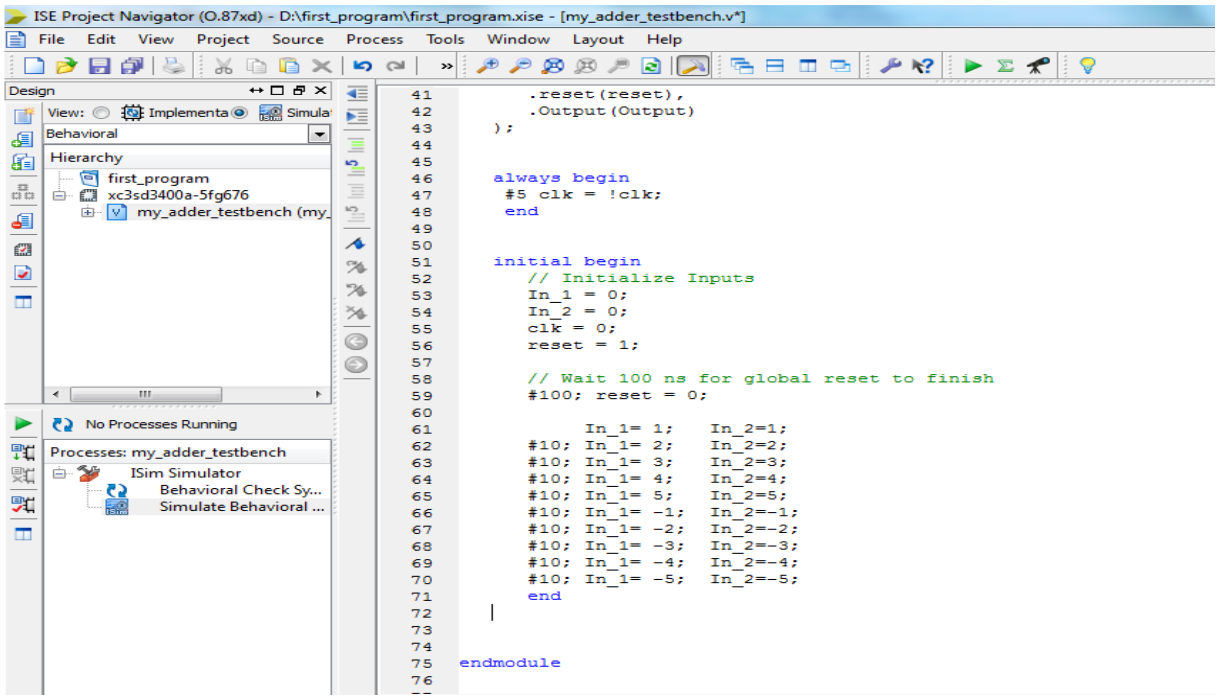

Figure 1.14 Stimulus values

Locating the Simulation Processes:

The simulation processes in the ISE software enable you to run simulation on the design using ISim. To locate the ISim processes, do the following:

1. In the View pane of the Project Navigator Design panel, select **Simulation**, and select **Behavioral** from the drop-down list.

2. In the Hierarchy pane, select the testbench file (**my_adder_testbench**).

3. In the Processes pane, expand **ISim Simulator** to view the process hierarchy. The following simulation processes are available:

♦ **Behavioral Check Syntax**
This process checks for syntax errors in the test bench.
♦ **Simulate Behavioral Model**
This process starts the design simulation.

Finally, click on the **Simulate behavioral model** to view the waveform associated with your implementation.

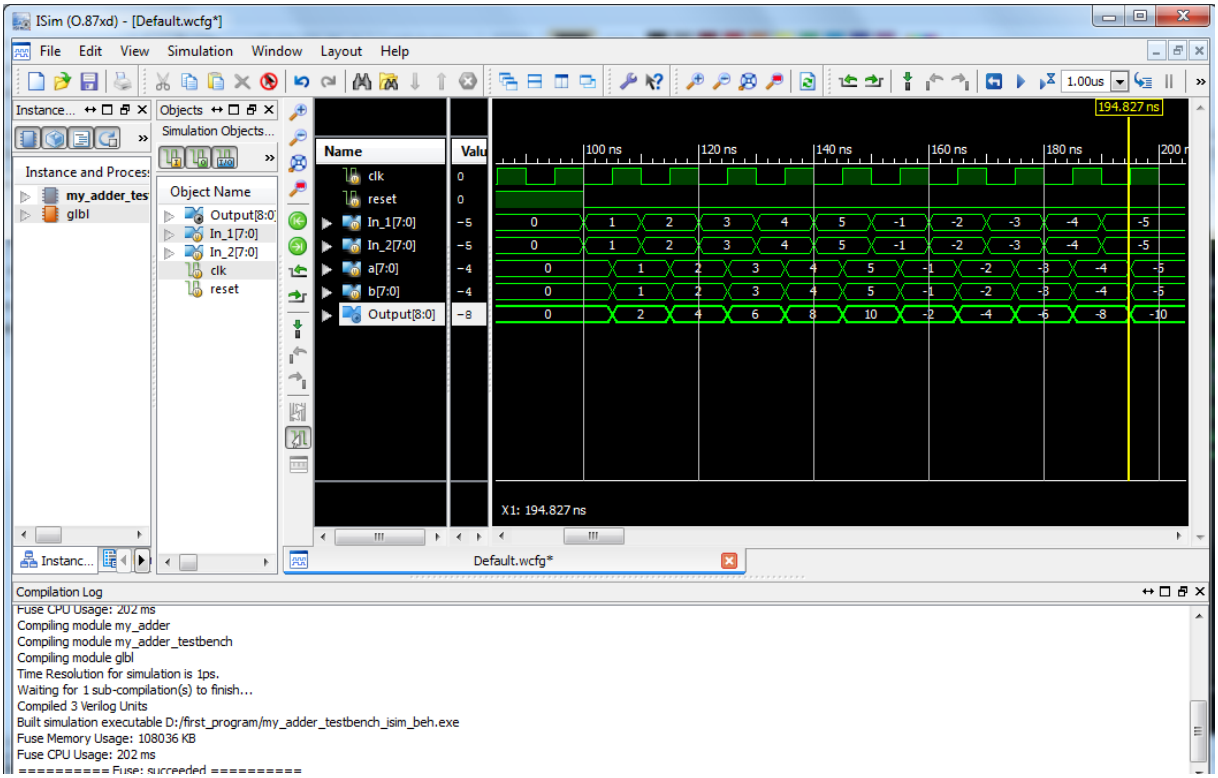

Figure 1.15 Simulation waveform

2. HOW TO MANAGE XILINX LICENSE:

For Linux:

1. Open the terminal
2. Go to the directory **“cd /opt/Xilinx/13.4/ISE_DS/common/bin/lin”**
3. Execute the file “**xlcm”** (refer fig 2.1)
4. After few seconds, Xilinx License Configuration Manager Window should pop-up
5. Select “Get My Purchased License(s)” and then click next (refer fig 2.2)
6. A new window should pop-up which contains local system information and then click on the “**Connect Now**” button (refer fig 2.3)
    - Note: make sure that your system is connected with wired network through LAN cable

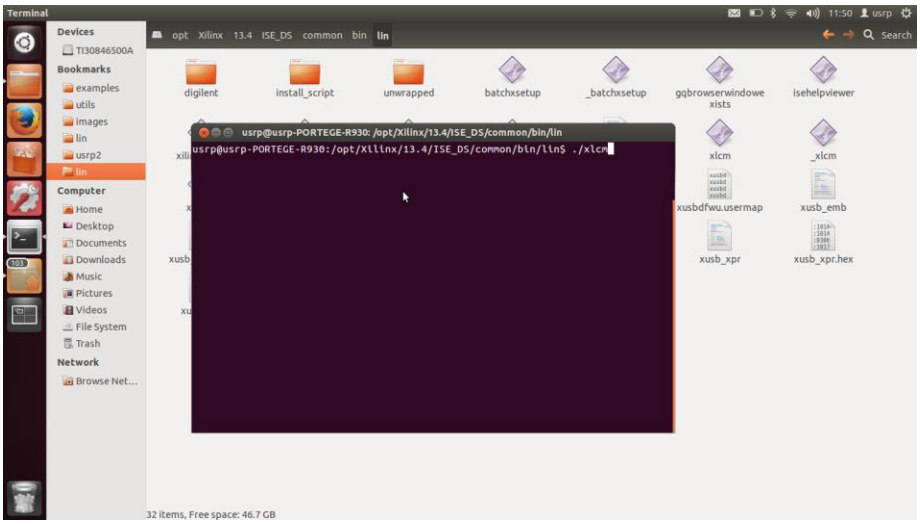

Fig 2.1 open license manage file

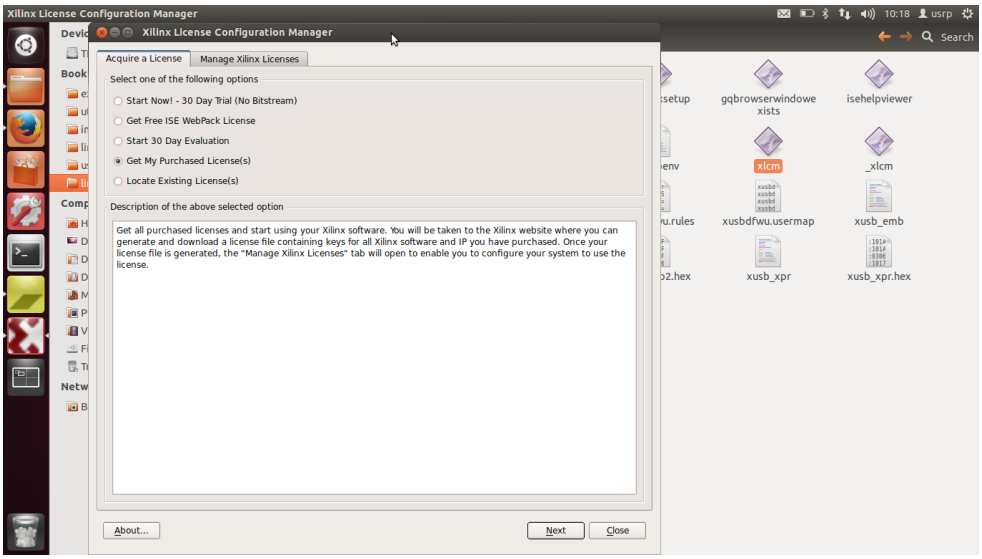

Fig 2.2 select suitable option of license

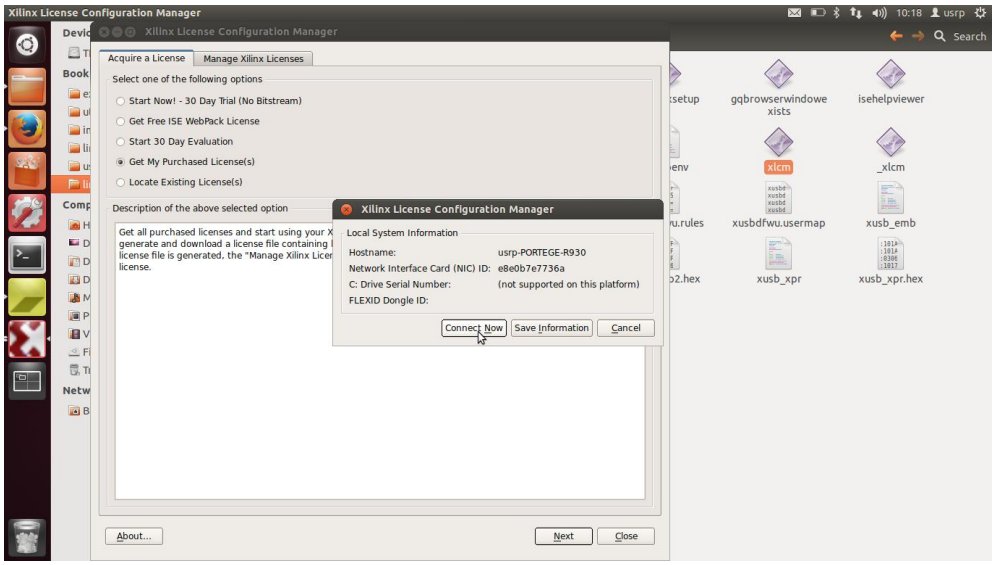

Fig 2.3 connect with server

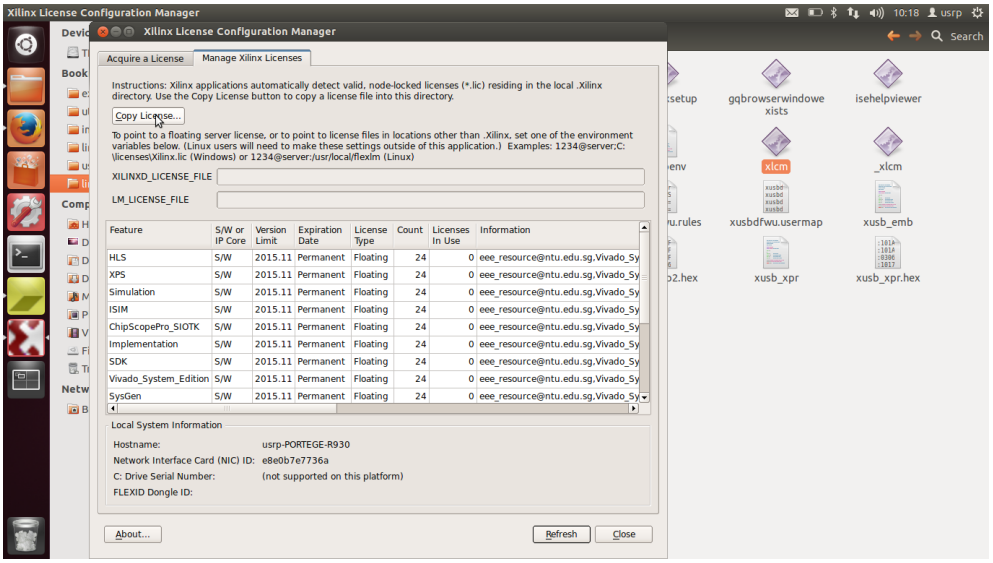

Fig 2.4 copy the license file

7. Then click on the **Copy License…** button and select the appropriate license file (refer fig 2.5)

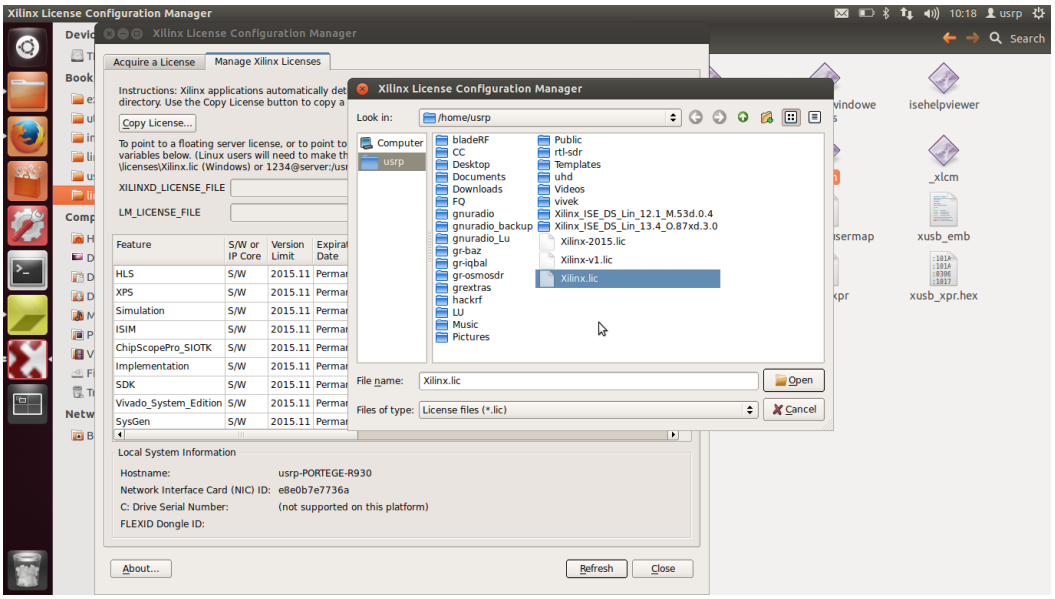

Fig 2.5 select the valid license file

For Windows:

Open the ISE project navigator and select **help -> Manage license… (Refer fig 2.6)**

After few seconds Xilinx License Configuration Manager Window should pop-up and then follow the steps as mentioned above (similar to Linux).

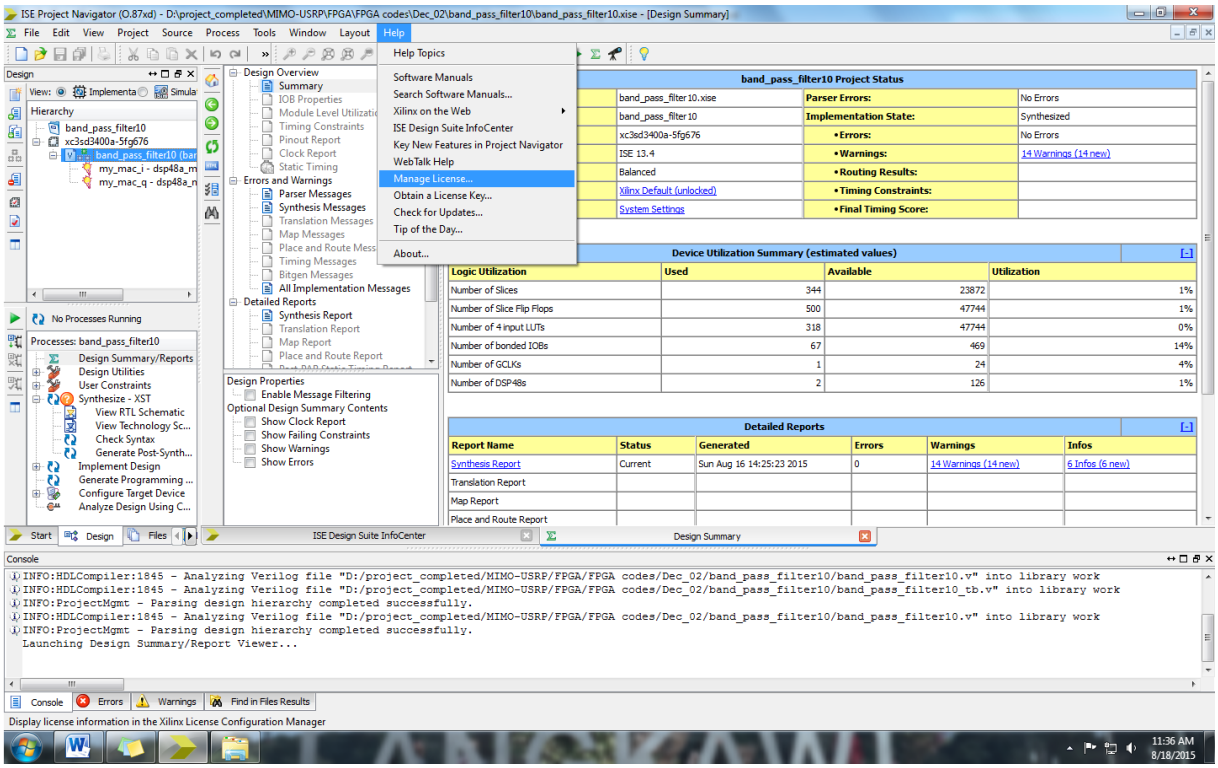

Fig 2.6 open Xilinx License Manage file