Tutorial-2

Introduction to IP cores with Xilinx ISE 13.4

Introduction:

In the world of digital design, engineers use Hardware Description Languages (HDL) to describe complex logic functions. These are included in design suites such as Xilinx's ISE and similar tools. However, if a digital engineer were to code an adder or run the multiply and accumulation each time they were doing a project; it would be reinventing the wheel and a waste of their time. Similarly, if the design engineer had to continually re-code commonly used complex digital circuits in large projects; they would end up wasting more time and money. Because of this, a digital design engineer may just use an IP core. An IP (Intellectual Property) core is a block of HDL code that other engineers have already written to perform a specific function. It is a specific piece of code designed to do a specific job. IP cores can be used in a complex design where an engineer wants to save time. Although they may simplify a given design, the engineer has to design the interfaces to send and receive data from this "*black box*". Xilinx cores are often beneficial to use as they are written by engineers with knowledge of the inner components of the FPGA. This allows them to be optimized for speed and resource.

Objective:

In this tutorial, the designer will get the answer for the following questions:

a) How to use Xilinx's CORE Generator System to generate IP cores to our HDL design?
b) How to instantiate the IP cores into a HDL design?
c) What are the benefits of using IP COREs into our HDL design?

Process:

1. Create customized cores by using the CORE Generator software system GUI
2. Instantiate cores into your HDL design
3. Run behavioral simulation on a design that contains cores

Implementation:

1. From the Project Navigator, select Project → **New Source**

2. Select **IP (CORE Generator & Architecture Wizard)** and enter a **Filename** (refer Figure1.1)

3. Click **Next** and then select the type of core (refer Figure1.2)

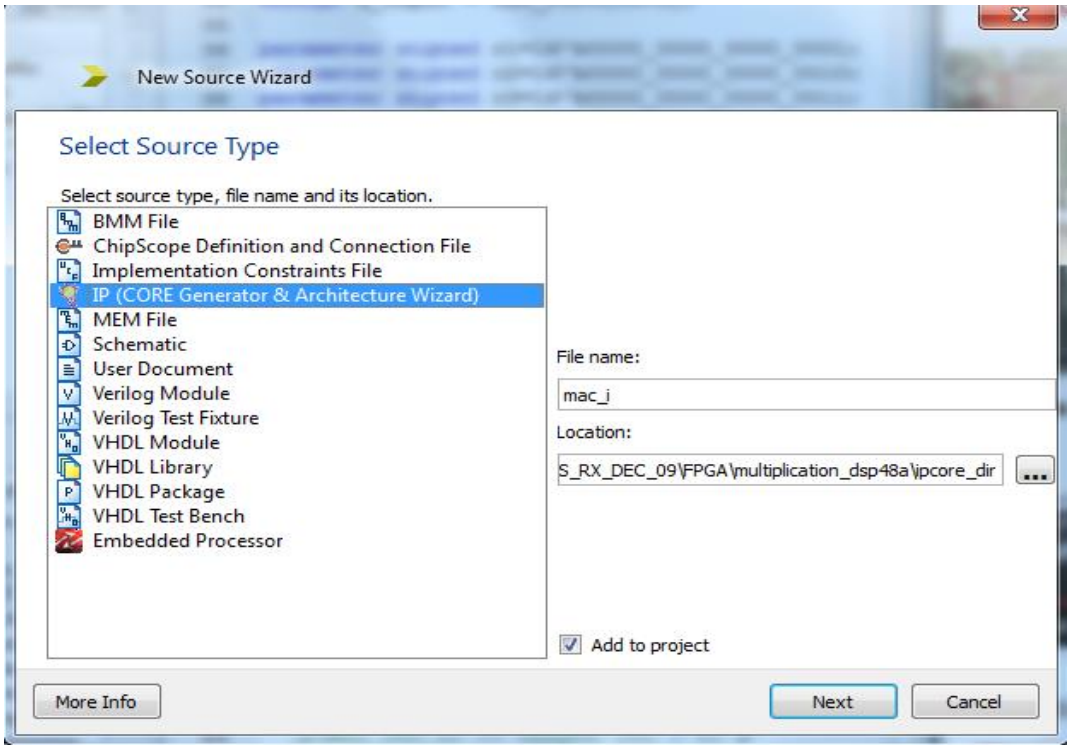

Figure 1.1 New Source Wizard (Select Source Type)

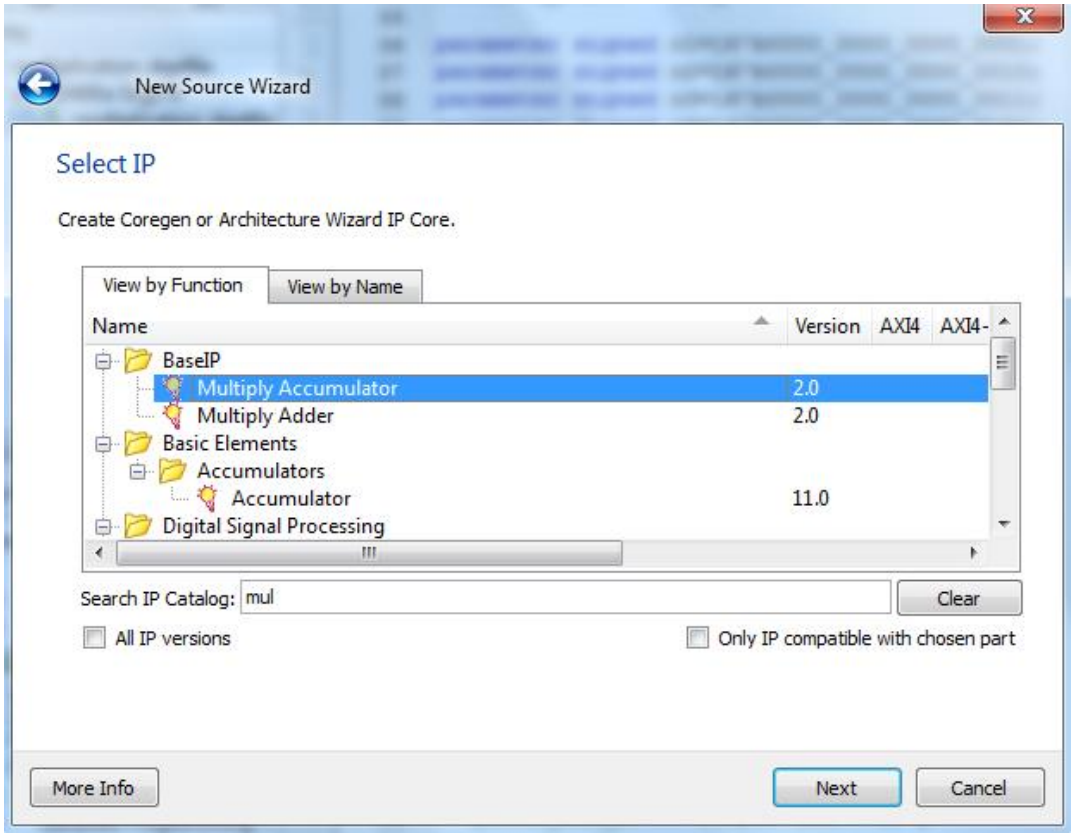

Figure 1.2 Select IP Core Type

4. After a few seconds a new window (LogiCore) should pop up. Customize the parameters for your design as you see in the figure below.

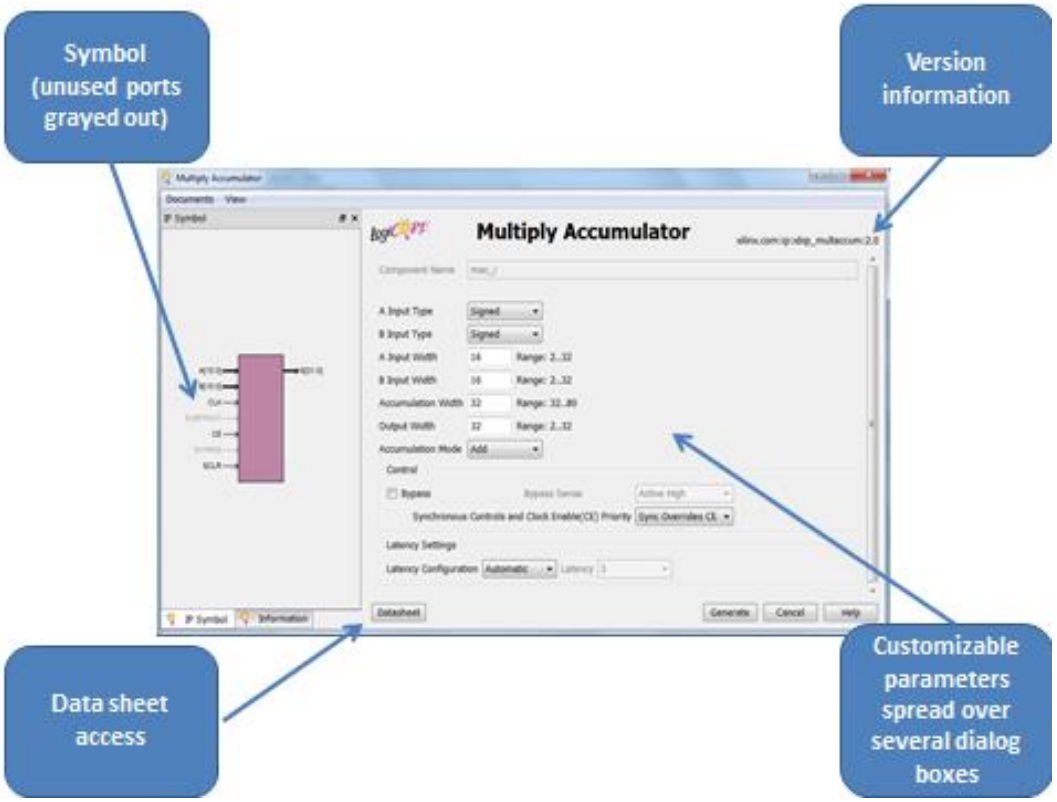

Figure 1.4 Core Customize Window

Take a minute to click on the Data Sheet… button on the bottom of the screen. The provided data sheets are essential in larger designs to understand many timing issues associated with a specific core as well as explaining all the different design choices.

When you create IP, the CORE Generator software produces a combination of the following files and places them in the specified directory for use in your ISE project:

- **XCO -** This file contains core options and parameters.
- **EDN/NGC -** This is the implementation netlist for the IP cores which output netlists. It is passed on to the Translate (NGDBuild) process.
- **SYM -** This schematic symbol is automatically generated for instantiating the IP in a schematic.
- **VHO or VEO template files -** These files are automatically generated for instantiating the IP in an HDL file.
- **VHD or V simulation wrapper files -** These files are provided for simulation of IP cores which output netlists.
- **VHD or V source-code files -** These files are the actual source-code required for both synthesis and simulation of IP cores which output source-code.
- **XISE, ISE, and GISE project files -** These files are used to help track and manage the core in the context of the ISE project. You should *not* need to interact directly with these files.

By default, when you create a new CORE Generator core, the core files are placed in a subdirectory of the main project directory called ***ipcore_dir***. If necessary, you can specify a different location in the New Source Wizard when you create the core.

It will take a few moments to generate all of the files. Progress made can be seen by looking at the messages in the Transcript window. When it is finished, core will be shown in the sources window inside the Project Navigator.

Instantiate CORE Generator IP in an HDL File:

1. Select the core file (.xco file) located in the source window then the contents in the process window will change to CORE Generator.
2. By expanding the CORE Generator we can find the HDL instantiation template file (VEO or VHO) then cut and paste the template into your HDL design (refer figure 1.4).

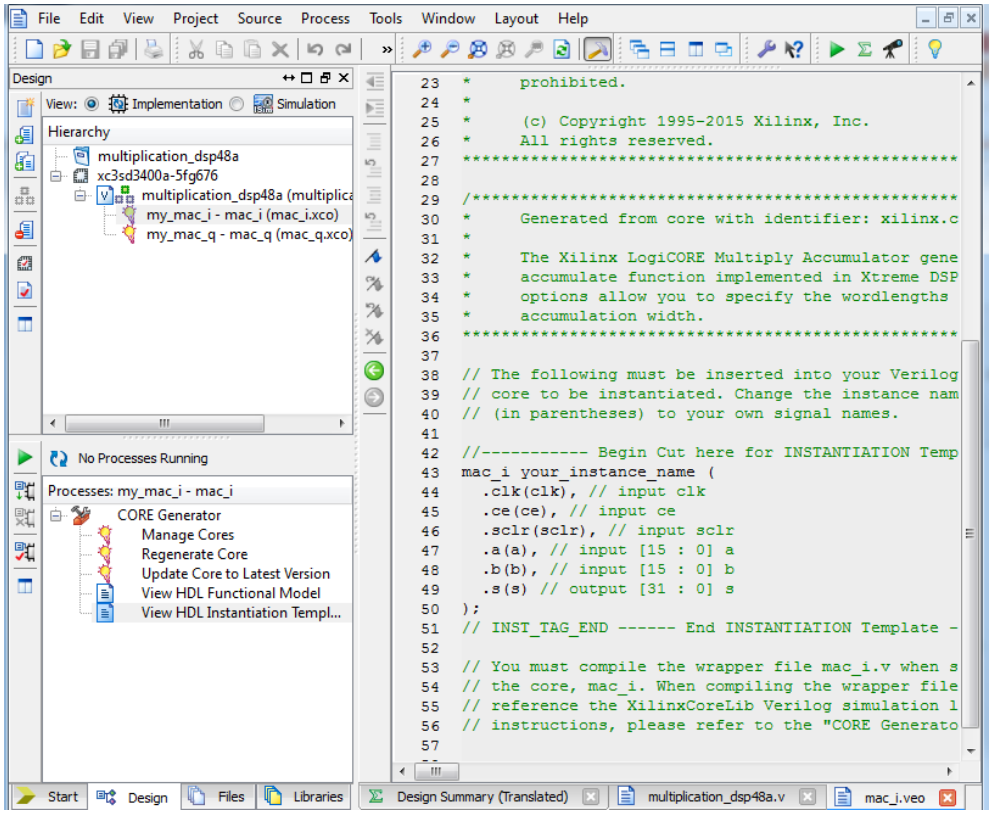

Figure 1.4 Instantiation template file

3. The design is ready for synthesis and implementation.

4. The ISE software automatically uses wrapper files when IP cores are present in the design.