Clocking and power control functions

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Clocking and Power Management

- The following slides describe
  - The generation of the various clocks needed by the LPC1768, and
  - The options of clock source selection, as well as power control and wake-up from reduced power modes
- Functions described in the following include:
  - Oscillators
  - Clock source selection
  - PLLs
  - Dividers
  - External clock output
  - Power control
  - Wake-up timer.

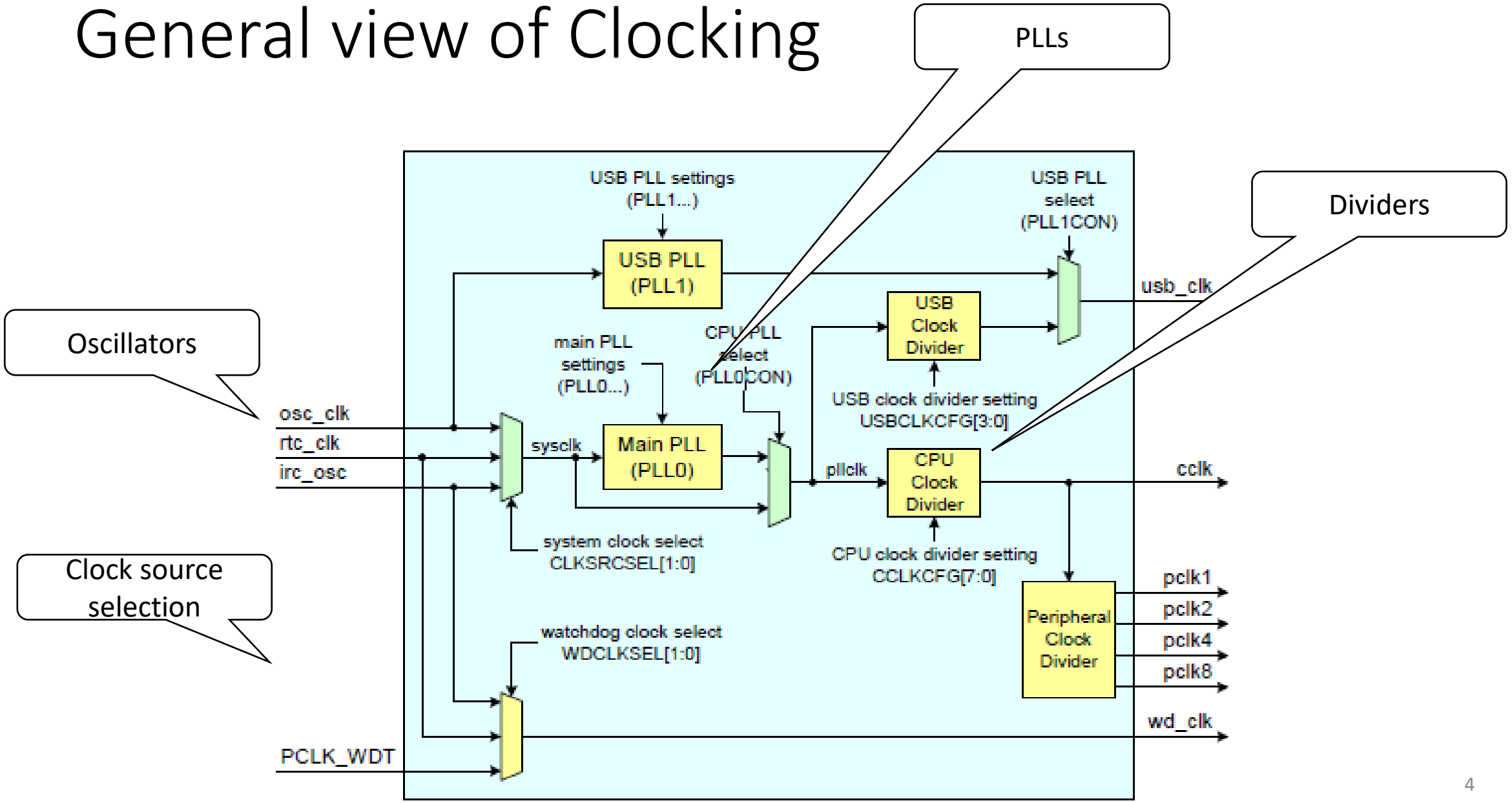
System Control Registers (pg. 31)

- It is a set of registers devoted to setup and control
  - Clock related functionalities
  - Power control features

Table 14. Summary of system control registers

Name	Description	Access	Reset value	Address
Clock source selection				
CLKSRCSEL	Clock Source Select Register	R/W	0	0x400F C10C
Phase Locked Loop (PLL0, Main PLL)				
PLL0CON	PLL0 Control Register	R/W	0	0x400F C080
PLL0CFG	PLL0 Configuration Register	R/W	0	0x400F C084
PLL0STAT	PLL0 Status Register	RO	0	0x400F C088
PLL0FEED	PLL0 Feed Register	WO	NA	0x400F C08C
Phase Locked Loop (PLL1, USB PLL)				
PLL1CON	PLL1 Control Register	R/W	0	0x400F C0A0
PLL1CFG	PLL1 Configuration Register	R/W	0	0x400F C0A4
PLL1STAT	PLL1 Status Register	RO	0	0x400F C0A8
PLL1FEED	PLL1 Feed Register	WO	NA	0x400F C0AC
Clock dividers				
CCLKCFG	CPU Clock Configuration Register	R/W	0	0x400F C104
USBCLKCFG	USB Clock Configuration Register	R/W	0	0x400F C108
PCLKSEL0	Peripheral Clock Selection register 0.	R/W	0	0x400F C1A8
PCLKSEL1	Peripheral Clock Selection register 1.	R/W	0	0x400F C1AC
Power control				
PCON	Power Control Register	R/W	0	0x400F C0C0
PCONP	Power Control for Peripherals Register	R/W	0x03BE	0x400F C0C4
Utility				
CLKOUTCFG	Clock Output Configuration Register	R/W	0	0x400F C1C8

General view of Clocking



Oscillators

- The LPC176x/5x includes three independent oscillators.
  - The Main Oscillator,
  - The Internal RC Oscillator,
  - The RTC oscillator
- Each oscillator can be used for more than one purpose as required in a particular application
- Following Reset, the LPC176x/5x will operate from the Internal RC Oscillator until switched by software
- This allows systems to operate without any external crystal, and allows the boot loader code to operate at a known frequency.

Oscillators – Internal oscillator

- The Internal RC Oscillator (IRC) may be used as the clock source for the watchdog timer, and/or as the clock that drives PLL0 and subsequently the CPU
- The nominal IRC frequency is 4 MHz
- Upon power-up or any chip reset, the LPC176x/5x uses the IRC as the clock source
- Software may later switch to one of the other available clock sources.

Oscillators – Main oscillator

- The main oscillator can be used as the clock source for the CPU, with or without using PLL0.
- The main oscillator operates at frequencies of 1 MHz to 25 MHz
- This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the Main PLL (PLL0)
- The oscillator output is called OSC_CLK
- The clock selected as the PLL0 input is PLLCLKIN and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations.

Oscillators - RTC oscillator

- The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be used as the clock source for PLL0 and CPU and/or the watchdog timer.
- ***Remark from the user manual:*** *The RTC oscillator must not be used as a clock source when the PLL0 output is selected to drive the USB controller; in this case select the main oscillator as clock source for PLL0 (see also Table 17).*

Clock Source Selection

- Several clock sources may be chosen to drive PLL0 and ultimately the CPU and on-chip peripheral devices. The clock sources available are
  - main oscillator
  - RTC oscillator
  - the Internal RC oscillator.

Table 17. Clock Source Select register (CLKSRCSEL - address 0x400F C10C) bit description

Bit	Symbol	Value	Description	Reset value
1:0	CLKSRC		Selects the clock source for PLL0 as follows:	0
		00	Selects the Internal RC oscillator as the PLL0 clock source (default).	
		01	Selects the main oscillator as the PLL0 clock source. **Remark**: Select the main oscillator as PLL0 clock source if the PLL0 clock output is used for USB or for CAN with baudrates > 100 kBit/s.	
		10	Selects the RTC oscillator as the PLL0 clock source.	
		11	Reserved, do not use this setting.	
		Warning: Improper setting of this value, or an incorrect sequence of changing this value may result in incorrect operation of the device.		
31:2	-	0	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Phase Locked Loop - PLLs

- PLLs are hardware component able to increase a given input frequency to a higher frequency
- In the LPC1768 there are 2 PLLs, namely PLL0 and PLL1.

PLL0 and PLL1

- PLL0 accepts an input clock frequency in the range of 32 kHz to 50 MHz and can produce a clock up to the maximum allowed for the CPU, which is 100 MHz.
- The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU, peripherals, and optionally the USB subsystem
  - Note that the USB subsystem has its own dedicated PLL1
- PLL1 receives its clock input from the main oscillator only and can be used to provide a fixed 48 MHz clock only to the USB subsystem.

Dividers

- The output of the PLL0 must be divided down for use by the CPU and the USB subsystem (if used with PLL0).
- Separate dividers are provided such that the CPU frequency can be determined independently from the USB subsystem.

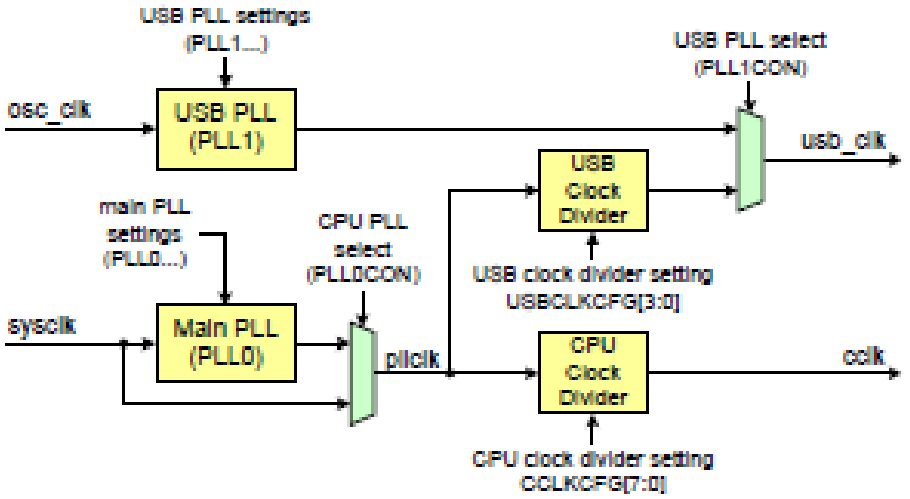


Fig 11. PLLs and clock dividers

Power Control general concepts

- The LPC176x/5x supports a variety of power control features:
  - Sleep mode,
  - Deep Sleep mode,
  - Power-down mode,
  - Deep Power-down mode.
- In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application.

System Control Register

- The SCR belongs to the core peripherals
- The SCR controls features of entry to and exit from low power state
- DO NOT USE SLEEPDEEP WHEN BEGUGGING.

Table 662. SCR bit assignments

Bits	Name	Function
[31:5]	-	Reserved.
[4]	SEVONPEND	Send Event on Pending bit: 0 = only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded 1 = enabled events and all interrupts, including disabled interrupts, can wakeup the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	-	Reserved.
[2]	SLEEPDEEP	Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = sleep 1 = deep sleep.
[1]	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = do not sleep when returning to Thread mode. 1 = enter sleep, or deep sleep, on return from an ISR. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	-	Reserved.

Debug Notes……

33.5 Debug Notes

Important: The user should be aware of certain limitations during debugging. The most important is that, due to limitations of the Cortex-M3 integration, the LPC176x/5x cannot wake up in the usual manner from Deep Sleep and Power-down modes. It is recommended not to use these modes during debug.

Macro Sequence too long
Internal driver error. Please report it to our support group.

Parameter Error
Internal driver error. Please report it to our support group.

JTAG

JTAG Communication Failure
JTAG communication is corrupted. Target JTAG interface is not working properly. Mainly caused by the target: debug block not powered or clocked properly. Avoid Deep-Sleep modes while debugging. Lower the Max Clock frequency in the **Target Driver Setup - Debug** dialog.

JTAG Device Chain Error
Devices on the JTAG chain do not meet the requirements, or the JTAG chain is not configured properly. Refer to Chaining Multiple Targets.

No Cortex-M Device found in JTAG chain
No Cortex-M processor-based device detected (using JTAG). Device is not connected, not powered, or the debug interface is not working. Enable the **SWJ** switch in the ULINK USB-JTAG/SWD Adapter section of the **Target Driver Setup - Debug** dialog.

No JTAG Devices Found
No JTAG device has been detected. Target not connected or not powered, or JTAG interface is not working.

Too Many JTAG Devices in Chain
Either too many JTAG devices have been detected in the chain (maximum 64 devices are allowed), or the JTAG communication is corrupted and it behaves as if too many devices are present. Check if the target is powered. Check if the JTAG interface is working properly. Lower the Max Clock frequency in the **Target Driver Setup - Debug** dialog.

No ARM Device found in JTAG chain
No ARM7/ARM9 processor-based device detected (using JTAG). Device is not connected, not powered, or the debug interface is not working. Check the connections, or try a manual RESET.

Serial Wire Debug

No Cortex-M SW Device Found
No Cortex-M processor-based device detected (using Serial Wire). Device is not connected, or not powered, or the debug interface is not working. Enable the **SWJ** switch in the ULINK USB-JTAG/SWD

Power Control registers

- They belong to the clock & power control group
- The Power Control function uses 2 registers
  - PCON – Power CONtrol register
  - PCONP – Power CONtrol for Peripherals.

Table 43. Power Control registers

Name	Description	Access	Reset value[1]	Address
PCON	Power Control Register. This register contains control bits that enable some reduced power operating modes of the LPC176x/5x. See Table 44.	R/W	0x00	0x400F C0C0
PCONP	Power Control for Peripherals Register. This register contains control bits that enable and disable individual peripheral functions, allowing elimination of power consumption by peripherals that are not needed.	R/W		0x400F C0C4

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

Instructions to entry in a reduced power state

- Entry to any reduced power mode begins with the execution of either a WFI (Wait For Interrupt) or WFE (Wait For Exception) instruction by the Cortex-M3
- The Cortex-M3 internally supports two reduced power modes: Sleep and Deep Sleep.
  - These are selected by the SLEEPDEEP bit in the cortex-M3 System Control Register
- Power-down and Deep Power-down modes are selected by bits in the PCON register.

Power Mode Control register (PCON)

- Controls for some reduced power modes and other power related controls are contained in the PCON register
- The same register contains flags that indicate whether entry into each reduced power mode actually occurred

Table 44. Power Mode Control register (PCON - address 0x400F C0C0) bit description

Bit	Symbol	Description	Reset value
0	PM0	Power mode control bit 0. This bit controls entry to the Power-down mode. See Section 4.8.7.1 below for details.	0
1	PM1	Power mode control bit 1. This bit controls entry to the Deep Power-down mode. See Section 4.8.7.1 below for details.	0
2	$\overline{\text{BODRPM}}$	Brown-Out Reduced Power Mode. When BODRPM is 1, the Brown-Out Detect circuitry will be turned off when chip Power-down mode or Deep Sleep mode is entered, resulting in a further reduction in power usage. However, the possibility of using Brown-Out Detect as a wake-up source from the reduced power mode will be lost. When 0, the Brown-Out Detect function remains active during Power-down and Deep Sleep modes. See the System Control Block chapter for details of Brown-Out detection.	0
3	$\overline{\text{BOGD}}$[1]	Brown-Out Global Disable. When BOGD is 1, the Brown-Out Detect circuitry is fully disabled at all times, and does not consume power. When 0, the Brown-Out Detect circuitry is enabled. See the System Control Block chapter for details of Brown-Out detection. **Note:** the Brown-Out Reset Disable (BORD, in this register) and the Brown-Out Interrupt (xx) must be disabled when software changes the value of this bit.	0
4	$\overline{\text{BORD}}$	Brown-Out Reset Disable. When BORD is 1, the BOD will not reset the device when the $V_{DD(REG)(3V3)}$ voltage dips goes below the BOD reset trip level. The Brown-Out interrupt is not affected. When BORD is 0, the BOD reset is enabled. See the Section 3.5 for details of Brown-Out detection.	0
7:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	SMFLAG	Sleep Mode entry flag. Set when the Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
9	DSFLAG	Deep Sleep entry flag. Set when the Deep Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
10	PDFLAG	Power-down entry flag. Set when the Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
11	DPDFLAG	Deep Power-down entry flag. Set when the Deep Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][4]
31:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Power Mode Control register (PCON)

- Controls for some reduced pow and other po controls are c the PCON reg
- The same reg contains flags indicate whether entry into each reduced power mode actually occurred

2-stage monitoring of the voltage on the VDD(REG)(3V3) pins. If this voltage falls below the BOD interrupt trip level (typically 2.2 V under nominal room temperature conditions), the BOD asserts an interrupt signal to the NVIC.

Table 44. Power Mode Control register (PCON - address 0x400F C0C0) bit description

Bit	Symbol	Description	Reset value
0	PM0	Power mode control bit 0. This bit controls entry to the Power-down mode. See Section 4.8.7.1 below for details.	0
1	PM1	Power mode control bit 1. This bit controls entry to the Deep Power-down mode. See Section 4.8.7.1 below for details.	0
2	BODRPM	Brown-Out Reduced Power Mode. When BODRPM is 1, the Brown-Out Detect circuitry will be turned off when chip Power-down mode or Deep Sleep mode is entered, resulting in a further reduction in power usage. However, the possibility of using Brown-Out Detect as a wake-up source from the reduced power mode will be lost. When 0, the Brown-Out Detect function remains active during Power-down and Deep Sleep modes. See the System Control Block chapter for details of Brown-Out detection.	0
3	BOGD[1]	Brown-Out Global Disable. When BOGD is 1, the Brown-Out Detect circuitry is fully disabled at all times, and does not consume power. When 0, the Brown-Out Detect circuitry is enabled. See the System Control Block chapter for details of Brown-Out detection. **Note:** the Brown-Out Reset Disable (BORD, in this register) and the Brown-Out Interrupt (xx) must be disabled when software changes the value of this bit.	0
4	BORD	Brown-Out Reset Disable. When BORD is 1, the BOD will not reset the device when the $V_{DD(REG)(3V3)}$ voltage dips goes below the BOD reset trip level. The Brown-Out interrupt is not affected. When BORD is 0, the BOD reset is enabled. See the Section 3.5 for details of Brown-Out detection.	0
7:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	SMFLAG	Sleep Mode entry flag. Set when the Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
9	DSFLAG	Deep Sleep entry flag. Set when the Deep Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
10	PDFLAG	Power-down entry flag. Set when the Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][3]
11	DPDFLAG	Deep Power-down entry flag. Set when the Deep Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [2][4]
31:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Encoding of Reduced Power Modes

- The PM1 and PM0 bits in PCON allow entering reduced power modes as needed.
- The encoding of these bits allows backward compatibility with devices that previously only supported Sleep and Power-down modes.

Table 45. Encoding of reduced power modes

PM1, PM0	Description
00	Execution of WFI or WFE enters either Sleep or Deep Sleep mode as defined by the SLEEPDEEP bit in the Cortex-M3 System Control Register.
01	Execution of WFI or WFE enters Power-down mode if the SLEEPDEEP bit in the Cortex-M3 System Control Register is 1.
10	Reserved, this setting should not be used.
11	Execution of WFI or WFE enters Deep Power-down mode if the SLEEPDEEP bit in the Cortex-M3 System Control Register is 1.

Sleep mode

- When Sleep mode is entered, the clock to the core is stopped, and the SMFLAG bit in PCON is set
- In Sleep mode, execution of instructions is suspended until either a Reset or an interrupt occurs.
  - Wake-up from Sleep mode will occur whenever any enabled interrupt occurs
- Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution.
- Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

Deep Sleep mode

- When the chip enters the Deep Sleep mode, the main oscillator is powered down, nearly all clocks are stopped, and the DSFLAG bit in PCON is set
- The IRC remains running and can be configured to drive the Watchdog Timer, allowing the Watchdog to wake up the CPU
- The 32 kHz RTC oscillator is not stopped and RTC interrupts may be used as a wake-up source
- The PLLs are automatically turned off and disconnected
  - The CCLK and USBCLK clock dividers automatically get reset to zero
- The FLASH memory is left in the standby mode allowing a quick wake-up.

Deep Sleep mode (II)

- Since all dynamic operation of the chip is suspended, Deep Sleep mode reduces chip power consumption to a very low value
- The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep Sleep mode and the logic levels of chip pins remain static
- The Deep Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks
  - For example, Wake-up from Deep Sleep mode can be brought about by NMI or External Interrupts EINT0 through EINT3.

Power-down mode and Deep Power-down mode

- Power-down mode does everything that Deep Sleep mode does, but also turns off the flash memory.
  - This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished
  - Entry to Power-down mode causes the PDFLAG bit in PCON to be set
- In Deep Power-down mode, power is shut off to the entire chip with the exception of the Real-Time Clock, the RESET pin, the WIC, and the RTC backup registers
  - Entry to Deep Power-down mode causes the DPDFLAG bit in PCON to be set.

Peripheral power control

- A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings
- This is detailed in the description of the PCONP register.

Power Control for Peripherals register (PCONP)

- The PCONP register allows turning off selected peripheral functions for the purpose of saving power
- This is accomplished by gating off the clock source to the specified peripheral blocks
- A few peripheral functions cannot be turned off (i.e., the Watchdog timer, the Pin Connect block, and the System Control block)
- Some peripherals, particularly those that include analog functions, may consume power that is not clock dependent
- These peripherals may contain a separate disable control that turns off additional circuitry to reduce power.
- Information on peripheral specific power saving features may be found in the user manual chapter describing that peripheral.

PCONP register (II)

- Each bit in PCONP controls one peripheral
  - If a peripheral control bit is 1, that peripheral is enabled
  - If a peripheral control bit is 0, that peripheral's clock is disabled (gated off) to conserve power
  - For example if bit 19 is 1, the I2C1 interface is enabled. If bit 19 is 0, the I2C1 interface is disabled
- Power saving oriented systems should have 1s in the PCONP register only in positions that match peripherals really used in the application
- Important: valid read from a peripheral register and valid write to a peripheral register is possible only if that peripheral is enabled in the PCONP register.

Table 46. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

Bit	Symbol	Description	Reset value
0	-	Reserved.	NA
1	PCTIM0	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	-	Reserved.	NA
6	PCPWM1	PWM1 power/clock control bit.	1
7	PCI2C0	The I^2C0 interface power/clock control bit.	1
8	PCSPI	The SPI interface power/clock control bit.	1
9	PCRTC	The RTC power/clock control bit.	1
10	PCSSP1	The SSP 1 interface power/clock control bit.	1
11	-	Reserved.	NA
12	PCADC	A/D converter (ADC) power/clock control bit. **Note:** Clear the PDN bit in the AD0CR before clearing this bit, and set this bit before setting PDN.	0
13	PCCAN1	CAN Controller 1 power/clock control bit.	0
14	PCCAN2	CAN Controller 2 power/clock control bit.	0
15	PCGPIO	Power/clock control bit for IOCON, GPIO, and GPIO interrupts.	1
16	PCRIT	Repetitive Interrupt Timer power/clock control bit.	0
17	PCMCPWM	Motor Control PWM	0
18	PCQEI	Quadrature Encoder Interface power/clock control bit.	0
19	PCI2C1	The I^2C1 interface power/clock control bit.	1
20	-	Reserved.	NA
21	PCSSP0	The SSP0 interface power/clock control bit.	1
22	PCTIM2	Timer 2 power/clock control bit.	0
23	PCTIM3	Timer 3 power/clock control bit.	0
24	PCUART2	UART 2 power/clock control bit.	0
25	PCUART3	UART 3 power/clock control bit.	0
26	PCI2C2	I2C interface 2 power/clock control bit.	1