31 Agosto 2021 – Architetture dei Sistemi di Elaborazione

Nome, MATRICOLA ……………………………………………………………………………

Considerando il processore MIPS64 e l'architettura descritta in seguito:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP multiplier unit: pipelined 8 stages
- FP arithmetic unit: pipelined 4 stages
- FP divider unit: not pipelined unit that requires 10 clock cycles
- branch delay slot: 1 clock cycle, and the branch delay slot disabled
- forwarding enabled
- it is possible to complete instruction EXE stage in an out-of-order fashion.

Usando il frammento di codice riportato, si calcoli il tempo di esecuzione dell'intero programma in colpi di clock e si completi la seguente tabella.

```
;    for (i = 0; i < 100; i++) {
;         v5[i] = v1[i]/v2[i];
;         v6[i] = (v1[i]*v2[i])+(v3[i]/v4[i]);
;}
```

.data																																												Clock cycles
V1: .double "100 values"																																												
V2: .double "100 values"																																												
V3: .double "100 values" … V5: .double "100 zeros"																																												
V4: .double "100 values"																																												
V5: .double "100 values"																																												
V6: .double "100 values"																																												
.text																																												
main: daddui r1,r0,0	F	D	E	M	W																																							5
daddui r2,r0,100		F	D	E	M	W																																						1
loop: l.d f1,v1(r1)			F	D	E	M	W																																					1…2
l.d f2,v2(r1)				F	D	E	M	W																																				1
l.d f3,v3(r1)					F	D	E	M	W																																			1
l.d f4,v4(r1)						F	D	E	M	W																																		1
div.d f5,f1,f2							F	D	/	/	/	/	/	/	/	/	/	/	M	W																								10

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s.d f5,v5(r1)								F	D	E	S	S	S	S	S	S	S	S	S	M	W																							1
mul.d f5,f1,f2									F	D	S	S	S	S	S	S	S	S	S	*	*	*	*	*	*	*	*	M	W															8
div.d f6,f3,f4										F	S	S	S	S	S	S	S	S	S	D	/	/	/	/	/	/	/	/	/	/	M	W												3
add.d f1,f5,f6																				F	D	S	S	S	S	S	S	S	S	S	+	+	+	+	M	W								4
s.d f1,v6(r1)																					F	S	S	S	S	S	S	S	S	S	D	E	S	S	S	M	W							1
daddui r1,r1,8																															F	D	S	S	S	E	M	W						1
daddi r2,r2,-1																																F	S	S	S	D	E	M	W					1
bnez r2,loop																																				F	S	D	E	M	W			2
halt																																						F	N	N	N	N		0…1
Total	**6 + 100 * 36**																																											**3606**

Please consider an optimization of 3CC for the DIV: 7CC instead of 10CC to execute.

.data																																												Clock cycles
V1: .double “100 values”																																												
V2: .double “100 values”																																												
V3: .double “100 values” … V5: .double “100 zeros”																																												
V4: .double “100 values”																																												
V5: .double “100 values”																																												
V6: .double “100 values”																																												
.text																																												
main: daddui r1,r0,0	F	D	E	M	W																																							5

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	daddui r2,r0,100		F	D	E	M	W																																								1
loop:	l.d f1,v1(r1)			F	D	E	M	W																																					1…2
	l.d f2,v2(r1)				F	D	E	M	W																																				1
	l.d f3,v3(r1)					F	D	E	M	W																																			1
	l.d f4,v4(r1)						F	D	E	M	W																																		1
	div.d f5,f1,f2							F	D	/	/	/	/	/	/	/	M	W																											10 → 7
	s.d f5,v5(r1)								F	D	E	S	S	S	S	S	S	M	W																										1
	mul.d f5,f1,f2									F	D	S	S	S	S	S	S	*	*	*	*	*	*	*	*	M	W																		8
	div.d f6,f3,f4										F	S	S	S	S	S	S	D	/	/	/	/	/	/	/	S	M	W																	3 → 1
	add.d f1,f5,f6																	F	D	S	S	S	S	S	S	S	+	+	+	+	M	W													4
	s.d f1,v6(r1)																		F	S	S	S	S	S	S	S	D	E	S	S	S	M	W												1
	daddui r1,r1,8																										F	D	S	S	S	E	M	W											1
	daddi r2,r2,-1																											F	S	S	S	D	E	M	W										1
	bnez r2,loop																															F	S	D	E	M	W								2
	halt																																	F	N	N	N	N							0…1
	Total	**6 + 100 * 31**																																											**3106**

$$\text{SPEEDUP}_{\text{enhanced}} = \frac{10+3}{7+1} = 1.63 \quad \& \quad \text{FRACTION}_{\text{enhanced}} = \frac{100 \cdot (10+3)}{3606} = 0.36$$

$$\text{SPEEDUP}_{\text{computation}} = \frac{1}{\left(1 - \text{FRACTION}_{\text{enhanced}}\right) + \dfrac{\text{FRACTION}_{\text{enhanced}}}{\text{SPEEDUP}_{\text{enhanced}}}} = 1.16 \quad \& \quad \text{SPEEDUP}_{\text{observation}} = \frac{3606}{3106} \approx 1.16 \implies ✔$$

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Domanda 2

Considerando il programma precedente e l'architettura del processore superscalare descritto in seguito; completare la tabella relativa alle prime 2 iterazioni.
Processor architecture:

- Issue 2 instructions per clock cycle
- jump instructions require 1 issue
- handle 2 instructions commit per clock cycle
- timing facts for the following separate functional units:
    i. 1 Memory address 1 clock cycle
    ii. 1 Integer ALU 1 clock cycle
    iii. 1 Jump unit 1 clock cycle
    iv. 1 FP multiplier unit, which is pipelined: 8 stages
    v. 1 FP divider unit, which is not pipelined: 10 clock cycles
    vi. 1 FP Arithmetic unit, which is pipelined: 4 stages
- Branch prediction is always correct
- There are no cache misses
- There are 2 CDB (Common Data Bus).

# iteration		Issue	EXE	MEM	CDB x2	COMMIT x2
1	l.d f1,v1(r1)	1	2	3	4	5
1	l.d f2,v2(r1)	1	3	4	5	6
1	l.d f3,v3(r1)	2	4	5	6	7
1	l.d f4,v4(r1)	2	5	6	7	8
1	div.d f5,f1,f2	3	6	—	16	17
1	s.d f5,v5(r1)	3	6	—	—	17
1	mul.d f5,f1,f2	4	6	—	14	18
1	div.d f6,f3,f4	4	16	—	26	27
1	add.d f1,f5,f6	5	27	—	31	32
1	s.d f1,v6(r1)	5	7	—	—	32
1	daddui r1,r1,8	6	7	—	8	33

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1	daddi r2,r2,-1	6	8	—	9	33
1	bnez r2,loop	7	10	—	—	34
2	l.d f1,v1(r1)	8	9	10	11	34
2	l.d f2,v2(r1)	8	10	11	12	35
2	l.d f3,v3(r1)	9	11	12	13	35
2	l.d f4,v4(r1)	9	12	13	14	36
2	div.d f5,f1,f2	10	26	—	36	37
2	s.d f5,v5(r1)	10	13	—	—	37
2	mul.d f5,f1,f2	11	13	—	21	38
2	div.d f6,f3,f4	11	36	—	46	47
2	add.d f1,f5,f6	12	47	—	51	52
2	s.d f1,v6(r1)	12	14	—	—	52
2	daddui r1,r1,8	13	14	—	15	53
2	daddi r2,r2,-1	13	15	—	16	53
2	bnez r2,loop	14	17	—	—	54