AI-assisted Design and Synthesis of Continuous-Time ADCs

Internal Report#3
AIR-CHIP Project (PID2022-138078OB-I00)

Author
Francisco Gómez Pulido

Distribution List
Gustavo Liñán-Cembrano
Jose M. de la Rosa

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1 ΣΔM's architectures

Date: Febrary 07, 2025

1.1 Introduction

Let's consider the following scheme:

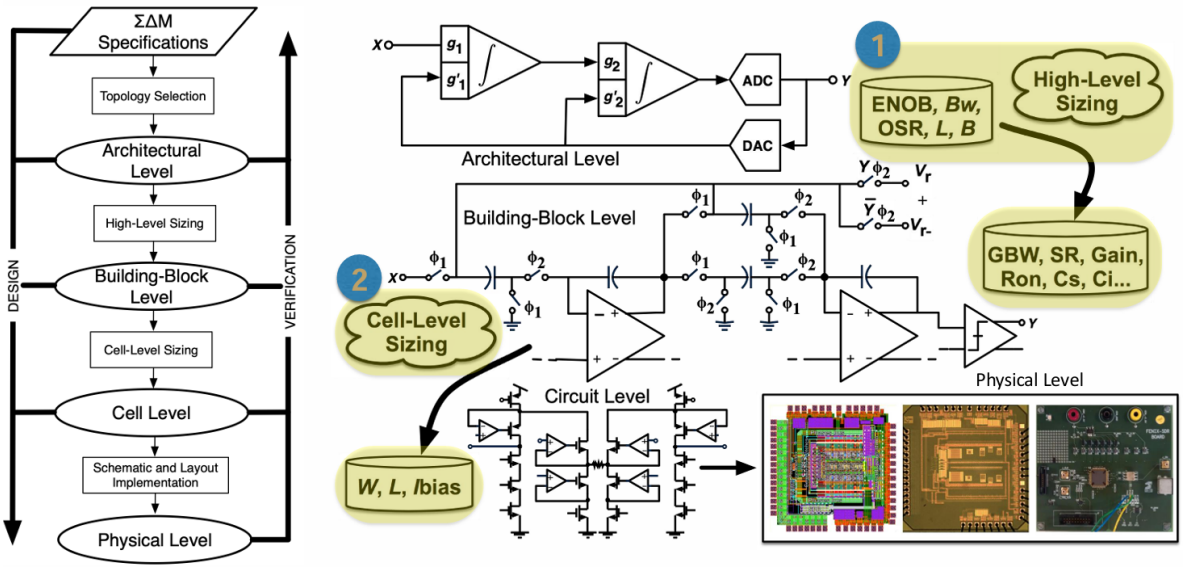

Figure 1: Main scheme of the project.

We are working on point 1, **high-level sizing**, which aims to move from the architecture level to the block level. To do this, we are given some specifications and variables, and we have to obtain the optimal design for the design variables. In the figure:

$$\{ENOB, B_W, OSR, L, B\} \implies \{GBW, SR, Gain, Ron, C_s, C_i\}$$

In this section, our purpose is to understand the main architectures of Sigma-Delta Modulators, and how they can be implemented.

1.2 Classification and taxonomy of ΣΔMs: basic architectures

Depending on some characteristics, we can classify the main architectures of ΣΔMs in the following categories:

1.2.1 Attending to the number of embedded quantizers

Single-loop or single-quantizer These have a single quantization stage and are generally simpler.

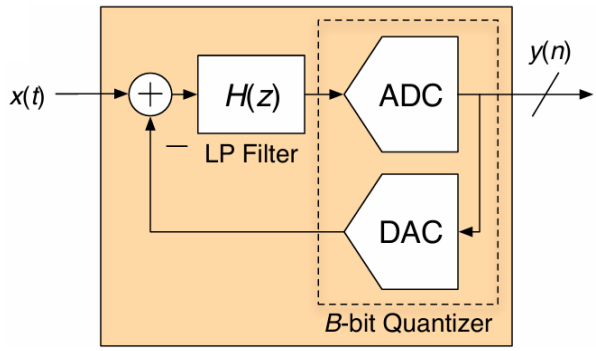

Figure 2: Single-loop or single-quantizer.

Multiple architectures exist where the ΣΔM is configured in different ways to optimize noise shaping and efficiency.

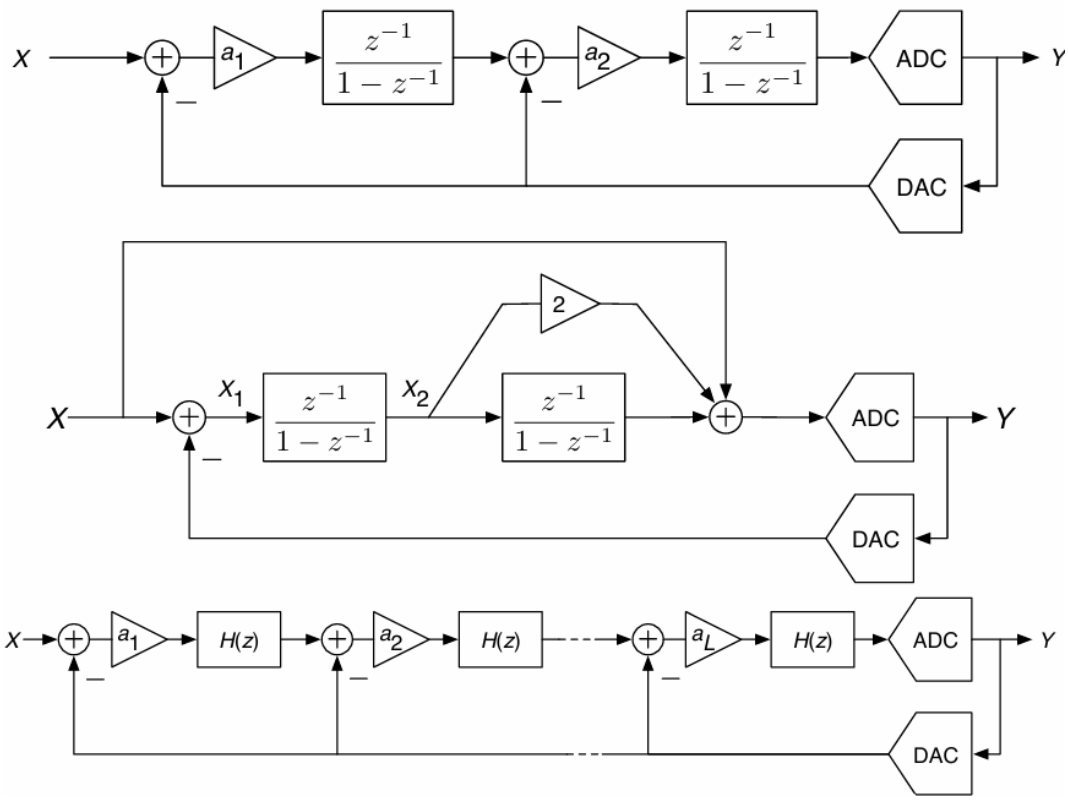

Figure 3: Multiple topologies of a single-loop or single-quantizer.

Cascade topologies These use multiple quantizers and digital cancellation logic to improve performance.

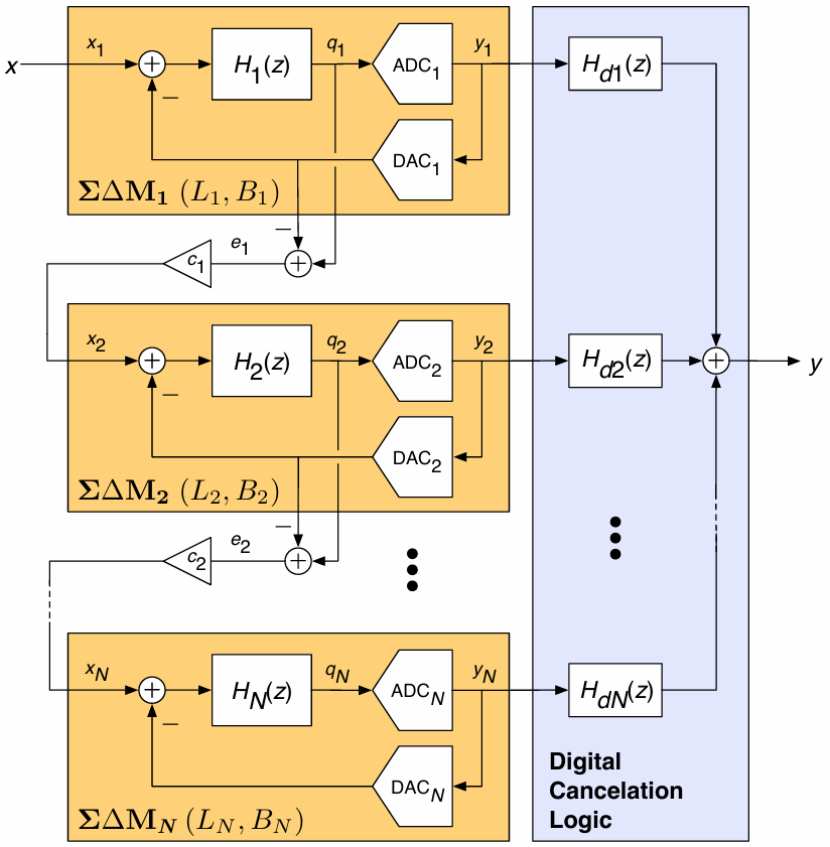

Figure 4: Cascade topologies.

1.2.2 Attending to the number of bits of the embedded quantizer

Single-bit ($B = 1$) Uses a simple 1-bit quantizer, which is easy to implement but has lower resolution.

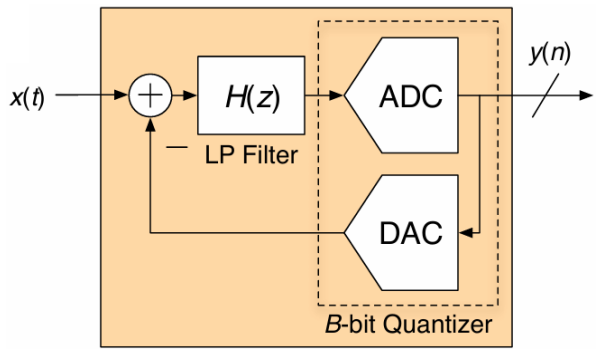

Figure 5: Single-bit.

Multi-bit ($B > 1$) Uses a higher-resolution quantizer, improving performance but increasing circuit complexity.

1.2.3 Attending to the nature of signals being converted

Low Pass (LP) Designed for signals with low-frequency content.

Band Pass (BP) Optimized for processing intermediate frequency (IF) signals, often used in radio receivers.

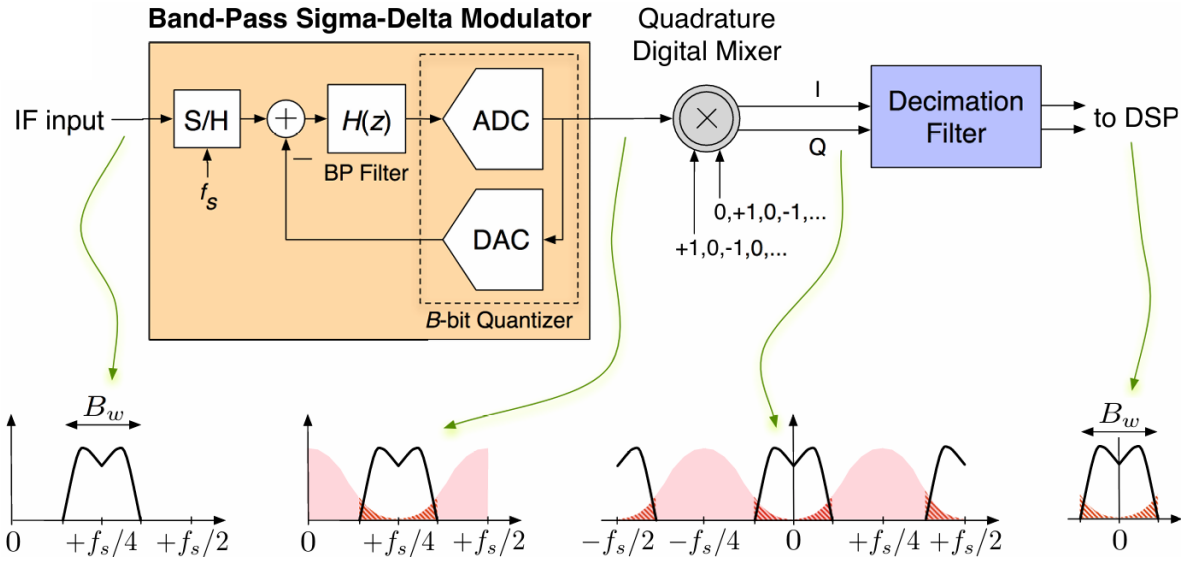

Figure 6: Band pass.

1.2.4 Attending to the nature of the loop-filter dynamics

Discrete-Time (DT) [usually Switched-Capacitor (SC)] Operate with sampled-data processing. Typically use Switched-Capacitor (SC) implementations. Instead of using resistors to process signals, SC circuits use capacitors and switches (clock-controlled switches) to perform operations like integration and amplification.

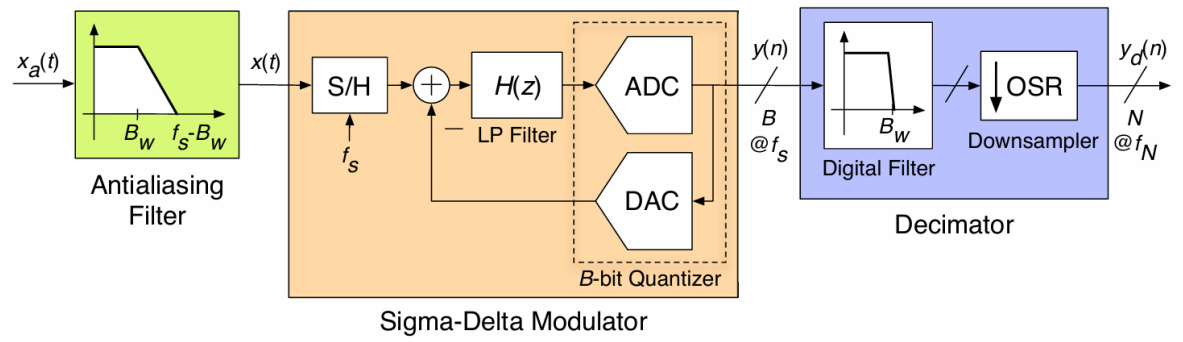

Figure 7: Discrete-Time (DT).

Continuous-Time (CT) [either Active-RC or Gm-C] Provide benefits like better anti-aliasing properties and higher bandwidth. Implemented using Active-RC or Gm-C filters.

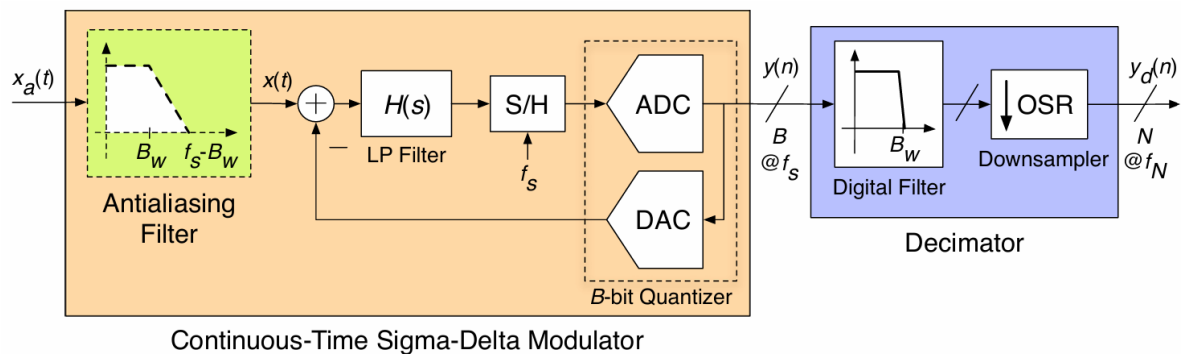

Figure 8: Continuous-Time (CT).

1.2.5 Summary

In summary, we have these kind of architectures:

- Attending to the number of quantizers:
  1. Single-loop
  2. Cascade
- Attending to the number of bits:
  1. Single-bit
  2. Multi-bit
- Attending to the nature of signals:
  1. Low Pass (LP)
  2. Band Pass (BP)
- Attending to the nature of the loop-filter:
  1. Discrete-Time (DT):
     (a) Switched-Capacitor (SC)
  2. Continuous-Time (CT)
     (a) Active-RC
     (b) Gm-C

1.3 SC Implementation of a 1st-order LP ΣΔM

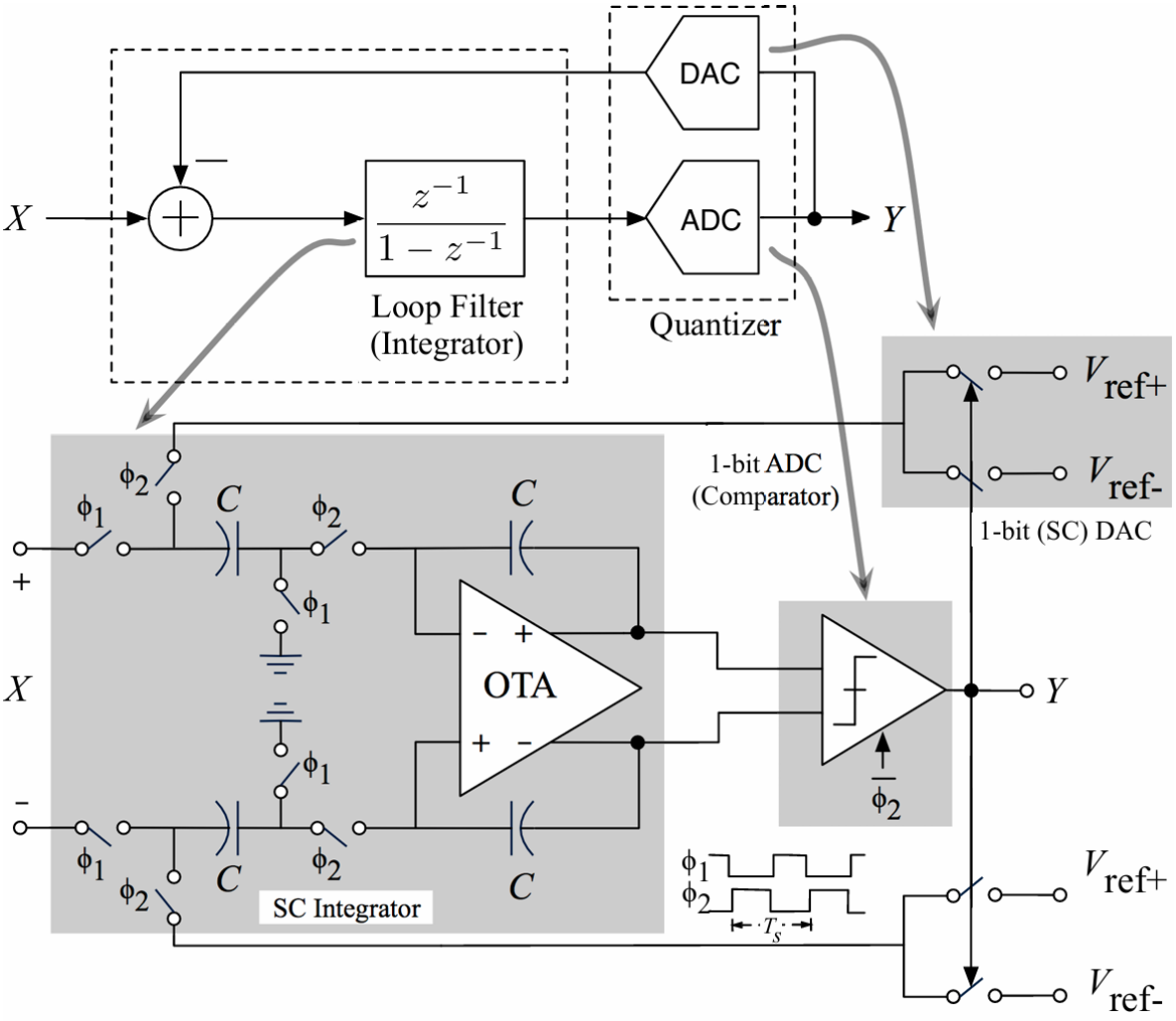

Figure 9: SC Implementation of a 1st-order LP ΣΔM.

Description of the circuit:

- **Loop Filter (Integrator SC)**. Its function is to **integrate** the input signal and feedback the quantization error. Components involved:
  - **Capacitors** C: store charge and enable integration.
  - **Switches** ϕ_1 and ϕ_2: alternate between charging and discharging capacitors in each clock cycle.
  - **Operational Transconductance Amplifier (OTA)**: acts like an integrator.

  During ϕ_1, the capacitor **charges** with the input signal, and during ϕ_2, the charge is **transferred to another capacitor**, accumulating the effect of previous samples (integration).
- **1-bit ADC (1-bit Quantizer - Comparator)**. This block **takes the integrated signal** and decides whether the output is 1 or 0 based on the signal magnitude. Components involved:

- **Comparator** (1-bit ADC): detects whether the signal is positive or negative.
- **Digital output**: only has two possible values: $+V_{ref}$ or $-V_{ref}$.

If the integrator output is positive, the ADC returns 1, and if it is negative, it returns 0.

- **1-bit DAC (Digital-to-Analog Converter)**. **Converts the digital output of the quantizer into an analog signal to feed back to the integrator**. If the ADC returns 1, the DAC generates $+V_{ref}$, and if the ADC returns 0, the DAC generates $-V_{ref}$. It corrects the quantization error by feeding back a corrected version of the signal and it improves the system's accuracy.
- **Feedback Loop**. The DAC's output is **subtracted from the input signal** in each cycle. This helps minimize quantization error.
- ϕ_1 **and** ϕ_2 are **clock signals** that control the **switches**. They are never active at the same time (not overlapping).
  - During ϕ_1 (**capacitor charging**), the capacitor charges with the input signal X. The integrator's output remains unchanged.
  - During ϕ_2 (**charge transfer**), the capacitor transfers its charge to the integrator. The integrator's output updates.

  The full cycle lasts T_s (**sampling period**), divided into ϕ_1 and ϕ_2. This mechanism enables signal processing without loss and ensures circuit stability.

1.4 SC Implementation of a 2nd-order ΣΔM

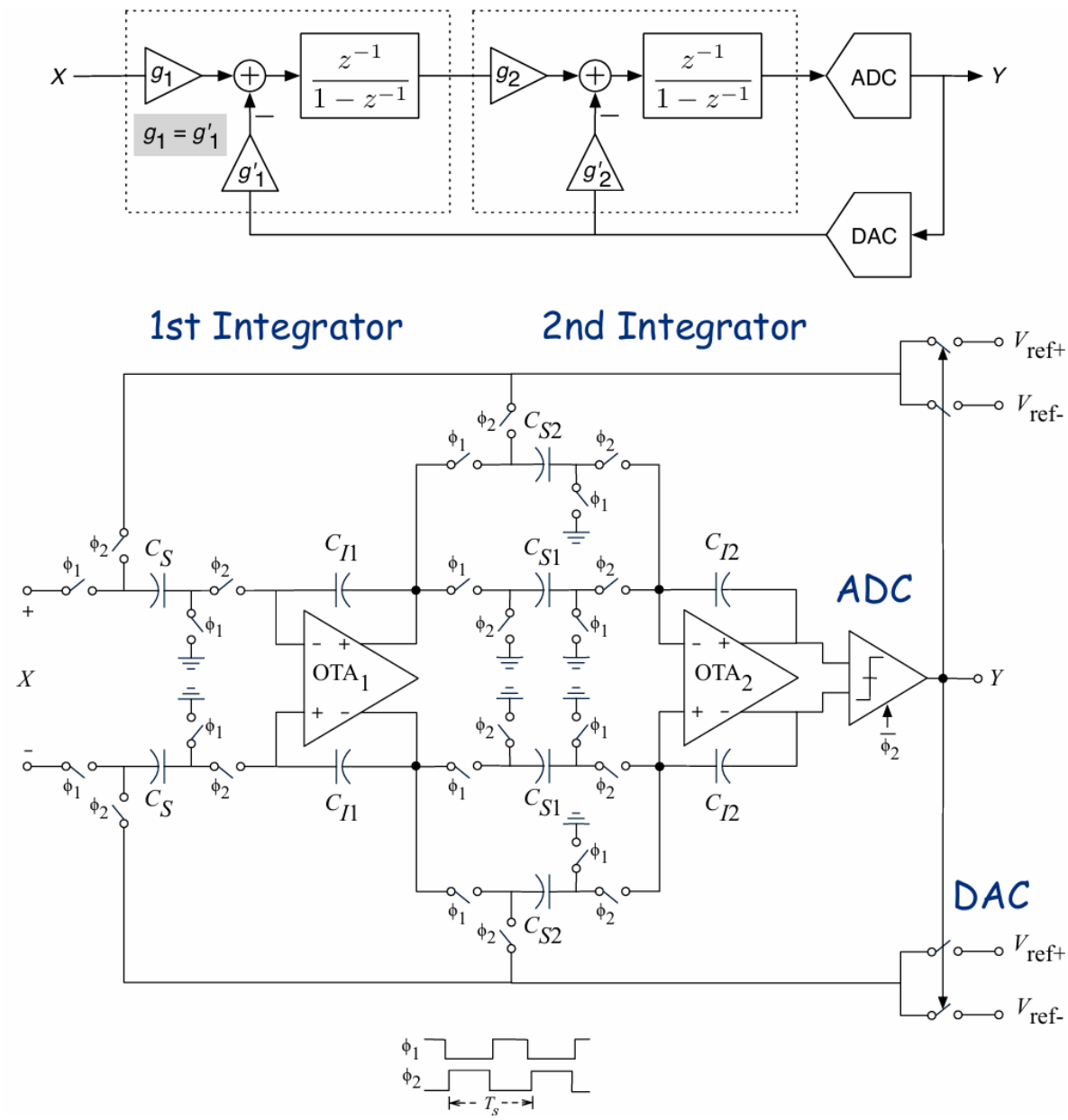

Figure 10: SC Implementation of a 2nd-order ΣΔM.

Description of the circuit:

- **Cascaded integrators (loop filter - two integration stages)**. The circuit has two cascaded SC integrators, meaning the signal undergoes two successive accumulations before being quantized. During ϕ_1 the first integrator accumulates the input signal, and during ϕ_2 the processed signal from the first integrator is transferred to the second integrator, accumulating even more information. At the end of the cycle, the signal is sent to the quantizer.
- **1-bit Quantizer (1-bit ADC - Comparator)**. It takes the integrated signal and decides

whether the output is 1 or 0 based on its magnitude. If the second integrator's output is positive, the ADC returns 1, and if it's negative, it returns 0.

- **1-bit DAC (Digital-to-Analog Converter - Feedback)**. Converts the quantizer's digital output into an analog signal to feed back into the integrator. If the ADC returns 1, the DAC generates $+V_{ref}$, and if the ADC returns 0, the DAC generates $-Vref$.
- **Feedback loop**. The DAC output is subtracted from the input signal in each cycle. This negative feedback minimizes quantization error by passing it through two integrations before quantization.

Step by step:

1. The analog input X enters the first SC integrator, where it accumulates.
2. The first integrator's output is sent to the second integrator, where it accumulates even more.
3. The 1-bit quantizer (ADC) decides whether the output is 1 or 0.
4. The DAC converts the digital output back into an analog signal $\pm V_{ref}$.
5. The DAC feeds back into the integrators, minimizing quantization error.
6. This process repeats in every clock cycle, generating a high-precision digital sequence.

1.5 Active-RC Implementation of a 2nd-order CT-ΣΔM

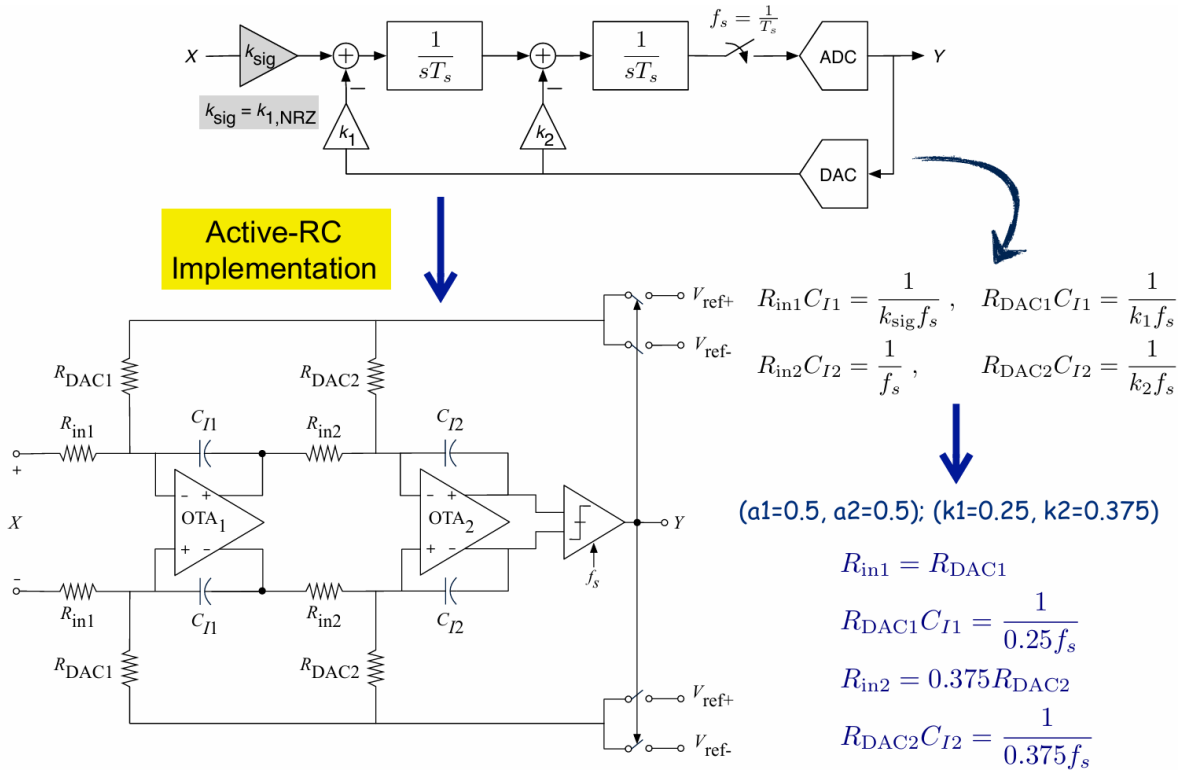

Figure 11: Active-RC Implementation of a 2nd-order CT-ΣΔM.

System level:

1. The input signal X is amplified by a factor k_{sig}.
2. It then passes through two cascaded integrators, each with feedback coefficient k_1 and k_2.
3. The integrated signal is digitized by a 1-bit ADC.
4. A 1-bit DAC converts the digital signal back to analog and feeds it back to the input.

Circuit level: to physically implement the model, an Active-RC architecture is used, based on:

- **Resistors** (R): control the current flow.
- **Capacitors** (C): store and release charge to implement integration.
- **Operational Transconductance Amplifiers** ($OTAs$): perform amplification and integration.

Description of the circuit:

1. **Integrator 1** (OTA_1): the input signal X passes through the resistor R_{in1}. It's stored in capacitor C_{I1}, which is connected to the input of OTA_1. The integrated signal is then fed into the second integrator.
2. **Integrator 2** (OTA_2): the output of first integrator passes through resistor R_{in2}. It is stored in capacitor C_2, connected to OTA_2. The output of this integrator is the signal that gets digitized by the ADC.
3. **DAC feedback**: the digital output is converted back to analog through resistors R_{DAC1} and R_{DAC2}. This generates a negative feedback signal, which helps reduce quantization noise.

The equations define the relationships between resistors and capacitors to ensure the circuit functions according to the mathematical model. Essentially, the resistors and capacitors implement the integration and feedback coefficients.

2 CT-ΣΔMs

Date: Febrary 11, 2025

2.1 Active-RC implementation in ΣΔMs

An Active-RC implementation uses **operational amplifiers** (OTA), **resistors** (R) and **capacitors** (C) to perform signal integration and filtering.

The fundamental integration principle is:

$$V_{\text{out}} = \frac{1}{sRC} V_{\text{in}}$$

This means that the circuit implements an **integrator**.

Example: Active-RC implementation 2nd-order CT-ΣΔM:

1. The modulator receives an analog input signal X, which is first fed into the first Active-RC integrator.

2. The signal passes through a resistor R_1, which converts the voltage input into a current:

$$I_{R1} = \frac{X}{R_1}$$

   This current charges the capacitor C_1, which is inside a feedback loop of an OTA. The OTA forces the circuit to behave as an ideal integrator, giving the output:

$$V_{\text{out1}} = -\frac{1}{sR_1C_1} X$$

   This first integration step smooths the input signal and shapes the noise spectrum.

3. The output of the first integrator is sent to a second Active-RC integrator, which follows the same principle:

$$V_{\text{out2}} = -\frac{1}{sR_2C_2} V_{\text{out1}}$$

4. The output of the second integrator is sent to a 1-bit quantizer (a comparator), which converts the analog signal into a digital one ($+1$ or -1):

$$Y = \text{sign}(V_{\text{out2}})$$

5. To minimize quantization error, the digital output is converted back into an analog signal using a DAC.

   Important: In Active-RC implementations, the feedback path uses resistors and capacitors to precisely inject the DAC signal into the integrators.

   This closes the feedback loop, ensuring stable operation and effective noise shaping.

2.2 Gm-C implementation in ΣΔMs

A Gm-C implementation uses **transconductors** (G_m) and **capacitors** (C) to perform signal integration, instead of operational amplifiers and resistors, as Active-RC.

A transconductor G_m is an electronic block that **converts a voltage signal into a proportional current**:

$$I_{\text{out}} = G_m V_{\text{in}}$$

This current is then integrated by a capacitor C, generating an output voltage:

$$V_{\text{out}} = \frac{1}{sC} I_{\text{out}} \implies V_{\text{out}} = \frac{G_m}{sC} V_{\text{in}}$$

This means the circuit implements an **integration function**, which is crucial in ΣΔMs.

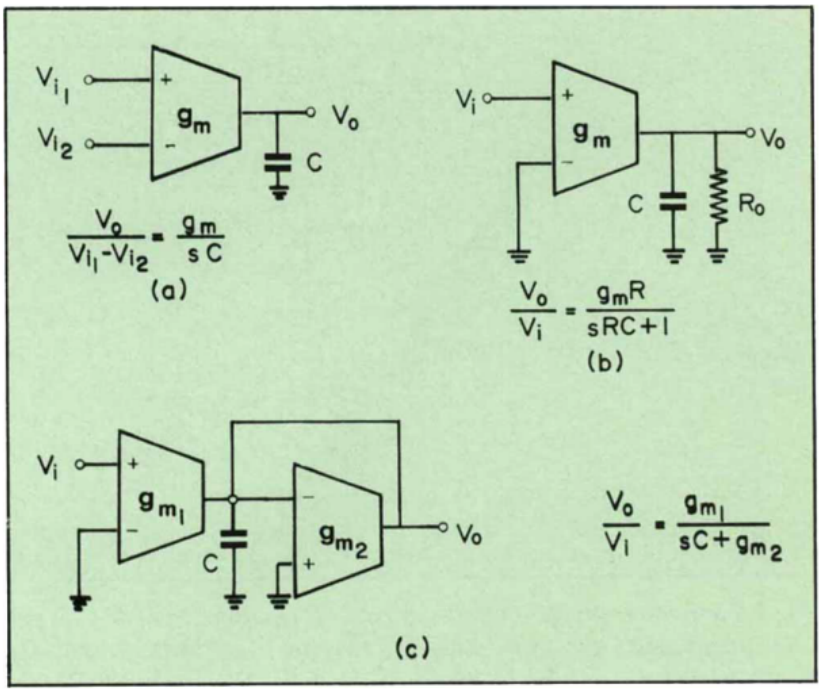

Fig. 4 Integrator structures. (a) Simple. (b) Lossy. (c) Adjustable.

Example: Gm-C implementation 2nd-order CT-ΣΔM:

1. The analog signal X is fed into the first Gm-C integrator. Instead of a resistor, a **transconductor** G_{m1} is used to convert the voltage signal into a proportional current:

$$I_{gm1} = G_{m1} X$$

2. The current generated by G_{m1} charges a capacitor C_1, performing the first integration:

$$V_{\text{out1}} = \frac{1}{sC_1} I_{\text{gm1}} \implies V_{\text{out1}} = \frac{G_{m1}}{sC_1} X$$

This means the first integrator attenuates high frequencies and accumulates the signal over time.

3. The output of the first integrator is sent to another transconductor G_{m2}, which again converts it into a current:

$$I_{gm2} = G_{m2} V_{\text{out1}}$$

This current charges a second capacitor C_2, performing a second integration:

$$V_{\text{out2}} = \frac{1}{sC_2} I_{\text{gm2}} \implies V_{\text{out2}} = \frac{G_{m2}}{sC_2} V_{\text{out1}}$$

The result is a second-order integration of the input signal, which further attenuates quantization noise.

4. The output of the second integrator is sent to a 1-bit **quantizer**, which converts the analog signal into a digital sequence ($+1$ or -1).

$$Y = \text{sign}(V_{\text{out2}})$$

5. To reduce quantization error, the digital output is converted back into an analog signal using a DAC.

Important: In the Gm-C implementation, DAC feedback also uses transconductors G_{mDAC1} and G_{mDAC2}, which inject a current proportional to the digital signal into the integrators.

This closes the feedback loop and helps filter quantization noise, improving system accuracy.

The system general equation is:

$$V_{\text{out2}} = \frac{G_{m2}}{sC_2} \left(\frac{G_{m1}}{sC_1} X \right) \tag{1}$$

3 Advanced ΣΔM's architectures

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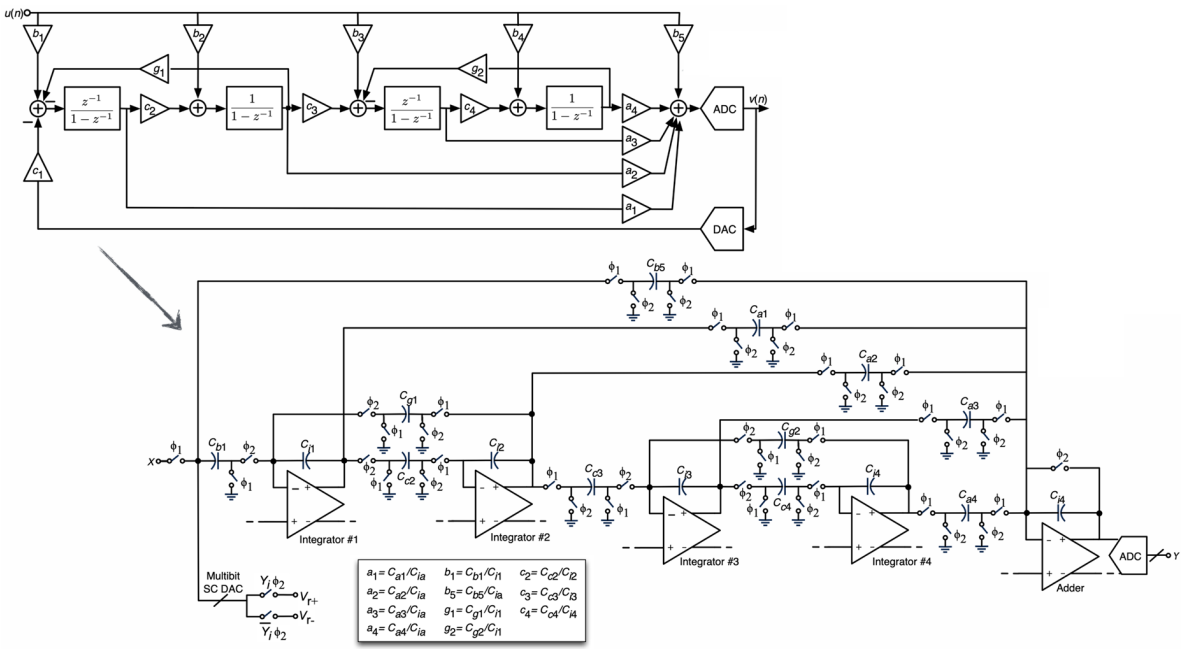

Figure 12: 4th-order CRFF LP/BP SC-ΣΔM with tunable notch.

Block diagram:

- The input signal $u(n)$ passes through a series of discrete-time integrators.
- Each integrator consists of a delay element z^{-1} and a transfer function $\frac{1}{1-z-1}$.
- A feedback loop, which helps shape the quantization noise.
- ADC and DAC enable the analog-to-digital conversion and feedback generation.

Circuit-level (SC) implementation:

- The modulator consists of four cascaded integrators implemented with OTA and capacitors.
- Several capacitor ratios define coefficients (a_1, b_1, c_1,...), which influence the noise transfer function.
- The feedback loop is implemented using a Multi-bit SC-DAC, which ensures high resolution and improves linearity.
- A tunable notch filter is incorporated, which allows flexibility in filtering specific frequency components.

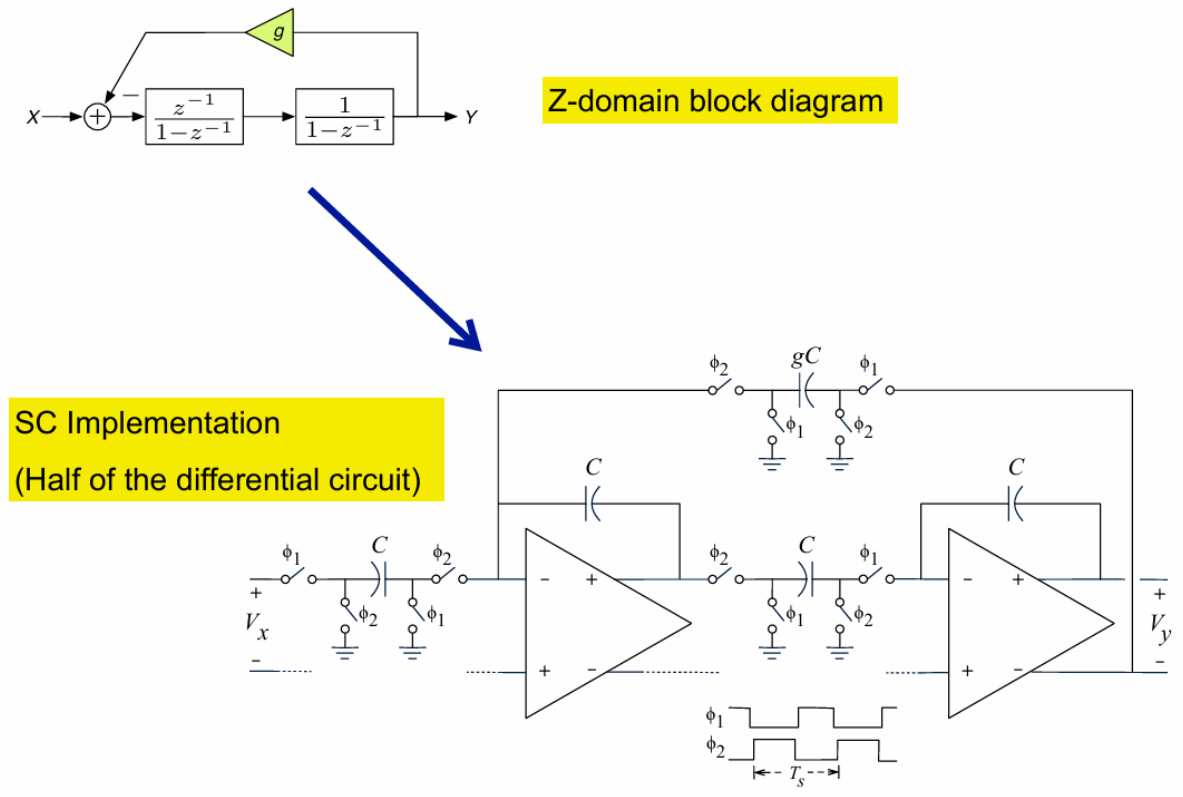

Figure 13: LDI Resonator and SC implementation.

The diagram consists of two cascaded integrators in a feedback loop. Each integrator has a transfer function of the form $\frac{z^{-1}}{1-z^{-1}}$ and $\frac{1}{1-z^{-1}}$. This configuration creates a second-order system, which exhibits resonant behavior at a specific frequency. The gain g is a scaling factor applied to the feedback path.

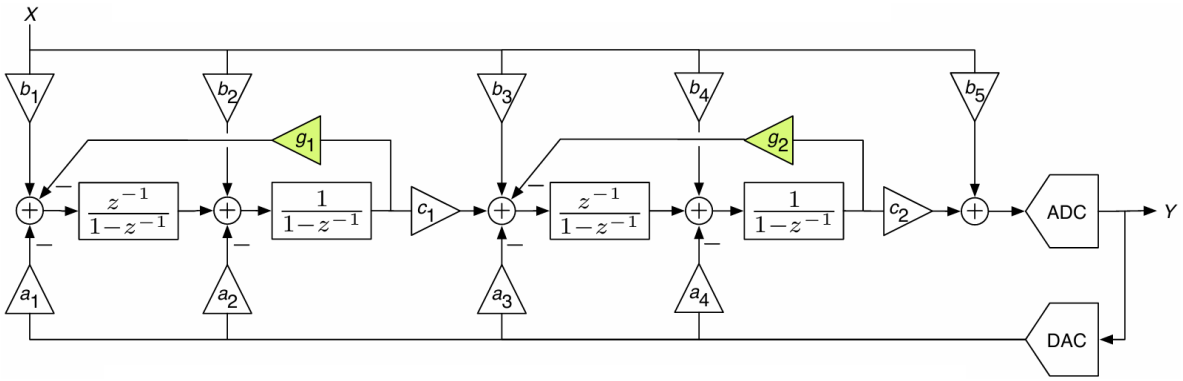

Figure 14: Cascade of resonators with feedback.

Each stage has a resonator block with a transfer function of the form $\frac{z^{-1}}{1-z^{-1}}$ and $\frac{1}{1-z^{-1}}$. These resonators accumulate and shape the quantization noise to push it out of the signal band. The feedback loops modify the dynamics of the modulator to improve stability and noise shaping.

Coefficients:

- a_i: weights applied to various paths inside the system, affecting how signals are combined.

- g_i: gains applied at specific points in the feedback path to control loop stability and filter characteristics.
- b_i: coefficients used in the weighted summation of signals before the quantizer (ADC).
- c_i: weights used to combine different paths in the structure before final quantization.

The feedback loop ensures that errors from the ADC stage influence earlier stages to improve overall accuracy.

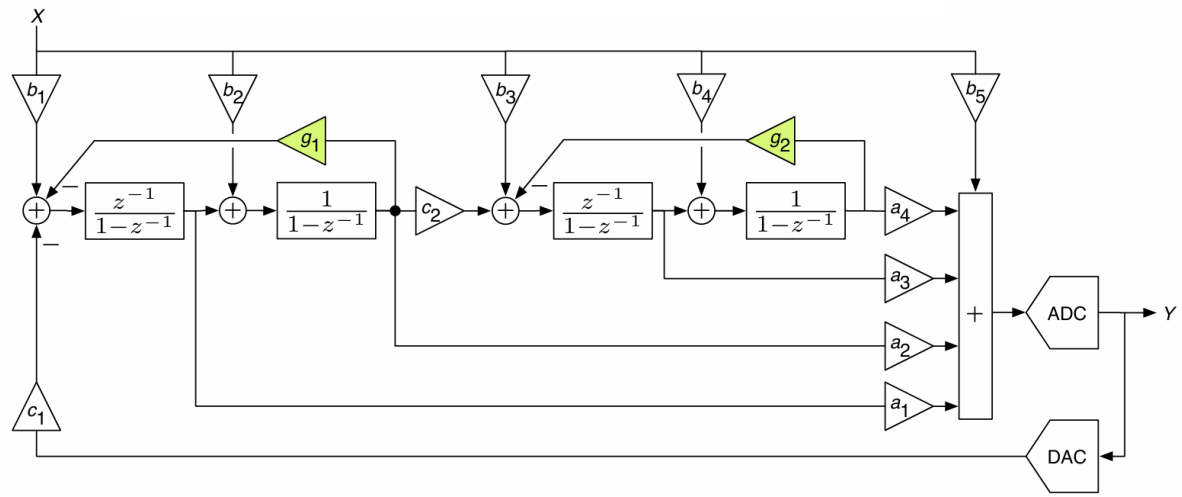

Figure 15: Cascade of resonators with feedforward.

Instead of feeding error signals back into earlier stages, this approach directly sums intermediate results to shape the noise spectrum.