Comparisions of Robert, Prewitt, Sobel operator based edge detection methods for real time uses on FPGA

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***Abstract*—Image processing has applications in real time embedded systems. Real time image processing requires processing on large data of image pixels in a stipulated time. Reconfigurable device such as FPGAs can be program to process on large image data and required processing time on image can be reduced by deploying parallelism, pipelining techniques in algorithm. Edge detection is very basic tool used in many image processing. Robert, Prewitt, Sobel edge detection are gradient based edge detection methods used to find edge pixels in an image. This paper presents comparisons of Robert, Prewitt, Sobel operators based edge detection techniques for real time uses. Edge detection algorithms are written with the help of hardware descriptive language VHDL. Xilinx ISE Design Suite-13 and MATLAB software platforms are used for simulation purpose. This paper focus on edge detection of gray scale image.**

Keywords—image edge detection; FPGA; VHDL; robert operator; prewitt operator; sobel operator

I. INTRODUCTION

Vision is the most advanced of our senses. Real-time image processing has applications in embedded systems such as autonomous vehicles and self guided armaments. These applications involve different processes like image enhancement, object detection and image analysis. Image edge detection is very important tool in digital image processing. A digital image is composed of picture element called pixel which represent the smallest sample of an image [1]. For simplicity we will focus only on the gray scale images. Edge detection is a process of identifying edges in image. Image edges correspond to points in an image where the gray value changes significantly. In gray scale image each pixel is represented by 8 bit, hence gray level values vary from 0 to 255, where 0 value stand for black color and 255 value stand for white color [1]. The data of edge detection is very large, for real time uses processing on image should be fast. FPGAs have large number of internal memory banks which can be accessed in parallel that allowed FPGA hardware to execute functions in a few clock cycles [2]. FPGA can be a promising solution for fast processing on images by deploying parallelism and pipelining techniques. Uses of FPGA in image processing systems enables rapid prototyping, minimizes the time to market cost [3]. For comparison purpose Robert, Prewitt, Sobel operator based edge detection algorithms are designed using VHDL language. In section 2, the overview of edge detection methods is described. In section 3, edge detection hardware system architecture is described. The simulation results and comparisons are presented in section 4 and a conclusion is given in section 5.

II. EDGE DETECTION

Edge is a basic feature of an image. Edges define the boundaries between regions in an image and basic step for segmentation and object recognition. An image defined as two dimensional function $f(x,y)$, where x and y are spatial coordinates and amplitude of f at any pair of coordinates (x,y) defines the light intensity at that point. Edge detection is a process of identifying edges, the sharp change in image pixel intensity. In real world image edges are blurred and have ramp profile, in such cases position of edges are thicker because of blurring effect. Derivative of ramp function is step function, first order derivative is zero at constant gray level and non zero value along entire ramp region hence magnitude of first order derivative can be used to detect an edge [1]. A gradient based edge detector method includes Roberts, Prewitt and Sobel operator. First order derivative in image processing are implemented using magnitude of gradient. For a function $f(x,y)$ the gradient of f at coordinates (x,y) is defined as 2 dimensional column vectors [1].

$$\nabla f = grad(f) = \begin{bmatrix} gx \\ gy \end{bmatrix} = \begin{bmatrix} \frac{\partial f}{\partial x} \\ \frac{\partial f}{\partial y} \end{bmatrix} \quad (1)$$

This vector points the direction of great rate of change of f at location (x,y). value at (x,y) is given by Equation 2

$$mag(\nabla f) = \sqrt{gx^2 + gy^2} \quad (2)$$

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It is more suitable computationally to approximate the square and square root operation by absolute values [1]. In digital Image processing filter marks or operators used to approximate the derivative. Filter masks are convolved with entire image to obtain the edge detected image.

z1	z2	z3
z4	z5	z6
z7	z8	z9

Fig.1. 3×3 region of an image

A. Robert edge detection

Roberts operator, approximate the gradient of an image through discrete differentiation. Robert mask is 2×2 matrix. Robert mask convolve with the entire image using horizontal and vertical Robert masks to give edge detected image in x direction and y direction respectively.

z1	z2
z3	z4

Fig.2. 2×2 region of an image

-1	0
0	1

0	-1
1	0

Fig.3. Robert masks

Horizontal derivative approximate as Equation 3 and vertical derivative approximate as Equation 4.

$$gx = (z4 - z1) \tag{3}$$

$$gy = (z3 - z2) \tag{4}$$

B. Prewitt edge detection

Prewitt mask is a discrete differentiation operator. This operator uses two 3×3 masks for calculating approximate derivative values in horizontal and vertical directions.

-1	-1	-1
0	0	0
1	1	1

-1	0	1
-1	0	1
-1	0	1

Fig.4. Prewitt masks

Horizontal derivative approximate as Equation 5 and vertical derivative approximate as Equation 6.

$$gx = (z3 + z6 + z9) - (z1 + z4 + z7) \tag{5}$$

$$gy = (z7 + z8 + z9) - (z1 + z2 + z3) \tag{6}$$

C. Sobel edge detection

Sobel mask is same as that of the Prewitt mask .There is only one difference, Sobel operator has '2' and '-2' values in center of first, third column of horizontal mask and first, third rows of vertical mask. This gives more weightage to the pixel values around the edge region, hence increases the edge intensity.

-1	-2	-1
0	0	0
1	2	1

-1	0	1
-2	0	2
-1	0	1

Fig.5. Sobel masks

Horizontal derivative approximate as Equation 7 and vertical derivative approximate as Equation 8.

$$gx = (z3 + 2z6 + z9) - (z1 + 2z4 + z7) \tag{7}$$

$$gy = (z7 + 2z8 + z9) - (z1 + 2z2 + z3) \tag{8}$$

III. EDGE DETECTION HARDWARE SYSTEM ARCHITECTURE

Xilinx integrated system environment design suite-13 software platforms are used for writing edge detection algorithm in VHDL language. Edge detection system architecture is mainly divided into two module first module is accumulation of input data, used for accumulation of input data in first in first out register memory. Second module is edge detection operation module and used for performing convolution, addition, threshold comparing operation on gathered correct pixel data [2]. Both modules are synchronies with input clock to system. When reset is low system go to reset position. For real-time uses system should be fast, more number of mathematical computations tends to increases time requires for processing. Hence while writing algorithm more attention given to write mathematical operation in different process statements because all process statements are executed in parallel in VHDL language [4]. Mathematical operation such as multiply by 2 operations is replaced by left shift of binary value by single bit.

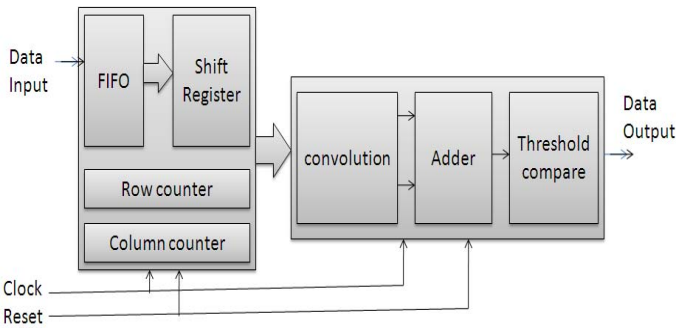

Fig.6. Edge detection system architecture

FIFO memory array and shift registers are used for accumulation of input pixel data for processing. Length of FIFO memory array is same as that of pixels in one row of input image [5]. Since Robert operator is 2×2 size mask, Robert operator based edge detection system requires only one FIFO memory array and one shift register to accumulate sufficient amount of pixel data to start processing. Prewitt, Sobel operator based edge detection system requires two FIFO memory array and three shifts register to accumulate sufficient amount of pixel data to start processing because Prewitt and Sobel operators are of size 3×3. At every rising edge of clock input pixel data is stored, take out from FIFO and pass through shift register. Row and column counter are used for synchronizing operation between accumulation of input data module and edge detection operation module. Input image size and output image size is same. Convolution operation is performed on accumulated input data to obtain a gradient in horizontal and vertical direction. The absolute values of gx and gy are added with adder and obtained magnitude is compare by threshold value. If the value is more than the threshold, the centre value in 3×3 image region is get replace by 255. If the value is less than the threshold, the centre value in 3 × 3 image region is get replace by 0 [6].

To test correctness of VHDL code a test bench code is used. Xilinx software provides feature called simulation which takes inputs and shows how it would work in hardware. To simulate design, both the design under test i.e. edge detection system and the stimulus provided by the test bench are required [7]. Test bench has three main purposes to generate stimulus for simulation, to apply this stimulus to the entity design under test and to collect output responses [4]. Figure 7 shows test design flow diagram. Gray scale image is read into MATLAB software. Using MATLAB software pixel data information is obtained from gray scale image and stored into a text file. This text file contains values between 0 to 255, each value represent the pixel intensity. The same text file is then read by Test bench code written in XILINX software and passes it to edge detection system module at rising edge of clock cycles. After processing on pixel data by Edge detection System, output of edge detection system is collected in another text file. Output text file's processed pixel data is then read in MATLAB software to obtained edge detected image. At output image with only two colors, black and white is obtained [8].

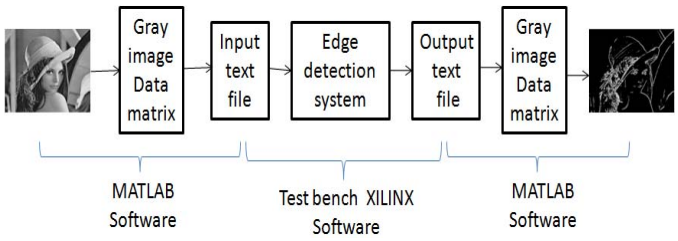

Fig.7. Test design flow

IV. SIMULATION RESULTS

Edge detection is fundamental image processing tool uses in various complex image processing systems particularly in the areas of feature detection and feature extraction. In real-time applications processes have to complete in stipulated time. Image edge detection process should be very fast so that you can get sufficient time to further processes on edge detected data and to generate related control action. Gray scale image of size 640x480 is used for experiment purpose. Number of rows are 480 and number of columns are 640. To meet real-time requirements, processing on single frame should be completed in desire time. In general CMOS digital camera sensor gives VGA output at maximum frame rate of 30 frames per second means one frame out in 33.33ms and pixel data outs from camera in synchronization with 24 MHz clock frequency [9]. To mimic digital camera sensor working in simulation, pixel data read from input text file is given to edge detection system at rising edge of the 24 MHz clock cycle. For real time uses processing on one frame should complete before next frame comes. After simulation it is observed that edge detection process on gray scale image of size 640×480 is completed in 12.8 ms, which is less than 33.33 ms and hence met real time image processing requirement. Edge detection process is performed on same gray scale image by Robert, Prewitt and Sobel operator and output obtained is shown in figure 8. From figure 8, it can be observed that edges detected by Sobel operator is very good visible as compare to Robert and Prewitt operator [10].

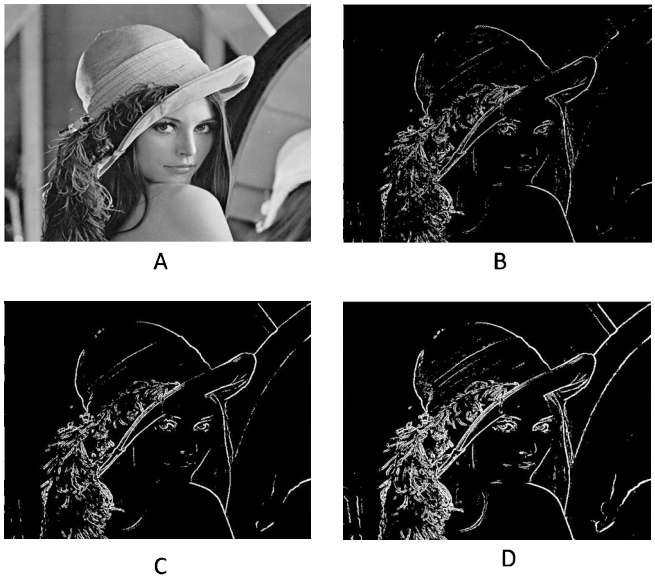

Fig.8. Simulation results. (A) Orignal image, (B), (C), (D) edge detected images obtained by Robert operator, prewitt operator and sobel operator respectively.

Robert operator is 2x2 size matrix hence only one FIFO and one shift register to accumulate sufficient amount of pixel data to start processing while Prewitt, Sobel operators are of size 3x3 and requires 2 FIFO and 3 shift registers. Therefore Hardware requirements for Robert operator based edge detection system is less than Prewitt, Sobel based edge detection system. Table I shows FPGA Spartan-6 device XC6SLX25 hardware utilizations for Robert, Prewitt, Sobel operator based edge detection methods.

TABLE I. HARDWARE UTILIZATION TO DESIGN ALGORITHM

Slice Logic Utilization	Robert	Prewitt	Sobel
Number used as Flip Flops	219	339	343
Number of Slice LUTs	1,598	1727	1728
Number used as logic	322	450	450
Number of occupied Slices	462	490	495

Table II gives information related to number of times addition, multiplication operations are used for edge detection process using Robert, Prewitt and Sobel operators. In Robert operator based edge detection system only addition operation is required to perform convolution. Number of times addition operation requires for convolution process is very less in Robert operator based edge detection system hence computational complexity is very less in case of Robert operator based edge detection system. Efficiency of image edge detection is more in case of Sobel operator based system as compare to Robert, Prewitt operator based system with small increase in computational complexity.

TABLE II. NUMBER OF TIMES ADDITION, MULTIPLICATION OPERATION REQUIRES FOR CONVOLUTION

Operation	Robert	Prewitt	Sobel
Addition	639×479×3	638×478×11	638×478×11
Multiplication	0	0	638 × 478 × 4

V. CONCLUSION

Efficiency of Robert, Prewitt, Sobel operator based edge detection systems is compared. The FPGA supports high levels of parallel processing data flow structures that are important for efficient designing of real time image processing algorithms. Written algorithm takes advantages of parallelism possible in FPGA. FPGAs can be a promising solution for real time image processing work. FPGA hardware utilization is less in Robert operator based edge detection as compare to Prewitt and Sobel operator. Edge detection efficiency of Sobel operator is better than Prewitt and Robert operator. Edges detected by Sobel operator based edge detection system are thick. For application like road lane detection in smart cars where fast processing is required, Robert operator based edge detection system can be use. For system like bar code reader, Sobel operator based edge detection system can be use to get sharp edges.

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