INTEL PROCESSOR ARCHITECTURE

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PIONEER IN ARCHITECTURE

WHO IS HE?

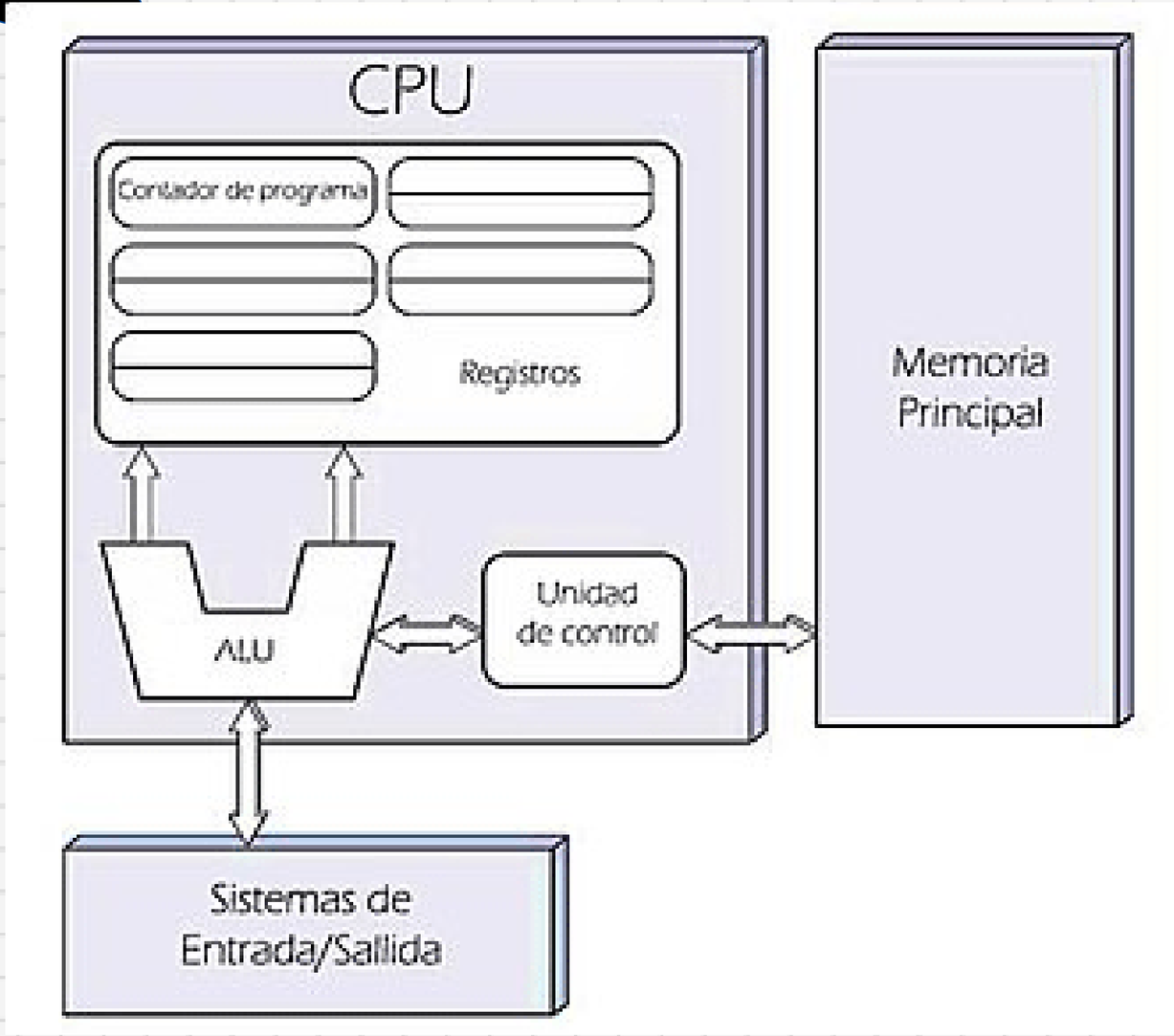
ENGINEER, MATHEMATICAL, ELECTRONIC, VISIONARY AND SCIENTIST BEING THE PIONEER IN COMPUTER SCIENCE WORKS AND ADVANCED COMPUTING SYSTEMS

BEST ACHIEVEMENTS

HE CREATES A BASIC STRUCTURE FOR COMPUTER PROCESSORS, I CREATE ADVANCED MATHEMATICAL SYSTEMS FOR COMPUTATIONAL DEVELOPMENT

Clasic Von Neuuman

Buscar



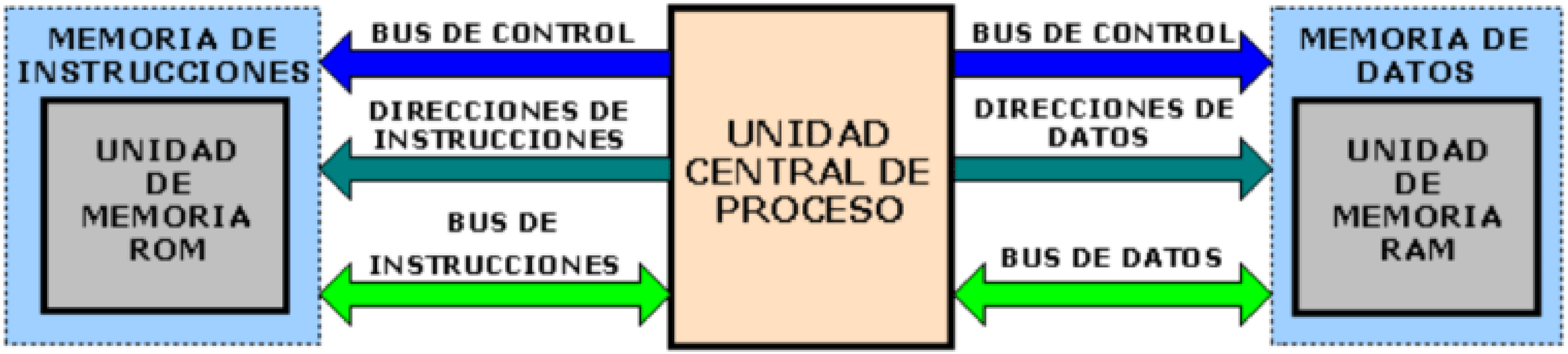
OPERATION DISPOSITY

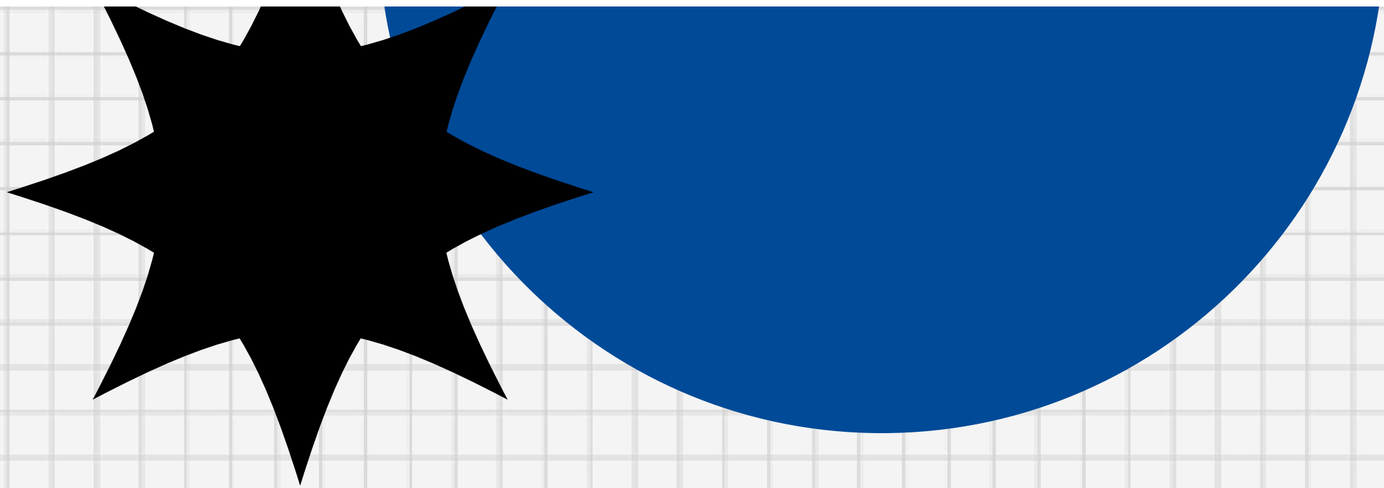
MEMORY

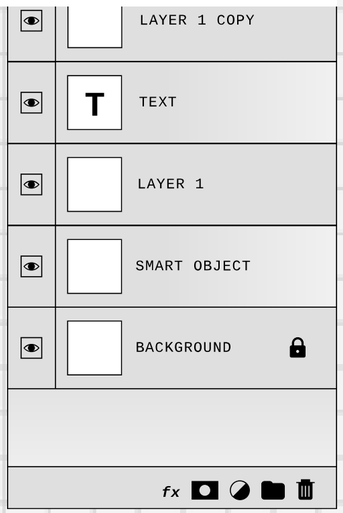
CONTROL UNITY

E/S DISPOSITIES

ARQUITECTURA HARVARD





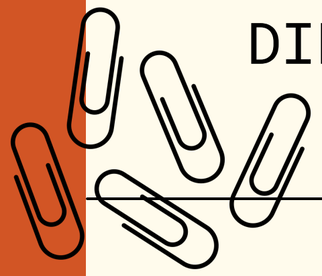


MAIN ASPECTS TO RECOGNIZE

1	DESIGNED A PHYSICAL ARITHMETIC SYSTEM IN WHICH INFORMATION IS ANALYZED BY A CENTRAL SYSTEM BASED ON A STACK
2	I DETERMINE WHICH WERE THE EFFICIENT FUNCTIONS THROUGH NUMERICAL OR TEXTUAL WORK IN THE INPUT/OUTPUT BUSES
3	IT WAS CHARACTERIZED BY USING AN OPERATION DEVICE, CONTROL UNIT, DEVICE MEMORY AND I/O DEVICE
4	HE CREATED AN OPTIMAL ARCHITECTURE DIFFERENT FROM ITS COMPETITION, WHICH WAS CHOSEN FOR ITS EASIER PROGRAMMING

ARCHITECTURE 8-16 BITS

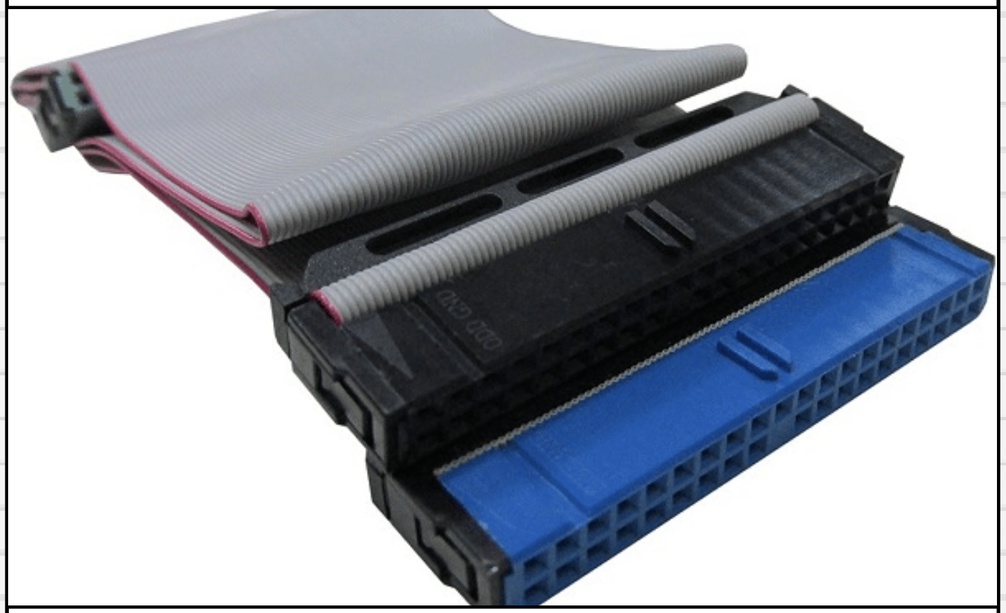
MAIN FEATURES 8 bits	8-BIT DATA BUSES	ADDRESSABLE MEMORY WITH 32 KBPS CAPACITY	INTEL 8008, 8080 FLUCTUATION 0-255
MAIN FEATURES 16 bits	16-BIT ADDRESSING BUSES	ADDRESSABLE MEMORY WITH 64 KBPS CAPACITY	INTEL 8086 80286 FLUCTUATION 0-255
DIFFERENCES	1 Octes 2 Octes From CPU and ALU	More energy More fluctuation	Content in its buses X8-x16



All buses

is a digital system that transfers data between components of a computer

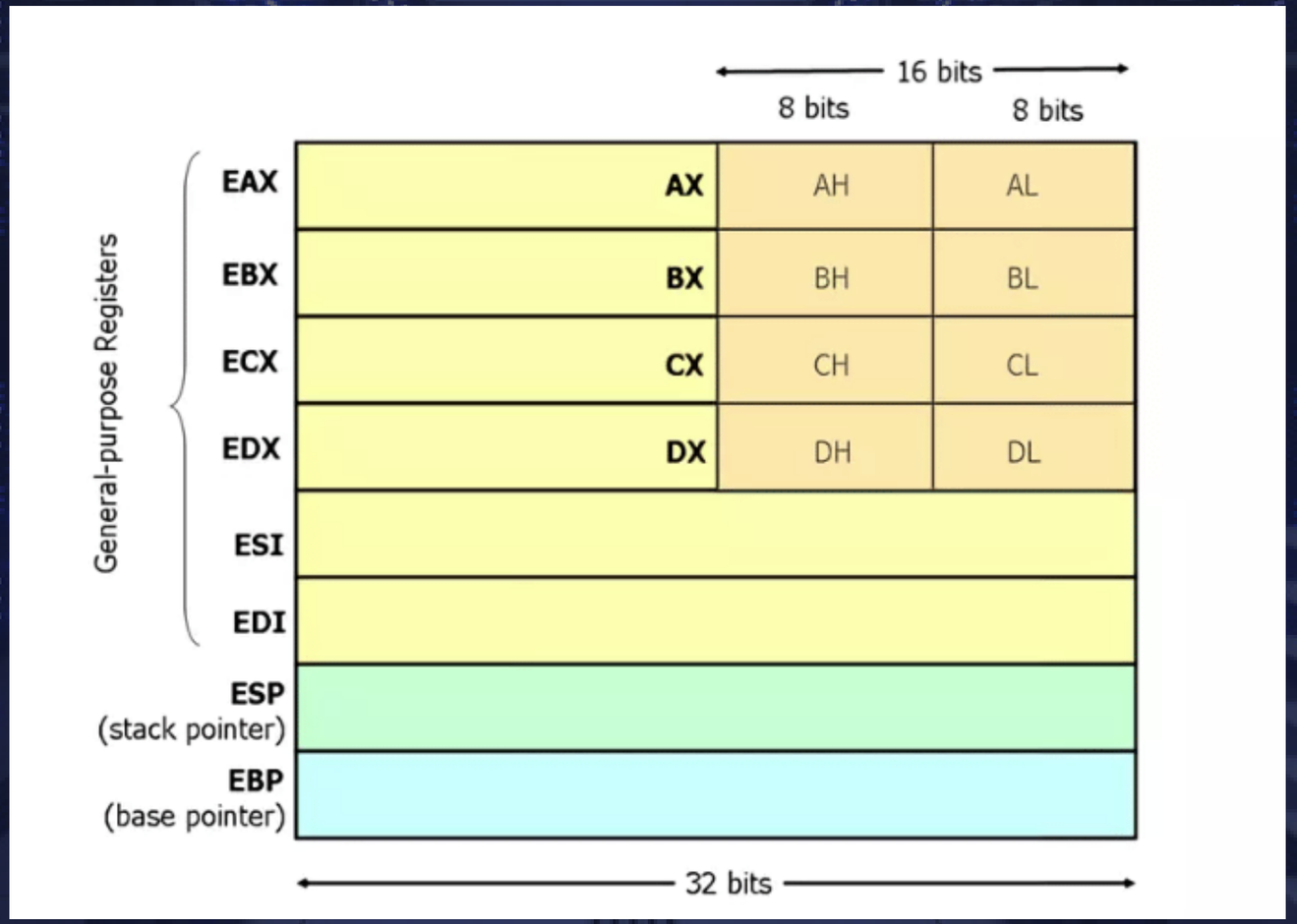
DATA BUS DDE

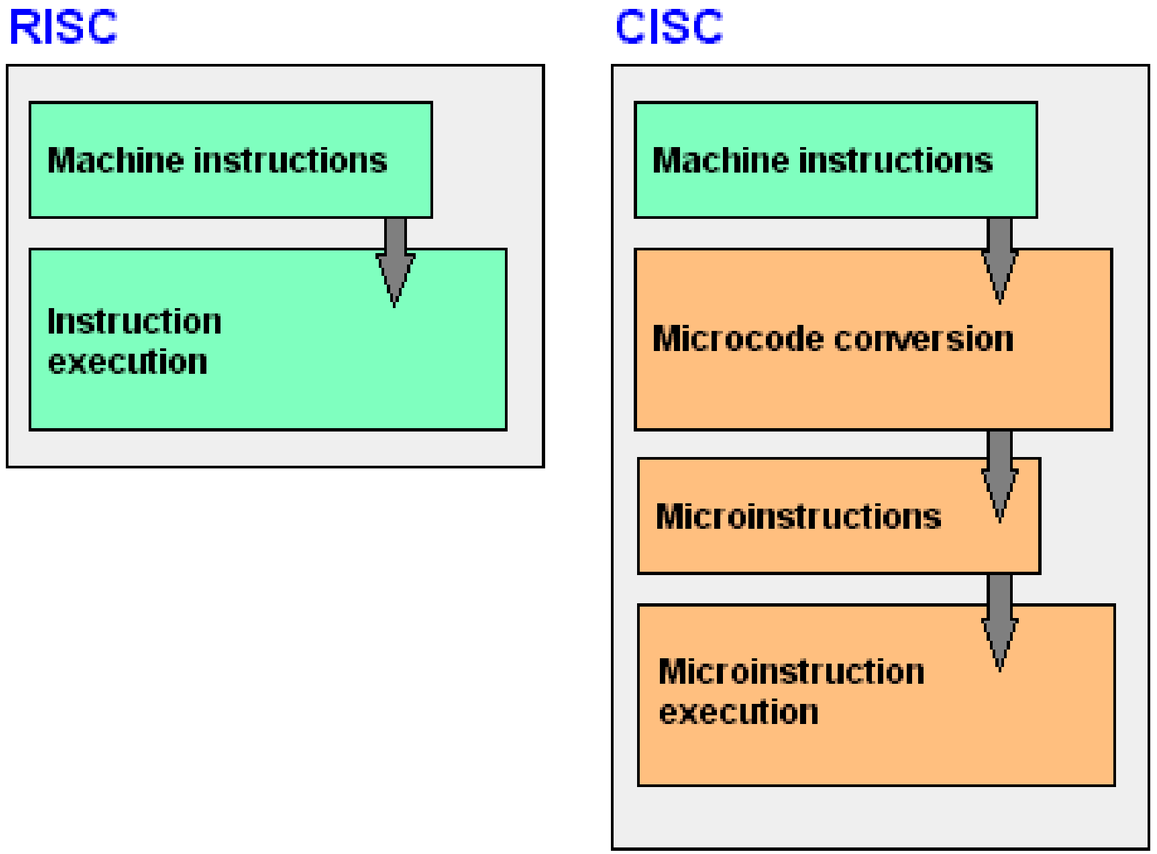


vs.

DATA BUS SCSI

32 Bits


16 bits
8 bits
8 bits
General-purpose Registers
EAX
AX
AH
AL
EBX
BX
BH
BL
ECX
CX
CH
CL
EDX
DX
DH
DL
ESI
EDI
ESP
(stack pointer)
EBP
(base pointer)
32 bits



ARCHITECTURE RISC

They have fundamental and simple characteristics being Fixed-size instructions and presented in a reduced number of formats.

ARCHITECTURE CISC

Promotes the use of a large number of instructions, allowing complex operations between operands located in memory or in internal registers

Objectives

The two serve different functions in that one is much cheaper and easier than the other, while the other has the potential to change.d

Real Mode and memory segmentation

- Real mode is characterized by 20 bits of segmented address space (meaning only 1 MB of memory can be addressed).
- direct software access to BIOS routines and peripheral hardware, and has no hardware-level multitasking or memory protection concepts
- It is a memory management technique that aims to get closer to the user's point of view
- One of the most obvious and straightforward implementations of a segmented memory space is to allocate a different segment to each of a process's sections of memory space.