ARM Cortex-A8
Intel Core i7

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ARM Cortex-A8

Introduced by ARM in 2005, it is the first processor supporting the ARMv7-A architecture.
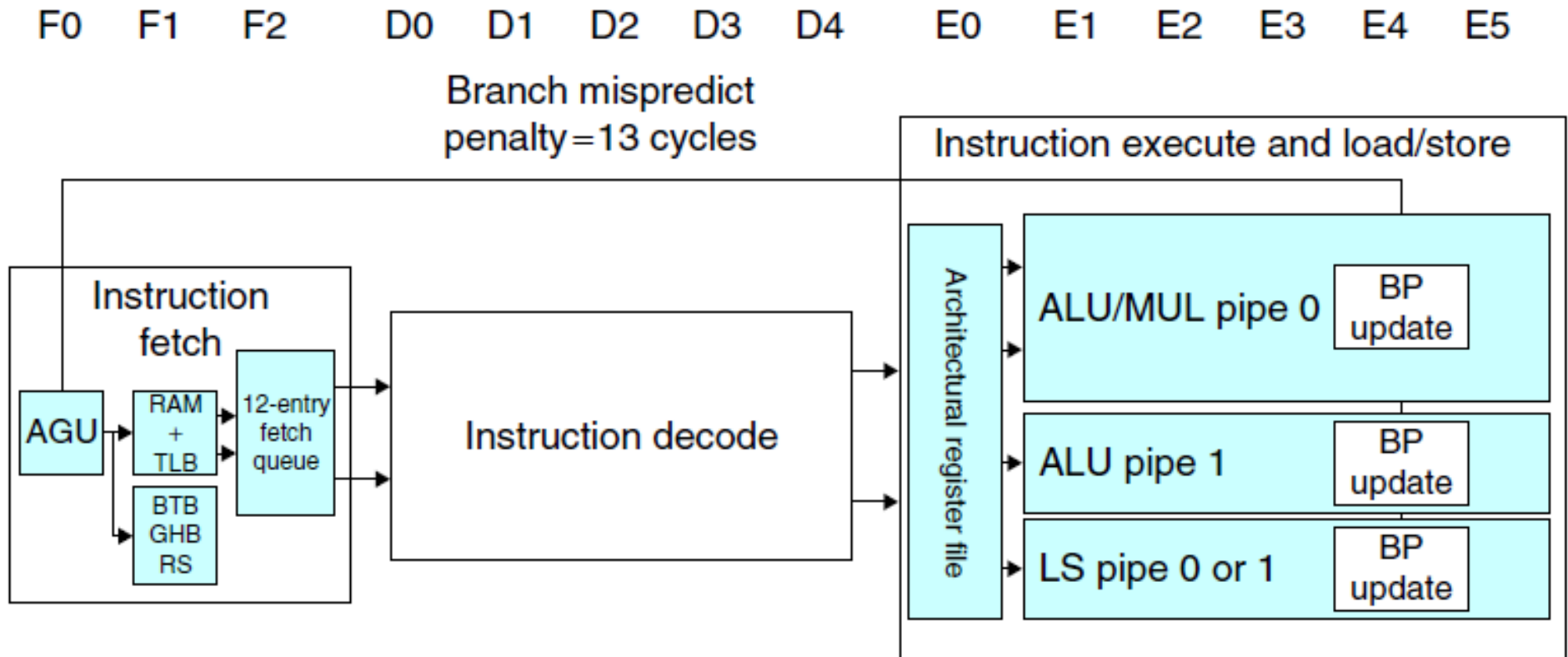
First ARM superscalar processor, running at high frequencies: from 600MHz to 1GHz.
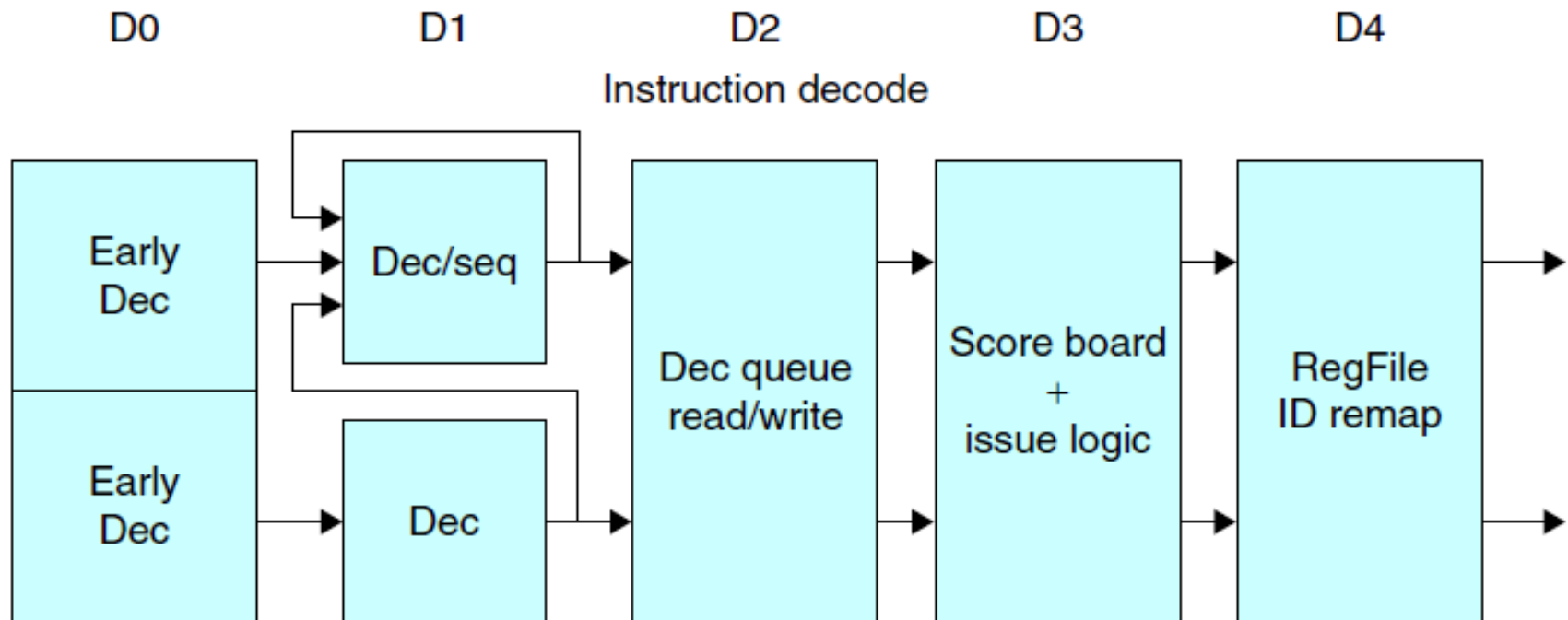
Used in PMD, mainly in smart phones, and tablets.

Main characteristics:

- Dual issue

- Statically scheduled

- Dynamic issue detection
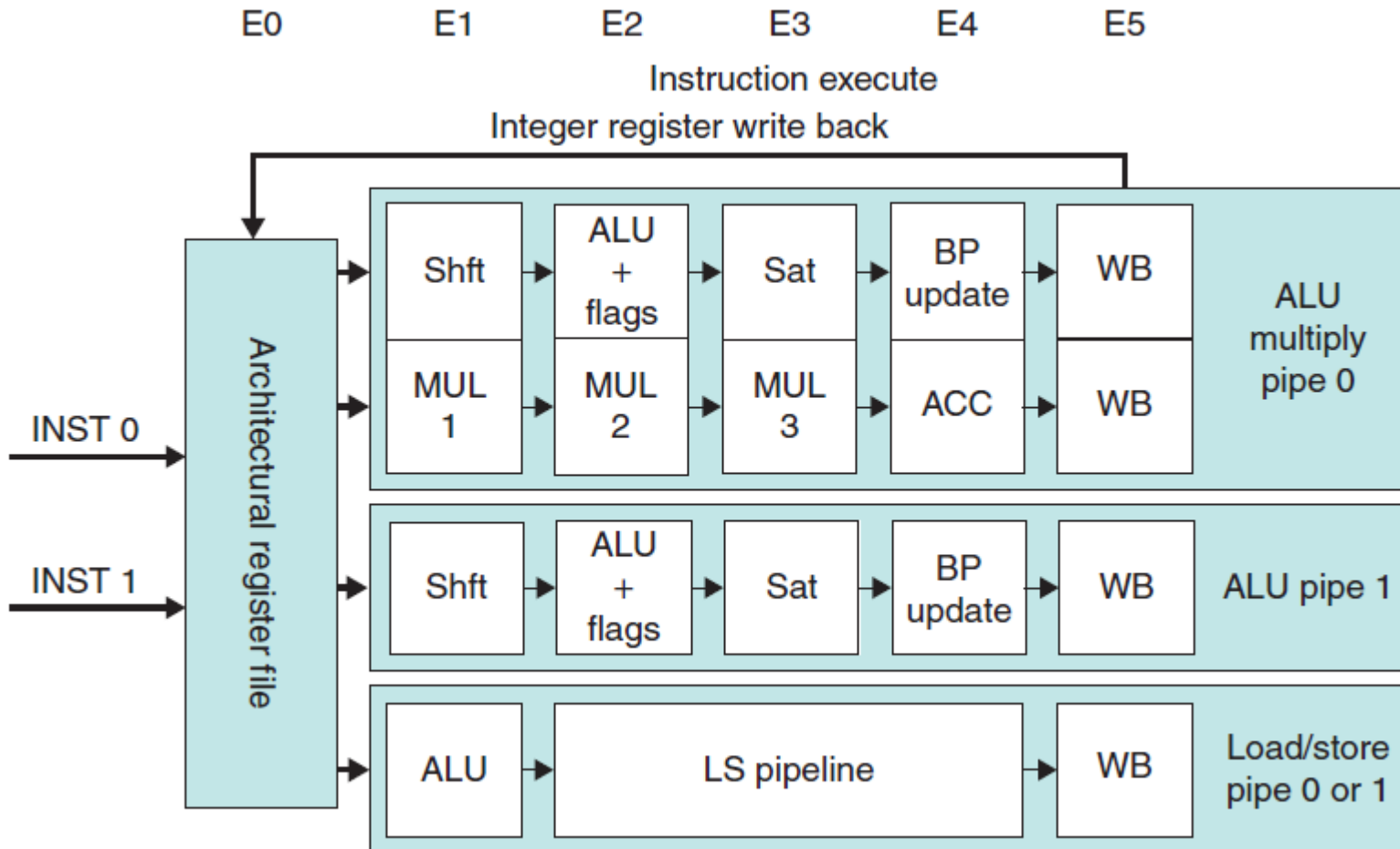
- Dynamic branch prediction two-level with a BTB.

A8 pipeline

F0　F1　F2　　D0　D1　D2　D3　D4　　E0　E1　E2　E3　E4　E5

Branch mispredict
penalty=13 cycles

Instruction execute and load/store

Instruction fetch

AGU

RAM + TLB

BTB GHB RS

12-entry fetch queue

Instruction decode

Architectural register file

ALU/MUL pipe 0 | BP update

ALU pipe 1 | BP update

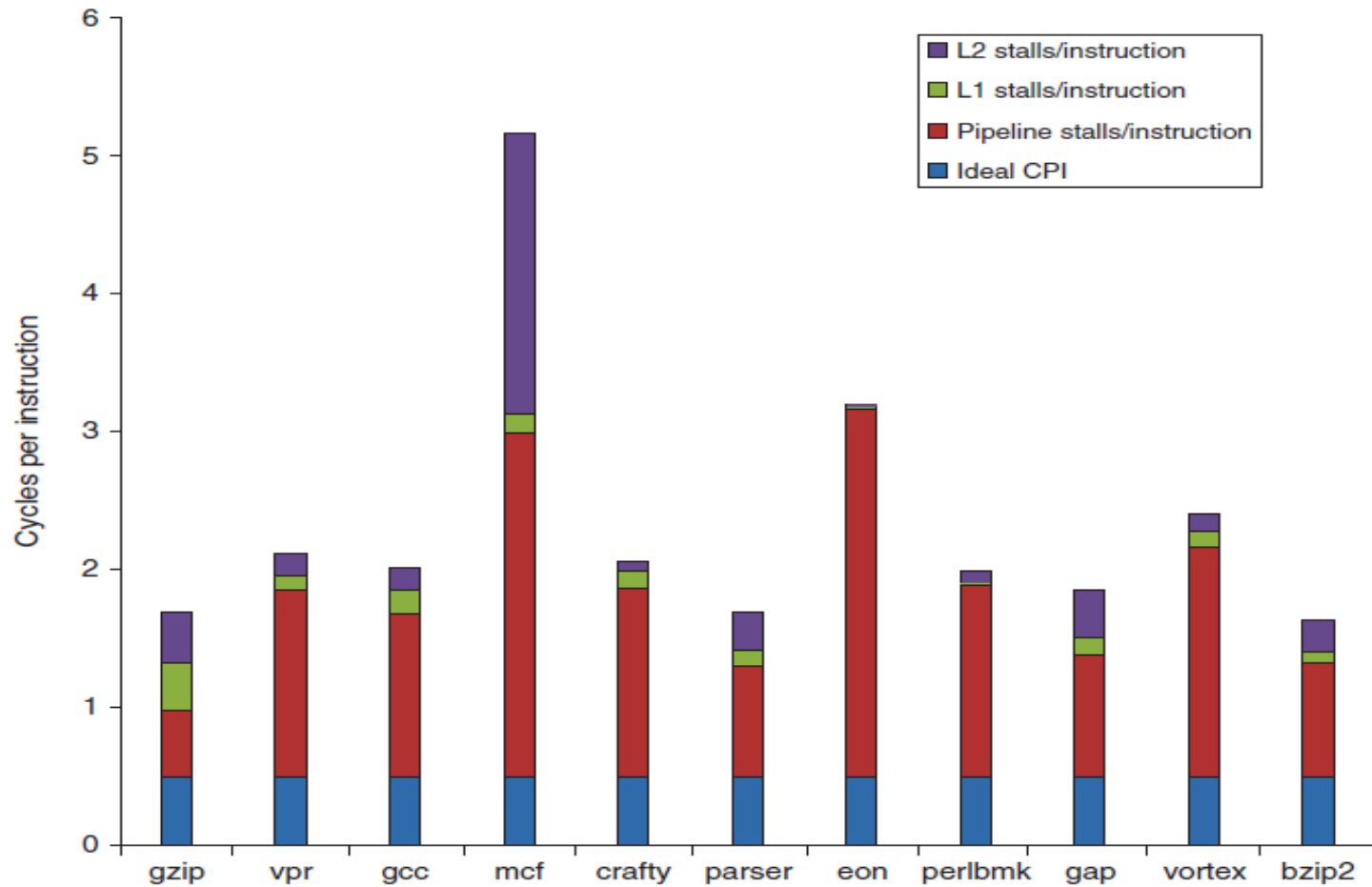LS pipe 0 or 1 | BP update

3

Decode unit

Execution unit

Pipeline stalls

- **Structural hazards**
    - **2 instruction in the issue packet use the same functional unit**
- **Data hazards**
    - **It is a compiler task to avoid data hazards**
- **Control hazards**
    - **Misprediction penalty: 13 cc**

A8 performance

Intel core i7

Intel 64-bit x86-64 processor introduced in 2008. Superscalar processor core with out-of-order and speculation features.

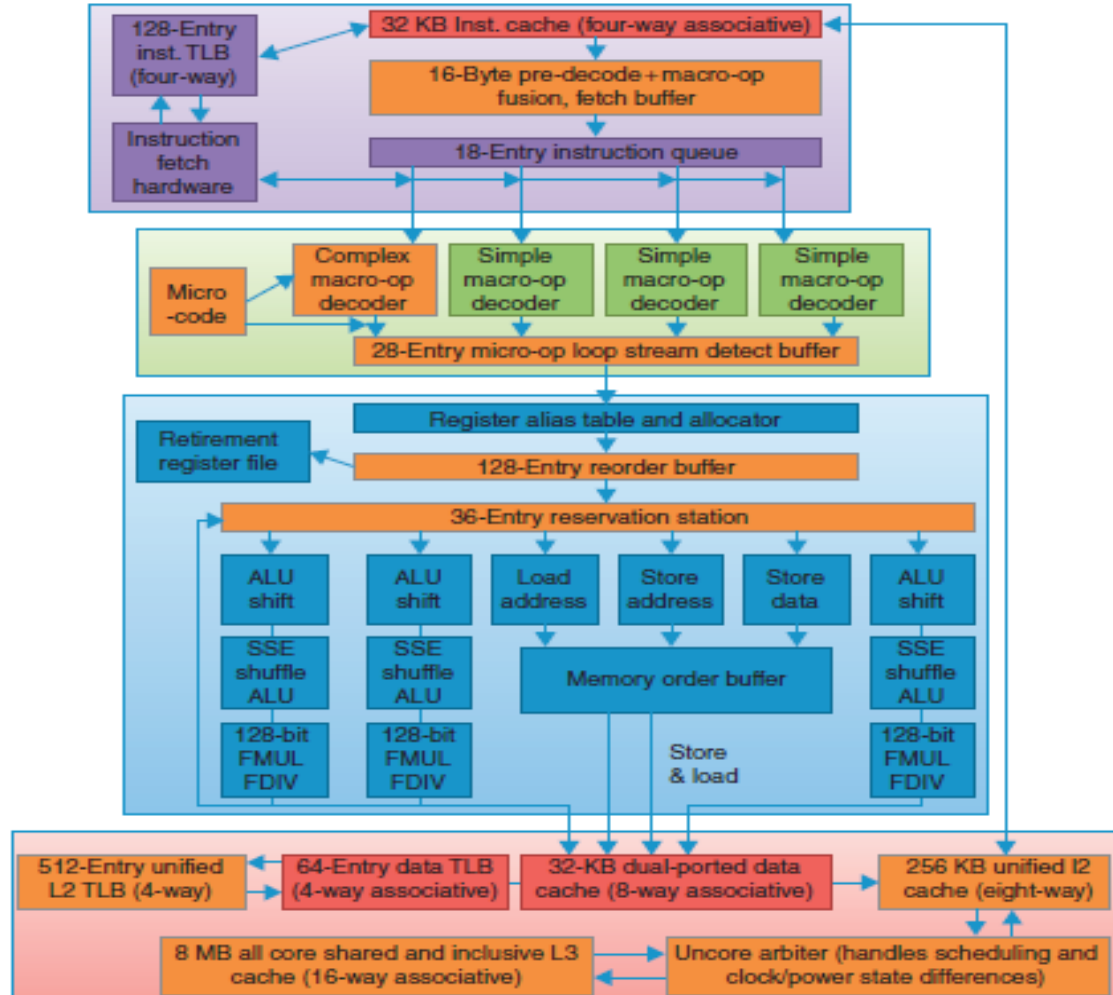Distributed as multicore devices for the desktop and laptop markets.

- 3 cache levels
- 45 nm
- ~ 730 million transistors
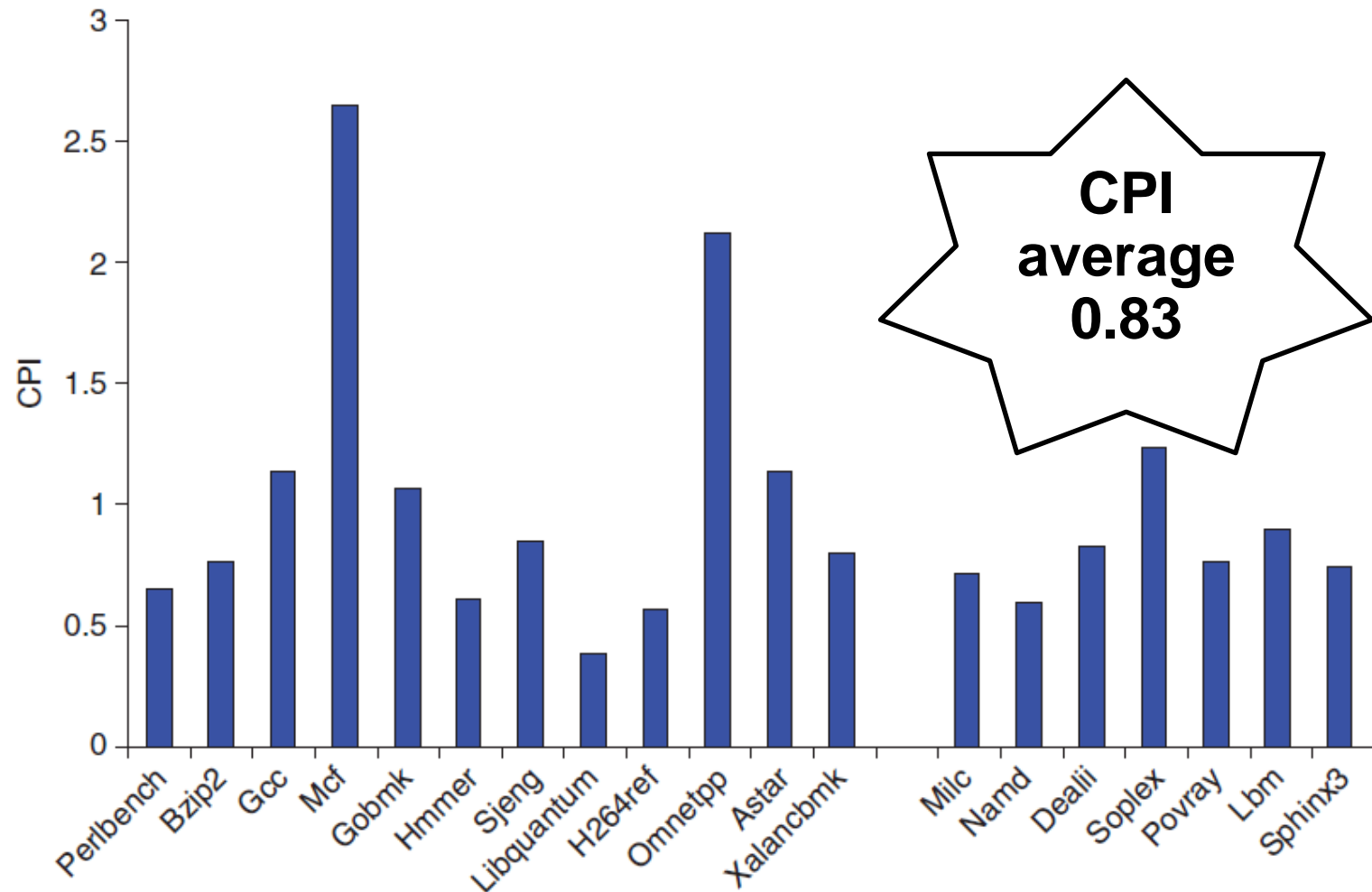- High clock frequencies: 2.66 GHz – 3.20 GHz

i7 pipeline details

i7 processor supports x86 instructions that can be decoded in 1 to 17 bytes.

- The total pipeline depth is 14 stages
- Up to 4 instructions issued for clock cycle
- Branch mispredictions cost 15 cycles
- 48 load and 32 store buffers
- Six independent functional units
- Up to six instruction issues in the same clock cycle
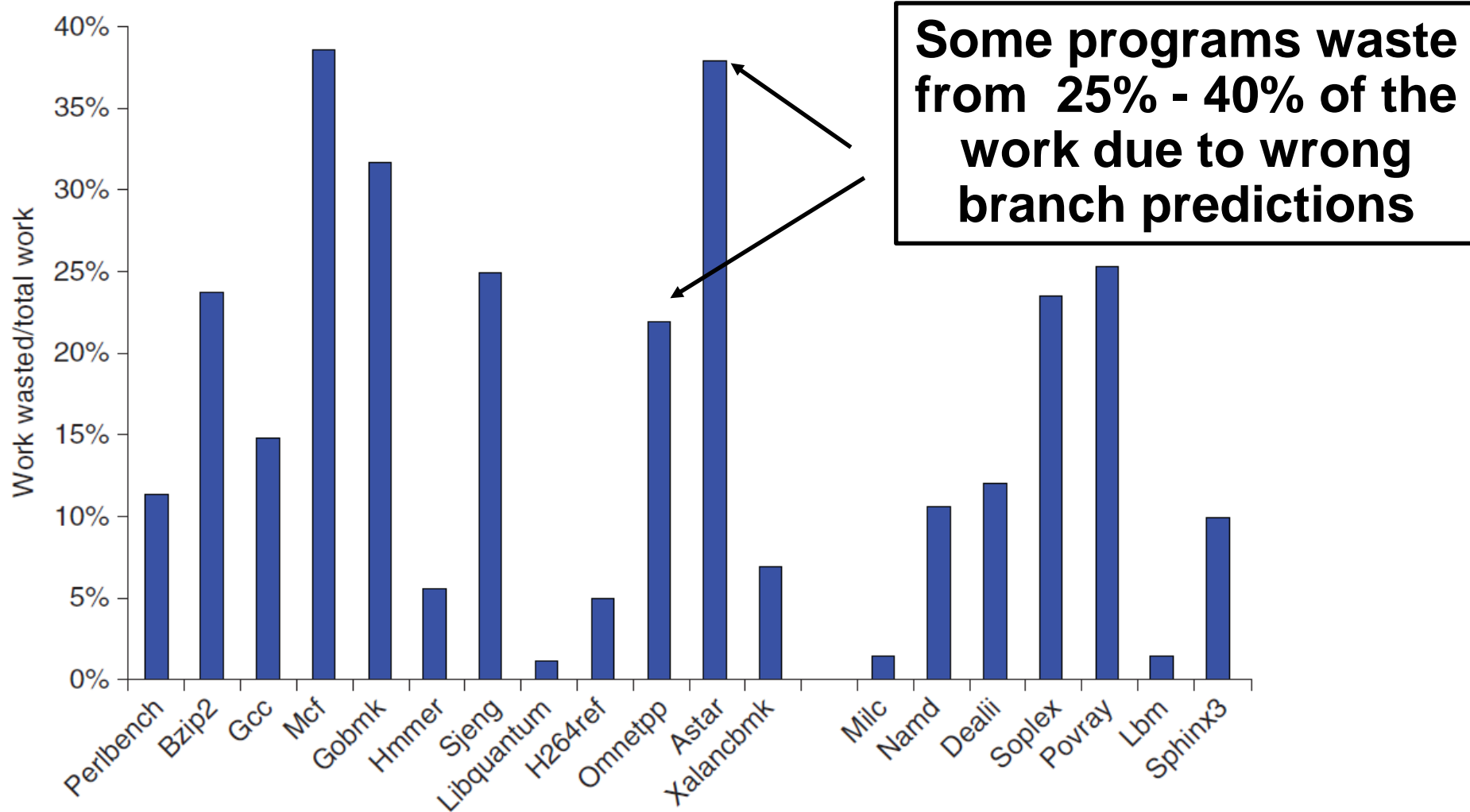- ROB 128 entries
- Reservation Stations 36 entries.

Intel Core i7 pipeline

Processor performance

Wasted work information

Some programs waste from 25% - 40% of the work due to wrong branch predictions

Area	Specific characteristic	Intel i7 920 Four cores, each with FP	ARM A8 One core, no FP	Intel Atom 230 One core, with FP
Physical chip properties	Clock rate	2.66 GHz	1 GHz	1.66 GHz
	Thermal design power	130 W	2 W	4 W
	Package	1366-pin BGA	522-pin BGA	437-pin BGA
Memory system	TLB	Two-level All four-way set associative 128 I/64 D 512 L2	One-level fully associative 32 I/32 D	Two-level All four-way set associative 16 I/16 D 64 L2
	Caches	Three-level 32 KB/32 KB 256 KB 2–8 MB	Two-level 16/16 or 32/32 KB 128 KB–1MB	Two-level 32/24 KB 512 KB
	Peak memory BW	17 GB/sec	12 GB/sec	8 GB/sec
Pipeline structure	Peak issue rate	4 ops/clock with fusion	2 ops/clock	2 ops/clock
	Pipeline scheduling	Speculating out of order	In-order dynamic issue	In-order dynamic issue
	Branch prediction	Two-level	Two-level 512-entry BTB 4K global history 8-entry return stack	Two-level