**Lab 4: Multiplexer Design**

ELEN/COEN 21

Anand Rajamani and Francesca Narea

2/17/2017

Friday 2:15 - 5:00 PM

**Introduction:**

During this lab, we used Altera software to create a 2-1 Mux symbol for use in our top level 8-1 Mux design. We used the Waveform analyzer to thoroughly to check our lower level design before placing it into a higher level design. We successfully simulated a 2-1 Mux and an 8-1 Mux using the Altera FPGA.

**Pre-labs:**

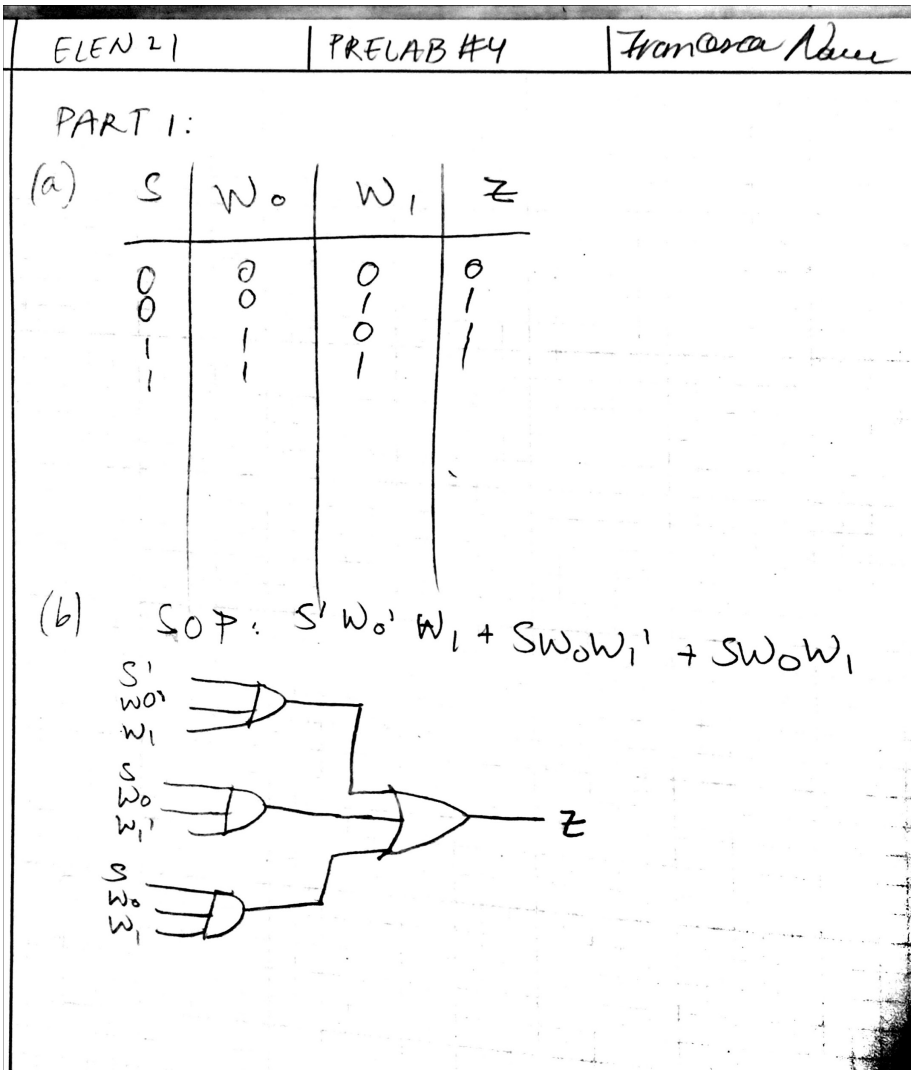
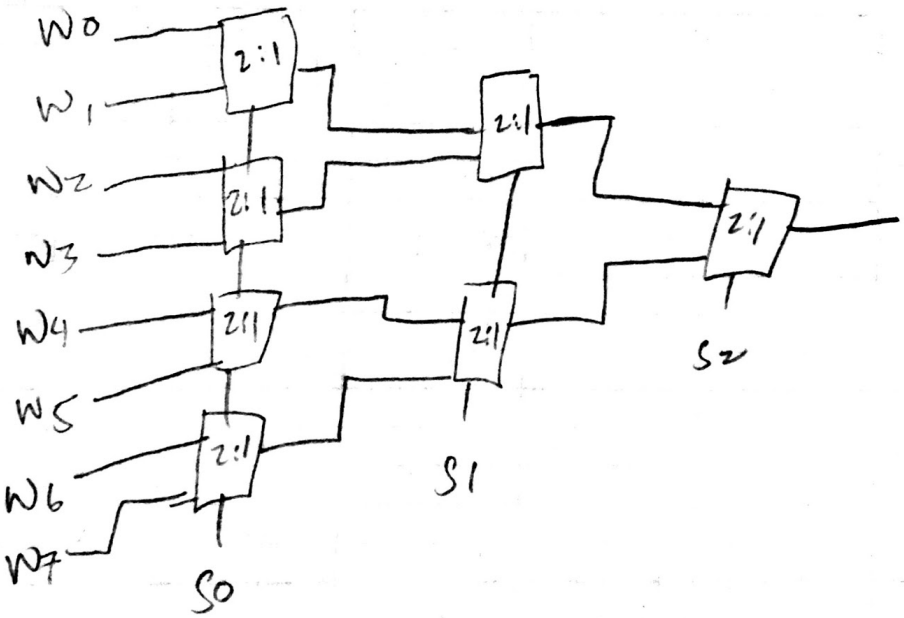



Figure 1: Pre-lab for Francesca Narea (page 1)

PART 2:

| $S_2$ | $S_1$ | $S_0$ | O |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |




$S_2\ S_1\ S_0 = 1, 0, 0 \rightarrow W_4$

$S_2\ S_1\ S_0 = 0, 0, 1$

Figure 2: Pre-lab for Francesca Narea (page 2)

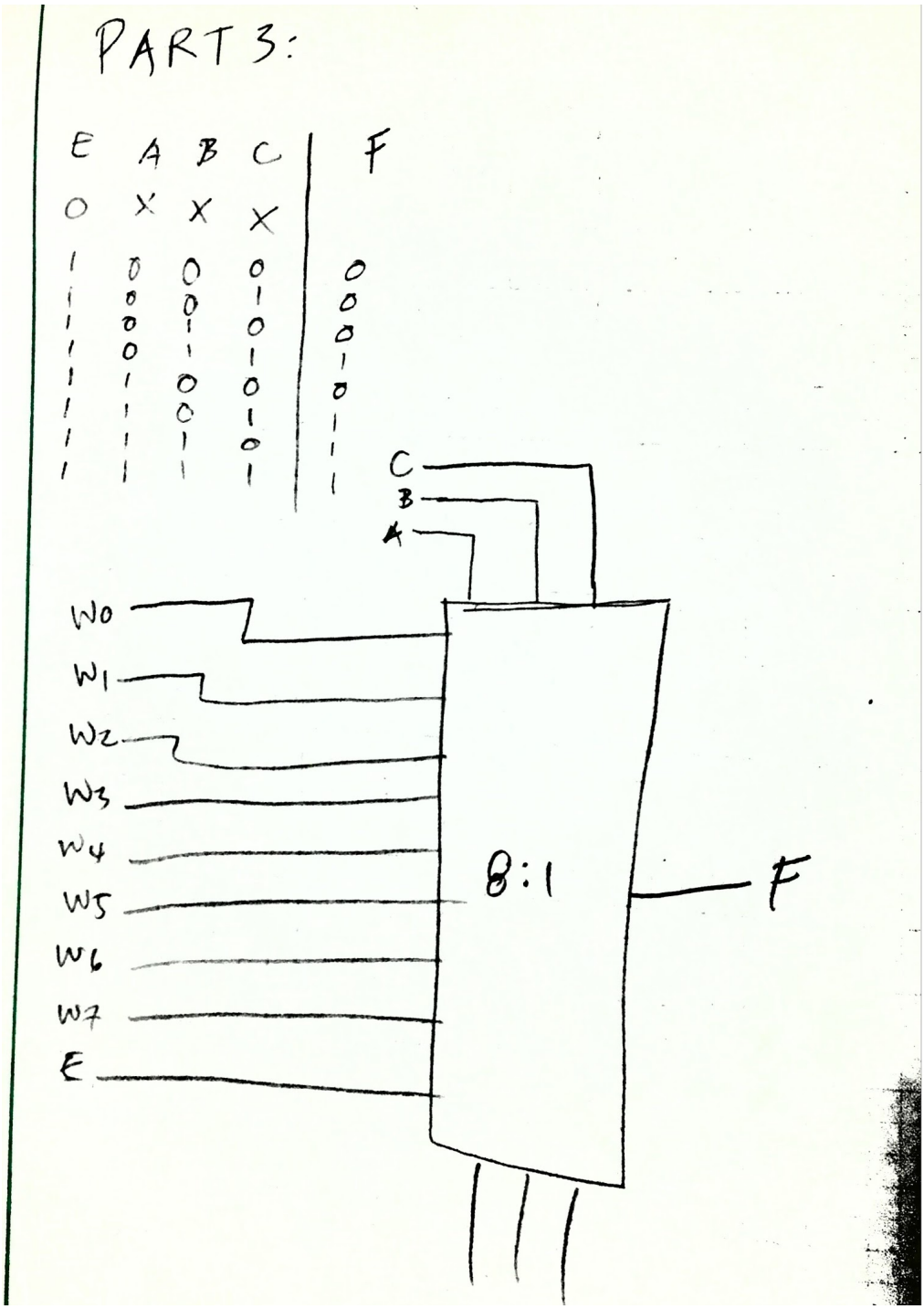



Figure 3: Pre-lab for Francesca Narea (page 3)

Anand Rajamani
Professor Ogunfunmi
ELEN21L
Lab 4 Prelab
2/6/17

| S | W0 | W1 | Z |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

K-map:

| | W0 / W1 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|---|
| S | | | | | |
| 0 | | 0 | 0 | 1 | 1 |
| 1 | | 0 | 1 | 1 | 0 |

SOP form: S*W1 + W0*W1 + S*W0

Part 2:

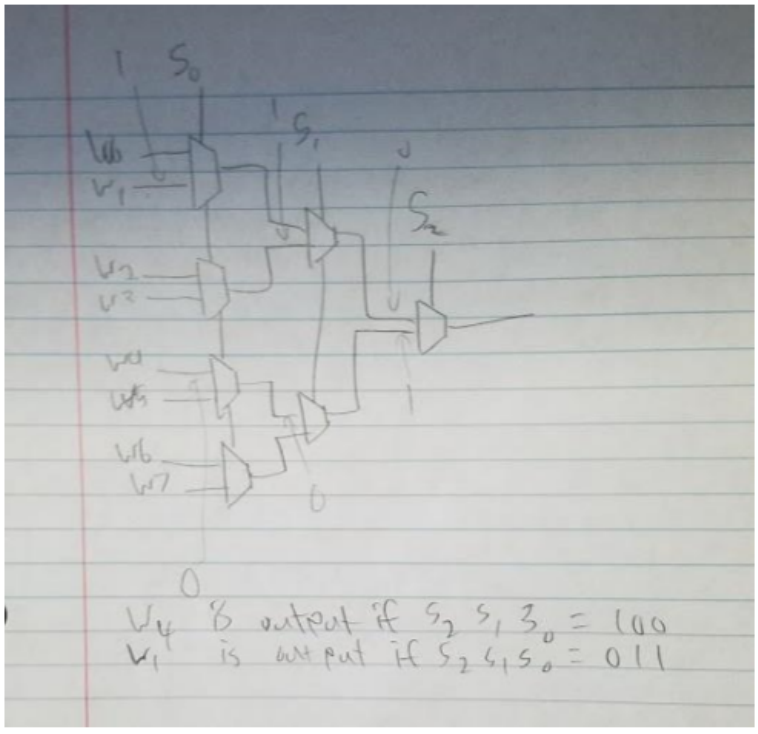



Figure 4: Pre-lab for Anand Rajamani (page 1)

Part 3:

Truth Table:

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

MUX:

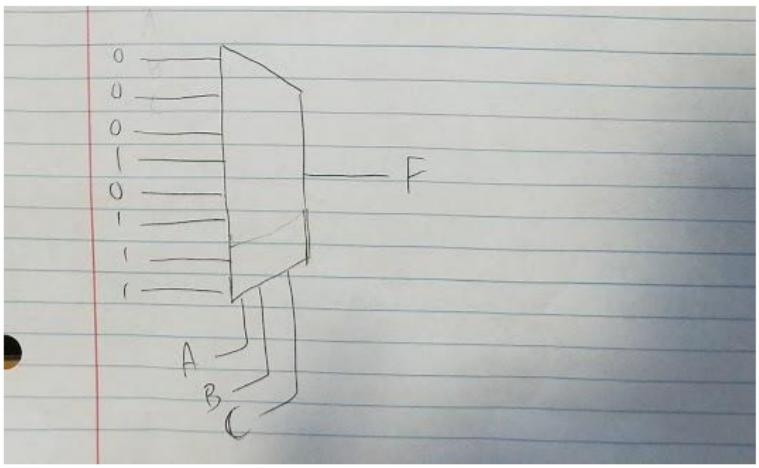



Figure 5: Pre-lab for Anand Rajamani (page 2)

**Procedures:**

We first created the schematic for a 2-1 Mux and converted it into a symbol using the Quartus software. We then used the waveform simulator to test the Mux to ensure it was working properly. We ran into some problems with the Mux, first with the circuit having unconnected wires, and then the order in which the variables were displayed on the waveform simulator screen. Next, we incorporated this symbol into a new schematic to create an 8-1 Mux. The simulation for the 8-1 ran much more smoothly, and we were able to finish very quickly. We added an enable input to the Mux afterwards. Lastly, we simulated both designs and tested our implementations of the Altera FPGA, using fixed inputs of 0s and 1s to simulate a 3-input XOR with 3 switches to control the switch on the Mux.

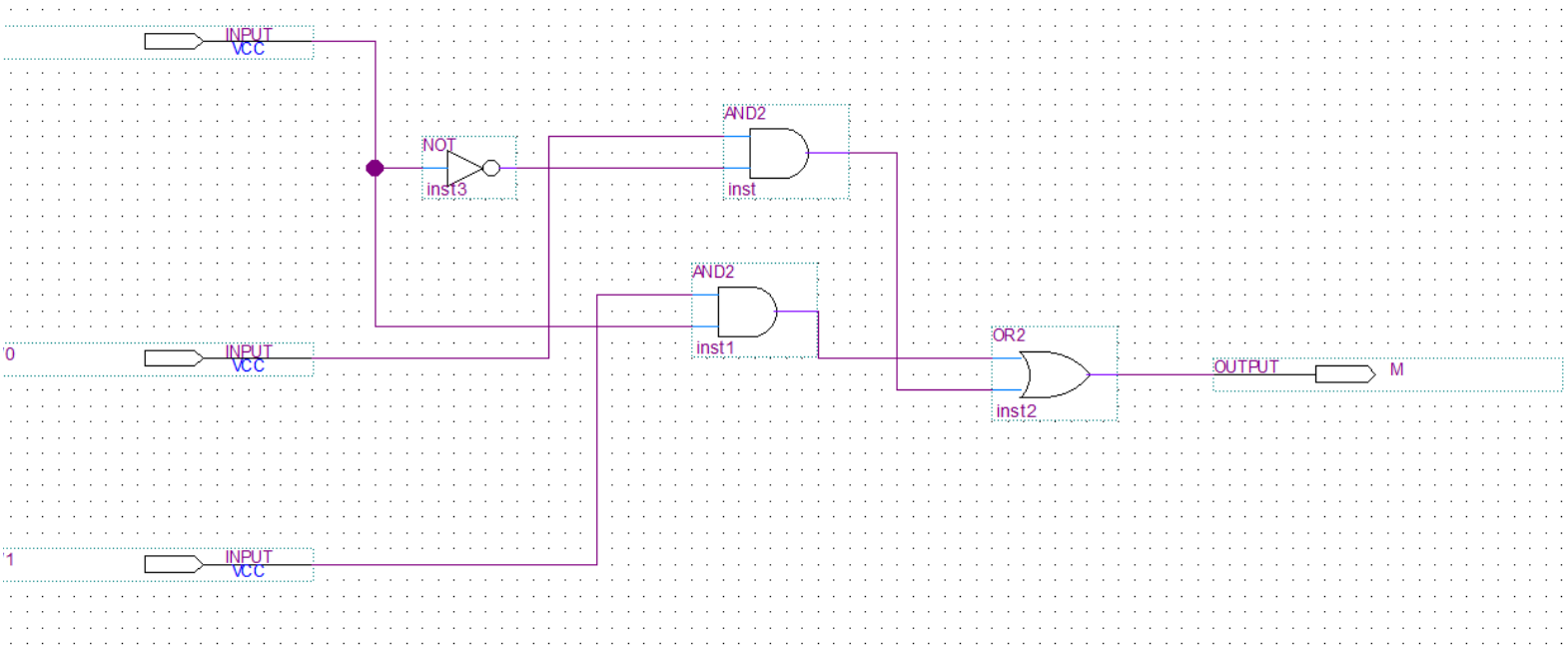



Figure 6: 2-1 Mux

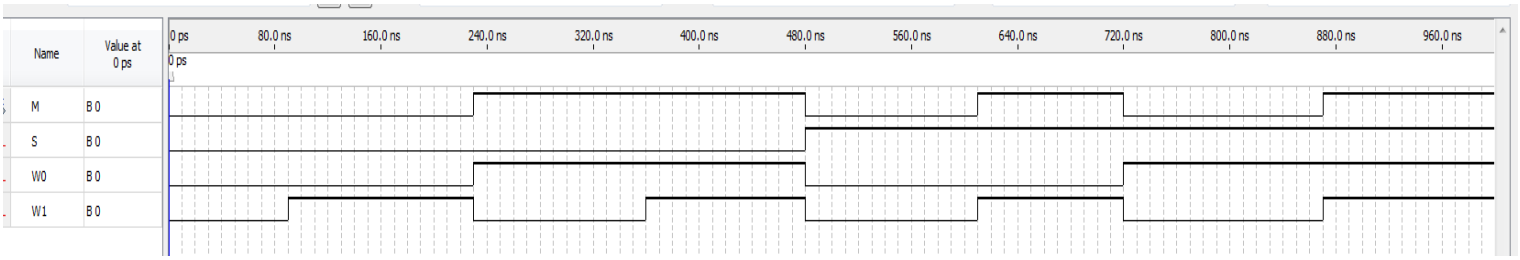



Figure 7: Waveform for 2-1 Mux

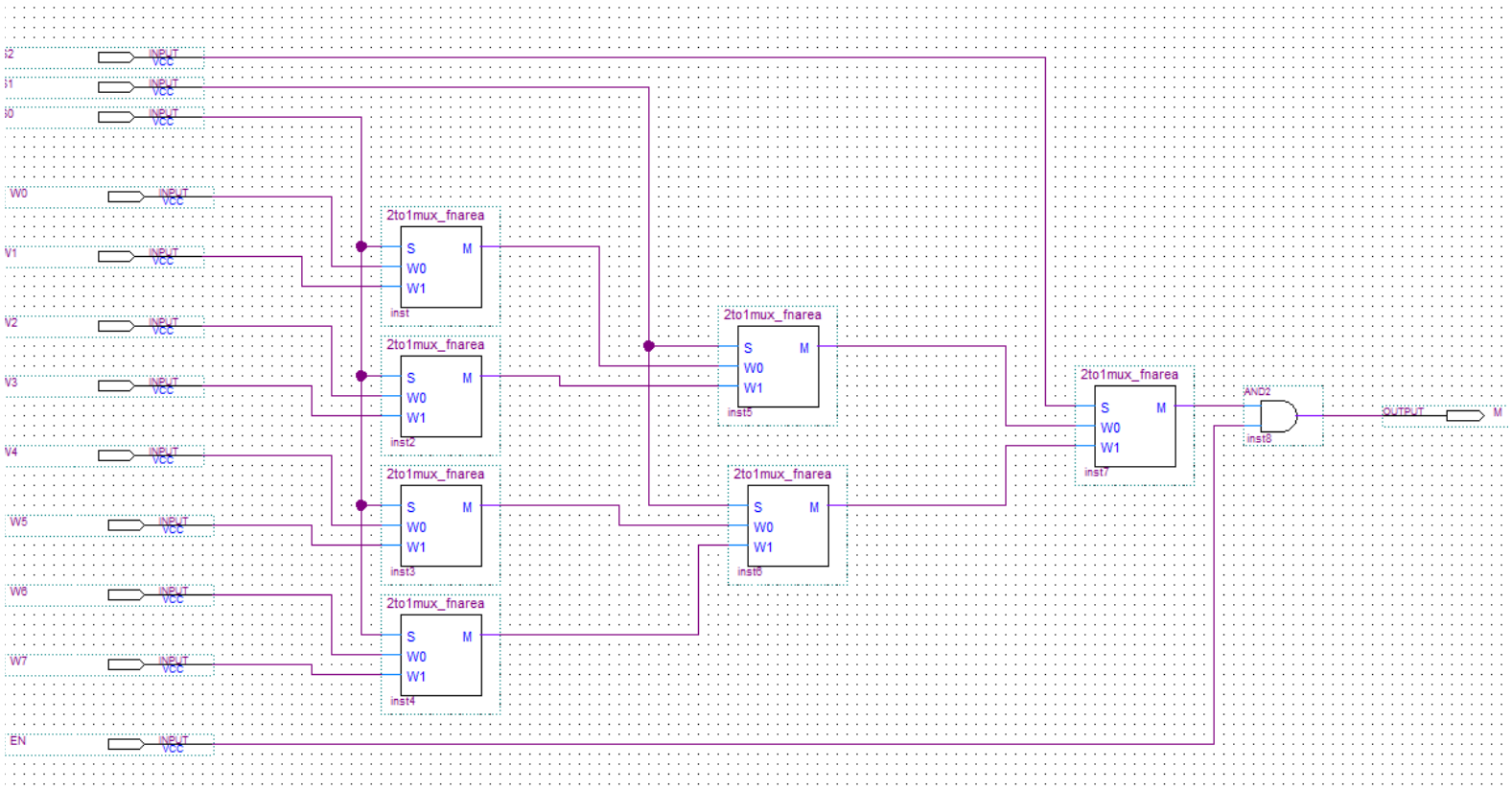
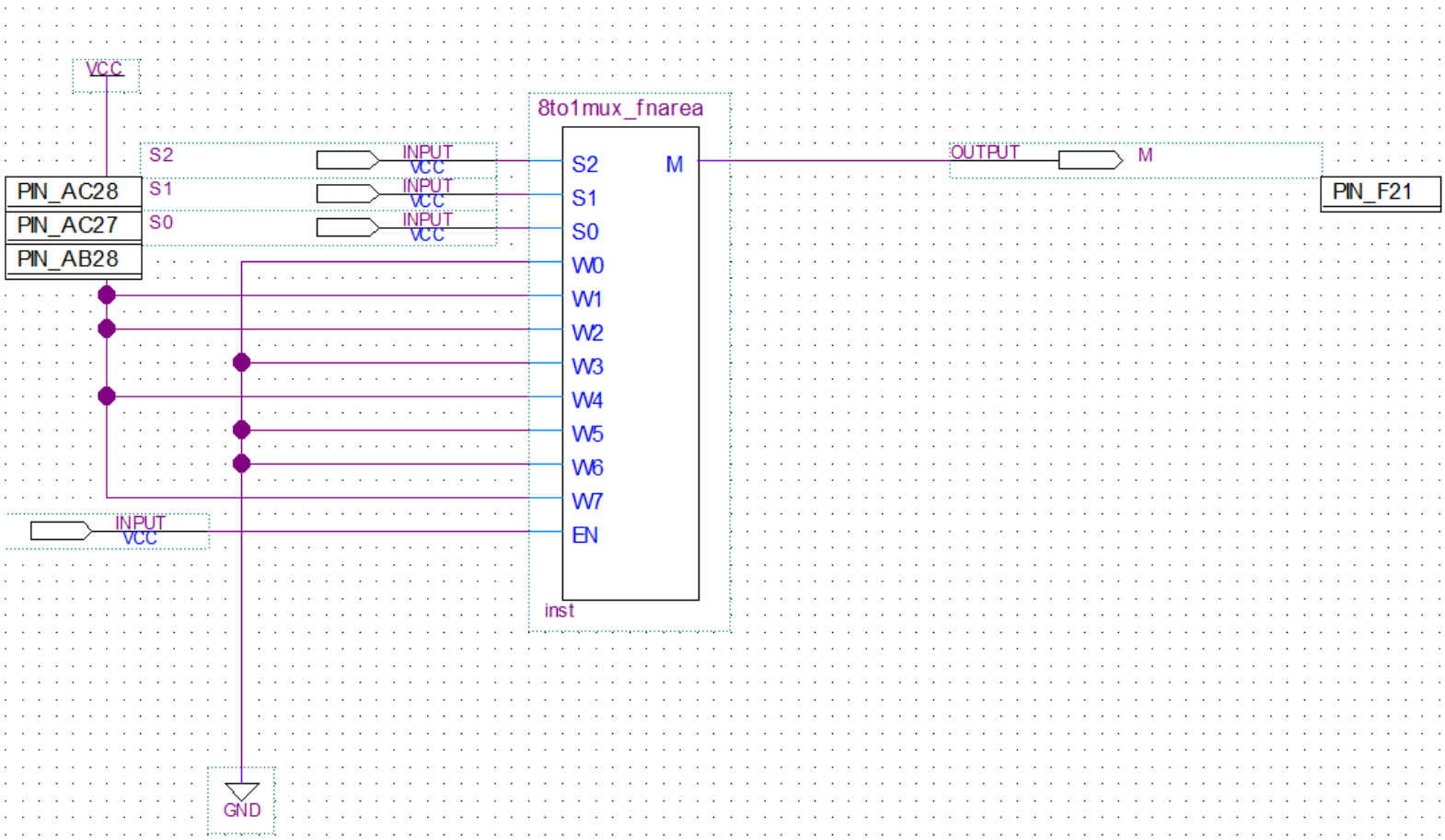



Figure 8: 8-1 Mux



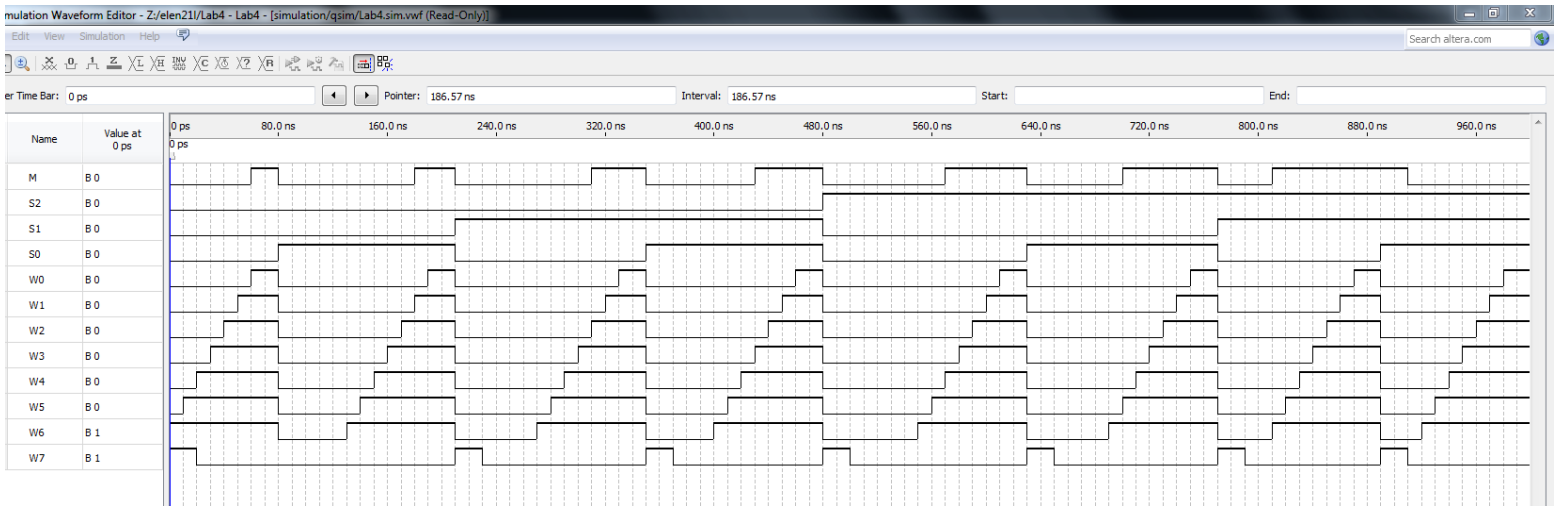




Figure 9: 8-1 Mux symbol

Figure 10: Waveform for 8-1 Mux

**Conclusion:**

This lab allowed us to further explore the topics we recently discussed in class. We used our skills of schematic drawing to create symbols for a 2-1 Mux and an 8-1 Mux, which we applied to a tangible circuit. The lab especially taught us the importance of simulating our schematic, since we had to troubleshoot properly before we could successfully run the circuit on the Altera FPGA.