ELEN/COEN 21
Laboratory 3: Two Level Circuit Design
Alex Heiler and Francesca Narea
Friday 2:15 - 5:00 PM
February 3, 2017

Introduction

During this lab, we designed, tested and implemented a highway entrance ramp metering controller, based on our pre-lab translation of the problem statement into a truth table and K-Maps. We drew our schematic in Quartus II, used Waveform for testing and worked with an Altera FPGA.

Pre-Labs

Pre-Lab #3
Francesca Narea

K-Map

CS	LS	RS	RR	CL	LL	RL
0	0	0	0	0	0	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

CL = CS
LL = ((CS)' * (RS)' * LS) + ((CS)' * RS * LS * RR)

RL = ((CS)' * (LS)' * RS) + ((CS)' * RS * LS * (RR)')

1.

CL = CS

			RS		
	0	0	0	0	
	0	0	0	0	
CS	1	1	1	1	RR
	1	1	1	1	
		LS			

Minimized SOP: CL = CS

Figure 1: Pre-Lab for Francesca Narea

2.

LL = ((CS)' * (RS)' * LS)+ ((CS)' * RS * LS * RR)

			RS		
	0	1	0	0	
	0	1	1	0	
CS	0	0	0	0	RR
	0	0	0	0	
		LS			

Minimized SOP: ((CS)' * (RS)' * LS) + ((CS)' * LS * RR)

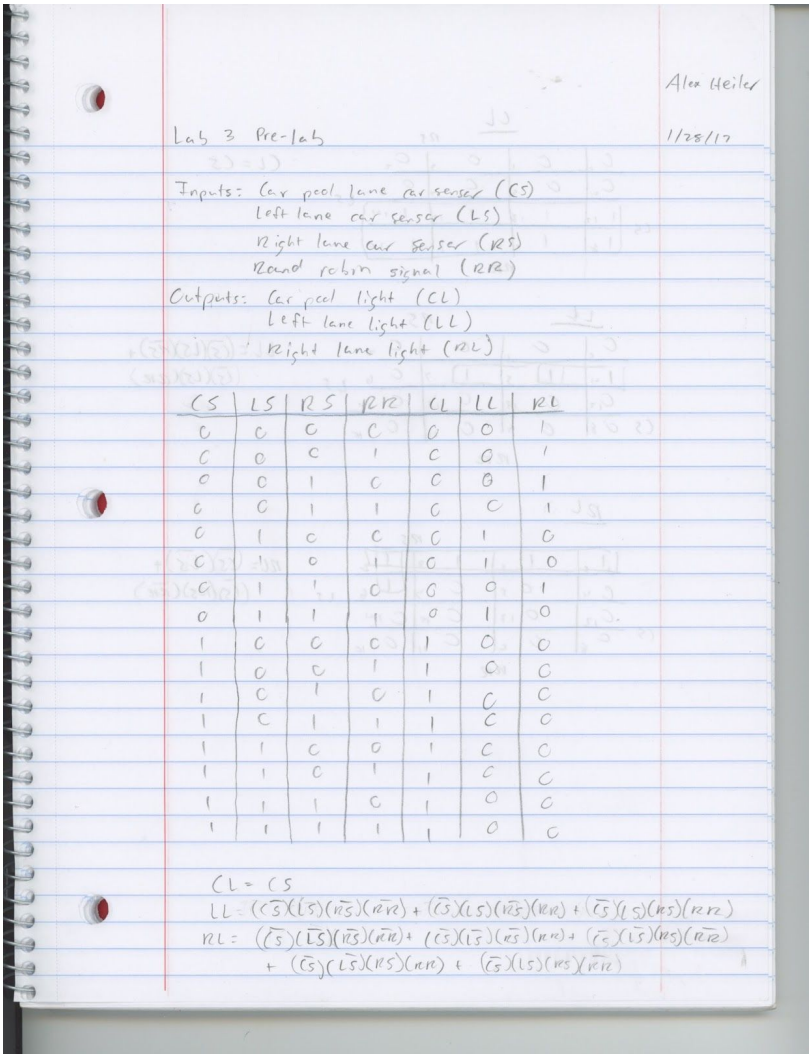
3.

RL = ((CS)' * (LS)' * RS) + ((CS)' * RS * LS * (RR)')

			RS		
	1	1	1	1	
	0	0	0	1	
CS	0	0	0	0	RR
	0	0	0	0	
		LS			

Minimized SOP: {(CS)' * (LS)' * RS)} + ((CS)' * (RR)' * (RS))

Figure 2: Pre-Lab for Francesca Narea page 2



Alex Heiler

Lab 3 Pre-lab 11/28/17

Inputs: Car pool lane car sensor (CS)
Left lane car sensor (LS)
Right lane car sensor (RS)
Round robin signal (RR)

Outputs: Car pool light (CL)
Left lane light (LL)
Right lane light (RL)

CS	LS	RS	RR	CL	LL	RL
0	0	0	0	0	0	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

$CL = CS$

$LL = (\overline{CS})(\overline{LS})(\overline{RS})(RR) + (\overline{CS})(LS)(\overline{RS})(RR) + (\overline{CS})(LS)(RS)(\overline{RR})$

$RL = (\overline{CS})(\overline{LS})(\overline{RS})(\overline{RR}) + (\overline{CS})(\overline{LS})(RS)(RR) + (\overline{CS})(LS)(RS)(\overline{RR})$
$+ (\overline{CS})(LS)(RS)(RR) + (\overline{CS})(LS)(RS)(\overline{RR})$

Figure 3: Pre-Lab for Alex Heiler page 1

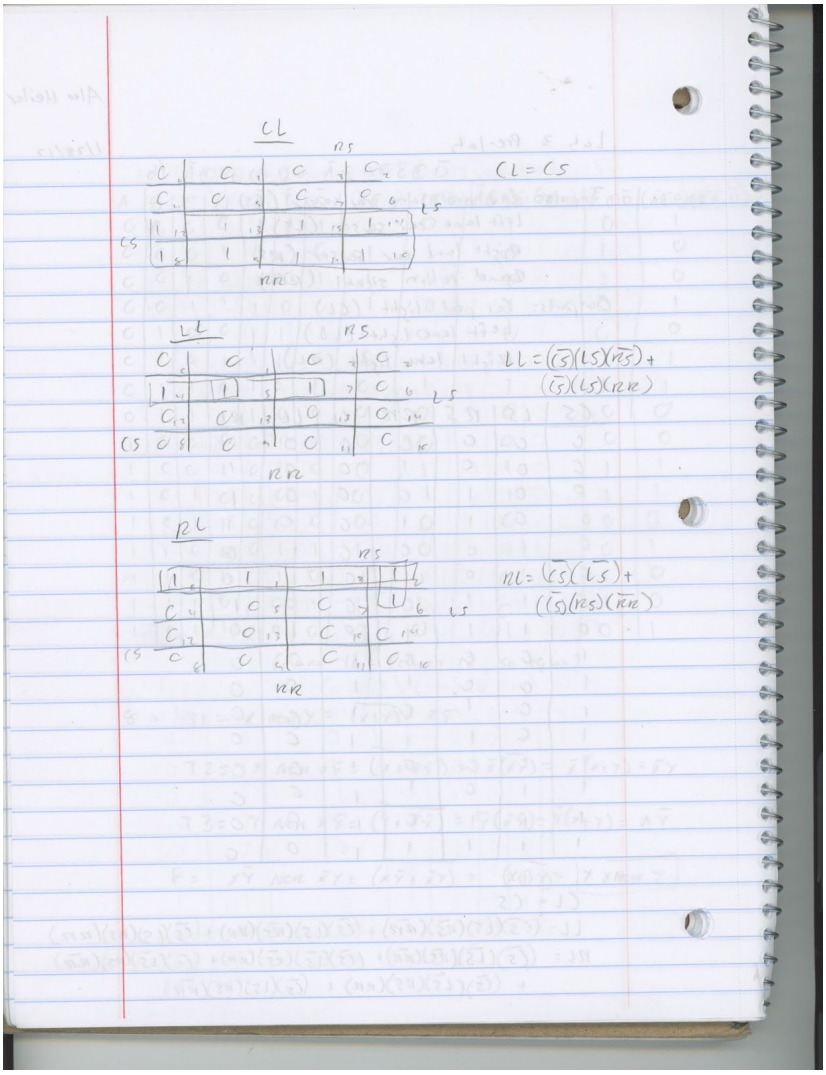


Figure 4: Pre-Lab for Alex Heiler page 2

Procedures

We initially drew our schematic for the problem statement in Quartus. In order to test our schematic, we first simulated the circuit. After verifying that the Waveform simulation displayed the correct output based on our truth tables, we then assigned pins to our inputs and outputs and downloaded our implementation of the circuit on an Altera FPGA.

Schematic

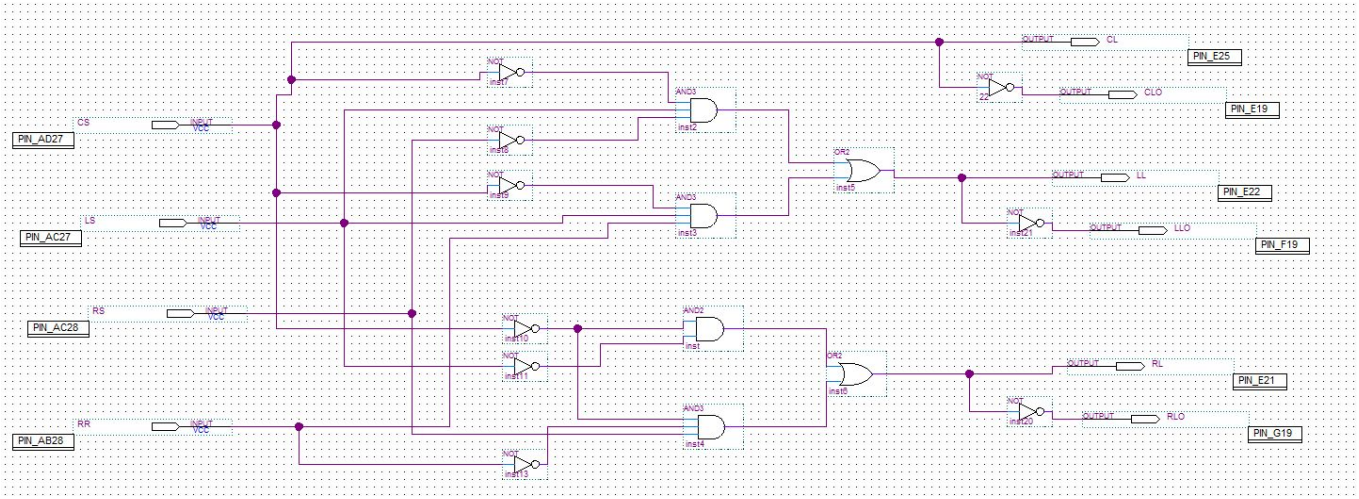


Figure 5: Quartus Schematic

Simulation Results

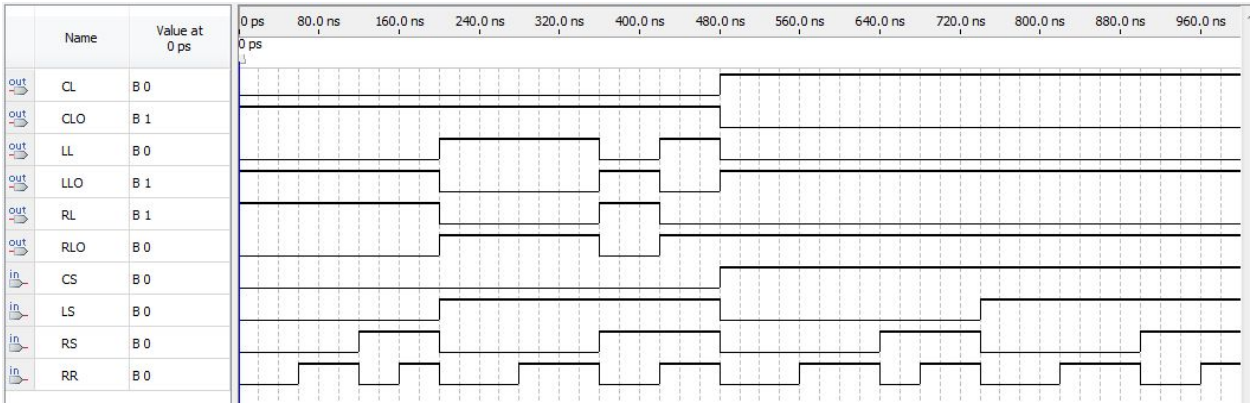


Figure 6: Waveform Simulation

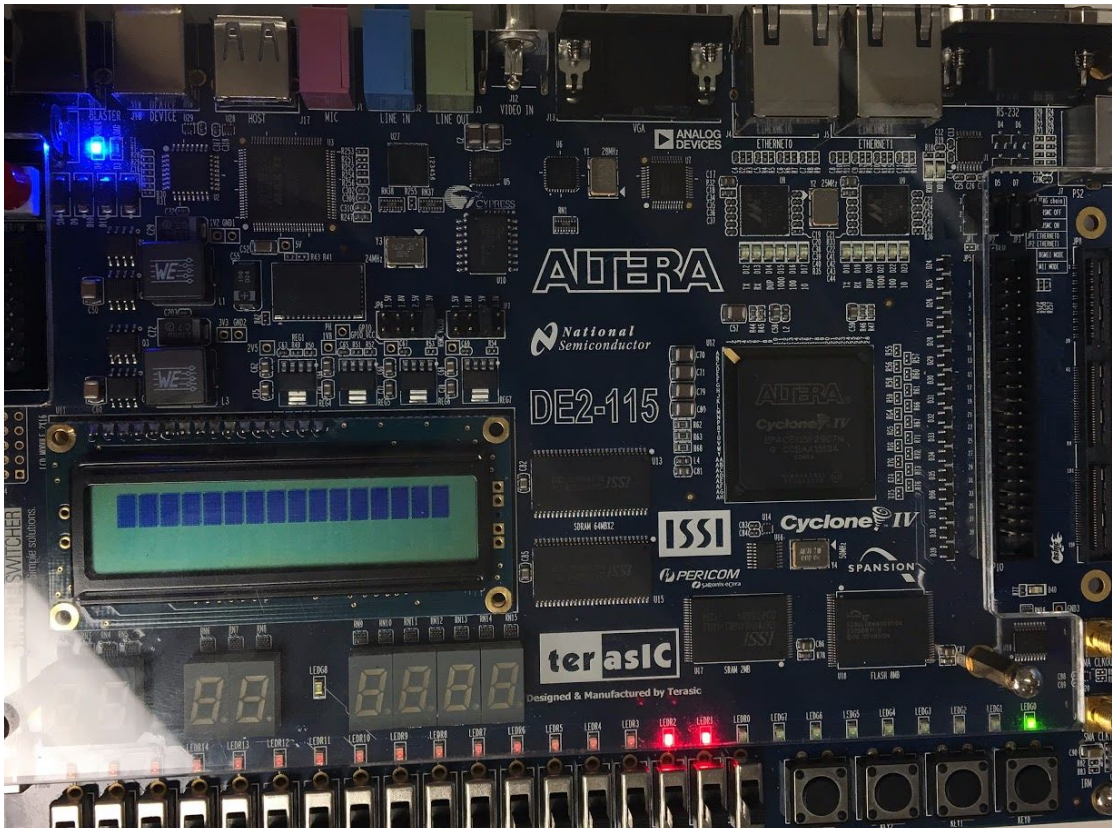


Figure 7: Functioning FPGA

Conclusion

We troubleshooted our circuit to properly model the problem statement and were able to successfully implement a two-level circuit onto the FPGA. Once we designed the initial circuit, we were able to integrate the red traffic light into the circuit so they turned on whenever the corresponding green lights were off.

Modification Analysis

To add the TM input into our circuit, we would increase the number of inputs for each AND gate by one and connect TM to the additional input of each AND gate. Because TM is ANDed to each minterm, CL, LL, and RL can only be 1 when TM is also 1. When TM is 0, the red lights for each traffic controller (CLO, LLO, and RLO) will be 1, so all the output lights will be red.