Politecnico di Torino

01NOMOQ - Integrated systems technology

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Bulk P-Type 40 nm

Group 21

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Contents

1 Introduction

The goal of this laboratory is to define the fabrication procedure for a p-mos transistor with a 40 nm channel and to study its performances.
The entire project has been developed taking into account the theoretical knowledge acquired during the course, and using the examples seen during the laboratories as a guiding path. The device has then been tested to evaluate whether its performances where in line with those of a functioning MOSFET.

2 Pen and Paper Design

The main constrain on the assignment regards the length of the device channel, in this case 40 nm, and the type of mosfet, which as already pointed out must be a p-type MOSFET.
Figure 1 portraits a generic p-type mosfet.

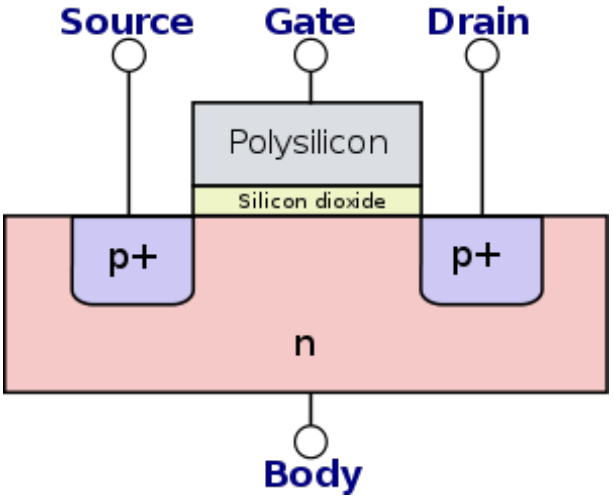
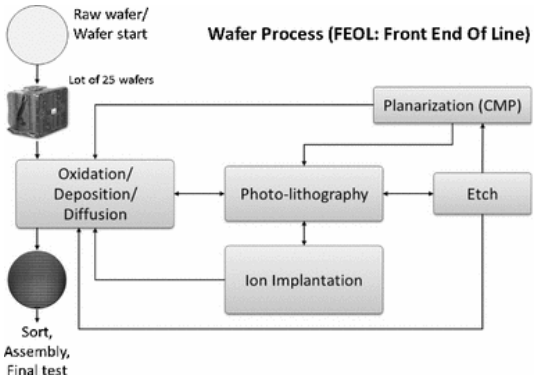


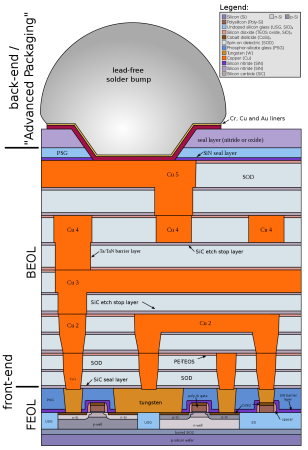
Figure 1: P-type MOSFET

The fabrication procedure can be divided into two different categories :

- **FEOL** (Front End Of Line), which refers to the fabrication procedures which are used directly on the semiconductor for the fabrication of the device, figure 2.a shows the main steps in a FEOL process flow.
- **BEOL** (Back End Of Line), creation of the interconnections among devices in order to connect them, BEOL processing generally begins when the first layer of a conducting metal is deposited on top of the wafer. Figure 2.b



((a)) FEOL process flow



((b)) Interconnections after BEOL

Figure 2

2.1 Design

The process used during the laboratories has been studied and optimized for the purpose of this project. The first step has been sizing the device to respect the constrain on the channel length. The MOSFET fabricated during the laboratory had a channel length of 180 nm, implying that to obtain a channel length of 40 nm a significant scaling down was necessary. The process flow used during the project has been very similar to the laboratory other than some improvements that have been deemed useful, namely:

- ***RMG*** replace metal gate technology, rather than using a polysilicon gate, tungsten has been employed to improve the device.
- ***Silicidation*** which is a process useful to reduce the resistance of the source and drain contacts.

Having to realize such a device whit such a short channel SCE (short channel effect) plays a significant role, causing a worsening in the device quality, these fabrication procedures along with the LDDs will help reducing its effects.

3 Fabrication

The various fabrication steps are illustrated and commented in the following section.

3.1 Step 1: Substrate

In the first step, the substrate on which the transistor will be built must be defined. The following shapes were arbitrarily selected: 10 µm and 0.3 µm.

An important aspect in the simulation of the manufacturing procedure is the definition of the mesh: this process will divide the area of the structure we are working on into the so-called mesh elements, which have a triangular shape here. The maximum precision is obtained near the upper surface of the "wafer", since the active device will be produced in this area, while moving away from it the size of the mesh elements increases in order to reduce the simulation time. This is shown in the following piece of code taken from the *sprocess_fps.cmd* command file.

```
# Declare initial grid (half #structure)

line x location= 0.0      spacing= 1.0<nm>  tag= SiTop
line x location= 50.0<nm> spacing= 10.0<nm>
line x location= 0.5<um>  spacing= 50.0<nm>
line x location= 2.0<um>  spacing= 0.2<um>
line x location= 4.0<um>  spacing= 0.4<um>
line x location= 10.0<um> spacing= 2.0<um>  tag= SiBottom

line y location= 0.0      spacing= 50.0<nm> tag= Mid
line y location= 0.3<um> spacing=50.0<nm>  tag= Right
```

Listing 1: Initial grid.

The tags *SiTop*, *SiBottom*, *Mid* and *Right* are used to define the silicon substrate:

```
region Silicon xlo= SiTop xhi= SiBottom ylo= Mid yhi= Right
```

Listing 2: Silicon substrate definition.

Only half of the device structure will be produce, and at the end of the fabrication the device will be mirrored and completed, taking advantage of its symmetry. Generally wafers are purchased already doped with the desired concentration and type of dopants. This can be done by defining an initial concentration which describes a uniform doping concentration of boron : 10^{16}cm^{-3}, here is the coding:

```
init concentration= 1.0e+16<cm-3> field= Boron
```

Listing 3: Initialize the simulation.

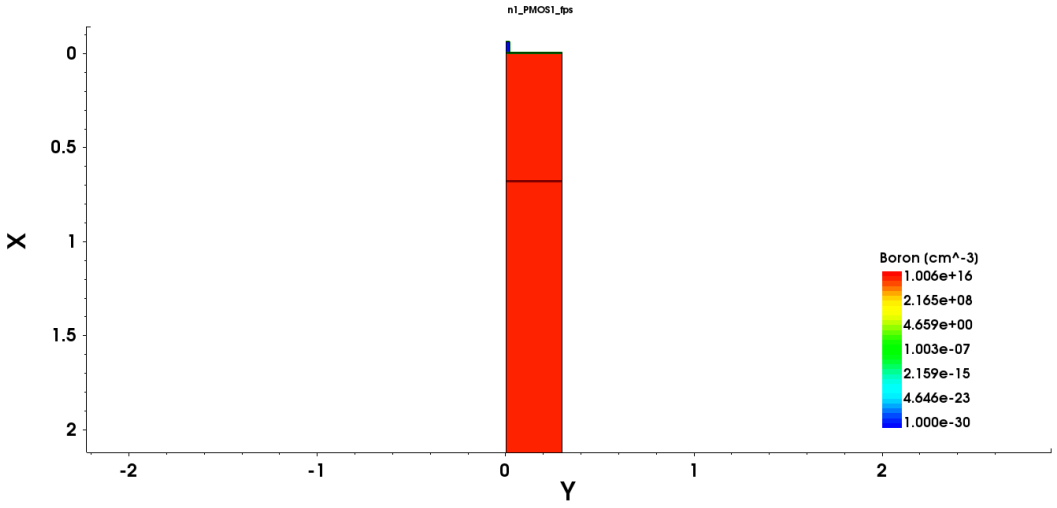


Figure 3: Boron substrate concentration.

At this point, having obtained the starting wafer, it is possible to proceed with the actual fabrication of the device.

3.2 Step 2: Phosphorus implantation

Well fabrication: being the device a p-type the substrate must be an n-type, this is achieved through an **implantation** step. The selected dose is $5 \times 10^{13}\text{cm}^{-2}$ and is implanted with an energy of 50 keV, producing a Gaussian doping profile with a peak of $2.04 \times 10^{18}\text{cm}^{-2}$, positioned at 0.08 µm.

The **implantation** procedure also requires a subsequent thermal process (annealing), necessary to repair the reticular structure which has been compromised during the implantation. The annealing will also be beneficial for the dopants activation. The annealing process has been conducted for 8 seconds at a temperature of 950 °C.

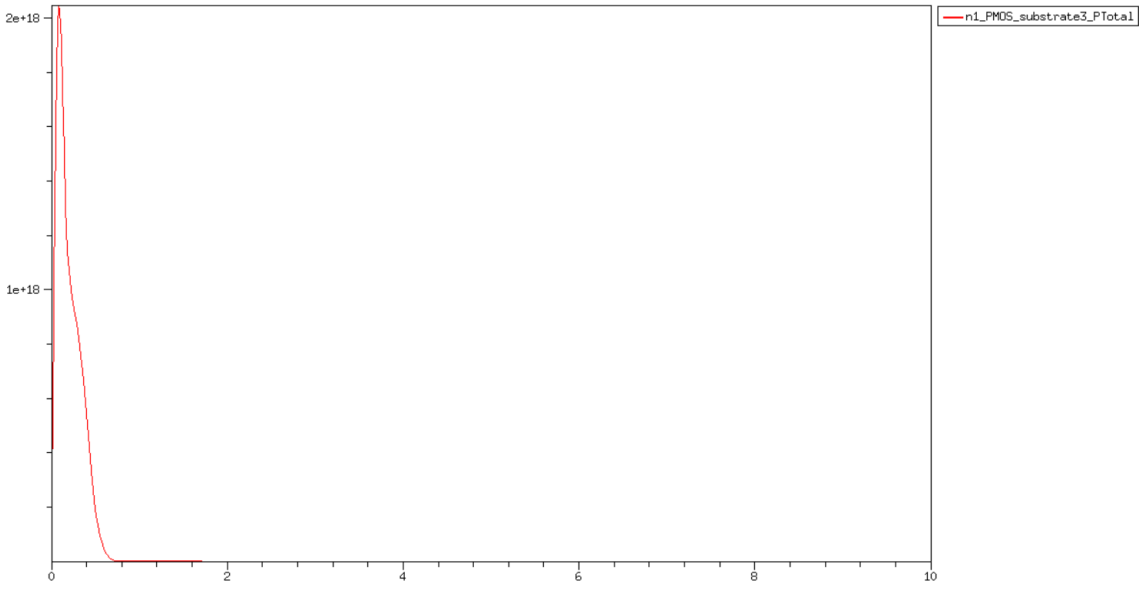


Figure 4: Phosphorus doping profile.

```
implant  Phosphorus  dose= 5.0e13<cm-2>  energy= 50<keV> tilt= 0 rotation= 0
SetPlxList   {PTotal}
WritePlx n@node@_PMOS_substrate.plx  y=0.0 Silicon


diffuse temperature= 950<C> time= 8.0<s>
SetPlxList   {PTotal}
WritePlx n@node@_PMOS_substrate3.plx  y=0.0 Silicon
```

Listing 4: P-well, anti-punchthrough Vt adjustment implants.

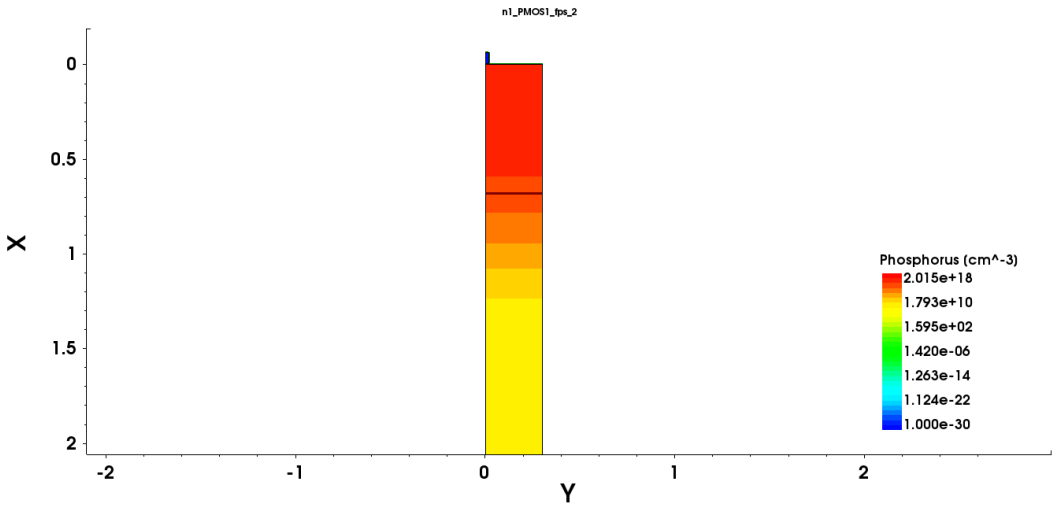


Figure 5: Phosphorus well concentration after the diffusion.

3.3 Step 3: Gate oxidation

A remeshing is now necessary, by decreasing the mesh elements in the area where the oxide will be grown the simulation will be more precise, since the electrical parameters will be deeply influenced by the quality of the gate dielectric.

```
grid set.min.normal.size= 1<nm> set.normal.growth.ratio.2d= 1.5
mgoals accuracy= 1e-5
pdbSet Oxide Grid perp.add.dist 1e-7
pdbSet Grid NativeLayerThickness 1e-7
```

Listing 5: Global Mesh settings.

High quality SiO_2 is obtained through **dry thermal oxidation**. The process requires for the wafer to be in a oxidizing atmosphere (being this a dry oxidation O_2 is the oxidant), and applying a high temperature to provide the atoms with the energy they need to react. A temperature of 850 °C was then selected and applied for 1 minute.

```
diffuse temperature= 850<C> time= 1.0<min> O2
```

Listing 6: Gate oxidation.

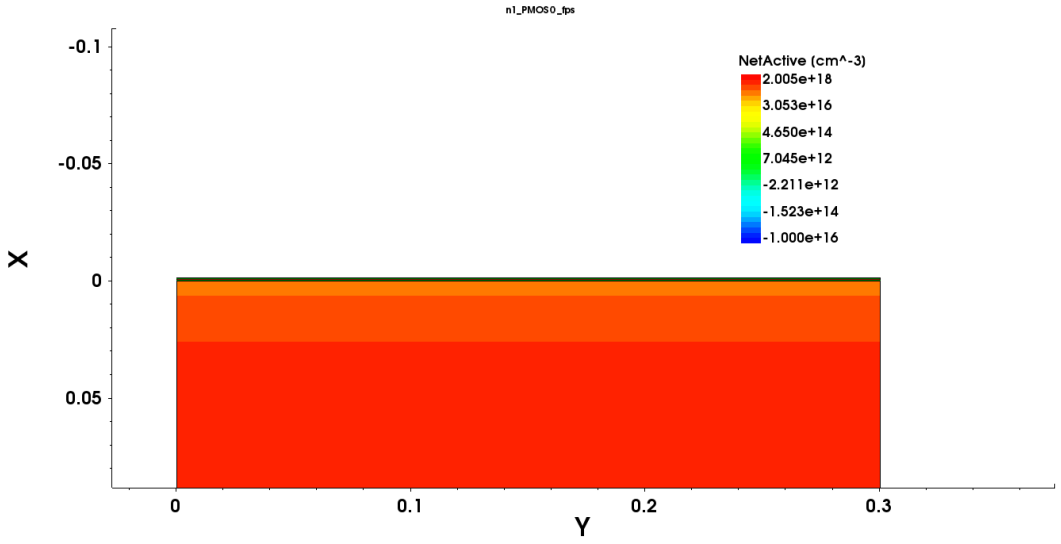


Figure 6: Oxide.

3.4 Step 4: Poly gate deposition

The next step is the creation of the gate. To deposit the *Polysilicon* uniformly over the entire surface a rate of 0.06 $\mu m/min$ for a time at 1 min has been chosen. The process is **anisotropic** since deposition only occurs from the top . The left edge is set at -1, and the right edge is defined after 19 nm. The **gate mask** is employed to protect the gate, while the remaining *Polysilicon* is etched away at a rate of 0.2 $\mu m/min$. **Anisotropic etching** is used to avoid undercuts in the figure 7. Finally, the oxide is also engraved on the entire surface, without the need for additional masks since the *Polysilicon* acts as a natural mask for this process, fig. 8. The following code shows how the gate's mask has been obtained.

```
deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.06}
mask name= gate_mask left=-1 right= 19<nm>
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.2} \
  mask= gate_mask
struct tdr= n@node@_PMOS1;
```

Listing 7: Poly gate deposition and pattern.

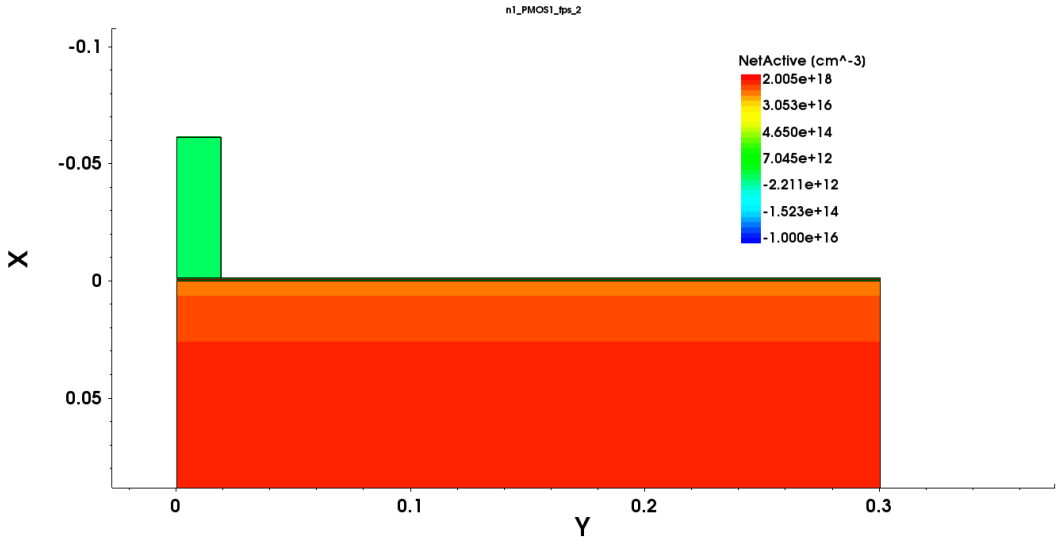


Figure 7: Polysilicon etching.

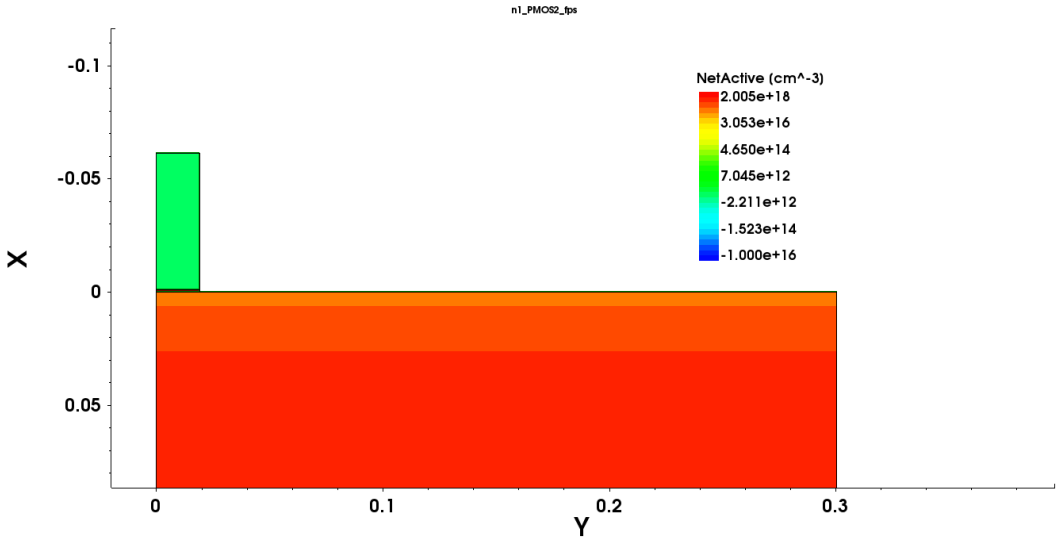


Figure 8: Oxide etching.

```
etch material= {Oxide}        type= anisotropic time= 1 rate= {0.003}
struct tdr= n@node@_PMOS2; # PolyGate
```

Listing 8: Poly gate etch.

3.5 Step 5: Polysilicon reoxidation

A thin layer of silicon oxide is grown on the *Polysilicon* to release stresses. This layer grows on all the exposed surfaces through a long **thermal annealing** process.

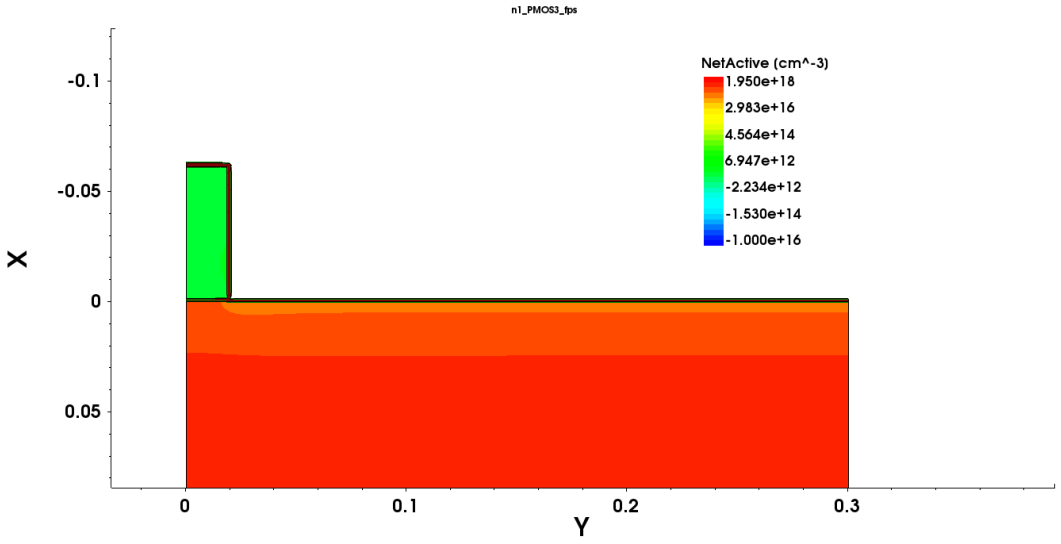


Figure 9: Polysilicon re-oxidation.

```
diffuse temperature= 850<C> time= 2.0<min>  O2
struct tdr= n@node@_PMOS3 ; # Poly Reox
```

Listing 9: Poly re-oxidation.

3.6 Step 6: LDD and Halo implantation

LDD (lightly doped drain) technology is used to reduce the doping of the drain extensions in order to prevent hot electrons injection. After performing a **remesh**, to increase the accuracy and to reduce the simulation time, the **LDD** is fabricated using an Arsenic implantation with a dose of $= 1 \times 10^{12}\text{cm}^{-2}$ at 1 keV, fig. 10.

```
refinebox Silicon min= {0.0 0.05} max= {0.1 0.12} xrefine= {0.01 0.01 0.01} \
                                                  yrefine= {0.01 0.01 0.01} add
grid remesh
implant Boron dose= 1e12<cm-2> energy= 1<keV> tilt= 0 rotation= 0
struct tdr= n@node@_PMOS4 ; # LDD Implant
diffuse temperature= 1050<C> time= 0.1<s> ; # Quick activation
struct tdr= n@node@_PMOS5 ; # LDD Diffuse
```

Listing 10: LDD implantation.

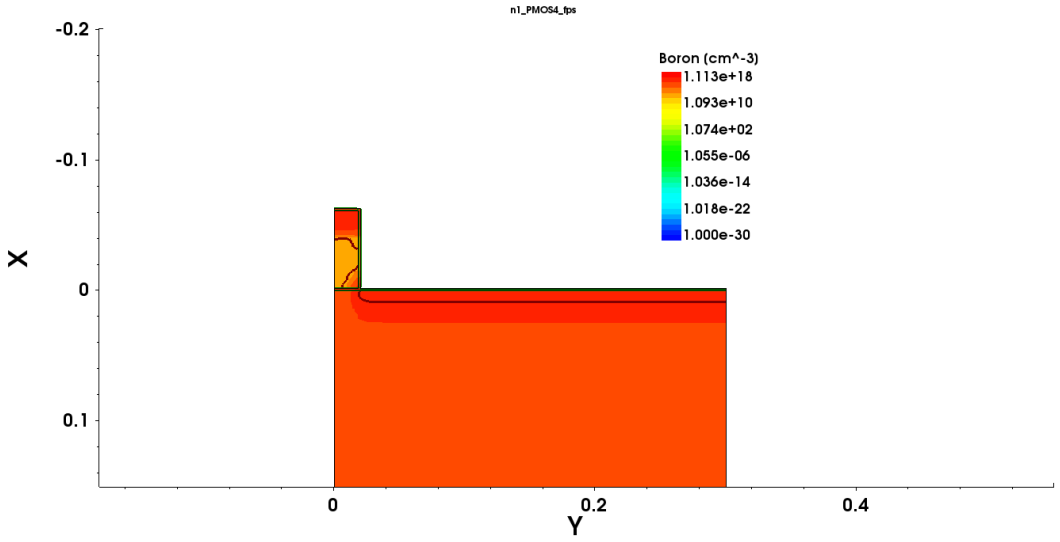


Figure 10: LDD implant.

RTA (rapid thermal annealing) is performed, which requires a very high temperature for a very small time in order to diffuse the Arsenic atoms, fig. 11.

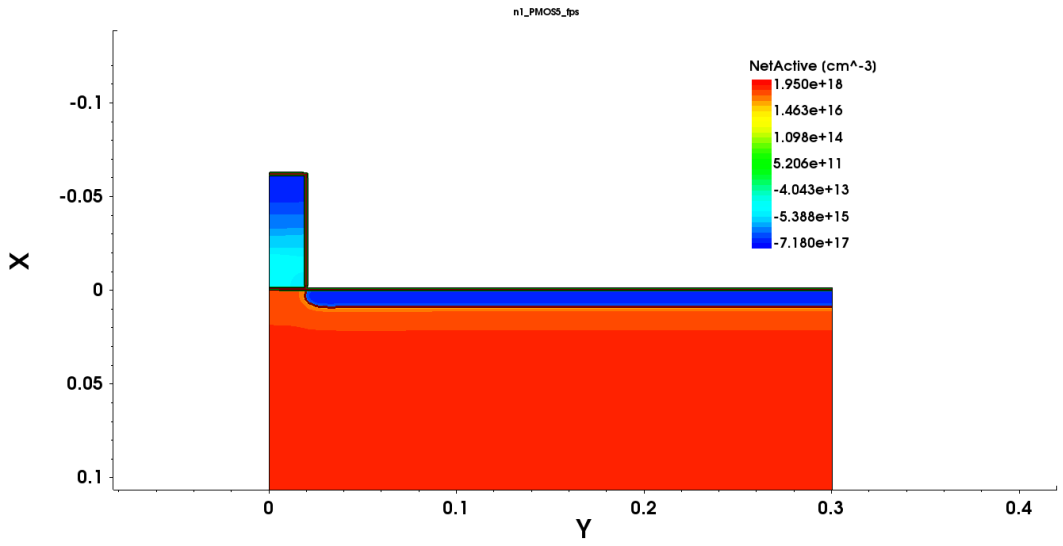


Figure 11: LDD diffusion.

At this point **HALOs** are implanted. Several implantations steps are employed, keeping the dopant dose constant but changing the incidence angle of the atoms beam by 30 each time. This procedure allows to obtain a better distribution of the atoms. **HALOs** allow to reduce the width of the depletion region near the source/substrate and drain/substrate regions, in order to reduce the effects of **DIBL**.

```
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> rotation= 0
struct tdr= n@node@_PMOS6 ; # Halo 1
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> ...
rotation= 90<degree>
struct tdr= n@node@_PMOS7 ; # Halo 1
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> ...
rotation= 180<degree>
struct tdr= n@node@_PMOS8 ; # Halo 1
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> ...
rotation= 270<degree>
struct tdr= n@node@_PMOS9 ; # Halo 1
```

Listing 11: Halo implantation.

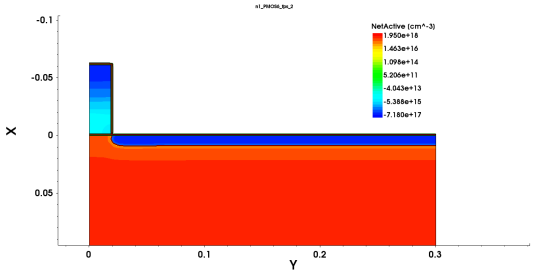


Figure 12: rotation $= 0°$

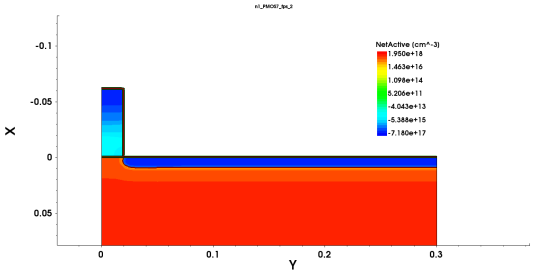


Figure 13: rotation $= 90°$

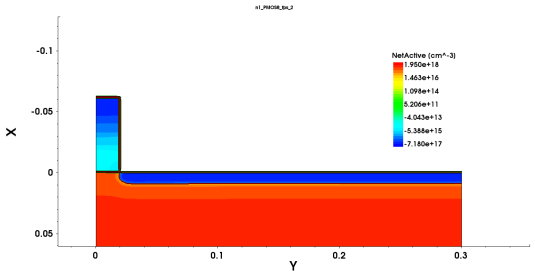


Figure 14: rotation $= 180°$

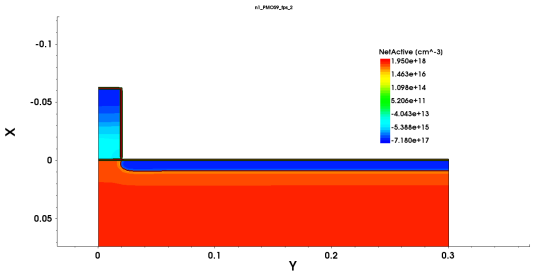


Figure 15: rotation $= 270°$

RTA is performed once again fig. 16.

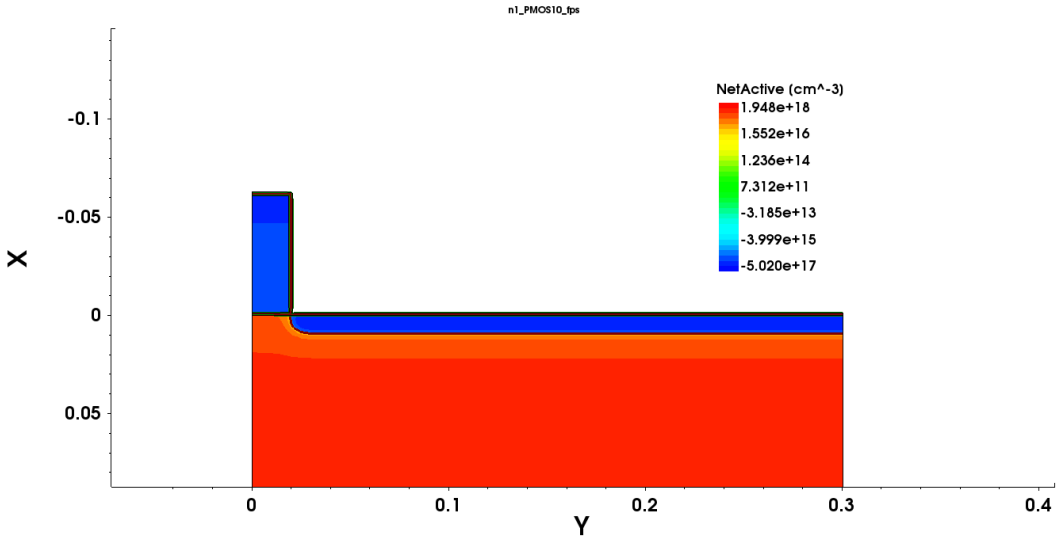


Figure 16: HALO RTA.

```
diffuse temperature= 1050<C> time= 1<s>
struct tdr= n@node@_PMOS10 ; # Halo RTA
```

Listing 12: RTA of LDD/HALO implants.

3.7 Step 7: Spacer formation

In this step *nitride* is deposited to create the spacers. **CVD** (chemical vapor deposition) of Si_3N_4 is isotropic, meaning that the deposition is perfectly uniform over the entire surface of the substrate, as can be seen from figure 17.

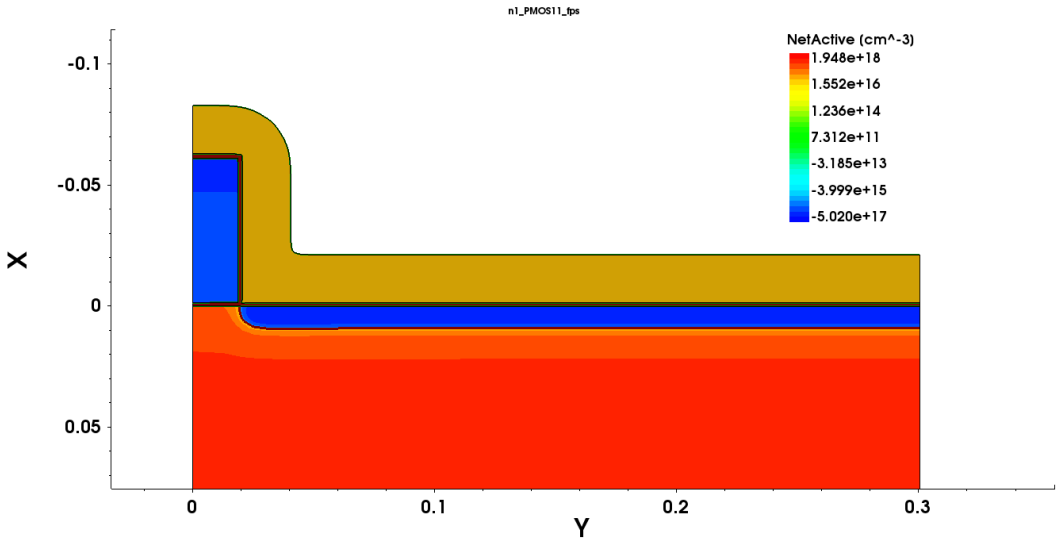


Figure 17: Spacer deposition.

Next, the nitride material is etched using **anisotropic etching**. Part of the nitride remains attached to the *Polysilicon* gate and will be used as a mask for the source/drain implantation process, fig. 18.

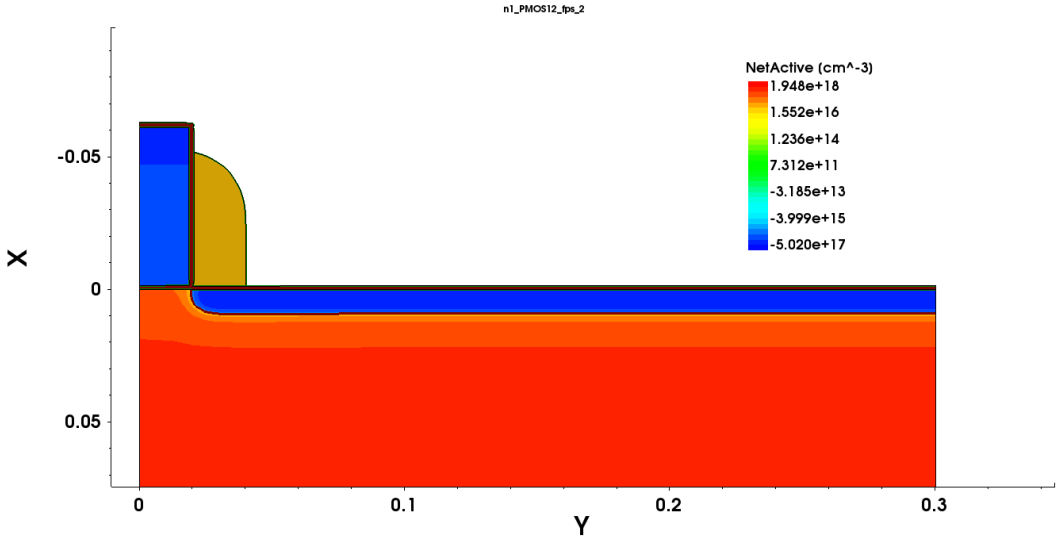


Figure 18: Spacer etching.

The thin oxide layer grown during the re-oxidation of the *Polysilicon* is also etched, figure 19.

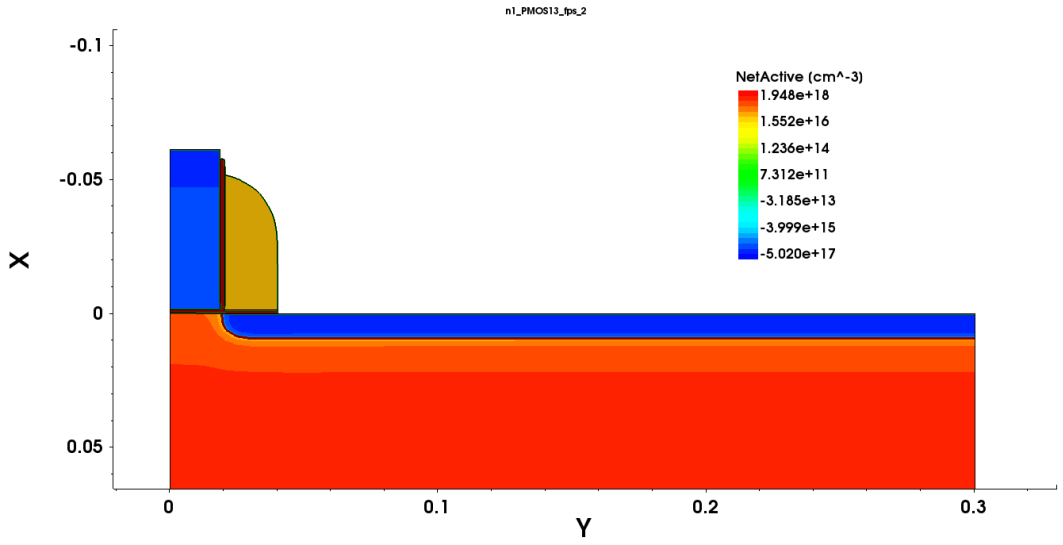


Figure 19: Spacer oxide removal.

```
deposit material= {Nitride} type= isotropic  time= 1 rate= {0.02}
struct tdr= n@node@_PMOS11 ; # Spacer deposition
etch    material= {Nitride} type= anisotropic time = 1 rate= {0.03} ...
isotropic.overetch= 0.01
struct tdr= n@node@_PMOS12 ; # Spacer etch
etch    material= {Oxide}   type= anisotropic time= 1 rate= {0.005}
struct tdr= n@node@_PMOS13 ; # Spacer oxide removal
```

Listing 13: Nitride spacer.

3.8 Step 8: S/D implantation

Subsequently, the doping of the source/drain region is carried out, a remeshing is first employed. An high dose of dopants is used to obtain reduce the resistivity. The inclination angle has been chosen to reduce channeling.

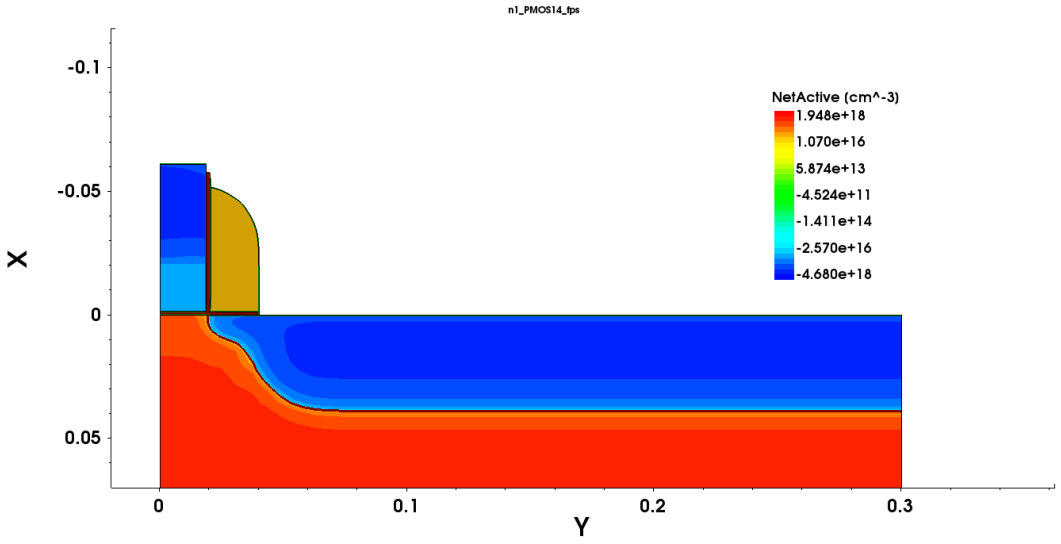


Figure 20: P^+ implantation.

Finally a **RTA** is done to diffuse the *Boron* inside the source/drain regions.

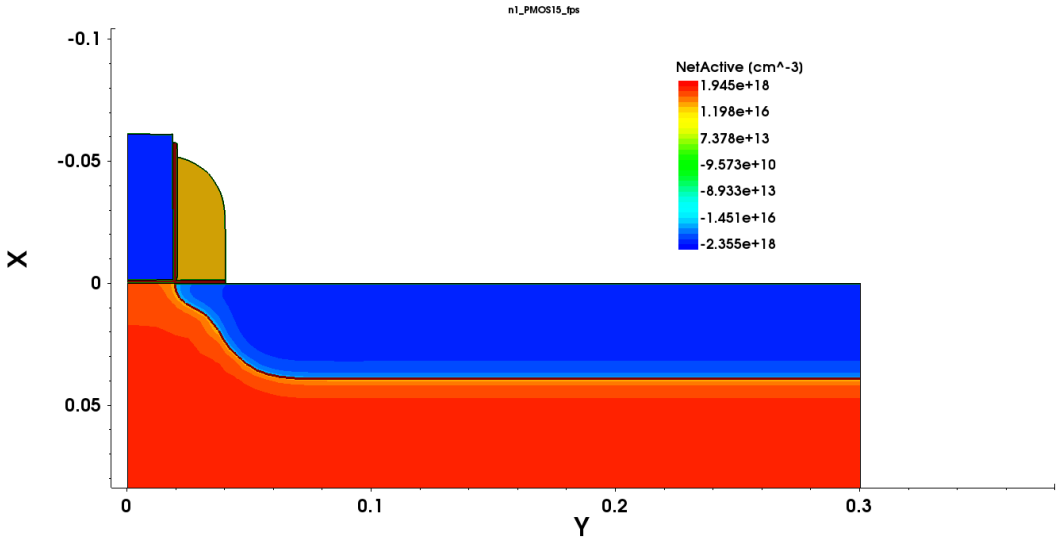


Figure 21: Final RTA.

3.9 Step 9: RMG

The **RMG** technology, that stands for Replace metal gate, is used to define the gate structure. Using a gate stack allows more freedom to improve the performances of the transistor, while maintaining the integrity of the dielectric.

```
refinebox Silicon min= {0.04 0.12} max= {0.18 0.4} xrefine= {0.01 0.01 0.01} \
                                                   yrefine= {0.05 0.05 0.05} add
grid remesh
implant Boron dose= 1e13<cm-2> energy= 4<keV> tilt= 7<degree> ...
rotation= -90<degree>
struct tdr= n@node@_PMOS14 ; # P+ implantation

# Final RTA
# --------------------------
diffuse temperature= 1050<C> time= 1<s>
struct tdr= n@node@_PMOS15 ; # Final RTA
```

Listing 14: P+ implantation.

The Polysilicon gate is etched away while masking the surrounding are to avoid it being damaged. The final result is shown in figure 22.

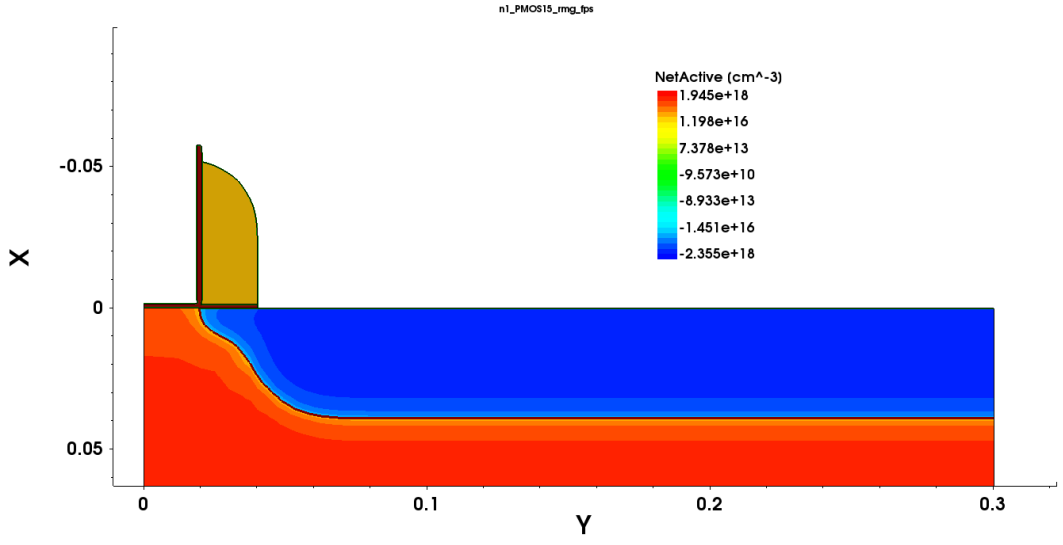


Figure 22: Etching of Polysilicon gate.

At this point it is possible to deposit the new layer of **high-k material**, in this case Hafnium has been chosen which has a dielectric constant equal to 24. A material with an high dielectric constant is used to improve the performances. However, performance at high operating clock frequency can be negatively impacted by and increased gate capacitance, even if the device current is improved. To minimize this problem when using High-k material it is mandatory to concurrently scale down the gate capacitance by reducing the gate length of the transistor. Figure 23.

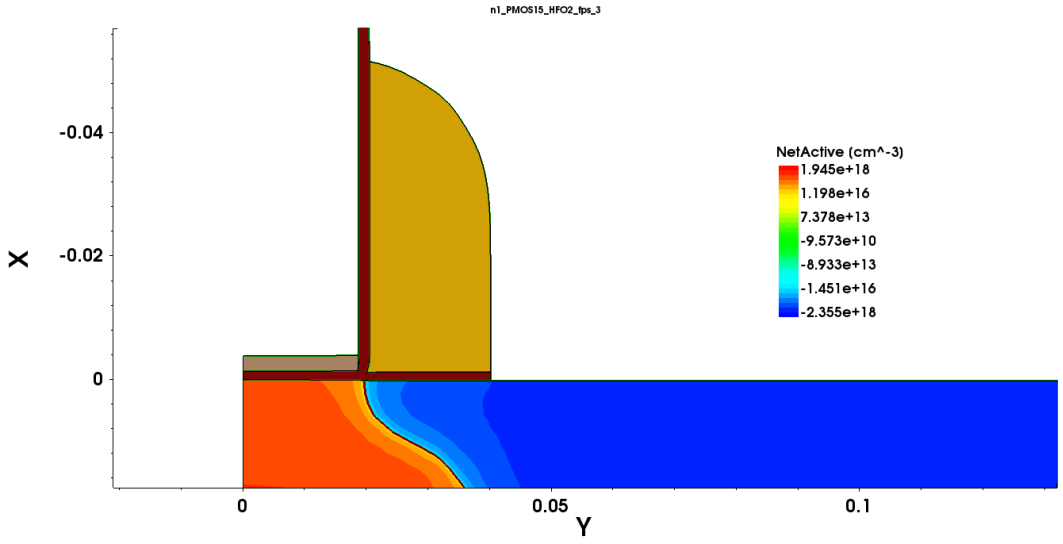


Figure 23: Deposition of HK material.

```
mask name= rmg_mask left= 0.01864<um> right= 0.30<um>
etch material= {PolySilicon} type= isotropic time= 1 rate= {0.07} mask= rmg_mask
struct tdr= n@node@_PMOS15_rmg;

#HK material deposizione anisotropic
deposit material= {HfO2} type= anisotropic time= 1 rate= {0.0025} mask= rmg_mask
struct tdr= n@node@_PMOS15_HFO2 ; # Hafnium Dioxide Dep
```

Listing 15: RMG.

The last point of this step is the definition of gate electrode by deposition of a metal to compose what is named metal-gate. The chosen metal is the Tungsten for its higher melting temperature with respect to other common metals like Alumina and for its low electromigration and high current density.

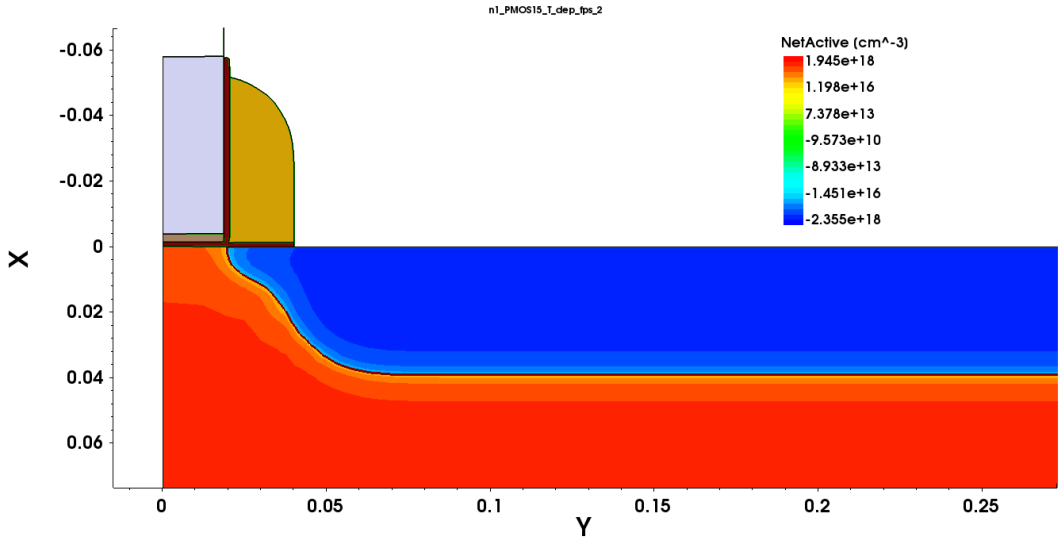


Figure 24: Tungsten deposition and etching.

```
deposit material= {Tungsten} type= anisotropic time= 1 rate= {0.054} ...
mask= rmg_mask
mask name= gate_mask_2 left= 0.01889<um> right= 0.055<um> negative
etch material= {Tungsten} type= anisotropic time= 1 rate= {0.15} ...
mask= gate_mask_2
struct tdr= n@node@_PMOS15_T_dep ; # Tungsten deposition and etching
```

Listing 16: Tungsten deposition and etching.

RMG isn't always employed. For low power applications, where is not required an aggressive EOT and an ultra low threshold voltage, a process without RMG is arguably the most common choice, however, for high performance applications, this solution allows to meet the performance requirements.

3.10 Step 10: Silicidation

Another optimization is what is named **Silicidation**. This technique is used to create a better interface between metal contacts and the heavily doped active regions. This is done to reduce the chances of electromigration. The chosen material, Titanium dilicide, is characterized by low resistivity that allows to obtain low parasitic resistances in the Metal-Silicon junction area. A mask is employed, the Titanium is deposited and then a drive in procedure takes place for 1 second at a temperature of $650°C$.

```
mask name= silicide_mask left= 0.00<um> right= 0.04081<um>
deposit material= {Titanium} type= anisotropic time= 1 rate= {0.0015} ...
mask= silicide_mask
struct tdr= n@node@_PMOS16_silicide_dep; # SilicideMask
diffuse temperature= 650<C> time= 1.00<s>
struct tdr= n@node@_PMOS16_silicide_diff;
```

Listing 17: Silicidation.

The layer as can be observed in figure 25 and 26 is very thin.

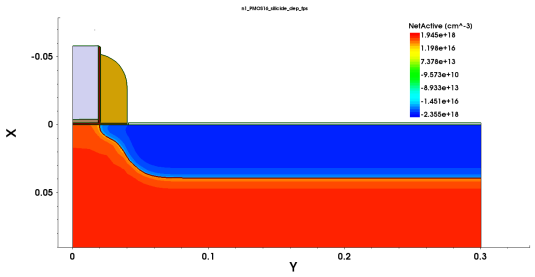


Figure 25: Titanium deposition.

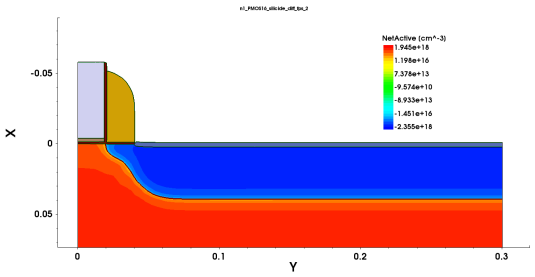


Figure 26: Diffusion process.

3.11 Step 11: Contacts

The last step is relative to the **isotropic deposition** of the metal contacts, starting by metal deposition. The chosen metal is the same used for the gate, Tungsten. In following step a mask is used to avoid metal deposition on the gate and on the spacers. Figure 27, 28 and 29 show the procedure results.

```
deposit material= {Tungsten} type= isotropic time= 1 rate= {0.02} ...
mask= silicide_mask
struct tdr= n@node@_PMOS17 ; # W deposition
mask name= contacts_mask left= 0.0<um> right= 0.25<um>
etch material= {Tungsten} type= anisotropic time= 1 rate= {0.15} ...
mask= contacts_mask
struct tdr= n@node@_PMOS18 ; # W etching 1
etch material= {Tungsten} type= anisotropic time= 1 rate= {0.15} ...
mask= gate_mask_2
struct tdr= n@node@_PMOS19 ; # W etching 2
```

Listing 18: Contacts.

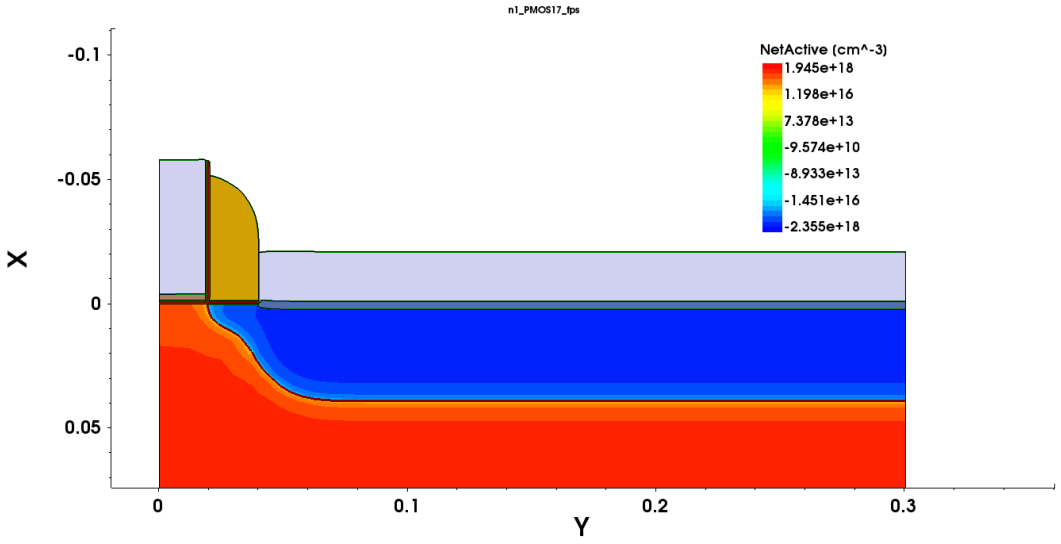


Figure 27: Tungsten deposition.

Using the first mask it is possible to cover the left part and protect from tungsten etching, fig. 28.

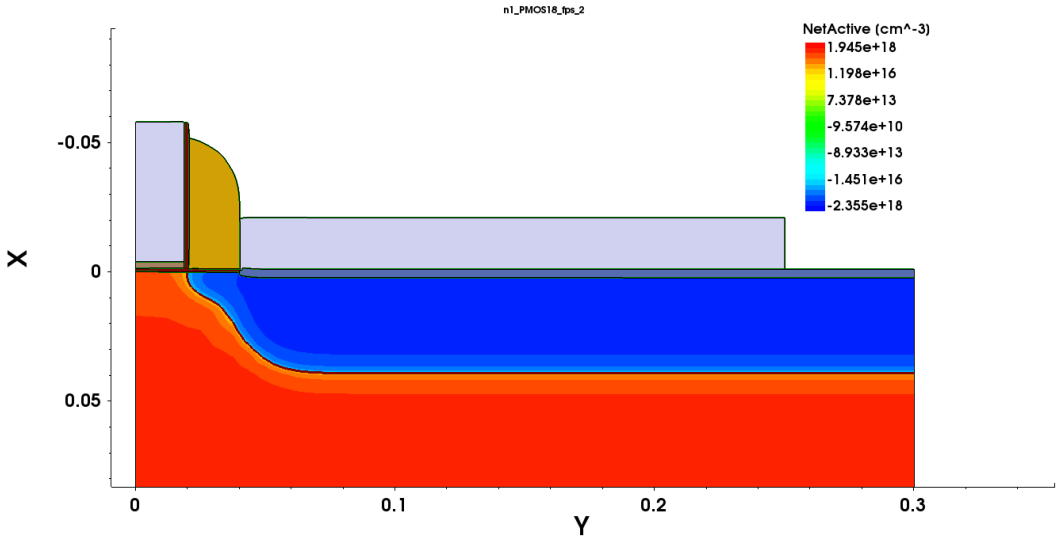


Figure 28: Tungsten first etching.

The second mask is used to separate the contact from the spacer, fig. 29.

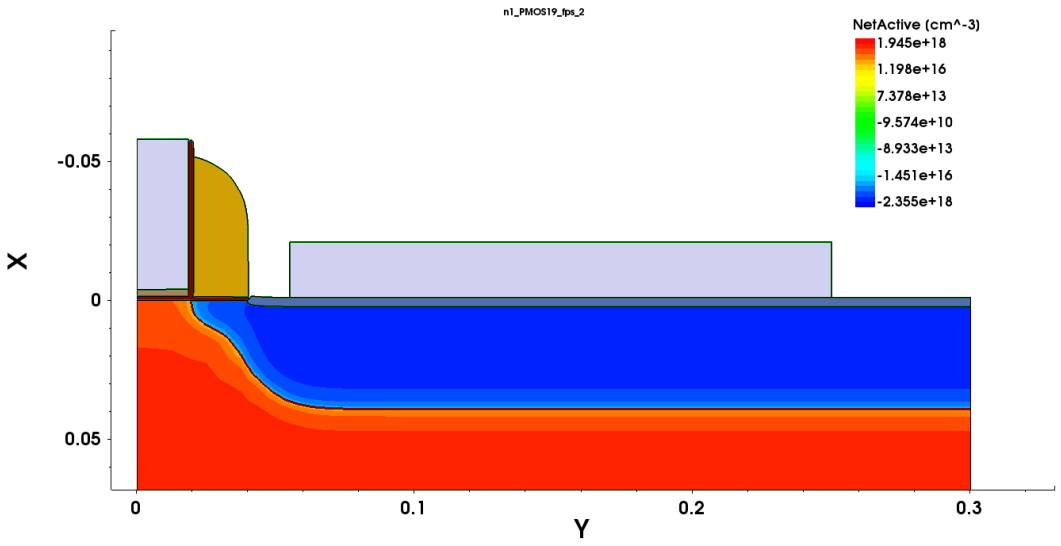


Figure 29: Tungsten second etching.

3.12 Step 12: Complete structure

In this step the final **symmetrical structure** is obtained by simply mirroring the obtained section and unifying the two parts.

Contact definition is also necessary, to define where the testing "probes" during the simulations will be positioned. The coding necessary for both this procedures has been attached underneath.

The final transistor structure is portrayed in figure 30.

```
transform reflect left

# save final structure:
#  - 1D cross sections
struct tdr= n@node@_PMOS20 ; # Final

SetPlxList   {PTotal NetActive}
WritePlx n@node@_PMOS_channel.plx  y=0.0 Silicon

SetPlxList   {BTotal PTotal NetActive}
WritePlx n@node@_PMOS_ldd.plx y=0.028 Silicon

SetPlxList   {BTotal PTotal NetActive}
WritePlx n@node@_PMOS_sd.plx y=0.19 Silicon

contact bottom name = substrate Silicon
contact name = gate x = -0.04 y = 0.0 Tungsten
contact name = source x = -0.019 y=-0.2 Tungsten
contact name = drain x = -0.019 y = 0.2 Tungsten
struct tdr= n@node@_presimulation
```

Listing 19: Final structure: reflect and contacts.

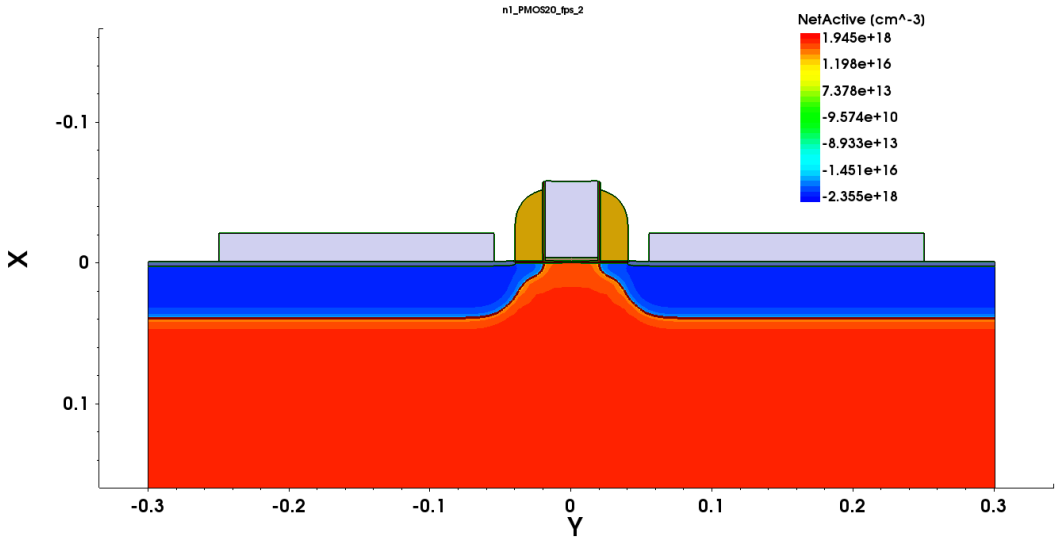


Figure 30: PMOS complete structure.

4 Simulation

A simulation of the device behaviour allows to verify its properties. The most significant analysis regards the control of the channel. In other words the ability to control the area underneath the gate to control conduction between the source and drain contacts through the gate potential. To do so the files *sdevicedes.cmd* and *sdevice.par* have been modified to allow testing of this transistor, the results have been plotted using Sentaurus Inspect. Figure 31 shows the $I_{ds} - V_{gs}$ curve:

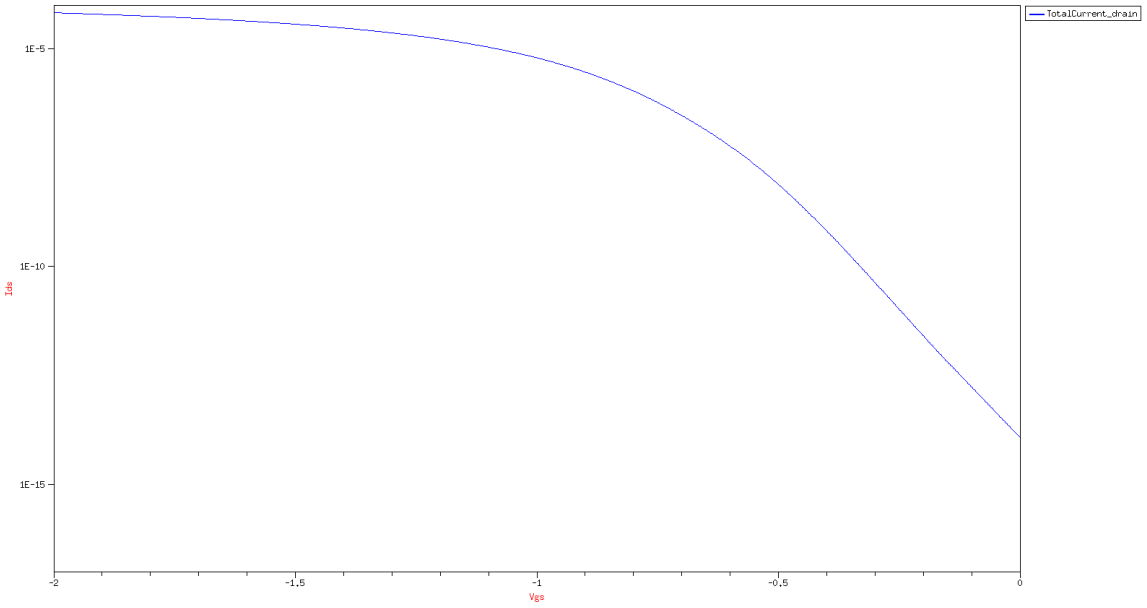


Figure 31: $I_{ds} - V_{gs}$ characteristic, current in logarithmic scale.

The plotted curve shows how the the current can be computed through the gate voltage (assuming the potential on the source to be zero), the two axes are:

- X-axis gate-source voltage V_{gs}.
- Y-axis logarithmic plot of the current flowing between source and drain I_{ds}.

The drain voltage has been set to be $V_d = -1\ V$ whilst the gate potential has been varied from 0 to -2 volts. The collected data showed that:

- $I_{on} \approx 20\ \mu A$
- $I_{off} \approx 1.6 \cdot 10^{-14}\ A$

Hence the ratio $\frac{I_{on}}{I_{off}}$ is equal to:

$$\frac{I_{on}}{I_{off}} = 1.25 \cdot 10^{9}$$

Such a ratio would be great news on a real transistor, since it would imply the presence of very low leakage currents, and improved device performances. This results show that the chosen procedure allowed to minimize the short channel effects. Being the obtained value of I_{off} so low and I_{on} not significantly high this device resembles the characteristics of a LSTP, low stand-by technology power transistor. The value of the threshold voltage has been extracted from from fig. 32:

$$V_{th} \ = \ -0.75\ V$$

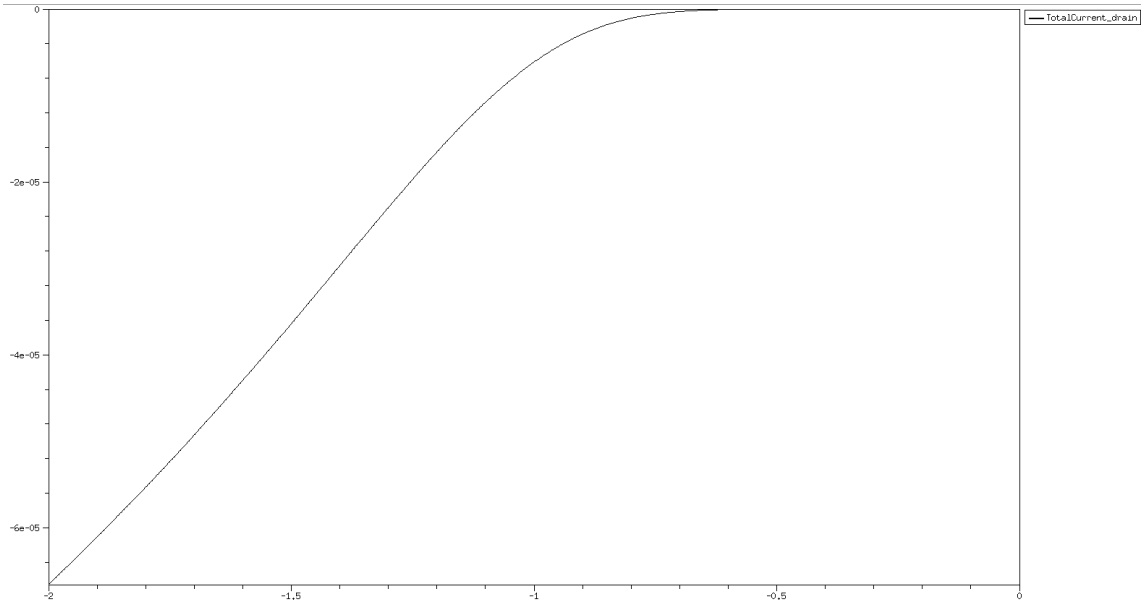


Figure 32: $I_{ds} - V_{gs}$ characteristic.

5 Appendix

5.1 sprocess commands

```
# 2D pMOSFET (40nm technology)
# ------------------------------

math coord.ucs

# Declare initial grid (half #structure)
# ----------------------------------------

line x location= 0.0       spacing= 1.0<nm>  tag= SiTop
line x location= 50.0<nm> spacing= 10.0<nm>
line x location= 0.5<um>  spacing= 50.0<nm>
line x location= 2.0<um>  spacing= 0.2<um>
line x location= 4.0<um>  spacing= 0.4<um>
line x location= 10.0<um> spacing= 2.0<um>  tag= SiBottom

line y location= 0.0       spacing= 50.0<nm> tag= Mid
line y location= 0.3<um> spacing=50.0<nm>  tag= Right

# Silicon substrate definition
# ------------------------------
region Silicon xlo= SiTop xhi= SiBottom ylo= Mid yhi= Right

# Initialize the simulation
# ---------------------------
init concentration= 1.0e+16<cm-3> field= Boron
AdvancedCalibration

# P-well, anti-punchthrough & Vt adjustment implants
# ----------------------------------------------------
implant  Phosphorus  dose= 5.0e13<cm-2>  energy= 50<keV> tilt= 0 rotation= 0
SetPlxList   {PTotal}
WritePlx n@node@_PMOS_substrate.plx  y=0.0 Silicon

#implant  Phosphorus  dose= 1.0e13<cm-2>  energy= 95<keV> tilt= 0 rotation= 0
#SetPlxList   {PTotal}
#WritePlx n@node@_PMOS_substrate1.plx  y=0.0 Silicon
#implant  Phosphorus  dose= 2.0e12<cm-2>  energy= 50<keV> tilt= 0 rotation= 0
#SetPlxList   {PTotal}
#WritePlx n@node@_PMOS_substrate2.plx  y=0.0 Silicon

diffuse temperature= 950<C> time= 8.0<s>
SetPlxList   {PTotal}
WritePlx n@node@_PMOS_substrate3.plx  y=0.0 Silicon

# Global Mesh settings for automatic meshing in newly generated layers
# ----------------------------------------------------------------------
grid set.min.normal.size= 1<nm> set.normal.growth.ratio.2d= 1.5
mgoals accuracy= 1e-5
pdbSet Oxide Grid perp.add.dist 1e-7
pdbSet Grid NativeLayerThickness 1e-7

# Gate oxidation
# ----------------
diffuse temperature= 850<C> time= 1.0<min> O2

# Poly gate deposition
# ----------------------
deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.06}

# Poly gate pattern/etch
# ------------------------
mask name= gate_mask left=-1 right= 19<nm>
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.2} \
  mask= gate_mask
struct tdr= n@node@_PMOS1;
etch material= {Oxide}       type= anisotropic time= 1 rate= {0.003}
struct tdr= n@node@_PMOS2; # PolyGate

# Poly reoxidation
# ------------------
diffuse temperature= 850<C> time= 2.0<min>  O2
struct tdr= n@node@_PMOS3 ; # Poly Reox

# LDD implantation
```

```
# ------------------
refinebox Silicon min= {0.0 0.05} max= {0.1 0.12} xrefine= {0.01 0.01 0.01} \
                                                  yrefine= {0.01 0.01 0.01} add
grid remesh
implant Boron dose= 1e12<cm-2> energy= 1<keV> tilt= 0 rotation= 0
struct tdr= n@node@_PMOS4 ; # LDD Implant
diffuse temperature= 1050<C> time= 0.1<s> ; # Quick activation
struct tdr= n@node@_PMOS5 ; # LDD Diffuse

# Halo implantation: Quad HALO implants
# ---------------------------------------
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> rotation= 0
struct tdr= n@node@_PMOS6 ; # Halo 1
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> rotation= 90<degree>
struct tdr= n@node@_PMOS7 ; # Halo 1
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> rotation= 180<degree>
struct tdr= n@node@_PMOS8 ; # Halo 1
implant Arsenic dose= 0.25e10<cm-2> energy= 5<keV> tilt= 30<degree> rotation= 270<degree>
struct tdr= n@node@_PMOS9 ; # Halo 1

# RTA of LDD/HALO implants
# ------------------------
diffuse temperature= 1050<C> time= 1<s>
struct tdr= n@node@_PMOS10 ; # Halo RTA

# Nitride spacer
# --------------
deposit material= {Nitride} type= isotropic  time= 1 rate= {0.02}
struct tdr= n@node@_PMOS11 ; # Spacer deposition
etch     material= {Nitride} type= anisotropic time = 1 rate= {0.03} isotropic.overetch= 0.01
struct tdr= n@node@_PMOS12 ; # Spacer etch
etch     material= {Oxide}   type= anisotropic time= 1 rate= {0.005}
struct tdr= n@node@_PMOS13 ; # Spacer oxide removal

# P+ implantation
# ---------------
refinebox Silicon min= {0.04 0.12} max= {0.18 0.4} xrefine= {0.01 0.01 0.01} \
                                                   yrefine= {0.05 0.05 0.05} add
grid remesh
implant Boron dose= 1e13<cm-2> energy= 4<keV> tilt= 7<degree> rotation= -90<degree>
struct tdr= n@node@_PMOS14 ; # P+ implantation

# Final RTA
# ---------
diffuse temperature= 1050<C> time= 1<s>
struct tdr= n@node@_PMOS15 ; # Final RTA

# RMG
# ---
mask name= rmg_mask left= 0.01864<um> right= 0.30<um>
etch material= {PolySilicon} type= isotropic time= 1 rate= {0.07} mask= rmg_mask
struct tdr= n@node@_PMOS15_rmg;

#HK material deposizione anisotropic
deposit material= {HfO2} type= anisotropic time= 1 rate= {0.0025} mask= rmg_mask
struct tdr= n@node@_PMOS15_HFO2 ; # Hafnium Dioxide Dep

deposit material= {Tungsten} type= anisotropic time= 1 rate= {0.054} mask= rmg_mask
mask name= gate_mask_2 left= 0.01889<um> right= 0.055<um> negative
etch material= {Tungsten} type= anisotropic time= 1 rate= {0.15} mask= gate_mask_2
struct tdr= n@node@_PMOS15_T_dep ; # Tungsten deposition and etching


# silicidation
# ------------
mask name= silicide_mask left= 0.00<um> right= 0.04081<um>
deposit material= {Titanium} type= anisotropic time= 1 rate= {0.0015} mask= silicide_mask
struct tdr= n@node@_PMOS16_silicide_dep; # SilicideMask
diffuse temperature= 650<C> time= 1.00<s>
struct tdr= n@node@_PMOS16_silicide_diff;

# Contacts
# --------
deposit material= {Tungsten} type= isotropic time= 1 rate= {0.02} mask= silicide_mask
struct tdr= n@node@_PMOS17 ; # W deposition
mask name= contacts_mask left= 0.0<um> right= 0.25<um>
etch material= {Tungsten} type= anisotropic time= 1 rate= {0.15} mask= contacts_mask
struct tdr= n@node@_PMOS18 ; # W etching 1
etch material= {Tungsten} type= anisotropic time= 1 rate= {0.15} mask= gate_mask_2
```

```
struct tdr= n@node@_PMOS19 ; # W etching 2

# Reflect
# ————————
transform reflect left

# save final structure:
#  - 1D cross sections
struct tdr= n@node@_PMOS20 ; # Final

SetPlxList    {PTotal NetActive}
WritePlx n@node@_PMOS_channel.plx  y=0.0 Silicon

SetPlxList    {BTotal PTotal NetActive}
WritePlx n@node@_PMOS_ldd.plx y=0.028 Silicon

SetPlxList    {BTotal PTotal NetActive}
WritePlx n@node@_PMOS_sd.plx y=0.19 Silicon

# Contacts
# ————————
contact bottom name = substrate Silicon
contact name = gate x = -0.04 y = 0.0 Tungsten
contact name = source x = -0.019 y=-0.2 Tungsten
contact name = drain x = -0.019 y = 0.2 Tungsten
struct tdr= n@node@_presimulation


exit
```

5.2 sdevice simulation commands

```
File
{
*INPUT FILES
Grid ="n1_presimulation_fps.tdr"
* physical parameters
Parameter = "sdevice.par"

*OUTPUT FILES
Plot = "n@node@_des.tdr"
* electrical characteristics at the electrodes
Current= "n@node@_des.plt"
}

Electrode
{
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="substrate" Voltage=0.0}
}

Thermode
{
{ Name = "source" Temperature = 300 }
{ Name = "drain" Temperature = 300 }
{ Name = "gate" Temperature = 300 }
{ Name = "substrate" Temperature = 300 }
}

Physics
{
eQuantumPotential
EffectiveIntrinsicDensity( BandGapNarrowing(oldSlotboom) )
Mobility( DopingDep
  eHighFieldSaturation ( GradQuasiFermi)
  hHighFieldSaturation ( GradQuasiFermi)
  Enormal )
Recombination (
  SRH (DopingDep TempDependence)
  Band2Band(Model = NonLocalPath)
  )
}

Plot
{
eDensity hDensity eCurrent hCurrent
```

```
ElectricField eEnormal hEnormal
eQuasiFermi hQuasiFermi
Potential Doping SpaceCharge
eMobility hMobility eVelocity hVelocity
DonorConcentration AcceptorConcentration
Doping
BandGap BandGapNarrowing ElectronAffinity
ConductionBandEnergy ValenceBandEnergy
eQuantumPotential
Band2BandGeneration
}


Math
{
Extrapolate
* use full derivatives in Newton method
Derivatives
* control on relative and absolute errors
RelErrControl
* relative error= 10^(-Digits)
Digits=5
* absolute error
Error(electron)=1e8
Error(hole)=1e8
* numerical parameter for space-charge regions
eDrForceRefDens=1e10
hDrForceRefDens=1e10
Notdamped=50
* maximum number of iteration at each step
Iterations=100
ExitOnFailure
* solver of the linear system
Method=ParDiSo
Wallclock
NoSRHperPotential
}

Solve
{
coupled {Poisson}
coupled{ Poisson Electron Hole }

quasistationary (InitialStep = 0.01 MaxStep = 0.01 MinStep=1e-2
Goal {name= "drain" voltage = -1}
plot { range=(-1, 1) intervals=1 }
){coupled { Poisson  Electron Hole }}

quasistationary (InitialStep = 1e-2 MaxStep = 0.001 MinStep=1e-3
Goal {name= "gate" voltage = -2}
plot { range=(-1, 1) intervals=3 }
){coupled { Poisson Electron Hole } }
}
```