ELECTRICALENGINEERING

Why MOSFET Pinchoff occurs

Ask Question

This question is regard to enhanced n-type MOSFETs. From what I

understand, an *inversion layer* is formed underneath the insulating layer below the gate of the MOSFET when a voltage is applied to the gate. When this voltage exceeds V_{T}, the *threshold voltage*; this inversion layer allows electrons to flow from the source to the drain. If a voltage $V_{\cdots}$ is now applied, the inversion region will begin to

to shrink in length (width) becoming closer and closer to the source.

My questions are:

- Is what I've said so far correct?
- Why does this pinch-off occur? I don't understand what my book says. It says something about the electric field at the drain being also proportional to the gate.
- It is my understanding that when the MOSFET is saturated, a depletion layer forms between the pinched-off bit and the drain. How does current flow through this depleted portion to the drain? I thought the depletion layer does not conduct... Like in a diode...

transistors mosfet pn-junction

edited Jul 28 '13 at 7:55

Anindo Ghosh

45.9k 7 84 166

asked Jul 28 '13 at 6:56

user968243

618 5 14 27

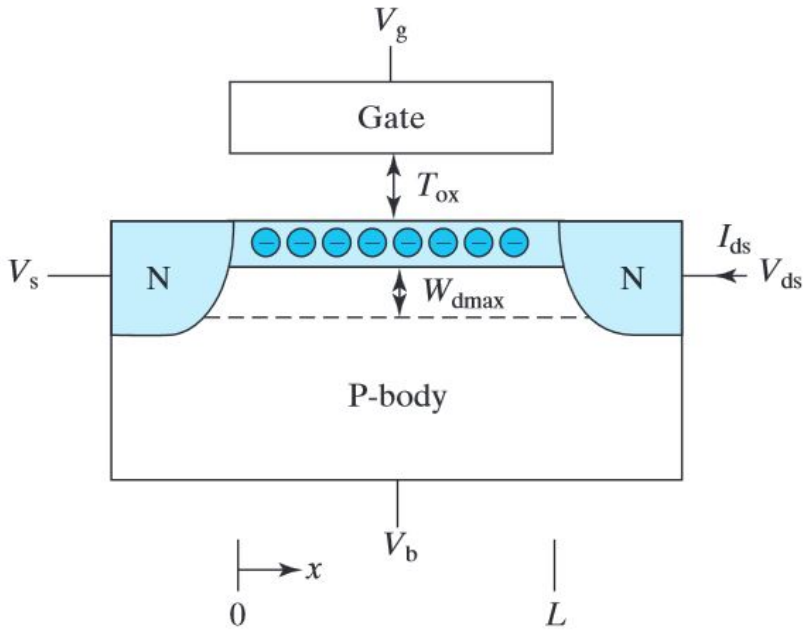
1 Answer

Your description is correct: given that $V_{GS} > V_T$, if we apply a Drain-to-Source voltage of magnitude $V_{SAT} = V_{GS} - V_T$ or higher, the channel will pinch-off.

I'll try to explain what happens there. I'm assuming n-type MOSFET in the examples, but the explanations also hold for p-type MOSFET (with some adjustments, of course).

The reason for pinch-off:

Think about the electric potential along the channel: it equals V_S near the Source; it equals V_D near the Drain. Recall also that potential function is continuous. The immediate conclusion from the above two statements is that potential changes continuously form V_S to V_D along the channel (let me be non-formal and use terms "potential" and "voltage" interchangeably).

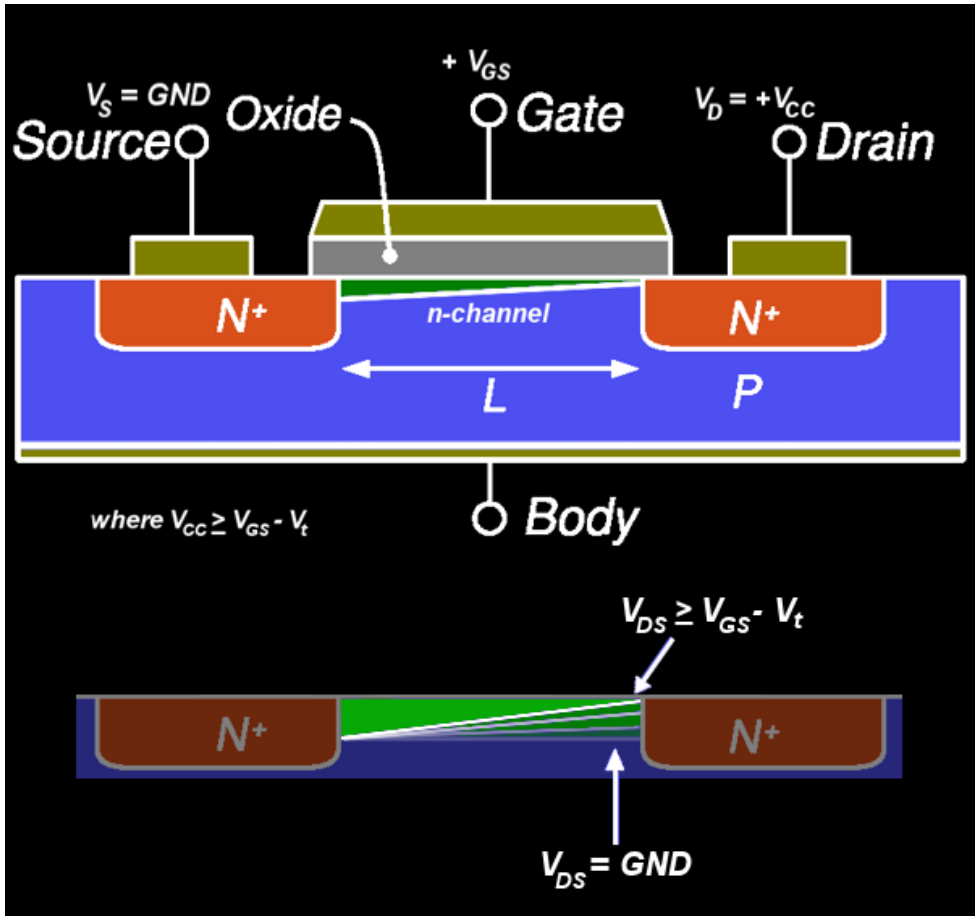


When $V_{ds} \neq 0$, the channel voltage V_c is a function of x.

Now, let's see how the above conclusion affects the charge in the inversion layer. Recall that this charge is accumulated under the Gate due to Gate-to-Substrate voltage (yes, Substrate, not Source. The reason we usually use V_{GS} in our calculations is because we assume that the Substrate and the Source are connected to the same potential). Now, if the potential change along the channel when we apply V_{DS}, the Gate-to-Substrate voltage also change along the channel, which means that the induced charge density will vary along the channel.

When we apply $V_{SAT} = V_{GS} - V_T$ to the Drain, the effective Gate-to-Substrate voltage near the Drain will become:
$V_{eff} = V_{GS} - V_{SAT} = V_T$. It means that near the Drain the Gate-to-Substrate voltage is just enough to form the inversion layer. Any higher potential applied to Darin will cause this voltage to reduce below the Threshold voltage and the channel will not be formed -

pinch-off occurs.



What happens between the pinch-off point and the Drain:

The Gate-to-Substrate voltage in this region is not enough for a formation of the inversion layer, therefore this region is only depleted (as opposed to inverted). While depletion region lacks mobile carriers, there is no restriction on current flow through it: if a carrier enters the depletion region from one side, and there is an electric field across the region - this carrier will be dragged by the

field. In addition, carriers which enter this depletion region have initial speed.

All the above is true as long as the carriers in question will not recombine in the depletion region. In n-type MOSFET the depletion region lacks p-type carriers, but the current consist of n-type carriers - this means that the probability for recombination of these carriers is very low (and may be neglected for any practical purpose).

Conclusion: charge carriers which enter this depletion region will be accelerated by the field across this region and will eventually reach the drain. It is usually the case that the resistivity of this region may be completely neglected (the physical reason for this is quite complex - this discussion is more appropriate for physics forum).

Hope this helps

edited Oct 1 '13 at 21:43

answered Jul 28 '13 at 9:06

Vasiliy

6,312 2 14 30

It certainly does help! Thank you, I understand most of it except for this "Now, if the potential change along the channel when we apply V_{DS}, the Gate-to-Substrate voltage also change along the channel, which means that the induced charge density will vary along the channel.". Is it like this: at the source, the electrons have a high potential, and therefore somehow the inversion layer is large towards the source, and towards the drain the electrons have lost most of their potential and somehow the inversion layer is thinner? – user968243 Jul 28 '13 at 14:52

4 No, this time your description is wrong. Go back to definition of MOS capacitor: the more the potential difference is between the Gate and the Substrate, the more charge will be accumulated under the gate (inversion charge). When there is no Drain-to-Source voltage, this potential difference is constant. However, when you apply higher potential to Drain, the potential of the Substrate near the Drain raises too. This local raise in Substrate's potential leads to a local reduction of Gate-to-Substrate voltage, which leads to less inversion charge (and, eventually, to pinch-off). – Vasiliy Jul 28 '13 at 15:10

Ah yes, so the Drain to Source voltage opposes the Gate to Substrate voltage and this opposition is very pronounced near the Drain and barely pronounced near the source. I guess, then that it is for this reason that when the Drain to Source voltage is equal to the Gate to Substrate voltage, the voltage at the Drain basically fully opposes that Gate to Substrate voltage, thus causing the inversion layer to be tiny (pinch off) near the drain. Thanks so much for this, you've certainly made it far more clear than any of my books! – user968243 Jul 29 '13 at 3:08

1 You welcome. One small note: pinch-off occurs when

$$V_{SAT} = V_{GS} - V_T$$

. It means that Gate-to-Substrate voltage is not necessarily zero in pinch-off region, but less than Threshold voltage – Vasiliy Jul 29 '13 at 6:40

Thanks Vasiliy for your answer. What I would like to ask you is whether the same applies for depletion mode nMOS or it holds only for enhancement mode transistors? I hope you understand. – user72546 Apr 17 '15 at 16:45

protected by Dave Tweed ♦ Feb 3 '17 at 23:50

Thank you for your interest in this question. Because it has attracted low-quality or spam answers that had to be removed, posting an answer now requires 10 reputation on this site (the association bonus does not count).

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