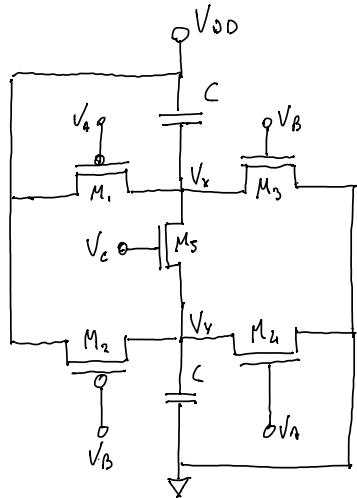


ES. 1

17/02/2011

#2



$$V_{DD} = 3.3 \text{ V} \quad \beta_n = 1.2 \frac{\mu\text{A}}{\text{V}^2}$$

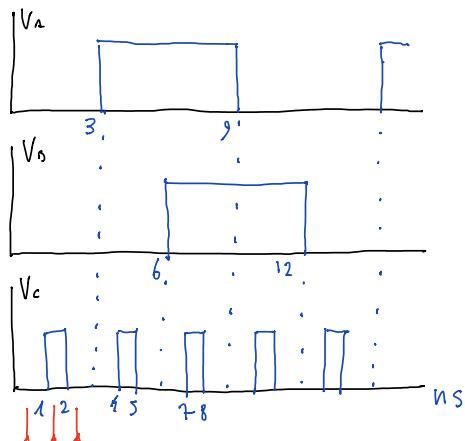
$$V_T = 0.35 \text{ V} \quad \beta_p = 0.9$$

soglia

V_x, V_y, V_c periodico 12 ns

→ ondeggia V_x, V_y

→ consumo radio polvera statica



→ ANDAMENTO: transistor concluso
i condensatori non carica

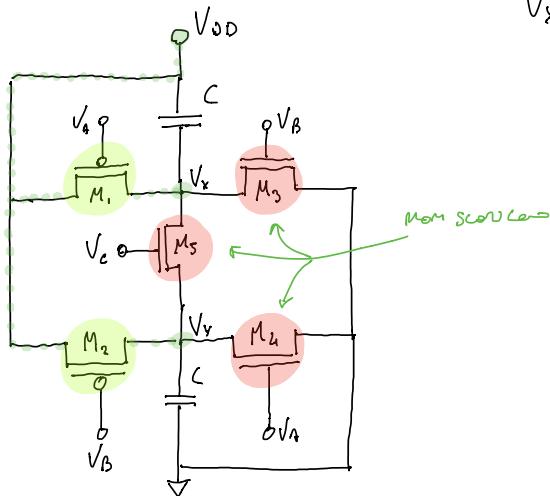
→ ogni transistore si esaurisce prima
del prossimo ingresso

Octans

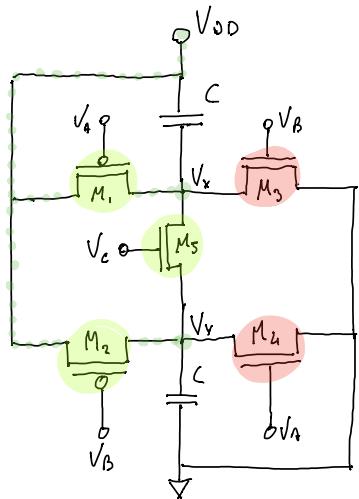
- NMOS spenti, PMOS accesi

$$V_x, V_y = V_{DD}$$

$\equiv 2 \text{ ns} < t < 3 \text{ ns}$



$1 \text{ ns} < t < 2 \text{ ns}$

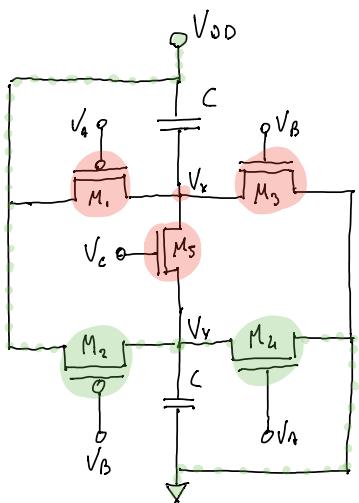


→ upgrade

$$V_x = V_y = V_{DD}$$

→ M_3 in realtà non è acceso, fissa
uguale ai capi, quindi da considerare
per potenza statica

$3 \text{ ns} < t < 4 \text{ ns}$



→ pull-up e pull-down
→ calcola corrente di uscita

$$\text{IPOTESI: } I_{out} = I_{in} \text{ LIN}$$

$$\beta_2 \left\{ (V_{S2} - V_T) V_{D2} - \frac{V_{D2}^2}{2} \right\} = \beta_4 \left\{ (V_{S4} - V_T) V_{D4} - \frac{V_{D4}^2}{2} \right\}$$

$$\beta_2 \left\{ (V_{D0} - V_T) (V_{D0} - V_y) - \frac{(V_{D0} - V_y)^2}{2} \right\} = \beta_4 \left\{ (V_{D0} - V_T) V_y - \frac{V_y^2}{2} \right\}$$

$$V_y = \begin{cases} 2.0, 1.27 \\ \text{non valido} \end{cases}$$

$> V_{DD}$

→ VERIFICA

$$V_{S4} > V_{SD2} + V_T$$

$$V_{DD} > V_{D0} - V_y + V_T$$

$$V_y > V_T \quad \underline{\text{OK}}$$

$$V_{L2} > V_{D2} + V_T$$

$$V_{DD} > V_y + V_T$$

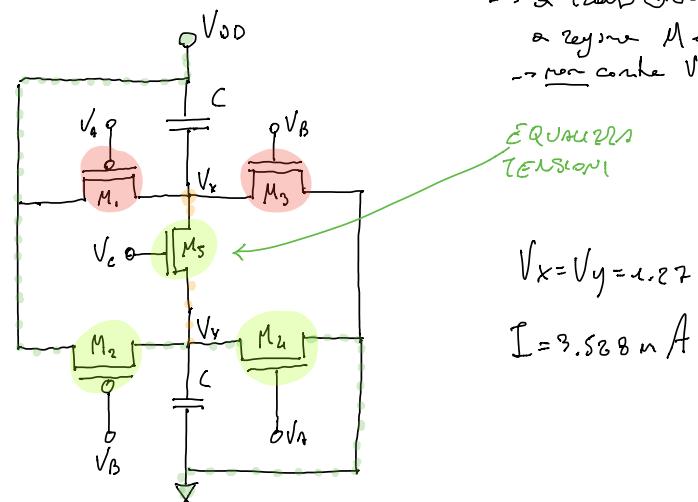
$$3.5 > 1.27 + 0.76 \quad \underline{\text{OK}}$$

→ POTESI STATICA

$$I = \beta_4 \left\{ (V_{DD} - V_T) V_y - \frac{V_y^2}{2} \right\} = 3.528 \text{ mA}$$

$$V_x = U.I.$$

$4 \text{ ns} < t < 5 \text{ ns}$



→ a transistors $V_x = V_y$ si equivalent
a reistor M_5 si spagnu
→ non corrisponde V_T

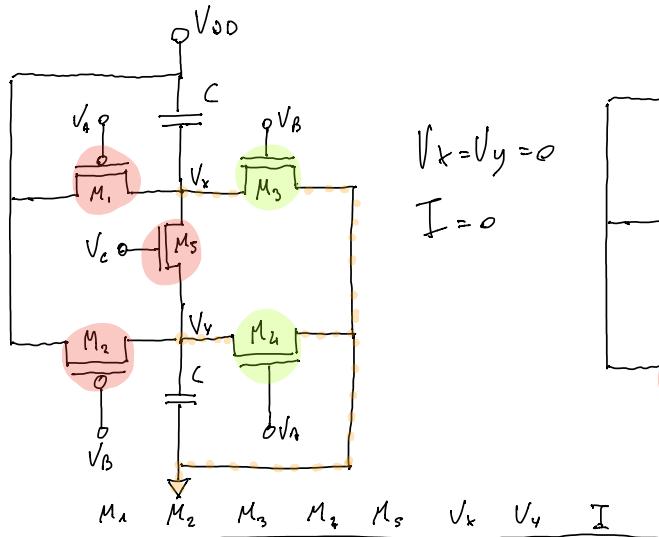
EQUALIS TENSIONI

$$V_x = V_y = 1.27$$

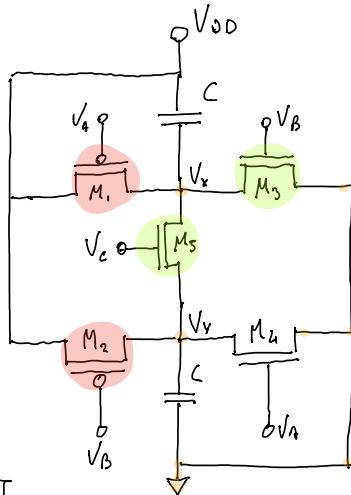
$$I = 3.528 \text{ mA}$$

$5 \text{ ns} < t < 6 \text{ ns}$ → static condizioni

$6 \text{ ns} < t < 7 \text{ ns}$



$7 \text{ ns} < t < 8 \text{ ns}$



	M_1	M_2	M_3	M_4	M_5	V_x	V_y	I
0	●	●						
1	●	●						
2	●	●				●		
3		●						
4		●						
5	●	●	●	●	●	1.27	1.27	3.52
6	●	●	●	●	●			
7	●	●	●	●	●			
8	●	●	●	●	●			
9	●	●	●	●	●			
10	●	●	●	●	●			

$$\begin{aligned} V_{DD} &= U_{DD} = 0 \\ V_{DD} &= U_{DD} = 0 \\ &= 1.27 \\ &= 1.27 \\ &= 3.52 \\ &= 3.52 \\ &= 3.52 \\ &= 3.52 \\ &\rightarrow \dots \\ &= 3.52 \end{aligned}$$

$$\begin{aligned} P &= \frac{1}{T} \int V_{DD} I_{DD} dt = \\ &= \frac{V_{DD}}{T} \int I_{DD} dt = \\ &= \frac{V_{DD}}{T} \int_{t=0}^{t=8} 3.528 \text{ mA} dt + \\ &= \frac{V_{DD}}{T} \int_{t=8}^{t=10} 3.52 \text{ mA} dt \end{aligned}$$

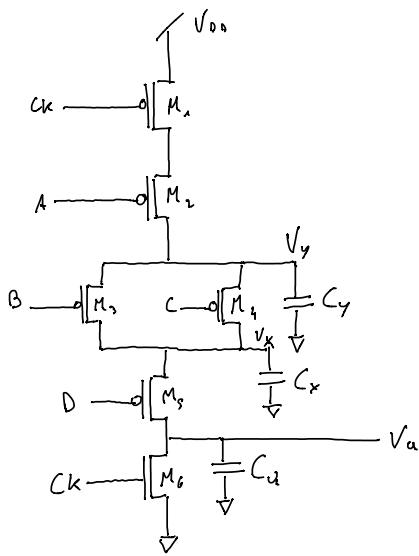
$$+ \int_{9 \text{ m}}^{3.378 \text{ m} A} \{ t = 5.83 \text{ m W}$$



ES. 2

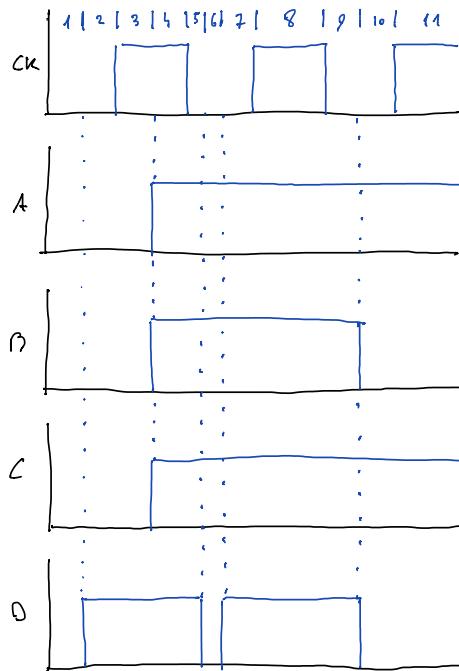
31/01/2008

$$V_{DD} = 3.3V \quad C_x = 20 \text{ pF} \quad C_y = 40 \text{ pF} \quad C_u = 60 \text{ pF}$$



→ funzione logica \Rightarrow funzione

→ V_u al tempo funzione



→ perche' V_u si sia = 1 b: segnale di ci sia uno contatto fra V_u e V_{DD} , tutti transistori in serie accesi, paralleli presenti.

→ s: quando sono orzelle concrete e se ottenere funzione booleana

$$V_u = \bar{A} \cdot \bar{D} \cdot (\bar{B} + \bar{C}) \quad \begin{matrix} \uparrow \\ \text{AND} \end{matrix} \quad \rightarrow \text{se possibile scrivere con my own possibili}$$

$$\overline{V_u} = \overline{\bar{A} \cdot \bar{D} \cdot (\bar{B} + \bar{C})} \quad \longrightarrow \quad \overline{V_u} = A + D + B C$$

→ determine transistors

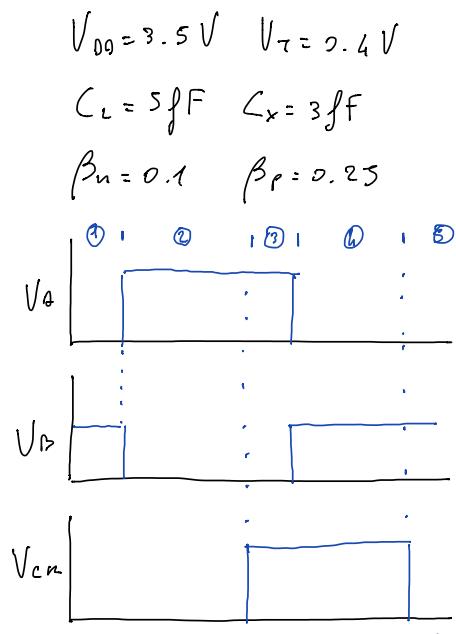
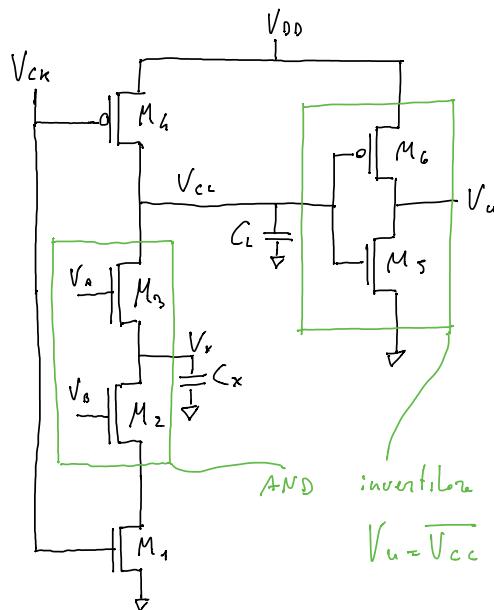
$$\begin{array}{ll}
 \textcircled{1} & V_u = V_{DD}, \quad V_x = V_y = V_{DD} \\
 \textcircled{2} & V_u = H1 = V_{DD}, \quad V_x = J_y = V_{DD} \\
 \textcircled{3} & V_u = 0, \quad V_x = V_y = H1 \leftarrow \begin{array}{l} \text{clock is low} \\ \text{da querden} \end{array} \\
 \textcircled{4} & " " \\
 \textcircled{5} & V_u = H1 \quad " " \\
 \textcircled{6} & V_u = V_x = 0.825 \quad V_y = H1 = V_{DD} \leftarrow \begin{array}{l} V_x, V_y \text{ is high} \\ \text{da untersetzen } V_{DD} \end{array} \\
 \textcircled{7} & \text{TUTTI } H1 \\
 \textcircled{8} & V_u = 0 \quad V_x = H1 = 0.825 \quad V_y = H1 = V_{DD} \\
 \textcircled{9} & \text{TUTTI } H1 \\
 \textcircled{10} & V_u = V_x = V_y = 1.25 \\
 \textcircled{11} & V_u = V_x = V_y = 0
 \end{array}$$

H1 = HIGH IMPEDANCE
 clock is low
 da querden
 Vx, Vy is high
 da untersetzen VDD
 TUTTI H1
 TUTTI H1
 Qf = Qf
 Q = CV
 Cx Vu + Cy Vy = Ca Vu + Cx Vy
 Vu_f = \frac{C_a Vu_i + C_x Vx_i}{C_a + C_x} = 0.825 V

Cx Vu + Cy Vy = Cx Vu_f + Cy Vy_f
 Vu_f = \frac{C_a Vu_i + C_x Vx_i + Cy Vy_i}{C_a + C_x + Cy} = 1.25 V

ES.3

16/06/2005



→ hysteresis loop

$$\overline{V_u} = \overline{V_{CC}}$$

→ si valenze solo per
clock attivo

$$\overline{V_{CC}} = V_A V_B$$

→ non si inserisce in espressione

$$\overline{V_u} = V_A V_B$$

↑
calcolo
fino a qui

→ intervalli:

$$\textcircled{1} \quad V_{CC} = V_{DD} \quad V_u = 0 \quad V_T = V_{DD}$$

$$\textcircled{2} \quad " \quad " \quad V_T = V_1$$

$$\textcircled{3} \quad V_{CC} = V_1 \quad V_u = 0 \quad V_T = 0$$

$$\textcircled{4} \quad V_{CC} = V_T \quad V_u = 0.7313$$

$\leftarrow V_{CC} \in V_T$ si equivalgono
→ distribuzione coniche

$$C_x V_T + C_L V_{CC} = C_x V_T + C_L V_{CC}$$

$$V_f = 2.1875V$$

→ per V_u si ipologgiato entrambi i
SAT e po' si aggiungono le corrette

HP = HYPOOTESIS

HP: $N_S M_G$ SAT

$$\cancel{\beta_G (V_{DD} - V_{CC} - V_T)^2 / 2} = \cancel{\beta_S (V_{CC} - V_T)^2 / 2} \leftarrow \text{non c'è } V_u \text{ nelle condizioni complete di saturazione}$$

HP: $M_S M_G$ LIN

$$\cancel{\beta_G \left\{ (V_{GS} - V_T) V_{SD} - V_{SD}^2 / 2 \right\}} = \beta_S \left\{ (V_{GS} - V_T) V_{DS} - V_{DS}^2 / 2 \right\}$$

$$\cancel{\beta_G \left\{ (V_{DD} - V_{DS} - V_T) (V_{DD} - V_u) - (V_{DD} - V_u)^2 / 2 \right\}} = \beta_S \left\{ (V_{CC} - V_T) V_L - V_L^2 / 2 \right\}$$

$$V_u = \begin{cases} 2.84 \\ 3.42 \end{cases} \rightarrow \text{entrambi accettabili} \rightarrow \text{corretto}$$

$$\cancel{V_{GS} \geq V_{DS} + V_T} \\ \cancel{2.1875 \geq 3.42 + V_T}$$

→ inoltre per CMOS non accettabile che entrambi lineari

HP: M5 Lin M6 Sat

$$\beta_s \left\{ \frac{(V_{DD} - V_{CC} - V_T)^2}{2} \right\} = \beta_s \left\{ (V_{CC} - V_T) V_u - \frac{V_u^2}{2} \right\}$$

2.84

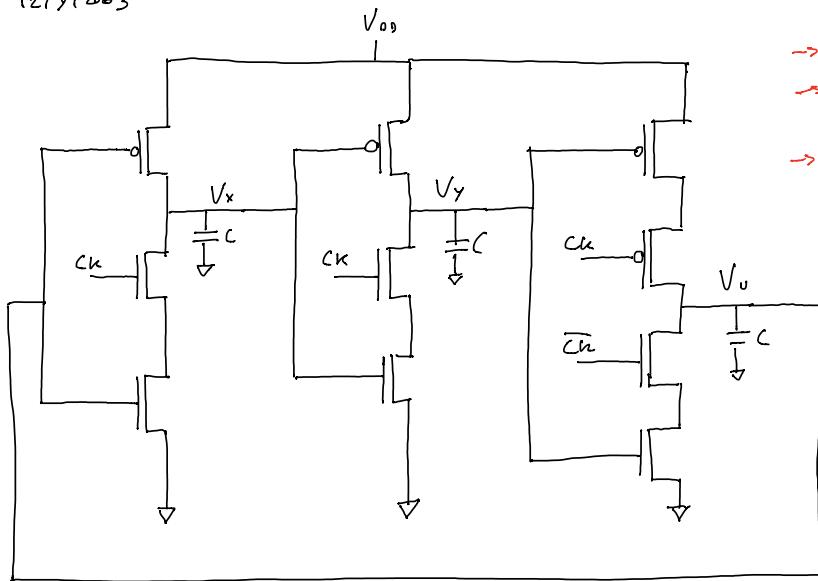
~~0.7313~~ $0.18 > 0.73 + \sqrt{\tau}$ ~~use~~

$$V_{DD} - V_{CC} < V_{DD} - 0.73 \sqrt{\tau}$$

OK

ES. 4

12/12/2003



→ ondulate temporali parallele
→ periodo n. 1 ms = 250 ns
→ altezza

→ potenze minime dissipate

$$\begin{aligned} V_T &= 0.33 V \\ V_{DD} &= 3.3 V \\ f_{CK} &= 100 \mu Hz \\ C &= 25 \text{ fF} \\ \beta_m &= 100 \\ R_P &= 8 \Omega \end{aligned}$$

→ condensato segnali

SONO LE 13:25, HO FAMIGLIA
SONO STANCO E STUFO DI
VEDERE rappresentazioni di

SEMICONDUTTORI
INUTILI

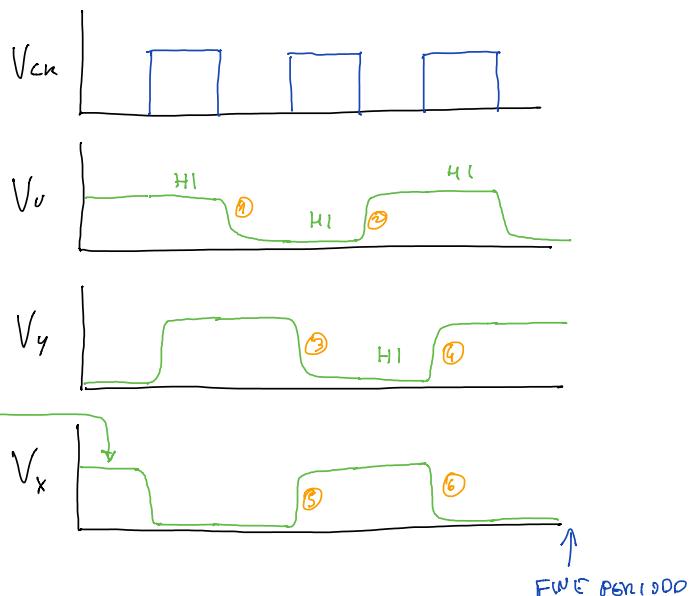
seguente

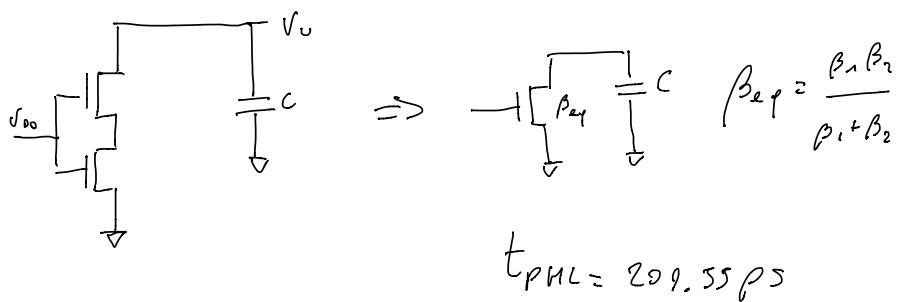
del tipo

"IDEAL NOT IN CENTER"

altrimenti: Vy alto

transistor da
controllare





→ feste am gleichen alle steilen u. s.

$$\textcircled{1} = 209.5 \text{ ps}$$

→ verhindern ein rein/sauber nmos/pmos ideale

$$\textcircled{2} = 261.9$$

$$\textcircled{3} = 209.9$$

$$\textcircled{4} = 139.4$$

S, t, u feste

$$P = 45.94 \text{ mW}$$