

# Advanced planar FDSOI devices

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# Acknowledgement

*-French National funding/projects :*  
**Nano2012, Nano 2017, ...**



*-European funding/projects :*  
**Reaching 22, Dynamic ULP, Places2Be, ...**



*-Industrial collaboration:*  
**STMicroelectronics, IBM, SOITEC**



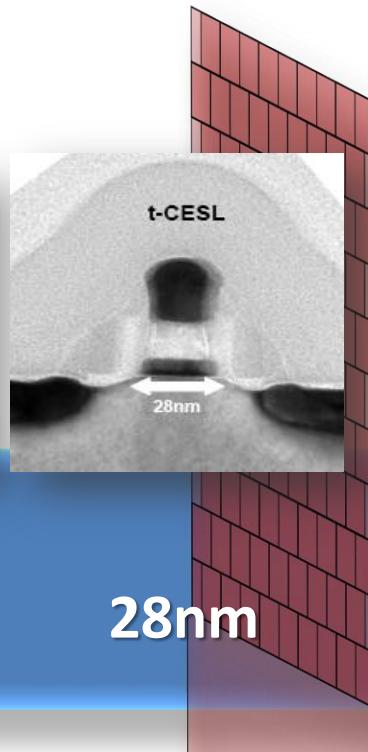
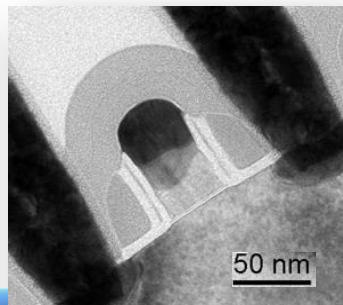
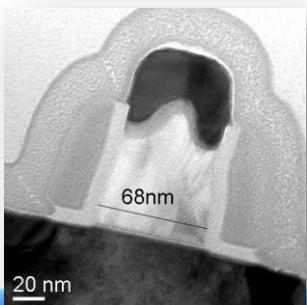
# Outline

- Introduction to planar FDSOI
- 28nm FDSOI [platform]
  - Process integration, results reminder, devices partitioning
  - Multi Vt, back bias effect, variability
- 14nm FDSOI [development]
  - Boosters, process integration
  - Scalability
- 10nm FDSOI [R&D]
  - Geometrical scaling, new modules, strain for  $\mu$  boost
- Conclusion

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# ITRS roadmap beyond 28nm



65nm

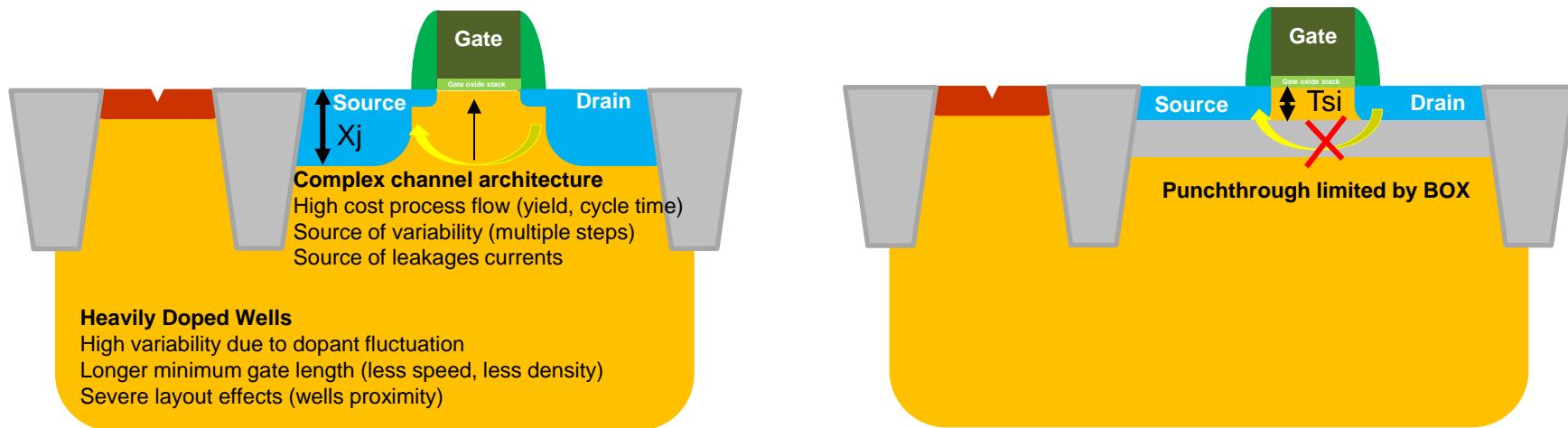
45nm

28nm

**Introduction of technological  
« boosters » for bulk**

**Limited control of the  
gate through the  
channel**

# Bulk transistor limitation beyond 20nm



- Short channel effects improvement ( $X_j$ ,  $T_{dep}$ )
- Low subthreshold slope
- Reduced junction capacitances
- Isolation between devices
- Better variability no channel doping

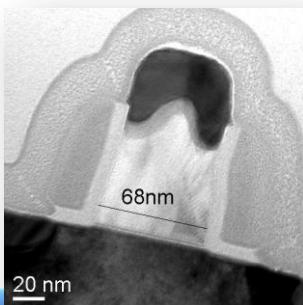
Depleted devices deliver improved electrostatic control and device scalability

$$SCE = 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} \times \left( 1 + \frac{T_{Si}}{L_{eff}^2} \right) \left( \frac{T_{ox}}{L_{eff}} \frac{T_{Si}}{L_{eff}} \right) \times \Phi_d$$

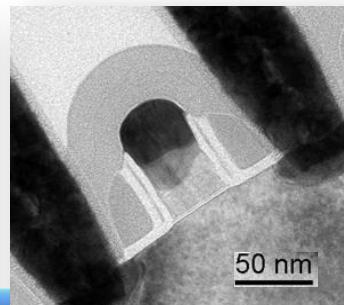
Ref: [Skotnicki – ESSDERC 00]

**FD-SOI technology very suitable for low power from 28nm nodes and beyond**

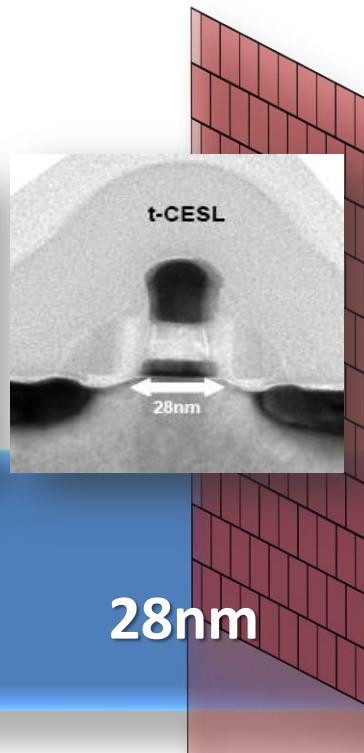
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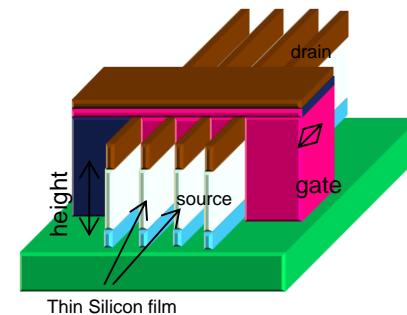


28nm

**Introduction of technological « boosters » for bulk**

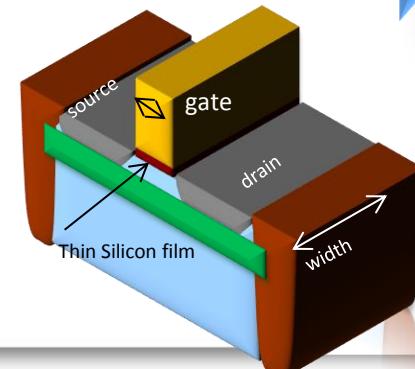
**Limited control of the gate through the channel**

**Transistor FinFET : 3D**



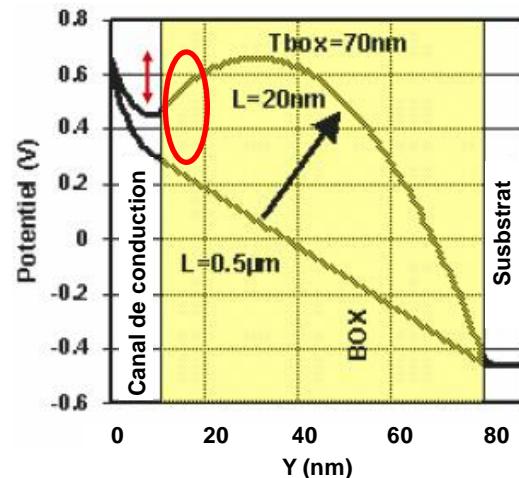
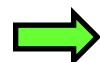
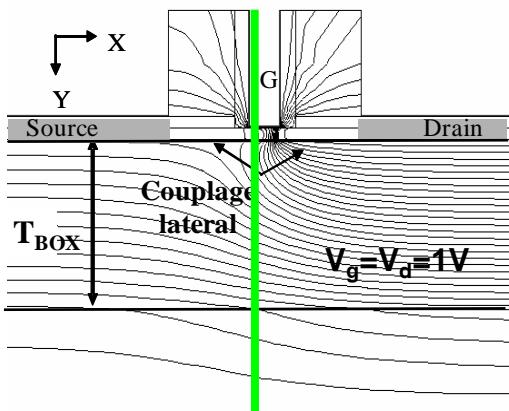
**Innovative structures**

**Planar FDSOI transistor**



# Why thin BOX?

## Thick BOX

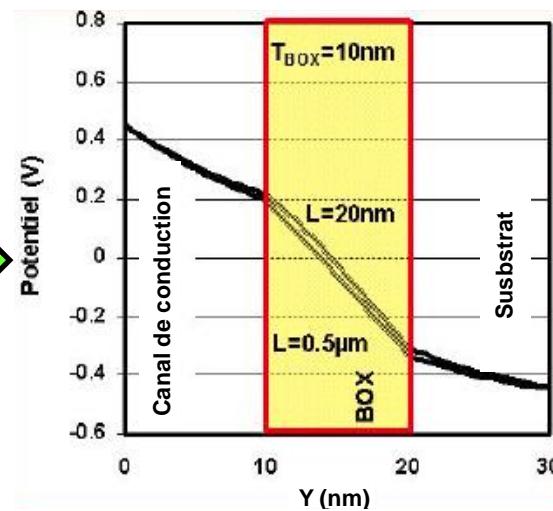
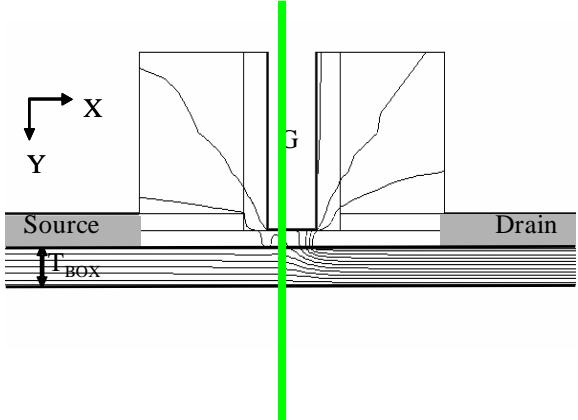


- Potential increases in BOX

- Strong lateral coupling, through the BOX, between the source and drain

- DIBL degradation

## Thin BOX



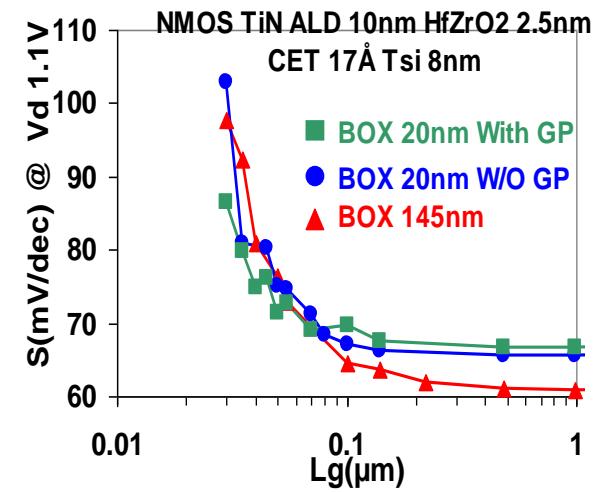
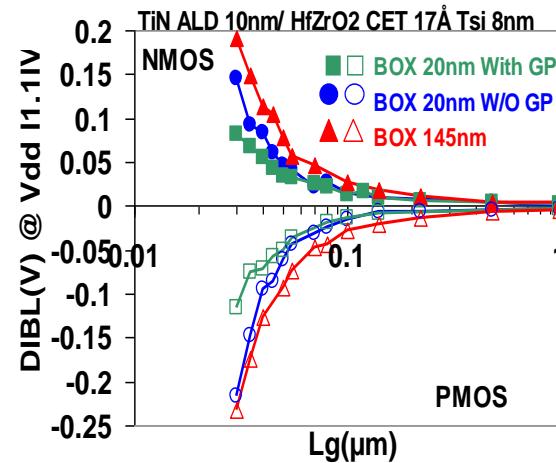
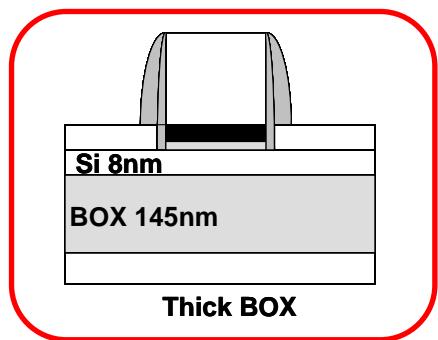
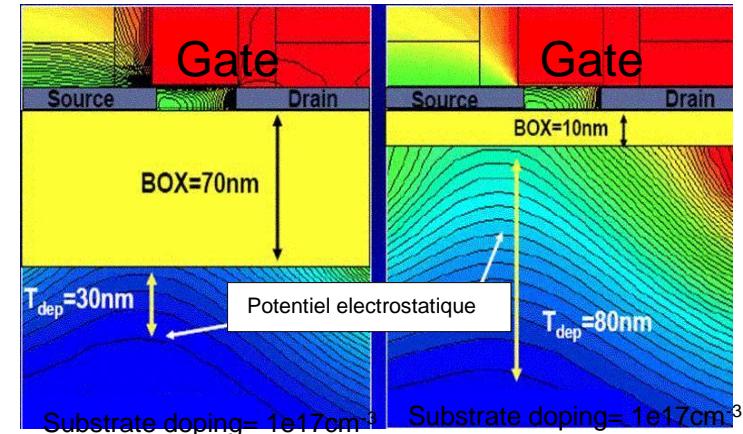
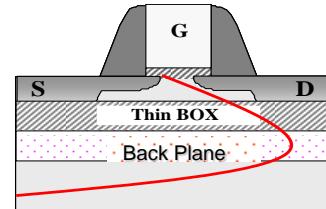
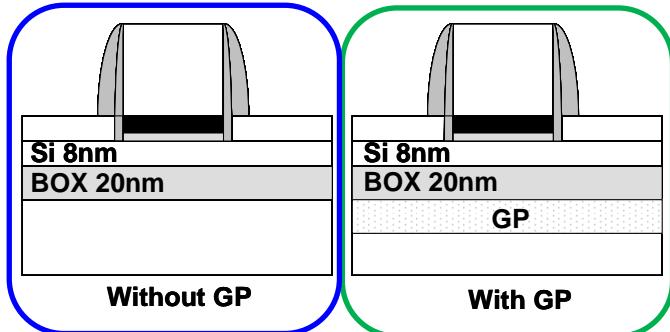
- Low potential modification in the BOX

- Low lateral coupling between source and drain

- DIBL improvement

# Thin BOX and Ground Plane (GP)

- Thin BOX improves the short channel effects
- Depletion area extended under the BOX
- Ground Plane introduction (GP or BP)



- $V_T$  modulation

- DIBL and subthreshold slope improvement

C. Fenouillet-Beranger et al,  
ESSDERC 2008

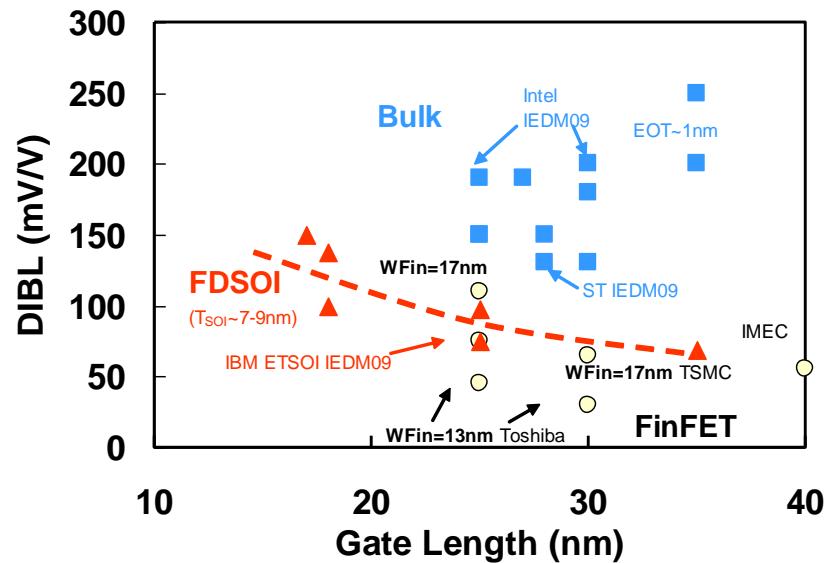
# FDSOI: Introduction

- Fully Depleted Silicon-On-Insulator (FDSOI)
  - Improves the device **scalability** (vs. bulk): enhanced electrostatics

$$\begin{array}{l} \text{bulk} \rightarrow DIBL = 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{ds} \\ \\ \text{FDSOI} \rightarrow DIBL = 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left( 1 + \frac{T_{Si}^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{Si}}{L_{el}} V_{ds} \end{array}$$

T. Skotnicki et al. IEEE EDL, March'88 & IEDM'1994

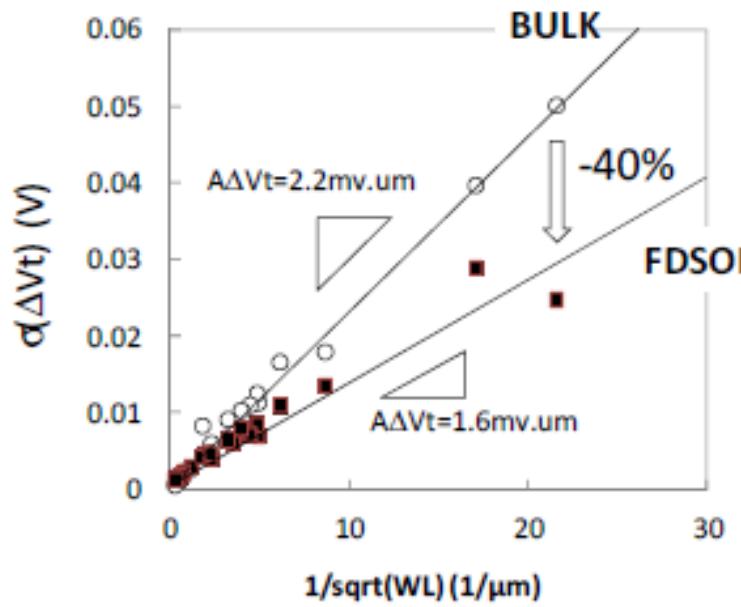
O. Faynot, SOI conf. 2011 short course



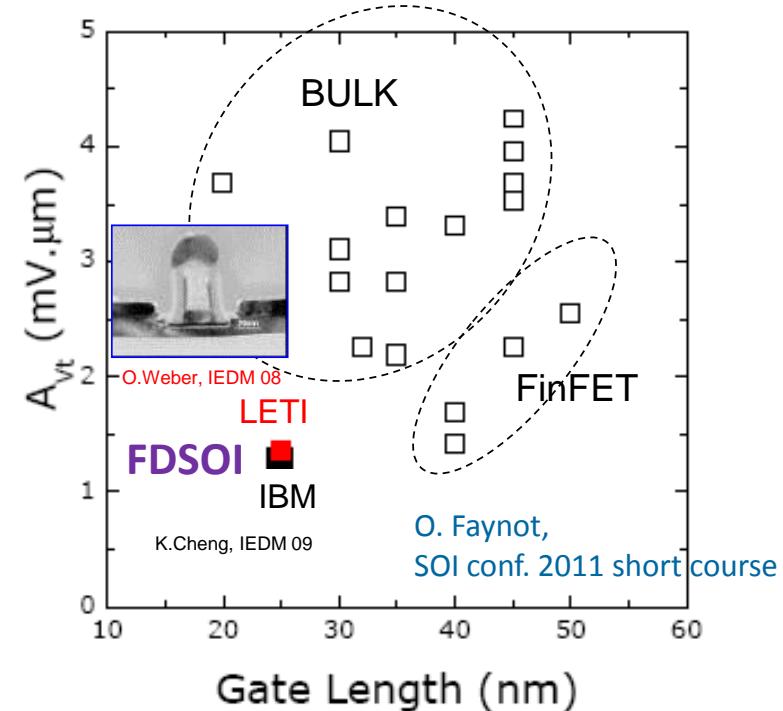
# FDSOI: Introduction

- Fully Depleted Silicon-On-Insulator (FDSOI)
  - Improves the device **scalability** (vs. bulk): enhanced electrostatics
  - Reduce the **variability** thanks to undoped channel: record variability  
 $1.4\text{mV}.\mu\text{m}$  in C28nm technology =  $150\text{mV SRAM } V_{\text{MIN}}$  reduction

Figure of merit: Pelgrom plot => slope  $A_{\Delta Vt}$



ST: N. Planes *et al.*, VLSI tech symp 2012



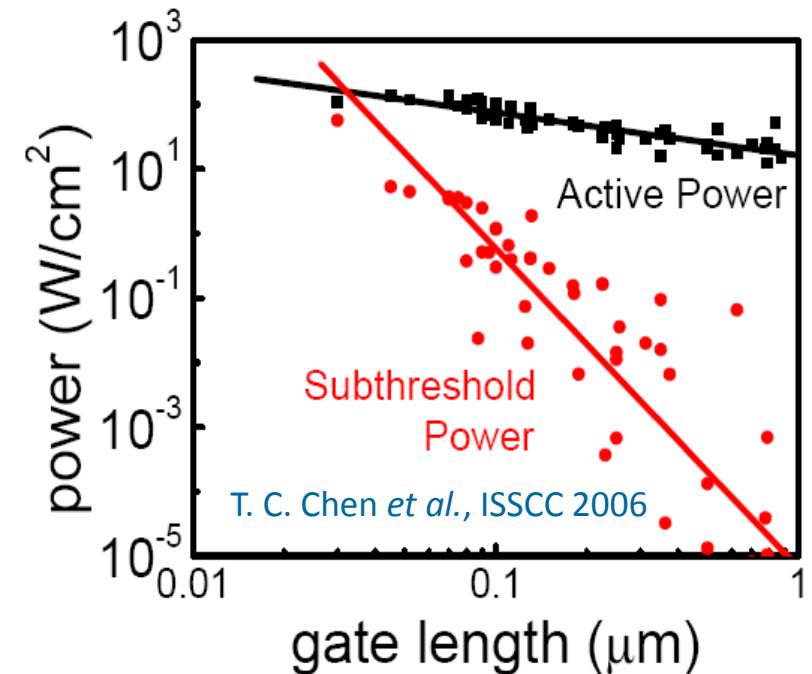
# FDSOI: Introduction

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  - Improves the device **scalability** (vs. bulk): enhanced electrostatics
  - Reduce the **variability** thanks to undoped channel
  - Limits the **static power** and **dynamic power consumptions**  
(low Vdd operation, lowest junction capa, improved subthreshold slope)
  - ...

$$P = f C V_{dd}^2 + I_{OFF} V_{dd}$$

Dynamic or active  
Power

Static or subthreshold  
Power





**Faster.**

- Transistors run at max frequencies up to 30% faster than bulk CMOS, enabling faster processors
- This puts devices more powerful in the hands of the end user



**Cooler.**

- Transistors are significantly more power efficient than bulk CMOS devices with lower leakage and much wider range of operation points down to lower voltages
- End user devices run cooler and last longer



**Simpler.**

- The manufacturing process for FD-SOI is much simpler than alternatives and makes extensive use of existing fab infrastructure
- Design porting from bulk is simple and fast

Adapted from ST (J. Hartmann 2012)

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# 28nm FDSOI platform: process integration

- Gate-first type FEOL

*same as ST/ISDA 28LP*

- No complex stressors

- FE process:

*80% common with ST/ISDA 28LP*

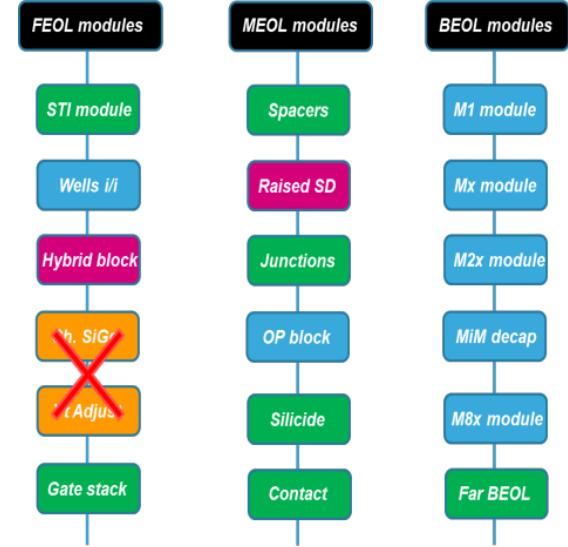
*20% specific*

- 15% less steps in UTBB vs. 28LP
- Same LDD implants for all GO1 devices, incl. SRAM
- No pocket implants

- BE process:

*identical to ST/ISDA 28LP*

Adapted from ST (J. Hartmann 2012)



**Caption:**

- Same as bulk
- New module
- Adjustment vs bulk
- Not use in FD-SOI

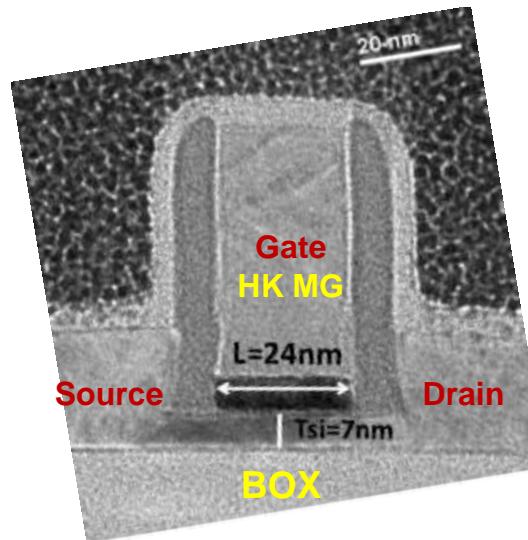
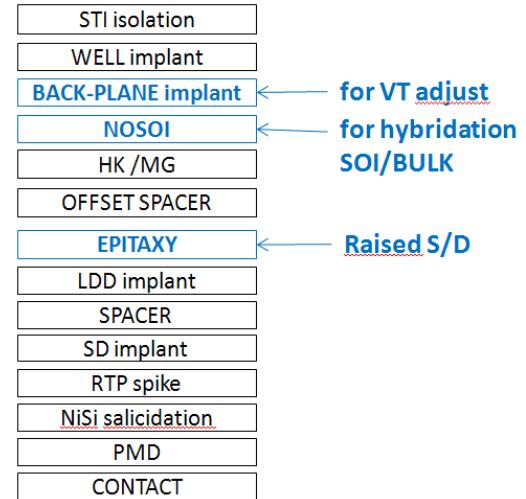
**36 masks for**

- Dual Vt core oxide
- 1.8V I/O oxide
- Full active/passives offer
- Deep Nwell
- 7 metal levels BEOL stack
- ...

# 28nm FDSOI platform: process integration

## Front End Process

- Starting wafers: SOI (Si 12nm/**BOX 25nm**)
- After process: **7nm** final Si body (undoped channel)
- Hybrid bulk-SOI co-integration
- Ground-Plane for  $V_{th}$  adjust
- Two  $V_{th}$  flavors: RVT, LVT
- Contact Poly Pitch (CPP): **114nm**
- Min. gate length: **24nm**
- High-K/Metal Gate, **Gate First**
- Si Raised Source & Drain
- Ion implantation for SD doping

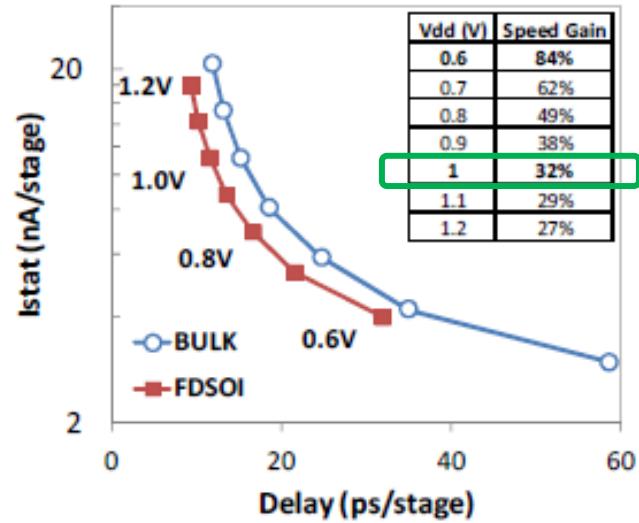
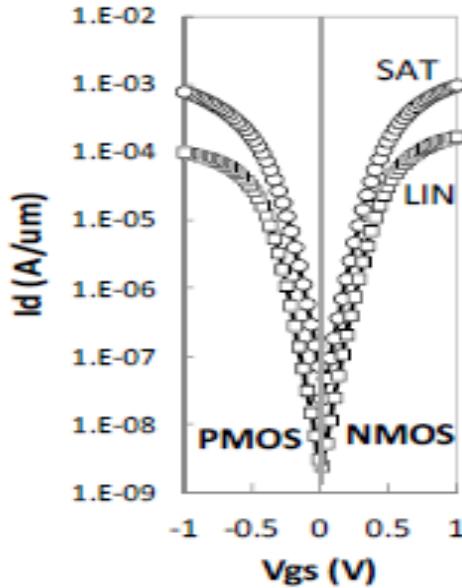
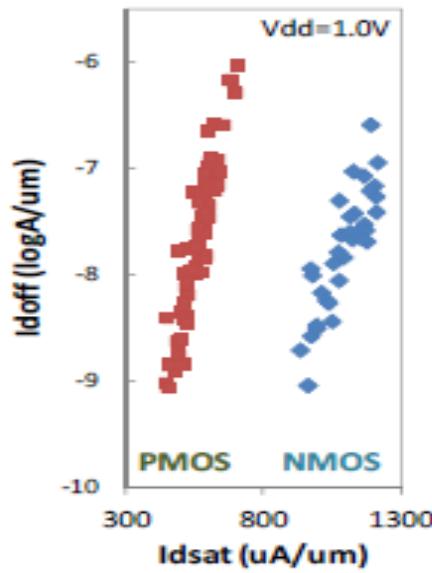


Key features	28FDSOI
Min Contact gate pitch CPP	114nm
M1 pitch	90nm
Std cell area	1X
VT flavours	RVT / LVT
Lgate in min CPP	24nm → 30nm
Channel	SOI 7nm
Buried oxide	BOX 25nm
Gate	HKMG single metal
Source-Drain	Single Si epi + I/I

ST: N. Planes *et al.*, VLSI tech symp 2012

# 28nm FDSOI platform

## Performance



- NMOS:  $I_{\text{ON}}=1070\mu\text{A}/\mu\text{m}$  @  $I_{\text{OFF}}=16\text{nA}/\mu\text{m}$
- PMOS:  $I_{\text{ON}}=610\mu\text{A}/\mu\text{m}$  @  $I_{\text{OFF}}=30\text{nA}/\mu\text{m}$   
@  $V_{DD}=1\text{V}$
- DIBL<100mV/V
- SS<85mV/dec
- FDSOI is 32% faster than bulk at same leakage @  $V_{DD}=1\text{V}$  (84% @  $V_{DD}=0.6\text{V}$ ) thanks to its superior electrostatics (DIBL)

ST: N. Planes *et al.*, VLSI tech symp 2012

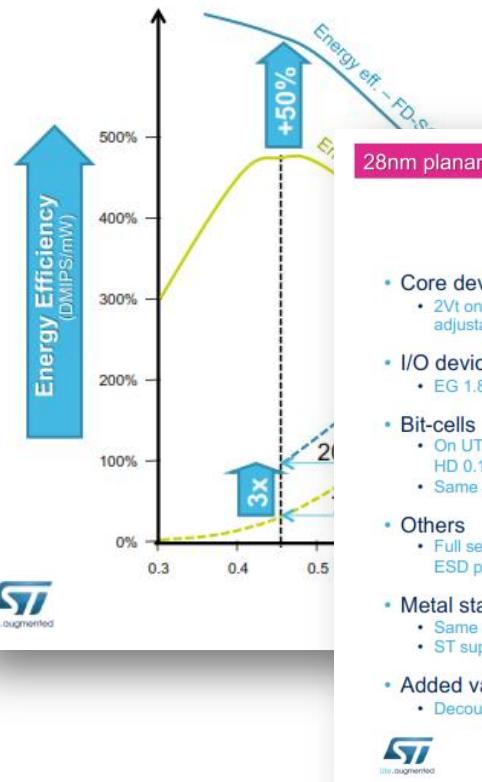
# 28nm FDSOI: ST results reminder



## Planar UTBB FD-SOI:

Best in class in core energy efficiency

6



- +50% energy efficiency, +30% peak performance @ 1.1V
- Full technology platform
- Longer life time of application processor

## Device Offer and Partitioning

17



### NovaThor™ L8580 - Cooler devices

- Core devices
  - 2Vt on UTBB SOI (RVT/LVT), adjustable through body bias
- I/O devices
  - EG 1.8V device on UTBB SOI
- Bit-cells
  - On UTBB SOI: HC 0.152 $\mu$ m<sup>2</sup>, HD 0.120 $\mu$ m<sup>2</sup>, HC/LV 0.197 $\mu$ m<sup>2</sup>
  - Same layouts as ST 28LP bit-cells
- Others
  - Full set of diodes, vertical bipolar, ESD protections
- Metal stack
  - Same as ST/ISDA 28LP
  - ST supported: 5U1x-0U2x-21
- Added value options
  - Decoupling planar MIM, 20fF

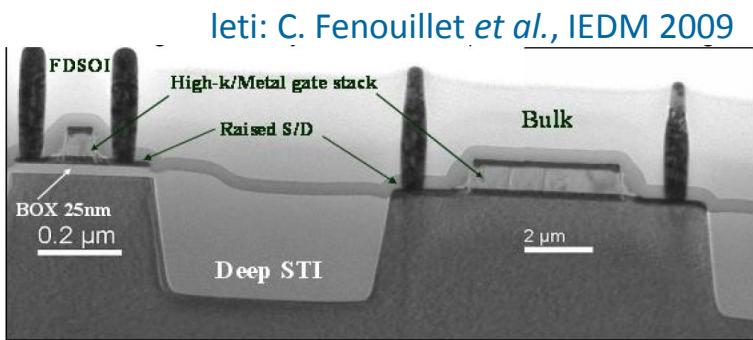
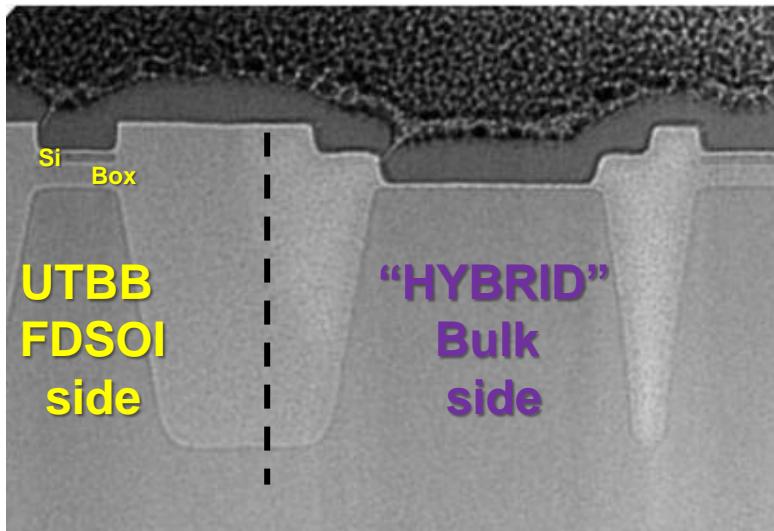


Cooler Smartphone can be used for longer time  
NovaThor™ L8580 platform running at 1GHz with Varm supplied at 0.65V



ST ERICSSON

# 28nm FDSOI: devices partitioning



Device Type	UTBB FD-SOI	BULK
Logic	2Vt / PB0-16nm*	
SRAM	✓	
Capacitance, Varactor	✓	
Drift MOS (OTP)		✓
Digital I/O	✓	
Analog MOS	✓	
RF MOS	✓	
Resistors	✓ (Poly)	✓ (Active)
Diodes (antenna)		✓
ESD Devices	✓ (FET)	✓ (FET, diode, SCR)
Vertical Bipolar		✓

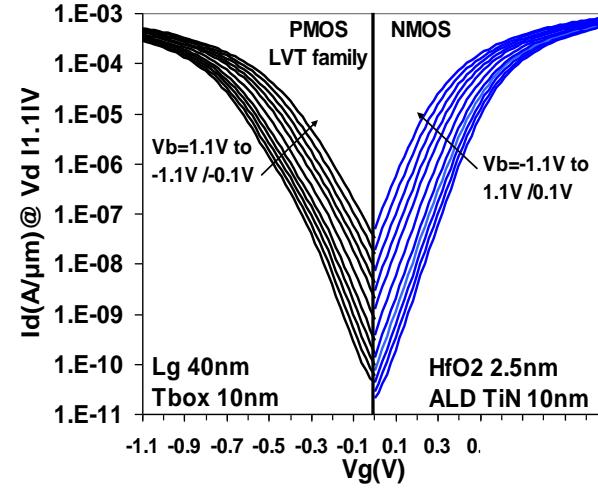
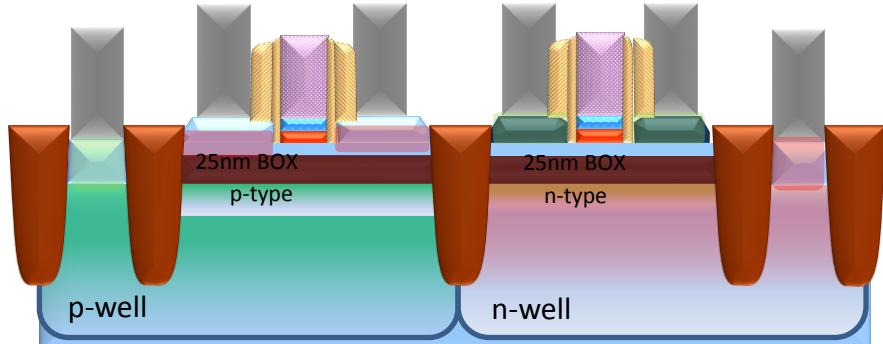
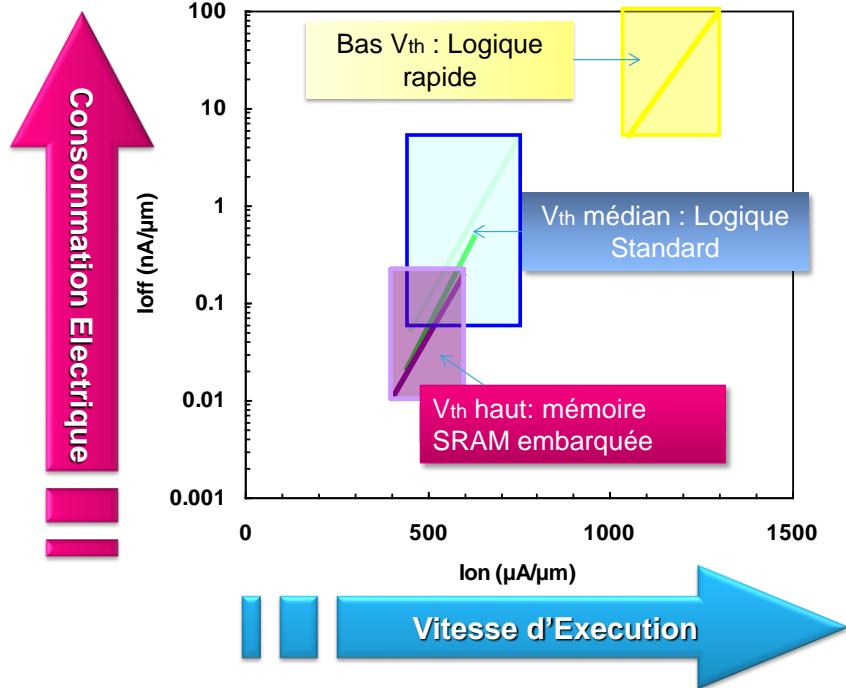
(\* ) PB = Poly Bias

Adapted from ST (J. Hartmann 2012)

- Key solutions for ESD protection & Performance enhancement

# Multi- $V_T$ and applications

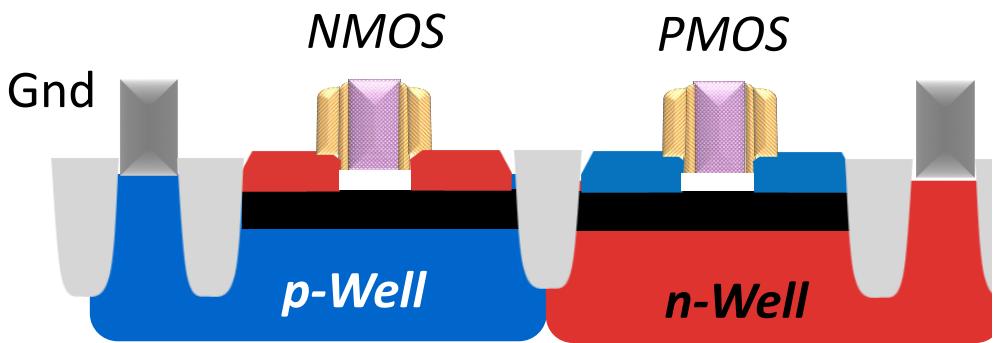
Adjustement of  $V_T$  versus the different elements that compose a circuit



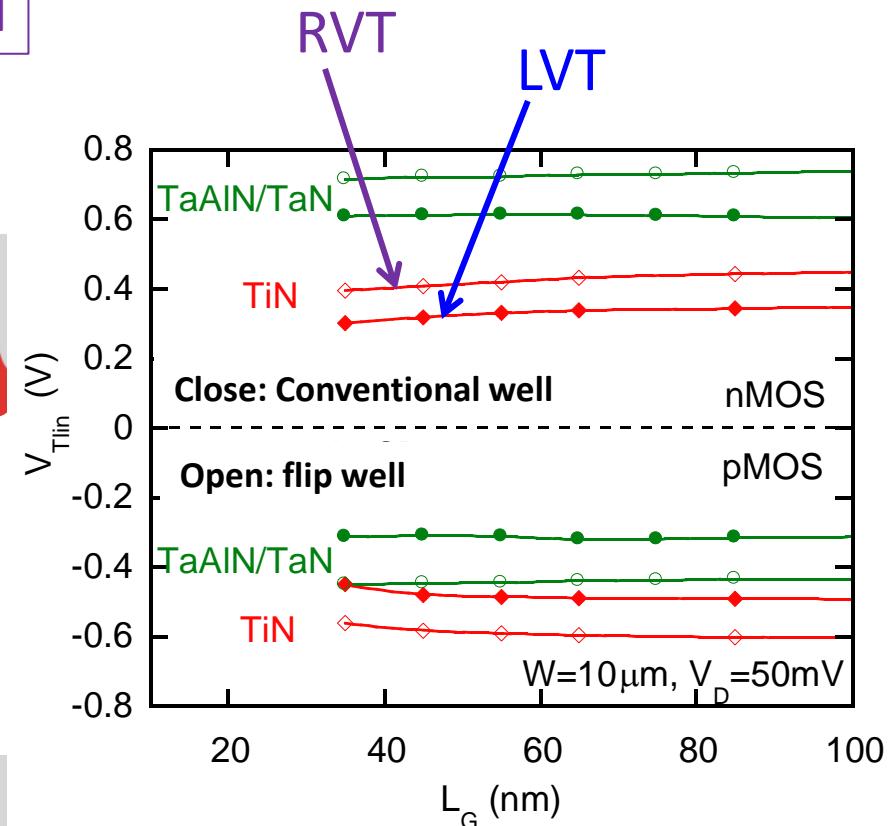
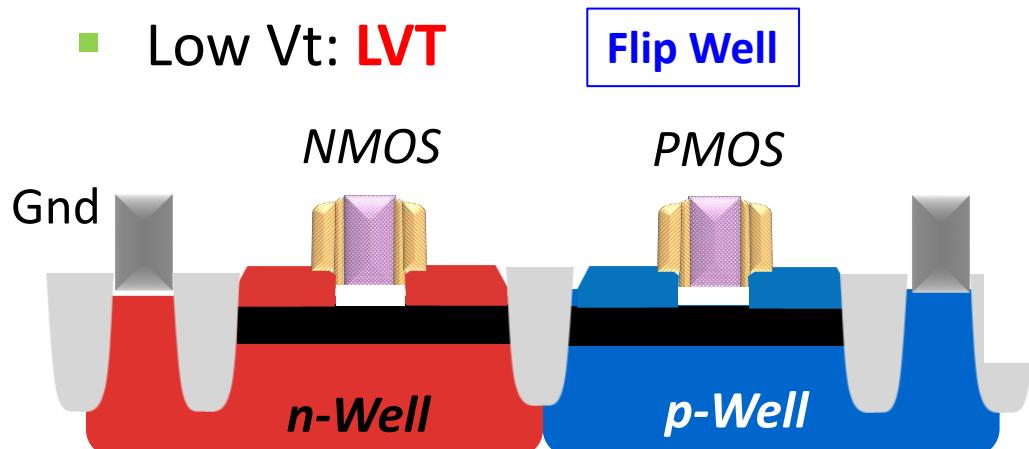
C. Fenouillet-Beranger et al. VLSI 2010

# 28nm FDSOI: Multi Vt

- Regular Vt: **RVT**



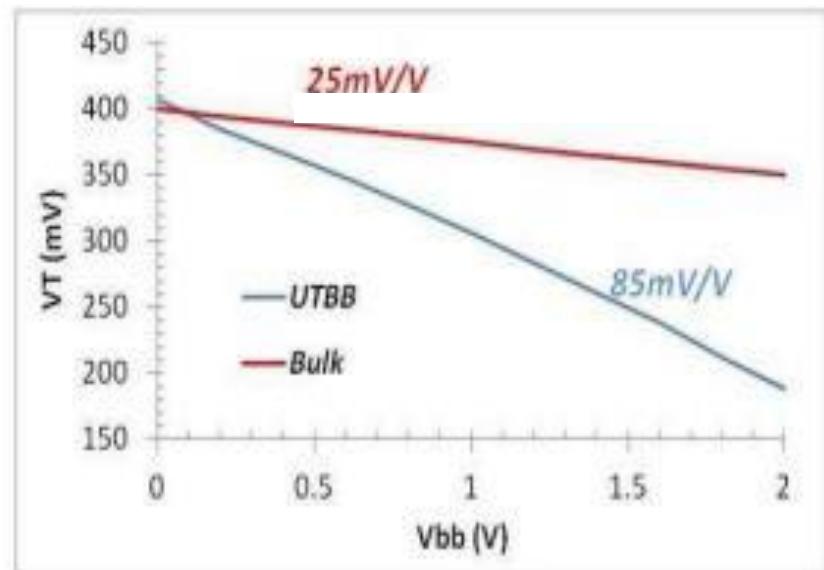
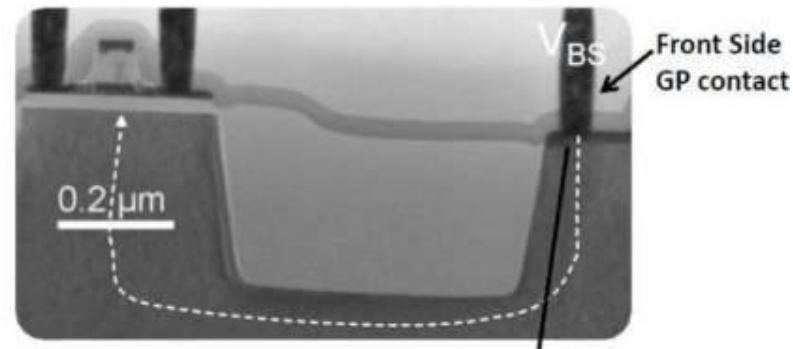
- Low Vt: **LVT**



Leti: O. Weber *et al.*, IEDM 2010

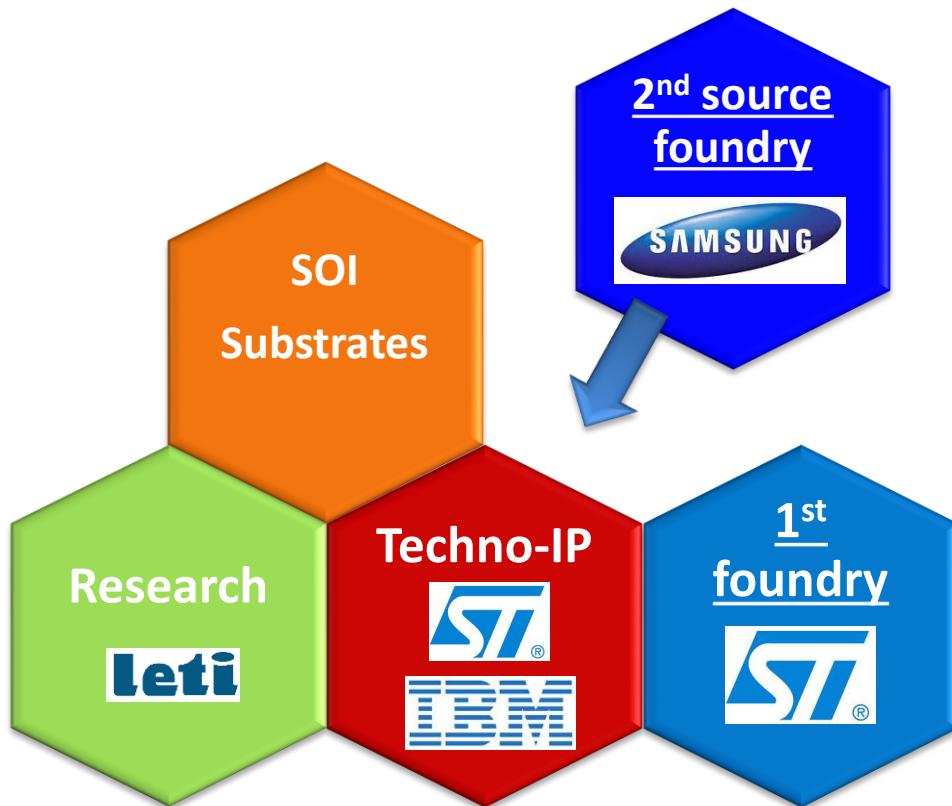
# 28nm FDSOI: Back bias effect

- Efficient to modulate the threshold voltage during circuit operation
- Reuse of Bulk design techniques
- No area penalty compared to Bulk
- Not possible with FinFET!
- $I_{ON}(I_{OFF})$  modulation through Forward and Reverse Back Bias
  - => improvement of the speed/Power tradeoff



# FDSOI

- May 2014:
  - Agreement on 28nm FDSOI



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## Samsung & ST Team Up on 28nm FD-SOI

Susan Rambo

5/14/2014 11:00 AM EDT  
11 comments

NO RATINGS  
LOGIN TO RATE

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SAN FRANCISCO — In a move that may extend 28nm mode and attract low-power, low-margin wearables and smartphone markets, European semiconductor manufacturer STMicroelectronics is partnering with Samsung on the 28nm FD-SOI (fully depleted silicon on insulator) process.

Under the agreement announced Wednesday (May 14), Samsung will license from ST 28nm FD-SOI design platform, thus making its foundry services effectively accessible to the broader semiconductor industry. Moreover, the two fabs have agreed to maintain compatible design processes.

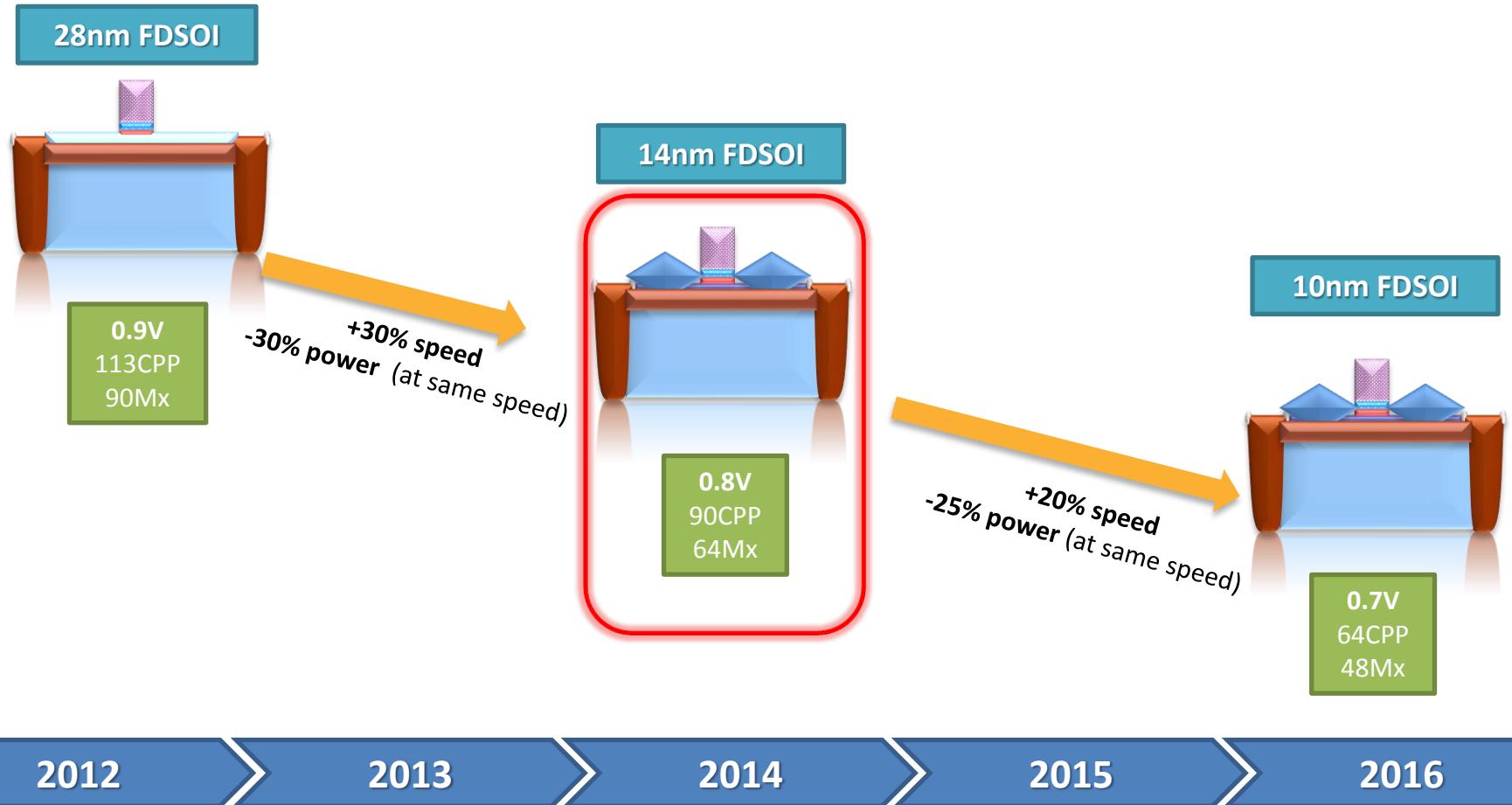
"It's not been a very well kept secret," Dean Freeman, Gartner's research vice president, told EE Times. ST even mentioned an agreement was signed in its earnings call in April. ST's investor day is tomorrow in New York.

Samsung brings reliable production capacity to 28nm FD-SOI, which the companies hope will encourage designers to adopt the process. While ST is already qualified for volume production at its Crolles facility, they needed more production volume. "ST couldn't support it [28nm FD-SOI] so they needed a partner," said Len Jelinek, IHS's research director for semiconductor manufacturing, in an interview with EE Times. "Choosing Samsung was a logical move."

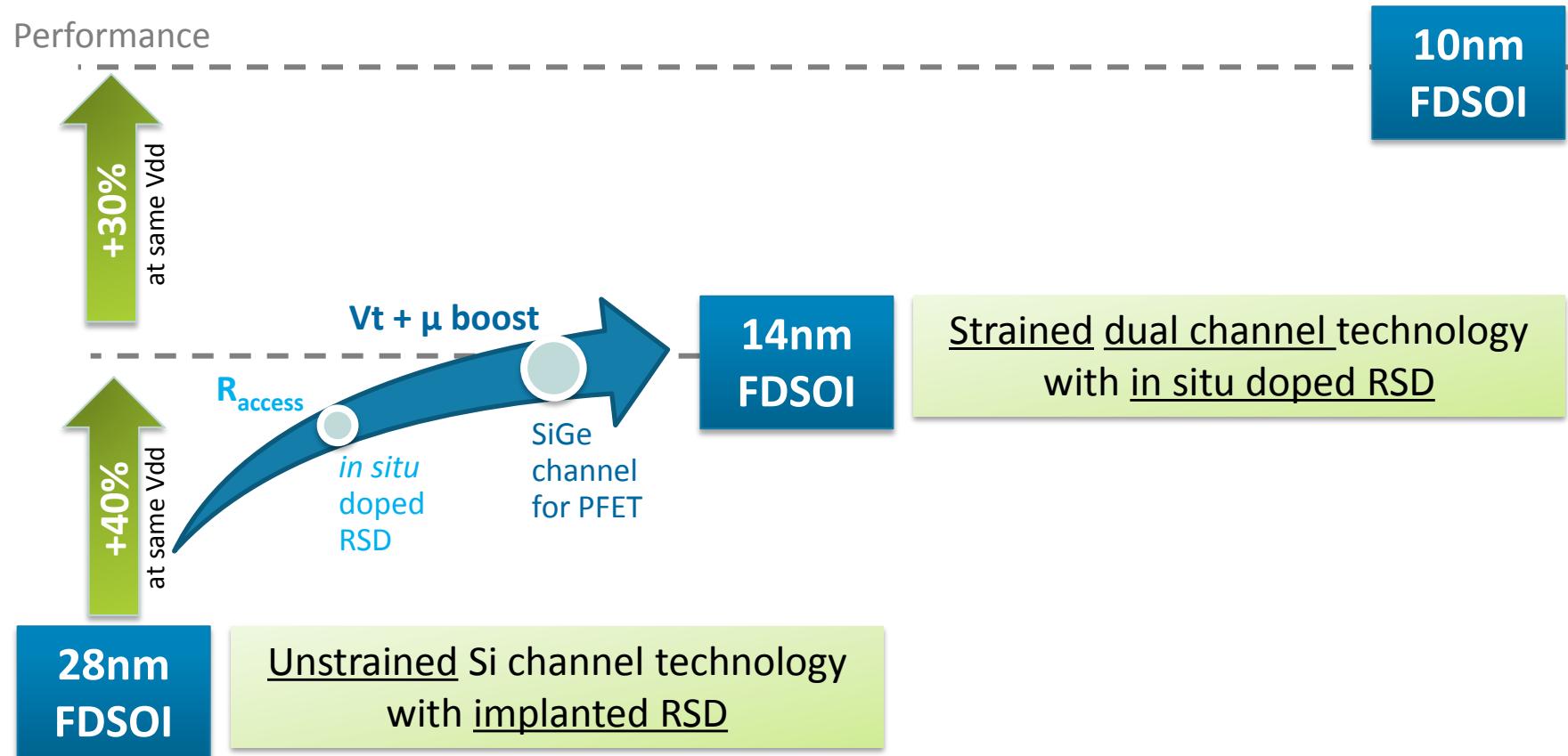
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# FDSOI is scalable



# FDSOI scalability: boosters roadmap

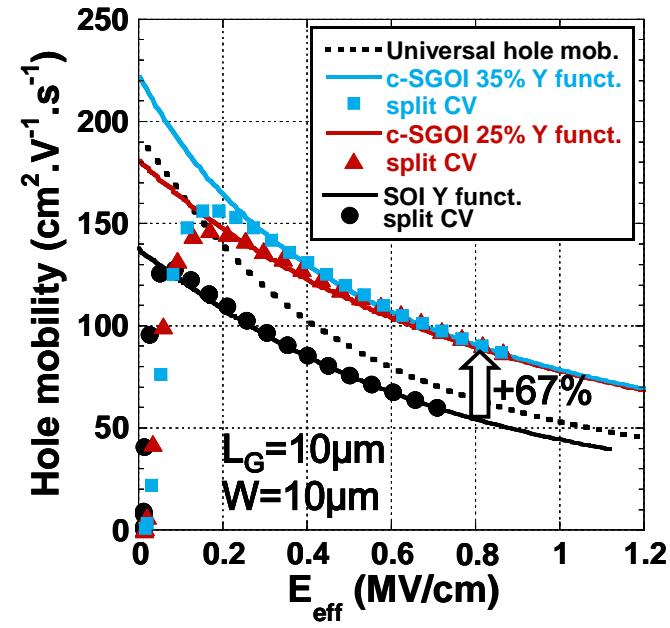
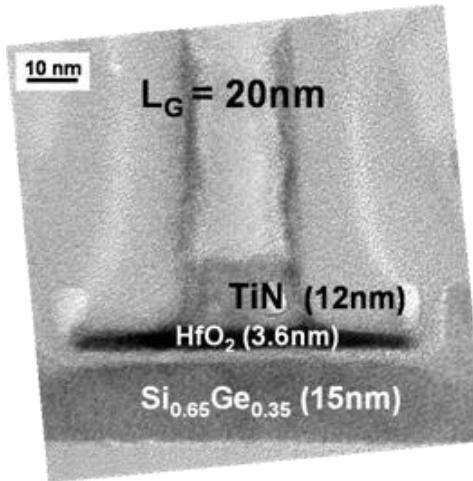
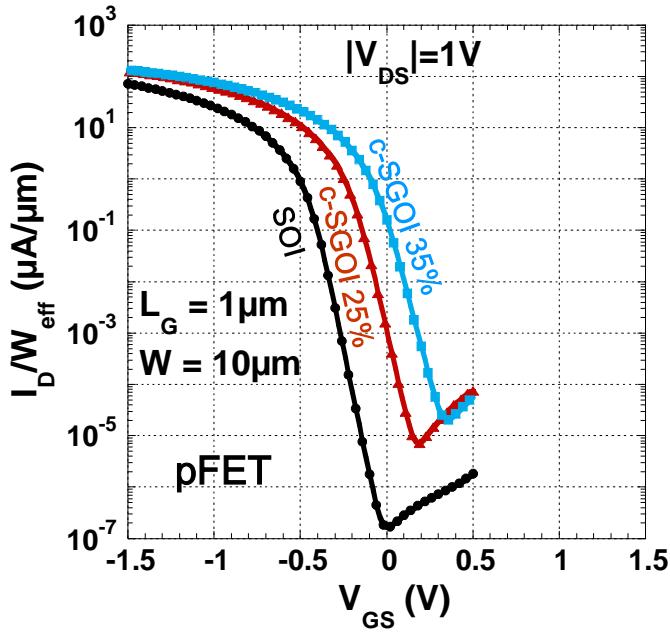


# 14nm FDSOI boosters

- SGOI pFET for  $V_{th}$  adjust &  $\mu$  boost

- Compressively strained SiGe channels with the Ge enrichment process\*

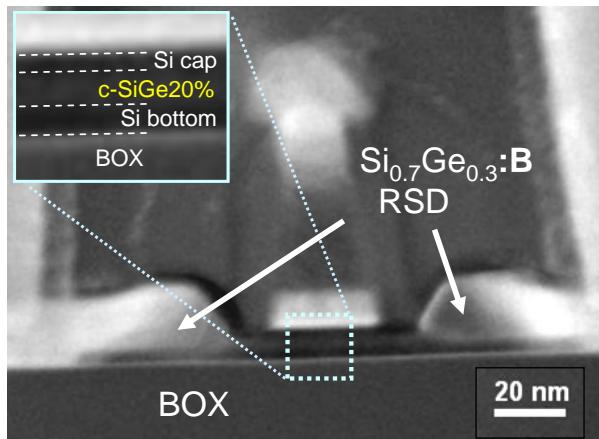
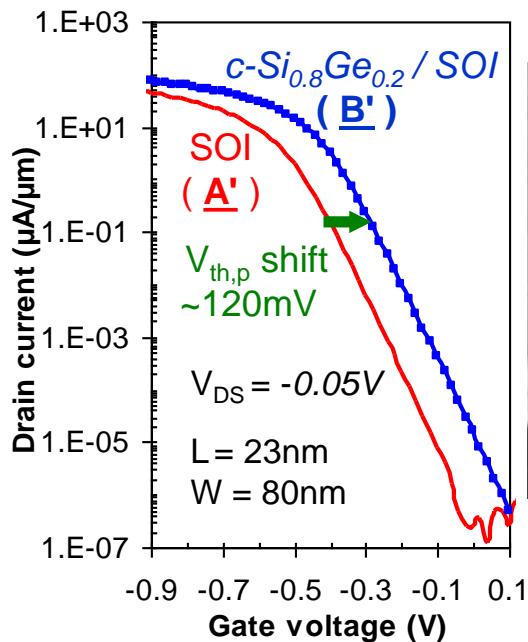
\*MIRAI: S. Nakaharai, et al. APL 83, p.3516 (2003)



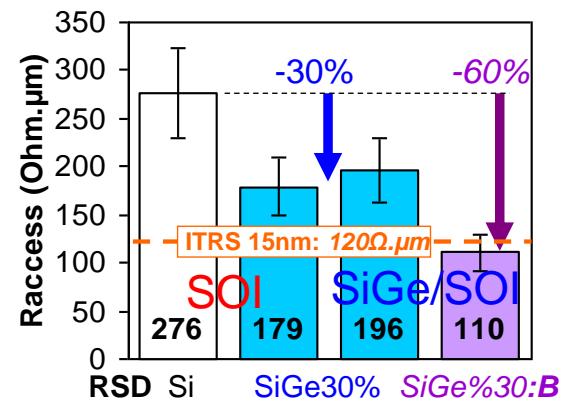
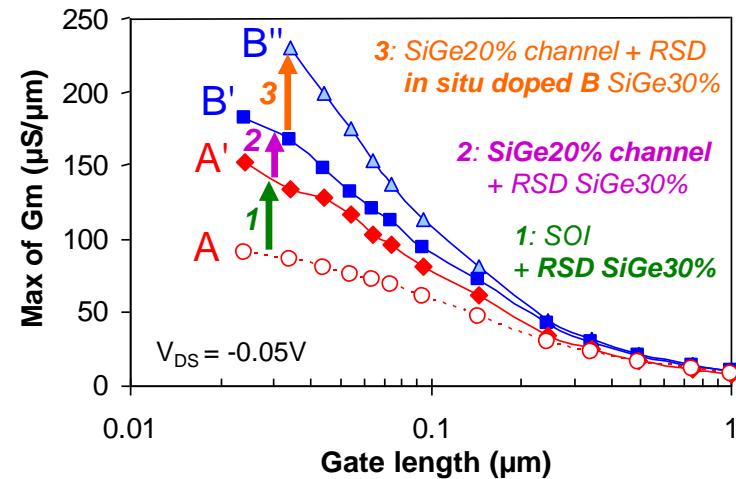
leti: L. Hutin et al., VLSI tech symp 2010

# 14nm FDSOI boosters

- Other option: SiGe/SOI pFET
  - Ultrathin SiGe on SOI for  $V_{th}$  adjust &  $\mu$  boost



- SiGe(:B) RSD for  $R_{access}$  reduction



leti: C. Le Royer et al., IEDM 2011

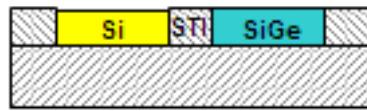
# 14nm FDSOI boosters

- Dual channel CMOS: SOI nFET + SGOI pFET

- Compressively strained SiGe channels with the Ge enrichment process\*

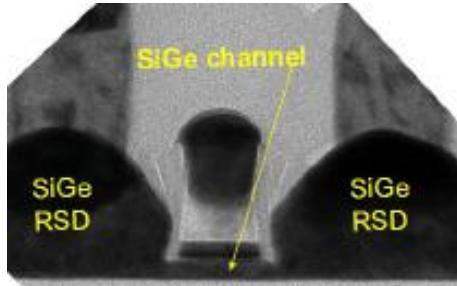


SiGe epi on SOI

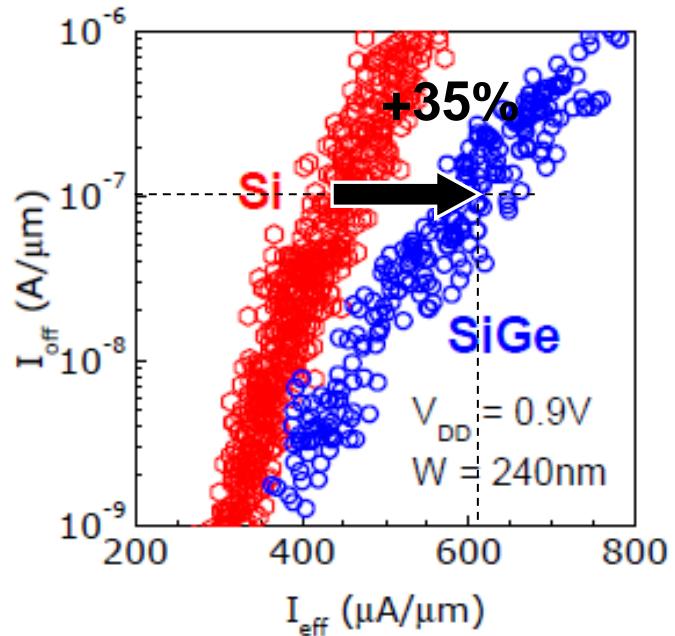


Ge enrichment

=> 6nm compressively strained  $\text{Si}_{0.75}\text{Ge}_{0.25}$  channel



\*MIRAI:  
S. Nakaharai, et al. APL 83, p.3516 (2003)

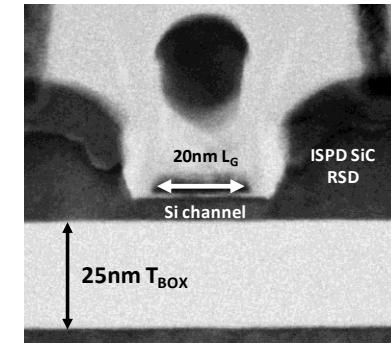
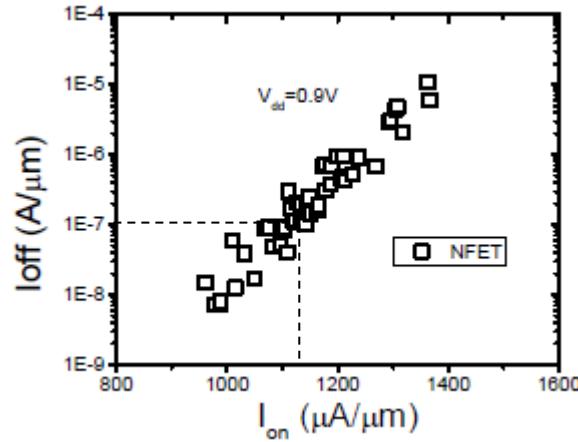
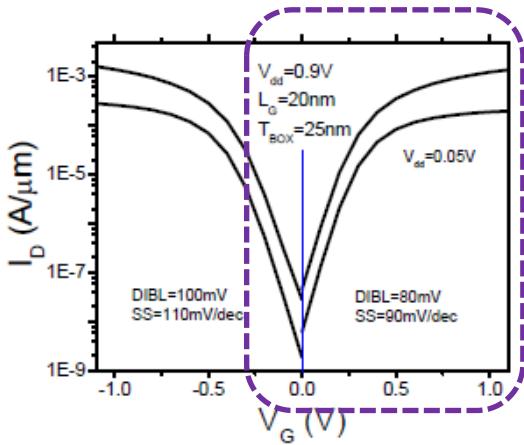


- SGOI pFET:  $I_{\text{EFF}} = 615\text{ }\mu\text{A}/\mu\text{m}$   
@  $I_{\text{OFF}} = 100\text{nA}/\mu\text{m}$ ,  $V_{\text{DS}} = -0.9\text{V}$

IBM: K. Cheng et al., IEDM 2012

# 14nm FDSOI boosters

- Dual channel CMOS: SOI nFET + SGOI pFET

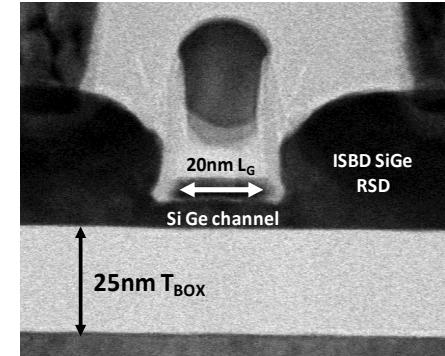
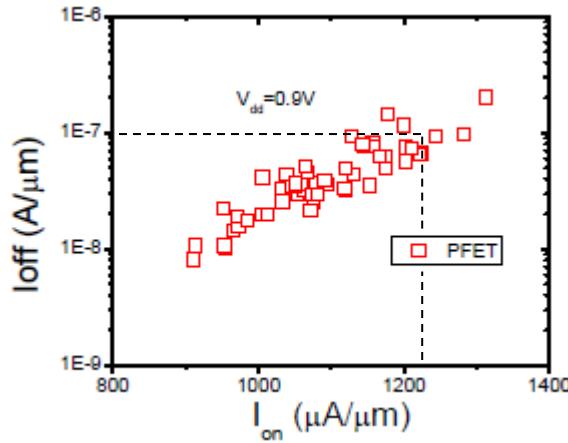
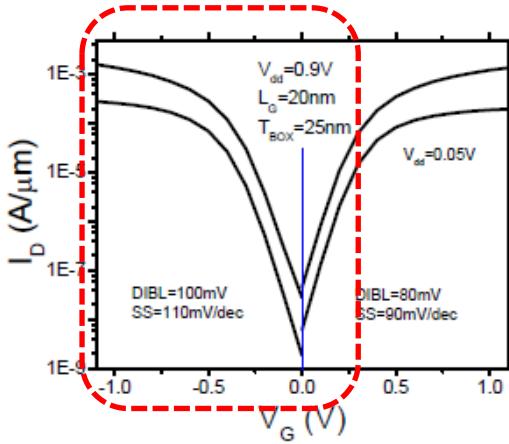


- SOI nFET:**
  - No strain in Si channel
  - $I_{ON} = 1120\mu\text{A}/\mu\text{m}$  @  $I_{OFF} = 100\text{nA}/\mu\text{m}$ ,  $V_{DS} = -0.9\text{V}$
  - $I_{EFF} = 630\mu\text{A}/\mu\text{m}$  @  $I_{OFF} = 100\text{nA}/\mu\text{m}$ ,  $V_{DS} = -0.9\text{V}$

ST-IBM: Q. Liu *et al.*, IEDM 2013

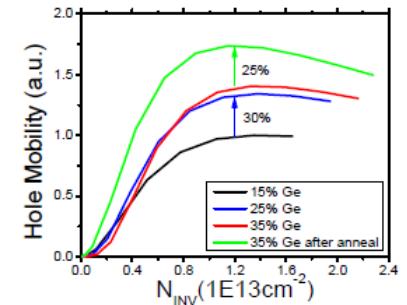
# 14nm FDSOI boosters

- Dual channel CMOS: SOI nFET + SGOI pFET



- SGOI pFET:**

- Compressively strained  $\text{Si}_{0.75}\text{Ge}_{0.25}$  channels:  **$\mu$  boost**
  - Ge enr. + SiGe:B RSD
- $I_{ON} = 1220\mu\text{A}/\mu\text{m}$  @  $I_{OFF} = 100\text{nA}/\mu\text{m}$ ,  $V_{DS} = -0.9\text{V}$
- $I_{EFF} = 670\mu\text{A}/\mu\text{m}$  @  $I_{OFF} = 100\text{nA}/\mu\text{m}$ ,  $V_{DS} = -0.9\text{V}$



ST-IBM: Q. Liu *et al.*, IEDM 2013

# 14nm FDSOI boosters

- Dual channel CMOS: SOI nFET + SGOI pFET
  - Benchmark: DC performance

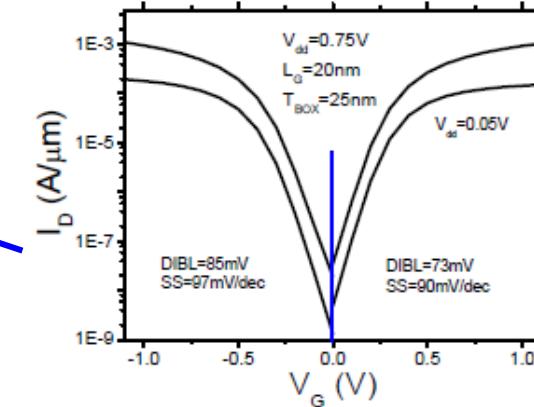
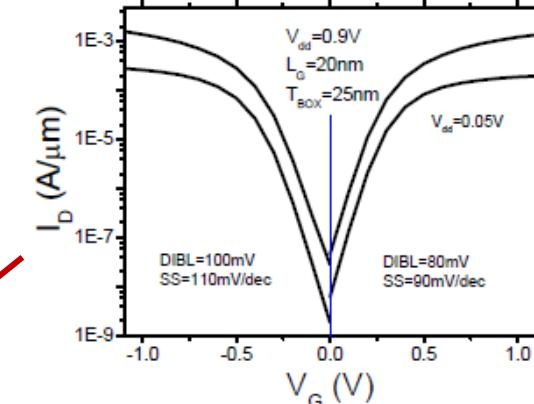
Intel VLSI 2012      Intel IEDM 2012

	Auth et al [8]	Jan et al [9]	ST-IBM: Q. Liu et al., IEDM 2013		
CGP (nm)	90	90	100		
$L_G$ (nm)	30	30	20		
$V_{dd}$ (V)	0.8	0.75	0.75	0.8	0.9
N/P DIBL (mV/V)	46/50	30/35	73/85	78/90	80/100
N/P SS (mV/dec)	69/72	71/72	90/97	90/101	90/110
$I_{off}$ (nA/ $\mu$ m)	100	100	100	100	100
N/P $I_{on}$ (mA/ $\mu$ m)	1.02/0.9	0.88/0.74	0.86/0.82	0.99/0.98	1.12/1.22
N/P $I_{eff}$ (mA/ $\mu$ m)	0.53/0.46		0.47/0.45	0.51/0.53	0.63/0.67

FinFET

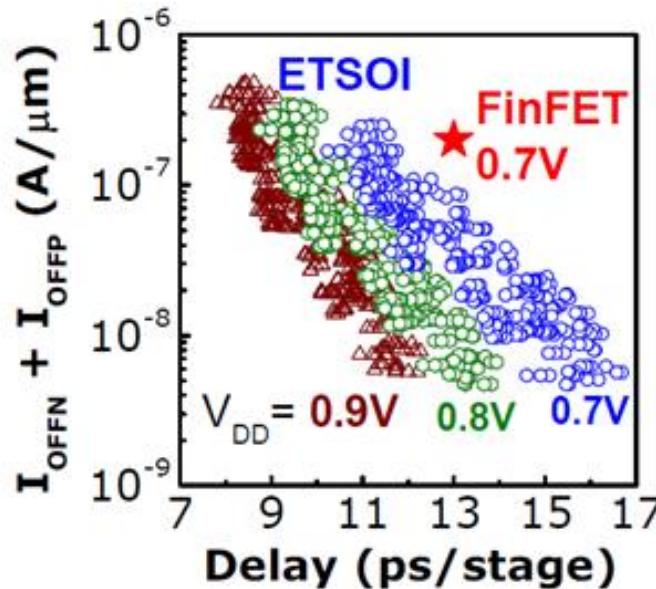
FinFET

FDSOI



# 14nm FDSOI boosters

- Dual channel CMOS: SOI nFET + SGOI pFET
  - Benchmark: AC performance



$V_{DD}$	I <sub>off</sub> = 200nA/ $\mu\text{m}$	
	ETSOI	finFET*
0.9V	8.5	
0.7V	11.2	13.5

\*C. Auth, et al. Presented  
at Symp. VLSI Tech., 2012

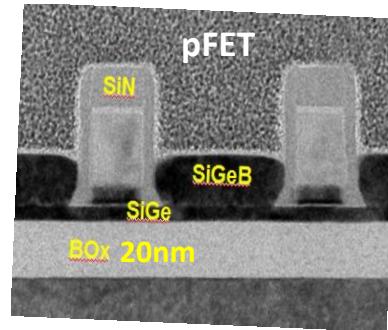
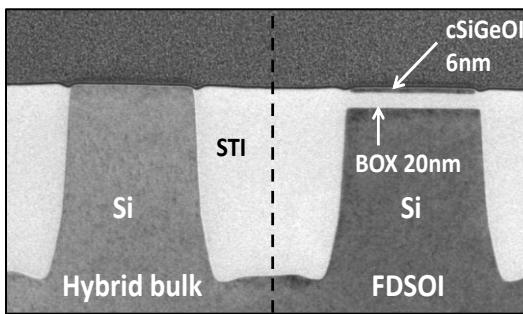
- Fastest Ring Oscillators performance ever reported!

ST-IBM: Q. Liu et al., IEDM 2013

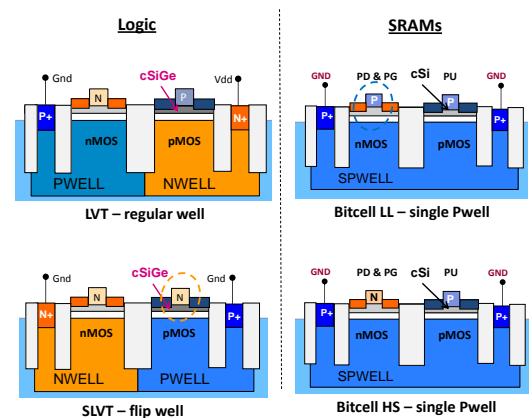
# 14nm FDSOI platform: process integration

## Process integration

- 6nm Si / cSiGe dualchannel w. 20nm BOX (undoped channel)
- Hybrid bulk-SOI co-integration
- Ground-Plane for  $V_{th}$  adjust
- Two  $V_{th}$  flavors: LVT, SLVT
- Contact Poly Pitch (CPP): 90nm
- Min. gate length: 20nm
- High-K/Dual Metal Gate, Gate First
- Dual-epi SiC:Ph / SiGe:B Raised S-D



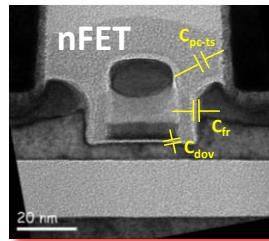
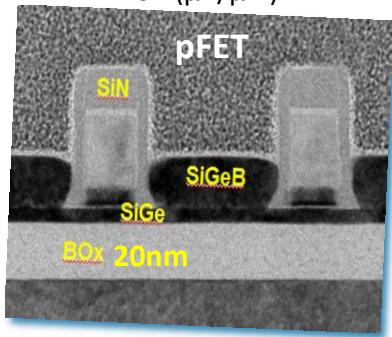
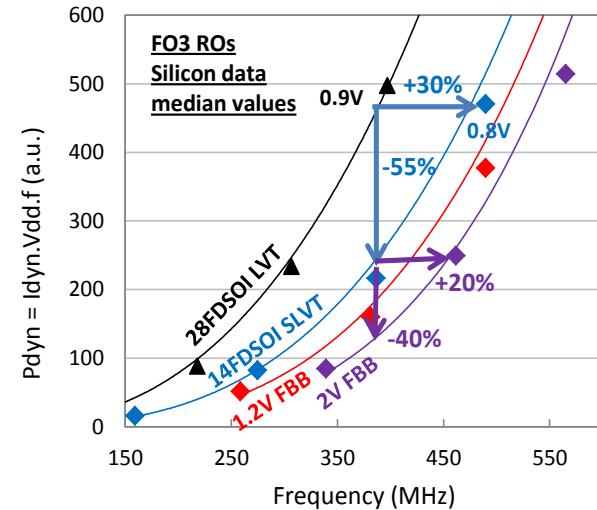
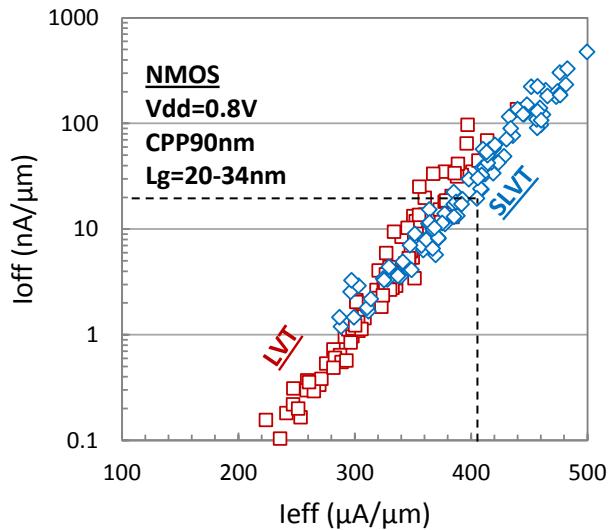
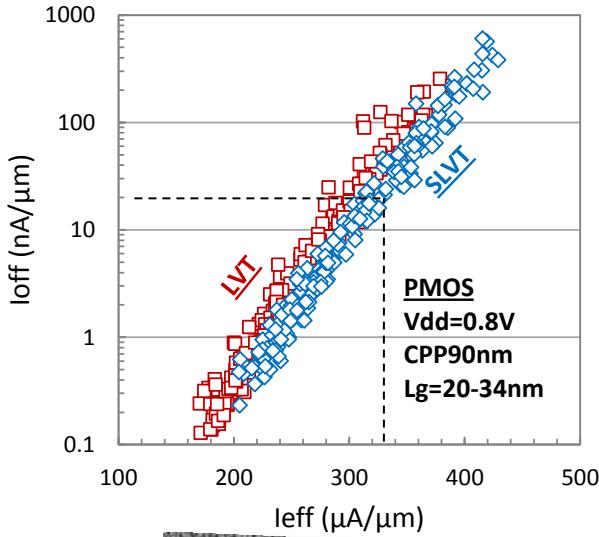
Key features	28FDSOI	14FDSOI
Min Contact gate pitch CPP	114nm	90nm
M1 pitch	90nm	64nm
Std cell area	1X	0.55X
VT flavours	RVT / LVT	LVT / SLVT
Lgate in min CPP	24nm → 30nm	20nm → 34nm
Channel	SOI 7nm	Dual SOI/SiGeOI 6nm
Buried oxide	BOX 25nm	BOX 20nm
Gate	HKMG single metal	HKMG dual WF
Source-Drain	Single Si epi + I/I	Dual epi SiGeB/Si:CP



ST-IBM-leti:  
O. Weber *et al.*, VLSI tech. symp. 2014

# 14nm FDSOI platform:

## Performance (2014 Q2):



- $I_{EFF,P} = 330 \mu\text{A}/\mu\text{m}$  &  $I_{EFF,N} = 405 \mu\text{A}/\mu\text{m}$   
@  $I_{OFF}=20\text{nA}/\mu\text{m}$ ,  $V_{DD}=0.8\text{V}$

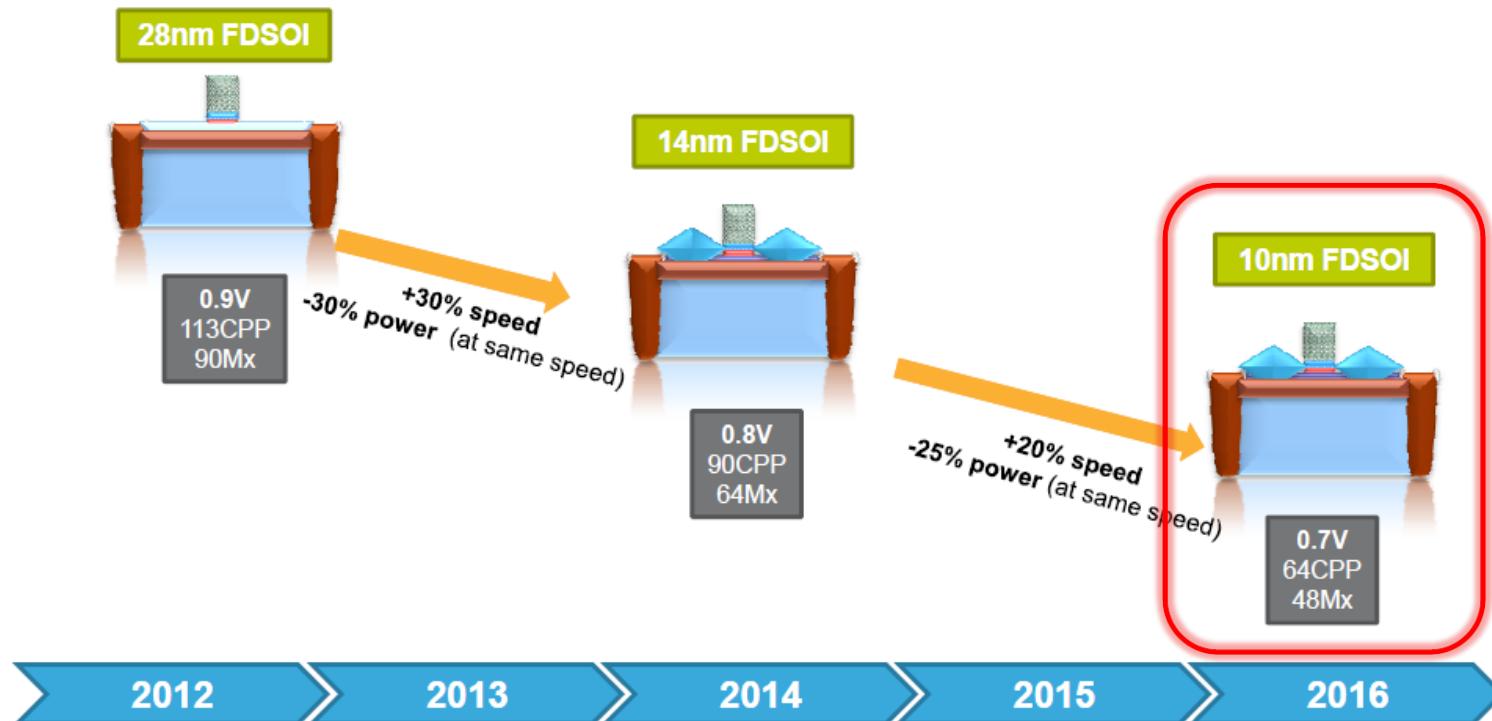
ST-IBM-leti:  
O. Weber *et al.*, VLSI tech. symp. 2014

# Outline

- Introduction to planar FDSOI
- 28nm FDSOI [platform]
  - Process integration, results reminder, devices partitioning
  - Multi Vt, back bias effect, variability
- 14nm FDSOI [development]
  - Boosters, process integration
  - Scalability
- 10nm FDSOI [R&D]
  - Geometrical scaling, new modules, strain for  $\mu$  boost
- Conclusions

# FDSOI is scalable

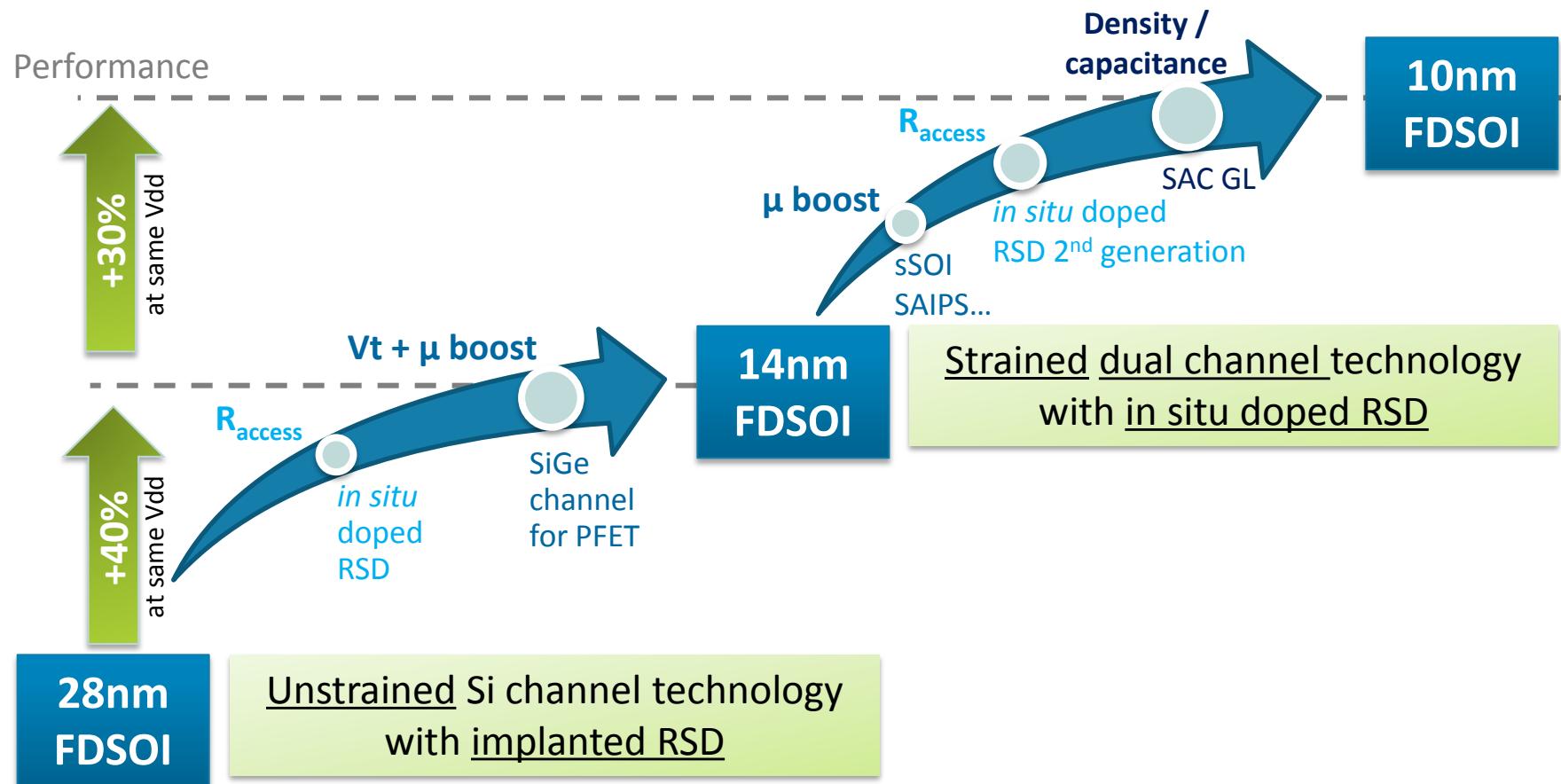
## Planar UTBB FD-SOI: Enabling Moore's Law with Planar Process & Design



leti

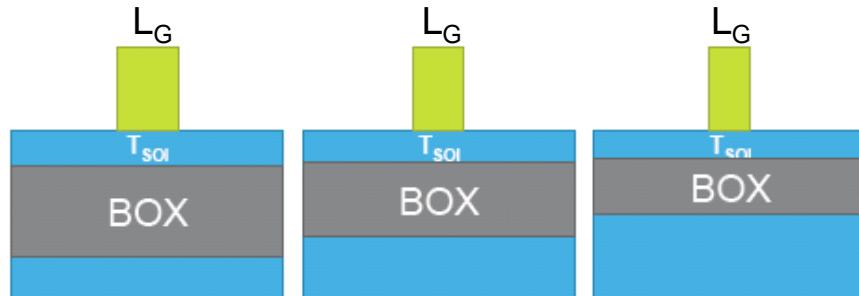
Planar FD-SOI Technology at 28nm and below for extremely power-efficient SoCs December 2012

# FDSOI scalability: boosters roadmap



# 10nm FDSOI: Geometrical scaling

- Thinner Si body, thinner BOX



O. Faynot *et al.*, IEDM 2010

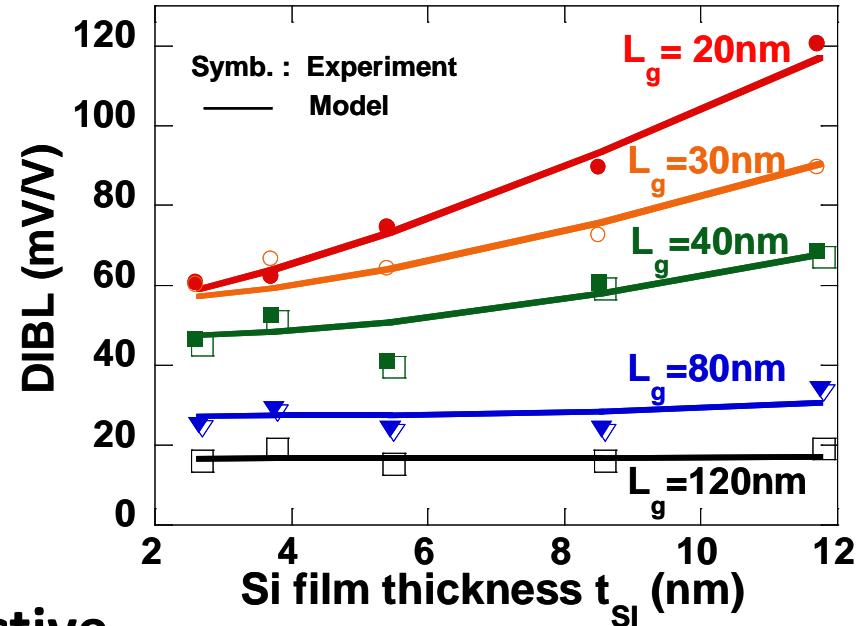
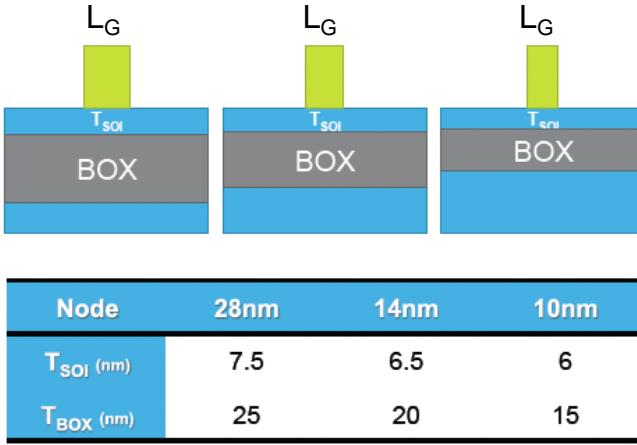
Node	28nm	14nm	10nm
T <sub>SOI</sub> (nm)	7.5	6.5	6
T <sub>BOX</sub> (nm)	25	20	15

- L<sub>G</sub>, T<sub>SOI</sub>, and T<sub>BOX</sub> have impact on DIBL
  - SOI : Si body scaling down to 3.5nm *without impact on performance*

A. Khakifirooz *et al.*, IEEE EDL 2012

# 10nm FDSOI: Geometrical scaling

- Thinner Si body for enhanced electrostatics



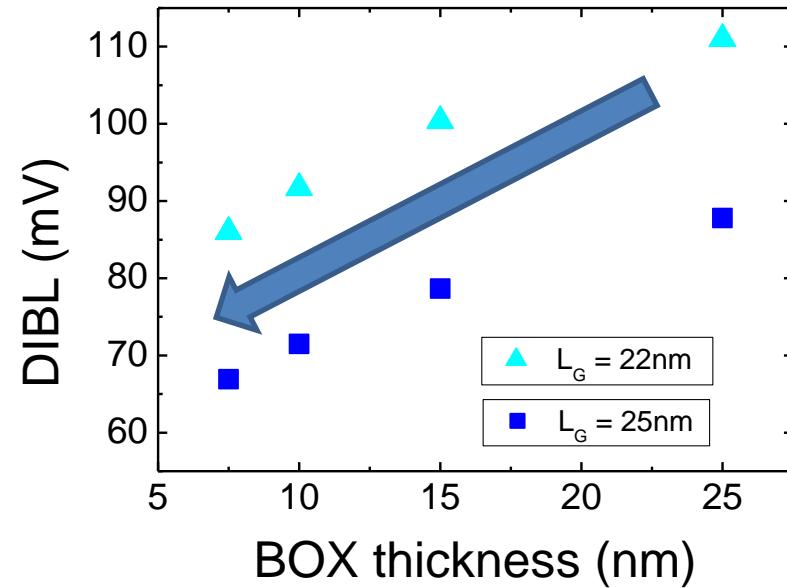
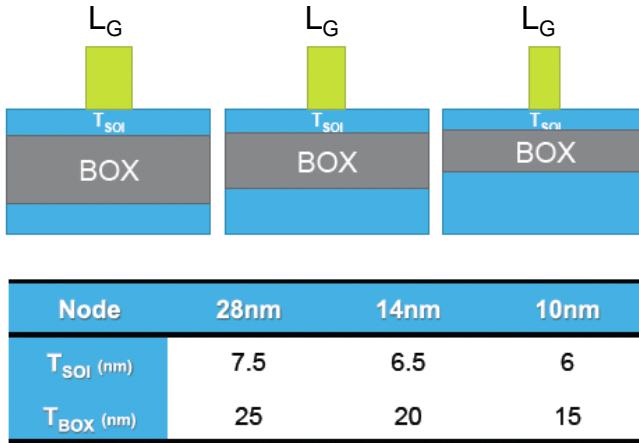
- Thinner Si body is effective to reduce SCE and DIBL

- Beware of Si film amorphisation (in case of ion implanted S-D)
- Thanks to selective *in situ* doped epi S-D, access resistance can be controlled down to 5nm SOI film

V. Barral *et al.*, VLSI tech symp 2007

# 10nm FDSOI: Geometrical scaling

- Thinner BOX for enhanced electrostatics

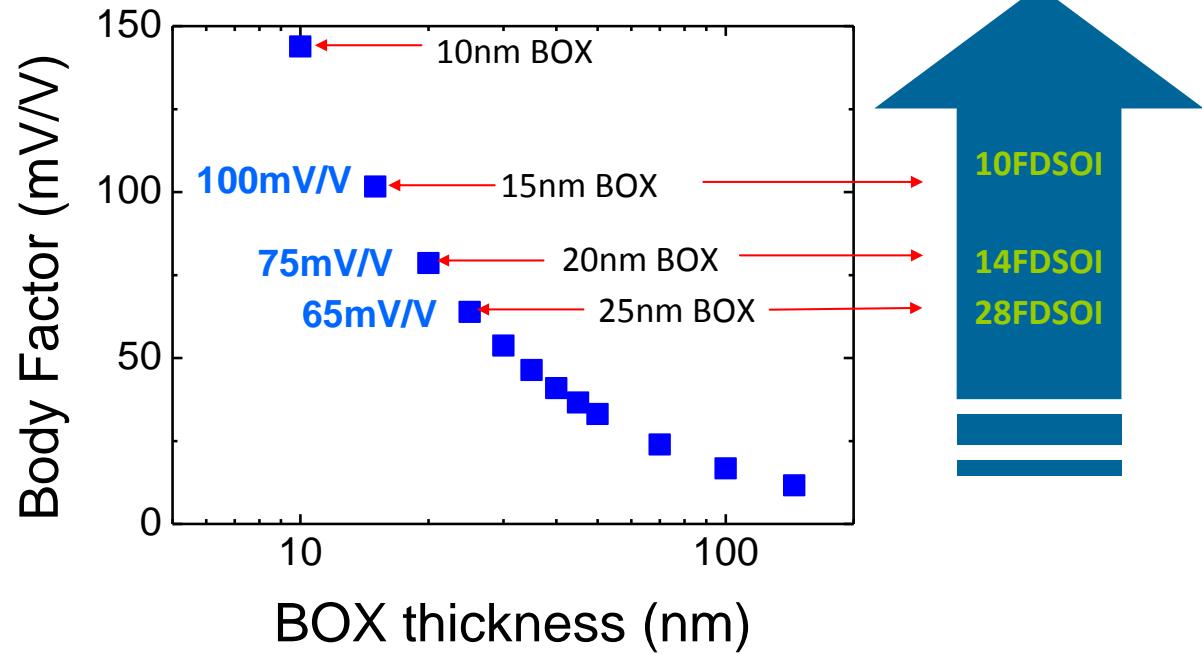
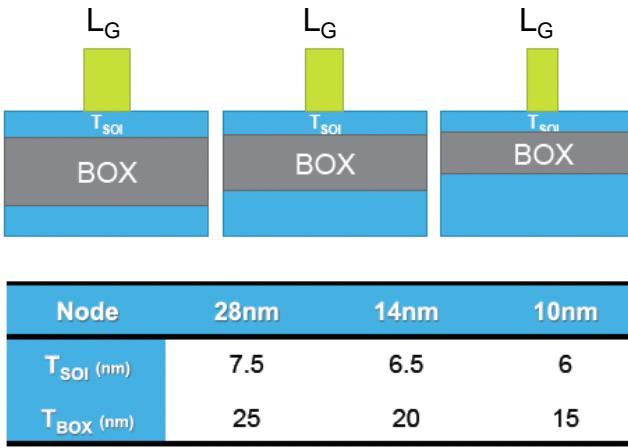


- Thinner BOX is effective to reduce SCE and DIBL

L. Grenouillet *et al.*, S3S conf 2013

# 10nm FDSOI: Geometrical scaling

- Thinner BOX for enhanced electrostatics

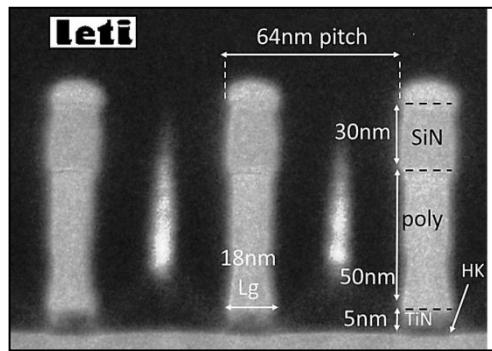
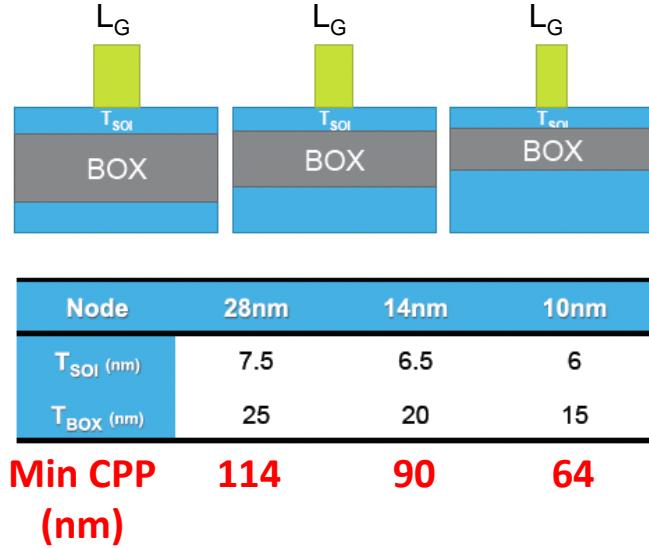


- Back bias efficiency improved  
(body factor improvement)

L. Grenouillet *et al.*, S3S conf 2013

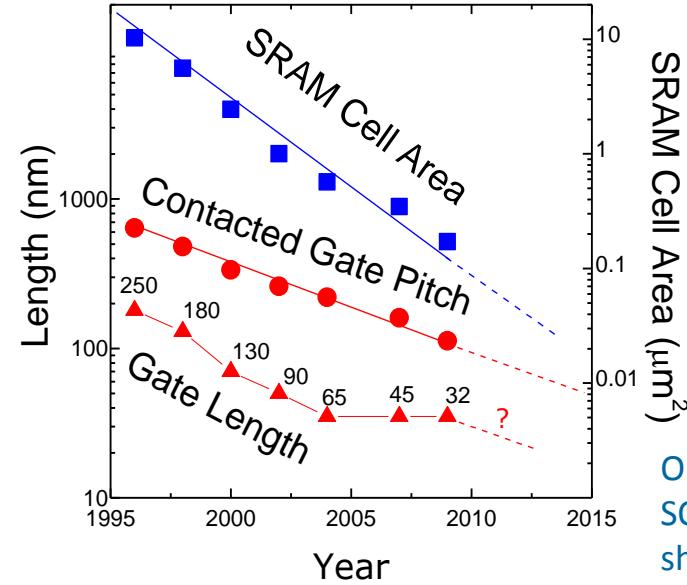
# 10nm FDSOI: Geometrical scaling

- Tighter CPP for higher device density

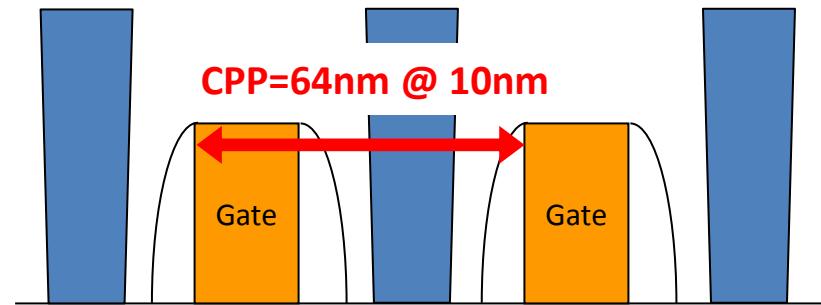


Leti-ST:

H. Niebojewski *et al.*, S3S conf. 2013

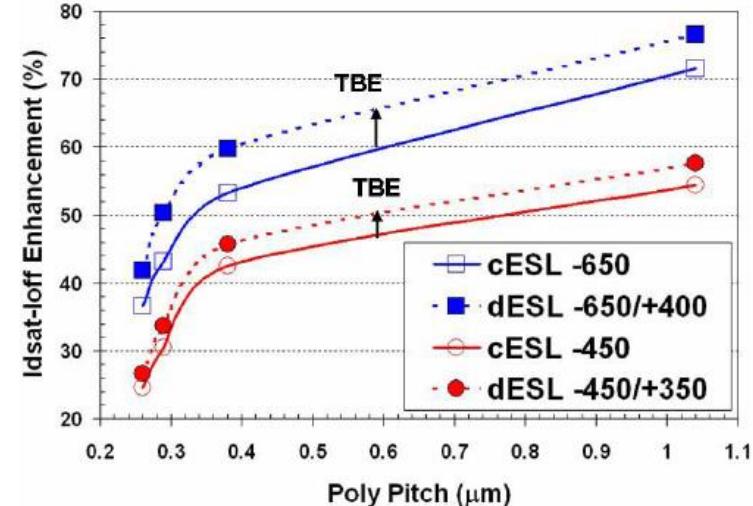
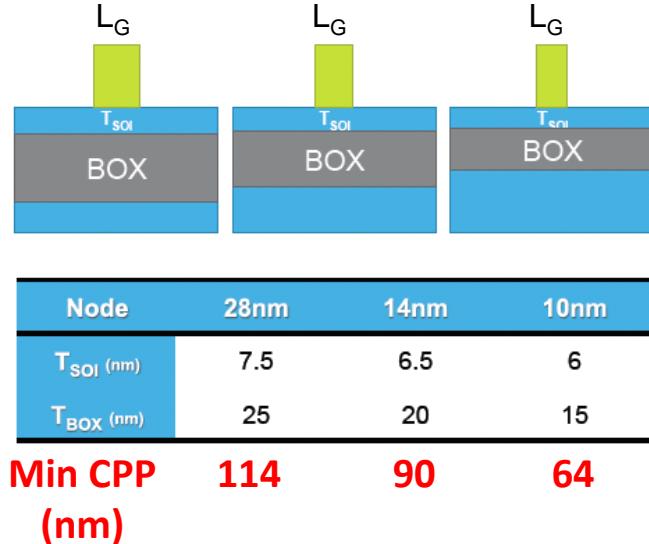


O. Faynot,  
SOI conf. 2011  
short course



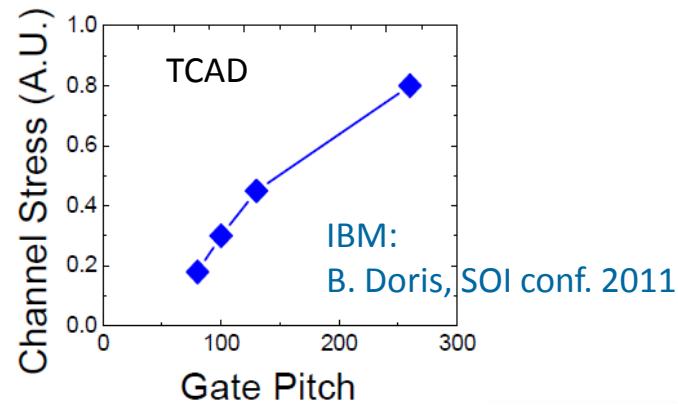
# 10nm FDSOI: Geometrical scaling

- Tighter CPP for larger device density



Freescale : P. Grudowski *et al.*, VLSI tech symp 2006

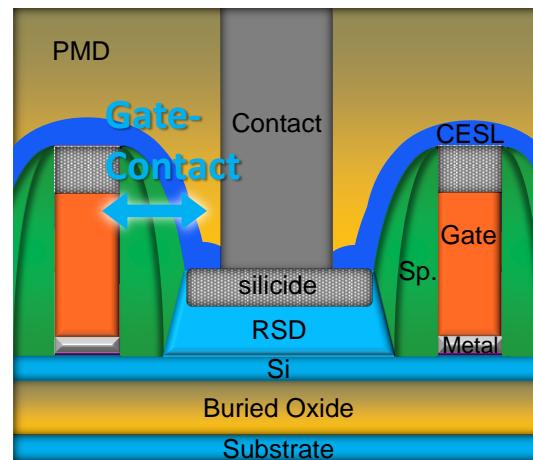
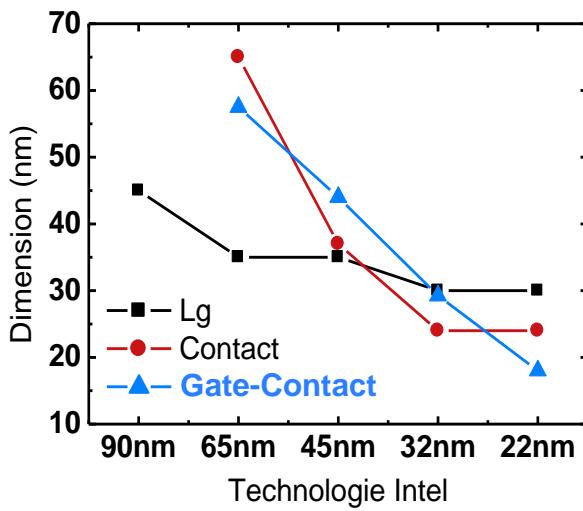
- Consequence (1/2):
  - Benefits of stressors get smaller for tight pitch (bulk, finFET, FD)  
=> Need to look at substrate for  $\mu$  boost



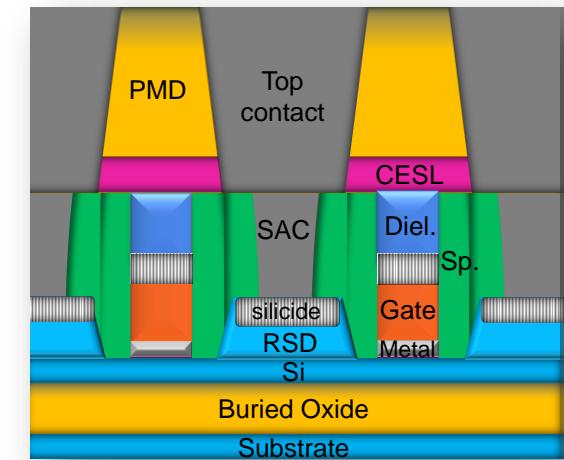
# 10nm FDSOI: Geometrical scaling

- Consequence (2/2):
  - Less space for contacts

=> *Self-Aligned contacts (SAC)*

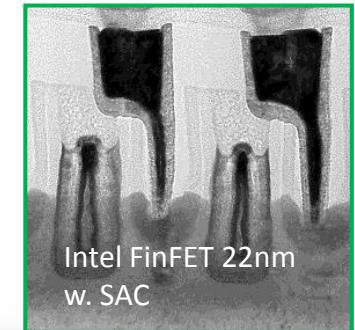


Classical contacts



SAC architecture

C. Auth *et al.*,  
VLSI tech symp 2012



Intel FinFET 22nm  
w. SAC

Leti-ST:

H. Niebojewski *et al.*, S3S conf. 2013

# 10nm FDSOI: new modules

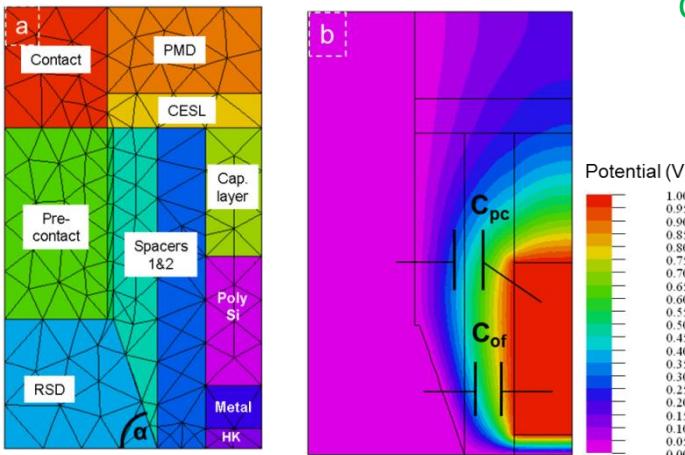
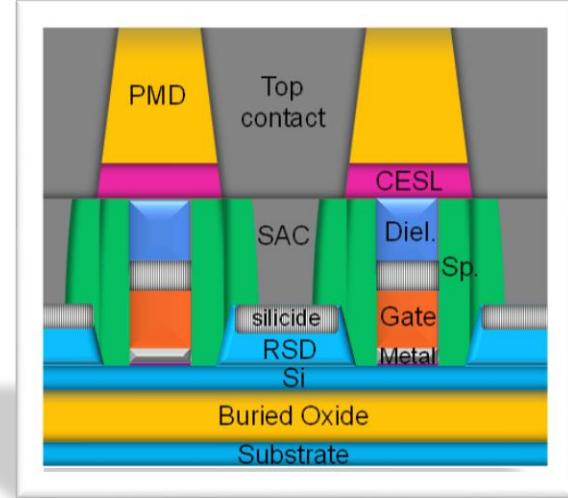
## ■ Self-Aligned contacts (SAC)

- Mandatory for tight CPP
- Misalignment-proof structure

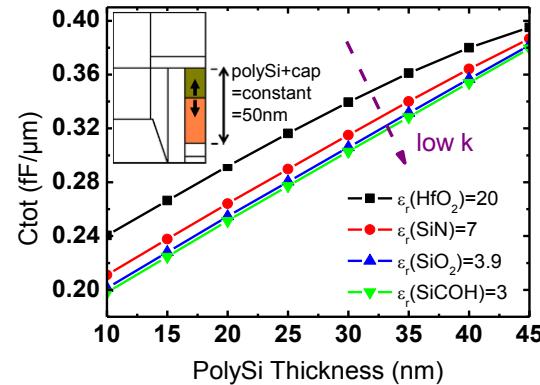
## ■ TCAD/SPICE results

### ▪ At the device level:

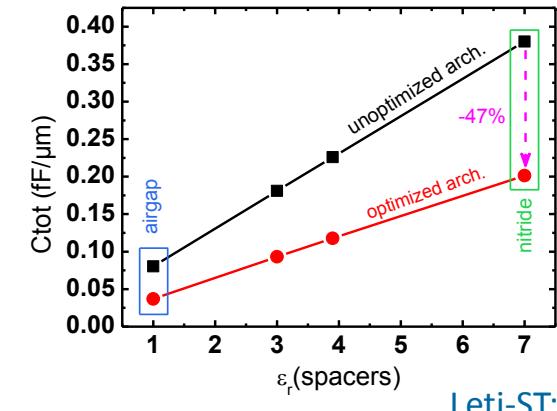
- Geometrical optimizations & **low-k spacers** to minimize parasitic capacitances



C<sub>tot</sub> reduced with PolySi thickness reduction



Further reduction with airgap



Leti-ST:

H. Niebojewski *et al.*, S3S conf. 2013

# 10nm FDSOI: new modules

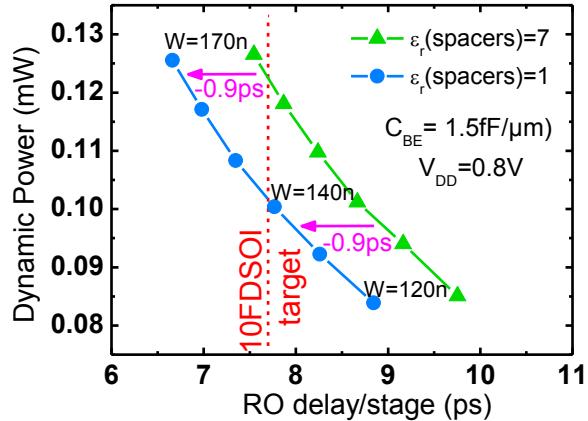
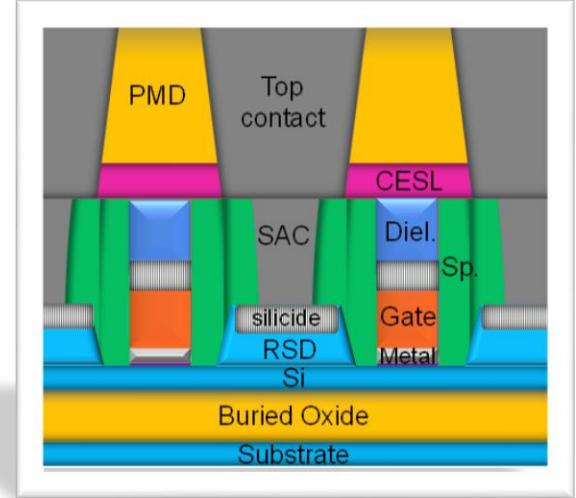
## ■ Self-Aligned contacts (SAC)

- Mandatory for tight CPP
- Misalignment-proof structure

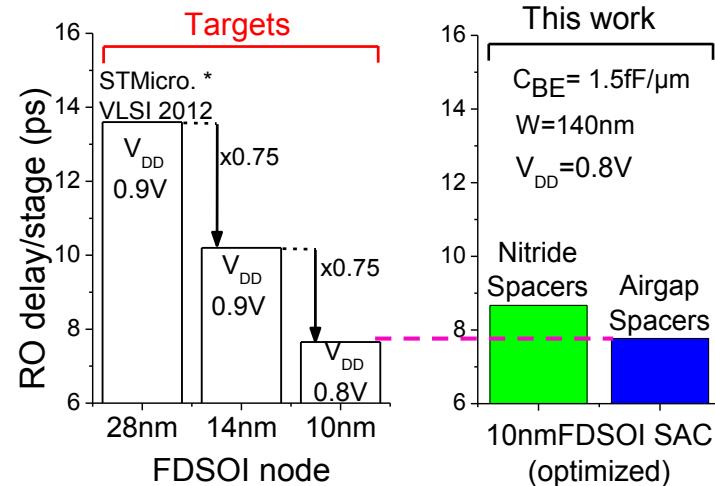
## ■ TCAD/SPICE results

### ▪ At the circuit level:

- The use of **low-k spacers** is mandatory to achieve 10nm node delay specifications



Airgap required to meet 10nm FDSOI target

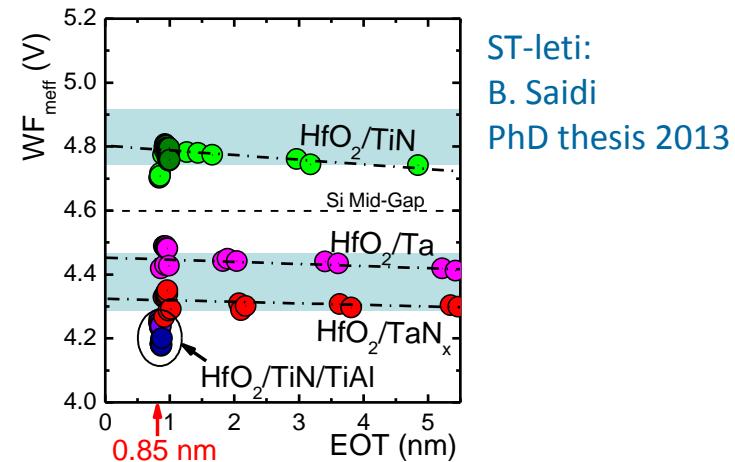
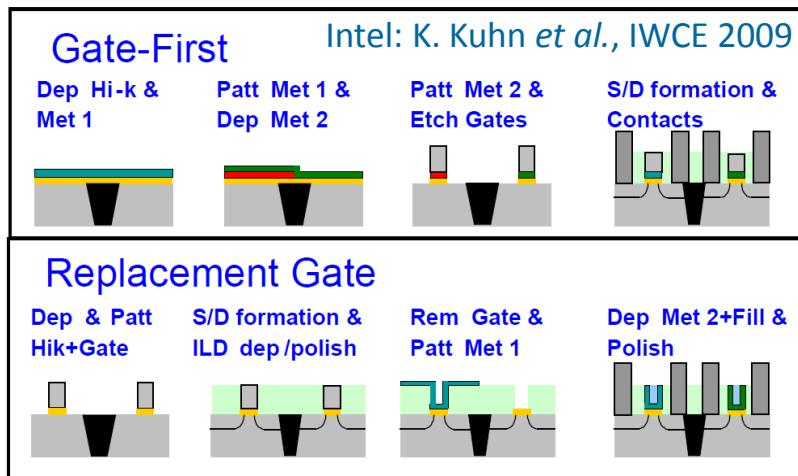


H. Niebojewski *et al.*, S3S conf. 2013

# 10nm FDSOI: new modules

## ■ Gate Last (GL)

- Pursue the **EOT scaling** ... with a good reliability
  - due to low thermal budget (in the case of HK last)
- Adjust the **threshold voltage**
  - Gate first: WF tend to midgap +  $V_{FB}$  roll-off
  - Gate last: Easier WF tuning + less  $V_{FB}$  roll-off (lower th. budget.)



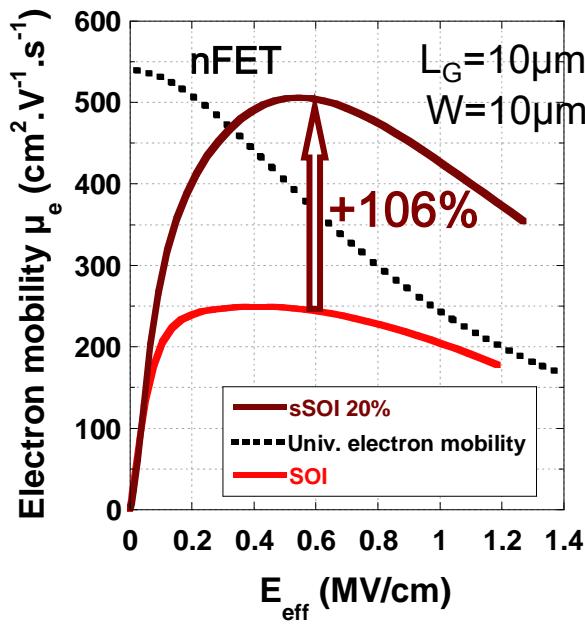
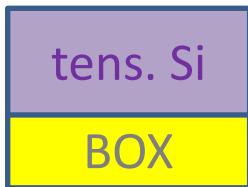
- Induce **more strain** in the channel: cf. next part

# 10nm FDSOI: strain for $\mu$ boost

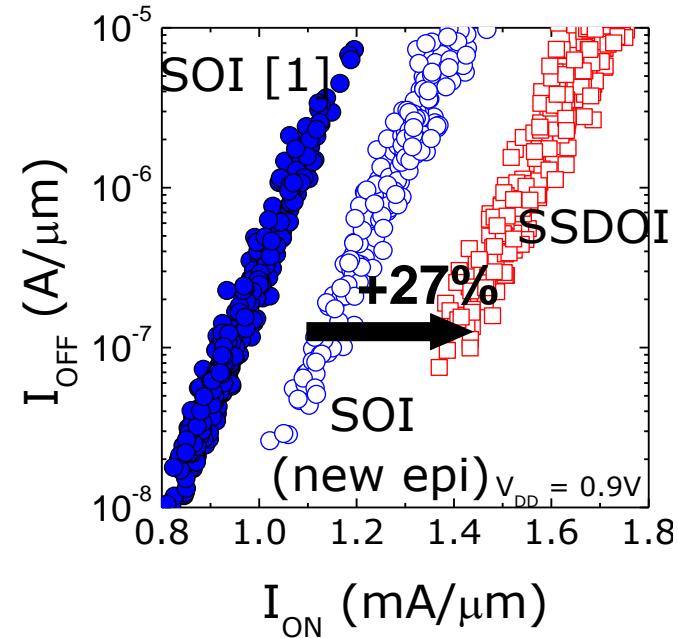
- sSOI (=SSDOI) wafers

- Tensilely strained Si :

- Enhanced electron  $\mu$ : sSOI improves nMOSFET perf. by 27%
    - Slightly reduced hole mobility



Leti: L. Hutin *et al.*, IEDM2010



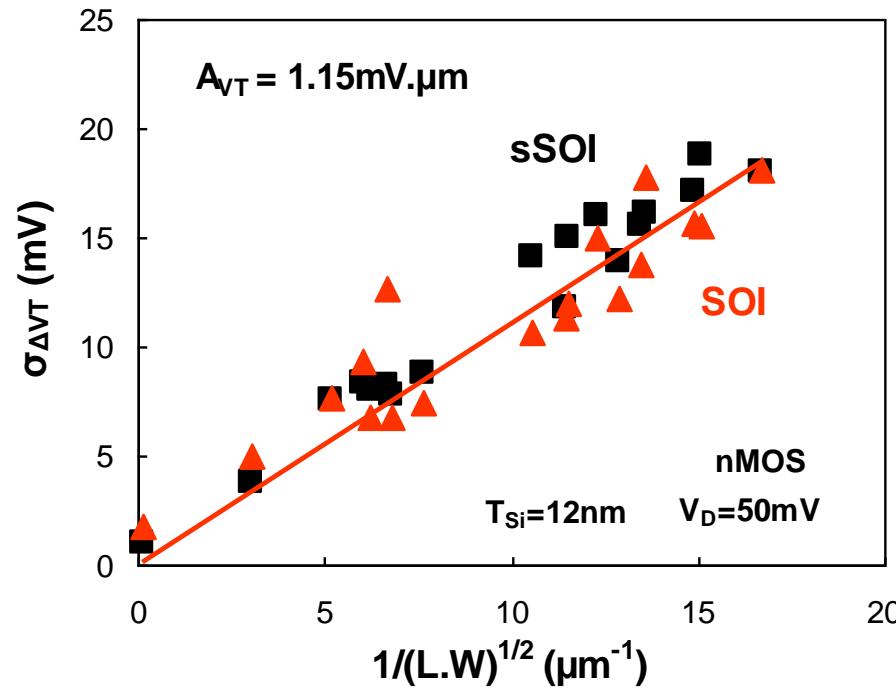
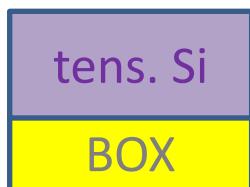
IBM: A. Khakifirooz *et al.*, VLSI tech. symp. 2012

# 10nm FDSOI: strain for $\mu$ boost

- sSOI wafers

- Tensilely strained Si :

- No variability degradation with sSOI (vs. SOI)

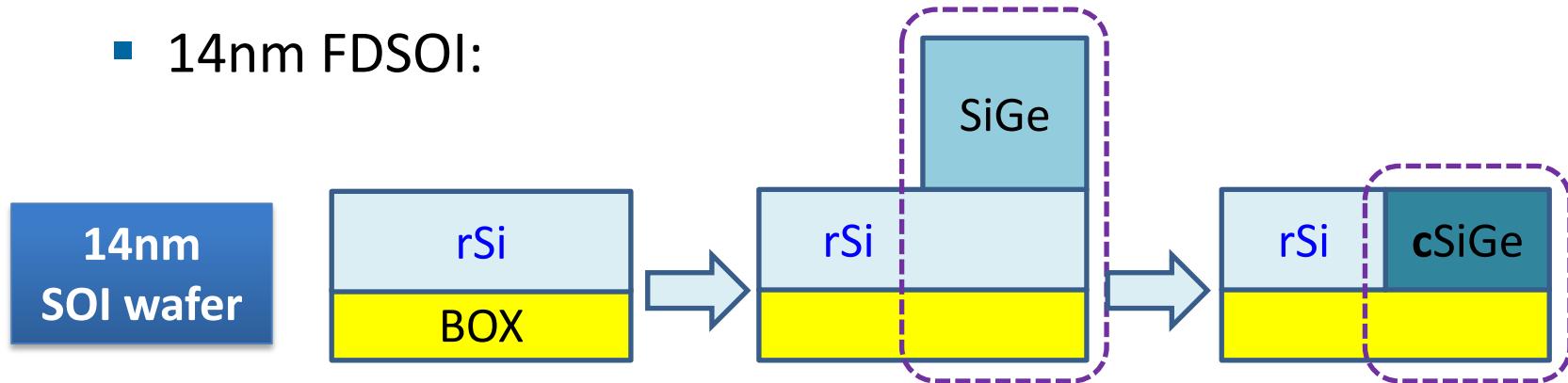


J. Mazurier et al., SOI conf. 2010

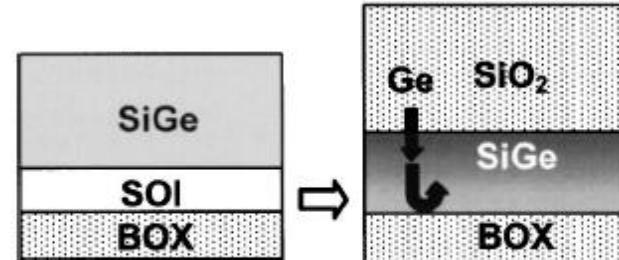
# 10nm FDSOI: strain for $\mu$ boost

- sSOI wafers: strained SGOI issue

- 14nm FDSOI:



The final SiGe film exhibits **compressive strain (& stress) corresponding to the lattice mismatch between SiGe and SOI**



From S. Nakaharai *et al.*, APL 83, p.3516 (2003)

Ge	Bi-axial strain	Bi-axial stress
	(%)	(GPa)
15%	-0.6	-1.09
25%	-1.03	-1.76
35%	-1.44	-2.4

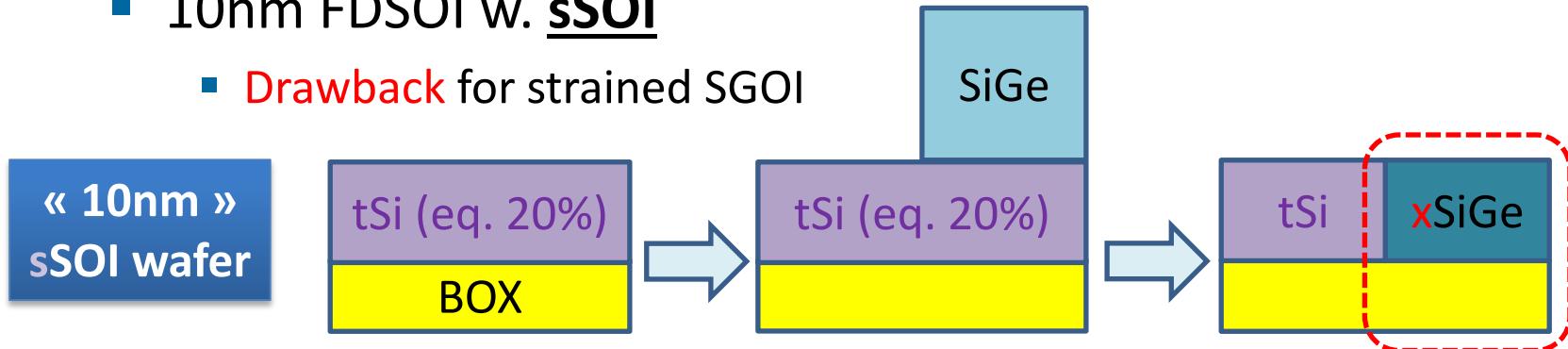
ST-IBM: Q. Liu *et al.*, IEDM 2013

# 10nm FDSOI: strain for $\mu$ boost

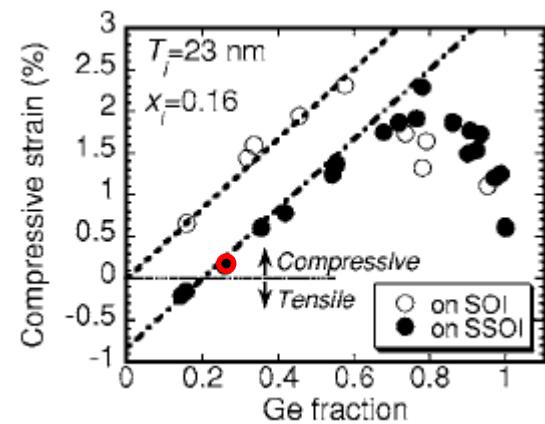
- sSOI wafers: strained SGOI issue

- 10nm FDSOI w. sSOI

- Drawback for strained SGOI



The strain in the final SiGe is **delayed** because of the tensilely strained Si (sSOI) lattice  
cq: **strain and  $\mu$  loss**



T. Tezuka *et al.*, APL 2003

# 10nm FDSOI: strain for $\mu$ boost

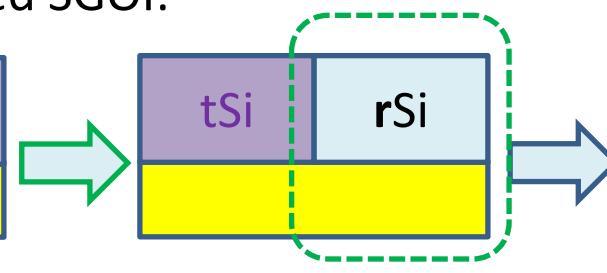
- sSOI wafers: strained SGOI issue

- 10nm FDSOI w. sSOI

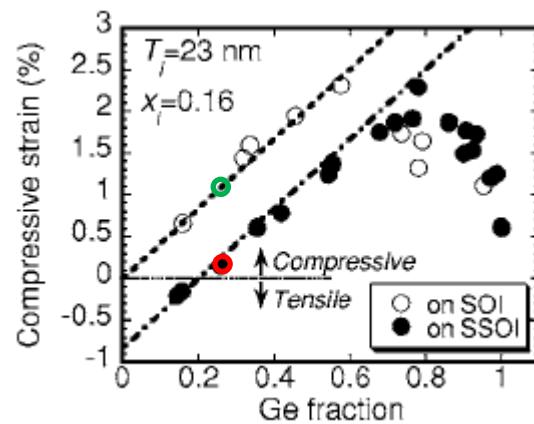
- Solution for strained SGOI:

10nm  
sSOI wafer

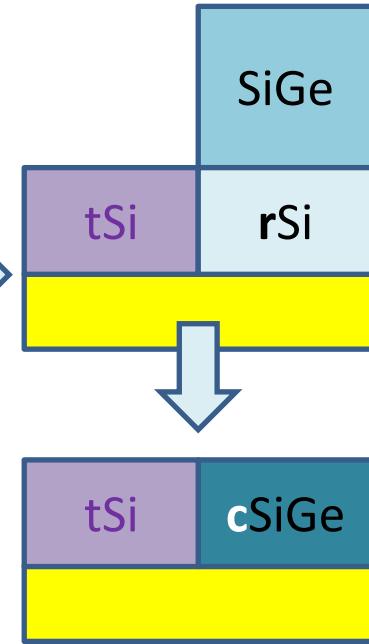
tSi (eq. 20%)  
BOX



Locally relax the tensile strain in the pMOSFET area (for efficient Ge enrichment)

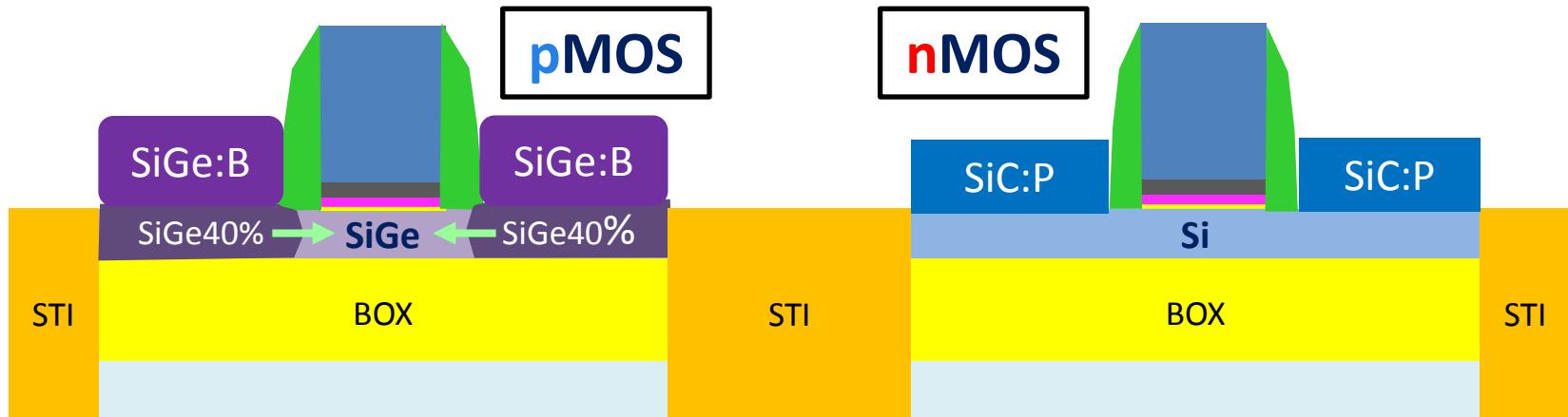


T. Tezuka *et al.*, APL 2003



# 10nm FDSOI: strain for $\mu$ boost

- **Self-Aligned In-Plane Stressors (SAIPS)**
  - Principle: Increase the Ge content in the SGOI film in the SD regions of pMOSFETs (before SD epi)



- Advantages:
  - Uniaxial compressive strain + high transmission efficiency
  - Self-aligned process
  - No modification of the channel itself

L. Grenouillet *et al.*, S3S conf 2013

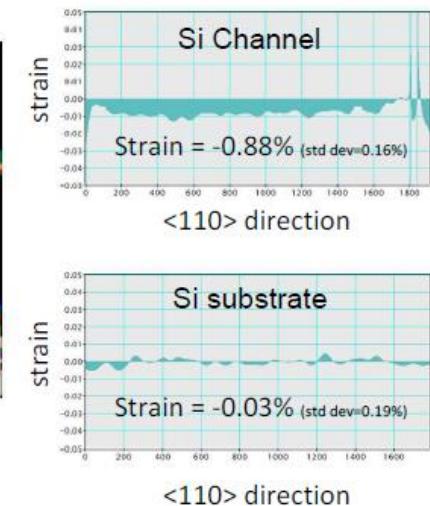
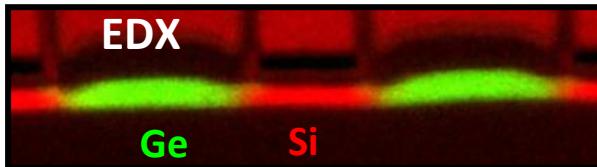
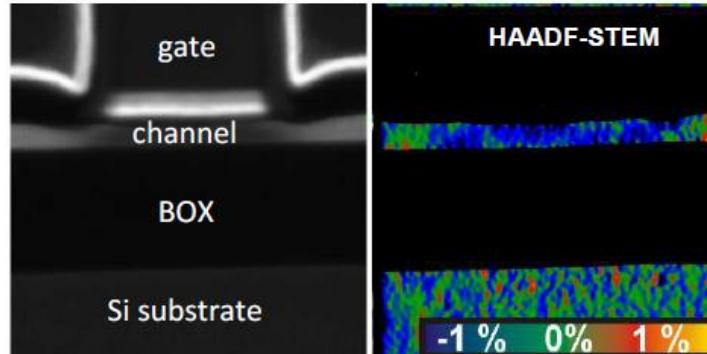
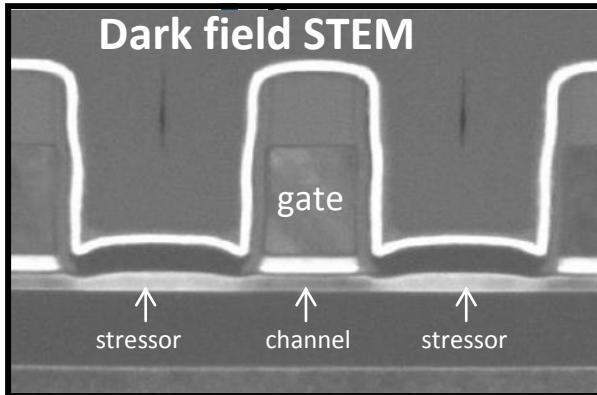
# 10nm FDSOI: strain for $\mu$ boost

## ■ Self-Aligned In-Plane Stressors (SAIPS)

- First morpho results: SOI case

- 1) Ge mapping

- 2) Strain mapping



- SAIPS induce an additional -0.9% compressive strain in the channel

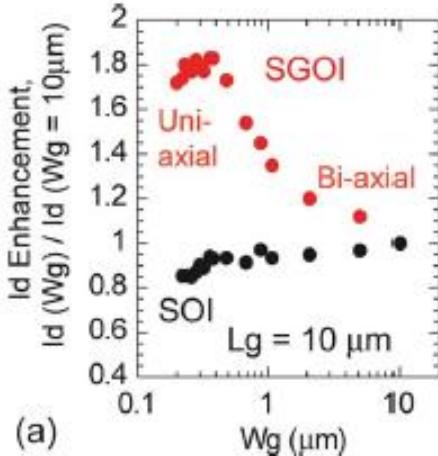
- 30% Ge content difference between channel and stressors

L. Grenouillet *et al.*, S3S conf 2013

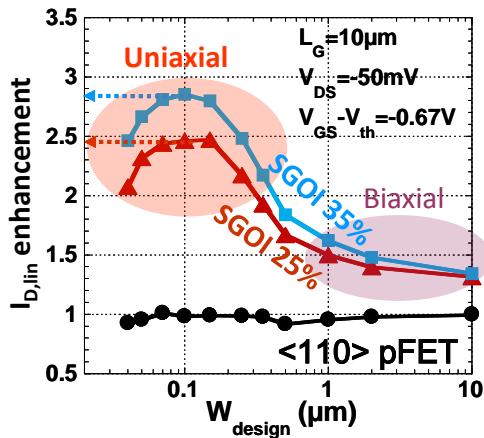
# 10nm FDSOI: strain for $\mu$ boost

## Slicing

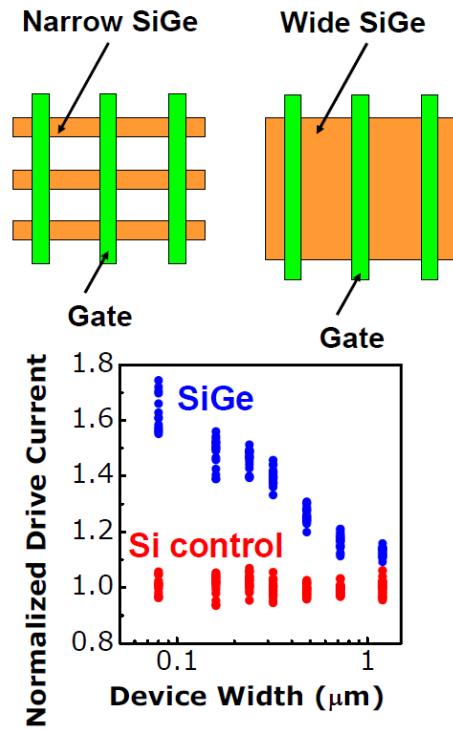
- Width effect:



MIRAI:  
S. Takagi *et al.*, IEEE TED 2008



leti:  
L. Hutin *et al.*, VLSI tech symp 2010



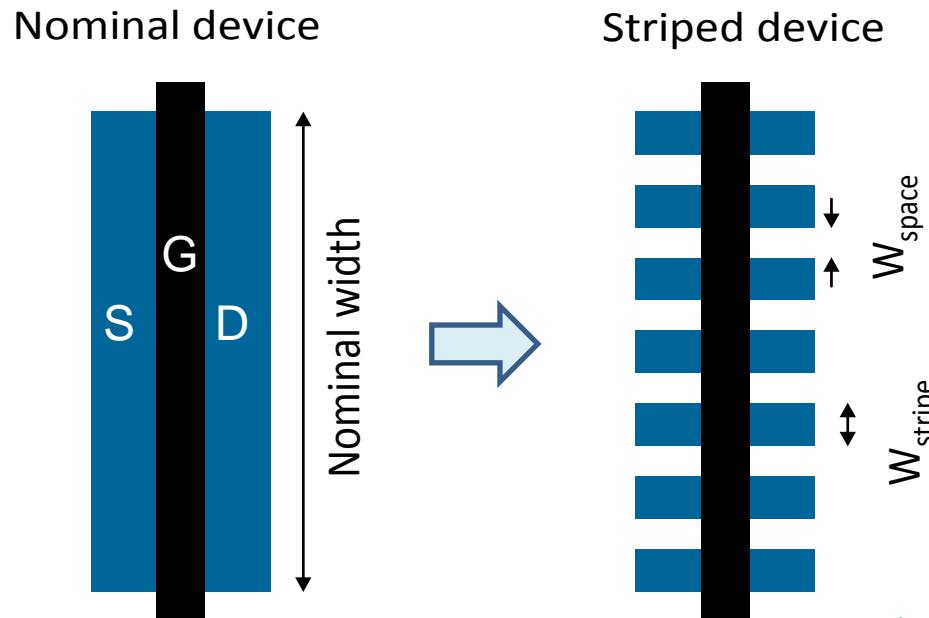
IBM:  
K. Cheng *et al.*, IEDM 2012

- Biaxial to uniaxial strain transition when width decreases
- FD cSiGe pMOSFET performance increase by >60%

# 10nm FDSOI: strain for $\mu$ boost

## Slicing: Cutting a nominal device into a striped device

- Current per active width increases 
- Effective active width decreases 
- Effective capacitance decreases 

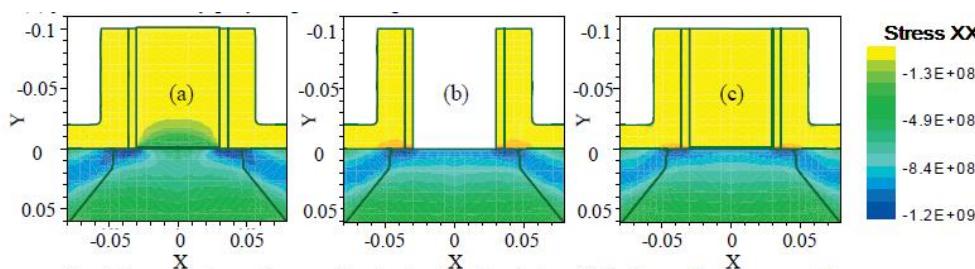


L. Grenouillet et al., S3S conf 2013

# 10nm FDSOI: strain for $\mu$ boost

## ▪ Gate Last

- Pursue the EOT scaling ... with a good reliability
  - Adjust the threshold voltage
  - Induce more strain in the channel
    - Dummy gate removal increases the stress from SiGe S-D
    - Bulk: Sony, Intel



Sony:  
J. Wang *et al.*,  
VLSI tech symp 2007

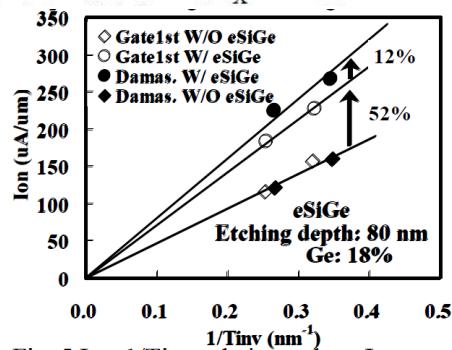


Fig. 5 Ion-1/Tinv relation, where Ions are extracted at  $I_{off} = 1\text{nA}/\mu\text{m}$  and  $V_d = V_\sigma = -10\text{V}$

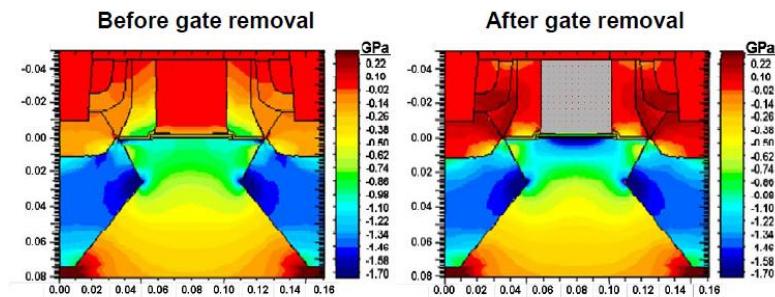
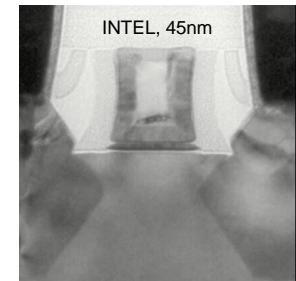


Fig. 7. Removal of poly gate increases channel stress by 50% [28].

Intel:  
C. Auth *et al.*,  
VLSI tech symp 2008



# What will scaled-FDSOI offer ...

... down to 10nm ?

## Performance

- Intrinsic gain in performance
- Back-bias: speed/power control

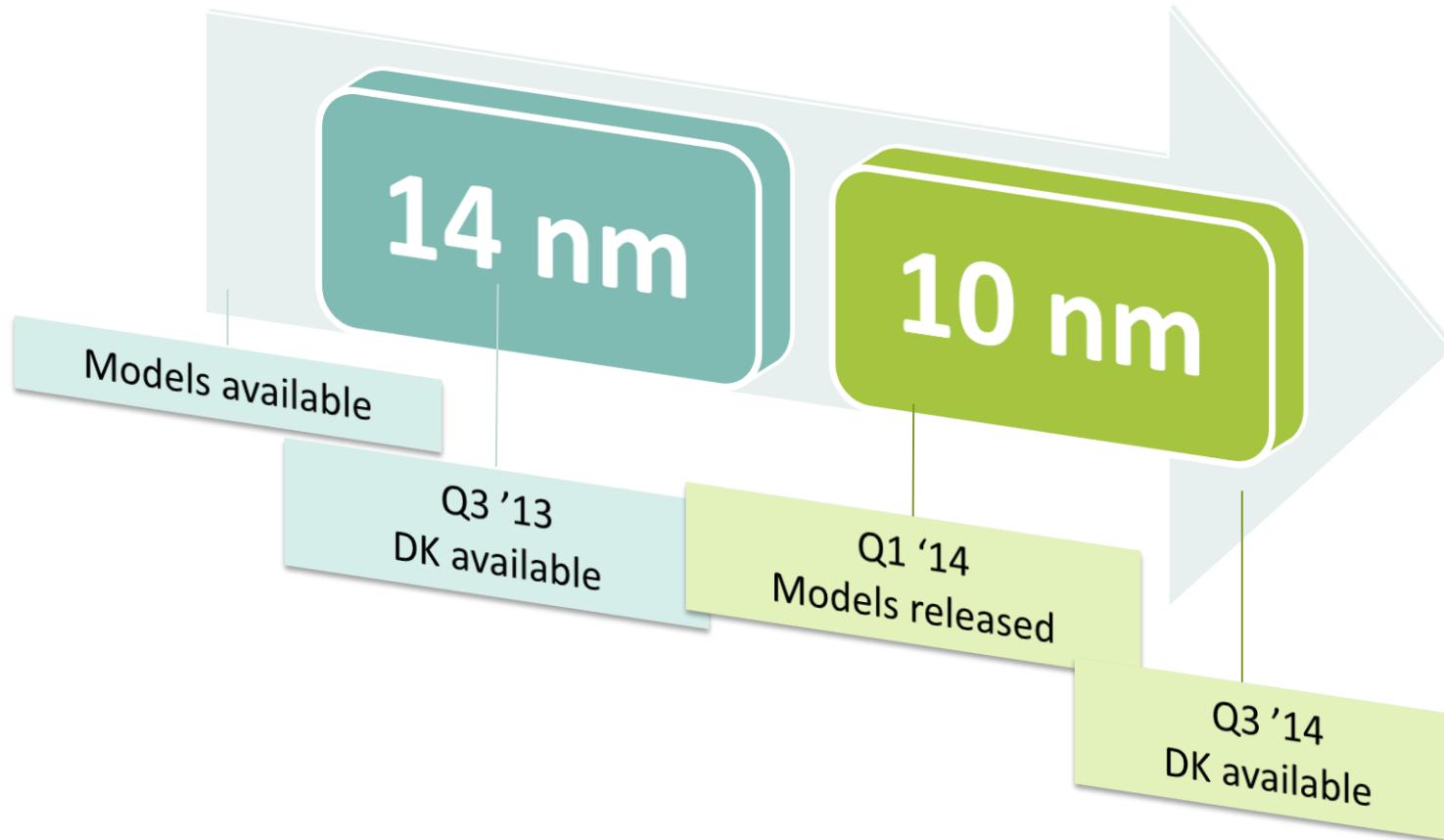
## Risk-contained design transition

- Soft design transition
- Low  $V_T$  dispersion
- Hybrid bulk/FDSOI for maximal IP re-use

## A cost- optimized silicon solution

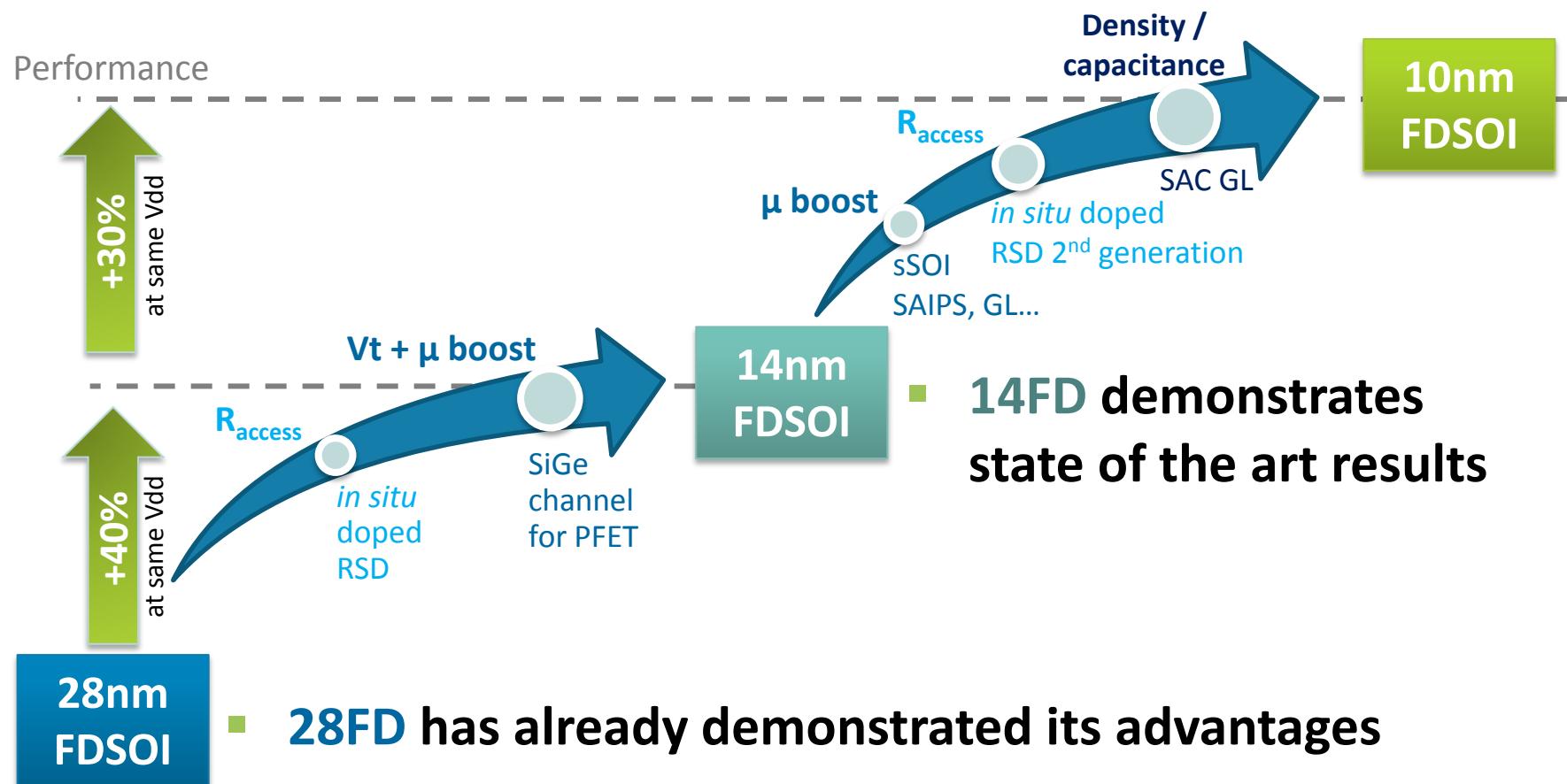
- A simple process (15% less step than 28LPM): positive impact on cost and yield

# When will scaled FDSOI deliver?



# FDSOI: conclusion

- Scaling enablers & perf. boosters identified to address the 10FD

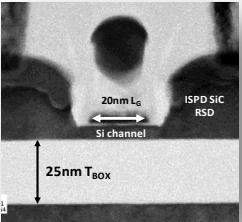


# Advanced CMOS roadmap

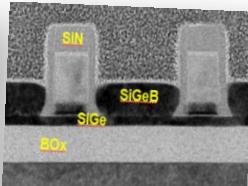
Early material and process coupling

Evolutionary scaling: technology driven performance improvement

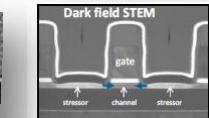
28FDSOI



14FDSOI

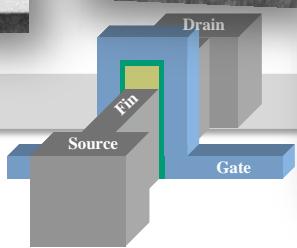


10FDSOI

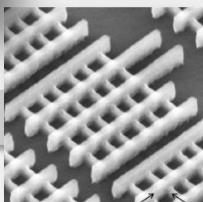


Non planar / trigate / stacked NW

FinFET

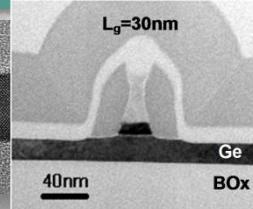
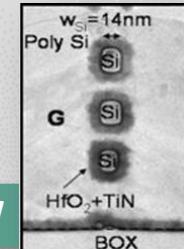


28nm



10nm

High mobility materials Ge and III-V

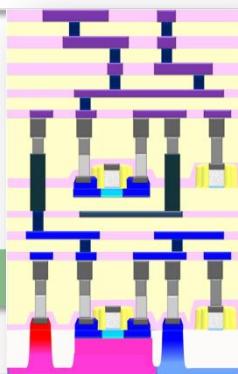


5nm

7nm

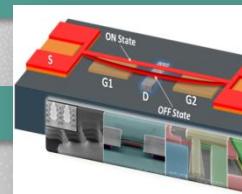
Alternative to scaling

Disruptive scaling

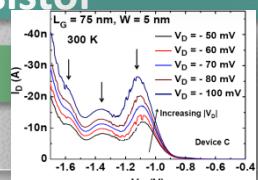


Steep slope devices

Mechanical switches



Single Electron Transistor



Monolithic3D – M3D

Early design coupling



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ET DE TECHNOLOGIES  
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## Thank you

