FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics

INVITED PAPER

FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics

Silicon-on-insulator devices designed for optimum operation at 0.3 V promise longer operational life than conventional application-specific integrated circuits.

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ABSTRACT | Ultralow-power electronics will expand the technological capability of handheld and wireless devices by dramatically improving battery life and portability. In addition to innovative low-power design techniques, a complementary process technology is required to enable the highest performance devices possible while maintaining extremely low power consumption. Transistors optimized for subthreshold operation at 0.3 V may achieve a 97% reduction in switching energy compared to conventional transistors. The process technology described in this article takes advantage of the capacitance and performance benefits of thin-body silicon-on-insulator devices, combined with a workfunction engineered mid-gap metal gate.

KEYWORDS | Low power; metal gate; silicon-on-insulator (SOI); subthreshold

I. INTRODUCTION

Ultralow-power (ULP) transistors are an enabling technology for many proposed applications. Ubiquitous sensor networks, RFID tags, implanted medical devices, portable biosensors, handheld devices, and space-based applications are among those which would benefit from extremely low power circuits [1]–[3]. ULP circuits could take advantage of new energy-harvesting devices which recharge batteries by scavenging power from motion or solar cells, such as a recently demonstrated wristwatch design requiring 50 nA of on-current at 0.42 V operation [4], [5]. In general, low standby power (LSTP) applications require less than 100 pA/μm leakage current, [5] while maximizing the on-current at a modest power supply voltage.

A recent study examined the impact of ULP techniques on a typical sensor system [6]. The analysis assumed ultralow-power digital electronics which consume 15–20$\times$ less energy per operation than conventional ASIC technology. With this assumption, the study showed it would be practical to build a sensor system that would have the same performance characteristics, but operate 4 times as long as would be possible using conventional ASIC digital logic. This paper will explore some of the methods that enable this longer operational lifetime without compromise to system performance.

Subthreshold operation transistors hold great promise for integration into ultralow-power designs, since the most efficient way to reduce power is to reduce the operating voltage [7]. With an operating voltage of 0.3 V, and an on-current of less than 1 μA/μm, subthreshold transistors use orders of magnitude less power than transistors operated in strong inversion. Subthreshold operation also provides the highest transconductance (g_m) for a given drain current [8]. In subthreshold, conduction is by diffusion rather than drift, which implies that the on-current is determined by subthreshold swing rather than mobility. Given similar subthreshold swing, it is possible to have equal NMOS and PMOS drive currents per unit of transistor width. This allows equal sizing of NMOS and PMOS transistors in contrast to the typical 2$\times$ wider PMOS transistor size for conventional devices, resulting in reduced circuit area and capacitance.

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Simply lowering the operating voltage of a conventional high-performance transistor will not produce very good device performance in subthreshold operation. Conventional transistors will have comparatively high off-state leakage and overlap capacitance, as well as poorer subthreshold slope and unequal NMOS and PMOS on-current. By designing a fabrication process from the substrate material through the interconnect metal, optimized for subthreshold transistor performance, it is possible to realize a device with the minimum switching energy and off-state current without significant impact to the energy-delay product. This paper will explore the advantages of SOI technology in ultralow-power applications, and detail the processing techniques which have been employed to optimize the devices for subthreshold operation.

II. BULK SILICON VERSUS SOI

Fig. 1(a) and (b) illustrates a schematic comparison of bulk silicon and SOI transistors. The benefits and disadvantages of SOI vs. bulk silicon technology have been discussed many times [2], [4], [9], [10]. Compared to bulk silicon, SOI provides up to 90% lower junction capacitance, near-ideal subthreshold swing, reduced device cross-talk, lower junction leakage, no latch-up, increased radiation hardness, and full dielectric isolation of the transistor. The low junction capacitance is extremely valuable to ultralow-power devices, as it allows reduction of the CV^2 switching energy of the transistor. Another significant advantage for low-power operation is that SOI devices do not suffer from substrate reverse bias effects, in that the depletion charge does not increase when a source potential is applied. Thin-body SOI also provides better electrostatic channel control, leading to reduced source-to-drain leakage and reduced short channel effects (SCE) [11]. In contrast, it has been suggested that bulk silicon is now facing GIDL limits with device scaling, making it inappropriate for ultralow-power applications [5].

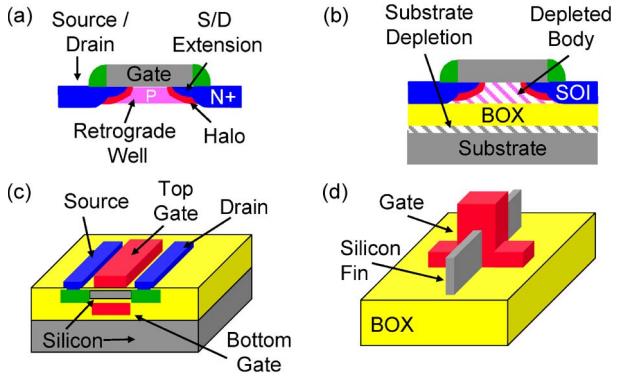

Fig. 1. *Transistor architectures: (a) bulk silicon, (b) partially depleted SOI, (c) double gate SOI, (d) FinFET. Adapted from Roy [11].*

SOI also provides significant advantages for extreme environment operation. At cryogenic temperatures, bulk silicon devices isolated by reverse-biased diodes can suffer from carrier freeze-out and increased crosstalk, to which SOI devices are not susceptible due to the full dielectric isolation. At high temperatures, thermally induced diode leakage is much smaller in SOI devices, due to the reduced junction area. In addition, impact ionization is more strongly balanced by thermal recombination [9]. Functional SOI transistor operation has been demonstrated at 4 K and 573 K [12], [13].

Perhaps the strongest drawbacks of SOI technology are the floating body effects. The body potential can shift over time based on the history of the transistor operation and the generation or recombination of carriers. This can cause shifts in threshold voltage, subthreshold swing, and kink-effect. Floating body effects can be minimized, though not eliminated, by using thinner silicon.

SOI technology can be fully depleted (FDSOI) or partially depleted (PDSOI). The depletion depth is given by

$$T_{\mathrm{dep}} = \sqrt{\frac{4\varepsilon\Phi_f}{qN_{\mathrm{ch}}}} \tag{1}$$

where $\Phi_f = kT \cdot \ln(N_{\mathrm{ch}}/N_{\mathrm{i}})/q$ is the Fermi potential, N_{ch} is the channel doping concentration, and N_{i} is the intrinsic carrier concentration [7]. When the depletion depth is larger than the physical silicon thickness, a neutral region no longer exists between the source and drain, and the silicon becomes fully depleted [4]. For a highly doped channel where $N_{\mathrm{ch}} = 1 \times 10^{18}$ cm^{-3}, $T_{\mathrm{dep}} = 32$ nm by (1).

FDSOI is more difficult to fabricate than PDSOI, as the silicon channel must be reduced to a very small and well-controlled thickness. Another disadvantage is that series resistance in thin FDSOI can be quite high [14]. Further, unlike a PDSOI device, the FDSOI device is very susceptible to charge in the buried oxide (BOX) layer, which can capacitively couple through the depleted silicon of the body, changing the front channel threshold voltage. However, FDSOI also has important advantages over PDSOI, such as higher g_m and reduction of floating body effects [4], [7], [14]. A comparison of PDSOI, FDSOI, and bulk silicon technologies is given in Table 1.

For subthreshold transistors, one of the most important FDSOI advantages is the near-ideal subthreshold swing. The drive current in the subthreshold regime is given by:

$$I_{\mathrm{sub}} = I_o \cdot 10^{\left([V_{\mathrm{gs}}+\eta V_{\mathrm{ds}}]/S\right)} \cdot \left(1 - e^{-V_{\mathrm{ds}}/U_{\mathrm{th}}}\right) \tag{2}$$

where I_o is a function of the transistor L and W, η is the DIBL factor, S is the subthreshold swing, and U_{th} is the thermal voltage [1]. Note that subthreshold transistor

Table 1 Comparison of Bulk, PDSOI, and FDSOI Transistors

Transistor Type	Bulk	PDSOI	FDSOI
Approximate Substrate Cost (300mm)	$300	$1000	$1000
Active Silicon Thickness (nm)	>1000	~100	<40
Subthreshold Swing (mV/dec)	>120	80-120	65-80
Junction Capacitance	High	Low	Low
Diode Leakage	High	Low	Low
V_t Sensitivity to Si Thickness	None	Medium	High
Extreme Environment Performance, (<4K or >300°C)	Poor	Good	Good
Series Resistance	Low	Medium	High
V_t Sensitivity to BOX Charge	None	Low	High
Transconductance	High	Medium	High
Kink Effect	None	High	Medium

performance is a strong function of η and S in (2), and will be very sensitive to short channel effects since both η and S increase as gate length decreases. BOX thickness can be varied to achieve a tradeoff between on-current and off-current; thinner BOX improves DIBL but degrades S [1].

The subthreshold I_{on}/I_{off} ratio is derived from (2) to be simply

$$I_{on}/I_{off} = 10^{V_{gs}/S} \tag{3}$$

thus S is a critical parameter for subthreshold operation. Simulations using the ATLAS device simulator predict that at low operating voltages ($V_{dd} = 0.3$ V), FDSOI devices still provide a superior subthreshold slope to bulk silicon devices, as shown in Fig. 2. Therefore an optimized ultralow-power process technology will benefit from the lower subthreshold swing and capacitance provided by FDSOI.

III. CHANNEL DOPING

The threshold voltage is a strong function of silicon film thickness when using FDSOI with highly doped channels.

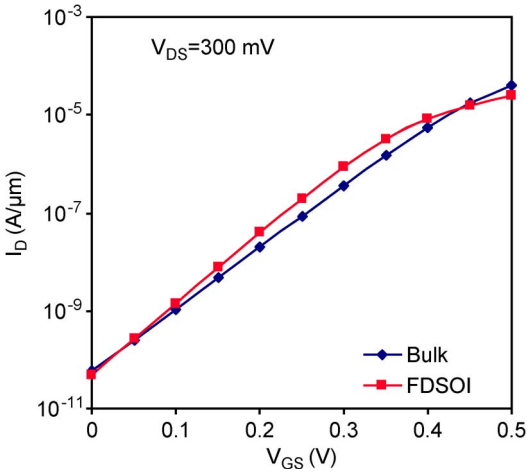

Fig. 2. *Simulation of ultralow-power transistors, for 65 nm gate length. FDSOI exhibits improved subthreshold slope and thus a 2.5× improvement in I_{on}/I_{off} ratio at 0.3 V operating voltage compared to bulk silicon.*

V_t changes by approximately 4 mV per 1 nm silicon thickness when the doping level is 1×10^{17} cm^{-3}, according to the data reproduced in Fig. 3 from Hsiao [15]. By comparison, when the channel doping is extremely low, below 5×10^{15} cm^{-3}, V_t is effectively independent of silicon film thickness. Since V_t control is critical for subthreshold transistors, it is highly desirable to use undoped (or more precisely, lightly doped) FDSOI, particularly for deeply scaled designs [14].

An undoped channel has additional benefits, including no V_t variation due to random dopant fluctuations, as well as higher carrier mobility. In addition, the depletion thickness given by (1) is large when the channel is undoped, which allows a more manufacturable silicon thickness to be used while maintaining the benefits of a FDSOI as opposed to a PDSOI device. Furthermore, low channel

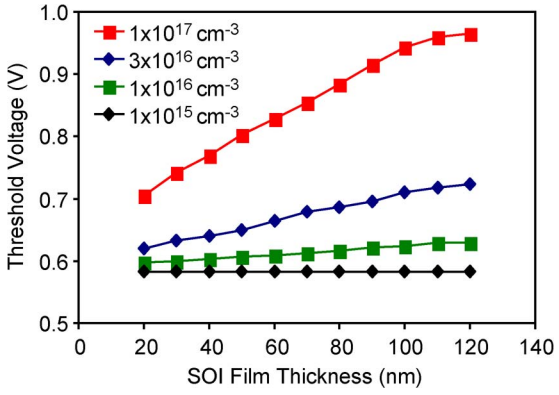

Fig. 3. *Threshold voltage as a function of silicon thickness and channel doping. Adapted from Hsiao [15].*

doping will reduce band-to-band tunneling and increase the S/D breakdown voltage, which could be important when integrating 3.3 V I/O transistors on the same chip as the subthreshold transistors [2], [14].

There are disadvantages to using an undoped channel as well. SCEs are more difficult to control without channel doping, though thin-body FDSOI is less sensitive to SCEs than bulk silicon devices [11]. Additionally, threshold voltage adjustments are more difficult without channel doping; this issue is discussed further in Section IV. Thus there are trade-offs involved with using undoped silicon channels, and it is likely that highly doped SOI will remain the standard for high-performance devices, whereas for ultralow-power devices the undoped channel advantages are compelling.

IV. GATE FABRICATION

When simplified to ignore back-channel effects, the threshold voltage of an SOI transistor is given by:

$$V_t = \Phi_{\mathrm{ms}} + 2\Phi_f - \frac{1}{C_{\mathrm{ox}}}\left(Q_{\mathrm{it}} + q\int_o^t \rho(x)dx - qN_{\mathrm{ch}}t_{\mathrm{soi}}\right) \quad (4)$$

where Φ_{ms} is the gate-to-semiconductor workfunction difference, C_{ox} is the gate dielectric capacitance, Q_{it} is the dielectric interface charge, $\rho(x)$ is the charge density in the dielectric, and t_{soi} is the silicon thickness. When N_{ch} is high, V_t is a sensitive function of t_{soi}, which is a drawback for thin FDSOI. However, when the channel is undoped, the Fermi potential and the depletion charge are approximately zero, and the expression for the threshold voltage becomes:

$$V_t = \Phi_{\mathrm{ms}} - \frac{Q_f}{C_{\mathrm{ox}}} \quad (5)$$

where Q_f is the total charge in the gate dielectric. Thus the threshold voltage of the transistor is essentially set by the gate workfunction.

Fig. 4 shows a graphical representation of (4), illustrating V_t as a function of N_{ch} for N^+ poly, P^+ poly, and mid-gap gates [10]. There are two solutions for achieving a threshold voltage of ~0.35 V, band-edge gate materials with high channel doping (1×10^{18} cm^{-3}), or a mid-gap gate material with very low channel doping (1×10^{15} cm^{-3}). As described in Section III, the undoped channel solution is preferred for subthreshold-optimized transistors.

Therefore, a workfunction-engineered mid-gap metal gate material [10], [16], [17] should be used to provide symmetric threshold voltages for NMOS and PMOS. There

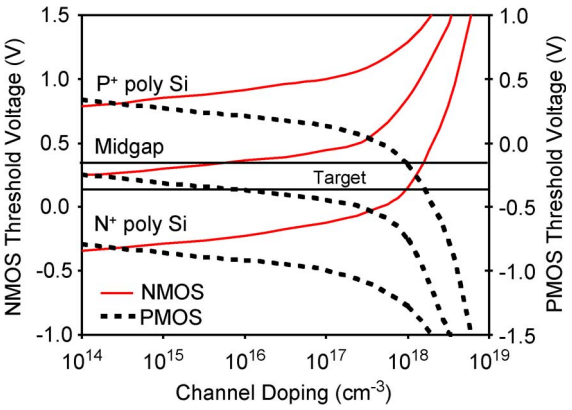

Fig. 4. *Threshold voltages of FDSOI NMOS and PMOS with mid-gap, N^+ poly, and P^+ poly gates as a function of SOI doping concentration. 10 nm-thick SOI and 5 nm-thick gate oxide are assumed. Adapted from Shimada [10].*

are several literature examples of successful integration of mid-gap metal gate transistors, including SiGe [15], Ta [10], [18], and TiN [19]–[26].

A metal gate stack typically consists of a thin metal layer sandwiched between a thicker polysilicon layer above, and the gate dielectric below. The gate dielectric may be a conventional SiO_2 or SiON gate oxide, or a high-k gate dielectric such as HfSiON. To prevent GOI issues, it is important that there is little diffusion of metal into the gate dielectric, or reaction between the metal and the dielectric. It is also important to minimize trapped charges in the gate dielectric (for example, during plasma sputtering of the metal gate material), which can shift the V_t of the transistor according to (4). Such charging effects have been noted after Ta gate deposition by Ar^+ sputtering, where an oxide charge density of 5×10^{11} cm^{-2} caused a 0.1 V shift in V_t [10].

TiN is a suitable mid-gap metal, with the advantage of being an accepted CMOS-compatible material. To evaluate the integration of TiN as a mid-gap metal gate material, capacitors were fabricated using 4 nm-thick SiO_2, 20 nm-thick TiN, and 200 nm-thick polysilicon. The capacitors were then phosphorous doped and capped with 250 nm-thick Al. Fig. 5 shows C–V curves comparing poly and two TiN gates with different N_2 flow rates during TiN PVD. The curves are fit with a quantum-corrected capacitor model from NCSU [27] to extract workfunction, equivalent oxide thickness (EOT), and other parameters. The workfunction of the TiN gates increases toward mid-gap compared to the N^+ poly gates, with $\Phi_m = 4.45$ eV and 4.60 eV for 100% N_2 flow and 66% N_2 flow (balance Ar) during TiN deposition. To increase Φ_m further, several postdeposition TiN anneal experiments were performed. A subatmospheric 626 °C N_2 anneal after TiN deposition increases Φ_m by 0.10–0.15 eV (Fig. 6), enabling tuning of the effective workfunction across the mid-gap range [28].

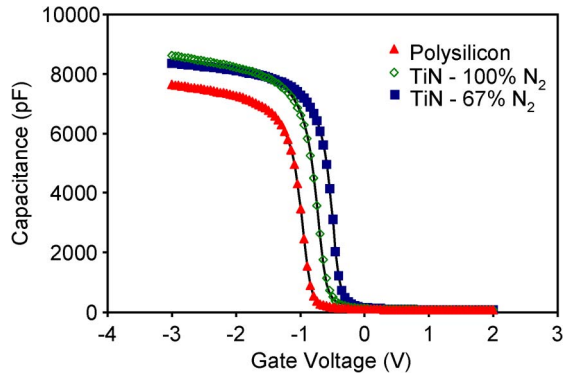

Fig. 5. *C–V curves of 1 mm² MOS capacitors, for TiN metal gates under two different TiN deposition conditions, and a polysilicon gate. TiN gates clearly show an increase in flatband voltage, and thus ϕ_{ms}, toward the silicon mid-gap. Metal gates also show increased accumulation capacitance due to elimination of poly depletion. Lines are quantum-corrected model fit to the data.*

Etching the TiN gate metal without damaging the polysilicon above the TiN or the gate dielectric below requires a delicate balance of plasma processing conditions. Lateral etching or notching of the overlying polysilicon could lead to undesirable penetration of implant species into the active channel beneath the gate, causing severe SCEs. Notching of the metal gate may lead to similar implant issues, as well as delamination of the narrower gates. A large foot on the metal must be avoided, as this will cause an undesirable increase in C_{gd}. Plasma etching selectivity to the underlying gate dielectric material is crucial, as punch-through of the gate dielectric will cause severe leakage or complete failure of the thin SOI device. Microloading effects must be minimized, to ensure that both dense and isolated gates have similar critical dimension (CD) and profile, in order to reduce variation in the transistor parametrics across the chip.

V. SPACER OPTIMIZATION

Eliminating the S/D extension implants (LDD implants) and increasing the spacer thickness results in a gate-to-S/D underlap which provides several benefits for ultralow-power operation. Most importantly, reduced overlap capacitance will allow lower CV^2 switching energy. In addition, increased spacer thickness will reduce subthreshold leakage, gate leakage, and DIBL. Simulations have shown that an optimized underlap can yield a 70% reduction in SRAM cell leakage and 200× lower cell read failure probability [11]. Since channel hot carrier (CHC) effects are not significant at low V_{dd}, the LDD implants are not required to maintain device reliability. Note that gate-to-S/D underlap can improve performance for FDSOI transistors as described above, whereas for conventional bulk silicon transistors the subthreshold slope would degrade significantly as the underlap increases.

The simulations of NMOS and PMOS $I_d - V_g$ curves for a ULP device at various gate-to-S/D underlap distances shown in Fig. 7 demonstrate that for $L_g = 150$ nm an optimized subthreshold slope and off-current occur for a 60 nm underlap. There have been some limited simulations of underlapped designs for shorter gate lengths. The optimum underlap for a FinFET with $L_g = 20$ nm was shown to be about 12 nm [29]. For a planar double-gate SOI design with $L_g = 16$ nm, subthreshold slope improves as the underlap increases to 16 nm [30]. Though the "optimum" underlap depends on which performance parameters one is trying to optimize, the above studies suggest the gate-to-S/D underlap should be approximately 0.5 to 1 times the gate length. Connelly has also described the use of an underlapped S/D technology for ultralow-power FDSOI, though in that case the underlap was only 4–9 nm [31]. That work also proposed the use of Schottky S/D to reduce the parasitic resistance of thin-body SOI.

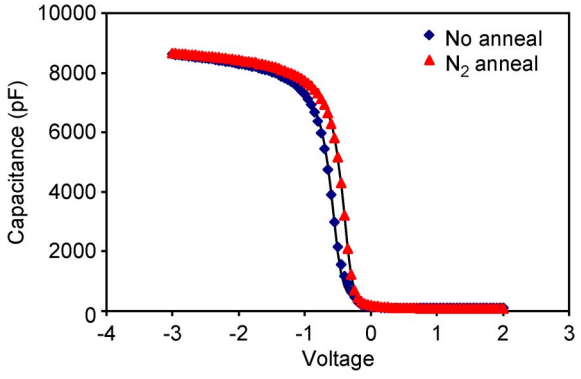

Fig. 6. *C–V curves of 1 mm² MOS capacitors, for TiN metal gates with and without 626 °C N_2 anneal. Anneal shifts metal gate workfunction by 100 meV toward silicon mid-gap. Solid lines are quantum-corrected model fit to the data.*

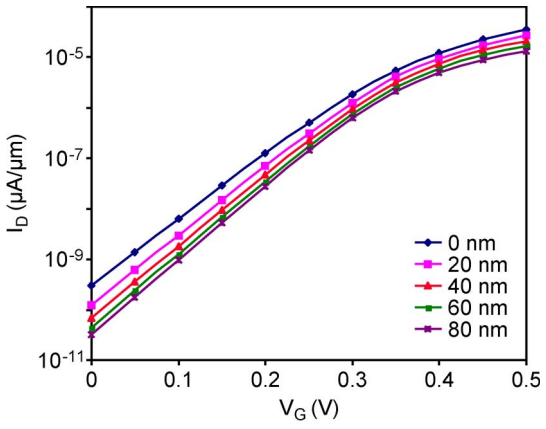

Fig. 7. *Simulated NMOS transistor I–V characteristics for 150 nm gate length ULP device, as a function of the S/D to gate underlap distance ($V_{dd} = 0.3$ V). Subthreshold swing decreases from 79 mV/decade at 0 nm underlap to 69 mV/decade at 80 nm underlap.*

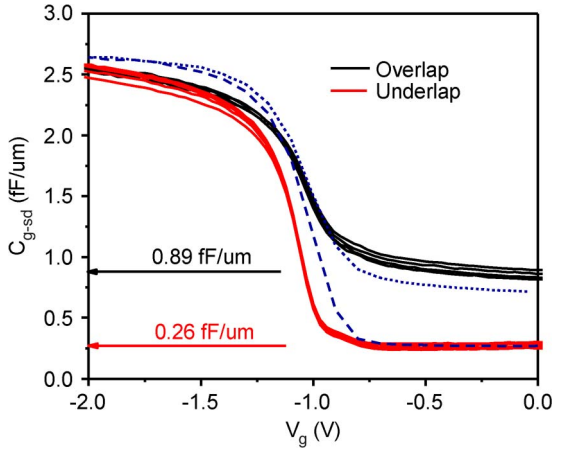

Fig. 8. *Comparison of total gate-to-S/D overlap capacitance ($C_{gd} + C_{gs}$) of conventional and ULP transistor designs, on 180 nm ($W = 100$ μm) PMOS transistors. Solid lines: measured data, dashed lines: ATLAS model simulation. ULP underlap design reduces capacitance by 71% compared to the standard overlap transistor design, with good agreement to device simulation.*

Fig. 8 compares experimental C–V curves from conventional devices and subthreshold-optimized devices with a 60 nm gate-to-S/D underlap. The capacitance for the underlapped devices is reduced by 71%.

Because of the gate-to-S/D underlap, there is a relatively wide region between the source and the gate which is not effectively controlled by the gate voltage. Carriers must diffuse through this region before they reach the channel under gate control. Simulations provided in Fig. 9 predict that as the doping level in the underlap region (and under the gate) increases above 1×10^{16} cm^{-3}, the drive current collapses. The underlap region becomes a high and wide barrier on the source side as body doping increases, and

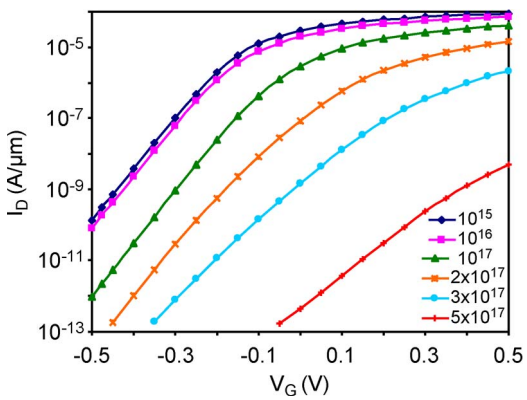

Fig. 9. *Model NMOS transistor I–V characteristics for 150 nm polysilicon gate ULP FDSOI device with 60 nm of gate-to-S/D underlap, as a function of body doping (atoms/cm^3). $V_{dd} = 0.3$ V. Increasing body doping causes a strong decrease in drive current due to the high and wide barrier in the source side underlap region.*

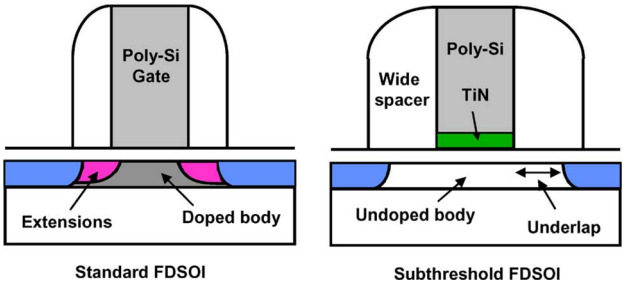

Fig. 10. *Schematic of standard FDSOI and subthreshold-optimized ultralow-power (ULP) FDSOI transistors.*

fewer carriers have the energy to tunnel through the barrier into the channel. Thus when a wide underlap is employed, the body doping must be kept very light. Fortunately, this is consistent with using a single mid-gap metal gate to set the threshold voltage.

To summarize, a schematic comparison between conventional and subthreshold-optimized ultralow-power transistors is shown in Fig. 10, illustrating the undoped body, elimination of S/D extension implants, and wide spacers.

VI. INTERCONNECT OPTIMIZATION

The current through the interconnect routing will be relatively small for ultralow-power circuits, and the standard interconnect metallization will be significantly oversized. At low current densities, electromigration is not a serious issue, nor is ohmic heating. It is therefore possible to reduce the capacitance of the circuit further by reducing the thickness of the interconnect metal. The increased interconnect resistance is not significant, since the resistance of the thin body transistor will be much larger than that of the interconnect.

Though the maximum possible reduction in interconnect thickness will depend on the details of the individual circuit design, a 50% reduction is conservative for most cases. ATLAS device simulations have been performed on a transistor driving a given length of interconnect to calculate the resistance and capacitance of the device. Due to the 60 nm underlap, the resistance of the FDSOI ultralow-power transistor is 114 times higher than that of a conventional bulk silicon transistor with no underlap. The capacitance, however, is decreased by 78%.

The characteristic switching time of the device is given by:

$$t_c = (R_t + R_i) \cdot (C_t + C_i) \tag{6}$$

where t and i indicate the transistor and the interconnect lines, respectively. The simulation results are given in

Table 2 ULP Transistor Simulation Results

Device Design	V_{dd}	Switching time (ps)	Switching energy (fJ)	Energy-delay product (fJ•ps)
Conventional Bulk Si + Conventional Metal	1.2	11	2.59	28
ULP Bulk Si + Conventional Metal	0.3	2750	0.23	641
ULP Bulk Si + ULP Metal	0.3	2211	0.21	458
ULP FDSOI + Conventional Metal	0.3	308	0.11	34
ULP FDSOI + ULP Metal	0.3	176	0.07	12

Table 2. A 50% reduction in interconnect metal thickness (designated ULP Metal) reduces t_c by 40%. The simulation predicts that the total CV^2 switching energy of the optimized FDSOI ultralow-power device is reduced by 97% compared to a traditional 1.2 V transistor. This exceeds the requirement for the 20× power reduction called for in Section I to enable the sensor application.

VII. SUBTHRESHOLD OPTIMIZED TRANSISTOR PERFORMANCE

FDSOI ultralow-power transistors were fabricated with the integration optimized for subthreshold operation as outlined above. NMOS and PMOS I_d–V_g characteristics are shown in Fig. 11, for mid-gap metal gate transistors with $L_g = 150$ nm and $W = 8$ μm. Nitride spacer thickness is 90 nm, yielding a 60 nm gate-to-S/D underlap after an 8 s, 1022 °C activation anneal. The TiN gate workfunction tuning provides closely matched NMOS and

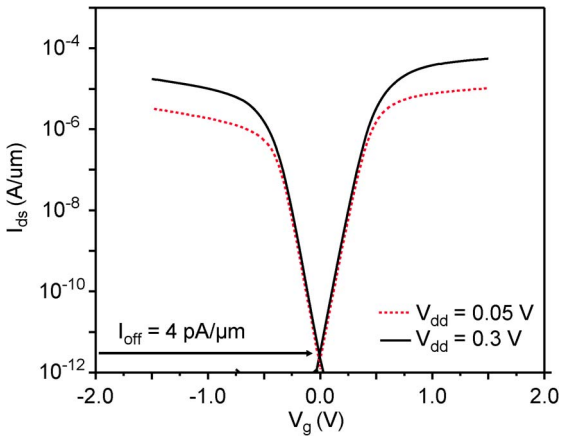

Fig. 11. *Representative ULP transistor I-V curves with a 150 nm TiN metal gate ($W = 8$ μm). The devices show very good subthreshold performance, and nearly ideal workfunction tuning.*

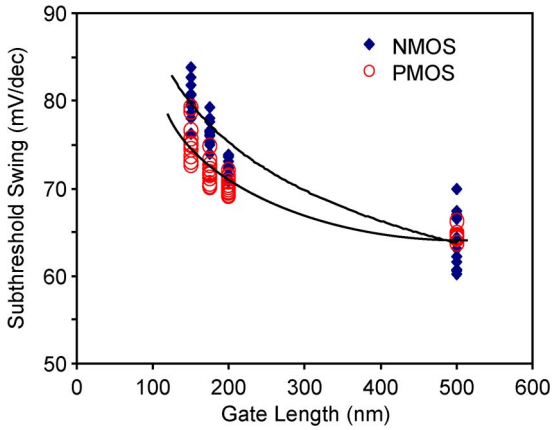

Fig. 12. *Subthreshold swing for 12 NMOS and 12 PMOS mid-gap metal gate transistors at 4 gate lengths, on a single wafer. S is near ideal at 64 mV/dec for 500 nm gates, but increases due to SCEs. $V_{dd} = 0.3$ V, $W = 8$ μm.*

PMOS $I_{on}(V_g = +/-0.3\ \text{V})$ and $I_{off}(V_g = 0\ \text{V})$ performance. It has been proposed that a suitable leakage limit for ultralow-power handheld electronics is 20–50 pA/μm, [5] which is well above the 4 pA/μm off-current of these FDSOI subthreshold-optimized transistors.

The subthreshold swing (S) for the fabricated mid-gap gate ultralow-power transistors is shown in Fig. 12 as a function of gate length. For long-channel devices ($L_g =$ 500 nm) S is nearly ideal at 64 mV/decade. As the gate length decreases, S increases to 80 mV/decade due to SCE. The subthreshold swing is lower for PMOS than for NMOS due to the difference in effective channel length for these underlapped devices; under the current process conditions, the NMOS phosphorus implant apparently diffuses farther than the boron PMOS implant, resulting in a shorter NMOS channel for a given gate length.

VIII. MANUFACTURABILITY AND FUTURE DIRECTIONS

SOI-based CMOS is commonly used today in high performance applications, such as gaming consoles (Wii, Xbox, PS3) [5]. However low-power applications are generally more cost sensitive than are high-performance applications, which has put the more expensive SOI starting material at a disadvantage. The process optimizations outlined in this paper help to minimize cost as well as provide enhanced ultralow-power performance. Using undoped channels with no LDD implants will eliminate four or more mask levels from the process. A single mid-gap metal gate transistor requires many fewer processing steps than a dual band-edge metal gate design. Further, gate-first processing is also much less costly than gate-last (fully silicided or damascene gate) processing. Aside from thinning the silicon thickness to 40 nm or less, there are few

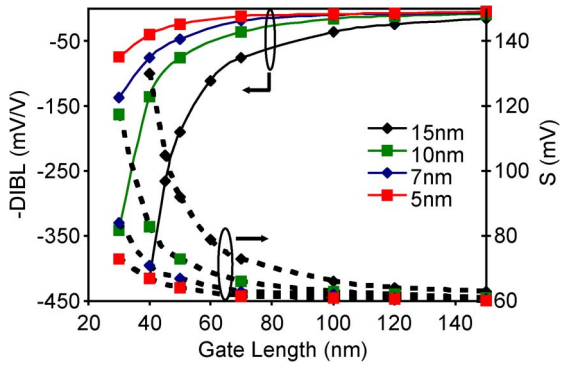

Fig. 13. ***Quasi-2-D estimates of S and DIBL in FDSOI MOSFETs as a function of L_g for t_{Si} = 15, 10, 7, and 5 nm. As t_{Si} is reduced, both DIBL and S decrease significantly at shorter gate lengths. Adapted from Trivedi [14].***

additional processing challenges associated with fabricating SOI devices compared to bulk silicon devices. FDSOI transistors are susceptible to V_t shifts due to trapped charge in the buried oxide layer, and they can show kink effect at high currents. However ultralow-power designs by definition are low current, and thus will not show significant kink effects.

Scaling gate length while maintaining reliable device performance is as challenging for ultralow-power transistor design as it is for high-performance transistors. For gate lengths below 100 nm, SCEs will increase DIBL and subthreshold swing unless the silicon channel thickness is also scaled. Fig. 13 is reproduced from Trivedi [12], showing that t_{Si} will have to be reduced to ultra-thin values below 15 nm to prevent leakage current from increasing. Though ultra-thin SOI devices have been fabricated for several research publications, the technology has not yet been demonstrated in a manufacturable way across 300 mm wafers.

At very thin silicon thicknesses, quantization effects have significant effects and V_t is again a function of t_{Si}. Mobility is also degraded, due to higher phonon and surface scattering. If a practical silicon thickness limit of 5 nm is assumed, the minimum gate length which allows acceptable ultralow-power performance is 25–30 nm [14].

Beyond this limit, nonplanar devices with enhanced channel control may be required. Fig. 1(b)–(d) compare several transistor technologies: SOI, double gate SOI, and FinFET. Double or triple gate designs can provide improved channel control, lower leakage, and improved SCEs [11]. Further, it has been shown that a mid-gap double gate will have lower subthreshold leakage and gate leakage than designs with band-edge gates [11]. However, the high cost associated with increased process integration complexity makes them less desirable for ultralow-power electronics at the present time. This may change if FinFETs or other multiple gate transistor designs become mainstream technology at the 22 nm-node or below.

IX. CONCLUSION

Widespread adoption of SOI technology will require significant performance advantages over bulk silicon to justify the higher cost of the SOI substrate, the additional processing steps associated with thinning and control of the active silicon thickness, and the development of infrastructure to support design kits, EDAs, and standard cell libraries. The processing technology for subthreshold-optimized transistors described in this paper has enabled the verification of several performance advantages of ultralow-power FDSOI devices. By designing the transistor from the substrate through the interconnect levels for subthreshold operation, the switching energy of the device is decreased by 97% with modest impact to the energy-delay product. ■

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