TÉCNICO LISBOA

Laboratory 3: AC/DC Converter

Msc. Aerospace Engineering, Técnico, University of Lisbon

Circuit Theory and Electronics Fundamentals

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Autores

Francisco Dores, 95790
Simão Martins, 95845
Tiago Pratas, 95848

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1 Introduction

The goal of this laboratory assignment is to model and analyse an AC/DC converter circuit, by designing both Envelop Detector and Voltage Regulator circuits.

It was chosen a full-wave bridge rectifier circuit, using 4 diodes, $D_{i=1,2,3,4}$. Furthermore, it was used 1 diode, D_e, 2 resistors, R_e and R_v, a capacitor, C, and 17 aditional diodes. The circuit described is portrayed in Figure-1.

Throughout the report it is presented a theoretical analysis, a simulation of the circuit and its analysis as well as a comparison of the obtained results.

In Section **??**, it is executed an incremental analysis by separating the AC and DC components, in order to do a theoretical analysis of the circuit, using the Octave maths tool. In Section 2, it is executed an analysis of the circuit using the Ngspice tool to simulate it. In Section 3, reults obtained with both Octave and Ngspice are displayed side-by-side, in order to compare the results. Lastly, in Section 4, it is performed a conclusion, bearing in mind the results from both the theoretical analysis and the simulation, from Section **??** and Section 2, respectively.

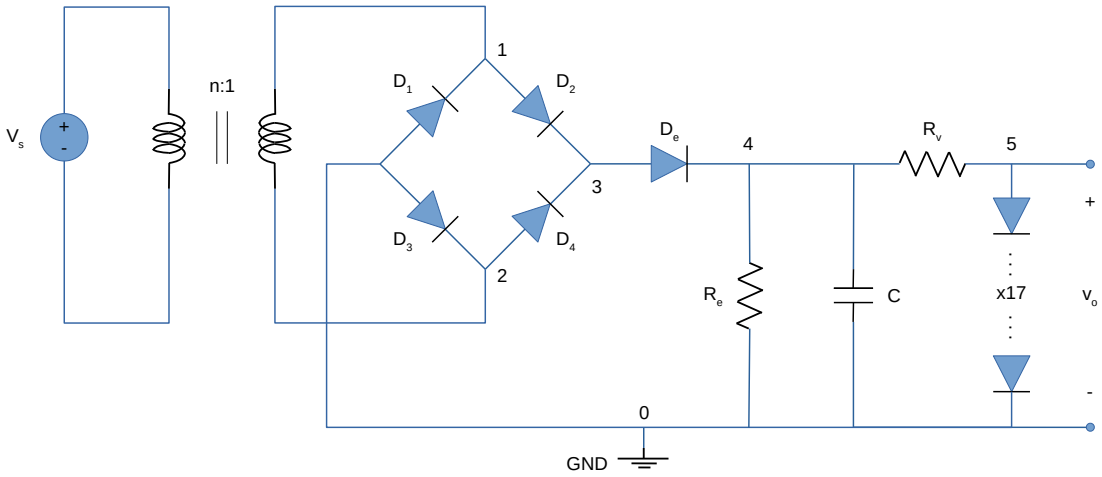

Figure 1: Circuit

2 Simulation Analysis

2.1 AC/DC Converter Simulation

In this section we simulate an AC/DC COnverter for 10 periods. It is our goal to understand how the values of each component affects the precision and the quality of the output voltage. This circuit transforms a variable voltage into a voltage with a DC component as closest as one can get to the pretended value, reducing, at the same time, the oscilation around that value.

Important note: Beyond modelling and analysing the circuit provided, one of the goals of this laboratory assignment is to maximize the merit, which is computed according to the following formula:

$$M = \frac{1}{\text{cost} * [\text{ripple}(v_0) + \text{average}(v_0 - 12) + 10^{-6}]} \tag{1}$$

Therefore, it was our intention to obtain the best value for this parameter,using each of the variables in order to maximize it, wich means that we have not tried to improve each of those separately, but as a all. In order to do it we used the values indicated in the begginig of Section **??** which resulted in the merit value bellow:

Merit	**Value**
1/(((950300)/1000+(920e-6)/1e-6+(22)*0.1)*(maximum(v(5))-minimum(v(5))+abs(mean(v(5))-12)+10e-6))	2.178736e+00

Table 1: Merit Calculation

2.2 Output Voltage Level and Ripple

In order to measure the output voltage level, we have used Ngspice's *average* function to determine its mean value. Beyond that it was from our interest to determine the ripple on the voltage. To do it, we have used Ngspice's *max* and *min* functions, which have allowed us to compute the amplitude of the oscilation. Beyond this, we also computed the V_{ON} value used by Ngspice's diode model. The results obtained are shown in the tables bellow:

Variable	**Value [V]**
maximum(v(5))-minimum(v(5))	1.597796e-04
mean(v(5))	1.199992e+01

Table 2: Output Voltage Level, Ripple in Volts[V]

V_{ON}	**Value [V]**
mean(v(5))/17	7.058779e-01

Table 3: V_{ON} in Volts[V]

2.3 Envelope Detector and Voltage Regulator - Output Voltages and Ripple

In this section, it is presented the plots regarding both envelope detector and voltage regulator output voltages and ripple. The values for each one of this 'subcircuits' are shown in the following tables:

Variable	**Value [V]**
maximum(v(4))-minimum(v(4))	7.852210e-02
mean(v(4))	2.276490e+02

Table 4: Envelope Detector - Output Voltage and Ripple in Volts[V]

Variable	**Value [V]**
maximum(v(5))-minimum(v(5))	1.597796e-04
mean(v(5))	1.199992e+01

Table 5: Voltage Regulator - Output Voltage and Ripple in Volts[V]

Next, we present the plot regarding the results obtained:

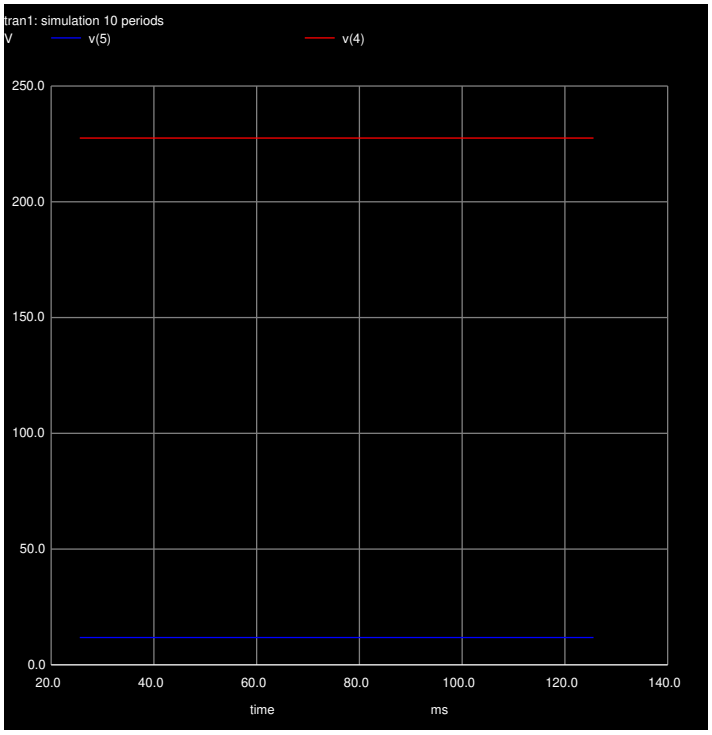

Figure 2: Total solution of the voltage source and the capacitor

As one can conclude from the plot analysis, the ripple suffers a significant reduction from the envelope detector to the the voltage regulator. This last circuit has the same output voltage as the ac/dc converter as a all. That is why table 5 is equal to table 2 in Subsection 2.1.

2.4 Final Result

As mentioned in Subsection 2.1 our goal is to obtain a voltage as stable as possible as well as closest as possible to 12V. Therefore, in this subsection we present a plot where the difference beetwen the output voltage and the pretended result is shown.

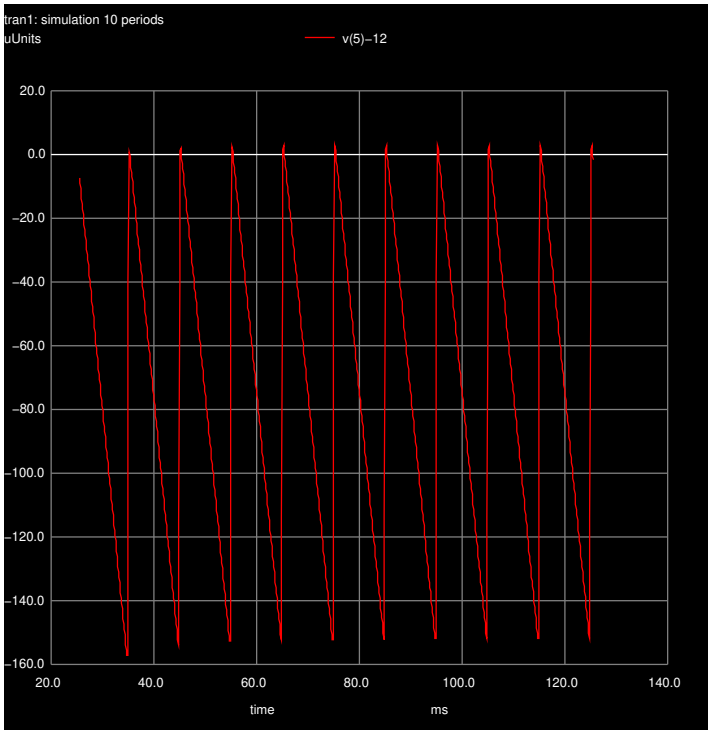

Figure 3: Total solution of the voltage source and the capacitor

As one can see, we were able to complete this laboratory objective, since we ended up with a voltage which as a DC component really close to 12V and with a minimum AC component.

3 Comparison between Octave and Ngspice results

Table 6 shows, on the left, the ripple voltage and the average output voltage of the evelope detector, which corresponds to the voltage on node 4, found by Octave, and, on the right, the same variables, but with the simulation results, by Ngspice, all for the circuit under analysis.

Name	**Value [V]**
$Ripple_{envelope}$	0.002240
$Average_{envelope}$	22.498882

Name	**Value [V]**
maximum(v(4))-minimum(v(4))	7.852210e-02
mean(v(4))	2.276490e+02

Table 6: Results for the ripple and average output voltages of the envelope detector.

By analysing the result from both the theoretical and simulated models is possible to observe differences in values. These discrepancies are, in its majority, due to the non-linearity of the diodes. Due to this complexity, we are forced to use a simplistic model in our calculations, through Octave, while Ngspice uses a more complete model for the analysis of this circuit. With this, discrepencies in values are expected.

Beyond the envelope detector, it can also be compared the ripple voltage and the average output voltage of the voltage regulator, corresponding to the voltage on node 5. The results from Octave, on the left, and NGspice, on the right, can be observed in Table 7.

Name	**Value [V]**
$Ripple_{regulator}$	0.000076
$Average_{regulator}$	11.822949

Name	**Value [V]**
maximum(v(5))-minimum(v(5))	1.597796e-04
mean(v(5))	1.199992e+01

Table 7: Results for the ripple and average output voltages of the voltage regulator.

Similarly to the envelope detector, discrepancies can also be found on the ripple and average output voltages of the voltage regulator, by reasons metioned above.

4 Conclusion

After the theoretical analysis, the simulation and the results' comparison, it can be concluded that, despite the objective of the work, the design and analysis of a AC/DC converter circuit, presented in Figure-1, has been accomplished.

There were performed both a theoretical and a simulation analysis, where the non linearity of some components became noticeable. This laboratory assignment allowed us to constact with a more realistic and complex problem in a way that its goal forced us to integrate all of our knowledge acquired untill this moment, and made us understand what is in stake when we need to use models to aproximate a circuit. It became clear thet Ngspice is a powerfull tool in circuit solving, representing a good resource in a possible future problem in the industry context. Concluding, we were able to achieve the proposed objective and became more aware of the real context of the applications of this course lectures.