TÉCNICO LISBOA

Laboratory 4: Audio Amplifier

Msc. Aerospace Engineering, Técnico, University of Lisbon

Circuit Theory and Electronics Fundamentals

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Contents

1 Introduction

The goal of this laboratory assignment is to model and analyse an audio amplifier circuit, by designing both Gain and Output amplifier stages.

The circuit annalised is formed by two voltage sources, V_{in} and V_{CC}, seven resistors, R_S, R_{B1}, R_{B2}, R_{C1}, R_{E1}, R_{E2} and R_L, three capacitors, C_i, C_b and C_o, and two transformers. The circuit described is portrayed in Figure-1.

Throughout the report it is presented a theoretical analysis, a simulation of the circuit and its analysis as well as a comparison of the obtained results.

In Section 2, it is executed an analysis of the circuit using the Ngspice tool to simulate it. In Section 3, it is executed an incremental analysis, in order to do a theoretical analysis of the circuit, using the Octave maths tool. Lastly, in Section 5, it is performed a conclusion, bearing in mind the results from both the theoretical analysis and the simulation, from Section 3 and Section 2, respectively.

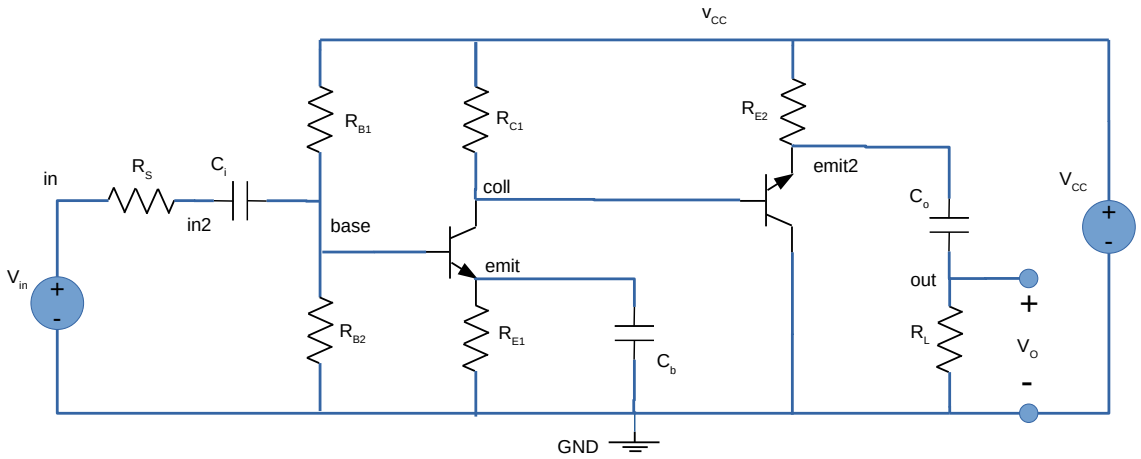

Figure 1: Circuit

2 Simulation Analysis

2.1 Audio Amplifier Simulation

In this section we simulate an audio amplifier through the NGspice tool. Our goal is to simulate the audio amplifier using two different kinds of transistors (NPN and PNP). It is our objetive to measure the output voltage gain in the passband and the lower and upper 3dB cut off frequencies, as well as the input and output impedances.

Important note: Beyond modelling and analysing the circuit provided, one of the goals of this laboratory assignment is to maximize the merit, which is computed according to the following formula:

$$M = \frac{\text{voltageGain} * \text{bandwidth}}{\text{cost} * \text{lowerCutoffFreq}} \tag{1}$$

Therefore, it was our intention to obtain the best value for this parameter,using each of the variables in order to maximize it, wich means that we have not tried to improve each of those separately, but as a all. In order to do it we used the values indicated the following values of the components: $R_{B1} = 79k\Omega$, $R_{B2} = 9.2k\Omega$, $R_{C1} = 2.4k\Omega$, $R_{E1} = 150\Omega$, $R_{E2} = 320\Omega$, $C_i = 5uF$, $C_b = 270uF$ and $C_o = 120uF$.

Merit	Value
Merit	1727.49
Cost	488.178 MU

Table 1: Merit Calculation

2.2 Output Voltage Gain

In order to measure the output voltage gain, we used Ngspice's *measure* function to determine the maximum value of the output voltage. By definition the gain is the magnitude coefficient between the output voltage and the input voltage. In this particular case, the input voltage has a magnitude of 1V, wich means that we can reduce the calculation of the gain phase and magnitude to the output voltage.

In the following table, we present the maximum magnitude of the gain (v(out)), in decibels:

Output Voltage Gain	Value
Output Voltage Gain	37.672

Table 2: Maximum Gain Magnitude, in dB

2.3 Frequency response

In this subsection, the same function as in the subsection 2.2 (*measure*) was used to compute the value of the lower and upper 3db cut off frequencies, which allowed the calculation of the bandwidth, which is the difference of the two variables previosuly mentioned. The results obtained are shown in the table bellow:

Variable	Value [Hz]
Low CO Freq	122.311
Up CO Freq	1.34864E+06
Bandwidth	1.34852E+06

Table 3: Lower and Upper Cut off Frequencies and Bandwidth, in Hz

In order to compare and understand the evolution of the circuit from the gain stage to the output stage we firtly show the magnitude and the the phase plots in the collector node (the output of the gain stage) and then the same quantities regarding the output stage:

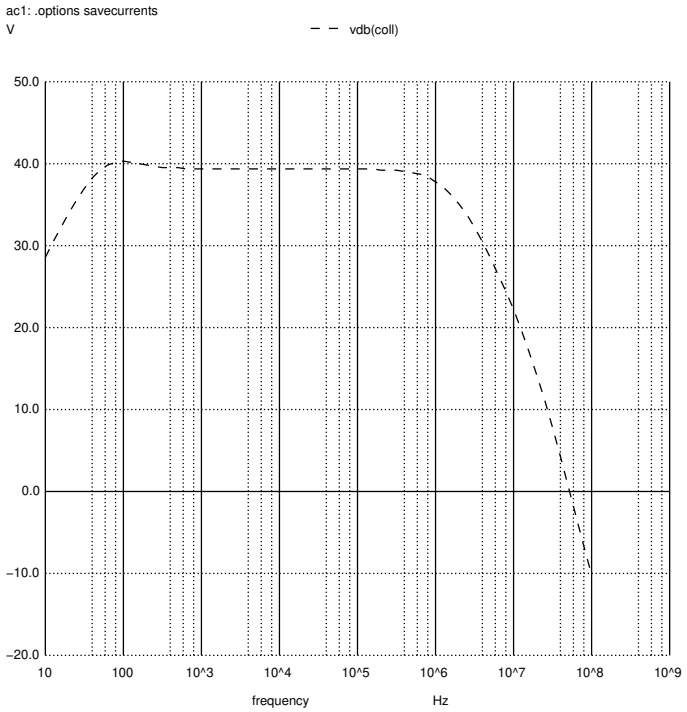

Figure 2: v(coll) magnitude, in dB

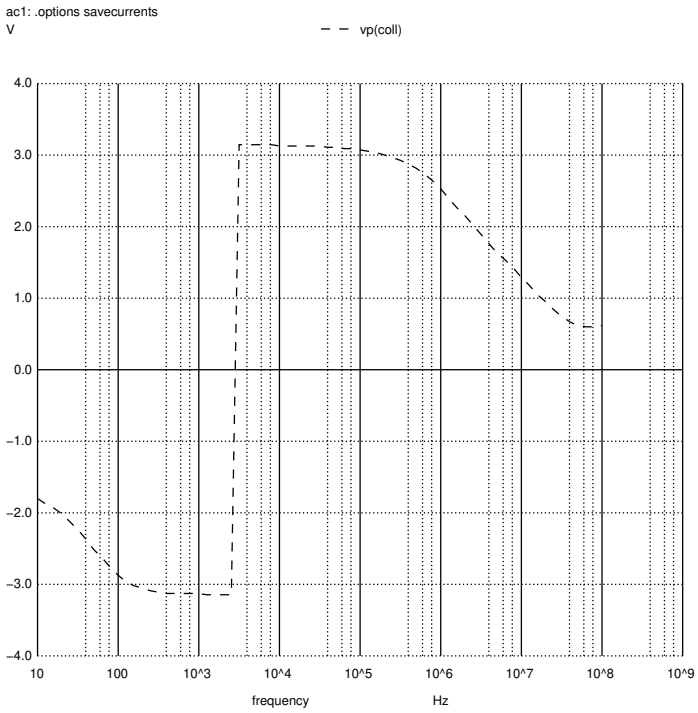

Figure 3: v(coll) phase, in rad

Next, we present the graphical representation of both the magnitude and the phase frequency response at the output stage:

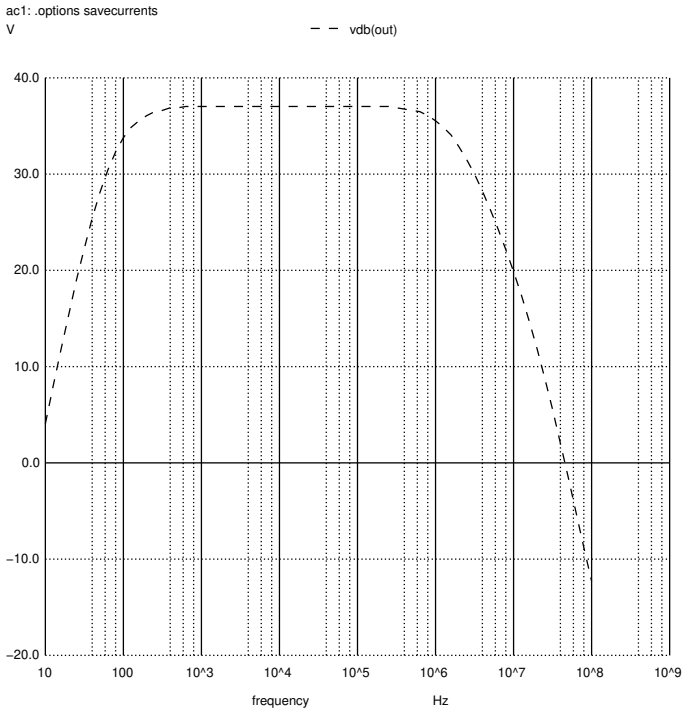

Figure 4: Gain / v(out) magnitude, in dB

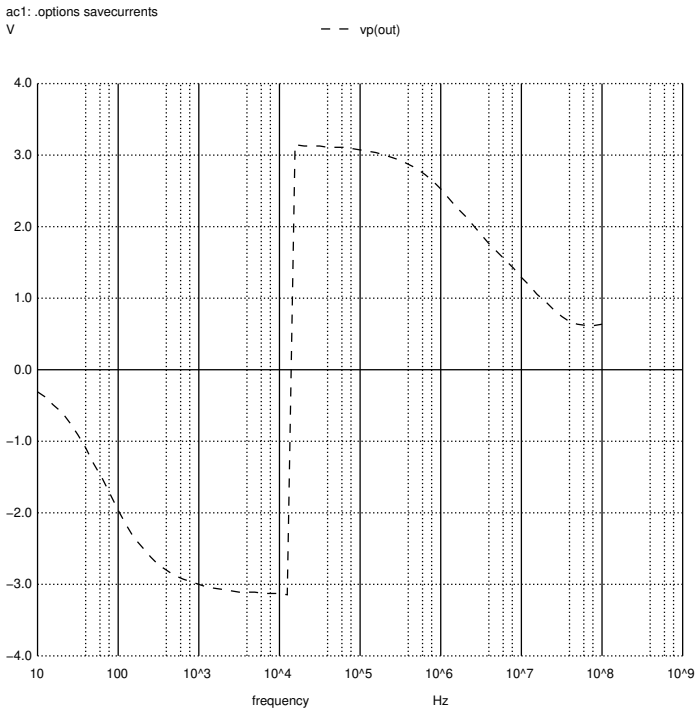

Figure 5: Gain / v(out) phase, in rad

2.4 Impedances

Finally, in this subsection the input impedance and the output impedance are presented. We can verify from them values that we achieved the goal of having a high input impedance and a low output impedance, wich allow to obtain a better amplifier:

Input Impedance	**Value [S]**
ZI	1362.56

Table 4: Input Impedance, in Siemens

Output Impedance	**Value [S]**
ZO	10.1249

Table 5: Output Impedance, in Siemens

3 Theoretical Analysis

In this section, we will analyse our theoretical model of the audio amplifier circuit in terms of the voltage gain, input and output impedances, and band width. The audio amplifier, as explained in the introduction is composed by two stages: the gain stage and the output stage. The first one provides a high gain and input impedance, however, it cames with a high output impedance that could degrade the signal transmitted to the load (by voltage division), which is not desirable. Thats why we need the second stage, which has a small gain (≈ 1), but provides also a small output impedance. Combining the two circuits, one can obtain a stable audio amplifier with good gain.

3.1 Gain stage

We will start by explaining why we need the components in the gain stage:

- The resistor R_{C1}, connected to the collector terminal of the transistor, is important to obtain a high gain as we will se in the operating point analysis.

- The resistor R_{E1}, connected to the emmiter terminal of the transistor, ensures a temperature stabilization effect by imposing a negative feedback loop. That is important because some paramaters of the transistor are temperature dependent.

- As we will see next, having the resistor R_{E1} is not good for the AC gain. So, using the capacitor C_b in parallel with the resistor we can make a short circuit for medium frequencies of v_{IN}, and the effect of the resistor can be neglected for the incremental analysis (because it is in parallel with a short circuit). For the operating point (DC), there is no AC component and the capacitor behaves like a open circuit, therefore, the resistor have the function of stabilization.

- Because v_{IN} has no DC component, we need a bias circuit, composed by the voltage supplier V_{CC} and two resitors R_{B1} and R_{B2}, that ensures the transistor is in the forward active region (FAR), where $V_{CE} > V_{BEON}$. We can simplify this circuit to a Thévenin's equivalent as showed in the next image.

- Also, we need another capacitor C_i to block the $0V$ DC component of v_{IN}, creating an open circuit for low frequencies (DC analysis). Otherwise, the transistor wouldn't be in FAR.

3.1.1 Operating point for gain stage

With the simplifications of the capacitors made before for low frequencies and without the voltage v_{IN} (which only has AC component), we can write the following circuit to make the operating point analysis:

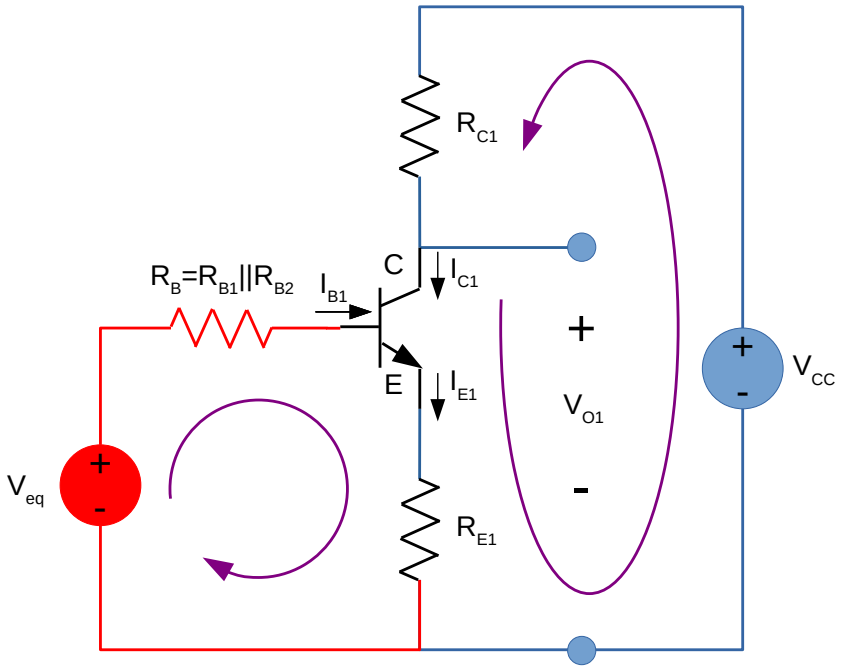

Figure 6: Gain stage circuit simplified to operating point.

First we reduce the bias circuit to a Thévenin's equivalent obtaining the resistor R_B and the equivalent voltage V_{eq}:

$$R_B = R_{B1}||R_{B2} = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}} \tag{2}$$

$$V_{eq} = \frac{R_{B2}}{R_{B1} + R_{B2}V_{CC}} \tag{3}$$

Then we can write KVL to the left mesh, where $V_{BEON} \approx 0.7$:

$$-V_{eq} + R_B I_B + V_{BEON} + R_{E1}I_{E1} = 0 \tag{4}$$

The currents in the NPN transistor are related by the parameter $\beta_{FN} = 178.7$ accordingly to the following equations:

$$I_{E1} = (1 + \beta_{FN})I_{B1} \tag{5}$$

$$I_{C1} = \beta_{FN}I_{B1} \tag{6}$$

With the previous equations, we can write a equation to obtain I_B and then, all the other currents in the transistor:

$$I_{B1} = \frac{V_{eq} - V_{ON}}{R_{B1} + (1 + \beta_F)R_{E1}} \tag{7}$$

After that, it's easy to compute the other DC voltages:

$$V_{O1} = V_{CC} - R_{C1}I_{C1} \tag{8}$$

$$V_{E1} = R_{E1}I_{E1} \tag{9}$$

$$V_{CE} = V_{O1} - V_{E1} \tag{10}$$

To ensure that the transistor is in the FAR, the next condition must be verified: $V_{CE} > V_{BEON}$. As we can see in the next table with the operating point values this was ensured.

Name	Value
v_{CE}	13.723093
v_{O1}	14.447977
I_{C1}	0.002801
I_{E1}	0.002817
I_{B1}	0.000016

Table 6: Some currents (A) and voltages (dB) from the operating point of gain stage.

Comparing this values with the ones in the simulation section, we can see that the DC values are much bigger in the simulation then the ones we got in theoretical calculations. This is a simple model with many simplifications that could justify that errors. For instance, we assume that the capacitors are either a short circuit or a open circuit; we fixed the value of V_{BEON} which depends of the values of the voltages in the rest of the circuit; we used a simple model for AC calculations, using only resistors and dependent current sources (the reality is much more complicated); the ngspice model is much more complex and has a lot of parameters not included in our model.

3.1.2 Incremental analysis for gain stage

Now, with the values of the operating point we can make the incremental analysis, for medium frequencies. As explained before, with this frequencies the capacitor C_b is an open circuit, therefore, we can use the following incremental model (without the resistor R_{E1}):

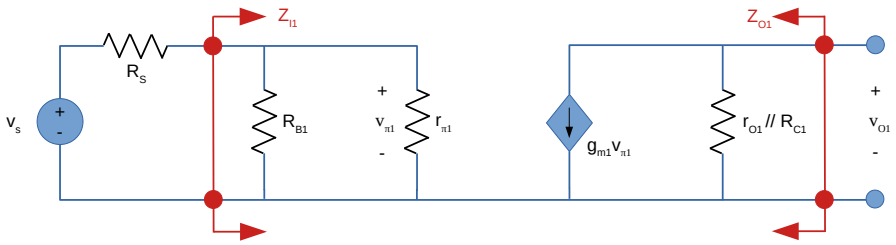

Figure 7: Incremental model circuit for gain stage.

The incremental parameters for this NPN transistor are given by:

$$gm1 = \frac{I_{C1}}{V_T} \tag{11}$$

$$r_{\pi 1} = \frac{\beta_{FN}}{g_{m1}} \tag{12}$$

$$r_{o1} = \frac{V_{AFN}}{I_{C1}} \tag{13}$$

With $V_{AFN} = 69.7V$ and $V_T = 25e^{-3}V$. Now we can compute the gain of the gain stage given by:

$$A_{V1} = \frac{R_{SB}}{R_S} R_{C1} \frac{-g_{m1} r_{\pi 1} r_{o1}}{(r_{o1} + R_{C1})(R_{SB} + r_{\pi 1})} \tag{14}$$

With $R_{SB} = \frac{R_B R_S}{R_B + R_S}$

To compute the impedances of the gain stage we must consider again the resistor R_{E1} between ground and emitter (not represented in the figure). To compute the output impedance we must also put $v_S = 0$, making a short circuit. The input and output impedances are given, respectively, by:

$$Z_{I1} = \frac{1}{\frac{1}{R_B} + \frac{1}{\frac{(r_{o1}+R_{C1}+R_{E1})*(r_{\pi 1}+R_{E1})+g_{m1}*R_{E1}*r_{o1}*r_{\pi 1}-R_{E1}^2)}{r_{o1}+R_{C1}+R_{E1}}}} \tag{15}$$

$$Z_{O1} = \frac{1}{\frac{1}{Z_X} + \frac{1}{R_{C1}}} \tag{16}$$

Where Z_X is given by:

$$Z_X = r_{o1} * \frac{R_{SB} + \frac{r_{\pi 1}*R_{E1}}{RSB+rpi1+RE1}}{\frac{1}{\frac{1}{r_{o1}}+\frac{1}{rpi1+RSB}+\frac{1}{RE1}+\frac{gm1*rpi1}{rpi1+RSB}}} \tag{17}$$

In the next table we print the theoretical results of the impedances and gain for the gain stage:

Name	Value
Z_{I1}	6260.534427
Z_{O1}	2385.199808
A_{V1}	47.165616

Table 7: Impedances and gain (dB) for gain stage.

As we can see, the output impedance is still very high, which is not desirable. However this is desirable for the input impedance, which has already a good value to ensure that the input voltage isn't being degraded by the resistor R_S. The gain obtained is also good. Notice that this stage is an inverting amplifier, and the gain (in volts) is negative.

3.1.3 Incremental analysis for output stage

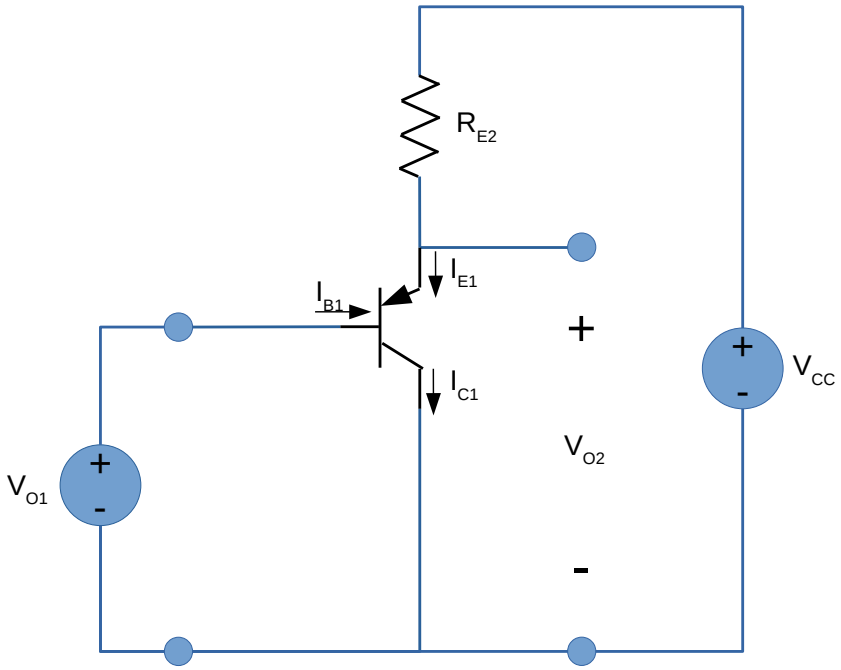

Figure 8: Output stage circuit simplified to operating point.

The output stage is similar to the gain stage, however it contains a PNP transistor with a higher value of the parameter $\beta_{FP} = 227.3$ and it doesn't have the bias circuit. The other parameters are given by $V_{AFP} = 37.2V$, $V_{EBON} = 0.7$. The main goal of this sub circuit is to achieve a small output impedance.

3.1.4 Operating point for the output stage

The calculations for this operating point follow the same logic of the ones derived in subsection 3.1.1. With KCL equations one can derive the following expression.

$$I_{E2} = \frac{V_{CC} - V_{EBON} - V_{O1}}{R_{E2}} \tag{18}$$

Then we can obtain the other currents in the transistors with the same raletions utilized in subsection 3.1.1. Notice that the output voltage of the first stage V_{O1} is now the input voltage of this stage.

Now we can obtain V_{O2}, the output DC voltage of the total circuit:

$$V_{O2} = V_{CC} - R_{E2}I_{E2} \tag{19}$$

The next table show the theoretical results for this operating point.

Name	Value
v_{O2}	15.529873
I_{C2}	0.018739
I_{E2}	0.018821
I_{B2}	0.000016

Table 8: Some currents (A) and voltages (dB) from the operating point of output stage.

3.1.5 Incremental analysis for the output stage

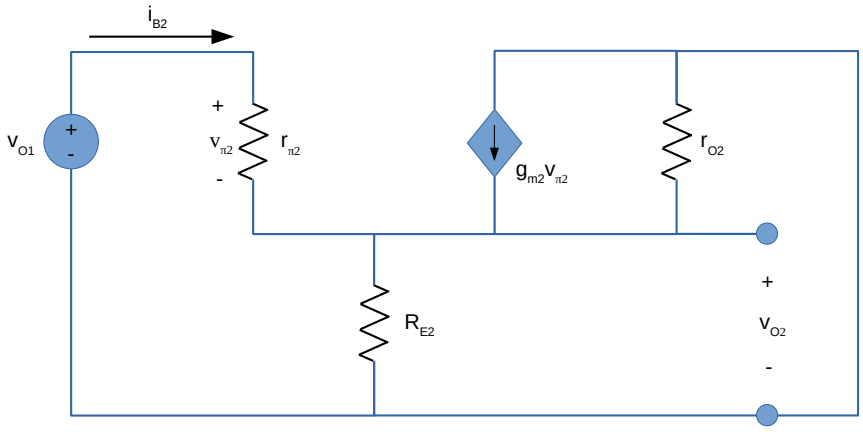

Figure 9: Incremental model circuit for output stage.

To make the incremental analysis we use the model in the image before. Using KCL in the transistor node, one can obtain this equation for gain:

$$A_{V2} = \frac{g_{m2}}{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}} \tag{20}$$

Where $g_{\pi 2} = \frac{1}{r_{\pi 2}}$, $g_{o2} = \frac{1}{r_{o2}}$ and $g_{e2} = \frac{1}{R_{E2}}$ are the condutancies.

Following the same logic of subsection , the input and output impedances for output stage are given by:

$$Z_{I1} = \frac{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}}{g_{\pi 2}(g_{\pi 2} + g_{o2} + g_{e2}} \tag{21}$$

$$Z_{O1} = \frac{1}{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}} \tag{22}$$

The results obtained are printed in the next table:

Name	Value
Z_{I2}	33119.705478
Z_{O2}	1.321902
A_{V2}	−0.079895

Table 9: Impedances and gain (dB) for output stage.

As we can see, the output impedance of this circuit is surprisingly small, which was our goal. The gain is ≈ 1, that means this circuit doesn't reduce much the voltage gain obtained in the first stage.

It's important to check if the two stages are compatible in terms of input and output impedances, to ensure that there are no significant losses in signal between stages. Because the output impedance of the gain stage Z_{O1} is much smaller than the input impedance of the second stage Z_{I1} (by more than a factor of 10), the voltage will be effectively transmited from the first stage to the second one, without many losses.

3.2 Total gain and impedances

Finally, we will calculate the total impedances and gain, in incremental terms. To achieve this, we can write the incremental model to the whole circuit, simplify the gain stage to a dependent voltage source and his impedances, and finally aplying KCL equation to the PNP transistor node. To compute the total output impedance Z_O we shut off input voltage and, therefore, the circuit becomes much simpler. The total input impedance is equal to Z_{I1}.

$$g_B = \frac{1}{\frac{1}{g_{\pi 2}} + Z_{O1}} \tag{23}$$

$$A_V = \frac{\frac{g_B + g_{m2}}{g_{\pi 2} g_B}}{\frac{g_B + g_{e2} + g_{O2} + g_{m2}}{g_{\pi 2} g_B}} A_{V1} \tag{24}$$

$$Z_I = Z_{I1} \tag{25}$$

$$Z_O = \frac{1}{g_{o2} + \frac{g_{m2} g_B}{g_{\pi 2} + g_{e2} + g_B}} \tag{26}$$

Name	Value
Z_I	6260.534427
Z_O	11.293345
A_V	46.802164

Table 10: Total impedances and gain (dB).

The theoretical value of Z_O is similar to the one obtained in the simulation and is very low, as we wanted. This is important when we connect a load with small impedance (like the speaker) to the amplifier. Z_I and the gain A_V are big values, as we wanted. Althought they are in the same order of magnitude as the values obtained in the simulation, the errors are still very large, due to the aproximations that this simple theoretical model does.

Although we obtained a constant value of gain in the theoretical calculations, regardless of the frequency of the signal, this is not the real scenario. As we saw on the simulation analysis, there is a lower and upper cut-off frequencies, where the gain starts droping. In this theoretical model we assumed medium frequencies and simplified the capacitors to short circuits or open circuits. To obtain more realistic results we should analyse the entire circuit with node or mesh incremental analysis, replacing the capacitors with his impedances. We are no doing that here, but we can observe the cut-off frequencies in the simulation chapter.

4 Comparison between Octave and Ngspice results

Table 11 shows, on the left, the values for the gain, input and output impedances, found with Octave, and, on the right, using the Ngspice simulation tool.

Name	**Value [V]**
Z_I	6260.534427
Z_O	11.293345
A_V	46.802164

Name	**Value [V]**
Output Voltage Gain	37.672
Low CO Freq	122.311
Up CO Freq	1.34864E+06
Bandwidth	1.34852E+06
ZI	1362.56
ZO	10.1249

Table 11: Results for the gain, input and output impedances.

In Section 3 it's highlighted some of the reasons for the discrepancies percieved on the results shown above.

5 Conclusion

After the theoretical analysis, the simulation and the results' comparison, it can be concluded that the design and analysis of the amplifier circuit, presented in Figure-1, has been accomplished.

There were performed both a theoretical and a simulation analysis, where the importance of this kind of circuits became noticeable. This laboratory assignment allowed us to contact with a more realistic problem in a way that its goal forced us to integrate all of our knowledge acquired untill this moment, and allowed us to understand what is in stake when we need to use models to aproximate a circuit. Beyond this, the circuit analysed is very usefull on our daily life.

We managed to obtain a good value of gain, wich means that the amplification was successfull.

Concluding, we were able to achieve the proposed objective and became more aware of the real context of the applications of this course lectures.