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FRANCIS SABADO II

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EDUCATION

Doctor of Philosophy in Computer Engineering **May 2017 (Expected)**
University of Arkansas, Fayetteville, AR **GPA: 4.00**
Awards: Doctoral Academy Fellowship

Masters of Science in Computer Engineering **August 2012 – Dec. 2015**
University of Arkansas, Fayetteville, AR **GPA: 4.00**
Graduate Courses: Integrated Circuit Design, Hardware Security, Low Power System Design, VLSI Design

B. S. in Computer Engineering with Minor in Mathematics *(Highest Distinction)* **August 2008 – May 2012**
University of Arkansas, Fayetteville, AR **GPA: 3.97**
Awards: Dean's List, Chancellor's List, Governor's Scholarship, Chancellor's Scholarship: (2008-2012)
Courses: Computer Architecture, Embedded Systems, Mobile Programming, Artificial Intelligence

EXPERIENCE

Software Engineer Intern **Hewlett-Packard** **June 2015 – August 2015**
Tools and Automation Team

- Provided support and maintenance for the Storage Automation Tool (SAT). SAT includes over 76 applications and is used by 6 internal HP teams. (Perl, HTML, JavaScript)
- Developed and deployed a password reset application on an Internet Information Services (IIS) server with enhanced security features including AES encryption, SSL, and HTTPS to support 65,0000 HP Inc employees. (ASP.net, C#, HTML, JavaScript, Active Directory, IIS)

Graduate Assistant **University of Arkansas** **August 2012 – Present**
TruLogic Circuit Design Lab

- Developed digital circuits and systems for ultra-low power, extreme temperature, hardware security, and asynchronous logic. (VHDL, Verilog/Verilog-A, TCL, Python)
- Instructed a course on programming foundations for 15 students, teaching students algorithms and data structures. Administered the programming foundations lab, advising 127 undergraduate students on course projects and homework. Supervised the Digital Design lab and instructed 52 students on fundamental topics of digital circuit design. (C++, VHDL)

CONFERENCE PUBLICATIONS

- Habimana J., **Sabado, F.,** and Jia Di, "Multi-Threshold Dual-spacer Dual-rail Delay-insensitive Logic: An Improved IC Design Methodology for Side Channel Attack Mitigation".IEEE International Symposium on Circuits & Systems 2016
- Caley, L., Chien-Wei Lo, **Sabado, F**., Jia Di, "A comparative analysis of 3D-IC partitioning schemes for asynchronous circuits," IC Design & Technology (ICICDT), 2014 IEEE International Conference on, pp.1,4, 28-30 May 2014
- **Sabado F.** and Jia Di, *"Comparison of Asynchronous and Synchronous Digital Circuits under Extreme Temperatures."* State Undergraduate Research Fellowship (SURF). May 2011

LANGUAGES AND TECHNOLOGIES

- **Languages:** C/C++, Java, Perl, Python, Bash, TCL, PHP, HTML, VHDL, Verilog
- **Operating Systems:** Linux, Windows
- **Development Tools:** Vim, Cadence Tool Suite, Synopsys Design Compiler, ModelSim

HONOR SOCIETY AND MEMBERSHIPS

- **Tau Beta Pi:** The Engineering Honor Society.
- **Eta Kappa Nu:** The International Electrical and Computer Engineering Honor Society.
- **Phi Kappa Phi:** The All-discipline Honor Society.
- **IEEE Student Member:** Institute of Electrical and Electronics Engineers.
- **ACM Member:** Association for Computing Machinery.

ADDITIONAL EXPERIENCE AND AWARDS

- Arkansas Challenge Scholarship (2008-2012)
- Phillip Murray-USWA Scholar (2008)
- Governor's Award for Musical Excellence (2008)
- Engineering Freshmen of the Year Finalist (2008)
- National Merit Corporation Scholar: Rheem (2008)
- Asian and Pacific Islander Scholar : Wal-Mart (2008)