Laboratory Report 3: AC/DC Converter

Circuit Theory and Electronics Fundamentals

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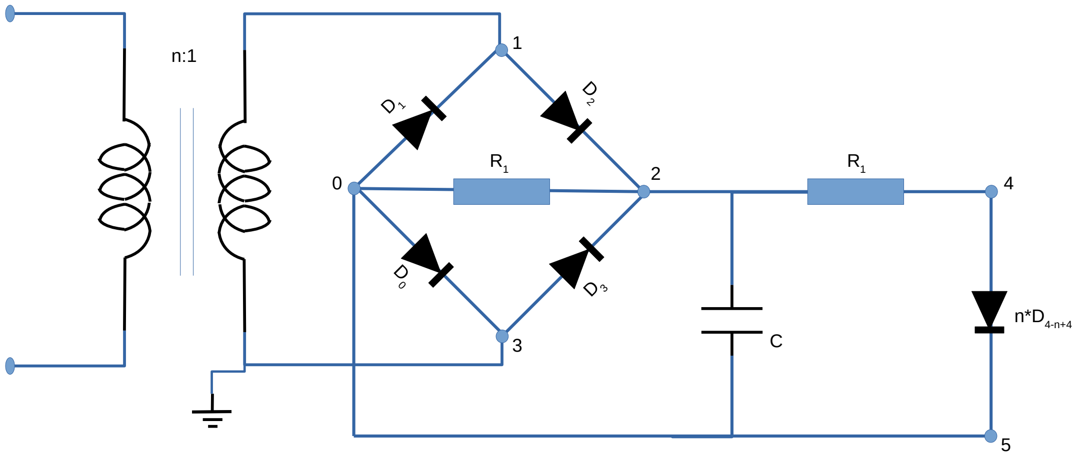
1 Introduction

The objective of this laboratory assignment is to transform an AC input voltage of 230V to a DC output voltage of 12V. To attain this goal, we used a circuit with three main parts: a transformer, an envelope detector (composed by a full-wave bridge rectifier with 4 diodes, 1 resistor and 1 capacitor) and a voltage regulator (containing 1 resistor and an undefined number of diodes that was computed by an algorithm which we had developed). The referred circuit is shown in the picture below.

Figure 1: AC/DC transformer circuit



As mentioned above, it is also important to refer that we have developed an optimization algorithm (in Octave) in order to find the number of diodes, the values of the resistors and capacitor and the consequent "n" (relation established by the number of coils in each side of the transformer) that would lead to the best value of merit, computed in Ngspice with the formula given by the Professor.

2 Theoretical Analysis

In this section we will discuss the theoretical analysis of our circuit. For this purpose, we will first explain seperately the envelope detector and the voltage regulator circuits on the AC/DC converter. The values used throughout this analysis are shown below. V_ON is achieved by using the Ngspice value for V_out. Theoretically, V_ON is given by equation 1.

$$V_{ON} = \frac{V_{out}}{N_{diodes}}, \tag{1}$$

V_{ON} value is computed using *Ngspice* results for V_{out}. By definition, $V_{ON} = \frac{V_{out}}{N_{diodes}}$

Symbol	Value
V_{ON}	0.6
A_f	$14.64891221288435V$
R_{ef}	$26k\Omega$
R_{rf}	$10k\Omega$
C	$3.3750e-05F$
$numberofdiodes$	20
η	1

Table 1: Values for theoretical analysis

2.1 Envelope Detector

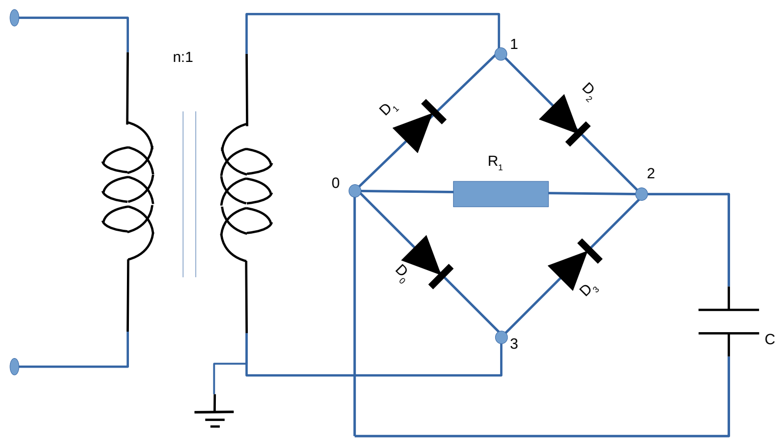


Figure 2: Envelope Detector Circuit.

As seen in figure 2, the envelope detector part of the circuit consists on a full wave bridge rectifier, a resistor (R_ef) and a capacitator (C), the last two in paralell. To reach the mininum ripple possible, we can increase the resistor impedance and the capacitor capacity, so that the time constant τ of the capacitor discharge is high enough ($\tau = RC$). Another method was to use a full wave rectifier, as said above, since the time of discharge of C is half of what it would be using a half wave rectifier. This part of the circuit was used to envelope the V_{in} sinusoidal wave, being V_{in} achieved from the following equation.

The envelope detector can be on a positive cycle where D_0 and D_2 let current pass or a negative cycle that corresponds to D_1 and D_3 letting the current pass.

$$V_{in} = \frac{230V}{n}, \tag{2}$$

Regardless of the cicle the envelope detector is on, using KVL we achieve the following equation.

$$V_o + 2V_{ON} - V_{in} = 0, \tag{3}$$

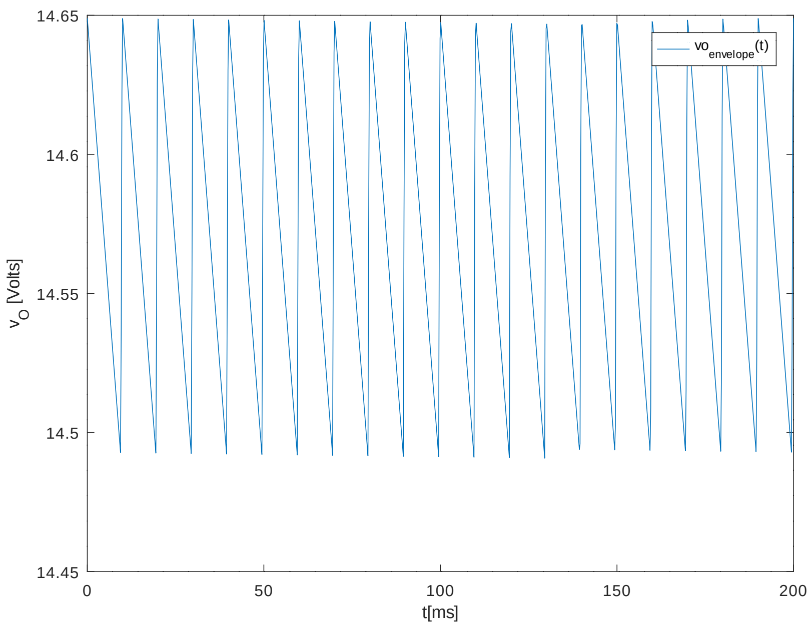
When the current on the resistor is equal to the current on the capacitor, the diodes shut off, leading to the following equation.

$$\frac{Acos(\omega t|_{OFF}) - 2V_{ON}}{R_{eq}} = A\omega sin(\omega t|_{OFF}) \tag{4}$$

where $R_{eq} = R_{env}||R_{vreg}$

$$V_o = V_o|_{t_{OFF}} e^{-\frac{t-t_{OFF}}{R_{eq}C}} \tag{5}$$

Figure 3: Envelope detector voltage



2.2 Voltage Regulator

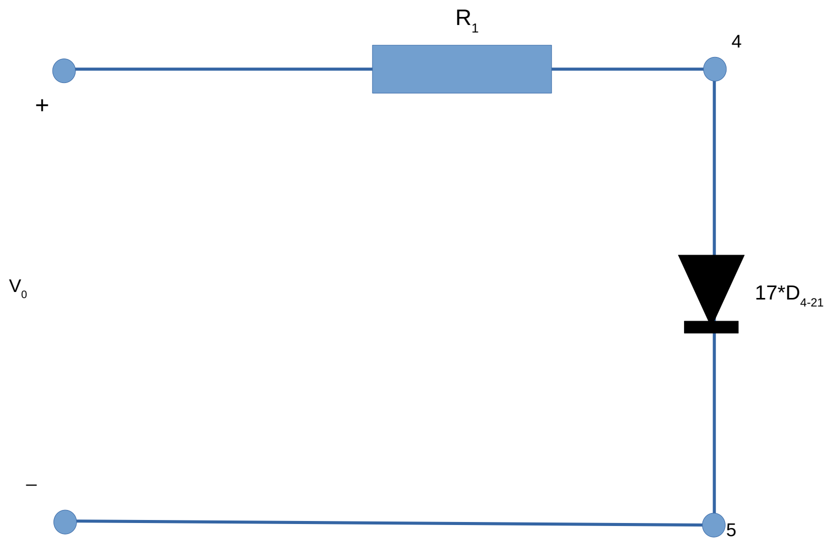


Figure 4: Voltage Regulator Circuit.

This part of this circuit was implemented so as to limit the voltage value and to soften the riple of the voltage that came from the previous part of the circuit (2.1). It involves a resistor and seventeen diodes in series.

The analysis has to be made by seperating the DC and AC components. The DC simulation uses the condition $V_o = N * V_{ON}$, so that we can replace each diode with V_{ON}.

In this section, the theoretical analysis requires we think about the DC and AC components separately ($V_o = V_O + v_o$).

The DC analysis is fairly simple since if $V_O > 17 * V_{ON}$, V_O is equal to $17 * V_{ON}$. The number 17 can be replaced by any number of diodes chosen.

As for AC, we achieve equation 6 by using equations 7 and 8. The variable k is the Boltzmann constant, T is the temperature in Kelvin and q is electron charge. To lower the v_{out} ripple, the value for r_d should also be low (see equation 7).

$$v_{out} = \frac{nr_d}{nr_d + R_{vreg}} v_o, \tag{6}$$

$$r_d = \frac{\eta V_T}{I_s e^{\frac{V_D}{\eta V_T}}}, \tag{7}$$

$$V_T = \frac{kT}{q}, \tag{8}$$

The cost is obviously the same as obtained above in the simulation analysis 9.

The plots shown below are related to the variables V_{input}, $V_{envelope}$ and V_{output} in function of time. Those were a result of the analysis in Ngspice. The values for the merit, ripple and average output voltage are in table 2.

Figure 5: Output voltage and Output voltage - 12 V

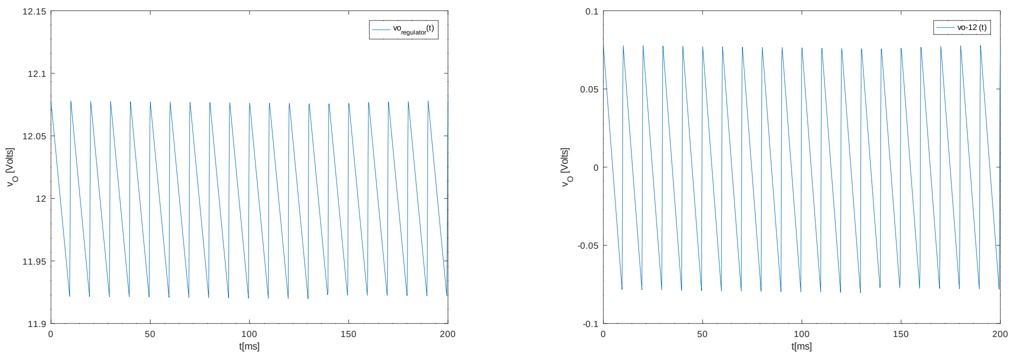
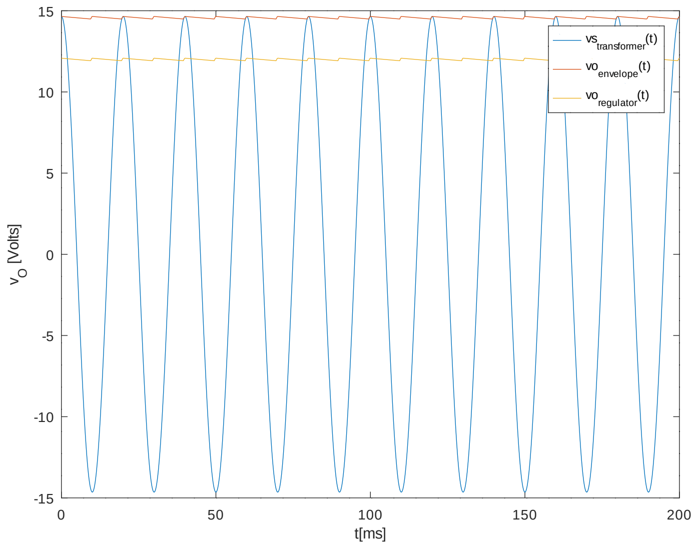


Figure 6: Input, Envelope and Output voltages



Element	Value
Average Output Voltage [V]	1.2000e+01
Output Voltage Ripple [V]	1.5813e-01

Table 2: Theoretical Values for Average and ripple.

3 Simulation Analysis

In this section, we will the obtained results by simulating the referred circuit in Ngspice.

In order to analyze the circuit and achieve the main goal of this laboratory assignment, we have developed an optimization ocatve algorithm that would give us the values which would leat to the greater merit value. The obtianed values were the following ones, presented in table 3:

Then, using the expression given by the Professor, we can automatically compute the cost:

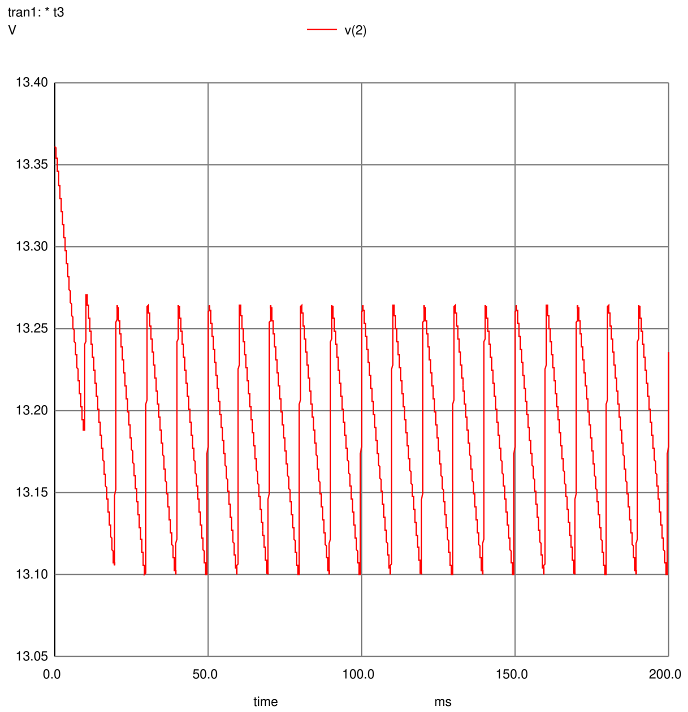
Element	Value
n (Transformer)	15.70082452
Number of diodes	20
C F	3.3750e-05 F
Renvelope	26k
Rregulator	10k

Table 3: Obtained values by optimization ocatve script

$$Cost = 72.15 \quad (9)$$

The plots shown below are related to the variables V_{input}, $V_{envelope}$ and V_{output} in function of time. Those were a result of the analysis in Ngspice. The values for the merit, ripple and average output voltage are in table 4.

Figure 7: Envelope detector voltage



Element	Value
Average Output Voltage [V]	1.199998e+01
Output Voltage Ripple [V]	7.809000e-02
Merit	1.774688e-01

Table 4: Simulation Values for Average, Ripple and Merit.

Figure 8: Output voltage and Output voltage - 12 V

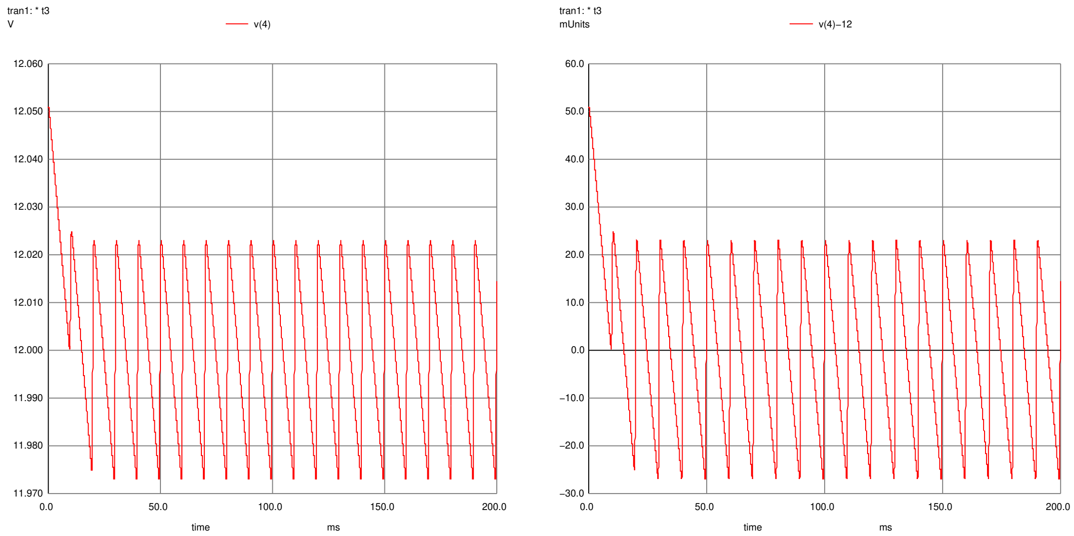
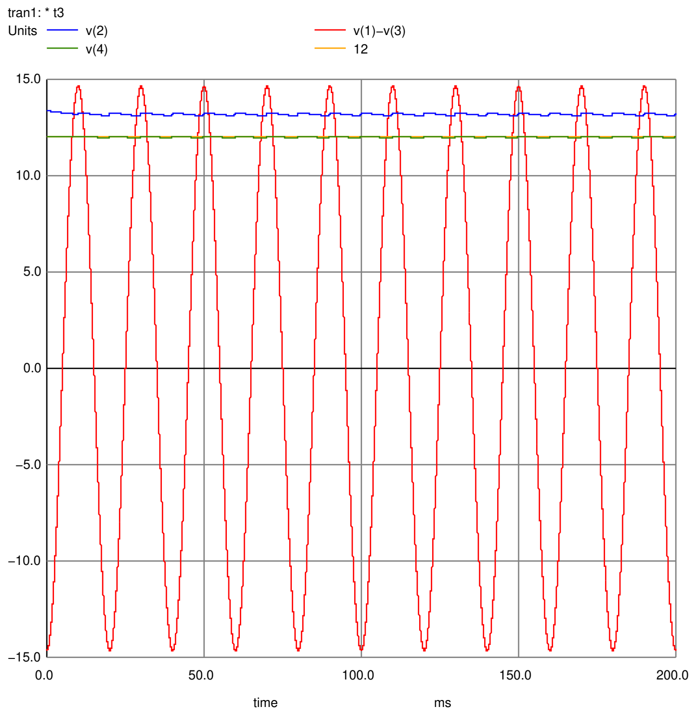


Figure 9: Input, Envelope and Output voltages



4 Conclusion

We can finally compare side by side the plots for the output voltages for the Envelope Detector and the Voltage Regulator, as well as the output AC component + DC deviation.

Below we can see that the plots obtained are similar and any differences are within the expected discrepancy. Those can be due to the complexity and non-linearity of the used model, both theoretically and in the simulation. For the simulation deviation we obtained a value of 7.809000e-02 and as for theoretically we obtained a value of 1.5813e-01. These are also similar, making this laboratory considerably sucessful. Another reason for this can be the fact that we used the same values for V_{on}, Is, η, V_T as Ngspice uses for the circuit model.

Finally, we can say we obtained a price of 72.15 and a merit of 1.774688e-01, values that were obtained through the already mentioned optimization program that can be found in folder mat, which created a new Ngspice in each cycle, making sure that the value n used for the transformer was well achieved throughout the required calculations and not a random number(since such assumption would drastically and wrongly improve the merit values).

Figure 10: Simulation envelope detector voltage

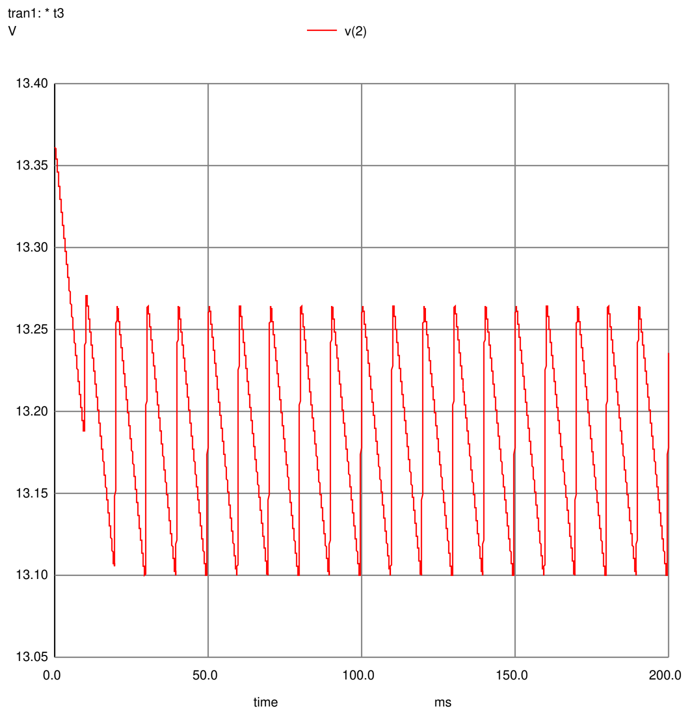


Figure 11: Theoretical envelope detector voltage

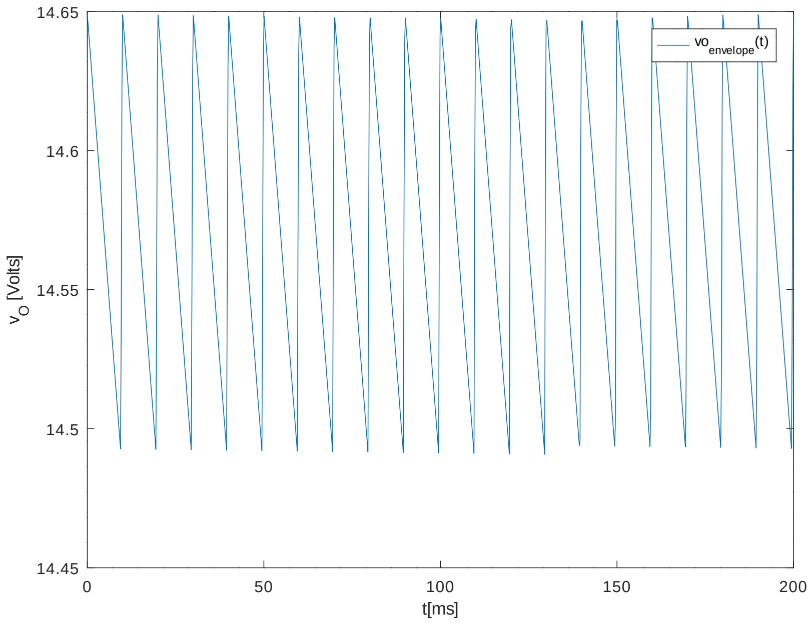


Figure 12: Simulation voltage regulator voltage

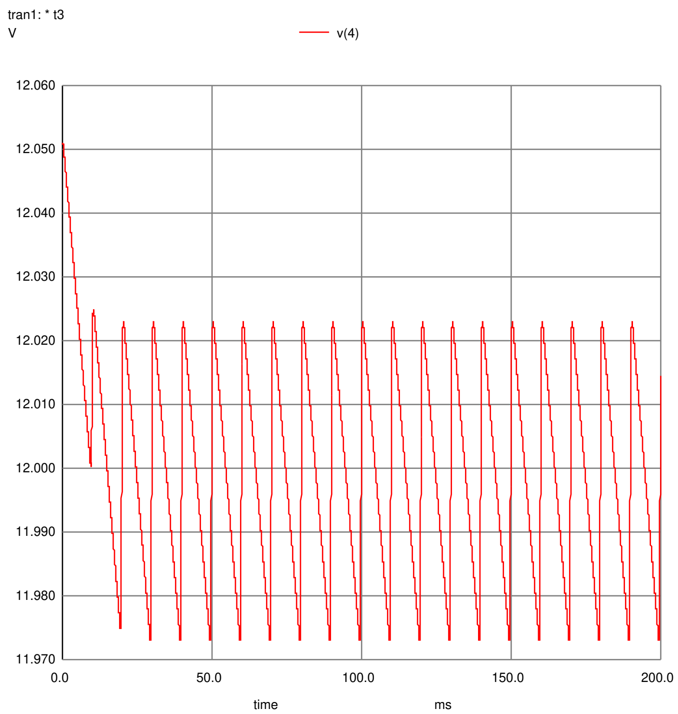


Figure 13: Theoretical voltage regulator voltage

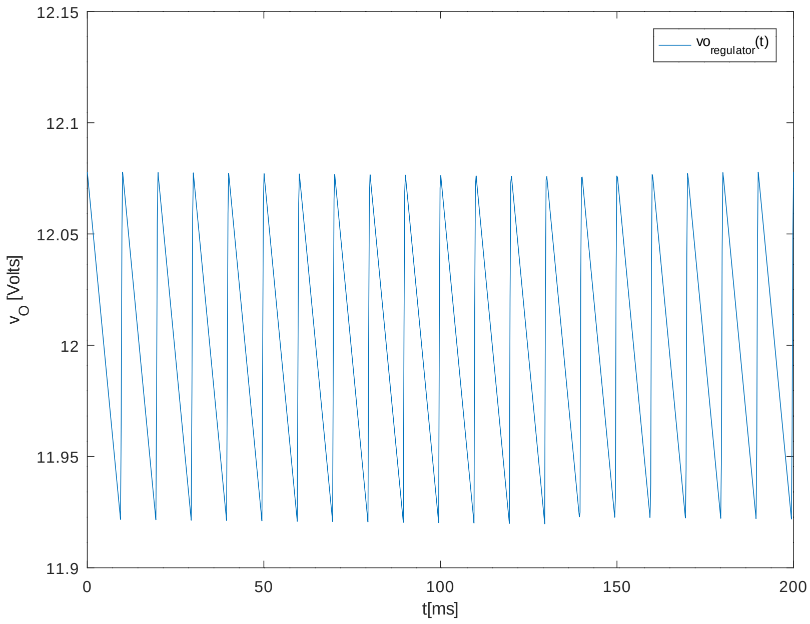


Figure 14: Simulation output AC component + DC deviation

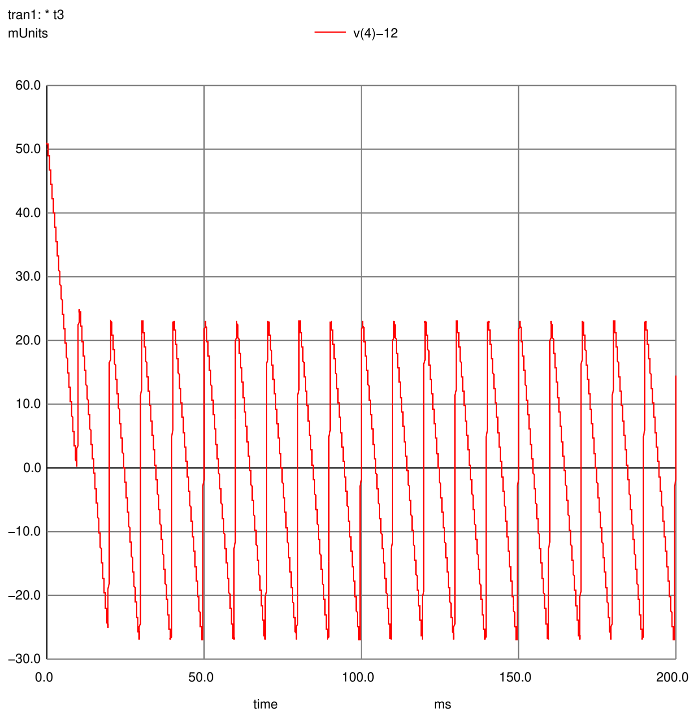


Figure 15: Theoretical output AC component + DC deviation