

POLYTECHNIC UNIVERSITY OF CATALONIA

MASTER THESIS

SafeDM a light-lockstep approach

Author:

Francisco BAS JALÓN

Supervisor:

Dr. James SMITH

*A thesis submitted in fulfillment of the requirements
for the degree of Master's degree in Electronic Engineering
in the*

Research Group Name
Department or School Name

May 21, 2022

Declaration of Authorship

I, Francisco BAS JALÓN, declare that this thesis titled, “SafeDM a light-lockstep approach” and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed:

Date:

“Thanks to my solid academic training, today I can write hundreds of words on virtually any topic without possessing a shred of information, which is how I got a good job in journalism.”

Dave Barry

Polytechnic University of Catalonia

Abstract

Faculty Name
Department or School Name

Master's degree in Electronic Engineering

SafeDM a light-lockstep approach

by Francisco BAS JALÓN

The Thesis Abstract is written here (and usually kept to just this page). The page is kept centered vertically so can expand into the blank space above the title too...

Acknowledgements

The acknowledgments and the people to thank go here, don't forget to include your project advisor...

Contents

Declaration of Authorship	iii
Abstract	vii
Acknowledgements	ix
1 Introduction	1
1.1 Motivation	1
1.2 Contribution	1
1.3 Structure of the Thesis	1
2 Background	3
2.1 Fault, Failures and Errors	3
2.2 Safety Related Systems	3
2.3 Fault detection	3
2.4 Redundancy and Sphere of Replication	3
2.5 Diversity	3
2.6 Lockstep execution	3
2.6.1 Hardware Lockstep Execution	3
2.6.2 Software Lockstep Execution	3
2.7 Other Fault detection Approaches	3
3 SafeDE	5
3.1 SafeDE Motivation	5
3.2 Architecture	5
3.3 Features and limitations analysis	5
3.4 N-modular redundancy	5
3.5 SafeDE Implementantion and Integration	5
3.5.1 De-RISC Platform	5
3.5.2 SELENE Platform	5
3.5.3 Hardware Integration	5
3.5.4 Configuration and Operation	5
3.5.5 Software Integration	5
3.6 SafeDE Evaluation	6
3.6.1 Functional Validation	6
3.6.2 Fault Injection	6
3.6.3 Time Overhead	6
3.6.4 Hardware Costs	6
3.7 Conclusions	6
4 Conclusions and Future Work	7
A Published Work	9

List of Figures

List of Tables

List of Abbreviations

LAH List Abbreviations **Here**
WSF What (it) Stands For

Physical Constants

Speed of Light $c_0 = 2.997\,924\,58 \times 10^8 \text{ m s}^{-1}$ (exact)

List of Symbols

a	distance	m
P	power	W (J s ⁻¹)
ω	angular frequency	rad

For/Dedicated to/To my...

Chapter 1

Introduction

1.1 Motivation

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

1.2 Contribution

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

1.3 Structure of the Thesis

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

Chapter 2

Background

2.1 Fault, Failures and Errors

2.2 Safety Related Systems

2.3 Fault detection

2.4 Redundancy and Sphere of Replication

2.5 Diversity

2.6 Lockstep execution

2.6.1 Hardware Lockstep Execution

2.6.2 Software Lockstep Execution

2.7 Other Fault detection Approaches

Chapter 3

SafeDE

3.1 SafeDE Motivation

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

3.2 Architecture

3.3 Features and limitations analysis

3.4 N-modular redundancy

3.5 SafeDE Implementantion and Integration

3.5.1 De-RISC Platform

3.5.2 SELENE Platform

3.5.3 Hardware Integration

3.5.4 Configuration and Operation

3.5.5 Software Integration

Sed ullamcorper quam eu nisl interdum at interdum enim egestas. Aliquam placerat justo sed lectus lobortis ut porta nisl porttitor. Vestibulum mi dolor, lacinia molestie gravida at, tempus vitae ligula. Donec eget quam sapien, in viverra eros. Donec pellentesque justo a massa fringilla non vestibulum metus vestibulum. Vestibulum in orci quis felis tempor lacinia. Vivamus ornare ultrices facilisis. Ut hendrerit volutpat vulputate. Morbi condimentum venenatis augue, id porta ipsum vulputate in. Curabitur luctus tempus justo. Vestibulum risus lectus, adipiscing nec condimentum quis, condimentum nec nisl. Aliquam dictum sagittis velit sed iaculis. Morbi tristique augue sit amet nulla pulvinar id facilisis ligula mollis. Nam elit libero, tincidunt ut aliquam at, molestie in quam. Aenean rhoncus vehicula hendrerit.

3.6 SafeDE Evaluation

3.6.1 Functional Validation

3.6.2 Fault Injection

3.6.3 Time Overhead

3.6.4 Hardware Costs

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

3.7 Conclusions

Chapter 4

Conclusions and Future Work

Appendix A

Published Work

Write your Appendix content here.