WANG, Tiffany 260684152
YE, Frank 260689448
GROUP 08 - MacroHard EE

G08 7-SEGMENT DECODER

Introduction

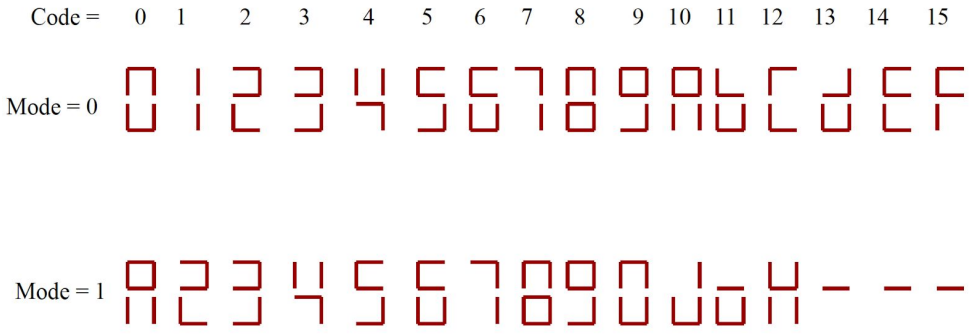
Seven-segment display is a popular way of representing numbers and is used in various scenarios such as clocks, crosswalk countdowns, etc. This lab will mainly transcribe a seven-bits input to a seven-segment display code.
The 7-segment lab component fully coded in VHDL by the authors of this report, Tiffany Wang and Frank Ye.

TABLE OF CONTENT

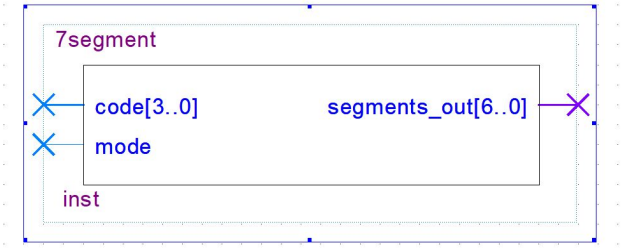
1. VHDL Code

The entity g08_7_segment_decoder takes in a 4-bits code and a 1-bit input. which determines the mode of the display: ‘0’ corresponds to HEX, and ‘1’ to cards. An intermediate 5-bit vector signal xcode merges the code and mode together for easier manipulation later. Each input code is associated to a corresponding 7-segment display output encoding using the With/Select method. This design offers the advantage of an one-to-one mapping between inputs/outputs.

The inputs and outputs corresponds to the following requirement:



The equivalent symbol diagram of the VHDL code:

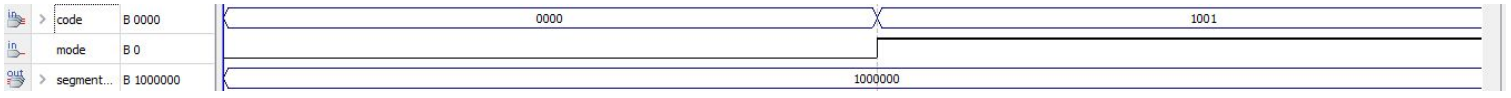


INPUT: code[3..0]
INPUT: mode
OUTPUT: segments_out[6..0]

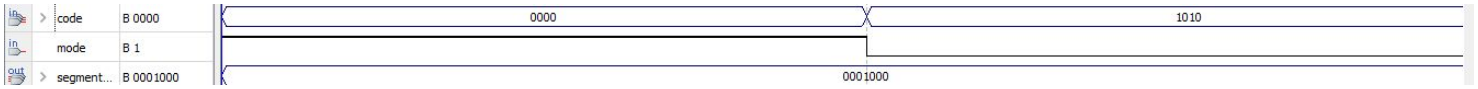
2. Testing

The VHDL code was tested with a simulated waveform. Since the way the With/Select code functions is straightforward, we simply tested the 32 possibilities of the input range to ensure desired behavior, since this component will be reused for the final project.
Below are some arbitrary test cases demonstrating the desired behavior. First, are two cases for which 1 output segment has 2 possible inputs, one with mode 0, one with mode 1. The third figure shows the case for an input that has an output with one mode, and no one for the other

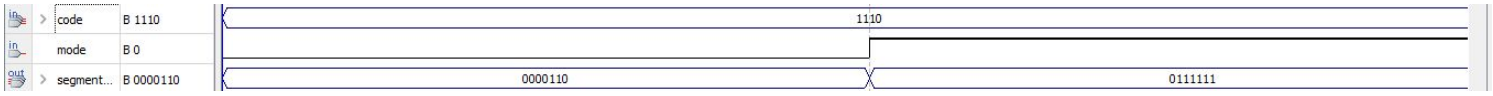
Output 0: “00000” + “10011” → “1000000”



Output A: “10101” + “00001” → “0001000”



Code “1110”
Mode 1: Output “0111111” (equivalent to -)
Mode 0: Output “0000110” (equivalent to E)



The results are as expected. Every output corresponds to the 7-segment encoding of the input. However, it is hard to visualize the result simply by comparing bits vectors. Mistake may have occurred when writing out the encoding of the input for example. This is a limitation we currently have for this lab. A better test would be conducted once we receive FPGA board with the actual integrated 7-segment display hardware.

3. References

[1] Clark J., *Lab #2 - Combinational Circuit Design with VHDL*, ECSE 323 Digital System Design, Fall 2017