

ECSE-323

Digital System Design

Lab #5 – *System Integration for the Card Game* *Fall 2017*

Introduction

In this lab you will put together all of the parts for the complete card game system and implement it on the Altera board.

Learning Outcomes

After completing this lab you should know how to:

- Get a complete digital system working on the Altera board, and will have gained experience in implementing user interfaces.

Table of Contents

This lab consists of the following stages:

1. Design and simulation of the computer player FSM
2. Design of the complete system Datapath
3. Design of the complete system controller FSM
4. Testing of the complete system on the Altera board
5. Writeup of the lab report

The Complete Card Game System

In this lab you will combine all of the parts you have developed in the previous labs and create the full Card Game system. Most of the work has been done in the previous labs, but in this lab you will need to construct the *user interface* circuitry, which permits a human player to control his/her play, and the *computer player* circuitry, which automatically makes a correct play during the computer's turn. The user interface will make use of the switches, buttons, and LED displays on the Altera DE1 board. You will also need to construct a controller (FSM) that will control the game play process.

The system should be designed to be able to play the game. The game should continue until either the player or the computer wins (previous lab has game rules)

Once you have constructed the full system, it will be downloaded to the Altera board hardware and tested (played!).

1. The Card Game User Interface

The interface of the system to the human player should have the following inputs and outputs:

USER INPUTS:

- Reset pushbutton - starts a new game
- Play pushbutton – requests a card from dealer
- Select Ace =1 or Ace =11
- Stop (no longer request cards, dealer's turn)
-

USER DISPLAYS (to be selected by the *Display Select* setting):

- Card on top of the Play Pile
- Total for Player and total for dealer
- Number of Games won by player
- Number of Games won by dealer
- Number of Games Played
- Number of Games won
- Invalid Play Indicator
- Game Over Indicator

2. Design of the Computer Player FSM

You will construct an FSM that will control the play of the Computer Player.

The Computer Player operational sequence should be as follows:

- Wait for its turn (i.e. look at the TURN control signal). De-assert the DONE signal when the TURN signal indicates the Human Player's turn.
- When it is the computer player (dealer) turn, it will select cards from the deck and determine whether to continue (sum of cards below the specified value) or to stop.
- The FSM will have to determine who wins and to increment the counter for winner (dealer or player) increment the number of games played, and determine whether there is a final winner (e.g. best 3 out of 5 games).
- After each game the deck should be shuffled (randomized) such that the order of cards should be different each game.

2. The Computer Player FSM Design

Begin the design process by drawing the state transition diagram for the computer player FSM. Show this diagram to the TA.



Next, write a VHDL description of the Computer Player FSM, and show it to the TA.



Compile the FSM and perform a functional simulation, entering suitable control signal values (e.g. TURN signal) by hand.





TIME CHECK

You should be this far at the end of your *first* 2-hour lab period!

2. The Complete System Datapath Design

Now you will put together all of the parts for the complete system. Begin by deciding on what modules you will need to provide the proper functionality (i.e. the datapath, which will also include the computer player FSM).

You should layout the datapath using schematic capture in Quartus, so that you have a nice block diagram for the report.

2. The Complete System Datapath Design

You can't just add in modules at will, without considering the FPGA resource utilization. In particular, you should go back to your report for lab #3 and check how many Embedded Array blocks were used for your stack circuit. How many stacks can you fit in the Cyclone II FPGA, without modification of the circuit?

One strategy is to minimize the space used for cards and other resources. Are there ways of reducing the demands your design will make?

While you or the dealer are adding cards, what is important is the total (accumulation) of the card values, you only need to add up to 21 at the most. The total number of cards that you will acquire is limited (statistically what is the expected value for “n” random draws of a deck?



TIME CHECK

You should be this far at the end of your *second* 2-hour lab period!

3. The Complete System Controller Design

The last step in the design of the complete system is the design of the system controller. This controller is an FSM that generates the control signals for the datapath module which produces the proper game playing behaviour.

Begin by drawing the state transition diagram for the FSM. Take care that you properly detect transitions on various external input and datapath status lines (i.e. to detect a rising edge, first wait for the signal to go low then wait for it to go high). Don't try to do too much in a single state, use as many states as you need. Show the state diagram to the TA.



Next, write a VHDL description of the system FSM, and show it to the TA.





TIME CHECK

You should be this far at the end of your *third* 2-hour lab period!

4. Testing of the Complete System on the Altera Board.

Finally, connect the system controller FSM up to the datapath and to the external inputs and outputs. Then compile the full circuit and download it to the Altera board.

Demonstrate the functioning of your system to the TA. Make sure to demonstrate the following:

- **Resetting of the system** (i.e. beginning new games). Make sure that the human player's hand is randomized, and that each player gets the right number of cards to start with.
- **Proper Display of all required items.**
- **Detection of Invalid Plays.**
- **Correct Computer Player Play.**
- **End-of-Game Detection and Winner Determination**



Note the speeds at which the computer player plays. It may be difficult to check whether the computer is playing correctly!



TIME CHECK

You should be this far (i.e. have completed the lab) at the end of your *fourth* 2-hour lab period!

5. Writeup of the Lab Report

Write up a report for the complete *Card Game* system that you designed.

The report must include the following items:

- A header listing the group number (and company name if you have one), the names and student numbers of each group member.
- A title, giving the name of your system.
- A description of the system's features (i.e. what it does).
- A block diagram of the entire system.
- A description of how your system works, referring to the block diagram.
- A description of the user interface (e.g. a users guide to operation).
- A discussion of how the complete system was tested.
- A summary of the FPGA resource utilization.
- A conclusion section discussing problems or significant issues that arose during the design process, as well as a discussion of possible enhancements or extensions that could be made to your system.

Some items to remember when preparing the report for lab #5:

- All diagrams, tables, and figures should have captions describing the contents of the figure and be given a figure number.
- All such figures must be referred to in the text of the report. Do not just throw a figure into the report without referring to it. Figures should be used to augment the textual matter.
- Hand-drawn figures and diagrams are not acceptable!
- Turn off the grid in the Quartus schematics when making screenshots!
- Break large block diagrams into multiple smaller ones when inserting them into the report.
- Do not include long vhdl descriptions into the report. Instead, include the .vhd files in your report submission zip file.

Don't wait until the last day to start writing the report. Start writing it early on in the lab 5 period. Remember, it is due on the last day of classes, and not one week later!

The report should be done in html or pdf (preferred), or in Microsoft Word, and uploaded to the myCourses site using the lab #5 assignment submission icon.

The presentation of the report (grammar, spelling, and clarity of the diagrams) will also be graded. *Professor Clark will grade the final reports.*

Make sure that you have uploaded ***all*** of the design files (e.g. .bdf and .vhd files) used in your project. Also include the device programming file (.sof or .pof file) so that the TA can download your design to an Altera board.

The report is due at 17:00 on the last day of classes. Late submissions will be accepted, but will be assessed a penalty of *1 mark per day*, (out of a possible maximum of 10). No submissions will be accepted after that date.



Grade Sheet for Lab #5

Winter 2017.

Group Number:_____.

Group Member Name:_____.

Student Number:_____.

Group Member Name:_____.

Student Number:_____.

Marks

	1.	State diagram for the Computer player FSM	_____.
	2.	VHDL Description of the Computer player FSM	_____.
	3.	Simulation of the Computer player FSM	_____.
	4.	State diagram for the system controller	_____.
	5.	Demonstration of system reset (game begin)	_____.
	6.	Demonstration of display of required items	_____.
	7.	Detection of invalid/losing play	_____.
	8.	Demonstration of correct computer play	_____.
	9.	Detection of end-of-game and determination of winner	_____.
			TA Signatures

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.