Example VHDL to Schematic Capture

If you are having difficulty with the simulation of a schematic capture designed circuit. You can describe the circuit using VHDL and then obtain the schematic and simulate the circuit using Quartus environment.

The advantage of writing the VHDL code is that you are explicitly defining the behaviour and the simulation uses the VHDL code to perform the behavioural simulation.

For example suppose you were defining 4-bit XOR in VHDL

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity example_ex_or is
    port ( a,b : in std_logic_vector (3 downto 0);
    f: out std_logic_vector (3 downto 0));
end example_ex_or;
architecture rtl of example_ex_or is

begin
    f<=a xor b;
end rtl;
```

Figure 1: VHDL description of 4-bit XOR

This can be compiled and the netlist generated for this circuit will be used by the simulator.

If you wanted to view the circuit diagram you could use the menu choice "tool➔ netlist viewer➔rtl viewer "

This will draw the circuit (which should look the same as what you would make using schematic capture for a simple circuit such as XOR). The result is shown below.

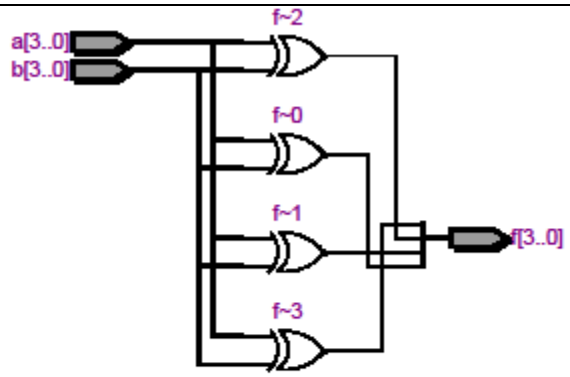

Figure 2: RTL viewer circuit